REPUBLIC OF TURKEY
YILDIZ TECHNICAL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

INVESTIGATION OF MOSFET AGING MODELING ON AN ANALOG CIRCUIT DESIGN

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MSc. THESIS
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İSTANBUL, 2017

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This work was partially supported by University of Diyala, Iraq, and by Yildiz Technical University, Turkey.

ACKNOWLEDGEMENTS

Firstly, praise is to Allah who helped me and gave me the strength and courage to accomplish this work.

I would like to express my deep gratitude to my supervisor, assistant professor Dr. Revna ACAR VURAL, for her sage guidance, advice, and encouragement support throughout this research. She has always made sure she was available for discussion and sharing her valuable knowledge with me and has always been willing to help me overcome all the obstacles encountered during this research. She gave me the freedom to explore the research interests on my study field, and she gave me advice at any time when I need it. I can never thank her enough for the efforts during the scientific supervision in working, correcting and improving my technical writing, and accomplishing this work. I really enjoy and I benefited a lot from the past years of her supervision.

I would like to offer my special thanks to professors of my committee members for taking time out of their busy schedules and accepting to review my work and give their invaluable feedback and comments. I thank all my friends who have stayed with me during the course of this research. I am extremely thankful to all the generous academic staff in the Department of electronics and communications engineering at Yildiz Technical University who provided me with such a wonderful academic atmosphere and who brought up the researcher in me.

Finally, I would like to express my great love, respect and appreciation to the symbol of tender and my role models in life, my father Prof. Dr. Khaleel Ibrahim (may Allah have mercy on him) and my mother (may Allah protect her), for their faithful love, unwavering support, advice, and encouragement throughout my life. They sacrificed everything to support me and my brother and sisters to finish our studies. I could have never become the person that I am today without them.

Last but not least, I would also like to extend my appreciation and gratitude to my wife, who is my soul twin and my way companion in the life, and my children, who are my life flowers and fruit of my happiness, for their encouragement and unwavering support to me and their confidence in me from the beginning.

November, 2016

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LIST OF SYMBOLS

A_v	Voltage gain
$A_{v,cm}$	Common-mode voltage gain
β_1	Transconductance parameter of transistor M1 in the saturation region
C_{ox}	Oxide capacitance
C_C	Compensation capacitor
C_L	Capacitance of load capacitor
$E(V_{GS}, V_{DS})$	The strength of the electric field of the dielectrics
ε	Permittivity
$F_{el,ox}$	Oxide electric field
f_t	Unity gain bandwidth frequency
Φ_F	Fermi level from intrinsic Fermi level or Fermi potential
Φ_{MS}	Work function difference between gate material and the semiconductor
g	Quantity models the effect of duty cycle
g_m	Transconductance
γ_n	Body factor for nMOSFET
I_B or I_{sub}	Substrate current which is induced by impact ionization
I_{bias}	Bias current
I_D	Drain current
I_{DS}	Drain-source current
I_G	Gate current
I_{ON}	Drive current
κ	Dielectric constant
K	Boltzmann’s constant
$\grave{K}$	Transconductance parameter of transistor in saturation region
$\grave{K}_n$	Transconductance parameter of nMOSFET in saturation region
$\grave{K}_p$	Transconductance parameter of pMOSFET in saturation region
L	Channel length
L_{eff}	Effective channel length
λ	Channel length modulation parameter
λ_n	Channel length modulation parameter of nMOSFET
λ_P	Channel length modulation parameter of pMOSFET
μ_{eff}	Effective channel carrier mobility
μ_0	Low field surface mobility
p_2	The undesired non-dominant or the output pole
P_{diss}	Power dissipation
Q_{deg}	Generated electrical charge in the oxide layer
T	Temperature

t	Time
θ	Mobility degradation coefficient
t_{ox}	Oxide or insulator thickness
T_S	Settling time
V	Voltage
V_b	Bulk or substrate voltage
V_{BS}	Bulk or substrate-source voltage
V_d	Drain voltage
V_{DD}	Positive power supply voltage
V_{DS}	Drain-source voltage
$V_{DS,sat}$	Saturation drain-source voltage
$V_{DS5(sat)}$	Drain-source saturation voltage of the transistor M5
V_{FB}	Flat-band voltage
V_g	Gate voltage
V_{GS}	Gate-source voltage
$V_{in(max)}$	Positive input common-mode range voltage
$V_{in(min)}$	Negative input common-mode range voltage
V_{OS}	Input-offset voltage
V_s	Source voltage
V_{SG}	Source-gate voltage
V_{SS}	Negative power supply voltage
V_{th}	Threshold voltage
$V_{th,n}$	Threshold voltage of nMOSFET
$V_{th,p}$	Threshold voltage of pMOSFET
ΔV_{th}	Aging-induced threshold voltage shift
$\Delta V_{th,AC}$	N/PBTI-induced threshold voltage shift under AC stress
$\Delta V_{th,IT}$	N/PBTI-induced threshold voltage shift related to the interface traps
$\Delta V_{th,OT}$	N/PBTI-induced threshold voltage shift related to the traps deep inside the dielectric layer
$\Delta V_{th,HCI}$	HCI-induced threshold voltage shift
W	Channel width
W_{eff}	Effective channel width
W/L	Aspect ratio
z_1	Right half plane (RHP) zero

LIST OF ABBREVIATIONS

API	Application Program Interface
BTI	Bias Temperature Instability
CMOS	Complementary Metal-Oxide-Semiconductor
CHCI	Conductive Hot Carrier Injection
CMI	Custom Common Model Interface
CCVS	Current-Controlled Voltage Source
CCCS	Current-Controlled Current Source
CMRR	Common Mode Rejection Ration
EDM	Energy Driven Model
GBW	Gain Bandwidth or Unity Gain Bandwidth
HCI	Hot Carrier Injection
ICs	Integrated Circuits
ICMR	Input Common-Mode Range
LEM	Lucky Electron Model
LDD	Lightly Doped Drain
LSHA	Local Self-Heating Activated
LDSH	Localized Drain Self-Heating
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOSRA	MOSFET Model Reliability Analysis
NBTI	Negative Bias Temperature Instability
NCHI	Non-Conductive Hot Carrier Injection
Op-Amp	Operational Amplifier
OTA	Operational Transconductance Amplifier
PBTI	Positive Bias Temperature Instability
PM	Phase Margin
$PSRR$	Power-Supply Rejection Ratio
$PSRR^+$	Positive Power-Supply Rejection Ratio
$PSRR^-$	Negative Power-Supply Rejection Ratio
RD	Reaction-Diffusion
RTN	Random Telegraph Noise
RTS	Random Telegraph Signal
RHP	Right Half Plane
SRAM	Static Random Access Memory
SOT	Switching Oxide Traps
SR	Slew Rate

SR^+	Positive Slew Rate
SR^-	Negative Slew Rate
TDDB	Time Dependent Dielectric Breakdown
VLSI	Very Large-Scale Integration
VCVS	Voltage-Controlled Voltage Source
VCCS	Voltage-Controlled Current Source

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ABSTRACT

INVESTIGATION OF MOSFET AGING MODELING ON AN ANALOG CIRCUIT DESIGN

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This work focuses on the study of one of the important reliability issues of the analog circuits in the nano-MOSFET transistors era emerging from the main aging mechanisms such as negative bias temperature instability (NBTI). In addition, an investigation and a detailed analysis are achieved; in particular, about the impact of the NBTI-induced threshold voltage V_{th} degradation effect of pMOSFET transistors on the performance specifications of the unbuffered two-stage CMOS operational amplifier (Op-Amp) which is designed using 90 nm CMOS technology parameters. MOSFET model reliability analysis (MOSRA) in HSPICE is used for analyzing the NBTI-induced threshold voltage V_{th} degradation of a single pMOSFET transistor and its impacts are analyzed on the unbuffered two-stage CMOS Op-Amp circuit. Using this procedure, a single pMOSFET transistor is simulated and its NBTI-induced threshold voltage V_{th} is investigated and analyzed, in addition, the unbuffered two-stage CMOS Op-Amp circuit is also simulated and the degradation of its performance specifications resulting from NBTI-induced threshold voltage V_{th} of each pMOSFET in the circuit is investigated and analyzed. It has been shown that the NBTI-induced threshold voltage V_{th} degradation of the pMOSFET transistor operating in the linear region is mainly dependent on the applied gate-source stress voltage value V_{GS}. Also, it has been shown that the degradations in the performance specifications of the unbuffered two-stage CMOS Op-Amp circuit are rather strongly dependent on its open-loop and unity-gain modes and on its applications than the absolute dependence on the threshold voltage V_{th} degradation of each pMOSFET transistor in the circuit resulting from the impact of NBTI aging effect.

Keywords: Reliability, analog circuit, negative bias temperature instability, hot carrier injection, threshold voltage degradation, performance degradation, *MOS* aging

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ÖZET

ANALOG DEVRE TASARIMINDA MOSFET YAŞLANMA MODELİNİN ARAŞTIRILMASI

Hayder Khaleel AL-Qaysi

Elektronik ve Haberleşme Mühendisliği Bölümü
Yüksek Lisans Tezi

Tez Danışmanı: Yrd. Doç. Dr. Revna ACAR VURAL

Bu tezde, nano-MOSFET transistörler çağında, “negatif kutuplama ısı kararsızlığı” gibi (NBTI)’ın temel yaşlanma mekanizmasından dolayı ortaya çıkan analog devrelerin önemli güvenirlilik sorunlarından biri ele alınmıştır. Ayrıca, 90 nano metre CMOS teknolojisi kullanılarak tasarlanan 2 katlı CMOS işlemsel kuvvetlendiricinin (Op-Amp) performans özellikleri ile ilgili, özellikle de pMOSFET transistörlerin NBTI-dan kaynaklanan eşik gerilimi (V_{th}) düşüşünün etkisi hakkında, araştırma ve detaylı bir analiz yapılmıştır. Tek bir pMOSFET transistörün NBTI-dan kaynaklanan eşik gerilimi (V_{th}) düşüşünün analizi için HSPICE da MOSFET model güvenirliliği analizi (MOSRA) kullanılmış ve 2 katlı CMOS Op-Amp lar ile ilgili tek bir pMOSFET transistörün NBTI-dan kaynaklanan eşik gerilimi (V_{th}) düşüşünün etkileri analiz edilmiştir. Bu prosedürü kullanarak, tek bir pMOSFET transistörünün simülasyonu yapılmış, NBTI dan kaynaklanan eşik geriliminin azalması araştırılmış ve analiz edilmiştir. Ayrıca arabelleksiz 2 katlı CMOS Op-Amp devresinin de simülasyonu yapılmış ve devrede kullanılan her bir pMOSFET’in NBTI’dan kaynaklanan eşik gerilimi (V_{th}) azalmasının sebep olduğu performans düşüşünün araştırması ve analizi yapılmıştır. Sonuçlar göstermektedir ki; doğrusal bölgede çalışan bir pMOSFET transistörün NBTI nedeniyle eşik geriliminin azalması, aslında uygulanan kapı-kaynak stress geriliminin değerinden (V_{GS}) kaynaklanmaktadır. Ayrıca, bu tezde, 2 katlı CMOS Op-Amp devresinin performansındaki düşüşünün, devrede kullanılan her bir pMOSFET’in NBTI yaşlanmasından kaynaklanan eşik gerilimindeki azalmadan ziyade, arabelleksiz 2 katlı CMOS Op-Amp’ın açık döngüsüne, birim kazanç moduna ve onun uygulamalarına daha çok bağlı olduğu kanıtlanmıştır.

Anahtar Kelimeler: Güvenirlilik, analog devre, negatif kutuplama ısı kararsızlığı, sıcak taşıyıcı enjeksiyonu, eşik gerilimindeki azalma, performans düşüşü, *MOS* devre elemanının yaşlanması

CHAPTER 1

INTRODUCTION

1.1 Literature Review

Since the 1960s, CMOS (Complementary Metal-Oxide-Semiconductor) technologies have been aggressively shrunk and have reached a few tens of nanometers in sizes. The consistent technology scaling of MOS (Metal-Oxide-Semiconductor) device's channel length L, channel width W, oxide thickness t_{ox}, and power supply voltage V_{DD} leads to the maintenance of essential MOS device characteristic, development of MOS device performance and reduction in the area and power consumed by MOS device. Due to these distinctive attributes, CMOS devices have form the main driving force in the present advanced microelectronics industry, ICs (Integrated Circuits), and the information technologies.

However, with the entering of CMOS technology scaling into 0.1 um regime, CMOS devices are facing a multiple of performance and reliability problems which have been turning into a source of increasing concern for ICs designers and manufacturing companies. Especially, CMOS devices' accelerating failure mechanisms in nanometer regime have become more severe than it was before because of the increasing power supply voltage and higher electric fields in the dielectric layer of CMOS devices. In addition, the existence of billions of smaller and highly integrated MOS devices which operate at slightly lower power supply voltages in the nano-scale ICs increases on-chip operation temperature which results in further devices wear-out. Consequently, the critical challenge for ICs designers and manufacturing companies is maintaining the ICs reliability, which should be processed in both design and test phases.

Gordon E. Moore in 1965 predicted the technology scaling theory that the number of transistors that can be fabricated on integrated circuits will double approximately every-

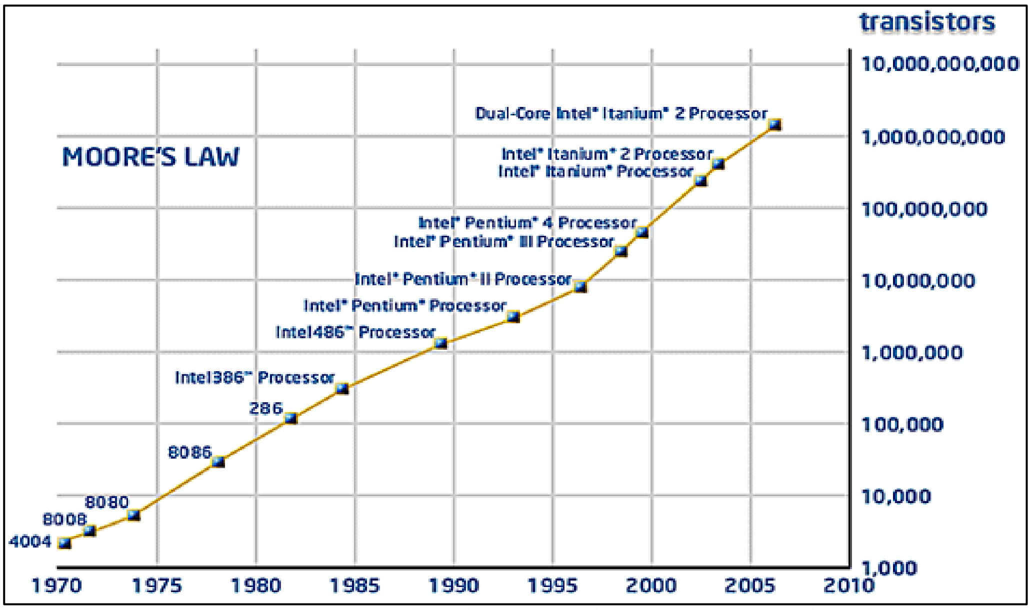


Figure 1.1 Moore's Law [2]

two years [1], which has been known since that time as Moore's Law as shown in Figure 1.1 [2]. Over the past five decades, Moore's Law has been followed well since that time by semiconductor manufacturing companies to scale-down the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices increasingly which results in the reduction of the cost, increasing the performance, and lowering the power consumption per MOSFET device of the IC components. Consequently, all of these downscaled MOS device features have made it the most dominant transistor types in IC technologies. The presently produced transistors are 20 times faster and occupy less than 1% of the area of those built 20 years ago [3]. The electronics industry is presently the largest industry in terms of output and additionally employment in many nations. The significance of electronics in the economic, social, and even political development in all over the world will undoubtedly keep on ascending [4]. As a result, the semiconductor manufacturing companies are increasingly looking to minimize the sizes of MOS devices more and more in order to obtain optimal improvement of area, power, and performance of electronics. But often the reliability of the MOS devices is the victim when trying to access these desired features resulting from the downscaling of MOS devices as technology advances. This is what makes the effect of aging is a growing concern in the reliability of modern CMOS devices-based circuits.

There has been significant progress in developing new methods for modeling and diagnosing the reliability at the individual MOSFET transistors' levels, but much less of work to the development of these models for analysis and optimization of reliability at -

the larger circuits' levels [5].

When the integrated circuit works, the electrical characteristics of MOSFET devices begin to degrade with time such as increasing the threshold voltage in magnitude and decreasing the drain current which is called MOSFET device aging and as a result of this individual MOSFET device degradation, the performance of the circuit becomes progressively worse with time which is called circuit aging. The major physical MOSFET devices aging mechanisms are NBTI (Negative Bias Temperature Instability) which is dominant in pMOS devices, PBTI (Positive Bias Temperature Instability) which is dominant in nMOS devices, and HCI (Hot Carrier Injection) which is dominant in both nMOS and pMOS devices. These aging mechanisms have been known to impact the MOSFET devices since the 1970s but have become more prominent in the nanometers regime because of changes in processing and scaling technologies which introduced over the last three decades in order to improve the performances of MOSFET devices, analog and digital circuits [6].

The introduction of new materials like high-κ materials into the metal gate stacks in advanced MOSFETs processing reduces of gate leakage current but generates device aging mechanisms like PBTI which was not present in classical SiO_2 or $SiON$ based gate of nMOS devices technologies. As BTI (Bias Temperature Instability) and HCI are among various aging effects represent major reliability concerns with continuous MOS devices scaling and limits the lifetime of the circuit, it is very important during the circuit design phase to understand, simulate, and alleviate their impact. The effect of aging at the MOSFET device level is the increase of the threshold voltage V_{th} (shown in Figure 1.2), as well as the channel carrier mobility affected due to the increased Coulomb scattering and the increase in the sub-threshold voltage slope [7].

The impact of MOSFET device aging effects at the level of analog and digital circuits performances degradation were investigated primitively in the past and considered as a secondary source of concern for the reliability of the circuit being responsible for a slight shift in device parameters which were avoided or alleviated its impact by the device operation within the safe margins. MOSFET device aging effects have received a special case of increasing interest at the time being lead to several investigations to study its impact at the level of analog and digital circuits. Effect of aging in digital circuits appear mainly through an increase in the time delay of logic gate switching, which results in the degradation of data stability over time. The increased propagation -

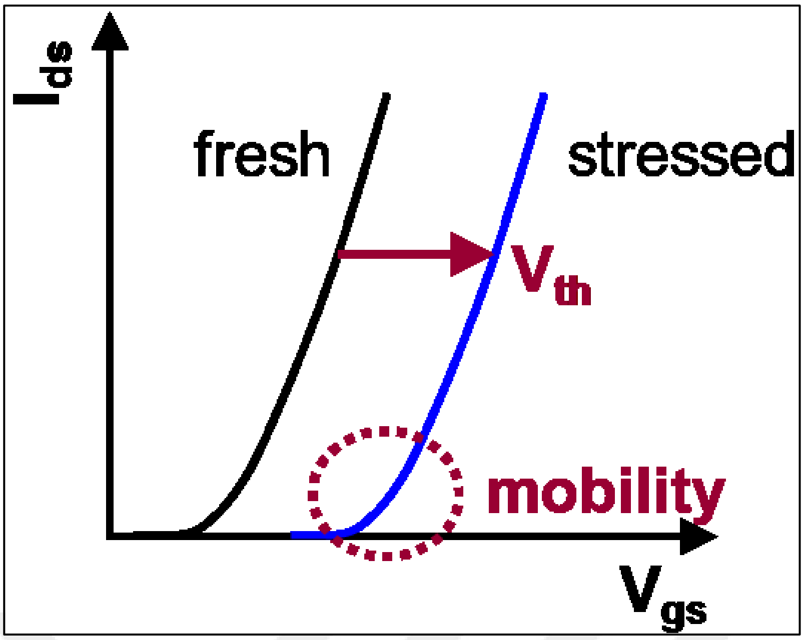


Figure 1.2 Impact on threshold voltage and carrier mobility with aging due to aging [7]

delay can cause a degradation of circuit timing in the critical data paths over time which causes circuit failure [8, 9, 10]. Similarly, the investigation of aging on SRAM (Static Random Access Memory) cell arrays revealed that degradation of MOS devices affects various performance metrics like the function of SRAM caches which resulting from the increasing delay time in the data paths, noise margin, power dissipation, data retention voltages, read/write failure, and operating frequency reduction (speed reduction) [11].

The complexity of analog processing technologies imposed by the application requirements of analog and mixed-signal circuits like high speed, low noise, low power, high precision, and high voltage and consequently the impacts of MOS devices aging on the analog circuits' performances are more complex than it is in digital circuits [12]. With the inclusion of high-κ materials in advanced CMOS devices technologies, CMOS device aging is found to be more severe in high-κ based CMOS technologies because of larger oxide electric fields compared to classical SiO_2 or $SiON$ based CMOS technologies [13].

A most important limitation for analog circuits' reliability is the effect of aging-induced mismatch of MOSFET devices pairs' characteristics on matched MOSFET devices pairs' characteristics due to the degradation of MOSFET devices with time [14, 15]. Asymmetric stress condition induces MOSFET device pair mismatches and thus shifts the output characteristics of the analog circuits [15]. The investigations made by Martin-

Martinez et al on the three different topologies of a CMOS differential amplifier circuit based on nMOSFET device differential input pair showed that the aging-induced MOSFET devices degradation impacts the gain and GBW (Gain Bandwidth) of the amplifier depending on circuit topology and they proposed that the reliability of the circuit can be improved depending on the correct selection of the circuit topology [16]. The basic investigation of Thewes et al about the various aging effects on a pMOSFET device differential input pair of a two-stage Op-Amp (Operational Amplifier) circuit under different analog circuit operation states showed that the degradation of circuit performance metrics like gain, linearity, noise, and input offset voltage are again due to aging effects. Also, BTI degradation effect which is caused by a high oxide electric field is expected to emerge as one of the most important challenges for robust circuit design in the future [17].

Furthermore, the investigations of Jha et al about the effects of MOS devices degradation due to NBTI on various analog circuits levels like three different current mirror topologies, two-stage CMOS Op-Amp, and comparator showed that the degradation of circuit performance metrics rather strongly depend on the analog circuit topology and its application than the absolute degradation of individual MOS devices. The study showed very big differences in the output currents shifts of the three different current mirror circuits. The investigations on two-stage CMOS Op-Amp circuit showed that the transconductance g_m and the DC biasing currents of the Op-Amp circuit stay stable because of using stable biasing current circuit and thus the impact of NBTI-induced threshold voltage V_{th} degradation on the DC gain and GBW of two-stage Op-Amp are small. The investigation also showed a large variations in the input offset voltage because of NBTI impact on V_{th} degradation when using a two-stage Op-Amp circuit as a comparator circuit in the open-loop configuration [18].

1.2 Objective of the Thesis

The main objective of this thesis is to study and investigate the most significant reliability issue in analog circuits which is NBTI aging effect and analyzing the NBTI-induced pMOSFET devices aging impacts on the unbuffered two-stage CMOS OP-Amp circuit performance metrics. Our contribution to address this significant reliability issue is the analysis of NBTI-induced aging degradation in terms of gain, gain bandwidth, slew rate, phase margin, power consumption, and input-offset voltage etc. of the unbuffered two-stage CMOS Op-Amp circuit by using HSPICE MOSRA and expansion of findings to develop more robust analog circuits toward the effects of aging in the future.

The thesis organization is as follows:

Chapter 2 presents the background of the most significant aging mechanisms which are BTI and HCI effects as well as the significance of their study.

Chapter 3 demonstrates the methodology to measure the amount of the degradation in the threshold voltage V_{th} resulting from aging effects at the levels of a single MOSFET transistor and CMOS-based circuits using MOSRA in HSPICE.

Chapter 4 investigates and analyzes the degradation in the threshold voltage V_{th} of a single pMOSFET transistor resulting from NBTI aging effect under various gate-source stress voltage V_{GS} values.

Chapter 5 investigates and analyzes the impact of the degradation in each pMOSFET transistor threshold voltage V_{th} resulting from NBTI aging effect on the performance specifications of the designed unbuffered two-stage CMOS operational amplifier circuit.

Chapter 6 concludes this work, discusses the results, and suggests the future work of this thesis.

1.3 Hypothesis

In advanced CMOS technology nodes, Nano-CMOS devices' accelerating failure mechanisms have become more severe than it was before. Consequently, the critical challenge for ICs designers and manufacturing companies is maintaining the ICs reliability. In this thesis, we will study and analysis the major issues of analog circuit reliability resulting from a serious NBTI aging mechanism. Then, we will describe a methodology to measure the amount of aging-induced degradation at the MOSFET transistor level and circuit level by using of MOSRA in HSPICE. Using this procedure, we will investigate and analysis the amount of NBTI-induced V_{th} degradation at the level of a single pMOSFET transistor and its impacts at the level of the unbuffered two-stage CMOS Op-Amp circuit performance specifications, as an example of an analog circuit, based on HSPICE MOSRA simulation results. Our findings will help to develop more robust analog circuits toward the effects of aging in the future.

CHAPTER 2

AGING MECHANISMS: BTI AND HCI

2.1 CMOS Device Wear-out

Integrated CMOS devices experience the effects of wear-out because of their utilization in electronic devices. The existence of billions of MOSFET transistors on a single die in modern ICs requests scaling down MOS insulator thickness to a few nanometers where the electric fields across the oxide reach MV/cm even though the MOS device operating in the 1V regime. Consequently, time-dependent insulators' properties wear-out occurs which inducing changes in the device characteristics or in worst case to its breakdown. Since advanced CMOS processing moves to the *non-constant field* scaling approach and inclusion of novel high-κ materials into the MOS gate stack, the wear-out worsens for every technology step [19].

Aging mechanisms can be divided in two categories: *non-destructive* aging mechanisms like bias temperature instability (BTI) and hot carrier injection (HCI) effects which leading to drift of MOS device characteristics, but not to an instantaneous failure of MOSFET transistor, and *destructive* aging mechanisms like TDDB (Time Dependent Dielectric Breakdown) [20, 21] leading to a permanent failure of the transistor.

Our investigation on MOSFET aging modeling on an analog circuit design addresses the NBTI aging mechanisms; because they can change circuit performance during the lifetime operation. Also, from the system standpoint drifts in the analog circuit's performance specifications can lead to failure of the overall system.

2.2 Impact on CMOS Devices Parameters

BTI and HCI aging mechanisms involved in insulator wear-out because of the inclusion of charges into the insulator region. Consequently, the MOSFET device characteristics change in many ways. The *threshold voltage* V_{th} of a typical nMOSFET with zero bulk-source voltage $V_{BS} = 0$ as shown in Figure 2.1 is defined as the inversion mode gate voltage where electron (minority carrier) density in the inversion region is equal to hole (majority carrier) density of the substrate in thermal equilibrium [19, 22].

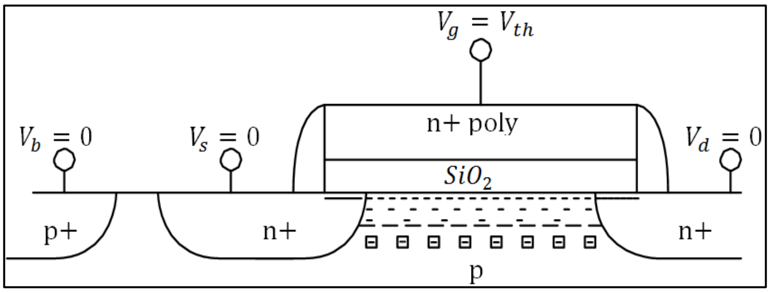


Figure 2.1 Threshold voltage of virgin nMOS device [19]

The threshold voltage, for a uniformly doped substrate is given by

$$V_{th} = V_{FB} + 2\Phi_F + \gamma_n\sqrt{2\Phi_F} \tag{2.1}$$

with V_{FB} the flat-band voltage, Φ_F the Fermi level from intrinsic Fermi level and γ_n the body factor for nMOSFET which is depend on the substrate doping and dielectric constant of the insulator.

A generated charge Q_{deg} in the oxide layer, as shown in Figure 2.2, would shift the flat-band voltage to

$$V_{FB} = \Phi_{MS} - \frac{Q_{deg}}{C_{ox}} \tag{2.2}$$

with Φ_{MS} the work function difference between gate material and the semiconductor and C_{ox} the oxide capacitance. Depending on the amount and polarity of the generated charge, V_{FB} and thus V_{th} is shifted by the amount of

$$\Delta V_{th} = \Delta V_{FB} = -\frac{Q_{deg}}{C_{ox}} \tag{2.3}$$

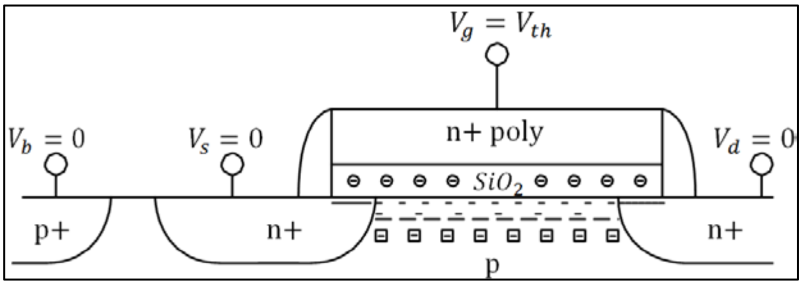


Figure 2.2 Threshold voltage of degraded nMOS device [19]

Moreover, the field-dependent effective channel carrier mobility μ_{eff} is also affected by induced oxide charges. The relationship between μ_{eff} and device operation condition is given by

$$\mu_{eff} = \frac{\mu_0}{1 + \theta\,(V_{GS} - V_{th,n})} \tag{2.4}$$

with μ_0 the low field surface mobility, θ the mobility degradation coefficient and V_{GS} the gate-source voltage. Equation (2.4) shows a direct relation of μ_{eff} to a drift in threshold voltage [23]. In addition, the oxide charges at the silicon-silicon dioxide interface which acting as Coulomb scattering centers can impact μ_0 and θ [24]. The drift of fundamental MOSFET parameters V_{th} and μ_0 resulting in the degradation of other device parameters such as *drain current* I_D and *transconductance* g_m. These obtained general impacts of a typical nMOS device wear-out are also valid for the pMOS device.

2.3 Bias Temperature Instability (BTI)

There exist two types of BTI degradation: negative bias temperature instability (NBTI) for pMOSFET and positive bias temperature instability (PBTI) for nMOSFET transistors. Both of these effects derived from the typical inversion mode operation of CMOS devices and their impact are increased with a rise in temperature leading to the degradation of transistors characteristic [19]. The oxide electric field-dependent BTI degradation given by equation (2.5) for strong inversion,

$$F_{el,ox} = \frac{V_{GS} - V_{FB} - 2\Phi_F}{t_{ox}} \tag{2.5}$$

with V_{FB} the flat-band voltage, Φ_F the Fermi potential and t_{ox} the insulator thickness. As illustrated by equation (2.5), the basic parameters for the BTI degradation are V_{GS} and t_{ox}.

In the late 1960s with the beginnings of MOSFET development, the BTI effects, particularly the NBTI effect in pMOSFET transistors, were observed [25] but the NBTI impact on the buried-channel n^+ poly gate pMOS devices was small, so it was not concerned as a main reliability issue. NBTI was well controlled because of *the constant field scaling* in CMOS technology development (i.e. a similar scaling of V_{GS} and t_{ox}). The NBTI impact enhanced as one major degradation mechanism during the turn out to surface-channel p^+ poly gate pMOS devices to counter the short-channel effects inherent in the downscaling process and with the introduction of *non-constant field* *scaling* in sub-0.1um CMOS technologies (i.e. keeping or slightly decreasing V_{GS} but scaling t_{ox} in the traditional way) [19]. PBTI for SiO_2 based nMOSFET transistors was negligible, but arose with using of high-κ materials in advanced CMOS technologies [26].

2.3.1 NBTI in pMOS Devices

The typical pMOS device in inversion mode NBTI stress condition and the resulting oxide degradation is shown in Figure 2.3; the pMOSFET transistor is in the linear region with zero voltage drops over the channel. pMOSFET gate is subjected to a high negative bias $V_{GS} = -V_{DD}$ with the other terminals grounded inducing an inversion layer in the n-type substrate and accumulation layer in the source and drain overlap regions. Under high oxide electric field $F_{el,ox}$ in the insulator which is given by equation 2.5, the oxide degrades because of charge trapping. In addition, the NBTI degradation takes place for a pMOSFET operates in saturation region as shown in Figure 2.4, but this degradation will be smaller because of the decreasing electric field from the source to the drain region [24].

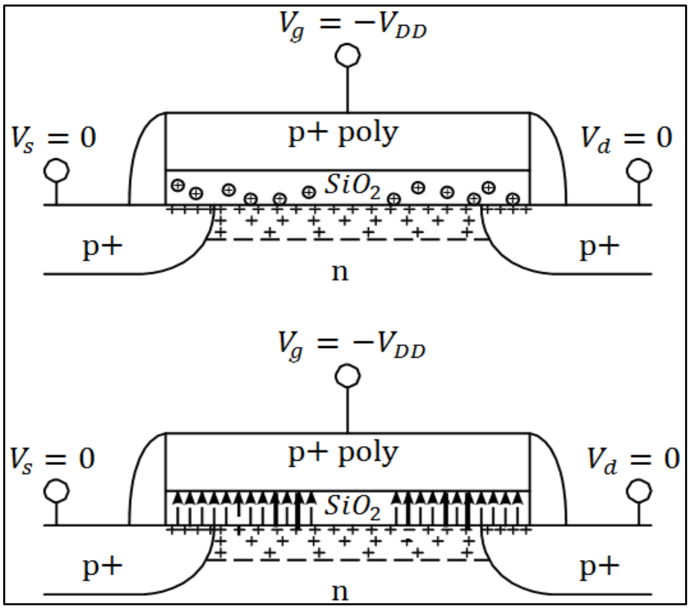


Figure 2.3 pMOS in linear operation: NBTI stress generated defects and arising electric field under NBTI stress [19]

Because of NBTI and its associated mechanisms are sensitive to different CMOS processing and included gate stacks materials, there exist a lot of NBTI degradations and effect explanations in the literature. The general consensuses on NBTI mechanisms are the generation of *interface states* (or *interface traps*) at the substrate-oxide interface-

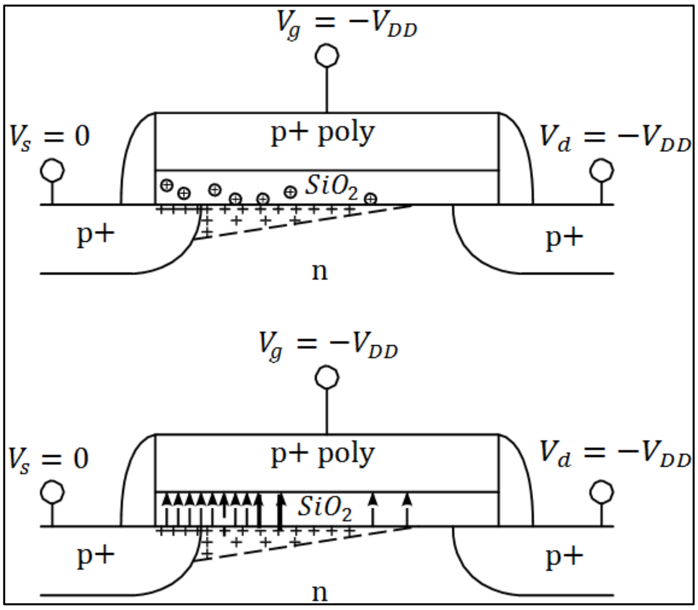


Figure 2.4 pMOS in saturation operation: NBTI stress generated defects and arising electric field under NBTI stress [19]

and the electrical activation of pre-existing defects or generation of new defects in the insulator during pMOS device operation [27]. The creation of an interface state is made by the release of hydrogen saturating an open Si bond at the SiO_2-Si interface. The residual *dangling bond* (or *trapping center*) is an electrically active defect which can be occupied by an electron or hole, but for inversion mode pMOSFET it is occupied by hole so it is positively charged [28]. The residual hydrogen diffuses away from the interface into the insulator or poly-Si gate under the influence of the electric field. As this interface trap generation process was believed to be the dominant NBTI contributor, various NBTI models have been proposed, of which the most prevalent RD (Reaction-Diffusion) model for NBTI prediction [29]. This model explained the positive oxide charge is due to trapping of $H^+$from RD process, but recent findings detected that the hole traps (or defects) and the total number of their precursors is pre-existing in the oxide before stress is applied and no signs of newly created defects [30].

NBTI degradation mechanisms were more comprehended during the prolonged investigations on the NBTI *recovery effect* (or the recovery of V_{th} shift ΔV_{th}). Because NBTI degradation will recover once the stress is removed, the measured time delay between stress and degradation measurement is very important because of this undefined time delay in NBTI dataset is also another cause of the deficiency in NBTI comprehension. Recently, many researches were made for measuring degradation during stress to locate the entire amount of participating effects [31, 32, 33, 34]. NBTI degradation was divided into: a recovery and a permanent component. Controversial results from many researches linked the recovery effect to passivation of interface traps [35] or detrapping of holes [32]. In addition, investigations for enhanced recovery under positive gate biasing (or under accumulation mode operation) did not show a distinct recovery root [36, 37]. The ultra-fast V_{th} measurement method to monitor recovery after stress, detected for a small pFETs a step height recovery curve showing the discharge of single defects with various contributions in size of step height, which can be connected to the random locations of the discrete dopants in the channel and single defects in insulator. In a large pFETs, this single defect recovery is not seen because of the mixing of all the enormous number of defects and the small impact of each single defect recovery to the total device V_{th}, leading to log (t) NBTI recovery behavior, which is inconsistent with the RD model [38]. Defect relaxation effect was connected to the model of *low frequency noise/flicker noise* or its appearance as RTN or RTS (Random Telegraph Noise or Signal) and expanded to the BTI stress and recovery timing range with individual capture and emission time constants for each defect [39, 40, 38]. With a model based on SOT (Switching Oxide Traps) from Grasser et al, it was shown that a thermally activated capture and emission of holes and electrons in oxide traps causes BTI [30, 41]. Capture and emission time constants are widely distributed from nanosecond to months or even longer. Investigations showed that metastable states of these defects present an additional noise portion and devices scaling down to nanometer dimensions can lead to significant induced variations because of high defect step height sizes of a handful of defects per device.

NBTI degradation changes with changing the insulator materials from SiO_2 to $SiON$ or high-κ materials gate stacks. For minimum NBTI degradation in $SiON$ devices, nitrogen should be located near the gate-insulator interface rather than the insulator-substrate interface [28]. NBTI degradations in high-κ materials gate stacks compared to NBTI degradations in SiO_2 and $SiON$ were similar [42]. Fernandez et al showed that NBTI highly depends on duty cycle and the NBTI-induced V_{th} shifts under AC stress are independent of frequency in the entire range of 1 Hz − 2 GHz [43], which is consistent with switching oxide traps model from Grasser et al. From recent discoveries, Kaczer et al proposed the usage of high-mobility substrates, like buried channel $SiGe$ pMOSFETs to guarantee restricted NBTI degradation in pMOS devices in future CMOS technology nodes [27].

2.3.2 PBTI in nMOS Devices

PBTI in nMOS devices also occurs in inversion mode operation under positive gate bias. PBTI degradation in SiO_2 and $SiON$ technologies were very small and negligible, but its effects significantly increase in high-κ materials gate stack technologies. The inversion mode PBTI stress condition and the resulting insulator degradation in the linear region operation for a typical high-κ metal gate nMOS device is shown in Figure 2.5. In this case the oxide degradation happens in the high-κ part of the gate stack, which is opposite to classical NBTI in pMOSFETs [26].

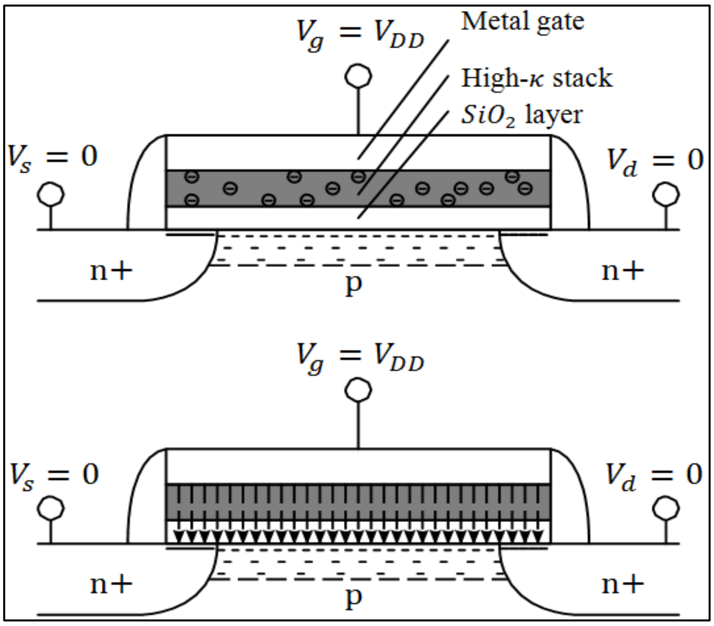


Figure 2.5 High-κ nMOS in linear operation: PBTI stress generated defects and arising electric field under PBTI stress [19]

PBTI degradation in nMOSFET is situated at a specific remoteness from the inverted channel region because of the existence of SiO_2 layer in-between the substrate-insulator interface, thus PBTI fundamentally affecting the threshold voltage V_{th} with nearly no effect on channel carrier mobility μ_0 [44].

As shown in Figure 2.6, nMOSFET operation in saturation region shows PBTI degradation concentration near the source resulting in a decreased PBTI degradation compared to the linear region operation which is comparable to what occurred in NBTI degradation in pMOSFET operation in the saturation region.

Because of PBTI in the high-κ gate stacks nMOSFET processes is a new kind of degradation mechanism and NBTI in pMOSFET is among the most discussed and most controversial topics in modern reliability research, most BTI investigations focused on -

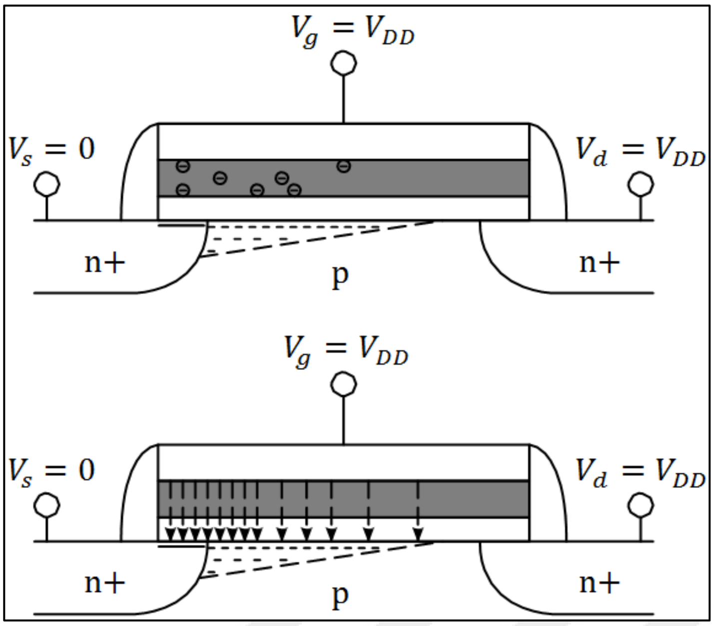


Figure 2.6 High-κ nMOS in saturation operation: PBTI stress generated defects and arising electric field under PBTI stress [19]

NBTI in order to a more comprehension of NBTI in pMOSFET [19]. However, there is a general agreement about PBTI degradation in nMOSFET is because of charge trapping (or electron trapping) in the high-κ layer [45, 46, 47, 26]. Recent findings for HfO_2 based high-κ gate stack linked the key parts of PBTI degradation to electron trapping at oxygen vacancies in the HfO_2 layer [27]. The recovery conduct of PBTI in nMOSFET also shows a defect recovery time is widely distributed from sub-microseconds to months which are comparable to the recovery conduct of NBTI in pMOSFET. In addition, the switching oxide traps approach fits well with PBTI degradation recovery behavior and the degradation dependent on AC gate stress [30, 45]. PBTI degradation can be decreased in HfO_2 based high-κ nMOSFET processes by passivating oxygen vacancies through the inclusion of group III elements [48].

2.4 Hot Carrier Injection (HCI)

MOS device types, nMOS and pMOS devices are affected by Hot Carrier injection degradation. The HCI degradation effect is corresponding to the BTI degradation effect, as in BTI insulator wear-out causing by a high vertical oxide electrical field whereas in HCI the lateral electric field causing the degradation. Consequently, HCI degradation emerges for high drain-source voltages V_{DS} with short channel lengths L. The insulator wear-out which results from HCI is an asymmetric phenomenon and concentrated in the drain region, which is unlike to a symmetric insulator wear-out resulting from BTI, thus the modeling of this an asymmetric HCI degradation is more difficult. The *hot carrier* is a carrier that if accelerated under an electric field and gains a kinetic energy higher than the lattice in thermal equilibrium, so it is called *hot* [19]. Hot carriers have enough energy to induce *impact ionization, interface states* generation or even it can surpass the insulator barrier and create *defects* in the oxide or *get trapped*. Consequently, all of these mechanisms produce a degradation of MOSFET parameters such as V_{th}, *drain current* I_D, and different *transconductances* like g_m or g_{ds} [49]. The measurements of hot carrier injection rates are typically made by gate current I_G, or by substrate current I_B (or I_{sub}) which is induced by impact ionization. The essential HCI degradation results from the trapping of only some of these hot carriers. MOSFET when operates in saturation region, the lateral electric field will be high and sufficient to generate hot carriers between drain junction and channel pinch-off and HCI degradation in this operation mode known as CHCI (Conductive Hot Carrier Injection) [19]. The resulting CHCI degradation from nMOSFET operation in saturation region is given in Figure 2.7.

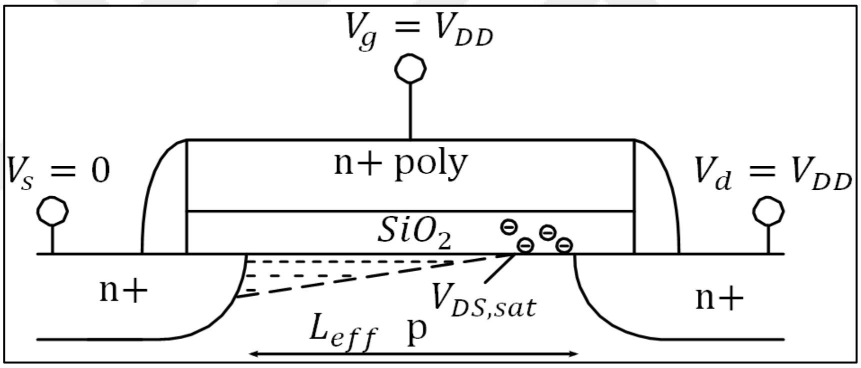


Figure 2.7 nMOS in saturation operation inducing CHCI degradation [19]

The CHCI degradation resulting from lateral electric field is connected to the effective channel length L_{eff} and the voltage difference between the drain side and the channel pinch-off point. Since the lateral electric field depends on the drain-source voltage V_{DS} and the gate-source voltage V_{GS} which both of them define the pinch-off point with $V_{DS,sat} = V_{GS} - V_{th}$, the voltage stress conditions for HCI degradations are more complex than that for BTI [19]. Moreover, the directions of the oxide electric field in the drain region and thus the polarity of defect trapping are controlled by the relationships between the gate-source voltage V_{GS} and the drain-source voltage V_{DS}. Different polarities of charge can be created simultaneously from CHCI degradation and the total CHCI degradation is measured by the dominant effect of generated defect or the combination of effects resulting from all generated defects [19].

In the late 1970s, HCI degradation for nMOSFETs became a main reliability concern and in the 1980s, many investigations were made about HCI degradation for nMOSFET and the commonly used LEM (Lucky Electron Model), which is yet utilized in lots of reliability simulators, was developed [50]. LEM predicts the CHCI degradation correctly for MOS devices sizes scaling up to $0.25um$ whereas it is no longer valid to predict HCI degradations with further down scaling in advanced CMOS technology. For example, the lucky electron model does not predict impact ionization or the damage caused by hot carrier degradation when the drain-source voltage $V_{DS} < 1.3V$ albeit both of them are demonstrated by measurements [19]. The EDM (Energy Driven Model) including further acceleration effects like electron-electron scattering was proposed for understanding hot carrier behavior in the modern technology nodes, particularly for MOSFETs at or below the 180 nm technology node [51]. NCHI (Non-Conductive Hot Carrier Injection) degradation condition is given in Figure 2.8 which arises for a very short channel lengths of a few tens of nanometers between the source and drain junction even for MOSFETs in off-state resulting from the injection of hot carriers in the sub-threshold currents [19].

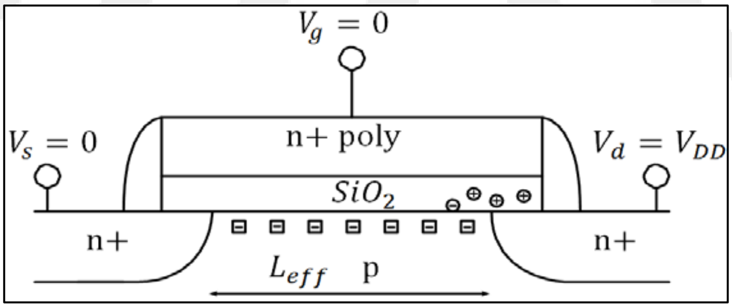


Figure 2.8 nMOS in off-state inducing NCHCI degradation [19]

The LDD (Lightly Doped Drain) technique is given in Figure 2.9 widely used as the HCI counteractive process to reduce the high electric fields in the drain region by the inclusion of a narrow, self-aligned, and low doped n^- regions between the channel-n^+ drain and the channel-n^+ source junctions to spread the high electric field in the drain pinch-off region into the n^- region resulting in an important improvement HCI degradation in nMOS devices, but this LDD structure increases the drain and source resistances because of the additional series resistances resulting from these n^- regions [52].

The simultaneous generation of BTI degradation, especially at high temperatures, represents the most challenging part of HCI characterization and the separation between

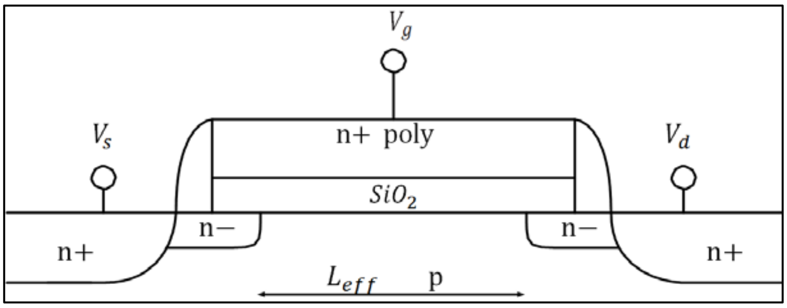


Figure 2.9 Cross-section of a typical LDD nMOSFET [19]

them represent an additional difficulty. The high gate-source voltage V_{GS} shifts CHCI degradations to maximum values and also exacerbates BTI degradations contributions, resulting in more difficulty in CHCI characterization. The recovery effect was also observed in CHCI measurement investigations, but is primarily connected to BTI degradation components [53, 54].

2.4.1 Conductive Hot-Carrier Injection in nMOS Devices

Depending on the gate-source voltage V_{GS} and the induced oxide electric field status in the drain region at high drain-source voltage $V_{DS} = V_{DD}$, CHCI degradation in SiO_2 nMOS devices can be divided into three regions. In each of these three regions, interface states are generated because of the injection of hot carrier with a maximum at gate-source bias voltage equal half of the drain-source voltage $V_{GS} = \frac{1}{2} V_{DS}$ for a long channel devices ($L_{eff} > 0.15\, um$) [19]. The hot carriers' injection leads to a degradation of device characteristics such as the degradation of electrical parameters of the device (i.e. Shifts in threshold voltage ΔV_{th} and drain current I_D etc.) but the HCI degradation interferes with the other device parameter degradation mechanisms like BTI. For low gate-source voltage $V_{GS} \approx V_{th}$ and high drain-source voltage $V_{DS} = V_{DD}$, the oxide electric field in the Drain region causes hole trapping as shown in Figure 2.10 and resulting in the threshold voltage V_{th} to decrease in magnitude and the drive current I_{ON} to increase. In the middle range of gate-source voltage $V_{th} < V_{GS} < V_{DS}$ and high drain-source voltage $V_{DS} = V_{DD}$ hot hole and hot electron injection interferes and partially compensated as shown in Figure 2.11 and resulting in the threshold voltage V_{th} to increase in magnitude and the drive current I_{ON} to decrease. For high gate-source voltage $V_{GS} \approx V_{DS}$ and high drain-source voltage $V_{DS} = V_{DD}$ the injection of hot electrons composes the main part of hot carrier injection as shown in Figure 2.12 and again resulting in the threshold voltage V_{th} to increase in magnitude.

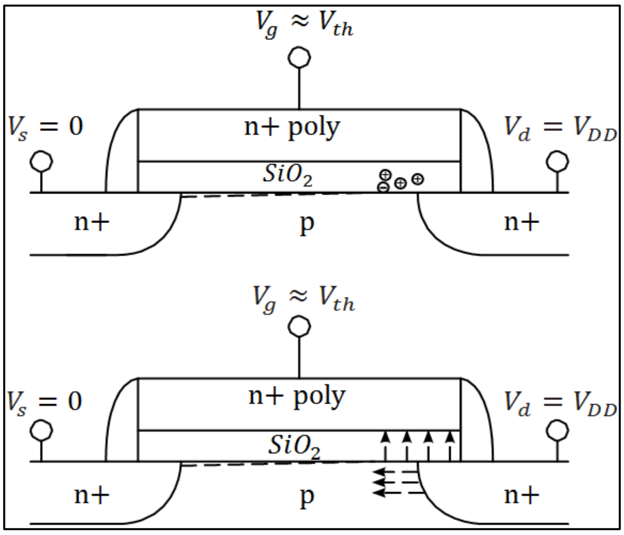


Figure 2.10 nMOSFET CHCI with $V_{GS} \approx V_{th}$ and $V_{DS} = V_{DD}$ [19]

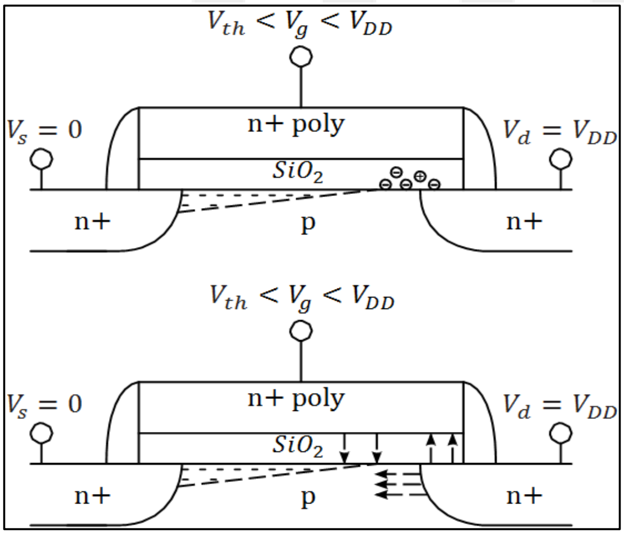


Figure 2.11 nMOSFET CHCI with $V_{th} < V_{GS} < V_{DS}$ and $V_{DS} = V_{DD}$ [19]

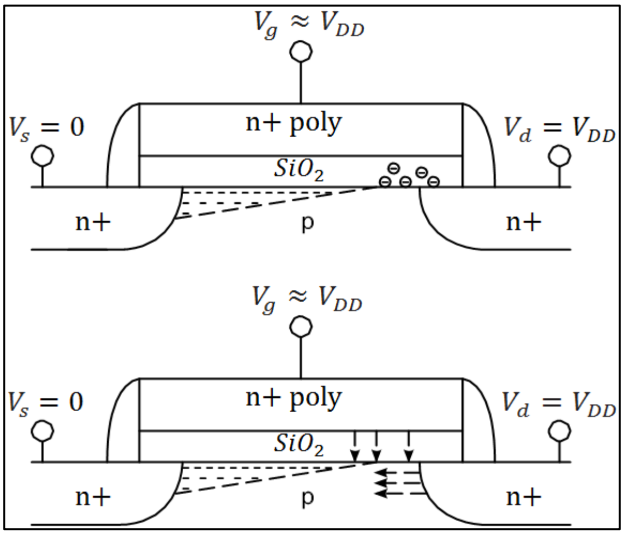


Figure 2.12 nMOSFET CHCI with $V_{GS} = V_{DS}$ and $V_{DS} = V_{DD}$ [19]

The role of hot charge injection falls and the generation of interface state becomes the dominant mechanism of the hot carrier injection degradation in modern CMOS technologies [19]. In addition, as a result of MOSFETs scaling, the maximum interface state generation shifts to drain-source voltage $V_{GS} = V_{DS}$ because of the high V_{GS} shifts of the peak electron concentration near the drain edge from the Si bulk to the $Si/Si02$ interface resulting in an increase in the electron-electron scattering rate as an impact of short channel effects in the short channel devices [55]. The essential CHCI behavior for nMOSFETs is independent of the SiO_2 gate and high-κ gate dielectric materials and this means changing the dielectric material from SiO_2 to high-κ does not change the CHCI behavior in long and short channel nMOS devices, but because of the maximum CHCI shifts to the high $V_{GS} = V_{DD}$ in short channel length devices an additional positive bias temperature instability (PBTI) components emerge, which must be separated from the essential CHCI effect [56].

2.4.2 Conductive Hot-Carrier Injection in pMOS Devices

CHCI degradation condition for classical SiO_2 pMOS devices is very similar to the nMOS devices degradation, but the contributing mechanisms are different and oxide electric fields are only inverse to that in nMOS devices. The maximum generation of interface states reaches at gate-source bias voltage equals of the drain-source voltage $V_{GS} = V_{DS}$ which considered as the essential contributors for CHCI degradation in pMOSFETs. For low gate-source voltage $V_{GS} \approx V_{th}$ and high drain-source voltage $V_{DS} = V_{DD}$, electron trapping is induced in the drain region by filling of pre-existing defects in the oxide and resulting in the threshold voltage V_{th} to decrease in magnitude and the drive current I_{ON} to increase. In modern technologies this is significantly reduced because of in modern CMOS technologies the oxide thickness are very thin and less sensitive for electron trapping. In the high gate-source bias region $V_{GS} < V_{th}$ and high drain-source voltage $V_{DS} = V_{DD}$, the hot holes become the dominant mechanism in CHCI degradation inducing hole trapping in the oxide and the generation of interface states and resulting in the threshold voltage V_{th} to increase in magnitude and the drive current I_{ON} to decrease [19]. Drain junction heating issue emerges as a secondary effect in the devices with further scaling in sub-100nm CMOS technologies because of ballistic phonons effects which resulting from the scattering of the channel carriers with the lattice at the drain region where the transistor channel length is sub-100nm and becomes dominant under DC stress conditions [57]. Under CHCI stress conditions, NBTI degradation in pMOS device enhances because of the effective temperature increases for NBTI resulting in the what's called LSHA (Local Self-Heating Activated) NBTI degradation which resulting from LDSH (Localized Drain Self-Heating) effects at the drain junction region [58, 59].

Recently, the investigation on CHCI for the short channel high-κ gate stack pMOSFET showed that CHCI degradation of high-κ gate stack pMOS devices increases with the gate voltage and become more intense than the CHCI degradation in the ultra-short channel SiO_2 dielectric and poly-Si gate pMOS devices and the worst case CHCI degradation takes place at higher gate-source voltage V_{GS} and drain-source voltage V_{DS} bias condition. Because of this CHCI larger degradation is connected to the lower quality of the interfacial sub-oxide layer which located in-between high-κ dielectric and silicon substrate in the high-κ gate stack pMOS devices [54], the oxide quality must be improved during the continuation of process development in order to decrease the CHCI degradation in high-κ gate stack pMOS devices.

CHAPTER 3

AGING SIMULATION: MOSRA

In advanced CMOS process technology nodes where the device sizes are scaled down to a few nanometer dimensions, the HCI and BTI arises as two of the most critical reliability issues that contribute in MOS devices aging. MOSRA (MOSFET Model Reliability Analysis), which was developed by Synopsys and integrated with HSPICE (an optimizing analog circuit simulator) and CustomSim (a Fast SPICE simulator, which delivers superior verification performance), is mainly used by the circuit designers for circuit-level aging analysis. HSPICE MOSRA analysis currently supports Level 49, Level 53, Level 54, Level 57, Level 62, Level 66, Level 69, Level 70, Level 71, Level 72, Level 73, Level 76 and external CMI (Custom Common Model Interface) MOSFET models [60].

3.1 MOSRA Aging Models

MOSRA can be used to accurately model the BTI and HCI degradation effects, which are the main physical mechanisms responsible for MOSFET device aging. These physical-based aging models in HSPICE and CustomSim can be used successfully to identify in addition to debug reliability issues in design at 45nm and below like BTI and HCI aging issues, consequently offering the ability to build a more reliable integrated circuit (IC). MOSRA BTI and HCI aging models provide accurate and scalable models for both BTI and HCI, especially, they take into account the *partial recovery effect* of BTI degradation that has been taken place, where some of the trapped charges can be de-trapped upon the removal of the stress voltage applied to the gate terminal, which is essential for both NBTI in pMOS and PBTI in nMOS devices. Taking into account the BTI degradation *partial recovery effect* by MOSRA BTI model resulting in the total amount of BTI degradation becomes smaller and this is very important for measuring the degree of circuit aging. A MOSRA aging model is used for translating the amount of electrical stress to the actual MOS device degradation, or “age” because of the MOS device aging is a result of the continuous degradation of MOS device characteristics under the applied electrical stress [61]. Such analysis in the course of design supports in designing circuits which are effective directly after fabrication (fresh or un-aged circuits) also after operating for a number of years (aged circuits). The advantages of aging analysis can result in increasing the age of the circuit by allowing enough safety margins which increase the lifetime of the circuit.

The MOSRA N/PBTI models are represented by consideration of two main physical mechanisms: one related to the contribution of the interface traps and another related to the traps deep inside the dielectric layer as given by equations 3.1 and 3.2 respectively [61].

$$\Delta V_{th,IT} \sim exp\left(-\frac{E_a}{K.T}\right).\left[\frac{\varepsilon}{t_{ox}}(V_{GS}-V_{th})\right]^{TITCE}.exp[TITFD.E(V_{GS},V_{DS})].t^{NIT} \quad (3.1)$$

$$\Delta V_{th,OT} \sim exp\left[-\frac{TOTFD+\frac{TOTTD}{T}}{E(V_{GS},V_{DS})}\right].t^{NOT} \quad (3.2)$$

where $E(V_{GS},V_{DS})$ denotes the strength of the electric field of the dielectrics. The MOSRA partial recovery effect model is given by equation 3.3 [61].

$$\Delta V_{th,AC} = TTD0\,.\Delta V_{th}\,.exp(-TDCD\,.g) \quad (3.3)$$

where g quantity models the effect of duty cycle. Some of parameters and their descriptions of Synopsys LEVEL1 MOSRA BTI model for V_{th} degradation are listed in Table 3.1[60].

Table 3.1 V_{th} Degradation BTI parameters

Name	**Default**	**Description**
TIT0	0	First parameter for interface trap inducing threshold voltage degradation
TITCE	0	Inversion charge exponent for interface trap inducing threshold voltage degradation
TITFD	0	Oxide electric field dependence for interface trap inducing threshold voltage degradation
E_a or TITTD	0	Temperature dependent component of interface trap inducing threshold voltage degradation

Table 3.1 (cont’d)

NIT or TN	0.25	Stress time exponent for interface trap inducing threshold voltage degradation
TOT0	0	First parameter for oxide trap inducing threshold voltage
TOTFD	0	Oxide electric field dependent component for oxide trap inducing threshold voltage degradation
TOTTD	0	Temperature dependent component for oxide trap inducing threshold voltage degradation
TOTDD	0	Drain voltage dependent coefficient for oxide electric field in threshold voltage degradation
NOT or TK	0.5	Stress time exponent for oxide trap inducing threshold voltage degradation
TTD0	1	First parameter for transient degradation of threshold voltage (Note: TTD0=0 disables the V_{th} recovery effect)
TDCD	0	Duty cycle dependent exponent for transient degradation of threshold voltage (Note: TDCD is expected to be 0 or negative)
TOTDE	1	Drain voltage exponent for oxide electric field in threshold voltage degradation

The MOSRA HCI model which accurately accounts for bias dependence over a wide range of drain, gate and substrate biases, and over different temperatures is given by equation 3.4 [61].

$$\Delta V_{th,HCI} \sim \left[THCI1.\left(\frac{I_{DS}}{W_{eff}}\right)^{TDCE}.\left(\frac{I_{sub}}{I_{DS}}\right)^{TDII} + THCI2.V_{DS}{}^{TDVD}.\left(\frac{I_{DS}}{W_{eff}}\right)^{TDID}\right].t^{HN} \quad (3.4)$$

Where the first term corresponds to the lucky electron model (LEM) and the second term improves model accuracy in the high current regime. Some of parameters and their descriptions of Synopsys LEVEL1 MOSRA HCI model for V_{th} and mobility degradation are listed in Table 3.2 [60]. In addition to the built-in HCI and BTI aging models which discussed above, the users can implement and develop their own special HCI and BTI aging models with special model equations through a MOSRA API (Application Program Interface) and compile them into dynamically linked library.

Table 3.2 V_{th} and mobility degradation HCI parameters

Name	**Default**	**Description**
THCI0	0	First parameter for threshold voltage degradation induced by HCI
TCHI1	0	Coefficient for I_{sub}-dependent term of mobility HCI degradation
TDII	0	Impact ionization current exponent for threshold voltage degradation induced by HCI
TDLE	1	Channel length exponent for threshold voltage degradation induced by HCI
TDCE	0	Channel current exponent for threshold voltage degradation induced by HCI
TEA	0	Equivalent activation energy of V_{th} HCI degradation
TDVD	0	V_{DS} term exponent of V_{th} HCI degradation
TDID	1	Channel current exponent for V_{DS}-dependent term of V_{th} HCI degradation
TDVB	1	Exponent for V_{BS} dependence of V_{th} HCI degradation
HN	0.5	Time exponent for threshold voltage degradation induced by HCI

3.2 Working Principle of MOSRA

The working of MOSRA occurs in two phases which called the pre-stress simulation phase and the post-stress simulation phase.

- **Pre-Stress Simulation Phase**

During this simulation phase, which is also known as fresh simulation phase, HSPICE computes the electrical stress of every user-selected MOSFET in the circuit based on the built-in MOSRA aging model equations and the circuit behavior. The calculated electrical stress value from MOSRA equation is firstly integrated over a user-specified time of circuit operation (age) through the duration of transient analysis and then the result of this integration is extrapolated to calculate the total MOSFET device performance degradation at the end of a user-specified time (for example: 10 years).

❖ Post-Stress Simulation Phase

For the post-stress simulation, a second simulation is running at the end of pre-stress simulation phase. During this simulation phase, HSPICE translates the combination of characteristics degradation of every user-selected MOSFET transistor which was calculated in pre-stress simulation phase into a degradation of circuit parameters. At each MOSRA aging analysis time step of the circuit, the MOSRA flow considers the accumulated degradation information from previous time steps, resulting in the accumulated electrical stress effect is taken into account implicitly. The post-stress MOSRA simulation can be done depending on either DC, or AC, or transient analysis [61].

Consequently, these two separate simulation phases which can be executed either in the same HSPICE simulation run or independently as needed are required to successfully accomplish the aging analysis by utilizing of MOSRA.

3.3 MOSRA Flow

The whole MOSRA flow as shown in Figure 3.1 consists of two separate simulation phases: the pre-stress simulation phase in which the resulted values related to a fresh MOSFET device and the post-stress simulation phase in which the resulted values related to the aged MOSFET device.

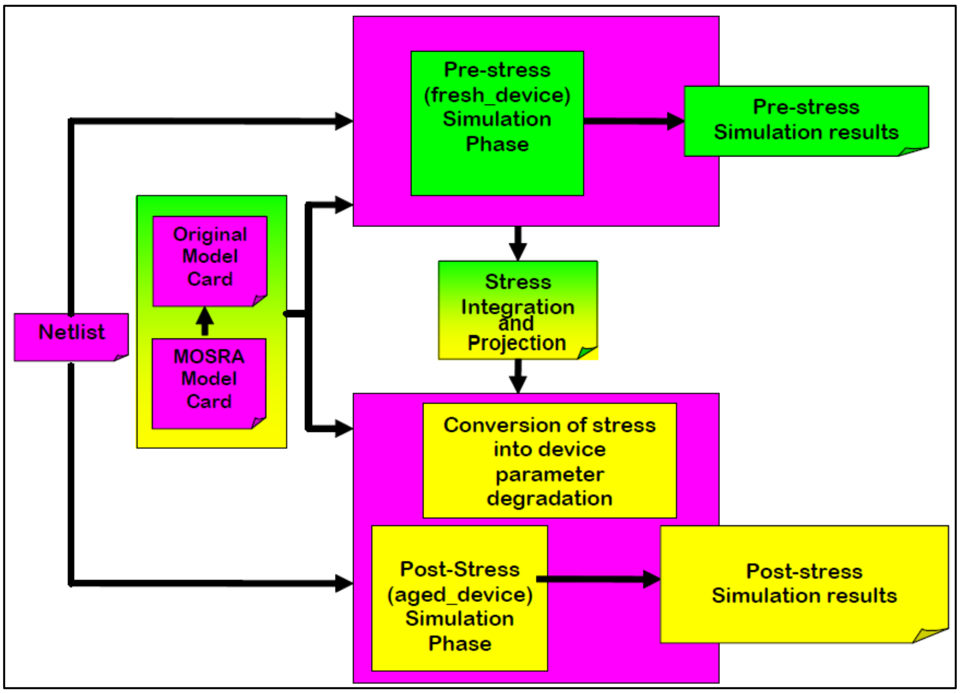


Fig. 3.1 HSPICE reliability simulation flow [60]

3.4 Important MOSRA Commands and Control Options

The commands and control options are significant for execution of HSPICE MOSRA reliability analysis in a successful way and some of them and their descriptions are mentioned in Appendix-A [62].

CHAPTER 4

ANALYSIS OF NBTI AGING SIMULATION ON A SINGLE PMOSFET TRANSISTOR

In chapter 2, a discussion was made about NBTI as a major physical aging mechanism in pMOS devices. Consequently, the degradation of main pMOS devices parameters such as increasing the threshold voltage V_{th} in magnitude resulting in decreasing of drain current I_D and transconductance g_m. The generation of interface states (or interface traps) which created by the diffusion of hydrogen atoms are the dominant physical mechanisms of NBTI degradation.

In order to investigate NBTI aging effect in a single pMOSFET transistor, a pMOSFET transistor is connected as depicted in Figure 2.3. Consequently, the pMOSFET transistor operates in the linear region and we varied the DC gate-source stress voltage V_{GS} from $-1.2V$ to $-0.4V$ in an increment of $0.4V$ while the other terminals of pMOSFET transistor are grounded. Based on HSPICE MOSRA simulation, the NBTI aging analysis of a single pMOSFET transistor with various V_{GS} values is done and the degradation of threshold voltage V_{th} is calculated for ten years with a time step of one year. The results of these experiments are listed in Table 4.1, 4.2, and 4.3 respectively. When gate-source stress voltage $V_{GS} = -1.2V$ is applied, V_{th} increases 57.917%. In case of $V_{GS} = -0.8V$, the V_{th} variation is 51.132%, and in case of $V_{GS} = -0.4V$ the change in V_{th} magnitude is 45.722%.

Table 4.1 The degradation of pMOS (W/L=900nm/90nm) threshold voltage values for $V_{GS} = -1.2V$

Age in Year	**V_{th} Shift x10^{-2} [V]**	**New V_{th} Values [V]**
0	0	0.285479

Table 4.1 (cont’d)

1	1.121086	0.296689
2	1.330878	0.309997
3	1.471678	0.324713
4	1.580613	0.340519
5	1.670668	0.357225
6	1.748060	0.374705
7	1.816293	0.392867
8	1.877552	0.411642
9	1.933301	0.430975
10	1.984571	0.450820

Table 4.2 The degradation of pMOS (W/L=900nm/90nm) threshold voltage values for $V_{GS} = -0.8$V

Age in Year	**V_{th} Shift x10^{-2} [V]**	**New V_{th} Values [V]**
0	0	0.285479
1	0.989355	0.295372
2	1.174736	0.307119
3	1.299139	0.320110
4	1.395386	0.334063
5	1.474952	0.348812
6	1.543332	0.364245
7	1.603620	0.380281
8	1.657747	0.396858
9	1.707006	0.413928
10	1.752309	0.431451

Table 4.3 The degradation of pMOS (W/L=900nm/90nm) threshold voltage values for $V_{GS} = -0.4V$

Age in Year	**V_{th} Shift x10^{-2} [V]**	**New V_{th} Values [V]**
0	0	0.285479
1	0.882058	0.294299
2	1.048950	0.304788
3	1.160854	0.316396
4	1.247418	0.328870
5	1.318984	0.342059
6	1.380495	0.355863
7	1.434735	0.370210
8	1.483439	0.385044
9	1.527769	0.400321
10	1.568546	0.416006

In all above mentioned experimental cases, the pMOSFET transistor channel length value is used as the minimum possible channel length permitted in the 90 nm fabrication process node which is $L = 90$ nm and the pMOSFET transistor channel width is used as 10 times L which is $W = 900$ nm. We noted that the impact of NBTI causes a shift in pMOSFET transistor threshold voltage V_{th} and NBTI is dependent on the applied gate-source stress voltage V_{GS} with a maximum threshold voltage degradation occurs at $V_{GS} = -1.2V$ for a pMOSFET transistor operating for 10 years which manifests as an increase in V_{th} by an amount of 57.917%.

By comparing the threshold voltage value $V_{th} = -0.285479V$ for a fresh pMOSFET transistor with the aged pMOSFET transistor V_{th} values for 10 years lifetime which obtained for different V_{GS} stress values, we observe an increase in the range of different millivolts in the magnitude of pMOSFET transistor V_{th} values. Consequently, we can observe from the HSPICE MOSRA simulation results that the shift and the increase or the degradation in the magnitude of pMOSFET transistor threshold voltage V_{th} value is dependent on the applied gate-source stress voltage value V_{GS}, and the impact of NBTI degradation for pMOSFET transistor exacerbates with stress time. The dependence of the shift and the degradation in the magnitude of the NBTI-induced threshold voltage V_{th} of the pMOSFET transistor on the applied gate-source voltage V_{GS} and on the stress time is shown in Figure 4.1 and 4.2, respectively.

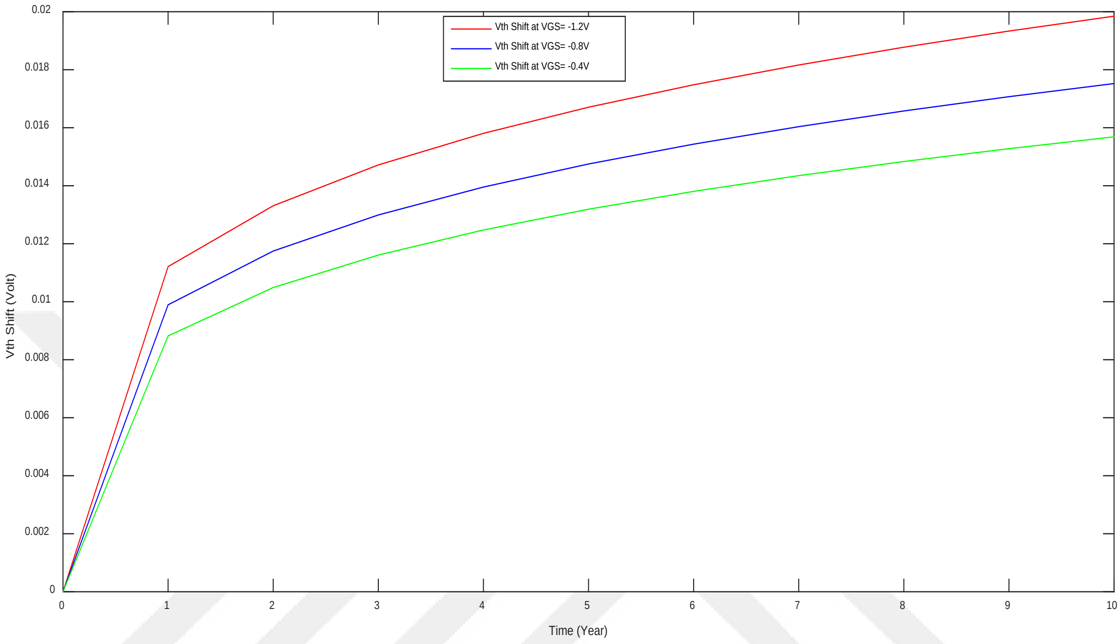


Figure 4.1 NBTI-induced threshold voltage shift ΔV_{th} of pMOSFET transistor increases with V_{GS} and stress time.

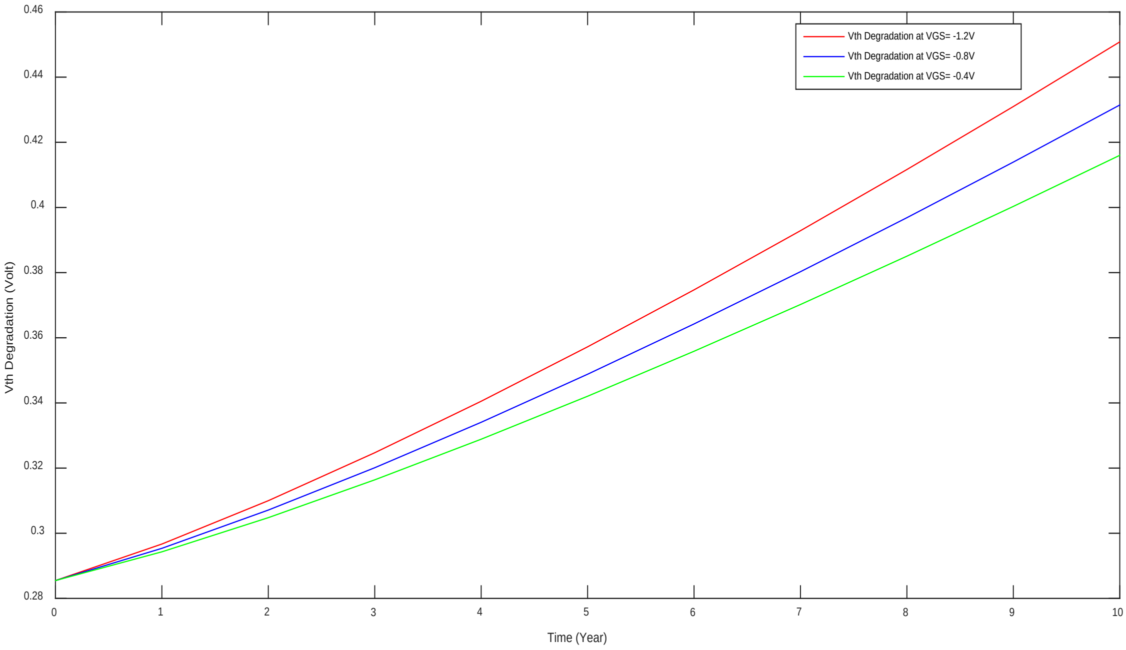


Figure 4.2 NBTI-induced threshold voltage V_{th} degradation of pMOSFET transistor increases with V_{GS} and stress time.

The knowledge of the precise value of the threshold voltage V_{th} of the MOSFET transistors parameters is of a significant importance in the design of integrated circuits (ICs). In addition, the other MOSFETs transistors performance parameters which dependent on or affected by the degradation of the threshold voltage value V_{th} such as the transconductance g_m and the drain current I_D are also important in ICs design. Consequently, the drifts in these MOSFETs transistors parameters values may affect the analog circuits performance metrics and in worst cases resulting in the overall circuits failure.

A detailed analysis is performed in Chapter 5 to investigate the NBTI aging effects impact on the design of unbuffered two-stage CMOS operational amplifier topology in order to deeply understand the impact of above discussed NBTI degradation of a single pMOSFET transistor on the analog circuit level.

CHAPTER 5

DESIGN OF A TWO-STAGE CMOS OP-AMP CIRCUIT AND ANALYSIS THE EFFECT OF NBTI

The operational amplifier (Op-Amp) is one of the most important and the most versatile integrated building block which is used in the design of many analog and mixed-signal VLSI (Very Large-Scale Integration) electronics circuits and systems. Generally, the operational amplifier from the standpoint of a signal is a device with three terminals: a differential input with an inverting input terminal identified by a “−” sign, a non-inverting input terminal identified by a “+” sign and one output terminal [63-70]. The difference between the use of unbuffered operational amplifier and buffered operational amplifier terminologies is that the first term is used to indicate the operational amplifier with a high output resistance (i.e. Operational Transconductance Amplifier or OTA) while the second term is used to indicate the operational amplifier with a low output resistance (i.e. buffered or voltage Op-Amp). The operational amplifier standard symbol is as shown in Figure 5.1 and its functioning can be represented by a two types of independent source: independent voltage source and independent current source, also as four types of dependent sources: VCVS (Voltage-Controlled Voltage Source), VCCS (Voltage-Controlled Current Source), CCVS (Current-Controlled Voltage Source) and CCCS (Current-Controlled Current Source) [63].

Many of the analog circuits and systems have been developed based on the fundamental principle used in operational amplifiers, this principle states that the operational amplifier should have a sufficient high forward DC gain so that when the negative feedback is applied, the operational amplifier’s closed-loop transfer function is practically independent of its gain [63, 64, 65].

The CMOS out of all transistors types being a greatly successful because it can be easily sized down to micrometer and nanometer dimensions due to the continuously shrinking-

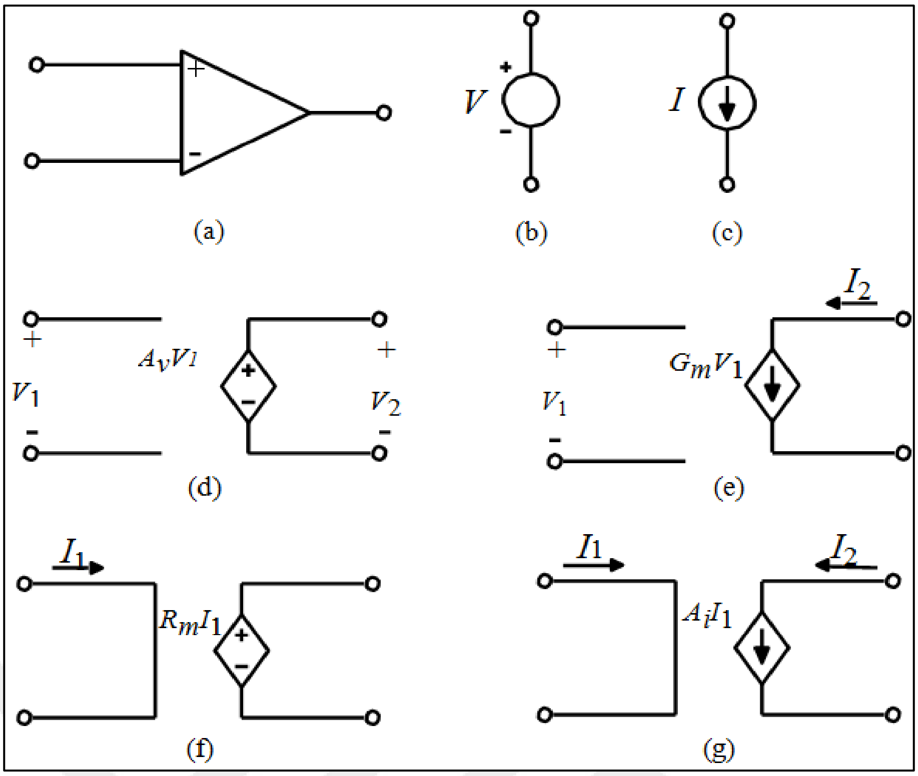


Figure 5.1 (a) Symbol for an operational amplifier. (b) Independent voltage source. (c) Independent current source. (d) Voltage-controlled voltage source (VCVS). (e) Voltage-controlled current source (VCCS). (f) Current-controlled voltage source (CCVS). (g) Current-controlled current source (CCCS) [63]

of the channel length and supply voltages of the MOSFET transistor in an advanced CMOS technology nodes. Consequently, a large number of fast and small MOSFET transistors can be integrated on a single chip which leads to the need for high-frequency operation and this can be achieved successfully by utilization of CMOS operational amplifier [71]. Operational amplifiers are linear devices being used extensively to perform various mathematical operations such as addition, subtraction, integration, differentiation etc. [72, 73, 74]. As well as, operational amplifiers are among the most widely used electronic devices extensively used in consumer, industrial and scientific devices and they have all the required properties to be used in many applications such as the generation of DC bias, signal conditioning and filtering at high speed [72-78]. At present, the growing demand for mobile applications with the smaller size and longer battery life in all marketing sectors which include computers, medical, telecommunications and consumer electronics has led to the trend of the industry towards silicon chip systems with low power and low voltages [74].

Moreover, as a result of the industry trend for the application of standard process technologies for the implementation of both analog and digital circuits on a single chip, CMOS technologies have become more dominant than the bipolar technologies for the design of analog circuits in mixed-signal systems. A majority of the existing analog circuits require significant changes in the design or even re-designed in order to adapt to the scaled down MOSFET devices levels with lower power supplies, while many of the digital circuits can be adapted to meet the same constraints. Consequently, the processes of improving analog circuits are becoming increasingly more challenging [73].

In order to use operational amplifiers to perform various functions which previously mentioned, they were built with different levels of complexities. The operational amplifier can perform a wide variety of analog signal processing functions when it is connected with a handful of external components. In order to get a higher gain from operational amplifiers, they are used with two or more stages. As a result, one of the most popular operational amplifiers is the two-stage operational amplifier which can be designed using the CMOS technology which is well known as a two-stage CMOS Op-Amp is the purpose of this work [73-78].

5.1 Architecture of Two-Stage CMOS Operational Amplifier

Operational amplifiers are one of the important and basic circuits which are used as the backbone in the analog circuits design in a wide variety of applications. These analog circuits' speed and accuracy depends on the DC gain and bandwidth of the operational amplifiers. The speed and accuracy of operational amplifier depend on its DC gain and bandwidth. Consequently, the operational amplifier with higher speed and accuracy results from larger DC gain and bandwidth of the operational amplifier [79].

A generic two-stage Op-Amp block diagram with an output buffer is shown in Figure 5.2 [63]. The first block, which represents the input of the operational amplifier, is a differential-transconductance stage and the differential amplifier is usually most commonly being used in this stage. The differential amplifier has two inputs which are the inverting voltage input and the non-inverting voltage input. Depending on the differential input applied it provides a differential voltage or current at its output. This differential-input stage provides normally the greater part of the operational amplifier circuit total gain, which consequently results in an improvement in the noise and offset of the operational amplifier circuit.

The following block represents the second stage of the operational amplifier which is an inverter acting as a differential to a single-ended converter. This second-stage inverter is

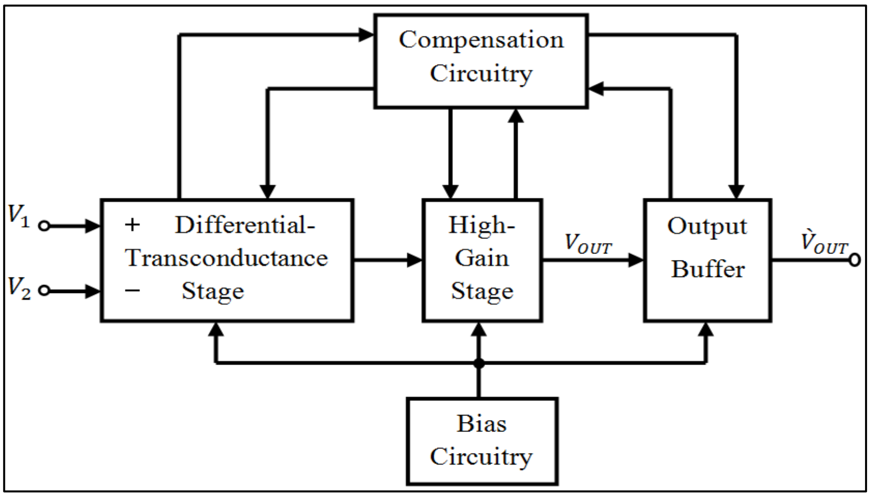


Figure 5.2 Block diagram of a generic two-stage Op-Amp [63]

used to convert the differential signal which generated from the differential-input stage to the single-ended signal in the case that the differential-input stage is not carried out the differential to single ended conversion. The differential-input stage gain is usually insufficient; therefore there is a need for additional amplification to the operational amplifier circuit gain which can be provided by the second stage. Output buffer stage used in the case of the operational amplifier should drive a low output load resistance. This stage should come after the second-stage inverter. The purpose of the output buffer stage is to provide low output impedance and larger current at the output which is necessary to drive the load of the operational amplifier as well it improves the slew rate or a large output swing of the operational amplifier. The slew rate allowed by the second gain stage of the operational amplifier is usually sufficient in many applications and in addition to that there is no need to the low output impedance in many applications. In these cases, the output buffer stage can be neglected [63].

When the operational amplifier is used to drive a small capacitive load as is the case in a lot of switched capacitor applications, in this case there is no need to use the output buffer stage. The operational amplifier circuit, which does not use the output buffer stage, is called an operational transconductance amplifier (OTA) or unbuffered operational amplifier. The proper DC operating point of each transistor in the saturation region is provided by the block of the bias circuitry. The existence of a compensation circuitry is very important in the operational amplifier circuit and their intended use is to achieve the stability of the unstable basic Op-Amp circuit when the Op-Amp works in the closed-loop configuration when negative feedback is applied, as well as to reduce the gain of the Op-Amp circuit at high frequencies [63].

5.2 Operation of Two-Stage CMOS Operational Amplifier

CMOS Op-Amps have several different topologies; a two-stage CMOS Op-Amp configuration is the most commonly used among of the different CMOS Op-Amps configurations. A two-stage CMOS Op-Amp topology is used where there is a requirement for a high input impedance and high output impedance. The specific unbuffered two-stage CMOS Op-Amp which is selected to meet all the required design specifications in this study is shown in Figure 5.3. This circuit is composed of three main sub-circuits: the differential-input stage which is the differential gain stage with an active load, the second gain stage which is the common source stage with an active load and bias circuit [63, 80, 81, 82, 83, 84].

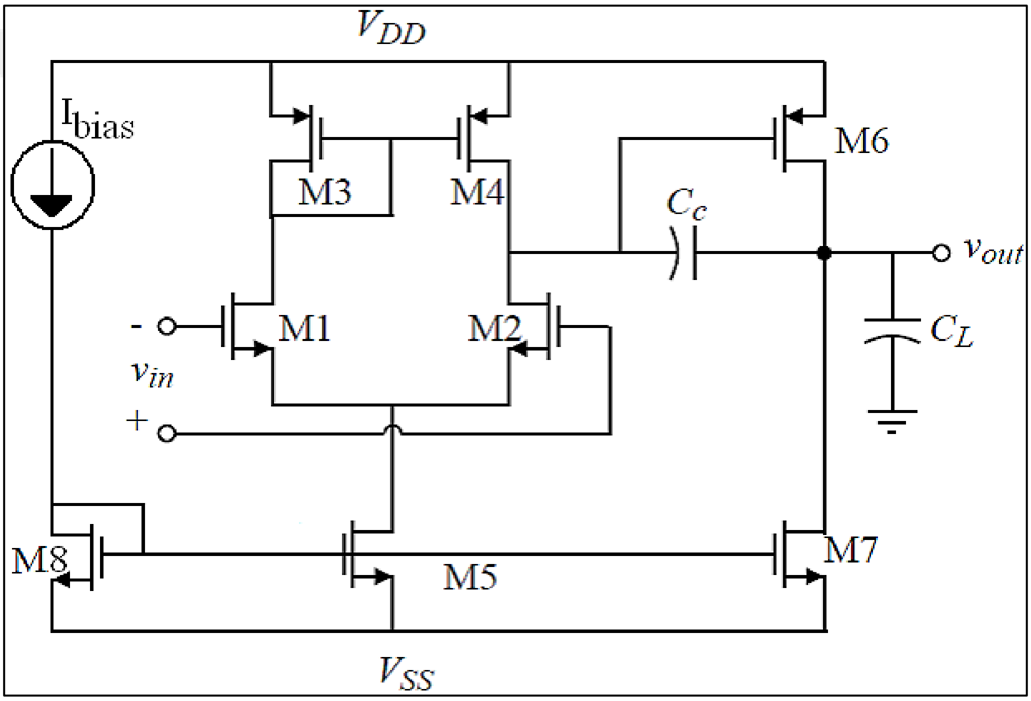


Figure 5.3 Topology of two-stage CMOS Op-Amp [63]

The selected two-stage CMOS Op-Amp topology provides several advantages, including high closed-loop voltage gain, large common-mode input voltage range, rail-to-rail output swing, the utilization of a single Miller capacitor for frequency compensation purpose, and a small number of CMOS transistors. But its main disadvantage is the creation of the non-dominant pole associated with the second stage output impedance and the capacity of the capacitive load and this non-dominant pole leads the bandwidth of the two-stage CMOS Op-Amp which can be achieved to decrease [81]. A thorough investigation of the two-stage CMOS Op-Amp sub-circuits will provide valuable insight about the two-stage CMOS Op-Amp operation.

5.2.1 Differential Gain Stage

The first sub-circuit of interest is the differential gain stage. This stage represents the first stage of the two-stage CMOS Op-Amp which is the differential amplifier with a differential to single ended converter built by the transistors M1, M2, M3, and M4. The input stage of the two-stage CMOS Op-Amp consists of the transistors M1 and M2, which are nMOSFET transistors. The inverting and non-inverting inputs of this first stage are the gate of transistor M1 and the gate of transistor M2, respectively. According to the amount of gain of the differential input stage, the differential input signal applied across the two inputs of this stage is amplified. The transconductance g_{m1} of transistor M1 or g_{m2} of transistor M2 represents the transconductance g_{mI} of this stage. The amount of gain provided by this stage is defined as the product of the transconductance of transistor M1 or M2 and the total output resistance of this stage, which is the resistance seen from the drain of transistor M2. There are two resistances mainly contribute to the total resistance of this stage which are the output resistance of the active load transistors M3 and M4 and the output resistance of the Input transistors M1 and M2. Transistors M3 and M4 are pMOSFET transistors which they constitute the current mirror active load circuit of the differential amplifier. There are three distinct benefits to the current mirror active load used in this circuit: it creates a large output resistance in a small area of the die, the topology of current mirror active load circuit converts the differential input signal to a single-ended one, and the CMRR (Common Mode Rejection Ration) is improved by the load [63, 82,83,84].

5.2.2 Second Gain Stage

This second gain stage is the current-sink inverter through which an additional gain is provided in the two-stage CMOS Op-Amp circuit. This stage consists of the transistors M6 and M7 which are pMOSFET transistor and nMOSFET transistor, respectively. The transistor M6 is connected in the common-source topology and works as a driver while the transistor M7 works as an active current-sink load for transistor M6. This stage receives the output of first differential gain stage through the drain of the transistors M2 and amplifies it through the transistor M6. The transconductance g_{m6} of transistor M6 represents the transconductance g_{mII} of this stage. The amount of gain provided by this stage is defined as the product of the transconductance of transistor M6 and the effective total resistance of this stage, which consists of the output resistances of the transistors M6 and M7 [63, 82, 83,84].

5.2.3 Bias Circuit

In bias circuit, the biasing of the two-stage CMOS Op-Amp circuit is achieved with the help of a current source and the transistors M8 which is nMOSFET, M5 which is also nMOSFET and M7. Transistor M8 and the current source provide the gate-source voltage of the transistors M5 and M7. Based on the value of these gate-source voltages of transistors M5 and M7, which are controlled by the bias circuit, a certain amount of current is sank by these transistors. The transistor M8 is connected as a diode in order to ensure that it remains operating in the saturation region. Proper biasing of the transistors M1, M2, M3, M4 and M5 in the two-stage CMOS Op-Amp circuit is controlled by the voltages of nodes which are present in the two-stage CMOS Op-Amp circuit. Most important thing here is that the transistor M6 is biased by the gate-source voltage of the current mirror load and this voltage is set up by the gate-source voltages of the transistors M1 and M2 [83].

5.3 Design Procedure for Two-Stage CMOS Operational Amplifier

There are several design steps that should be taken into account when designing an unbuffered two-stage CMOS Op-Amp circuit. Design steps assist in achieving the appropriate sizing of all MOSFET transistors used in the circuit. These steps start with selecting the value of MOSFET transistor length which should be used throughout the unbuffered two-stage CMOS Op-Amp circuit and this selected channel value for all MOSFET transistors lengths assists in maintaining the channel length modulation parameter λ constant which is an important parameter in calculating the gain of unbuffered two-stage CMOS Op-Amp circuit. It has been assumed that all MOSFET transistors are operating in saturation region in all the following steps involved in designing the unbuffered two-stage CMOS Op-Amp circuit [63]:

1. Select the minimum value for the compensation capacitor C_C by using equation (5.1) in order to achieve a desired 60 degree phase margin, this requirement demands that the placement of the undesired non-dominant or the output pole $p_2 \geq 2.2\,GBW$ (Gain Bandwidth or Unity Gain Bandwidth), assuming that the right half plane (RHP) zero is $z_1 \geq 10\,GBW$.

$$C_c > 0.22\, C_L \tag{5.1}$$

where C_L is the capacitance of the load capacitor.

2. Determine the value of the minimum tail current I_{D5} (the drain current of the transistor M5) by using equation (5.2) from the largest value of the SR (Slew Rate) and C_c values.

$$I_{D5} = SR.C_c \tag{5.2}$$

3. Design for W_1/L_1 (W_2/L_2) in order to achieve the desired gain bandwidth (GBW) using the transconductance of the differential-input stage ($g_{mI} = g_{m1} = g_{m2}$) by equations (5.3) and (5.4).

$$g_{m1,2} = GBW.C_c = 2\pi f_t C_c \tag{5.3}$$

$$W_1/L_1 = W_2/L_2 = \frac{(g_{m1,2})^2}{\grave{K}_{1,2} I_{D5}} \tag{5.4}$$

where f_t is the unity gain bandwidth frequency and $\grave{K}_{1,2}$ is the transconductance parameter of transistor M1 or M2 in saturation region.

4. Design for W_3/L_3 (W_4/L_4) in order to satisfy the positive ICMR (Input Common-Mode Range) voltage specification by using equation (5.5).

$$W_3/L_3 = W_4/L_4 = \frac{I_{D5}}{\grave{K}_{3,4}[V_{DD} - V_{in(max)} - \left|V_{th03,4}\right|_{(max)} + V_{th01(min)}]^2} \geq 1 \tag{5.5}$$

where $\grave{K}_{3,4}$ is the transconductance parameter of transistor M3 or M4 in saturation region, V_{DD} is the positive power supply voltage, $V_{in(max)}$ is the positive input common-mode range voltage and V_{th01} is the threshold voltage of transistor M1.

5. Design for $W_5/L_5\,(W_8/L_8)$ in order to satisfy the negative ICMR voltage specification by using equations (5.6) and (5.7).

$$V_{DS5(sat)} = V_{in(min)} - V_{SS} - \sqrt{\frac{I_{D5}}{\beta_1}} - V_{th01(max)} \;\geq 100mV \tag{5.6}$$

$$W_5/L_5 = W_8/L_8 = \frac{2I_{D5}}{\grave{K}_5\;[V_{DS5(sat)}]^2} \tag{5.7}$$

where $V_{DS5(sat)}$ is the drain-source saturation voltage of the transistor M5, $V_{in(min)}$ is the negative input common-mode range voltage, V_{SS} is the negative power supply voltage and β_1 is the transconductance parameter of transistor M1 in the saturation region in terms of M5 physical parameters (i.e. W_5/L_5).

6. Design for W_6/L_6 by using equation (5.8); assuming that the source-gate voltage of transistor M4 V_{SG4} is equal the source-gate voltage of transistor M6 V_{SG6} in order to achieve the appropriate mirroring for the current mirror active load transistors M3 and M4.

   $$W_6/L_6 = W_4/L_4\left(\frac{g_{m6}}{g_{m4}}\right) \tag{5.8}$$

   where g_{m6} is the value of the transistor M6 transconductance which can be calculated by using equation (5.9) for achieving a reasonable PM (Phase Margin) requirement.

   $$g_{m6} \geq 10g_{m1} \tag{5.9}$$

   and g_{m4} is the value of the transistor M4 transconductance which can be calculated using equation (5.10).

   $$g_{m4} = \sqrt{2\grave{K}_4(W_4/L_4)(I_{D5}/2)} \tag{5.10}$$

7. Now we solve for the current I_{D6} by using equation (5.11) which is the transistor M6 drain current that most likely determine the majority of the unbuffered two-stage CMOS Op-Amp circuit's power dissipation.

   $$I_{D6} = \frac{(g_{m6})^2}{2\grave{K}_6(W_6/L_6)} \tag{5.11}$$

8. Design for W_7/L_7 by using equation (5.12) in order to achieve the desired current ratios between I_{D5} which is the drain current of transistor M5 and I_{D6}.

   $$W_7/L_7 = W_5/L_5\left(\frac{I_{D6}}{I_{D5}}\right) \tag{5.12}$$

9. Check for specifications of the gain and power dissipation of the unbuffered two-stage CMOS Op-Amp circuit by using equation (5.13) and (5.14), respectively.

   $$A_v = \frac{2g_{m2}g_{m6}}{I_{D5}(\lambda_2 + \lambda_3)I_{D6}(\lambda_6 + \lambda_7)} \tag{5.13}$$

   $$P_{diss} = (I_{D5} + I_{D6})(V_{DD} + |V_{SS}|) \tag{5.14}$$

   where λ is the parameter of channel length modulation.

10. Finally simulate the unbuffered two-stage CMOS Op-Amp circuit in order to check if all specifications are met.

The design specifications which have been taken for designing the selected topology of the unbuffered two-stage CMOS Op-Amp circuit with 90 nm technology parameters which is shown in Figure 5.3 are listed in Table 5.1. The values of all MOSFET transistors aspect ratios W_i/L_i where $i = 1\ to\ 8$ and the DC currents for this selected topology can be calculated by making the calculations through the appropriate relationships provided above which used for all design steps in the circuit. Consequently, the retrieved aspect ratios of the different MOSFET transistors which are used in this circuit are listed in Table 5.2 and the value of the compensation capacitor is $C_c = 3pF$.

Table 5.1 The design specifications of the unbuffered two-stage CMOS Op-Amp circuit

Design Specifications Names	**Desired Values**
Gain	> 60dB
Unity Gain Bandwidth	≥ 3MHz
Phase Margin	$\geq 60^{\circ}$
Slew Rate	$\geq 10\,V/us$
$V_{in(min)}$	$\geq -1.2V$
$V_{in(max)}$	$\leq 1.2V$
CMRR	≥ 60dB
$PSRR^{+}$	≥ 60dB
$PSRR^{-}$	≥ 60dB
Load Capacitance	≥ 10pF
Power Dissipation	$\leq 1mW$
V_{DD}	$1.2V$
V_{SS}	$-1.2V$
Settling time T_S	$\leq 1us$

Table 5.1 (cont'd)

Input-offset Voltage V_{OS}	$< 500mV$
Output Voltage Swing	$-1.2V$-$1.2V$

Table 5.2 The aspect ratios of different MOSFET transistors

MOSFET Transistor	**Type**	**Aspect Ratio ($\boldsymbol{W/L}$)**
M1	nMOSFET	$0.275um/0.5um$
M2	nMOSFET	$0.275um/0.5um$
M3	pMOSFET	$16.33um/0.5um$
M4	pMOSFET	$16.33um/0.5um$
M5	nMOSFET	$3.869um/0.5um$
M6	pMOSFET	$48.27um/0.5um$
M7	nMOSFET	$5.719um/0.5um$
M8	nMOSFET	$3.869um/0.5um$

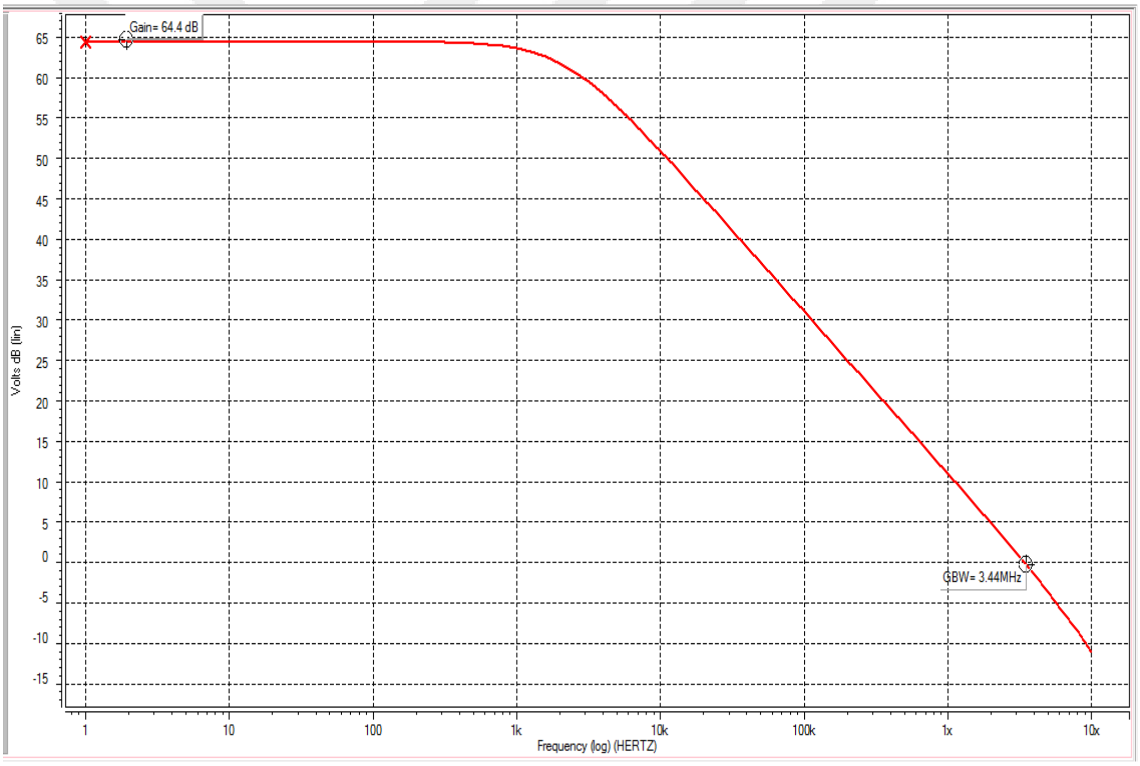
5.4 Simulation Results

In this section, the simulation results for the designed unbuffered two-stage CMOS Op-Amp circuit using 90 nm CMOS technology parameters which is shown in Figure 5.3 are provided without and with the NBTI aging effects impact on the circuit, respectively. This circuit has the design specifications and MOSFET transistors aspect ratios which are listed in the Tables 5.1 and 5.2 respectively, and $V_{th,n} = 0.279572V$, $V_{th,p} = -0.285479V$, $\grave{K_n} = 538.34\,uA/V^2$, $\grave{K_p} = 103.755\,uA/V^2$, $\lambda_n = 0.48V^{-1}$, $\lambda_P = 1.45V^{-1}$, and the bias current is $I_{bias} = 30uA$. The chosen channel length values for all MOSFET transistors in the circuit are $L_i = 0.5um$ where $i = 1\ to\ 8$ in order to minimize the channel length modulation parameter effect λ which is an important parameter results in increasing the gain of the unbuffered two-stage CMOS Op- Amp circuit [63, 82].

5.4.1 Simulation Results for the Unbuffered Two-Stage CMOS Op-Amp

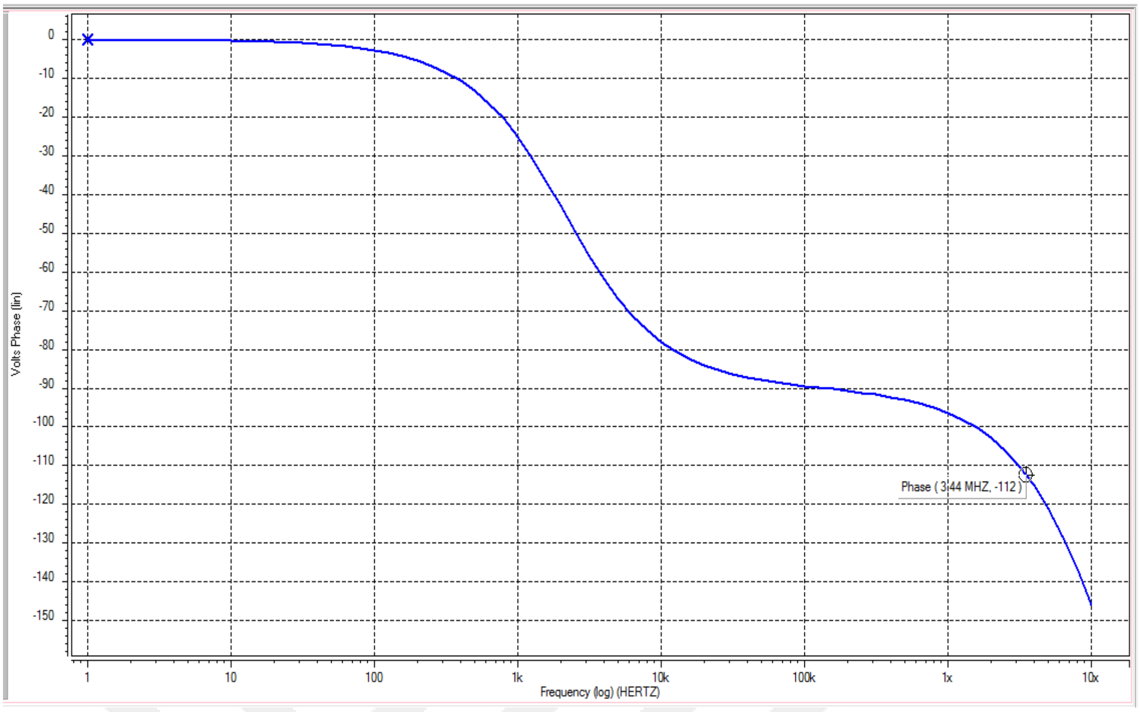
The simulation of the unbuffered two-stage CMOS operational amplifier circuit is done using HSPICE simulator and the obtained results are plotted using the Cscope tool of Synopsys in order to check the validity of the design. The gain A_v, gain bandwidth (GBW), phase margin, power dissipation, input resistance, output resistance, DC input-offset voltage, and the output voltage swing can be determined from the HSPICE simulation results of the unbuffered two-stage CMOS Op-Amp circuit in the open-loop configuration. The HSPICE input file is shown in Table B.1 in the Appendix-B.

Figure 5.4 shows the frequency response of the circuit. The results show that the gain A_v is 64.4dB, gain bandwidth (GBW) is 3.44MHz, and the phase margin for a $10pF$ load capacitor is 68°.



(a)

Figure 5.4 Frequency response of the unbuffered two-stage CMOS Op-Amp circuit
(a) Gain of the circuit. (b) Phase margin of the circuit.



(b)

Figure 5.4 (cont’d)

The power dissipation is found to be $258.79uW$, the input resistance is 739.6430MΩ, and the output resistance is 96.5636kΩ. Figure 5.5 shows the simulation results of the DC input-offset voltage which is $351mV$ and the output voltage swing range which is from $-1.19V$ to $+1.17V$.

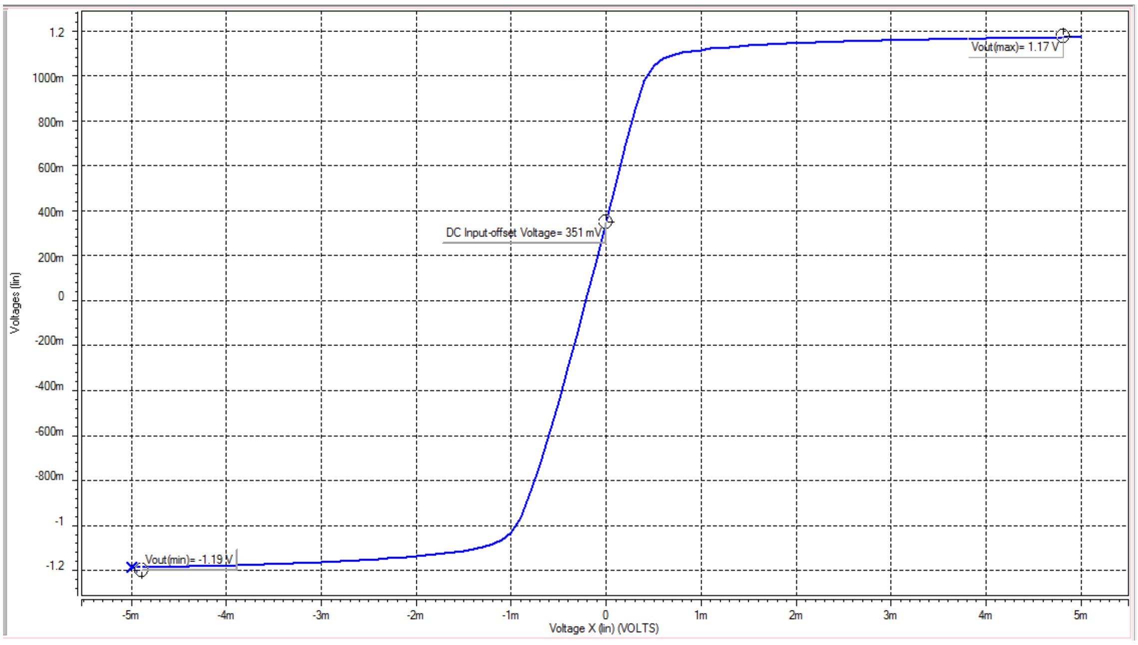


Figure 5.5 The simulation results of the DC input-offset voltage and the output voltage swing

Figure 5.6 shows the simulation result of $A_{v,cm}$ (Common-Mode Voltage Gain) of the unbuffered two-stage CMOS Op-Amp circuit which is found to be -5.52dB. The CMRR (Common-Mode Rejection Ratio) of the circuit can be calculated by subtracting the magnitude of $A_{v,cm}$ from A_v. Consequently, CMRR is found to be 69.92dB which means that the unbuffered two-stage CMOS Op-Amp has a good common-mode noise rejection.

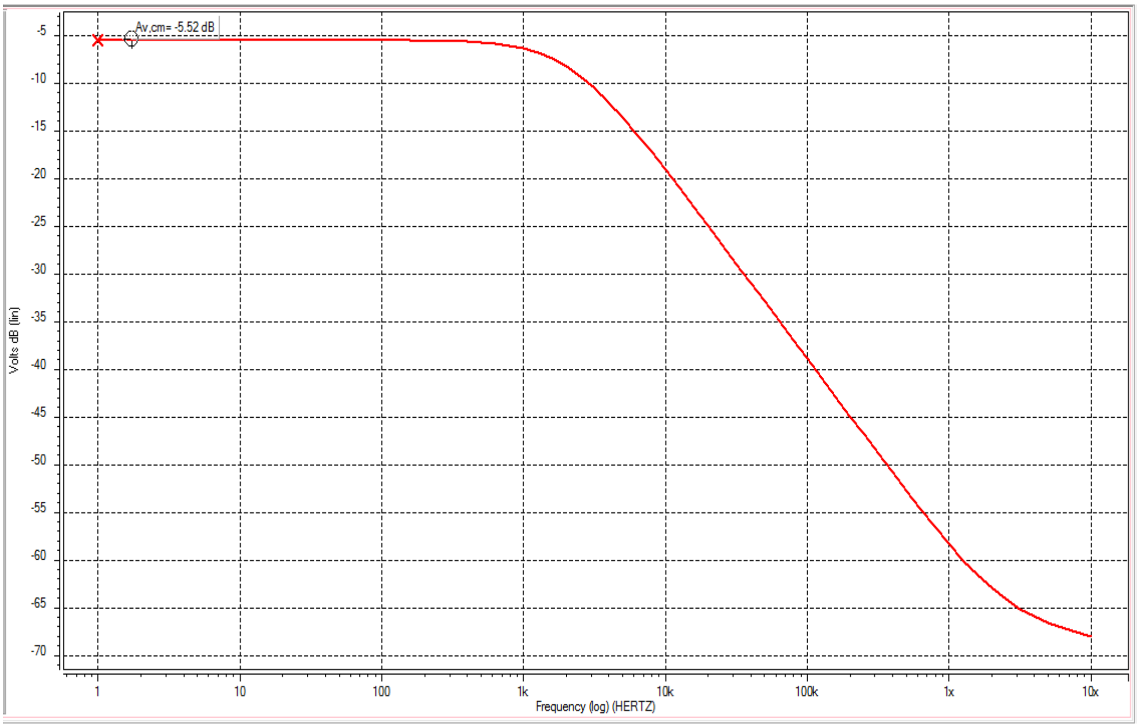


Figure 5.6 The simulation result of common-mode voltage gain $A_{v,cm}$ of the unbuffered two-stage CMOS Op-Amp circuit

The slew rate SR, settling time T_S, input common-mode range voltage (ICMR), and $PSRR$ (Power-Supply Rejection Ratio) can be determined from the HSPICE simulation results of the unbuffered two-stage CMOS Op-Amp circuit in the unity-gain configuration. The HSPICE input file is shown in Table B.2 in the Appendix-B.

Figure 5.7 shows the simulation results for slew rate SR and the settling time T_S of the circuit. It can be observed from Figure 5.7 that the achieved SR^+ (Positive Slew Rate) is $8.681V/us$, SR^- (Negative Slew Rate) is $3.712V/us$, and the settling time is $244ns$.

The simulation result of the input common-mode range voltage (ICMR) is shown in Figure 5.8 which found to be from $V_{in(min)} = -0.3V$ to $V_{in(max)} = 1.1V$.

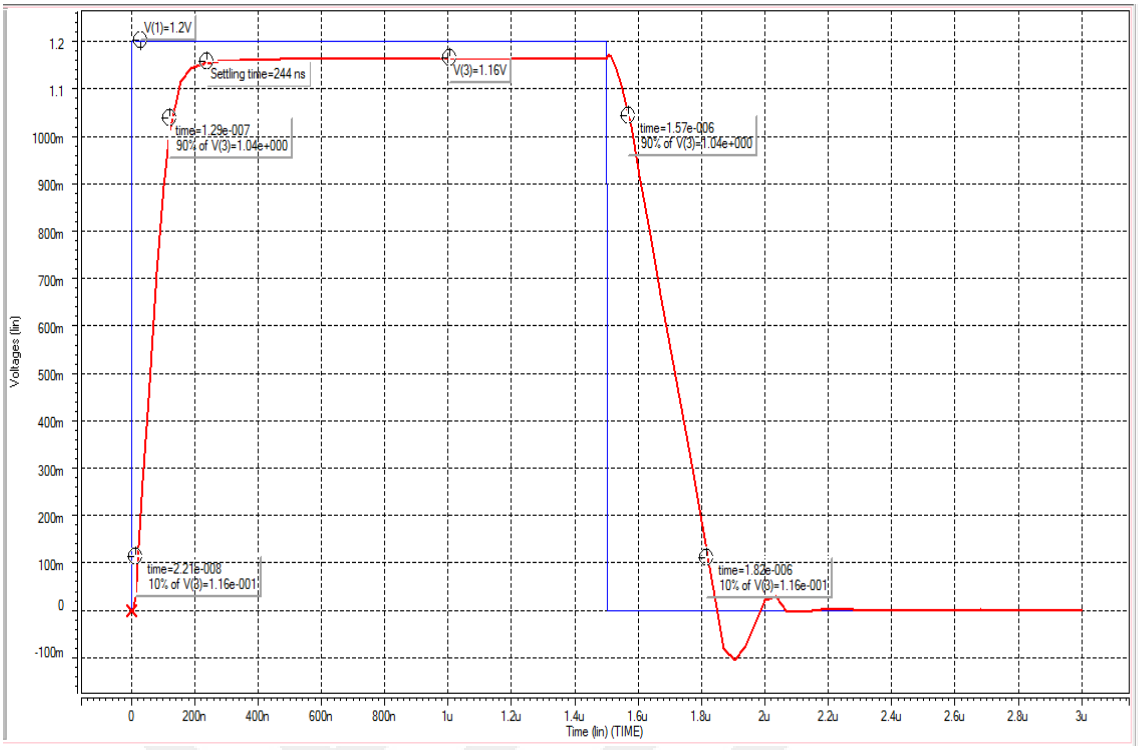


Figure 5.7 Slew rate and settling time simulation result for the unbuffered two-stage CMOS Op-Amp circuit

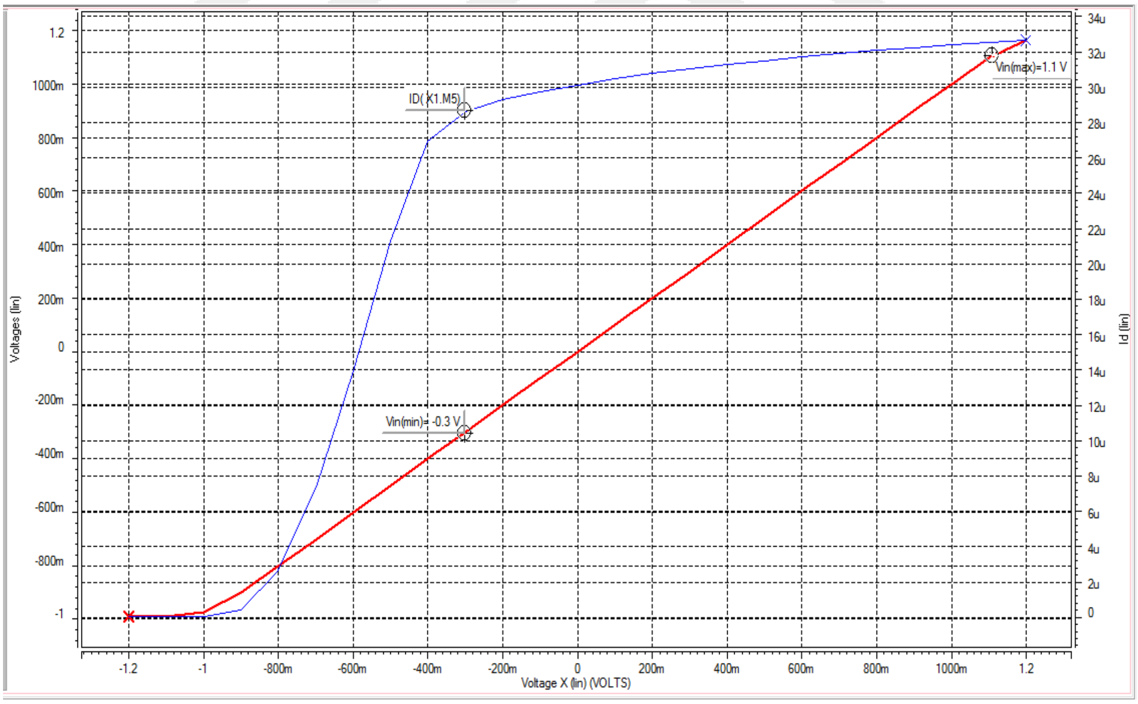
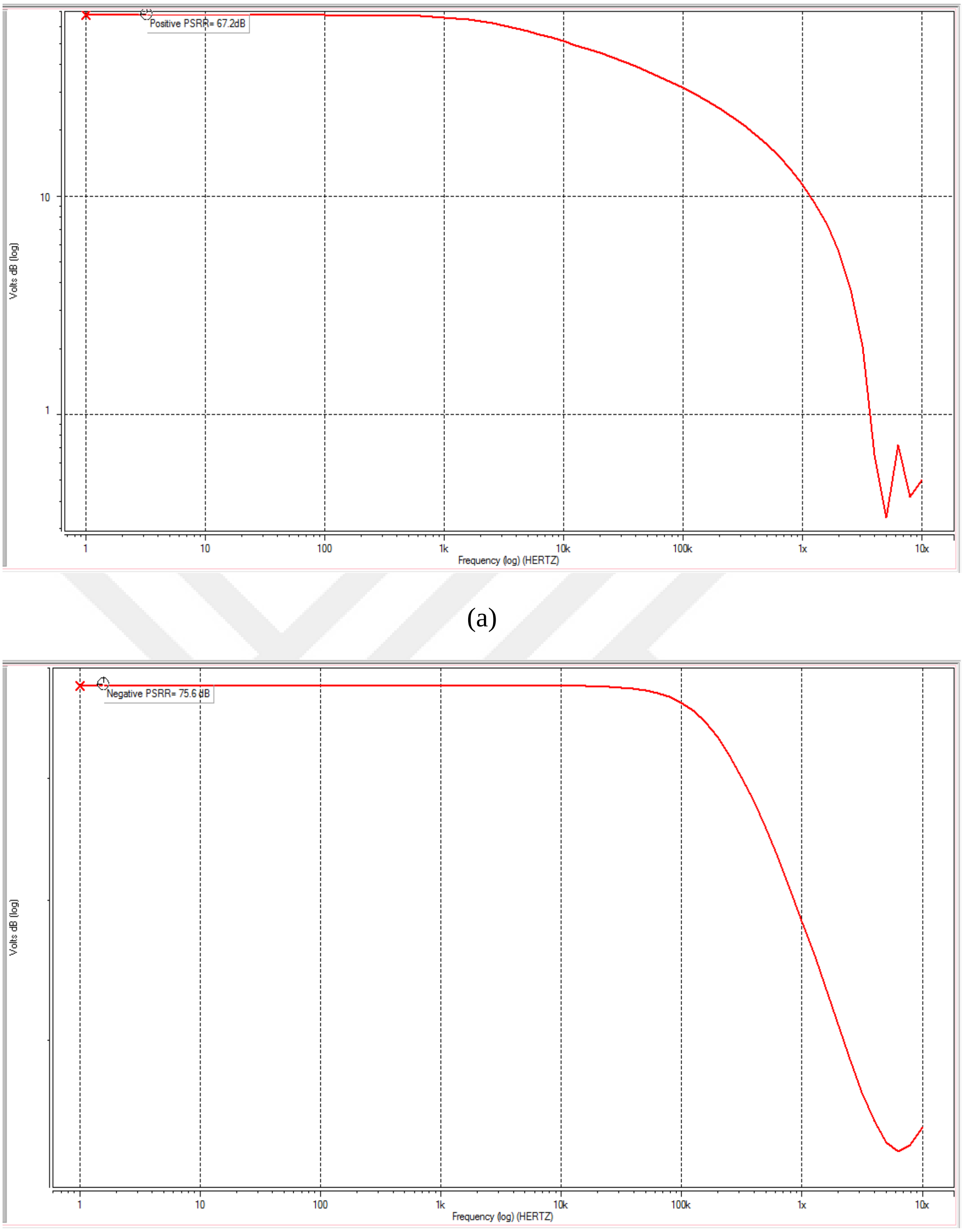


Figure 5.8 Input common-mode range voltage ICMR simulation result for the unbuffered two-stage CMOS Op-Amp circuit

Figure 5.9 shows the simulation results for $PSRR^{+}$ (Positive Power-Supply Rejection Ratio) and $PSRR^{-}$ (Negative Power-Supply Rejection Ratio), $PSRR^{+}$is found to be 67.2dB and $PSRR^{-}$ is 75.6dB.



(a)

(b)

Figure 5.9 Power-supply rejection ratio $PSRR$ simulation results for the unbuffered two-stage CMOS Op-Amp circuit. (a) Magnitude of $PSRR^{+}$. (b) Magnitude of $PSRR^{-}$.

Table 5.3 shows the HSPICE simulation results which extracted from the designed unbuffered two-stage CMOS Op-Amp circuit and also compare these results with desired design specifications. The results demonstrate that the unbuffered two-stage CMOS Op-Amp circuit satisfies most of the desired design specifications.

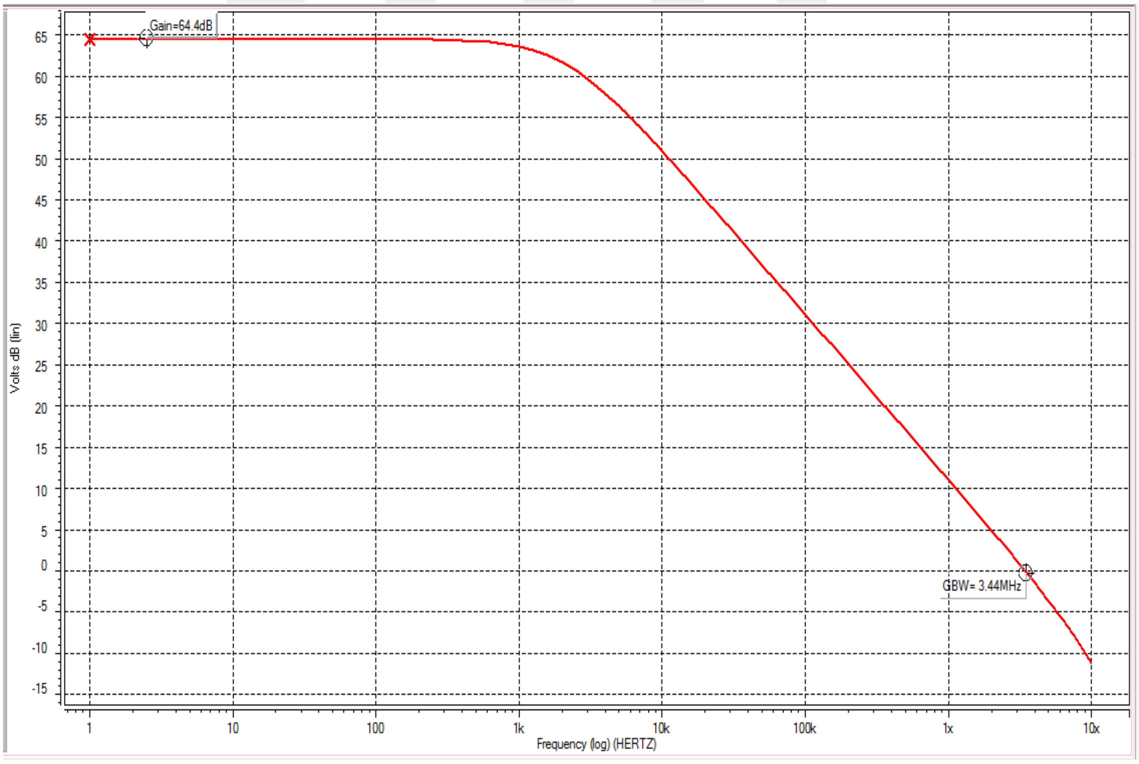
Table 5.3 Comparison of the simulation results with the desired design specifications of the unbuffered two-stage CMOS Op-Amp

Design Specifications Names	**Desired Values**	**Simulated Values**
Gain	$>$ 60dB	64.4dB
Unity Gain Bandwidth	$\geq$ 3MHz	3.44MHz
Phase Margin	$\geq 60^{\circ}$	68°
Slew Rate	$\geq 10\,V/us$	SR^{+} =8.681V/us, SR^{-} =3.712V/us
$V_{in(min)}$	$\geq -1.2V$	$-0.3V$
$V_{in(max)}$	$\leq 1.2V$	$1.1V$
CMRR	$\geq$ 60dB	69.92dB
$PSRR^{+}$	$\geq$ 60dB	67.2dB
$PSRR^{-}$	$\geq$ 60dB	75.6dB
Load Capacitance	$\geq$ 10pF	$10pF$
Power Dissipation	$\leq 1mW$	$258.79uW$
V_{DD}	$1.2V$	$1.2V$
V_{SS}	$-1.2V$	$-1.2V$
Settling time T_{S}	$\leq 1us$	$244ns$
Input-offset Voltage V_{OS}	$< 500mV$	$351mV$
Output Voltage Swing	$-1.2V$-$1.2V$	$-1.19V$-$1.17V$

5.4.2 Simulation Results for the NBTI Aging Effects Impact on the Unbuffered Two-Stage CMOS Op-Amp

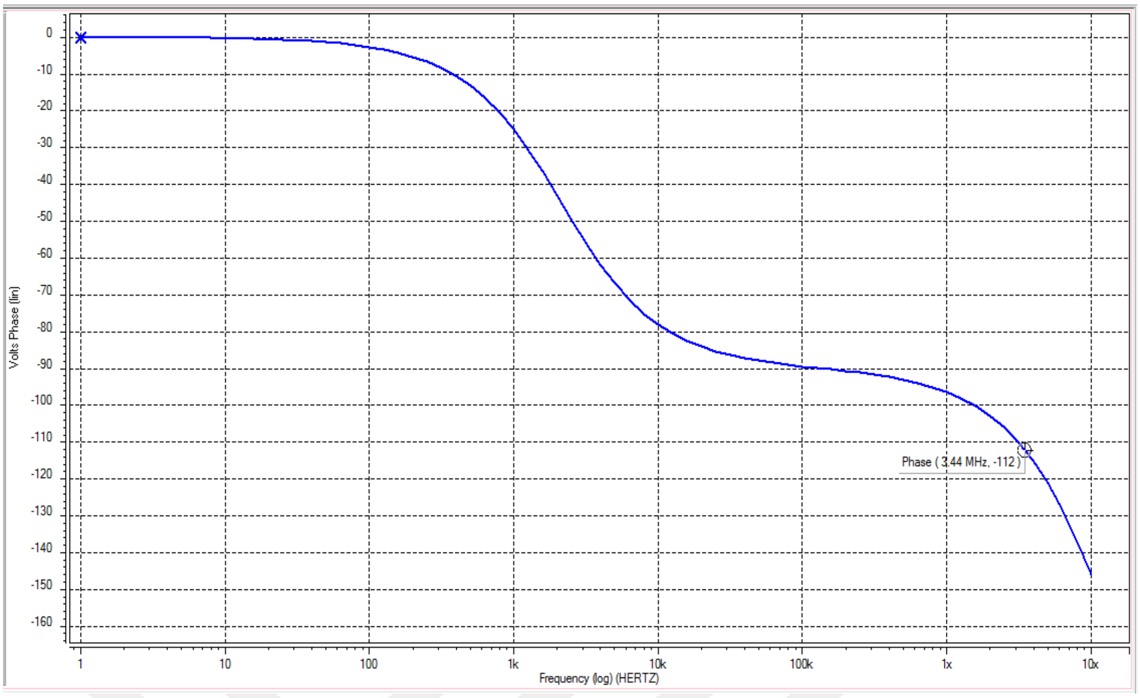
The simulation of the NBTI aging effects impact on the unbuffered two-stage CMOS Op-Amp circuit is done using HSPICE MOSRA for ten years with a time step of one year, and the obtained results are plotted using the Cscope tool of Synopsys in order to analyze the NBTI effects on the designed unbuffered two-stage CMOS Op-Amp circuit performance specifications. The gain A_v, gain bandwidth (GBW), phase margin, power dissipation, input resistance, output resistance, DC input-offset voltage, and the output voltage swing can be determined from the HSPICE MOSRA simulation results of the aged unbuffered two-stage CMOS Op-Amp circuit in the open-loop configuration. The HSPICE MOSRA input file is shown in Table B.3 in the Appendix-B.

Figure 5.10 shows the frequency response of the circuit. The results show that there is no change in the gain A_v, gain bandwidth (GBW), and the phase margin for a $10pF$ load capacitor which are 64.4dB, 3.44MHz, and 68°, respectively.



(a)

Figure 5.10 Frequency response of the aged unbuffered two-stage CMOS Op-Amp circuit. (a) Gain of the circuit. (b) Phase margin of the circuit.



(b)

Figure 5.10 (cont'd)

The power dissipation and the input and output resistances are also found to be not changed which are $258.79uW$, 739.6430MΩ, and 96.5636kΩ, respectively. Figure 5.11 shows the simulation results of the DC input-offset voltage is $351mV$ and the output voltage swing range is from $-1.19V$ to $+1.17V$, these results also not changed.

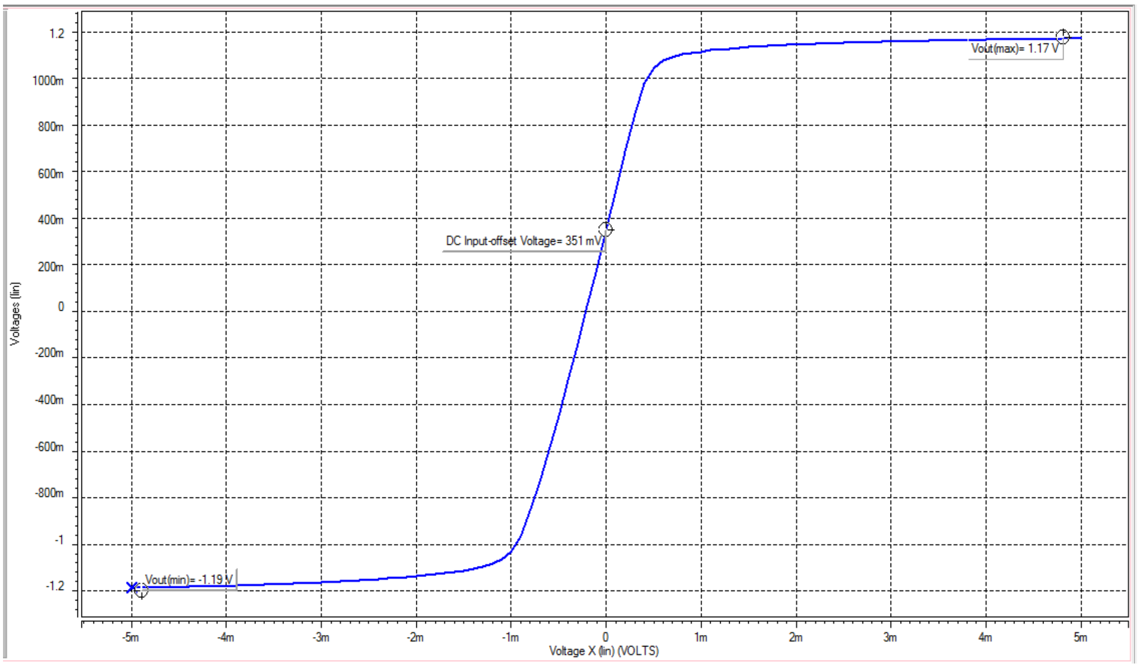


Figure 5.11 The simulation results of the DC input-offset voltage and the output voltage swing for the aged unbuffered two-stage CMOS Op-Amp circuit

Figure 5.12 shows the simulation result of common-mode voltage gain $A_{v,cm}$ of the aged unbuffered two-stage CMOS Op-Amp circuit which is found to be -5.52dB. The common-mode rejection ratio (CMRR) of the circuit can be calculated by subtracting the magnitude of $A_{v,cm}$ from A_v. Consequently, CMRR is 69.92dB which means that its value has not changed because of there is no change in the $A_{v,cm}$ and A_v values.

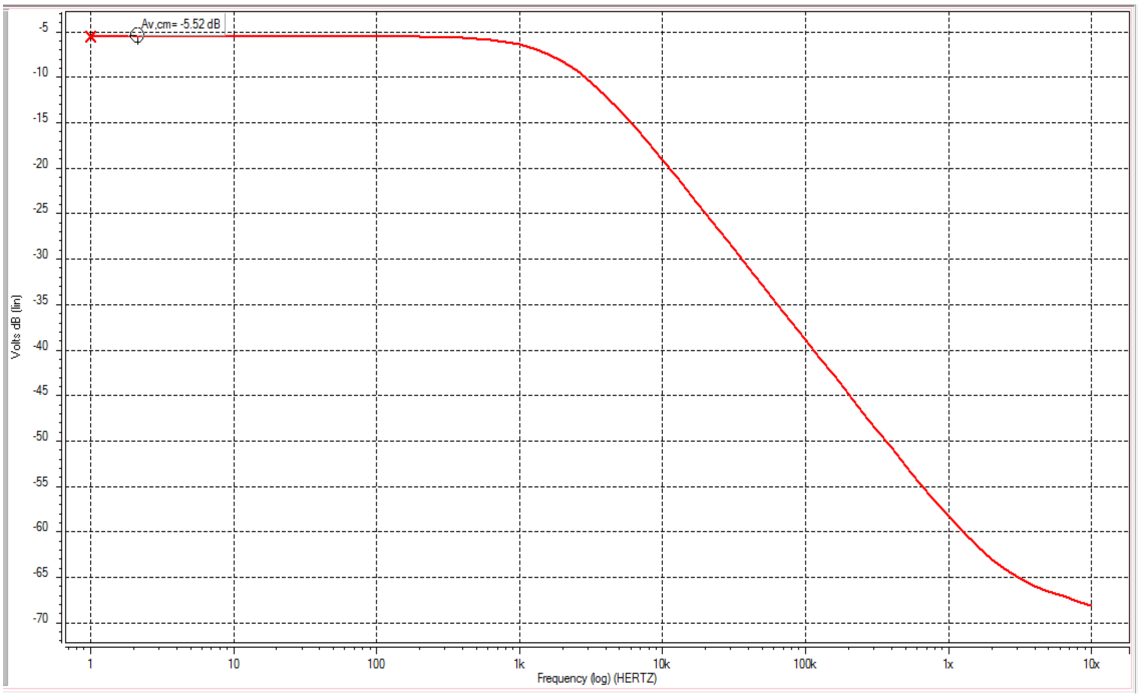


Figure 5.12 The simulation result of common-mode voltage gain $A_{v,cm}$ of the aged unbuffered two-stage CMOS Op-Amp circuit

The slew rate SR, settling time T_S, input common-mode range voltage (ICMR), and power-supply rejection ratio ($PSRR$) can be determined from the HSPICE MOSRA simulation results of the aged unbuffered two-stage CMOS Op-Amp circuit in the unity-gain configuration. The HSPICE MOSRA input file is shown in Table B.4 in the Appendix-B. Figure 5.13 shows the simulation results for the slew rate SR and the settling time T_S of the circuit. It can be observed from Figure 5.13 that the SR^+ (Positive Slew Rate) is become 8.600V/us, SR^- (Negative Slew Rate) is 3.712V/us, and the settling time is $244ns$. We can observe from these simulation results that the SR^+ (Positive Slew Rate) value has been reduced by 0.93%, but the SR^- (Negative Slew Rate) and the settling time are not changed.

The simulation result of the input common-mode range voltage (ICMR) is shown in Figure 5.14 which is also found to be from $V_{in(min)} = -0.3V$ to $V_{in(max)} = 1.1V$ and this means that there is no change in ICMR values.

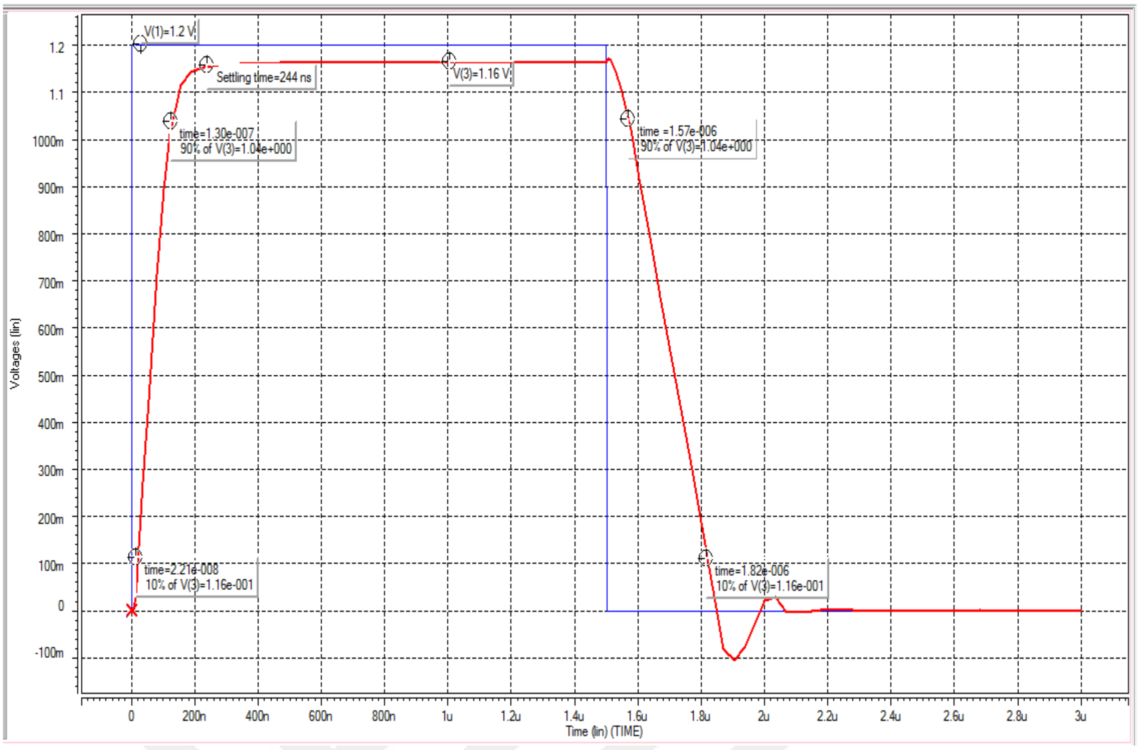


Figure 5.13 Slew rate and settling time simulation result for the aged unbuffered two-stage CMOS Op-Amp circuit

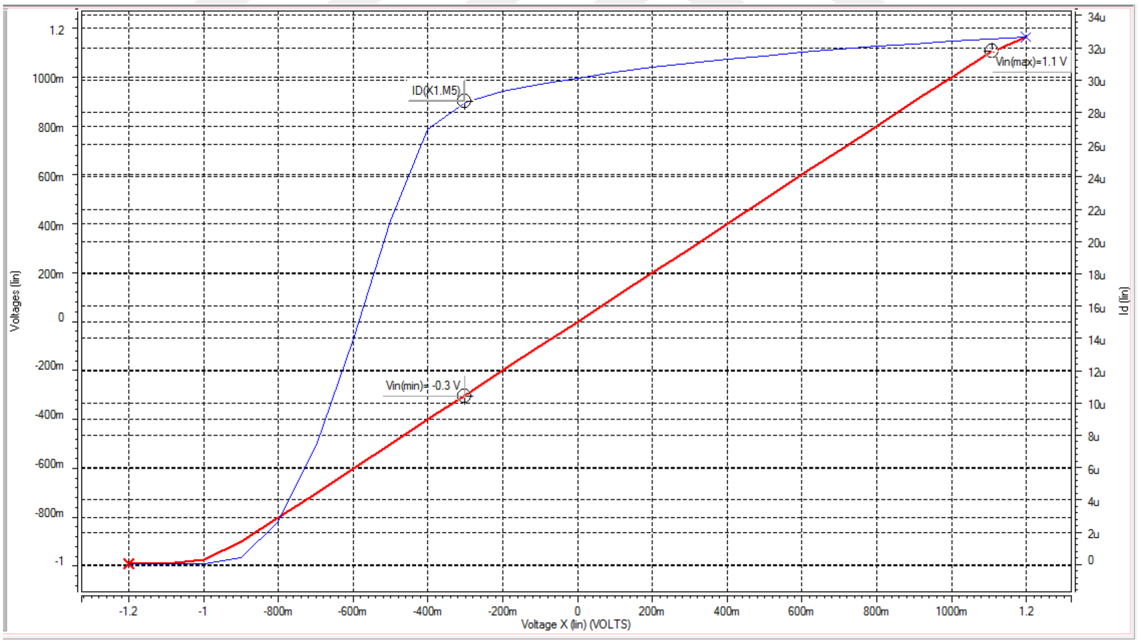
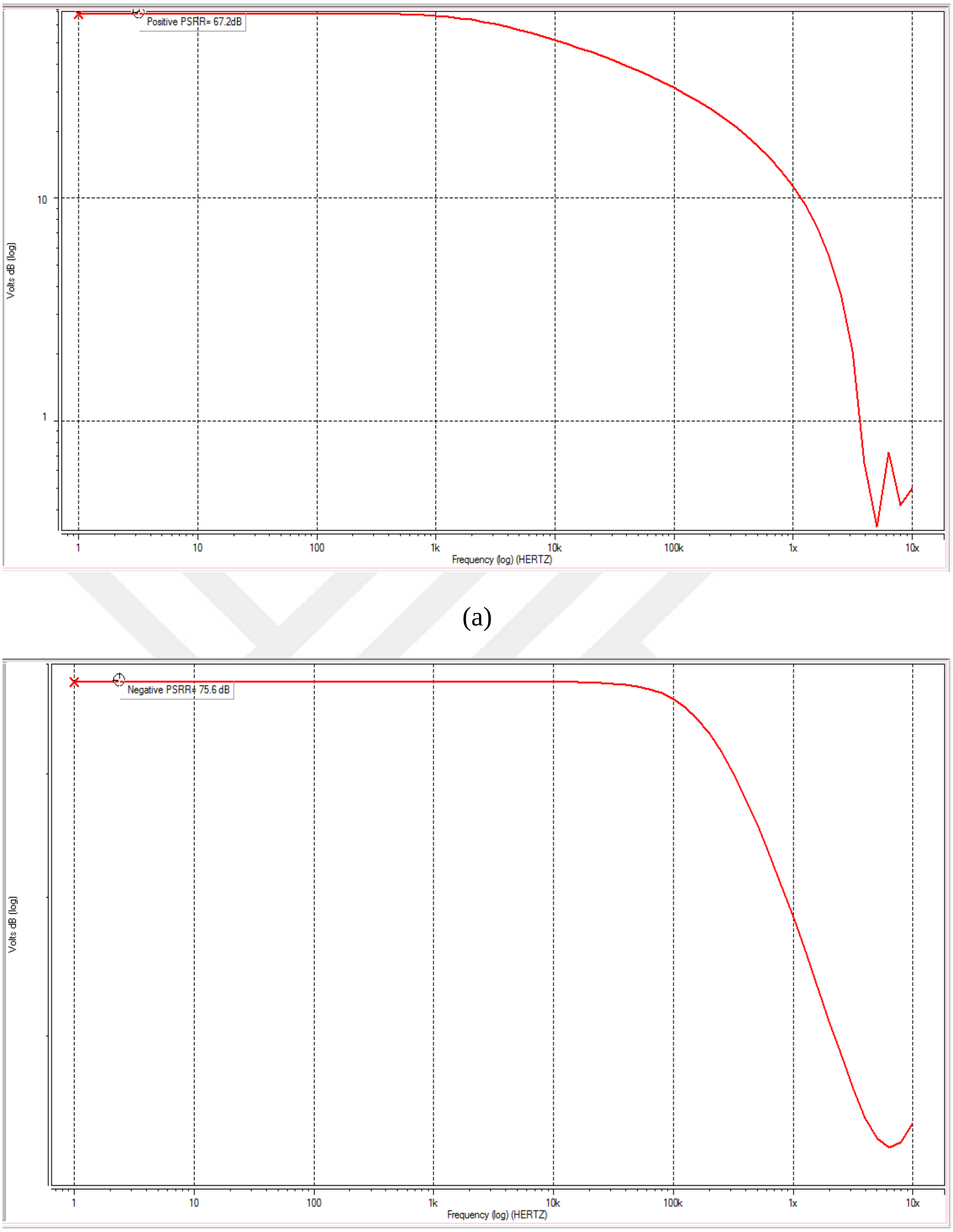


Figure 5.14 Input common-mode range voltage ICMR simulation result for the aged unbuffered two-stage CMOS Op-Amp circuit

Figure 5.15 shows the simulation results for positive power-supply rejection Ratio ($PSRR^{+}$) and negative power-supply rejection ratio ($PSRR^{-}$), both of $PSRR^{+}$ and $PSRR^{-}$ values have not changed which are found to be 67.2dB and 75.6dB, respectively.



(a)

(b)

Figure 5.15 Power-supply rejection ratio $PSRR$ simulation results for the aged unbuffered two-stage CMOS Op-Amp circuit. (a) Magnitude of $PSRR^{+}$. (b) Magnitude of $PSRR^{-}$.

We observed from our investigations on the simulation results of the unbuffered two-stage CMOS Op-Amp circuit's performance specifications that the degradation of this circuit's performance specifications induced by NBTI aging effects under different input voltage stress conditions are strongly depending on its open-loop mode and unity-gain mode and on its applications such as comparator and analog filter rather than the absolute dependence on the NBTI-induced threshold voltage $V_{th,p}$ degradation and consequently the degradations of the drain current I_D and the transconductance g_m of each pMOSFET transistor in the circuit. We observed that when the unbuffered two-stage CMOS Op-Amp circuit operates under different input voltage stress conditions in the open-loop and unity-gain configurations, only the positive slew rate SR^+ is slightly degraded where SR^+ reduced by 0.93%, whereas the other performance specifications of the unbuffered two-stage CMOS Op-Amp circuit such as A_v, GBW, the phase margin, the negative slew rate SR^- etc. are not degraded because of regardless of the NBTI-induced variations in the threshold voltages $V_{th,p}$ of pMOSFET transistors, the bias currents and the transconductances g_m in the unbuffered two-stage CMOS Op-Amp circuit are maintained at constant values through adjusting the gate-source voltages by biasing circuit which is utilized in the unbuffered two-stage CMOS Op-Amp circuit when NBTI-induced threshold voltage $V_{th,p}$ shifts occur. Table 5.4 shows the performance specifications of the aged unbuffered two-stage CMOS Op-Amp circuit for 10 years and also compare these specifications with performance specifications of the fresh unbuffered two-stage CMOS Op-Amp circuit.

Table 5.4 Comparison between the performance specifications of the aged and fresh unbuffered two-stage CMOS Op-Amp circuit

Design Specifications Names	**Specifications Values of the Fresh Circuit**	**Specifications Values of the Aged Circuit**
Gain	64.4dB	64.4dB
Unity Gain Bandwidth	3.44MHz	3.44MHz
Phase Margin	68°	68°
Slew Rate	$SR^+ = 8.681 V/us$, $SR^- = 3.712 V/us$	$SR^+ = 8.600 V/us$, $SR^- = 3.712 V/us$
$V_{in(min)}$	$-0.3V$	$-0.3V$
$V_{in(max)}$	$1.1V$	$1.1V$
CMRR	69.92dB	69.92dB

Table 5.4 (cont'd)

$PSRR^{+}$	67.2dB	67.2dB
$PSRR^{-}$	75.6dB	75.6dB
Load Capacitance	$10pF$	$10pF$
Power Dissipation	$258.79uW$	$258.79uW$
V_{DD}	$1.2V$	$1.2V$
V_{SS}	$-1.2V$	$-1.2V$
Settling time T_S	$244ns$	$244ns$
Input-offset Voltage V_{OS}	$351mV$	$351mV$
Output Voltage Swing	$-1.19V$-$1.17V$	$-1.19V$-$1.17V$

CHAPTER 6

CONCLUSION AND FUTURE WORK

In this thesis, the major issues of analog circuit reliability such as NBTI has been studied and the detailed analysis of the performance degradation of the unbuffered two-stage CMOS Op-Amp circuit resulting from a serious NBTI aging mechanism-induced threshold voltage V_{th} drift in pMOSFET transistors have been done. The circuit is designed by using 90 nm CMOS technology parameters. First, the physics of the degradation mechanisms including the BTI and HCI aging mechanisms have been explained. Then, the methodology to measure the amount of aging-induced degradation for each time step at the MOSFET transistor level and circuit level is described. For aging analysis, MOSFET model reliability analysis (MOSRA) in HSPICE is utilized. Using this procedure, the amount of NBTI-induced threshold voltage V_{th} degradation at the level of a single pMOSFET transistor and its impacts at the level of the unbuffered two-stage CMOS Op-Amp circuit performance specifications were investigated and analyzed based on the HSPICE MOSRA simulation results. Through the accurate observations of the NBTI-induced aging effect simulations results of a single pMOSFET transistor, it has been shown that the degradation in the threshold voltage V_{th} value is mainly dependent on the value of the applied gate-source stress voltage V_{GS} and on the stress time, and the larger degradation in the magnitude of the threshold voltage V_{th} has been occurred under the worst case stress voltage value $V_{GS} = V_{DS}$ for the pMOSFET transistor operation in the linear region. Finally, the unbuffered two-stage CMOS Op-Amp circuit, which was designed to meet all desired design specifications, has been simulated in order to investigate the degradation of the circuit's performance specifications resulting from the impact of NBTI-induced threshold voltage V_{th} degradation of each pMOSFET transistor in the circuit. It has been shown that there are no significant degradations occurred in the performance specifications of the unbuffered two-stage CMOS Op-Amp circuit resulting from NBTI-induced threshold voltage V_{th} variations of pMOSFET transistors in the circuit under different input voltage stress values in the open-loop and unity-gain configurations because of biasing currents and the transconductance g_m values are maintained at constant values through adjusting the gate-source voltages by biasing circuit. As a result, the degradations of the unbuffered two-stage CMOS Op-Amp circuit performance specifications resulting from the NBTI-induced threshold voltage V_{th} degradation are rather strongly dependent on its open-loop and unity-gain modes and on its applications than the absolute dependence on the NBTI-induced threshold voltage V_{th} degradation of each pMOSFET transistor in the circuit. The degradation in the positive slew rate SR^+ of the unbuffered two-stage CMOS Op-Amp circuit performance specifications resulting from the NBTI-induced threshold voltage V_{th} degradation must be taken into consideration during the design phase of the circuit by modifying the parameters of the circuit as needed in order to avoid the failure of the circuit over time in the future.

In the future, the proposed framework in this thesis can be extended to take into consideration the mapping of the other issues of analog circuit reliability than NBTI such as hot carrier injection (HCI) and time dependent dielectric breakdown (TDDB) at the level of MOSFET transistors in order to investigate and analysis their overall impact on the degradation of the unbuffered two-stage CMOS Op-Amp circuit performance specifications or at the level of the performance specifications of the analog circuits.

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APPENDIX-A

IMPORTANT MOSRA COMMANDS AND CONTROL OPTIONS

Some of the significant commands and control options and their descriptions which are used to execute of HSPICE MOSRA reliability analysis successfully are mentioned below.

- Command: “. MOSRA”

  Description: Initiates HCI and/or BTI analysis using two-phase simulation: the fresh simulation phase and the post-stress simulation phase.

  Syntax:

  ```
  .MOSRA RelTotalTime = time_value
  + [RelStartTime = time_value] [DEC = value] [LIN = value]
  + [RelStep = time_value] [RelMode = 0|1|2] SimMode = [0|1|2|3]
  + [AgingStart = time_value] [AgingStop = time_value]
  + [AgingPeriod = time_value] [AgingWidth = time_value]
  + [AgingInst = "inst_name"]
  + [Integmod = 0|1|2] [Xpolatemod = 0|1|2]
  + [Tsample1 = value] [Tsample2 = value]
  + [Agethreshold = value] [DegradationTime = value]
  + [MosraLlife = degradation_type_keyword] [DegF = value]
  + [DegFN = value] [DegFP = value]
  + [Frequency = value]
  + [hci = 0|1] [bti = 0|1] [tddb = 0|1]
  + [circuit_report = 0|1] [trelax = value] [area_scaling = value]
  ```

Example: the following syntax calculates the age of MOSFET transistor for 10 year with reliability time step of 1 year

```
.mosra reltotaltime='10*365*24*60*60'  relstep='1*365*24*60*60'
```

- Command: “ .MODEL”

  Description: used to define the user-defined MOSFET reliability model name, MOSRA model level and parameters.

  Syntax: .model mname mosra

  + Level | mosralevel = *value*

  + [*relmodelparam*]

  Example: .model PMOS1_ra mosra level=1

- Command: “.APPENDMODEL”

  Description: appends the parameter values from the source model card (SrcModel) to the destination model card (DestModel). Consequently, the parameters which used in the built-in MOSRA aging models like TITCE, TITTD, and TITFD etc. are appended to HSPICE and utilized during aging simulation.

  Syntax:

  .APPENDMODEL *SrcModel ModelKeyword1 DestModel ModelKeyword2*

  Example: .appendmodel PMOS1_ra mosra PMOS1 PMOS

- Command: “.OPTION MOSRASORT”

  Description: enables the descending sort of reliability degradation (RADEG) output. In the following example, this option does a descending sort for RADEG output on *delvth0*’s value.

  Syntax: .OPTION MOSRASORT=*degradation_type_keyword*

  Example: .option mosrasort=delvth0

- Command: “.OPTION RADEGFILE”

  Description: specifies a MOSRA degradation file name to be used with SIMMODE=1 (post-stress simulation only). HSPICE will read in the degradation information in the specified file and do a MOSRA post-stress simulation.

Syntax: .OPTION RADEGFILE = *file_name*

Example: .mosra reltotaltime='10*365*24*60*60' lin=11 simmode=1

.Option radegfile = '1.radeg0'

- Command: “.OPTION RADEGOUTPUT”

  Description: outputs the MOSRA degradation information to the Microsoft Excel CSV format.

  Syntax: .OPTION RADEGOUTPUT=CSV

APPENDIX-B

HSPICE INPUT FILES

Table B.1 HSPICE input file for simulation of the unbuffered two-stage CMOS Op-Amp circuit specifications in the open-loop configuration.

```
.OPTION POST PROBE SYMB=1
VIN+ 1 0 DC 0 AC 1.0
VDD 4 0 DC 1.2
VSS 0 5 DC 1.2
VIN- 2 0 DC 0
CL 3 0 10P
X1 1 2 3 4 5 OPAMP
.SUBCKT OPAMP 1 2 6 8 9
M1 4 2 3 3 NMOS1 W=0.27500E-06 L=0.50000E-06
M2 5 1 3 3 NMOS1 W=0.27500E-06 L=0.50000E-06
M3 4 4 8 8 PMOS1 W=16.33000E-06 L=0.50000E-06
M4 5 4 8 8 PMOS1 W=16.33000E-06 L=0.50000E-06
M5 3 7 9 9 NMOS1 W=3.86950E-06 L=0.50000E-06
M6 6 5 8 8 PMOS1 W=48.27000E-06 L=0.50000E-06
M7 6 7 9 9 NMOS1 W=5.71900E-06 L=0.50000E-06
M8 7 7 9 9 NMOS1 W=3.86950E-06 L=0.50000E-06
CC 5 6 3.0P
.MODEL NMOS1 NMOS
+ LEVEL = 5.40000E+01 VERSION = 4.20000E+00 BINUNIT = 1.00000E+00
+ PARAMCHK = 0.00000E+00 MOBMOD = 0.00000E+00 CAPMOD = 2.00000E+00
+ RDSMOD = 0.00000E+00 IGCMOD = 1.00000E+00 IGBMOD = 1.00000E+00
+ FNOIMOD = 1.00000E+00 TNOIMOD = 0.00000E+00 DIOMOD = 1.00000E+00
+ PERMOD = 0.00000E+00 TOXE = 2.30000E-09 TOXP = 1.92000E-09
```

```
+ EPSROX = 3.90000E+00 XJ = 8.00000E-08 NDEP = 1.60000E+18
+ NGATE = 2.00000E+20 NSD = 1.00000E+20 VTH0 = 2.79572E-01
+ K1 = 2.82928E-01 K2 = -1.03648E-02 K3 = -2.55690E+00
+ K3B = 1.17310E+00 W0 = 1.00000E-10 VFB = -1.00000E+00
+ PHIN = 0.00000E+00 LPE0 = 1.20898E-07 LPEB = 3.26229E-08
+ DVT0 = 6.74408E-03 DVT1 = 3.23649E-02 DVT2 = -1.61846E-02
+ DVTP0 = 0.00000E+00 DVTP1 = 0.00000E+00 DVT0W = -1.26693E-01
+ DVT1W = 8.61226E+05 DVT2W = 1.96959E-01 U0 = 3.58576E+02
+ UA = 0.00000E+00 UB = 1.86125E-18 UC = 1.60862E-10
+ EU = 1.67000E+00 VSAT = 1.35800E+05 A0 = 1.67233E+00
+ AGS = 8.89796E-01 B0 = -2.00000E-08 B1 = 0.00000E+00
+ KETA = -6.30471E-02 A1 = 0.00000E+00 A2 = 1.00000E+00
+ RDSW = 1.40444E+02 RDSWMIN = 2.17931E+00 PRWB = 1.04000E-01
+ PRWG = -1.14651E-01 WR = 1.00000E+00 WINT = 1.26879E-08
+ LINT = 5.50000E-09 DWG = -9.55519E-10 DWB = 0.00000E+00
+ VOFF = -6.11435E-02 VOFFL = 0.00000E+00 MINV = 2.80000E+00
+ NFACTOR = 4.00000E-01 ETA0 = 6.32663E-04 ETAB = -1.55000E-04
+ DSUB = 3.13217E-02 CIT = 9.00000E-04 CDSC = 4.02133E-05
+ CDSCB = 2.41457E-05 CDSCD = 0.00000E+00 PCLM = 2.07565E+00
+ PDIBLC1 = 5.15347E-06 PDIBLC2 = 5.24808E-04 PDIBLCB = -7.05723E-01
+ DROUT = 2.90945E-02 PSCBE1 = 7.50025E+08 PSCBE2 = 3.70361E-07
+ PVAG = 1.50000E+01 DELTA = 7.37000E-03 ALPHA0 = 3.00000E-11
+ ALPHA1 = 0.00000E+00 BETA0 = 3.80000E+00 AGIDL = 2.43759E-08
+ BGIDL = 1.95095E+09 CGIDL = 5.00000E-01 EGIDL = 2.56798E-01
+ RSH = 0.00000E+00 FPROUT = 0.00000E+00 PDITS = 0.00000E+00
+ PDITSL = 0.00000E+00 PDITSD = 2.60000E-01 JSS = 1.56388E-07
+ JSWS = 1.07166E-13 JSWGS = 2.53515E-13 IJTHSREV = 1.00000E-01
+ IJTHSFWD = 1.00000E-01 XJBVS = 1.00000E+00 BVS = 1.00000E+01
+ AIGBACC = 1.30106E-02 BIGBACC = 3.80785E-03 CIGBACC = 2.21617E-01
+ NIGBACC = 4.00000E+00 AIGBINV = 1.91321E-02 BIGBINV = 6.35793E-03
+ CIGBINV = 1.49880E-03 EIGBINV = 2.01293E-03 NIGBINV = 1.00000E+00
+ AIGC = 1.05435E-02 BIGC = 1.63743E-03 CIGC = 4.57381E-02
+ AIGSD = 8.90242E-03 BIGSD = 1.00000E-06 CIGSD = 2.06887E-02
+ DLCIG = 5.00000E-09 NIGC = 1.72466E+00 POXEDGE = 1.00000E+00
+ PIGCD = 1.00000E+00 NTOX = 1.00000E+00 TOXREF = 2.30000E-09
```

```
+ XPART = 0.00000E+00 CGSO = 1.42000E-10 CGDO = 1.42000E-10
+ CGBO = 0.00000E+00 CJS = 1.00000E-03 MJS = 3.23722E-01
+ MJSWS = 1.00000E-01 CJSWS = 5.21900E-11 CJSWGS = 2.10400E-10
+ MJSWGS = 7.00000E-01 PBSWS = 1.00000E+00 PBS = 6.98994E-01
+ PBSWGS = 5.50000E-01 CGSL = 8.00000E-11 CGDL = 8.00000E-11
+ CKAPPAS = 6.00000E-01 CF = 1.20000E-10 CLC = 1.00000E-07
+ CLE = 6.00000E-01 DLC = 2.30000E-08 DWC = 1.26879E-08
+ VFBCV = -1.00000E+00 NOFF = 2.10000E+00 VOFFCV = -3.00000E-02
+ ACDE = 1.00000E+00 MOIN = 7.00000E+00 WL = -8.07124E-21
+ WLN = 9.72043E-01 WW = 1.00000E-16 WWN = 1.10000E+00
+ WWL = -2.10000E-23 LL = 5.00000E-16 LLN = 1.00000E+00
+ LW = 2.63398E-16 LWN = 1.19880E+00 LWL = -2.49331E-23
+ TNOM = 2.50000E+01 UTE = -1.20000E+00 KT1 = -2.05642E-01
+ KT1L = 4.00000E-10 KT2 = -3.50186E-02 UA1 = 1.68569E-09
+ UB1 = -1.32806E-18 UC1 = -4.00000E-11 AT = 1.00000E+03
+ PRT = -5.00000E+01 NJS = 1.05000E+00 XTIS = 3.00000E+00
+ TPB = 1.50000E-03 TPBSW = 2.00000E-03 TPBSWG = 1.20000E-03
+ TCJ = 9.00000E-04 TCJSW = 7.00000E-04 TCJSWG = 6.00000E-04
+ NOIA = 1.00000E+20 NOIB = 5.00000E+04 NOIC = -1.40000E-12
+ EM = 4.10000E+07 AF = 1.00000E+00 EF = 1.00000E+00
+ KF = 0.00000E+00 NTNOI = 1.00000E+00 TNOIA = 1.50000E+00
+ TNOIB = 3.50000E+00 LMIN = 8.00000E-08 LMAX = 1.00000E-05
+ WMIN = 1.20000E-07 WMAX = 1.00000E+00
+ LLC = 0.00000E+00 WLC = 0.00000E+00 LWC = 0.00000E+00
+ WWC = 0.00000E+00 LWLC = 0.00000E+00 WWLC = 0.00000E+00
+ PVSAT = -2.76718E+01
+ PPVAG = -5.91262E-02 LK3 = -7.01570E-01 LPVAG = -4.50007E-01
+ XL = 0.00000E+00 XW = 0.00000E+00 PU0 = -2.62732E-01
+ PUB = -1.06728E-20
.MODEL PMOS1 PMOS
+ LEVEL = 5.40000E+01 VERSION = 4.20000E+00 BINUNIT = 1.00000E+00
+ PARAMCHK = 0.00000E+00 MOBMOD = 0.00000E+00 CAPMOD = 2.00000E+00
+ RDSMOD = 0.00000E+00 IGCMOD = 1.00000E+00 IGBMOD = 1.00000E+00
+ FNOIMOD = 1.00000E+00 TNOIMOD = 0.00000E+00 DIOMOD = 1.00000E+00
+ PERMOD = 0.00000E+00 TOXE = 2.40000E-09 TOXP = 1.98000E-09
```

```
+ EPSROX = 3.90000E+00 XJ = 8.00000E-08 NDEP = 5.20000E+17
+ NGATE = 1.40000E+20 NSD = 1.00000E+20 VTH0 = -2.85479E-01
+ K1 = 3.17233E-01 K2 = -8.76234E-03 K3 = 3.08981E-01
+ K3B = 8.70132E-01 W0 = 6.57581E-10 VFB = -1.00000E+00
+ PHIN = 0.00000E+00 LPE0 = 7.46456E-08 LPEB = -1.50000E-08
+ DVT0 = 1.12021E-02 DVT1 = 2.92015E-02 DVT2 = -5.01808E-02
+ DVTP0 = 0.00000E+00 DVTP1 = 0.00000E+00 DVT0W = 3.23543E-01
+ DVT1W = 8.32111E+05 DVT2W = 1.65532E-01 U0 = 7.21140E+01
+ UA = 1.59639E-12 UB = 1.06685E-18 UC = -2.40118E-11
+ EU = 1.67000E+00 VSAT = 1.99000E+05 A0 = 2.50000E+00
+ AGS = 9.03713E-01 B0 = 6.03511E-08 B1 = 6.14485E-07
+ KETA = -2.00471E-02 A1 = 0.00000E+00 A2 = 1.00000E+00
+ RDSW = 9.25230E+01 RDSWMIN = 1.66186E+00 PRWB = -1.00000E-01
+ PRWG = -3.87950E-02 WR = 1.00000E+00 WINT = -1.40000E-08
+ LINT = 4.05000E-09 DWG = -9.55519E-10 DWB = 0.00000E+00
+ VOFF = -6.11435E-02 VOFFL = 0.00000E+00 MINV = 1.00000E+00
+ NFACTOR = 4.00000E-01 ETA0 = 2.71789E-04 ETAB = -7.00000E-05
+ DSUB = 1.76962E-02 CIT = 9.00000E-04 CDSC = 4.20827E-05
+ CDSCB = 3.90335E-05 CDSCD = 2.06172E-06 PCLM = 1.00000E-01
+ PDIBLC1 = 2.23872E-07 PDIBLC2 = 5.24808E-04 PDIBLCB = -7.05723E-01
+ DROUT = 7.73693E-01 PSCBE1 = 7.50025E+08 PSCBE2 = 3.70361E-07
+ PVAG = 1.50000E+01 DELTA = 1.17000E-02 ALPHA0 = 3.57396E-10
+ ALPHA1 = 0.00000E+00 BETA0 = 9.58015E+00 AGIDL = 2.08400E-08
+ BGIDL = 2.22154E+09 CGIDL = 3.88392E-01 EGIDL = 2.95809E-01
+ RSH = 0.00000E+00 FPROUT = 0.00000E+00 PDITS = 3.80000E-01
+ PDITSL = 7.20000E+05 PDITSD = 4.14448E-01 JSS = 7.09895E-08
+ JSWS = 2.16035E-14 JSWGS = 3.29856E-14 IJTHSREV = 1.00000E-01
+ IJTHSFWD = 1.00000E-01 XJBVS = 1.00000E+00 BVS = 1.00000E+01
+ AIGBACC = 1.10487E-02 BIGBACC = 4.89185E-03 CIGBACC = 4.37154E-01
+ NIGBACC = 4.00000E+00 AIGBINV = 1.69834E-02 BIGBINV = 5.94953E-03
+ CIGBINV = 1.17277E-03 EIGBINV = 1.34560E-06 NIGBINV = 1.00000E+00
+ AIGC = 6.56697E-03 BIGC = 9.26824E-04 CIGC = 5.31466E-02
+ AIGSD = 5.05243E-03 BIGSD = 9.99952E-07 CIGSD = 2.06845E-02
+ DLCIG = 5.00000E-09 NIGC = 3.09099E-01 POXEDGE = 1.00000E+00
+ PIGCD = 1.00000E+00 NTOX = 1.00000E+00 TOXREF = 2.45000E-09
```

```
+ XPART = 1.00000E+00 CGSO = 1.40000E-10 CGDO = 1.40000E-10
+ CGBO = 0.00000E+00 CJS = 1.00000E-03 MJS = 4.14311E-01
+ MJSWS = 2.54709E-01 CJSWS = 8.14000E-11 CJSWGS = 4.20000E-10
+ MJSWGS = 6.00000E-01 PBSWS = 5.05350E-01 PBS = 7.69082E-01
+ PBSWGS = 9.29453E-01 CGSL = 9.50000E-11 CGDL = 9.50000E-11
+ CKAPPAS = 5.00000E-01 CF = 1.20000E-10 CLC = 1.00000E-07
+ CLE = 6.00000E-01 DLC = 2.45000E-08 DWC = -1.40000E-08
+ VFBCV = -1.00000E+00 NOFF = 2.10000E+00 VOFFCV = -3.00000E-02
+ ACDE = 1.00000E+00 MOIN = 7.00000E+00 WL = 2.50325E-19
+ WLN = 9.21748E-01 WW = 0.00000E+00 WWN = 1.00000E+00
+ WWL = 6.45309E-24 LL = 4.00000E-16 LLN = 1.00000E+00
+ LW = -1.36171E-14 LWN = 9.70905E-01 LWL = 7.86145E-22
+ TNOM = 2.50000E+01 UTE = -1.00000E+00 KT1 = -2.75642E-01
+ KT1L = -1.00000E-09 KT2 = -3.50186E-02 UA1 = 1.05958E-09
+ UB1 = -1.68375E-18 UC1 = -2.31906E-11 AT = 1.00000E+03
+ PRT = -7.20000E+01 NJS = 1.00000E+00 XTIS = 3.00000E+00
+ TPB = 1.00000E-03 TPBSW = 5.00000E-04 TPBSWG = 1.00000E-04
+ TCJ = 8.50000E-04 TCJSW = 1.00000E-03 TCJSWG = 1.00000E-04
+ NOIA = 1.00000E+20 NOIB = 5.00000E+04 NOIC = -1.40000E-12
+ EM = 4.10000E+07 AF = 1.00000E+00 EF = 1.00000E+00
+ KF = 0.00000E+00 NTNOI = 1.00000E+00 TNOIA = 1.50000E+00
+ TNOIB = 3.50000E+00 LMIN = 8.00000E-08 LMAX = 1.00000E-05
+ WMIN = 1.20000E-07 WMAX = 1.00000E+00
+ LLC = 0.00000E+00 WLC = 0.00000E+00 LWC = 0.00000E+00
+ WWC = 0.00000E+00 LWLC = 0.00000E+00 WWLC = 0.00000E+00
+ LLPE0 = 9.40000E-09
+ PVSAT = 5.35918E+02 LKETA = 1.00000E-03 LK3 = 1.02690E+00
+ LPCLM = 0.00000E+00 XL = 0.00000E+00 XW = 0.00000E+00
+ PU0 = -3.75073E-02 PUB = 6.29168E-21
IBIAS 8 7 30U
.ENDS
.OP
.TF V(3) VIN+
.DC VIN+ -0.005 0.005 100U
.PRINT DC V(3)
```

```
.TRAN 0.05U 3U
.PRINT TRAN V(3) V(1)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
.END
```

Table B.2 HSPICE input file for simulation of the unbuffered two-Stage CMOS Op-Amp circuit specifications in the unity-gain configuration.

```
.OPTION POST PROBE SYMB=1
VIN+ 1 0 PULSE (0 1.2 0 1NS 1NS 1.5US 3US)
VDD 4 0 DC 1.2 AC 1.0
VSS 0 5 DC 1.2
CL 3 0 10P
X1 1 3 3 4 5 OPAMP
.SUBCKT OPAMP 1 2 6 8 9
M1 4 2 3 3 NMOS1 W=0.27500E-06 L=0.50000E-06
M2 5 1 3 3 NMOS1 W=0.27500E-06 L=0.50000E-06
M3 4 4 8 8 PMOS1 W=16.33000E-06 L=0.50000E-06
M4 5 4 8 8 PMOS1 W=16.33000E-06 L=0.50000E-06
M5 3 7 9 9 NMOS1 W=3.86950E-06 L=0.50000E-06
M6 6 5 8 8 PMOS1 W=48.27000E-06 L=0.50000E-06
M7 6 7 9 9 NMOS1 W=5.71900E-06 L=0.50000E-06
M8 7 7 9 9 NMOS1 W=3.86950E-06 L=0.50000E-06
CC 5 6 3.0P
.MODEL NMOS1 NMOS
+ LEVEL = 5.40000E+01 VERSION = 4.20000E+00 BINUNIT = 1.00000E+00
+ PARAMCHK = 0.00000E+00 MOBMOD = 0.00000E+00 CAPMOD = 2.00000E+00
+ RDSMOD = 0.00000E+00 IGCMOD = 1.00000E+00 IGBMOD = 1.00000E+00
+ FNOIMOD = 1.00000E+00 TNOIMOD = 0.00000E+00 DIOMOD = 1.00000E+00
+ PERMOD = 0.00000E+00 TOXE = 2.30000E-09 TOXP = 1.92000E-09
+ EPSROX = 3.90000E+00 XJ = 8.00000E-08 NDEP = 1.60000E+18
+ NGATE = 2.00000E+20 NSD = 1.00000E+20 VTH0 = 2.79572E-01
+ K1 = 2.82928E-01 K2 = -1.03648E-02 K3 = -2.55690E+00
```

```
+ K3B = 1.17310E+00 W0 = 1.00000E-10 VFB = -1.00000E+00
+ PHIN = 0.00000E+00 LPE0 = 1.20898E-07 LPEB = 3.26229E-08
+ DVT0 = 6.74408E-03 DVT1 = 3.23649E-02 DVT2 = -1.61846E-02
+ DVTP0 = 0.00000E+00 DVTP1 = 0.00000E+00 DVT0W = -1.26693E-01
+ DVT1W = 8.61226E+05 DVT2W = 1.96959E-01 U0 = 3.58576E+02
+ UA = 0.00000E+00 UB = 1.86125E-18 UC = 1.60862E-10
+ EU = 1.67000E+00 VSAT = 1.35800E+05 A0 = 1.67233E+00
+ AGS = 8.89796E-01 B0 = -2.00000E-08 B1 = 0.00000E+00
+ KETA = -6.30471E-02 A1 = 0.00000E+00 A2 = 1.00000E+00
+ RDSW = 1.40444E+02 RDSWMIN = 2.17931E+00 PRWB = 1.04000E-01
+ PRWG = -1.14651E-01 WR = 1.00000E+00 WINT = 1.26879E-08
+ LINT = 5.50000E-09 DWG = -9.55519E-10 DWB = 0.00000E+00
+ VOFF = -6.11435E-02 VOFFL = 0.00000E+00 MINV = 2.80000E+00
+ NFACTOR = 4.00000E-01 ETA0 = 6.32663E-04 ETAB = -1.55000E-04
+ DSUB = 3.13217E-02 CIT = 9.00000E-04 CDSC = 4.02133E-05
+ CDSCB = 2.41457E-05 CDSCD = 0.00000E+00 PCLM = 2.07565E+00
+ PDIBLC1 = 5.15347E-06 PDIBLC2 = 5.24808E-04 PDIBLCB = -7.05723E-01
+ DROUT = 2.90945E-02 PSCBE1 = 7.50025E+08 PSCBE2 = 3.70361E-07
+ PVAG = 1.50000E+01 DELTA = 7.37000E-03 ALPHA0 = 3.00000E-11
+ ALPHA1 = 0.00000E+00 BETA0 = 3.80000E+00 AGIDL = 2.43759E-08
+ BGIDL = 1.95095E+09 CGIDL = 5.00000E-01 EGIDL = 2.56798E-01
+ RSH = 0.00000E+00 FPROUT = 0.00000E+00 PDITS = 0.00000E+00
+ PDITSL = 0.00000E+00 PDITSD = 2.60000E-01 JSS = 1.56388E-07
+ JSWS = 1.07166E-13 JSWGS = 2.53515E-13 IJTHSREV = 1.00000E-01
+ IJTHSFWD = 1.00000E-01 XJBVS = 1.00000E+00 BVS = 1.00000E+01
+ AIGBACC = 1.30106E-02 BIGBACC = 3.80785E-03 CIGBACC = 2.21617E-01
+ NIGBACC = 4.00000E+00 AIGBINV = 1.91321E-02 BIGBINV = 6.35793E-03
+ CIGBINV = 1.49880E-03 EIGBINV = 2.01293E-03 NIGBINV = 1.00000E+00
+ AIGC = 1.05435E-02 BIGC = 1.63743E-03 CIGC = 4.57381E-02
+ AIGSD = 8.90242E-03 BIGSD = 1.00000E-06 CIGSD = 2.06887E-02
+ DLCIG = 5.00000E-09 NIGC = 1.72466E+00 POXEDGE = 1.00000E+00
+ PIGCD = 1.00000E+00 NTOX = 1.00000E+00 TOXREF = 2.30000E-09
+ XPART = 0.00000E+00 CGSO = 1.42000E-10 CGDO = 1.42000E-10
+ CGBO = 0.00000E+00 CJS = 1.00000E-03 MJS = 3.23722E-01
+ MJSWS = 1.00000E-01 CJSWS = 5.21900E-11 CJSWGS = 2.10400E-10
```

```
+ MJSWGS = 7.00000E-01 PBSWS = 1.00000E+00 PBS = 6.98994E-01
+ PBSWGS = 5.50000E-01 CGSL = 8.00000E-11 CGDL = 8.00000E-11
+ CKAPPAS = 6.00000E-01 CF = 1.20000E-10 CLC = 1.00000E-07
+ CLE = 6.00000E-01 DLC = 2.30000E-08 DWC = 1.26879E-08
+ VFBCV = -1.00000E+00 NOFF = 2.10000E+00 VOFFCV = -3.00000E-02
+ ACDE = 1.00000E+00 MOIN = 7.00000E+00 WL = -8.07124E-21
+ WLN = 9.72043E-01 WW = 1.00000E-16 WWN = 1.10000E+00
+ WWL = -2.10000E-23 LL = 5.00000E-16 LLN = 1.00000E+00
+ LW = 2.63398E-16 LWN = 1.19880E+00 LWL = -2.49331E-23
+ TNOM = 2.50000E+01 UTE = -1.20000E+00 KT1 = -2.05642E-01
+ KT1L = 4.00000E-10 KT2 = -3.50186E-02 UA1 = 1.68569E-09
+ UB1 = -1.32806E-18 UC1 = -4.00000E-11 AT = 1.00000E+03
+ PRT = -5.00000E+01 NJS = 1.05000E+00 XTIS = 3.00000E+00
+ TPB = 1.50000E-03 TPBSW = 2.00000E-03 TPBSWG = 1.20000E-03
+ TCJ = 9.00000E-04 TCJSW = 7.00000E-04 TCJSWG = 6.00000E-04
+ NOIA = 1.00000E+20 NOIB = 5.00000E+04 NOIC = -1.40000E-12
+ EM = 4.10000E+07 AF = 1.00000E+00 EF = 1.00000E+00
+ KF = 0.00000E+00 NTNOI = 1.00000E+00 TNOIA = 1.50000E+00
+ TNOIB = 3.50000E+00 LMIN = 8.00000E-08 LMAX = 1.00000E-05
+ WMIN = 1.20000E-07 WMAX = 1.00000E+00
+ LLC = 0.00000E+00 WLC = 0.00000E+00 LWC = 0.00000E+00
+ WWC = 0.00000E+00 LWLC = 0.00000E+00 WWLC = 0.00000E+00
+ PVSAT = -2.76718E+01
+ PPVAG = -5.91262E-02 LK3 = -7.01570E-01 LPVAG = -4.50007E-01
+ XL = 0.00000E+00 XW = 0.00000E+00 PU0 = -2.62732E-01
+ PUB = -1.06728E-20
.MODEL PMOS1 PMOS
+ LEVEL = 5.40000E+01 VERSION = 4.20000E+00 BINUNIT = 1.00000E+00
+ PARAMCHK = 0.00000E+00 MOBMOD = 0.00000E+00 CAPMOD = 2.00000E+00
+ RDSMOD = 0.00000E+00 IGCMOD = 1.00000E+00 IGBMOD = 1.00000E+00
+ FNOIMOD = 1.00000E+00 TNOIMOD = 0.00000E+00 DIOMOD = 1.00000E+00
+ PERMOD = 0.00000E+00 TOXE = 2.40000E-09 TOXP = 1.98000E-09
+ EPSROX = 3.90000E+00 XJ = 8.00000E-08 NDEP = 5.20000E+17
+ NGATE = 1.40000E+20 NSD = 1.00000E+20 VTH0 = -2.85479E-01
+ K1 = 3.17233E-01 K2 = -8.76234E-03 K3 = 3.08981E-01
```

```
+ K3B = 8.70132E-01 W0 = 6.57581E-10 VFB = -1.00000E+00
+ PHIN = 0.00000E+00 LPE0 = 7.46456E-08 LPEB = -1.50000E-08
+ DVT0 = 1.12021E-02 DVT1 = 2.92015E-02 DVT2 = -5.01808E-02
+ DVTP0 = 0.00000E+00 DVTP1 = 0.00000E+00 DVT0W = 3.23543E-01
+ DVT1W = 8.32111E+05 DVT2W = 1.65532E-01 U0 = 7.21140E+01
+ UA = 1.59639E-12 UB = 1.06685E-18 UC = -2.40118E-11
+ EU = 1.67000E+00 VSAT = 1.99000E+05 A0 = 2.50000E+00
+ AGS = 9.03713E-01 B0 = 6.03511E-08 B1 = 6.14485E-07
+ KETA = -2.00471E-02 A1 = 0.00000E+00 A2 = 1.00000E+00
+ RDSW = 9.25230E+01 RDSWMIN = 1.66186E+00 PRWB = -1.00000E-01
+ PRWG = -3.87950E-02 WR = 1.00000E+00 WINT = -1.40000E-08
+ LINT = 4.05000E-09 DWG = -9.55519E-10 DWB = 0.00000E+00
+ VOFF = -6.11435E-02 VOFFL = 0.00000E+00 MINV = 1.00000E+00
+ NFACTOR = 4.00000E-01 ETA0 = 2.71789E-04 ETAB = -7.00000E-05
+ DSUB = 1.76962E-02 CIT = 9.00000E-04 CDSC = 4.20827E-05
+ CDSCB = 3.90335E-05 CDSCD = 2.06172E-06 PCLM = 1.00000E-01
+ PDIBLC1 = 2.23872E-07 PDIBLC2 = 5.24808E-04 PDIBLCB = -7.05723E-01
+ DROUT = 7.73693E-01 PSCBE1 = 7.50025E+08 PSCBE2 = 3.70361E-07
+ PVAG = 1.50000E+01 DELTA = 1.17000E-02 ALPHA0 = 3.57396E-10
+ ALPHA1 = 0.00000E+00 BETA0 = 9.58015E+00 AGIDL = 2.08400E-08
+ BGIDL = 2.22154E+09 CGIDL = 3.88392E-01 EGIDL = 2.95809E-01
+ RSH = 0.00000E+00 FPROUT = 0.00000E+00 PDITS = 3.80000E-01
+ PDITSL = 7.20000E+05 PDITSD = 4.14448E-01 JSS = 7.09895E-08
+ JSWS = 2.16035E-14 JSWGS = 3.29856E-14 IJTHSREV = 1.00000E-01
+ IJTHSFWD = 1.00000E-01 XJBVS = 1.00000E+00 BVS = 1.00000E+01
+ AIGBACC = 1.10487E-02 BIGBACC = 4.89185E-03 CIGBACC = 4.37154E-01
+ NIGBACC = 4.00000E+00 AIGBINV = 1.69834E-02 BIGBINV = 5.94953E-03
+ CIGBINV = 1.17277E-03 EIGBINV = 1.34560E-06 NIGBINV = 1.00000E+00
+ AIGC = 6.56697E-03 BIGC = 9.26824E-04 CIGC = 5.31466E-02
+ AIGSD = 5.05243E-03 BIGSD = 9.99952E-07 CIGSD = 2.06845E-02
+ DLCIG = 5.00000E-09 NIGC = 3.09099E-01 POXEDGE = 1.00000E+00
+ PIGCD = 1.00000E+00 NTOX = 1.00000E+00 TOXREF = 2.45000E-09
+ XPART = 1.00000E+00 CGSO = 1.40000E-10 CGDO = 1.40000E-10
+ CGBO = 0.00000E+00 CJS = 1.00000E-03 MJS = 4.14311E-01
+ MJSWS = 2.54709E-01 CJSWS = 8.14000E-11 CJSWGS = 4.20000E-10
```

```
+ MJSWGS = 6.00000E-01 PBSWS = 5.05350E-01 PBS = 7.69082E-01
+ PBSWGS = 9.29453E-01 CGSL = 9.50000E-11 CGDL = 9.50000E-11
+ CKAPPAS = 5.00000E-01 CF = 1.20000E-10 CLC = 1.00000E-07
+ CLE = 6.00000E-01 DLC = 2.45000E-08 DWC = -1.40000E-08
+ VFBCV = -1.00000E+00 NOFF = 2.10000E+00 VOFFCV = -3.00000E-02
+ ACDE = 1.00000E+00 MOIN = 7.00000E+00 WL = 2.50325E-19
+ WLN = 9.21748E-01 WW = 0.00000E+00 WWN = 1.00000E+00
+ WWL = 6.45309E-24 LL = 4.00000E-16 LLN = 1.00000E+00
+ LW = -1.36171E-14 LWN = 9.70905E-01 LWL = 7.86145E-22
+ TNOM = 2.50000E+01 UTE = -1.00000E+00 KT1 = -2.75642E-01
+ KT1L = -1.00000E-09 KT2 = -3.50186E-02 UA1 = 1.05958E-09
+ UB1 = -1.68375E-18 UC1 = -2.31906E-11 AT = 1.00000E+03
+ PRT = -7.20000E+01 NJS = 1.00000E+00 XTIS = 3.00000E+00
+ TPB = 1.00000E-03 TPBSW = 5.00000E-04 TPBSWG = 1.00000E-04
+ TCJ = 8.50000E-04 TCJSW = 1.00000E-03 TCJSWG = 1.00000E-04
+ NOIA = 1.00000E+20 NOIB = 5.00000E+04 NOIC = -1.40000E-12
+ EM = 4.10000E+07 AF = 1.00000E+00 EF = 1.00000E+00
+ KF = 0.00000E+00 NTNOI = 1.00000E+00 TNOIA = 1.50000E+00
+ TNOIB = 3.50000E+00 LMIN = 8.00000E-08 LMAX = 1.00000E-05
+ WMIN = 1.20000E-07 WMAX = 1.00000E+00
+ LLC = 0.00000E+00 WLC = 0.00000E+00 LWC = 0.00000E+00
+ WWC = 0.00000E+00 LWLC = 0.00000E+00 WWLC = 0.00000E+00
+ LLPE0 = 9.40000E-09
+ PVSAT = 5.35918E+02 LKETA = 1.00000E-03 LK3 = 1.02690E+00
+ LPCLM = 0.00000E+00 XL = 0.00000E+00 XW = 0.00000E+00
+ PU0 = -3.75073E-02 PUB = 6.29168E-21
IBIAS 8 7 30U
.ENDS
.DC VIN+ -1.2 1.2 0.1
.PRINT DC V(3) ID(X1.M5)
.PROBE DC V(3) ID(X1.M5)
.TRAN 0.05U 3U
.PRINT TRAN V(3) V(1)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
```

```
.PROBE AC VDB(3) VP(3)
.END
```

Table B.3 HSPICE MOSRA input file for simulation of the NBTI aging impact on the aged unbuffered two-stage CMOS Op-Amp circuit specifications in the open-loop configuration.

```
.OPTION POST PROBE APPENDALL SYMB=1
VIN+ 1 0 DC 0 AC 1.0
VDD 4 0 DC 1.2
VSS 0 5 DC 1.2
VIN- 2 0 DC 0
CL 3 0 10P
X1 1 2 3 4 5 OPAMP
.SUBCKT OPAMP 1 2 6 8 9
M1 4 2 3 3 NMOS1 W=0.27500E-06 L=0.50000E-06
M2 5 1 3 3 NMOS1 W=0.27500E-06 L=0.50000E-06
M3 4 4 8 8 PMOS1 W=16.33000E-06 L=0.50000E-06
M4 5 4 8 8 PMOS1 W=16.33000E-06 L=0.50000E-06
M5 3 7 9 9 NMOS1 W=3.86950E-06 L=0.50000E-06
M6 6 5 8 8 PMOS1 W=48.27000E-06 L=0.50000E-06
M7 6 7 9 9 NMOS1 W=5.71900E-06 L=0.50000E-06
M8 7 7 9 9 NMOS1 W=3.86950E-06 L=0.50000E-06
CC 5 6 3.0P
.MODEL NMOS1 NMOS
+ LEVEL = 5.40000E+01 VERSION = 4.20000E+00 BINUNIT = 1.00000E+00
+ PARAMCHK = 0.00000E+00 MOBMOD = 0.00000E+00 CAPMOD = 2.00000E+00
+ RDSMOD = 0.00000E+00 IGCMOD = 1.00000E+00 IGBMOD = 1.00000E+00
+ FNOIMOD = 1.00000E+00 TNOIMOD = 0.00000E+00 DIOMOD = 1.00000E+00
+ PERMOD = 0.00000E+00 TOXE = 2.30000E-09 TOXP = 1.92000E-09
+ EPSROX = 3.90000E+00 XJ = 8.00000E-08 NDEP = 1.60000E+18
+ NGATE = 2.00000E+20 NSD = 1.00000E+20 VTH0 = 2.79572E-01
+ K1 = 2.82928E-01 K2 = -1.03648E-02 K3 = -2.55690E+00
+ K3B = 1.17310E+00 W0 = 1.00000E-10 VFB = -1.00000E+00
+ PHIN = 0.00000E+00 LPE0 = 1.20898E-07 LPEB = 3.26229E-08
```

```
+ DVT0 = 6.74408E-03 DVT1 = 3.23649E-02 DVT2 = -1.61846E-02
+ DVTP0 = 0.00000E+00 DVTP1 = 0.00000E+00 DVT0W = -1.26693E-01
+ DVT1W = 8.61226E+05 DVT2W = 1.96959E-01 U0 = 3.58576E+02
+ UA = 0.00000E+00 UB = 1.86125E-18 UC = 1.60862E-10
+ EU = 1.67000E+00 VSAT = 1.35800E+05 A0 = 1.67233E+00
+ AGS = 8.89796E-01 B0 = -2.00000E-08 B1 = 0.00000E+00
+ KETA = -6.30471E-02 A1 = 0.00000E+00 A2 = 1.00000E+00
+ RDSW = 1.40444E+02 RDSWMIN = 2.17931E+00 PRWB = 1.04000E-01
+ PRWG = -1.14651E-01 WR = 1.00000E+00 WINT = 1.26879E-08
+ LINT = 5.50000E-09 DWG = -9.55519E-10 DWB = 0.00000E+00
+ VOFF = -6.11435E-02 VOFFL = 0.00000E+00 MINV = 2.80000E+00
+ NFACTOR = 4.00000E-01 ETA0 = 6.32663E-04 ETAB = -1.55000E-04
+ DSUB = 3.13217E-02 CIT = 9.00000E-04 CDSC = 4.02133E-05
+ CDSCB = 2.41457E-05 CDSCD = 0.00000E+00 PCLM = 2.07565E+00
+ PDIBLC1 = 5.15347E-06 PDIBLC2 = 5.24808E-04 PDIBLCB = -7.05723E-01
+ DROUT = 2.90945E-02 PSCBE1 = 7.50025E+08 PSCBE2 = 3.70361E-07
+ PVAG = 1.50000E+01 DELTA = 7.37000E-03 ALPHA0 = 3.00000E-11
+ ALPHA1 = 0.00000E+00 BETA0 = 3.80000E+00 AGIDL = 2.43759E-08
+ BGIDL = 1.95095E+09 CGIDL = 5.00000E-01 EGIDL = 2.56798E-01
+ RSH = 0.00000E+00 FPROUT = 0.00000E+00 PDITS = 0.00000E+00
+ PDITSL = 0.00000E+00 PDITSD = 2.60000E-01 JSS = 1.56388E-07
+ JSWS = 1.07166E-13 JSWGS = 2.53515E-13 IJTHSREV = 1.00000E-01
+ IJTHSFWD = 1.00000E-01 XJBVS = 1.00000E+00 BVS = 1.00000E+01
+ AIGBACC = 1.30106E-02 BIGBACC = 3.80785E-03 CIGBACC = 2.21617E-01
+ NIGBACC = 4.00000E+00 AIGBINV = 1.91321E-02 BIGBINV = 6.35793E-03
+ CIGBINV = 1.49880E-03 EIGBINV = 2.01293E-03 NIGBINV = 1.00000E+00
+ AIGC = 1.05435E-02 BIGC = 1.63743E-03 CIGC = 4.57381E-02
+ AIGSD = 8.90242E-03 BIGSD = 1.00000E-06 CIGSD = 2.06887E-02
+ DLCIG = 5.00000E-09 NIGC = 1.72466E+00 POXEDGE = 1.00000E+00
+ PIGCD = 1.00000E+00 NTOX = 1.00000E+00 TOXREF = 2.30000E-09
+ XPART = 0.00000E+00 CGSO = 1.42000E-10 CGDO = 1.42000E-10
+ CGBO = 0.00000E+00 CJS = 1.00000E-03 MJS = 3.23722E-01
+ MJSWS = 1.00000E-01 CJSWS = 5.21900E-11 CJSWGS = 2.10400E-10
+ MJSWGS = 7.00000E-01 PBSWS = 1.00000E+00 PBS = 6.98994E-01
+ PBSWGS = 5.50000E-01 CGSL = 8.00000E-11 CGDL = 8.00000E-11
```

```
+ CKAPPAS = 6.00000E-01 CF = 1.20000E-10 CLC = 1.00000E-07
+ CLE = 6.00000E-01 DLC = 2.30000E-08 DWC = 1.26879E-08
+ VFBCV = -1.00000E+00 NOFF = 2.10000E+00 VOFFCV = -3.00000E-02
+ ACDE = 1.00000E+00 MOIN = 7.00000E+00 WL = -8.07124E-21
+ WLN = 9.72043E-01 WW = 1.00000E-16 WWN = 1.10000E+00
+ WWL = -2.10000E-23 LL = 5.00000E-16 LLN = 1.00000E+00
+ LW = 2.63398E-16 LWN = 1.19880E+00 LWL = -2.49331E-23
+ TNOM = 2.50000E+01 UTE = -1.20000E+00 KT1 = -2.05642E-01
+ KT1L = 4.00000E-10 KT2 = -3.50186E-02 UA1 = 1.68569E-09
+ UB1 = -1.32806E-18 UC1 = -4.00000E-11 AT = 1.00000E+03
+ PRT = -5.00000E+01 NJS = 1.05000E+00 XTIS = 3.00000E+00
+ TPB = 1.50000E-03 TPBSW = 2.00000E-03 TPBSWG = 1.20000E-03
+ TCJ = 9.00000E-04 TCJSW = 7.00000E-04 TCJSWG = 6.00000E-04
+ NOIA = 1.00000E+20 NOIB = 5.00000E+04 NOIC = -1.40000E-12
+ EM = 4.10000E+07 AF = 1.00000E+00 EF = 1.00000E+00
+ KF = 0.00000E+00 NTNOI = 1.00000E+00 TNOIA = 1.50000E+00
+ TNOIB = 3.50000E+00 LMIN = 8.00000E-08 LMAX = 1.00000E-05
+ WMIN = 1.20000E-07 WMAX = 1.00000E+00
+ LLC = 0.00000E+00 WLC = 0.00000E+00 LWC = 0.00000E+00
+ WWC = 0.00000E+00 LWLC = 0.00000E+00 WWLC = 0.00000E+00
+ PVSAT = -2.76718E+01
+ PPVAG = -5.91262E-02 LK3 = -7.01570E-01 LPVAG = -4.50007E-01
+ XL = 0.00000E+00 XW = 0.00000E+00 PU0 = -2.62732E-01
+ PUB = -1.06728E-20
.MODEL PMOS1 PMOS
+ LEVEL = 5.40000E+01 VERSION = 4.20000E+00 BINUNIT = 1.00000E+00
+ PARAMCHK = 0.00000E+00 MOBMOD = 0.00000E+00 CAPMOD = 2.00000E+00
+ RDSMOD = 0.00000E+00 IGCMOD = 1.00000E+00 IGBMOD = 1.00000E+00
+ FNOIMOD = 1.00000E+00 TNOIMOD = 0.00000E+00 DIOMOD = 1.00000E+00
+ PERMOD = 0.00000E+00 TOXE = 2.40000E-09 TOXP = 1.98000E-09
+ EPSROX = 3.90000E+00 XJ = 8.00000E-08 NDEP = 5.20000E+17
+ NGATE = 1.40000E+20 NSD = 1.00000E+20 VTH0 = -2.85479E-01
+ K1 = 3.17233E-01 K2 = -8.76234E-03 K3 = 3.08981E-01
+ K3B = 8.70132E-01 W0 = 6.57581E-10 VFB = -1.00000E+00
+ PHIN = 0.00000E+00 LPE0 = 7.46456E-08 LPEB = -1.50000E-08
```

```
+ DVT0 = 1.12021E-02 DVT1 = 2.92015E-02 DVT2 = -5.01808E-02
+ DVTP0 = 0.00000E+00 DVTP1 = 0.00000E+00 DVT0W = 3.23543E-01
+ DVT1W = 8.32111E+05 DVT2W = 1.65532E-01 U0 = 7.21140E+01
+ UA = 1.59639E-12 UB = 1.06685E-18 UC = -2.40118E-11
+ EU = 1.67000E+00 VSAT = 1.99000E+05 A0 = 2.50000E+00
+ AGS = 9.03713E-01 B0 = 6.03511E-08 B1 = 6.14485E-07
+ KETA = -2.00471E-02 A1 = 0.00000E+00 A2 = 1.00000E+00
+ RDSW = 9.25230E+01 RDSWMIN = 1.66186E+00 PRWB = -1.00000E-01
+ PRWG = -3.87950E-02 WR = 1.00000E+00 WINT = -1.40000E-08
+ LINT = 4.05000E-09 DWG = -9.55519E-10 DWB = 0.00000E+00
+ VOFF = -6.11435E-02 VOFFL = 0.00000E+00 MINV = 1.00000E+00
+ NFACTOR = 4.00000E-01 ETA0 = 2.71789E-04 ETAB = -7.00000E-05
+ DSUB = 1.76962E-02 CIT = 9.00000E-04 CDSC = 4.20827E-05
+ CDSCB = 3.90335E-05 CDSCD = 2.06172E-06 PCLM = 1.00000E-01
+ PDIBLC1 = 2.23872E-07 PDIBLC2 = 5.24808E-04 PDIBLCB = -7.05723E-01
+ DROUT = 7.73693E-01 PSCBE1 = 7.50025E+08 PSCBE2 = 3.70361E-07
+ PVAG = 1.50000E+01 DELTA = 1.17000E-02 ALPHA0 = 3.57396E-10
+ ALPHA1 = 0.00000E+00 BETA0 = 9.58015E+00 AGIDL = 2.08400E-08
+ BGIDL = 2.22154E+09 CGIDL = 3.88392E-01 EGIDL = 2.95809E-01
+ RSH = 0.00000E+00 FPROUT = 0.00000E+00 PDITS = 3.80000E-01
+ PDITSL = 7.20000E+05 PDITSD = 4.14448E-01 JSS = 7.09895E-08
+ JSWS = 2.16035E-14 JSWGS = 3.29856E-14 IJTHSREV = 1.00000E-01
+ IJTHSFWD = 1.00000E-01 XJBVS = 1.00000E+00 BVS = 1.00000E+01
+ AIGBACC = 1.10487E-02 BIGBACC = 4.89185E-03 CIGBACC = 4.37154E-01
+ NIGBACC = 4.00000E+00 AIGBINV = 1.69834E-02 BIGBINV = 5.94953E-03
+ CIGBINV = 1.17277E-03 EIGBINV = 1.34560E-06 NIGBINV = 1.00000E+00
+ AIGC = 6.56697E-03 BIGC = 9.26824E-04 CIGC = 5.31466E-02
+ AIGSD = 5.05243E-03 BIGSD = 9.99952E-07 CIGSD = 2.06845E-02
+ DLCIG = 5.00000E-09 NIGC = 3.09099E-01 POXEDGE = 1.00000E+00
+ PIGCD = 1.00000E+00 NTOX = 1.00000E+00 TOXREF = 2.45000E-09
+ XPART = 1.00000E+00 CGSO = 1.40000E-10 CGDO = 1.40000E-10
+ CGBO = 0.00000E+00 CJS = 1.00000E-03 MJS = 4.14311E-01
+ MJSWS = 2.54709E-01 CJSWS = 8.14000E-11 CJSWGS = 4.20000E-10
+ MJSWGS = 6.00000E-01 PBSWS = 5.05350E-01 PBS = 7.69082E-01
+ PBSWGS = 9.29453E-01 CGSL = 9.50000E-11 CGDL = 9.50000E-11
```

```
+ CKAPPAS = 5.00000E-01 CF = 1.20000E-10 CLC = 1.00000E-07
+ CLE = 6.00000E-01 DLC = 2.45000E-08 DWC = -1.40000E-08
+ VFBCV = -1.00000E+00 NOFF = 2.10000E+00 VOFFCV = -3.00000E-02
+ ACDE = 1.00000E+00 MOIN = 7.00000E+00 WL = 2.50325E-19
+ WLN = 9.21748E-01 WW = 0.00000E+00 WWN = 1.00000E+00
+ WWL = 6.45309E-24 LL = 4.00000E-16 LLN = 1.00000E+00
+ LW = -1.36171E-14 LWN = 9.70905E-01 LWL = 7.86145E-22
+ TNOM = 2.50000E+01 UTE = -1.00000E+00 KT1 = -2.75642E-01
+ KT1L = -1.00000E-09 KT2 = -3.50186E-02 UA1 = 1.05958E-09
+ UB1 = -1.68375E-18 UC1 = -2.31906E-11 AT = 1.00000E+03
+ PRT = -7.20000E+01 NJS = 1.00000E+00 XTIS = 3.00000E+00
+ TPB = 1.00000E-03 TPBSW = 5.00000E-04 TPBSWG = 1.00000E-04
+ TCJ = 8.50000E-04 TCJSW = 1.00000E-03 TCJSWG = 1.00000E-04
+ NOIA = 1.00000E+20 NOIB = 5.00000E+04 NOIC = -1.40000E-12
+ EM = 4.10000E+07 AF = 1.00000E+00 EF = 1.00000E+00
+ KF = 0.00000E+00 NTNOI = 1.00000E+00 TNOIA = 1.50000E+00
+ TNOIB = 3.50000E+00 LMIN = 8.00000E-08 LMAX = 1.00000E-05
+ WMIN = 1.20000E-07 WMAX = 1.00000E+00
+ LLC = 0.00000E+00 WLC = 0.00000E+00 LWC = 0.00000E+00
+ WWC = 0.00000E+00 LWLC = 0.00000E+00 WWLC = 0.00000E+00
+ LLPE0 = 9.40000E-09
+ PVSAT = 5.35918E+02 LKETA = 1.00000E-03 LK3 = 1.02690E+00
+ LPCLM = 0.00000E+00 XL = 0.00000E+00 XW = 0.00000E+00
+ PU0 = -3.75073E-02 PUB = 6.29168E-21
IBIAS 8 7 30U
.APPENDMODEL PMOS1_ra MOSRA PMOS1 PMOS
.ENDS
.MODEL PMOS1_ra MOSRA level=1
+tit0 = 5e-8 titfd = 7.5e-10 tittd = 1.45e-20
+tn = 0.25 ttd0 = 1 tdcd = -2.8
.MOSRA Reltotaltime='10*365*24*60*60'  Relstep='1*365*24*60*60'
+ Simmode=2  Relmode=2  Aginginst="X1.*"
.OP
.TF V(3) VIN+
.DC VIN+ -0.005 0.005 100U
```

```
.PRINT DC V(3)
.TRAN 0.05U 3U
.PRINT TRAN V(3) V(1)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
.END
```

Table B.4 HSPICE MOSRA input file for simulation of the NBTI aging impact on the aged unbuffered two-stage CMOS Op-Amp circuit specifications in the unity-gain configuration.

```
.OPTION POST PROBE APPENDALL SYMB=1
VIN+ 1 0 PULSE (0 1.2 0 1NS 1NS 1.5US 3US)
VDD 4 0 DC 1.2 AC 1.0
VSS 0 5 DC 1.2
CL 3 0 10P
X1 1 3 3 4 5 OPAMP
.SUBCKT OPAMP 1 2 6 8 9
M1 4 2 3 3 NMOS1 W=0.27500E-06 L=0.50000E-06
M2 5 1 3 3 NMOS1 W=0.27500E-06 L=0.50000E-06
M3 4 4 8 8 PMOS1 W=16.33000E-06 L=0.50000E-06
M4 5 4 8 8 PMOS1 W=16.33000E-06 L=0.50000E-06
M5 3 7 9 9 NMOS1 W=3.86950E-06 L=0.50000E-06
M6 6 5 8 8 PMOS1 W=48.27000E-06 L=0.50000E-06
M7 6 7 9 9 NMOS1 W=5.71900E-06 L=0.50000E-06
M8 7 7 9 9 NMOS1 W=3.86950E-06 L=0.50000E-06
CC 5 6 3.0P
.MODEL NMOS1 NMOS
+ LEVEL = 5.40000E+01 VERSION = 4.20000E+00 BINUNIT = 1.00000E+00
+ PARAMCHK = 0.00000E+00 MOBMOD = 0.00000E+00 CAPMOD = 2.00000E+00
+ RDSMOD = 0.00000E+00 IGCMOD = 1.00000E+00 IGBMOD = 1.00000E+00
+ FNOIMOD = 1.00000E+00 TNOIMOD = 0.00000E+00 DIOMOD = 1.00000E+00
+ PERMOD = 0.00000E+00 TOXE = 2.30000E-09 TOXP = 1.92000E-09
+ EPSROX = 3.90000E+00 XJ = 8.00000E-08 NDEP = 1.60000E+18
+ NGATE = 2.00000E+20 NSD = 1.00000E+20 VTH0 = 2.79572E-01
```

```
+ K1 = 2.82928E-01 K2 = -1.03648E-02 K3 = -2.55690E+00
+ K3B = 1.17310E+00 W0 = 1.00000E-10 VFB = -1.00000E+00
+ PHIN = 0.00000E+00 LPE0 = 1.20898E-07 LPEB = 3.26229E-08
+ DVT0 = 6.74408E-03 DVT1 = 3.23649E-02 DVT2 = -1.61846E-02
+ DVTP0 = 0.00000E+00 DVTP1 = 0.00000E+00 DVT0W = -1.26693E-01
+ DVT1W = 8.61226E+05 DVT2W = 1.96959E-01 U0 = 3.58576E+02
+ UA = 0.00000E+00 UB = 1.86125E-18 UC = 1.60862E-10
+ EU = 1.67000E+00 VSAT = 1.35800E+05 A0 = 1.67233E+00
+ AGS = 8.89796E-01 B0 = -2.00000E-08 B1 = 0.00000E+00
+ KETA = -6.30471E-02 A1 = 0.00000E+00 A2 = 1.00000E+00
+ RDSW = 1.40444E+02 RDSWMIN = 2.17931E+00 PRWB = 1.04000E-01
+ PRWG = -1.14651E-01 WR = 1.00000E+00 WINT = 1.26879E-08
+ LINT = 5.50000E-09 DWG = -9.55519E-10 DWB = 0.00000E+00
+ VOFF = -6.11435E-02 VOFFL = 0.00000E+00 MINV = 2.80000E+00
+ NFACTOR = 4.00000E-01 ETA0 = 6.32663E-04 ETAB = -1.55000E-04
+ DSUB = 3.13217E-02 CIT = 9.00000E-04 CDSC = 4.02133E-05
+ CDSCB = 2.41457E-05 CDSCD = 0.00000E+00 PCLM = 2.07565E+00
+ PDIBLC1 = 5.15347E-06 PDIBLC2 = 5.24808E-04 PDIBLCB = -7.05723E-01
+ DROUT = 2.90945E-02 PSCBE1 = 7.50025E+08 PSCBE2 = 3.70361E-07
+ PVAG = 1.50000E+01 DELTA = 7.37000E-03 ALPHA0 = 3.00000E-11
+ ALPHA1 = 0.00000E+00 BETA0 = 3.80000E+00 AGIDL = 2.43759E-08
+ BGIDL = 1.95095E+09 CGIDL = 5.00000E-01 EGIDL = 2.56798E-01
+ RSH = 0.00000E+00 FPROUT = 0.00000E+00 PDITS = 0.00000E+00
+ PDITSL = 0.00000E+00 PDITSD = 2.60000E-01 JSS = 1.56388E-07
+ JSWS = 1.07166E-13 JSWGS = 2.53515E-13 IJTHSREV = 1.00000E-01
+ IJTHSFWD = 1.00000E-01 XJBVS = 1.00000E+00 BVS = 1.00000E+01
+ AIGBACC = 1.30106E-02 BIGBACC = 3.80785E-03 CIGBACC = 2.21617E-01
+ NIGBACC = 4.00000E+00 AIGBINV = 1.91321E-02 BIGBINV = 6.35793E-03
+ CIGBINV = 1.49880E-03 EIGBINV = 2.01293E-03 NIGBINV = 1.00000E+00
+ AIGC = 1.05435E-02 BIGC = 1.63743E-03 CIGC = 4.57381E-02
+ AIGSD = 8.90242E-03 BIGSD = 1.00000E-06 CIGSD = 2.06887E-02
+ DLCIG = 5.00000E-09 NIGC = 1.72466E+00 POXEDGE = 1.00000E+00
+ PIGCD = 1.00000E+00 NTOX = 1.00000E+00 TOXREF = 2.30000E-09
+ XPART = 0.00000E+00 CGSO = 1.42000E-10 CGDO = 1.42000E-10
+ CGBO = 0.00000E+00 CJS = 1.00000E-03 MJS = 3.23722E-01
```

```
+ MJSWS = 1.00000E-01 CJSWS = 5.21900E-11 CJSWGS = 2.10400E-10
+ MJSWGS = 7.00000E-01 PBSWS = 1.00000E+00 PBS = 6.98994E-01
+ PBSWGS = 5.50000E-01 CGSL = 8.00000E-11 CGDL = 8.00000E-11
+ CKAPPAS = 6.00000E-01 CF = 1.20000E-10 CLC = 1.00000E-07
+ CLE = 6.00000E-01 DLC = 2.30000E-08 DWC = 1.26879E-08
+ VFBCV = -1.00000E+00 NOFF = 2.10000E+00 VOFFCV = -3.00000E-02
+ ACDE = 1.00000E+00 MOIN = 7.00000E+00 WL = -8.07124E-21
+ WLN = 9.72043E-01 WW = 1.00000E-16 WWN = 1.10000E+00
+ WWL = -2.10000E-23 LL = 5.00000E-16 LLN = 1.00000E+00
+ LW = 2.63398E-16 LWN = 1.19880E+00 LWL = -2.49331E-23
+ TNOM = 2.50000E+01 UTE = -1.20000E+00 KT1 = -2.05642E-01
+ KT1L = 4.00000E-10 KT2 = -3.50186E-02 UA1 = 1.68569E-09
+ UB1 = -1.32806E-18 UC1 = -4.00000E-11 AT = 1.00000E+03
+ PRT = -5.00000E+01 NJS = 1.05000E+00 XTIS = 3.00000E+00
+ TPB = 1.50000E-03 TPBSW = 2.00000E-03 TPBSWG = 1.20000E-03
+ TCJ = 9.00000E-04 TCJSW = 7.00000E-04 TCJSWG = 6.00000E-04
+ NOIA = 1.00000E+20 NOIB = 5.00000E+04 NOIC = -1.40000E-12
+ EM = 4.10000E+07 AF = 1.00000E+00 EF = 1.00000E+00
+ KF = 0.00000E+00 NTNOI = 1.00000E+00 TNOIA = 1.50000E+00
+ TNOIB = 3.50000E+00 LMIN = 8.00000E-08 LMAX = 1.00000E-05
+ WMIN = 1.20000E-07 WMAX = 1.00000E+00
+ LLC = 0.00000E+00 WLC = 0.00000E+00 LWC = 0.00000E+00
+ WWC = 0.00000E+00 LWLC = 0.00000E+00 WWLC = 0.00000E+00
+ PVSAT = -2.76718E+01
+ PPVAG = -5.91262E-02 LK3 = -7.01570E-01 LPVAG = -4.50007E-01
+ XL = 0.00000E+00 XW = 0.00000E+00 PU0 = -2.62732E-01
+ PUB = -1.06728E-20
.MODEL PMOS1 PMOS
+ LEVEL = 5.40000E+01 VERSION = 4.20000E+00 BINUNIT = 1.00000E+00
+ PARAMCHK = 0.00000E+00 MOBMOD = 0.00000E+00 CAPMOD = 2.00000E+00
+ RDSMOD = 0.00000E+00 IGCMOD = 1.00000E+00 IGBMOD = 1.00000E+00
+ FNOIMOD = 1.00000E+00 TNOIMOD = 0.00000E+00 DIOMOD = 1.00000E+00
+ PERMOD = 0.00000E+00 TOXE = 2.40000E-09 TOXP = 1.98000E-09
+ EPSROX = 3.90000E+00 XJ = 8.00000E-08 NDEP = 5.20000E+17
+ NGATE = 1.40000E+20 NSD = 1.00000E+20 VTH0 = -2.85479E-01
```

```
+ K1 = 3.17233E-01 K2 = -8.76234E-03 K3 = 3.08981E-01
+ K3B = 8.70132E-01 W0 = 6.57581E-10 VFB = -1.00000E+00
+ PHIN = 0.00000E+00 LPE0 = 7.46456E-08 LPEB = -1.50000E-08
+ DVT0 = 1.12021E-02 DVT1 = 2.92015E-02 DVT2 = -5.01808E-02
+ DVTP0 = 0.00000E+00 DVTP1 = 0.00000E+00 DVT0W = 3.23543E-01
+ DVT1W = 8.32111E+05 DVT2W = 1.65532E-01 U0 = 7.21140E+01
+ UA = 1.59639E-12 UB = 1.06685E-18 UC = -2.40118E-11
+ EU = 1.67000E+00 VSAT = 1.99000E+05 A0 = 2.50000E+00
+ AGS = 9.03713E-01 B0 = 6.03511E-08 B1 = 6.14485E-07
+ KETA = -2.00471E-02 A1 = 0.00000E+00 A2 = 1.00000E+00
+ RDSW = 9.25230E+01 RDSWMIN = 1.66186E+00 PRWB = -1.00000E-01
+ PRWG = -3.87950E-02 WR = 1.00000E+00 WINT = -1.40000E-08
+ LINT = 4.05000E-09 DWG = -9.55519E-10 DWB = 0.00000E+00
+ VOFF = -6.11435E-02 VOFFL = 0.00000E+00 MINV = 1.00000E+00
+ NFACTOR = 4.00000E-01 ETA0 = 2.71789E-04 ETAB = -7.00000E-05
+ DSUB = 1.76962E-02 CIT = 9.00000E-04 CDSC = 4.20827E-05
+ CDSCB = 3.90335E-05 CDSCD = 2.06172E-06 PCLM = 1.00000E-01
+ PDIBLC1 = 2.23872E-07 PDIBLC2 = 5.24808E-04 PDIBLCB = -7.05723E-01
+ DROUT = 7.73693E-01 PSCBE1 = 7.50025E+08 PSCBE2 = 3.70361E-07
+ PVAG = 1.50000E+01 DELTA = 1.17000E-02 ALPHA0 = 3.57396E-10
+ ALPHA1 = 0.00000E+00 BETA0 = 9.58015E+00 AGIDL = 2.08400E-08
+ BGIDL = 2.22154E+09 CGIDL = 3.88392E-01 EGIDL = 2.95809E-01
+ RSH = 0.00000E+00 FPROUT = 0.00000E+00 PDITS = 3.80000E-01
+ PDITSL = 7.20000E+05 PDITSD = 4.14448E-01 JSS = 7.09895E-08
+ JSWS = 2.16035E-14 JSWGS = 3.29856E-14 IJTHSREV = 1.00000E-01
+ IJTHSFWD = 1.00000E-01 XJBVS = 1.00000E+00 BVS = 1.00000E+01
+ AIGBACC = 1.10487E-02 BIGBACC = 4.89185E-03 CIGBACC = 4.37154E-01
+ NIGBACC = 4.00000E+00 AIGBINV = 1.69834E-02 BIGBINV = 5.94953E-03
+ CIGBINV = 1.17277E-03 EIGBINV = 1.34560E-06 NIGBINV = 1.00000E+00
+ AIGC = 6.56697E-03 BIGC = 9.26824E-04 CIGC = 5.31466E-02
+ AIGSD = 5.05243E-03 BIGSD = 9.99952E-07 CIGSD = 2.06845E-02
+ DLCIG = 5.00000E-09 NIGC = 3.09099E-01 POXEDGE = 1.00000E+00
+ PIGCD = 1.00000E+00 NTOX = 1.00000E+00 TOXREF = 2.45000E-09
+ XPART = 1.00000E+00 CGSO = 1.40000E-10 CGDO = 1.40000E-10
+ CGBO = 0.00000E+00 CJS = 1.00000E-03 MJS = 4.14311E-01
```

```
+ MJSWS = 2.54709E-01 CJSWS = 8.14000E-11 CJSWGS = 4.20000E-10
+ MJSWGS = 6.00000E-01 PBSWS = 5.05350E-01 PBS = 7.69082E-01
+ PBSWGS = 9.29453E-01 CGSL = 9.50000E-11 CGDL = 9.50000E-11
+ CKAPPAS = 5.00000E-01 CF = 1.20000E-10 CLC = 1.00000E-07
+ CLE = 6.00000E-01 DLC = 2.45000E-08 DWC = -1.40000E-08
+ VFBCV = -1.00000E+00 NOFF = 2.10000E+00 VOFFCV = -3.00000E-02
+ ACDE = 1.00000E+00 MOIN = 7.00000E+00 WL = 2.50325E-19
+ WLN = 9.21748E-01 WW = 0.00000E+00 WWN = 1.00000E+00
+ WWL = 6.45309E-24 LL = 4.00000E-16 LLN = 1.00000E+00
+ LW = -1.36171E-14 LWN = 9.70905E-01 LWL = 7.86145E-22
+ TNOM = 2.50000E+01 UTE = -1.00000E+00 KT1 = -2.75642E-01
+ KT1L = -1.00000E-09 KT2 = -3.50186E-02 UA1 = 1.05958E-09
+ UB1 = -1.68375E-18 UC1 = -2.31906E-11 AT = 1.00000E+03
+ PRT = -7.20000E+01 NJS = 1.00000E+00 XTIS = 3.00000E+00
+ TPB = 1.00000E-03 TPBSW = 5.00000E-04 TPBSWG = 1.00000E-04
+ TCJ = 8.50000E-04 TCJSW = 1.00000E-03 TCJSWG = 1.00000E-04
+ NOIA = 1.00000E+20 NOIB = 5.00000E+04 NOIC = -1.40000E-12
+ EM = 4.10000E+07 AF = 1.00000E+00 EF = 1.00000E+00
+ KF = 0.00000E+00 NTNOI = 1.00000E+00 TNOIA = 1.50000E+00
+ TNOIB = 3.50000E+00 LMIN = 8.00000E-08 LMAX = 1.00000E-05
+ WMIN = 1.20000E-07 WMAX = 1.00000E+00
+ LLC = 0.00000E+00 WLC = 0.00000E+00 LWC = 0.00000E+00
+ WWC = 0.00000E+00 LWLC = 0.00000E+00 WWLC = 0.00000E+00
+ LLPE0 = 9.40000E-09
+ PVSAT = 5.35918E+02 LKETA = 1.00000E-03 LK3 = 1.02690E+00
+ LPCLM = 0.00000E+00 XL = 0.00000E+00 XW = 0.00000E+00
+ PU0 = -3.75073E-02 PUB = 6.29168E-21
IBIAS 8 7 30U
.APPENDMODEL PMOS1_ra MOSRA PMOS1 PMOS
.ENDS
.MODEL PMOS1_ra MOSRA level=1
+tit0 = 5e-8 titfd = 7.5e-10 tittd = 1.45e-20
+tn = 0.25 ttd0 = 1 tdcd = -2.8
.MOSRA Reltotaltime='10*365*24*60*60'  Relstep='1*365*24*60*60'
+ Simmode=2  Relmode=2  Aginginst="X1.*"
```

```
.DC VIN+ -1.2 1.2 0.1
.PRINT DC V(3) ID(X1.M5)
.PROBE DC V(3) ID(X1.M5)
.TRAN 0.05U 3U
.PRINT TRAN V(3) V(1)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
.PROBE AC VDB(3) VP(3)
.END
```

CURRICULUM VITAE

PERSONAL INFORMATION

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EDUCATION

Degree	**Department**	**University**	**Date of Graduation**
Undergraduate	Electronic Engineering	University of Diyala	2004
High School	Applied Sciences	Dialaa School	2000

PUBLISHMENTS

Conference Papers

1. AL-Qaysi, H. K. and KIYAN, T., (2017). “Investigation of MOSFET Aging Modeling on an Analog Circuit Design”, Proceedings of International Conference on Progress in Applied Science 2017 (ICPAS 2017), 04-06 January 2017, Istanbul, Turkey. ISBN: 978-605-9546-02-7.