# AN ANALYTICAL PERFORMANCE ESTIMATION TOOL FOR ANALOG COMPUTER AIDED DESIGN



by

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# ABSTRACT

## AN ANALYTICAL PERFORMANCE ESTIMATION TOOL FOR ANALOG COMPUTER AIDED DESIGN

Automatic analog design tools are very attractive for the integrated circuit (IC) providers, because they increase the employees' efficiency and productivity; eliminate the high time and effort consumption. A performance evaluator is needed to spend no time for optimization of the unfeasible circuits and circuits which can not meet specifications.

The work in this thesis is part of a complete analog design automation system from top level to the lowest level of synthesis. The work concentrates on analog circuits built with CMOS (Complementary Metal Oxide Semiconductor) transistors which are the current and future trend of analog circuit design. Partitioning of the problem to simpler sub problems is the major strategy used. General design equations valid for all analog systems are used to model the sub-blocks. Design equations of the sub blocks are arranged according to the sub block type and the succeeding block. Finally equations are found relating design specifications to the design parameters.

The system has been realized and used and the results are compared with the results of the industry standard simulation tools. The tool is very fast as aimed and useful; it has been seen that it is enough fast and it gives the information to ease the actual design for a optimizer.

# ÖZET

## ANALOG BİLGİSAYAR DESTEKLİ TASARIMDA ANALİTİK BAŞARI TAHMİNİ

Analog otomasyon gereçleri, tümdevre üreticileri için ,çalışanların verimliliği ve üretkenliğini arttırdığı ve zaman kaybı ve emek harcanmasını azalttığından dolayı oldukça ilgi çekmektedir. Yaklaşık başarım tahmin ediciler, gerçeklenemeyen ve istenilen özellikleri veremeyecek devrelerin optimizasyonu için harcanacak zamanı ortadan kaldıracağından dolayı gereklidirler.

Bu tezdeki çalışma yüksek seviyeden en alt düzeyde sentezleme yapan bir analog tasarım otomasyon sisteminin bir parçası olacaktır. Çalışmada bugün ve yakın gelecekte teknoloji trendi olan CMOS transistorlü analog devreleri kullanılmıştır. Tasarım probleminin daha küçük parçaları bölünmesi izlenen temel stratejidir. Tüm elektronikte geçerli olan genel tasarım denklemleri kullanılmıştır. Bir blok için tasarım denklemleri çıkarılırken o bloğun tipi ve bir sonraki bloğun özellikleri göz önüne alınmıştır. Sonuçta, tasarımdan istenen özellikler (kazanç, bant genişliği v.b.), dizayn parametrelerine (alan,güç v.b.) bağlanan denklemler elde edilmiştir.

Sistem gerçeklenmiş ve çalıştırılmış ve sonuçlar endüstri standardı devre simulatorları ile karşılaştırılmıştır. Amaçlandığı gibi bir optimizasyon gerecine yardım edebilecek hızda olduğu ve tasarımı kolaylaştıracak bilgileri sağladığı görülmüştür.

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| | |
|---|---|
| $A$ | Area of the circuit block |
| $B$ | 3 dB cutoff frequency of the circuit block |
| $C$ | Capacitance of a node |
| $Dsub$ | Substrate doping coefficient for mosfet transistor |
| $\epsilon_{si}$ | Permitivity of the silicon |
| $\epsilon_{ox}$ | Permitivity of the oxide |
| $f$ | 3 db cutoff frequency of the circuit |
| $g_{ds}$ | Small signal output transconductance of a transistor |
| $g_m$ | Small signal input transconductance of a transistor |
| $G_m$ | Small signal input transconductance of the analog block |
| $I$, $Id$ | DC current of the analog block |
| $L$ | Mosfet channel length |
| $P$ | Power |
| $R_{out}$ | Output resistance of a block |
| $T_{ox}$ | Gate oxide thickness of a mosfet transistor |
| $x_j$ | Mosfet transistor junction depth |
| $vds$ | Drain-to-source voltage of a transistor |
| $vdsat$ | Drain-to-source saturation voltage |
| $Vgs$ | Gate to source voltage of a MOSFET transistor |
| $Vo$ | Output voltage of an analog block |
| $Vsupply$ | Supply voltage |
| $vth$ | Threshold voltage of the transistor |
| $\Theta$ | Drain induced barrier coefficient |
| APE | Analog performance estimator |
| *Area* | Integrated circuit area |
| Bandwidth | 3 db cutoff point of an analog block |
| BSIM3v3 | Berkeley Simulation Research Group version 3 transistor model |

| | |
|---|---|
| BTS | Basic two stage operational amplifier |
| CMOS | Complementary metal oxide field effect transistor |
| CLM | Channel length modulation in mosfet transistors |
| CPU | Central processing unit |
| DIBL | Drain induced barrier lowering effect in mosfet transistors |
| EKV | Enz, Krummenacher, Vitoz mos transitor model |
| Gain | Voltage gain of the circuit |
| IC | Integrated circuit |
| MOS | Mosfet transistor |
| MOS9 | Mosfet Model 9 developed by Philips company |
| Opamp | Operational amplifier |
| OPTIMAN | Optimization tool for analog systems |
| SCBE | Substrate current induced body effect in mosfet transistors |

# 1. INTRODUCTION

After the invention of the transistor in 1950's, electronics appear increasingly in our lives. Electronics become a fast evolving science and a sector, where large investments are done and many researchers are working. With the availability to produce integrated circuits, complex circuits with many transistors can be produced easily. Fabrication opportunities are at the same time have developed, reducing the cost of producing more and more complex circuits with increasing number of transistors. At the present time digital signal processing algorithms were becoming increasingly more powerful while advances in integrated circuit (IC) technology provided compact, efficient implementation of these algorithms in silicon. While many types of signal processing have indeed moved to the digital domain, analog circuits have proved fundamentally necessary in many of today's complex, high performance systems.

In the past decades CMOS (Complementary Metal Oxide Semiconductor) technology has rapidly introduced the field of analog integrated circuits, providing low-cost, high performance solutions and rising to dominate the market. Design of analog systems are much more complicated to the digital systems since many aspects of performance has to be taken at the same time into account such as gain , speed, supply voltage, voltage swings, power dissipation ,input output impedances ,power dissipation ,noise ,linearity , etc. Most of the time, these aspects are cross coupled i.e. changing one of them changes the others as well. Hence, makes the analog design area very complicated that designs requires many trade-offs between the specifications.

Unfortunately, analog design area lacks of powerful Computer Aided Tools (CAD) which are used widely in digital designs and reduce the effort for the design very much. This leads to spent great time and effort of human resources. A solution to this problem will be an 'Analog Design Automation Tool'.

An Analog Design Automation Tool is composed of different 'hierarchical synthesis blocks'. Such an organization is given in the below figure.

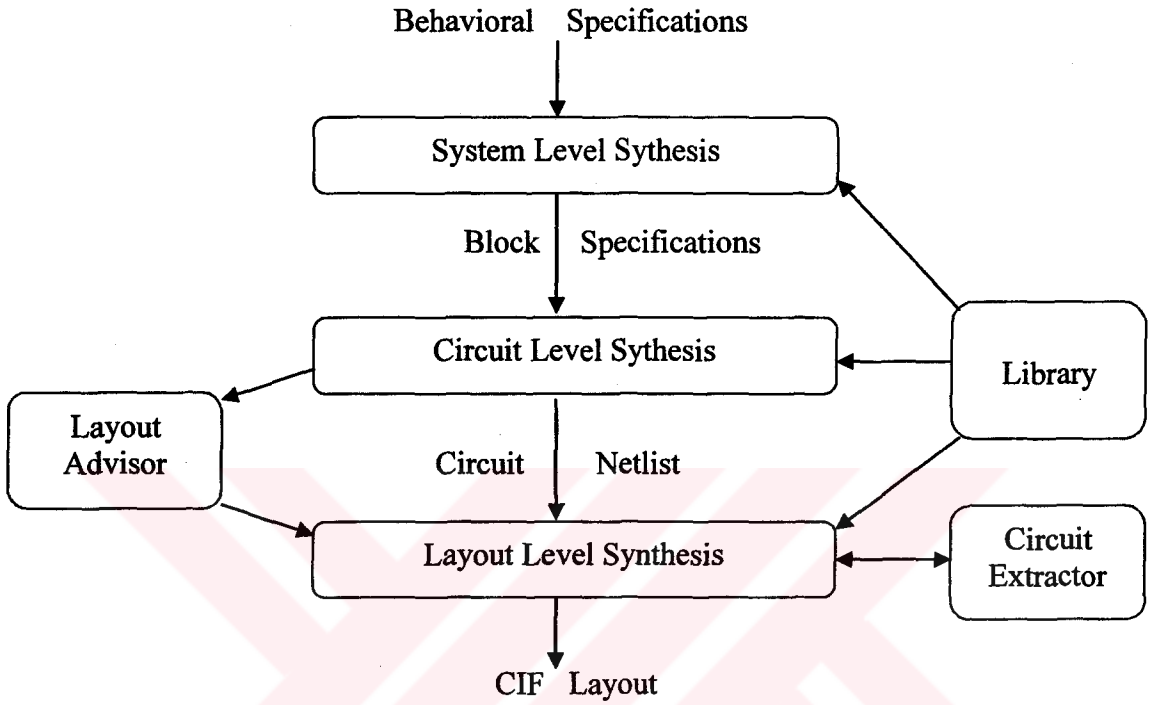



Figure 1.1. Analog design flow

At the top of the system 'High level system synthesis' block is present, which is responsible for decomposition of the hardware into an architecture consisting of functional blocks required to realize the specified behavioral description. This includes partitioning the circuit to its analog blocks. The specifications of the various blocks that are part of the design are defined. At the second place, 'Circuit Level Synthesis' block is present, which is responsible for the detailed implementation of the given specifications from the system level block. According to selected technology, full sized device level circuit schematic is prepared. More complex blocks will be decomposed into a set of sub blocks. Fabrication considerations (such as mismatch and tolerances) should be taken into account.

At the bottom part 'Layout level synthesis takes place', this simply makes the translation of the electrical schematic of the higher block into geometrical representation of layout. 'Circuit extractor' is the necessary part for making a detailed circuit simulation

with the presence of layout parasitic in order not to deviate from the performance characteristics due to the parasitic. A 'Layout advisor' would speed up the layout generation and verification process by giving necessary information on different parasitic effect of the circuit before generation of the layout.

The need of a speed up tool between 'High level Synthesis' block and 'Circuit level synthesis' block can be understood if we think that analog circuits consist of many transistors, and each of the transistor has several independent input variables that can be controlled . To many possibilities which contain unfeasible and data that does not meet the performance specifications will overload 'System Level Synthesizer' and increasing the total design time and most of the time will be spent on unwanted results. A quick block, which will give some pre-optimization hints to the circuit level part avoiding the unwanted parts data space will speed up the whole process .The system blocks containing such a tool, is given in Figure 1.2.

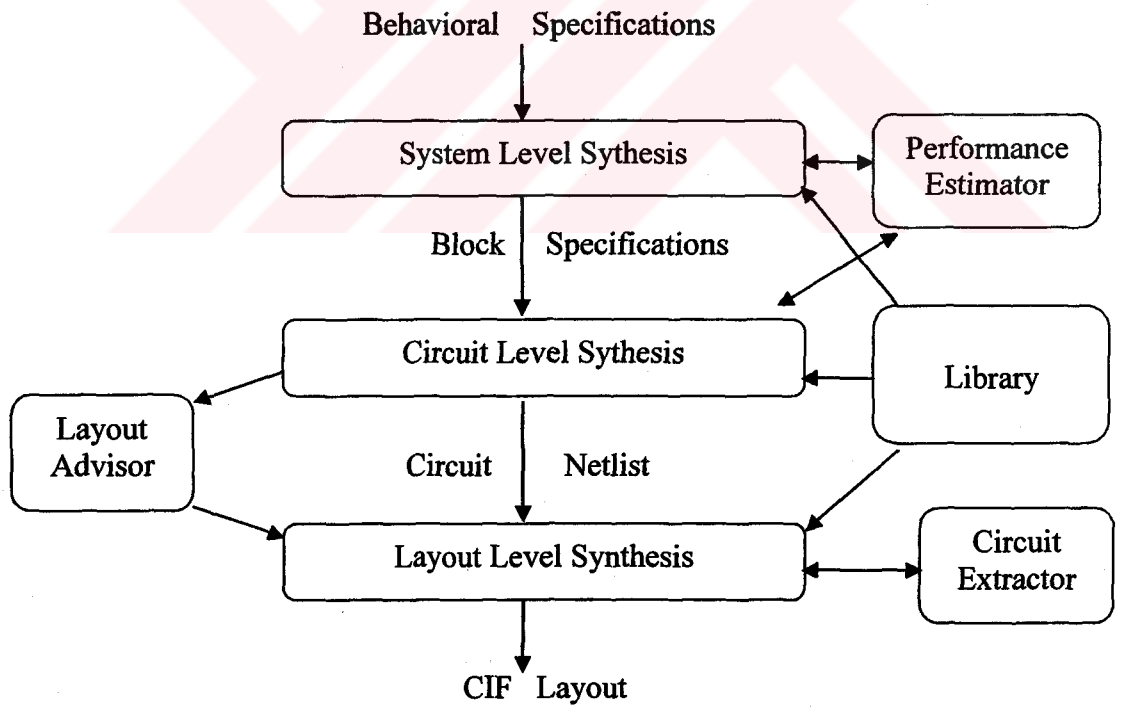



Figure 1.2. Modified analog design flow

In this thesis, an analytical fast performance estimation tool will be explained. A high accuracy is desired as if in the actual design phase but completely solving the device equation and sizing them accordingly should not be the path to be followed. This will be

done in the circuit level synthesizer using optimization algorithms. Instead, a fast performance estimator was developed which uses analytical design equations limits the input boundary conditions for the performance specifications.

In the next chapter, formulation of the problem and investigation of the literature is given. Chapter 2 represents overview of the work while chapter 3 and 4 are related for the methodology used. Chapter 5 concludes the work.

# 2. REVIEW OF THE LITERATURE, BACKGROUND OF THE PROBLEM

Performance estimation is very crucial to speed up the process of an Analog Automation Tool. Moreover, as used alone it gives the designer about the tradeoff of analog design. If we denote $y_i$ as a performance criteria of any analog circuit ( such as gain, bandwidth, slew rate, output resistance,etc.), and $x_j$ independent circuit parameter that determines the performance (such as width ,length of the mosfet (Metal oxide field effect transistor) , current of the transistors,etc.) ; one can define the performance response of the circuit as below:

$$y_1 = f_1(x_1, x_2, \ldots\ldots\ldots, x_j),$$
$$y_2 = f_2(x_1, x_2, \ldots\ldots\ldots, x_j),$$
$$\vdots \qquad\qquad \vdots$$
$$y_i = f_2(x_1, x_2, \ldots\ldots\ldots, x_j),$$

The problem is to find solutions for the $y_i$ in terms of $y_j$'s without solving each of them according to $x_j$'s. The relation functions are usually highly nonlinear and most of the time it is very complicated to find an analytical equation for it.

Different ways are proposed for the solution to the problem. A very simple solution would be to form a look up table for every data points, i.e. all different $x_j$ combinations. Assuming how many different transistor width, and length combinations are (from 0.8 μ to several thousand micrometers with 0.1 μ steps) one ends up with several thousand data points for each width or length and a 10 transistor device results with huge number of transistors. These huge data then can be filtered to some extend by filtering useless solutions (e.g. solutions that drives transistors in cut-off or linear regions).

Authors of [1] have implemented a system named OPTIMAN (Optimization tool for analog systems) that finds solution from a circuit level synthesizer .This eliminates large number of waste solutions within 48 hours using a powerful CPU.

Reduction of the sample data points are represented by Harjani and Shao[2] by choosing the data samples based on examination of the data space. A feasibility region is defined that sets boundary points to the data point space. The region is searched by vertical and radial search algorithms, then dynamic slicing is done according to the frequency of the boundaries, also the independent variables of the solution space are screened according to their significance and finally solution volume is constructed with doing regression analysis

Interval analysis is another method for performance estimation as in Veselinovic's [3] work. The earlier use of interval analysis in electronics was only capable on linear equations. This method can be used to predict the response of the output function as an interval according to the intervals of the input variables. However, the equations are highly nonlinear which cannot be linearized regionally.

Another solution to the estimation problem had been proposed with the tool APE (Analog Performance Estimator) [4]. APE is not a kind of an estimator according to our definition; but instead it tries to make prediction for the nonlinear performance equations. But the interesting part of this tool is the hierarchical decomposition of the circuits to its analog sub blocks which is the method used in this thesis. In APE at the lowest level there are elements like resistors, capacitors, etc. which are modeled analytically. Basic analog building blocks such as current mirrors, differential amplifiers are constructed using these elements. These are also modeled using analog equations. At the top of the system Opamps (Operational Amplifiers) are modeled, thereby a large system is modeled at several levels at the same time.

Prior to this work another estimator [5] has been built in this university. The estimator in that work, models transistors with neural networks and then tries to construct analog blocks using these transistors. Finally the blocks are cascaded and the whole circuit output parameters are calculated.

In the next chapter, the method used in this thesis is introduced.

# 3. PERFORMANCE ESTIMATION IN ANALOG COMPUTER AIDED DESIGN

The estimator block in Figure 1.2 is to established, which will connect the circuit level and system levels synthesis tools in a typical 'Automated analog design tool' in some sense, thus increasing the speed of the design generation. The circuit level has usually an optimizer in it, which is very accurate most of the time and the results of this part are very reliable. Thus, the aim was to construct a tool which makes crude but fast approximations based on its input parameters. However, the error level should not be very large, since in that case circuit level synthesizer has to realize circuits or blocks which cannot meet the desired performance specifications. If the resulting tool can also give an idea of effect of changing input parameters on output response, it will be a plus for the circuit designer.

## 3.1. Methodology Used for Performance Estimation

In this thesis, performance input and output variables of analog blocks are reduced and fixed which are circuit area and power and phase margin; whereas the input variables consist of gain, bandwidth and the output resistance. Supply voltages and mosfet technology parameters are fixed throughout the design of the circuit. The resulting performance estimator should not have input parameters such as specific devices widths, lengths and bias voltages like it is done by any circuit simulator. It should rather give an idea of circuit parameters relations.

A higher level system level synthesizer will order performance specifications to the circuit synthesizer according to a selected analog circuit. Therefore, for a given topology and performance specifications a performance region (it can be an n-dimensional volume or a surface in its simplest way) has to be constructed which will show the responses of the change of the output response with different input parameters.

This region can be constructed in two ways:

- Each of the input parameters are can in intervals and a search can be done on the constructed body when deciding if the input specifications are feasible. It is clear that this method consumes too much time either for constructing its performance region (due to the large availabilities of input parameters) or when searching on it according to the wanted specifications.
- The output and input parameters can be bound to each other by analytical modeling and these analytical equations can be used when constructing the output response body or when searching on it.

After deciding to use the analytical modeling, due to its fast computational property and ease for construction of data points, the next problem will be to decide how to write analytical expressions for large analog circuits. There is a decision to be made how to construct the analytical expression for the behavior of the whole circuit:

- One method will be to construct equations of the large circuit by first modeling an analog building block (such as current mirror, differential amplifiers) analytically, then putting its equation in the large system equation .Using this method will give a very large equation highly nonlinear and input parameters will be cross coupled, which is very hard to solve.
- An alternative method will be to partition the circuit to its analog building blocks; model each analog building block with it simple equations analytically, translate the input specifications of the whole system to its consisting blocks. Therefore the problem will be partitioned to its lowest parts.

An analog system is therefore decided to be decomposed to its physical sub blocks. The overall performance specifications should be translated to sub blocks. Given the type of the topologies there are many block specifications allocation possibilities that satisfy the overall system performance parameters. Most of the time designer wants to see the performance response of one item to change of two variables. The response data point will create a surface but the surface changes with how input parameters are allocated.

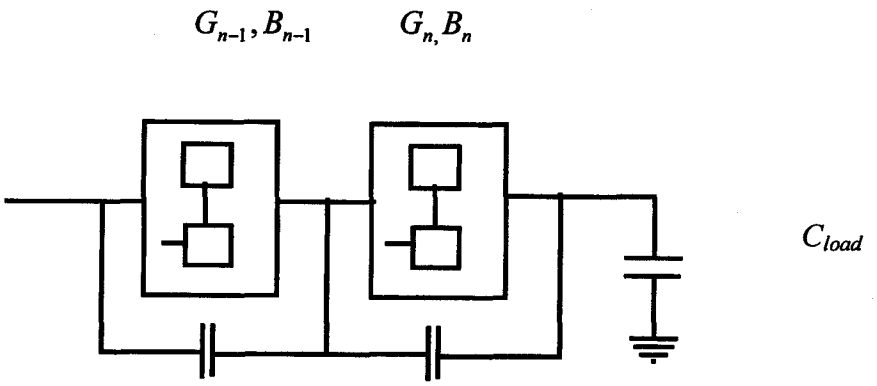



Figure 3.1. A typical analog circuit consisting of sub-blocks

For example such a combination is shown for a BTS (Basic Two Stage Opamp) in the below figure.

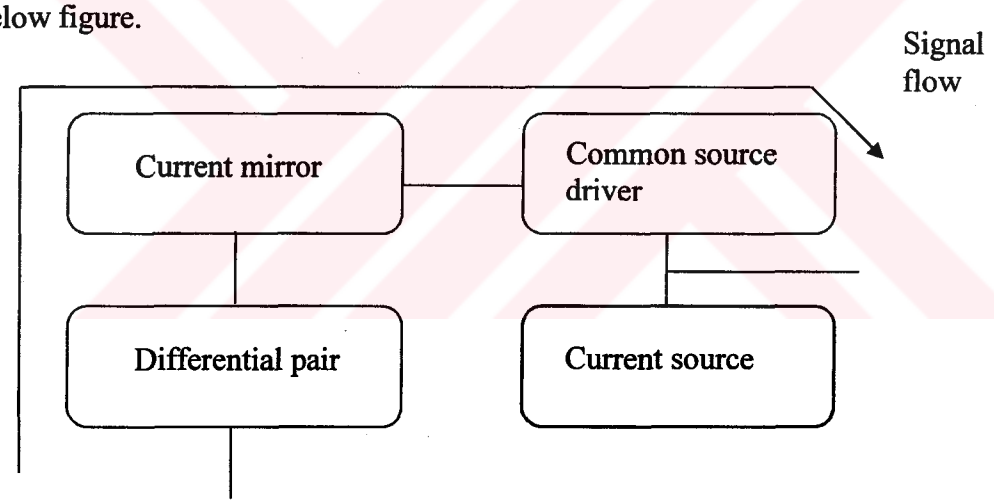


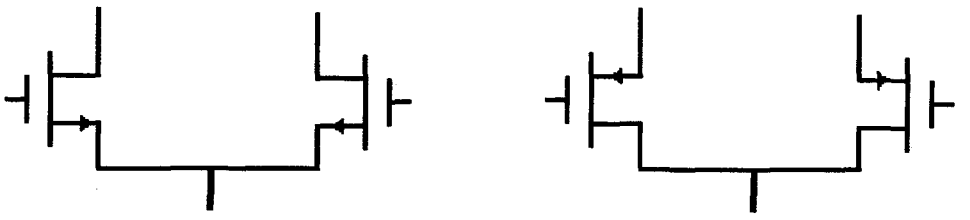

Figure 3.2. Subblocks in a basic two stage opamp

In figure 3.1 a typical BTS opamp is shown decomposed to its analog subblocks. Typical BTS opamp is decomposed of four analog building blocks namely: Differential input pair, current mirror, common source driver and a current source. At a one step higher level differential input pair and a push-pull output stage can be seen.

So, analog block libraries based on analytical equations should be constructed. The methodology when designing a big circuit will be to begin from the last block and moving to the previous block until we reach the first block.

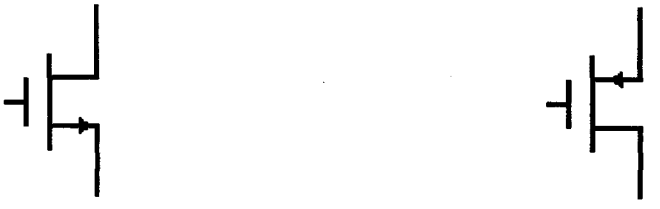
### 3.2. Blocks Modeled in the Library

Basic analog building blocks that are used to construct analog amplifiers, buffers etc., are listed below. The tool can realize any analog circuits which consist of the following sub blocks.



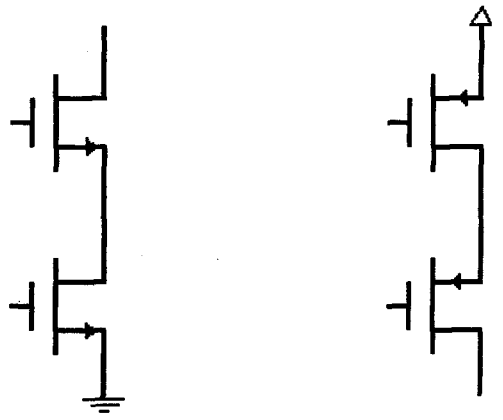
Block type 1: Differential input pair (n and p types)

Block type 2: Basic current mirror (n and p types)

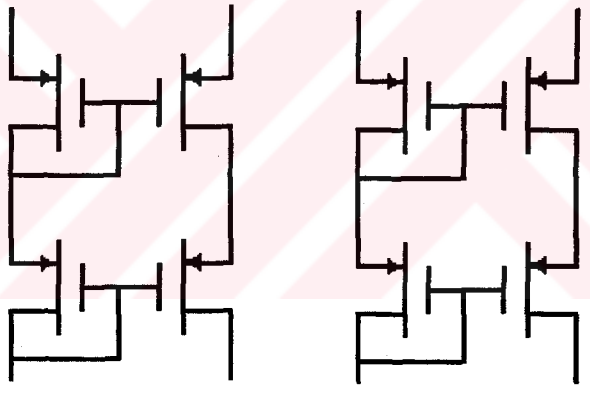


Block type 3: Common source driver (n and p types)

Figure 3.3. Analog building blocks modeled in the library



Block type 4: Cascode stage (n and p types)



Block type 5: Cascode Current Mirrors (n and p types)

Figure 3.3. Analog building blocks modeled in the library (continued)

Some of usable analog circuit parts constructed from the blocks listed in Figure 3.3 are given in the below figure.

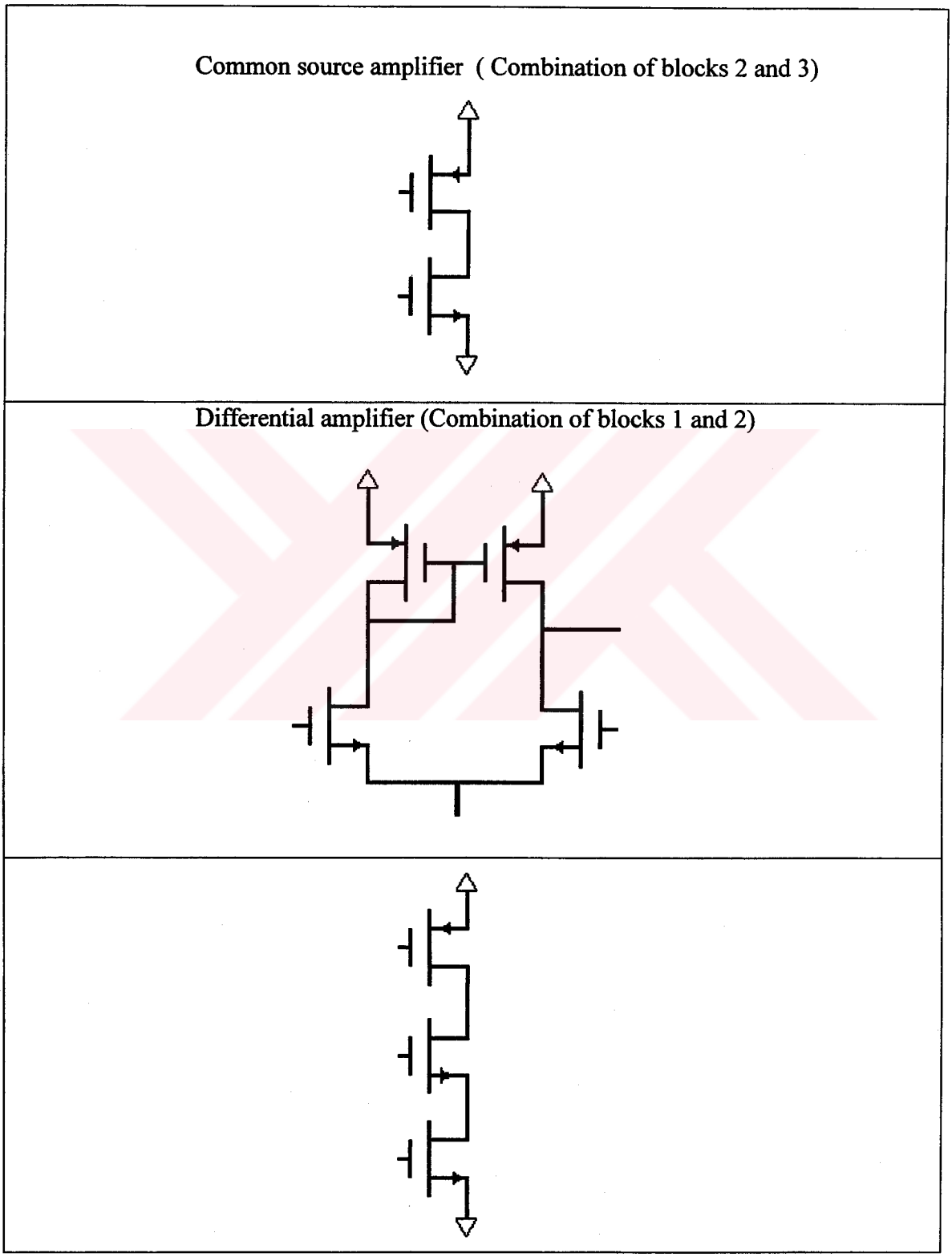



Figure 3.4. Usable analog blocks constructed from the library elements

## 3.3. Analytical Models of Analog Subcircuits

Analog subblocks listed in Figure 3.3 are combined to construct usable analog blocks such as amplifiers, output stages etc. Since user performance parameters such as gain, bandwidth, power dissipation etc. are defined for standalone analog blocks (i.e. blocks that can be used alone without the necessity of any other circuit), performance specifications are allocated to these blocks. Then general design equations that relate parameters gain, bandwidth, power, area with each other can be used for defining the *volumes or surfaces of the design*, in the unlimited data points. The idea is to limit the data space which is a 'nxn dimensional unbounded space' if we have 'n' design criteria. To do it, a boundary checking (BC) filtering can be done firstly for a very crude data filtering. For example, if a performance parameter is known to get a specific value for the design condition data related to that dimension can be filtered.

Afterwards parameter relations to each other are taken into account to construct a surface or a volume slice. But this is rather a complicated work since to get a surface or volume slice the n-dimensional space should be restricted in some coordinates to reduce its dimension to tow or three. The methodology of modeling different analog blocks is given below.

### 3.3.1. Output Stage Block

Output stages are used frequently in two stage opamps and amplifiers to get a low output resistance and high current capability to avoid slewing of the capacitive output loads. Low output resistance is a desired condition for this type of analog blocks. So, using equations that relate output resistance with circuit parameters is necessary. Unfortunately, basic transistor equations used for hand calculations lack for a proper output conductance ( $G_{ds} = \frac{\partial id}{\partial vds}$ ) equation to compatible values with the today's high performance MOS(mosfet transistor) simulation models (BSIM3v3, EKV, MOS9 etc). An analytical model for the conductance has been constructed for using with analog blocks design equation.

Recent MOS models such as BSIM, model the $R_{out}$ (output resistance of a mosfet transistor) in four distinct regions. In the first region the MOS operates in linear region. The second region is where 'Channel Length Modulation (CLM)' is the net effect that changes $R_{out}$; the third region is where 'Drain Induced Barrier Lowering (DIBL)' dominates the response. The last region is where $R_{out}$ decreases because of the 'Substrate Current Induced Body Effect (SCBE)'. For the MOS aspect ratios we are dealing CLM and DIBL can be used only to model the output resistance.

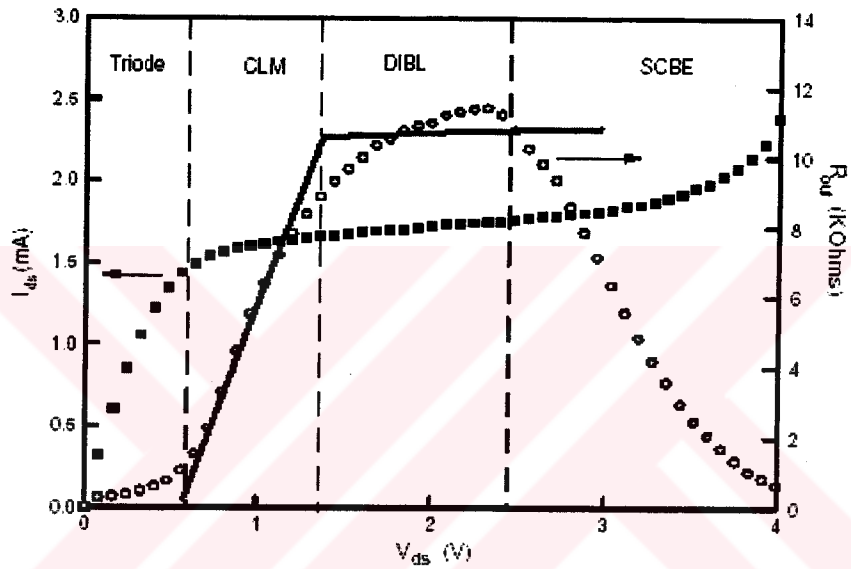



Figure 3.5. $R_{out}$ vs. vds graph of a MOS transistor

Figure 3.4 shows how $R_{out}$ is changing in different regions of the mosfet transistor. The dotted $R_{out}$ curve is the actual response; whereas the solid curve is the approximation which is used when modeling in this thesis. For a given drain to source voltage (vds) value of a transistor; its W (transistor width) over L (channel length of the transistor) ratio and its current, what determines the conductance region the transistor operates. The CLM effect has a characteristics to increase the $R_{out}$ of a MOS with the increase in 'vds', while DIBL effect will limit the $R_{out}$ and make it somehow constant. SCBE effect is important only in short channel devices which are beyond the scope of this thesis since very short channel devices are not preferred in analog design area. Therefore, this effect will be discarded.

When $R_{out}$ is only affected by the CLM the output resistance can be found by solving quasi 2-D Poisson equation at the point where channel pinched off and approximated to the following equation:

$$R_{out,CLM} \approx \frac{L}{l'} \times \frac{vds - vdsat}{Id} \approx \frac{L}{l'} \times \frac{vds - \sqrt{2\frac{Id}{\beta}}}{(Id)} \tag{3.1}$$

where

$$\beta = \mu\, Cox\, {}^{W}\!/_{L}\,. \tag{3.2}$$

Here $l'$ is a junction depth related parameter which is dependent on the fabrication process.

$$l' = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} x_j T_{ox}} \tag{3.3}$$

Refer [6] and [7] for details. In Equation 3.1 no bulk charge is assumed and drain saturation voltage is as below,

$$vdsat = vgs - vth\,. \tag{3.4}$$

Similarly using the DIBL model proposed in [8] we can write the change of the threshold voltage as:

$$\Delta Vth = e^{-L/2l'}(1 + 2e^{-L/2l'})((2vbi - \Phi s) + vds))\,. \tag{3.5}$$

Assuming square law device equation for the MOSFET, current equation and output conductance due to the variation of the threshold voltage can be written as,

$$Id = \frac{\beta}{2}(vgs - (vth - \Delta vth))^2 \tag{3.6}$$

$$\frac{\partial id}{\partial vd} = \frac{\partial id}{\partial vth}\frac{\partial vth}{\partial vds} = \beta\,(vgs - vth) \times \Theta_{DIBL} = \Theta_{DIBL}\sqrt{\beta}\sqrt{2Id} \tag{3.7}$$

$$\Theta_{DIBL} = [\exp(-D_{sub}L/2l_{to}) + 2\exp(-D_{sub}L/l_{to}). \quad (3.8)$$

where '*lt0*' is the '*lt*' value at zero bias. Parameter '*lt*' is referred as *characteristic length* in [6] and is defined as follows:

$$lt = \sqrt{\frac{\varepsilon_{si} T_{ox} X_{dep}}{\varepsilon_{ox} \eta}}. \quad (3.9)$$

Parameter 'η' is an empirical constant to get an average value of the junction depth $X_{dep}$. Finally the two output conductance in two region values can be written as:

$$gds_{DIBL} = \Theta \times \sqrt{\beta} \times \sqrt{2I} \quad (3.10)$$

$$gds_{CLM} = I \times \frac{l'}{L} \times \frac{1}{\left(vds - \sqrt{2 \times I/\beta}\right)}. \quad (3.11)$$

Actually the transition from one region two other is gradual ,this is modeled in simulators so that $R_{out\ DIBL}$ is parallel with $R_{out\ CLM}$; i.e. output conductance of a saturated MOS can be expressed with a unique expression as below.

$$gds_{Total} = \Theta \times \sqrt{\beta} \times \sqrt{I} + I \times \frac{l'}{L} \times \frac{1}{\left(vds - \sqrt{2 \times I/\beta}\right)} \quad (3.12)$$

An interesting phenomenon is the Gain equation of a common source amplifier with a MOS load.

$$G = \frac{g_m}{g_{ds}}$$

$$= \frac{\sqrt{2}\sqrt{I}\sqrt{\beta_1}}{(\Theta_1 \times \sqrt{\beta_1} \times \sqrt{2I} + \Theta_2 \times \sqrt{\beta_2} \times \sqrt{2I} + I \times \frac{l'}{L} \times \frac{1}{\left(vds - \sqrt{2 \times I/\beta_1}\right)} + I \times \frac{l'}{L} \times \frac{1}{\left(vds - \sqrt{2 \times I/\beta_2}\right)})} \quad (3.13)$$

Assuming the aspect ratios of the current source transistor is N times of the driver transistor. We get:

$$G_{\max} = \frac{1}{\Theta_1 + N\Theta_2}. \quad (3.14)$$

This property is useful for allocating a specification to the common source output stage, since its gain feasibility region is limited by the above formula. Design equations used are:

$$GAIN = gm\, R_{out} = \frac{\sqrt{A_1}}{L_1} \times \sqrt{I} \times \sqrt{2k} \times R_{out} = \frac{\sqrt{A_1}}{\sqrt{n+1}L_1} \times \sqrt{I} \times \sqrt{2k} \times R_{spec} \quad (3.15)$$

$$k = \mu\, Cox$$

$$GAIN \times BANDWIDTH = \frac{g_m}{2\Pi C_{out}} \quad (3.16)$$

$$g_m = \frac{\sqrt{2kId}\sqrt{A}}{L} \quad (3.17)$$

Therefore, gain-bandwidth product equation can relate two of gain, bandwidth, area and power while the other held constant. When $R_{out}$ is given as a design parameter; gain, area, power are also related to each other using Equation 3.16.

$$B_{output} = \frac{1}{2\Pi\left\{\frac{A_{output}\alpha}{L_1(N+1)}\left(1 + \alpha_2/\alpha_1 \frac{L_2}{L_1} N\right) + Cload\right\}} \times \frac{1}{R_{out}} \quad (3.18)$$

The drain capacitance of a transistor can be easily written in relation with its area and channel length:

$$C_d = C_{db} + C_{gd} = \alpha W = \alpha \ {Area}/{L} \ . \tag{3.19}$$

N is the ratio of the current source transistors area to the driver transistors area. In order to get equal positive and negative maximum output swings by n and p-type transistors, they are made with approximately 1:3 ratio. Assigning a bandwidth value to this block will give us its area for a given $R_{out}$. A unique current satisfy the parameters.

### 3.3.2. Differential Amplifier Stage

Differential amplifier is an example for input stages. Input stages should be considered with the effect of loading of the succeeding stage. Transistor channel lengths can be big so the output resistances are flexible according to the output voltage level. Therefore equations not using $R_{out}$ are preferred. Such equations are gain-bandwidth product Equations 3.16 and 3.18 is used for writing design equations.

$$B \times G = \frac{\sqrt{A_{driver}}/L_{driver} \sqrt{I}\sqrt{2k}}{2\Pi\left\{\alpha_1 \frac{A_{driver}}{L_{driver}} + \alpha_2 \frac{A_{mirror}}{L_{mirror}} + Cin\right\}} \tag{3.20}$$

Current mirror parts in differential amplifiers are used for biasing the next cascading stage. So, the voltage at the output node is important.

$$\left|V_o - V_{SUPPLY}\right| = vgs - vth \tag{3.21}$$

For a square law mosfet current equation was given in Equation (3.4). Using these information we can write the equation again as:

$$B \times G = \frac{\sqrt{A_{driver}} / L_{driver} \sqrt{I}\sqrt{2k}}{2\Pi\left\{\alpha_1 \frac{A_{driver}}{L_{driver}} + \alpha_2 \frac{I \times L_{mirror}}{(V_{SUPPLY} - Vo - vth)^2 k} + Cin\right\}} \tag{3.22}$$

Arranging the coefficients finally we get for a given gain and bandwidth an equation which relates area and current .Given one of them we can solve the equation quadratically and get the result simply by finding the roots of Equation 3.23 .

$$aA + bI + c = \sqrt{A}\sqrt{I} \tag{3.23}$$

$$A = \frac{I - 2abI - 2ac \pm \sqrt{(2abI - I + 2ac)^2 - 4a^2(b^2I^2 + 2bcI + c^2)}}{2a^2} \tag{3.24}$$

$$I = \frac{A - 2abA - 2bc \pm \sqrt{(2abA - A + 2bc)^2 - 4b^2(a^2I^2 + 2acA + c^2)}}{2b^2} \tag{3.25}$$

After getting the results from the tool for the above equations, it is seen that only solutions from equations using the negative sign before the square root term give true solutions. Other solutions are too big for a physical actual use.

### 3.4. Combining the Blocks

The above formulated block should be combined to get an ordinary analog block consisting of many blocks. Such a combination was a BTS opamp given in Figure 3.2. The whole circuit specifications must be distributed to blocks in order to get one blocks solution space, and finally combining the solution spaces to get the whole circuit's solution space.

Some '*boundary checking filtering*' [9] can be done when allocating analog building specifications; hence solution spaces can be restricted in someway. For some of the analog blocks maximum attainable gain is restricted with the channel length (Someone cannot get thousand of gain from a short channel output stage).

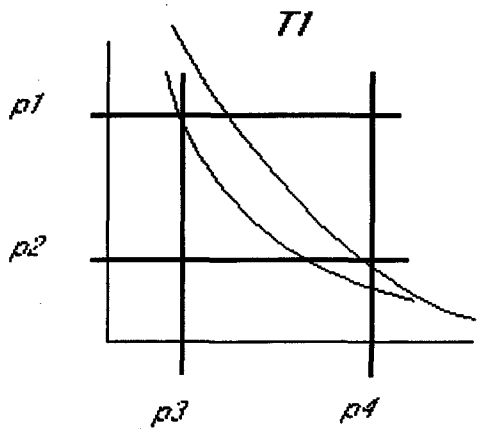



Figure 3.6. Feasibility of performance parameters

For the circuit topology 'T1': p1, p2, p3, p4 are the boundary conditions of the performance parameters. For example, vertical axis can be gain and the horizontal axis can be bandwidth of an analog block. In this case p1 is the maximum attainable gain from the block; p2 is the minimum gain which is one for the gain stages. Value of p2 is more determined by the succeeding block's maximum gain to achieve a certain gain value together. Values p3 and p4 are minimum and maximum achievable bandwidths of the block. The curve moves with parameters like circuit are and power. So an interval of these will create area between two curves which is the set of the solution.

For combination of the blocks, blocks equations have to be solved by taking care of the effect of the succeeding block. Since mosfet transistors are used they do not load the previous blocks resistively since mosfet gates are connected to the output of the previous stage. However, there is significant amount of capacitive loading which should be taken into care.

Next a complete basic two stage opamp design will be done to illustrate how the combination is done.

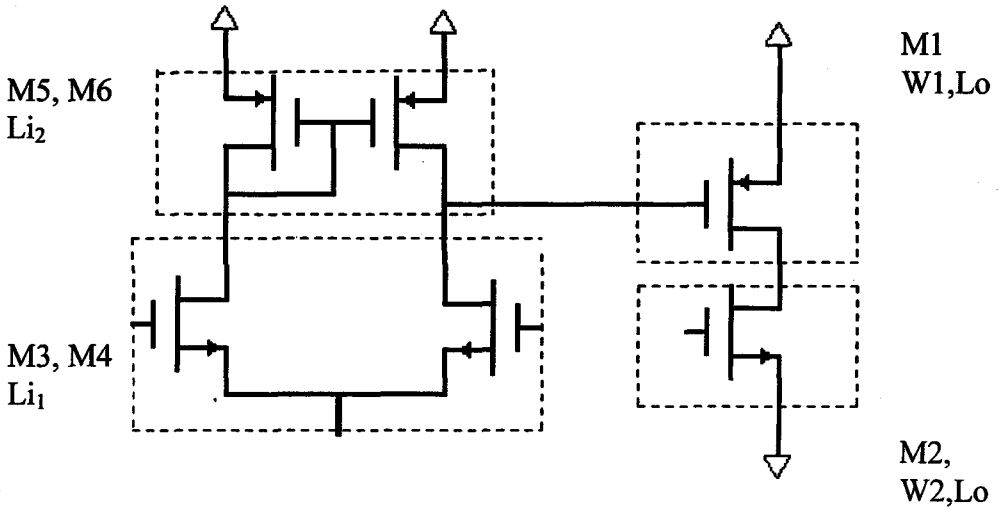



Figure 3.7. Schematic of a Basic two stage opamp

The output stage can be designed using its design equations. Once the design is complete, the design of the first block is constraint by the next block. Use Equations 3.15 - 3.18 to complete the output stage. The input capacitance of this block which will load the previous one will be:

$$C_{in} = \frac{2}{3} A_{output} \times Cox \times G_{input} \frac{1}{N+1} + Cgdo \frac{A_{output}}{L_{out}} \frac{1}{N+1} \tag{3.26}$$

As it can be seen the input capacitance of the succeeding blocks capacitance is directly related to its area. 'N' is the output stages complementary transistor ratio which is selected as 'three' in our case. The next thing will be to use gain-bandwidth product equation of the fist stage (differential amplifier) which given as below. Let 'M' be the ratio of the area of the output stages driver transistor to the input stages driver transistor. This type of a conditioning is needed because gain-bandwidth product equation is highly nonlinear this area ratio which can be related to the two blocks area ratio to eliminate the square rooted area term in the numerator. Then bandwidth of the input stage can be written as:

$$B_{input} = \frac{\sqrt{I}\sqrt{2k}}{2\Pi\sqrt{A_{input}}\left\{\left(\alpha_1 + \alpha_2 \frac{L_1}{L_2} N + \frac{2}{3} M \times CoxL_1\right) + G_{output} MCgdo \times \frac{L_1}{L_{out}}\right\}} \times \frac{1}{G_{input}} \tag{3.27}$$

Goutput term comes from the Miller multiplication of the overlap capacitor of the output stage. Equation 3.27 is the linearized type of Equation 3.22. Here the letter 'N' is used to show the ratio of the area of the current mirror transistor area the differential amplifier driver transistor areas. We know from our differential amplifier analysis that current mirror is responsible for the bias of the next stage and in the above formula term multiplied with $\alpha_2$ is current dependent, i.e. the ratio 'N' is current dependent. Current mirror transistors are responsible for biasing the output stages driver transistor; therefore it is responsible for the systematic output voltage. So, parameters M and N can be related and finally general form of differential amplifier equation can be preserved. Writing N as currents and M and manipulating the equation we get finally:

$$B_{input} = \frac{\sqrt{I}\sqrt{2k}}{2\Pi G_{TOTAL}\sqrt{A_{input}}\left\{\frac{\left(\alpha_1 + \alpha_2 \frac{L_1}{L_2}\left(\frac{L_2}{L_o}\right)^2 M\left(\frac{I_{in}}{I_{out}}\right) + 2/3\, MCoxL_1\right)}{Gout} + \frac{MCgdoL_1}{L_{out}}\right\}} \quad (3.28)$$

Equation 3.28 shows the bandwidth of the first stage relations to its area, current; succeeding stage's gain-bandwidth.We can use the formula for calculating the position of the dominant pole for a two stage device.

Given that the poles of the blocks are at f1, f2:

$$\frac{1}{f_{total}} = \sqrt{\frac{1}{f_1^2} + \frac{1}{f_2^2}} \quad (3.29)$$

$$B_{input} = \frac{1}{\sqrt{\left|\frac{1}{B_{out}^2} - \frac{1}{B_{total}^2}\right|}} \quad (3.30)$$

Total area of the difamp can be from there calculated using the N value. Hence, for a given 'M' and 'Iin' a response for the area according to change of the output stage's gain

and bandwidth parameters can be achieved. An idea for how to allocate gain and bandwidth can be deduced. By changing M value and Iin, the change in the response surface can be observed.

# 4. RESULTS

The developed tool was run and some performance specifications surfaces are plotted. They are given in their related sections.

## 4.1. Single Blocks' Results

### 4.1.1. Common Source Output Stage Modeling Results

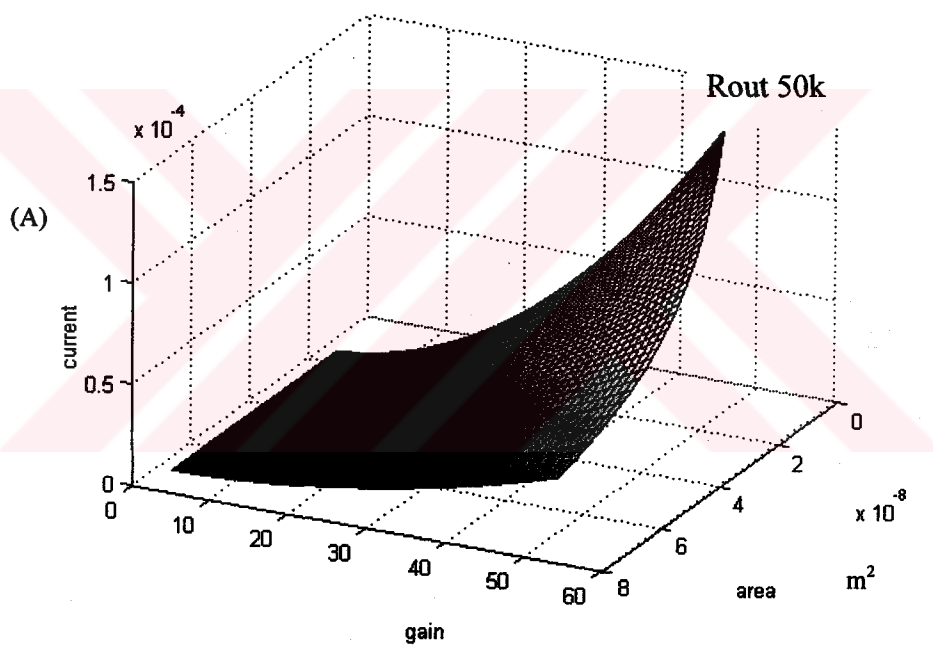



Figure 4.1. Area, gain ,current relation of a common source output stage

Figures 4.1-4.4 are showing current (which is related by power, P = V supply x current), area, gain and bandwidth relation. Since $R_{out}$ is given as a constraint, it eliminates one dimension of the performance space therefore for a specific *Rout* we can draw surfaces. Figure 4.3 shows that a high gain, high bandwidth amplifier consumes much more power, but the area should be small.

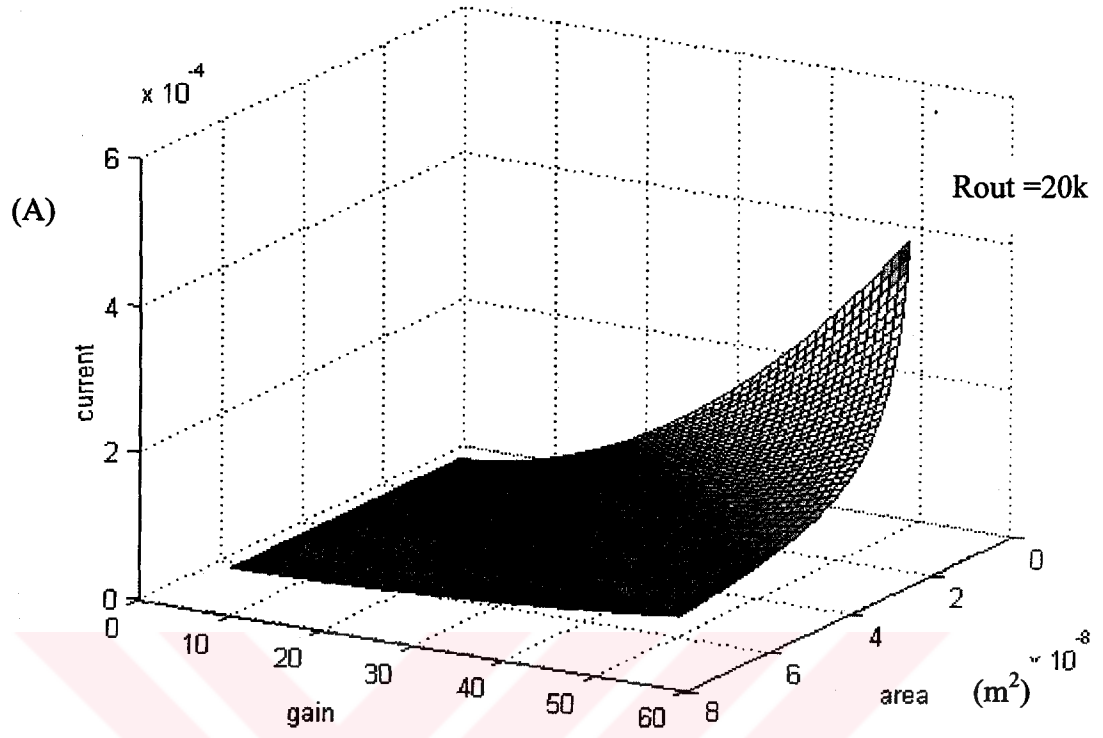



Figure 4.2. Effect of rout on common source performance

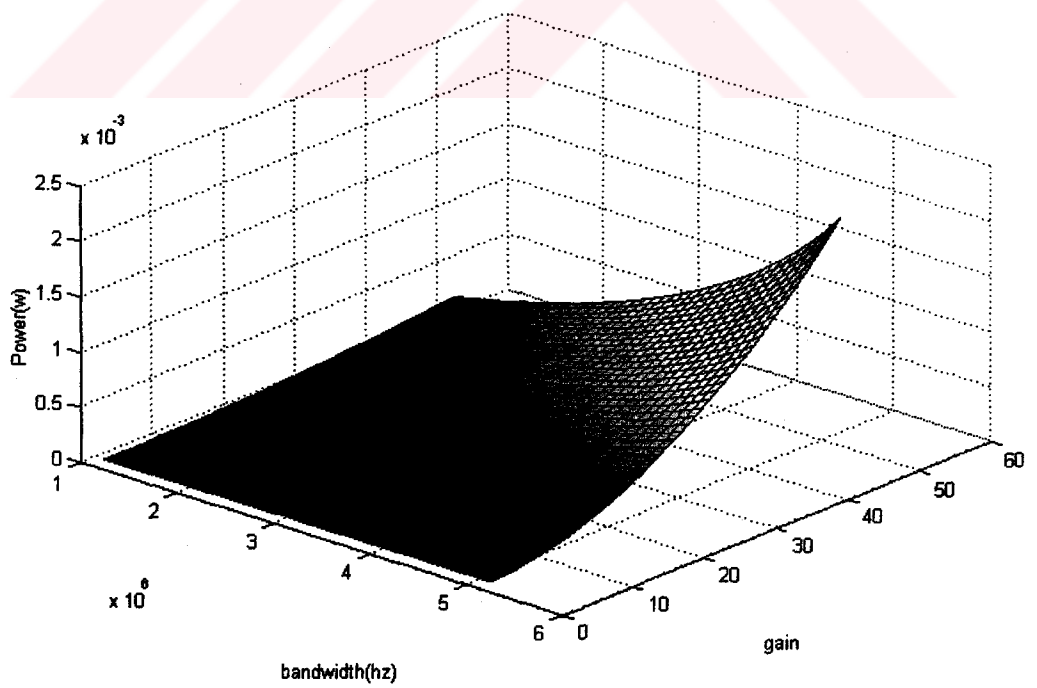



Figure 4.3. Gain, bandwidth , power relation of a common source output stage

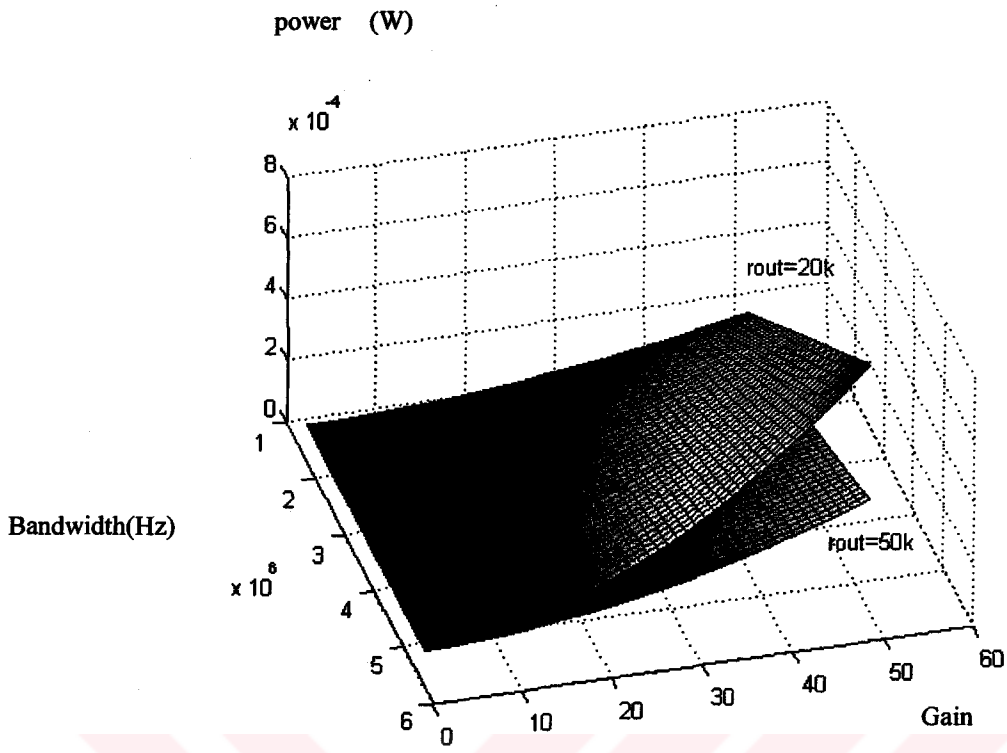



Figure 4.4. Gain, bandwidth, power relation of a common source output stage

Figure 4.4 shows that decreasing $R_{out}$ constraint which is mostly desirable increases the current consumption for a specific gain and bandwidth.

### 4.1.2. Differential Amplifier Stage Results

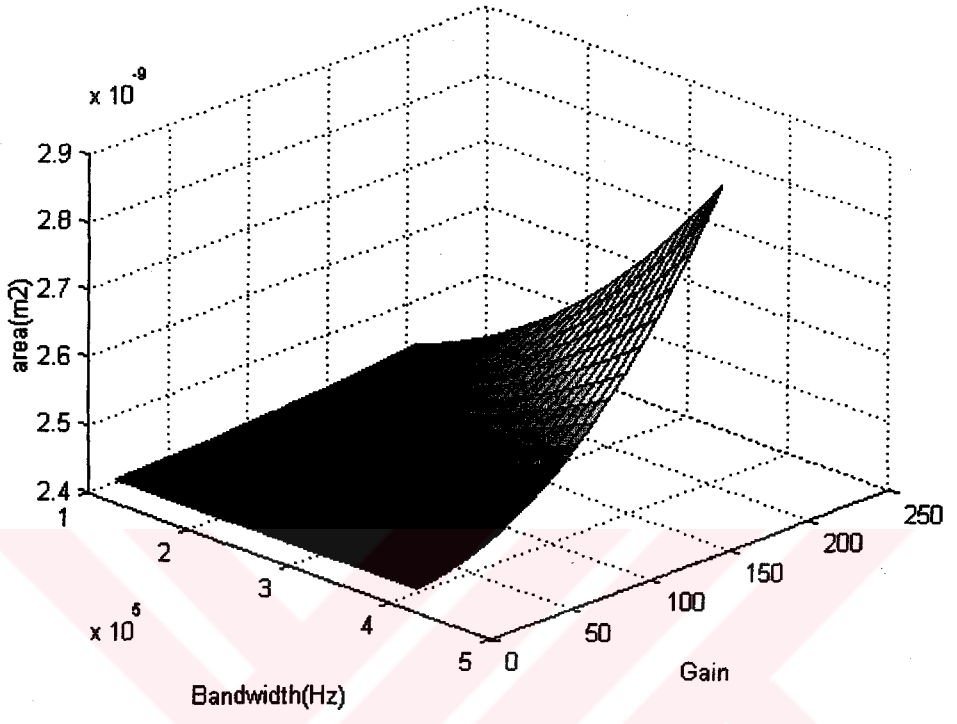



Figure 4.5. Gain, bandwidth, area relation of a differential amplifier

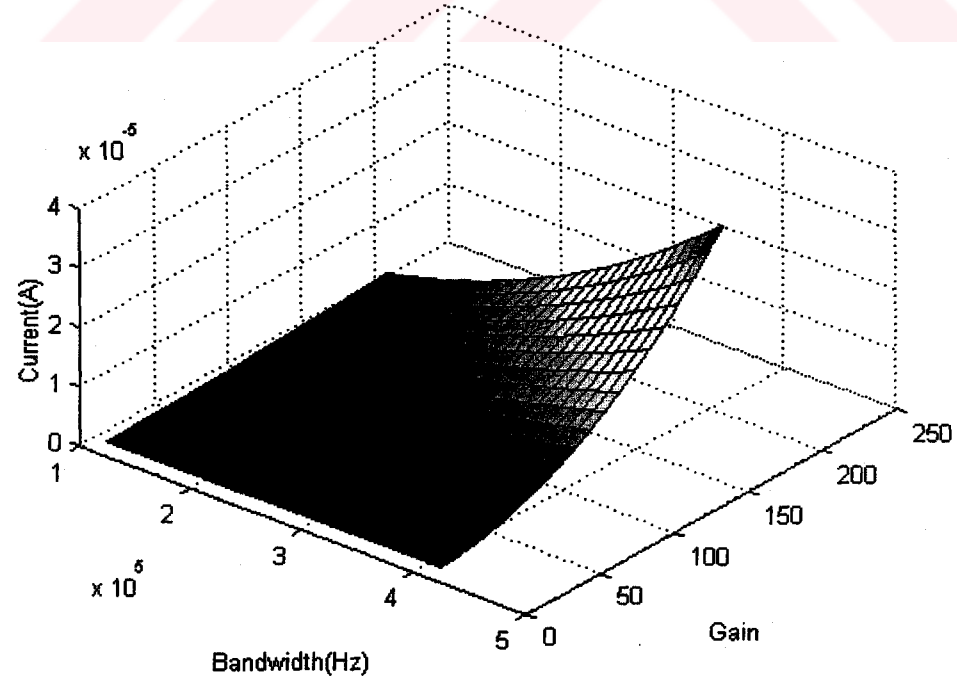



Figure 4.6. Gain, bandwidth, current relation of a differential amplifier

## 4.2 Basic Two Stage Opamp Results

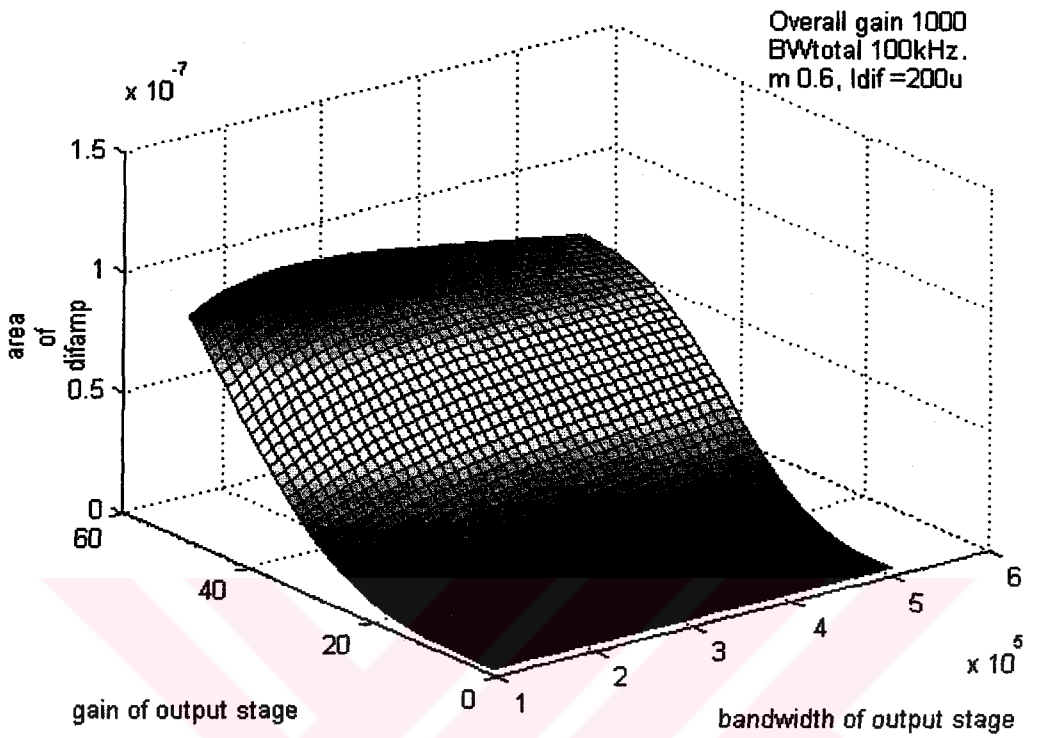



Figure 4.7. Effect of gain and bandwidth of the output stage on difamp area

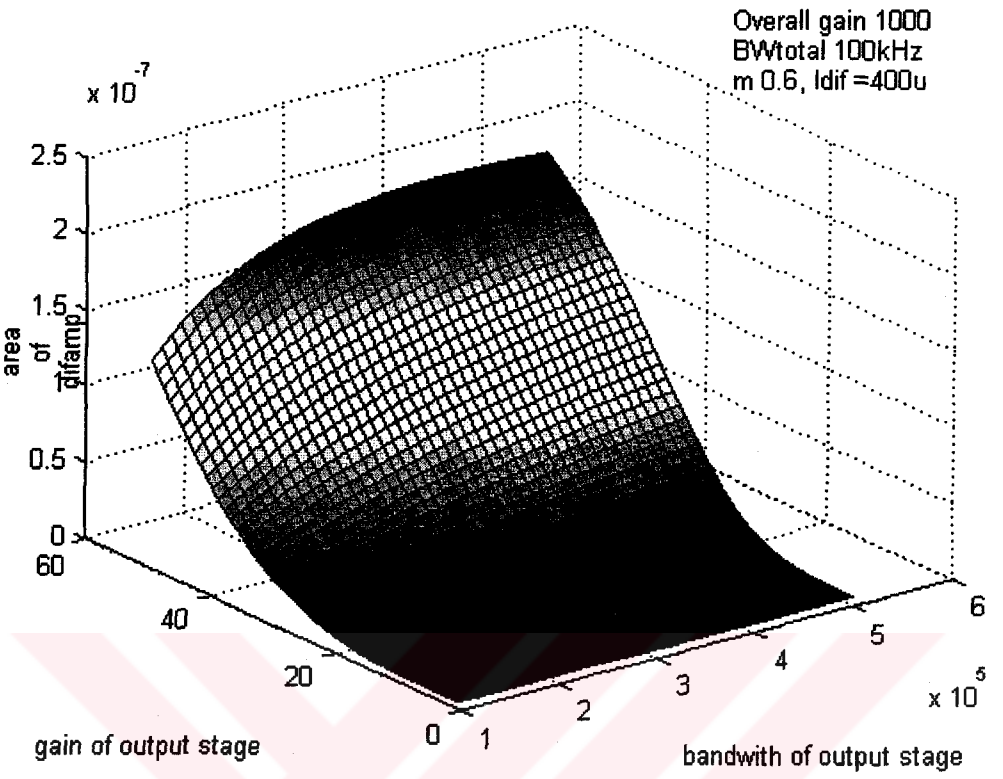



Figure 4.8. Effect of differential amplifier current and gain-bandwidth of the output stage on differential amplifier area

In the above figure, effect of increasing differential amplifier current can be seen. In fact increasing current will result in an increase in area.

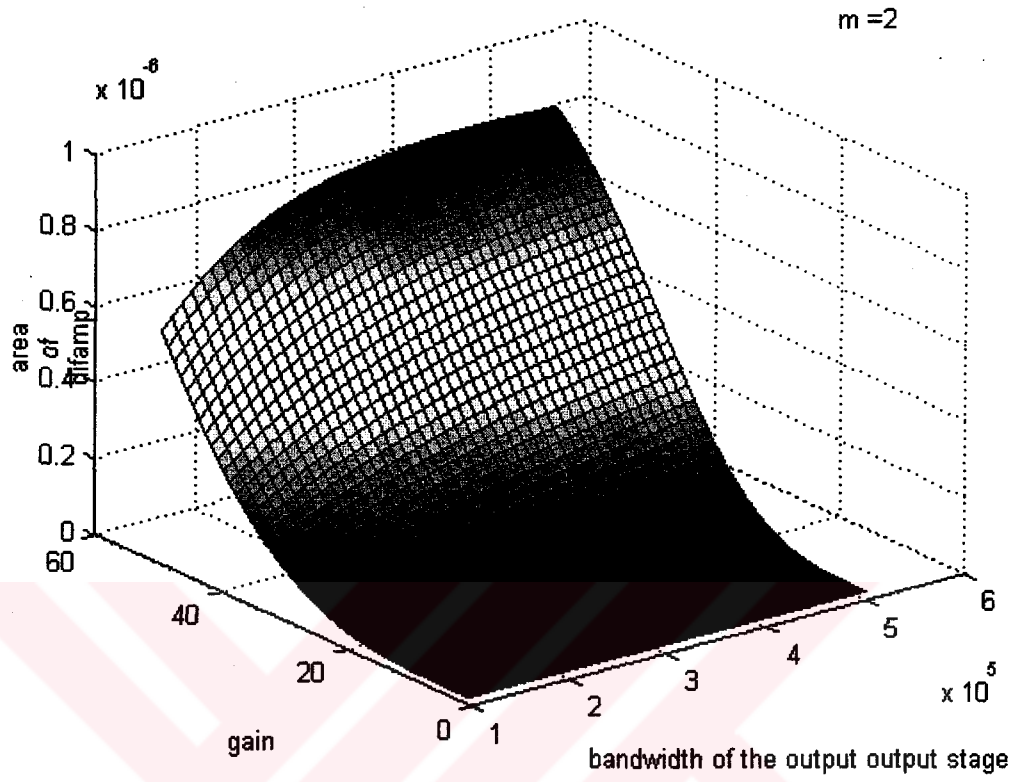



Figure 4.9. Effect of parameter m on the differential amplifier area

It can be seen in Figure 4.9, that increase in 'm' will decrease the area for a gain and bandwidth.

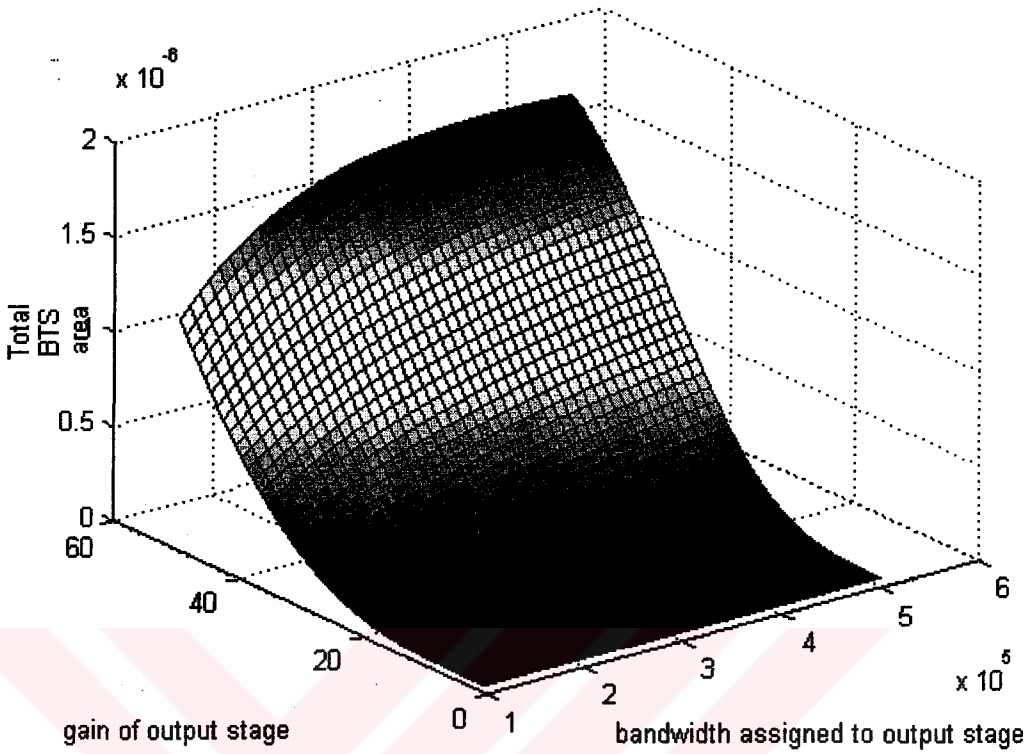



Figure 4.10. Effect of output stage's bandwidth and gain to total BTS area

The total opamps area is a similar figure in shape. Again increasing M or increasing differential amplifier current increases the area.

# 5. CONCLUSION

In this thesis an Analog Performance Estimator which will be used with circuit level synthesizer (usually it consist an optimizer). The performance specifications coming from system level synthesis tool is examined somehow if it is feasible to ease the job of the circuit level synthesizer. Moreover, it can be used for determining the tradeoff relations of the circuit performance parameters (such as area, bandwidth, power).

The analytical equations which are used to solve the subcircuit performance parameters in terms of each other will speed up the process which is superior to the systems that use detailed circuit simulation for every point and then after grouping the result getting the performance response to other independent variables.

The performance response graph similar to that is given in the below chapter also gives ideas of circuit tradeoffs to the designer, therefore it can be used as a standalone tool.

Some of the analog blocks used in circuit design such as source follower are not implemented due to the lack of time. Also an automatic equation constructor for use with analog circuits can be implemented as a future work.

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