Characterization of Perovskite-like High k Dielectric Materials for Metal-Insulator-Metal Capacitors

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Abstract

Metal-Insulator-Metal (MIM) capacitors are one of the key building blocks in radio frequency analog/mixed signal integrated circuits. According to International Technology Roadmap for Semiconductors requirements, MIM capacitors should exhibit high capacitance densities accompanied with low leakage current density, small voltage dependency and high quality factor for future applications. However, based on conventional dielectric materials, like SiO_2 and Si_3N_4, it is not possible to meet these requirements mainly due to limited capacitance density values and reliability issues. Therefore, there is urgent need to replace the conventional dielectric material with high dielectric constant materials as this is the most promising solution.

In this thesis, the focus is on screening of different alternative dielectric materials using single or multilayer dielectric structures for future MIM capacitor applications. Moreover, influences of post-deposition annealing and electrode materials on MIM capacitor properties are investigated. Special attention is given on the characterization of MIM capacitors in terms of physical and main electrical properties.

Zusammenfassung

MIM-Kondensatoren sind eine wichtige Schlüsselkomponente in integrierten Analog/ Mixed-Signal Hochfrequenz-Schaltkreisen. Entsprechend der International Technology Roadmap for Semiconductors sollen MIM-Kondensatoren für zukünftige Hochfrequenzanwendungen hohe Kapazitätsdichten bei geringen Leckstromdichten, geringe Spannungsabhängigkeiten sowie hohe Gütefaktoren aufweisen. Aufgrund der begrenzten Kapazitätsdichte und Zuverlässigkeit von SiO_2 and Si_3N_4 erscheint es nicht möglich diesen Anforderungen mit konventionellen Dielektrika gerecht zu werden. Deshalb besteht die zwingende Notwendigkeit konventionelle Dielektrika durch high k Dielektrika zu ersetzen.

In dieser Dissertation liegt der Fokus auf der Untersuchung von verschiedenen alternativen Dielektrika unter Verwendung ein- und mehrlagiger Dielektrikumsstrukturen für zukünftige MIM-Kondensator Applikationen. Es werden Einflüsse von nachfolgenden Ausheilungsprozessen und verschiedenen Elektrodenmaterialien auf die Eigenschaften der MIM- Kondensatoren untersucht. Dabei soll speziell die Charakterisierung von MIM-Kondensatoren in Bezug auf physikalischen und elektrischen Eigenschaften Beachtung geschenkt werden.

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1 Overview

1.1 General Introduction & Dissertation Aim

The semiconductor industry has been pushed by the drive for lower cost of modern electronic systems including computers, mobile phones etc., in order to develop integrated circuits (ICs) with increased levels of integration, performance and functionality. Over the last 40 years, amazing progress has been made in silicon technology. It has been accomplished by the continued shrinking dimensions of semiconductor devices which results in a constant increase in the number of components per chip. This phenomenal trend is popularly quantified as “Moore’s Law” predicting that the number of components per chip doubles every 18 month [1].

Moore’s law has allowed the development of complementary metal oxide semiconductor (CMOS) technologies with the required performance and precision for radio frequency / analog mixed signal (RF/AMS) circuits, and for digital signal processing circuits as well. However, the silicon based microelectronics industry is rapidly coming close to a point where device fabrication can no longer be simply scaled to a progressively smaller size. On the other hand, the new generation CMOS technologies already provide RF CMOS transistors with sufficient performance. However, the semiconductor industry still needs to continue to improve low cost/high performance technologies. In parallel with this requirement, there is a concept called “More than Moore” which emphasizes the necessity of specialized functionality introduction among ICs for the next generation rather than transistor density. These functionalities can be introduced by including components such as sensors,

optoelectronics (Si-photonics), passives etc. Among them, performances of passives always play a significant role in determining the overall characteristic of the entire circuits. In particular, metal-insulator- metal (MIM) capacitors are key components being widely integrated and finding many applications among RF and analog ICs.

The conventional MIM capacitor structure consists of SiO_2 or Si_3N_4 as dielectric and TiN as metal electrode. The capacitance densities of the MIM structure fabricated from these materials are in the range of 1 to 2 fF/μm^2 due to low k value of the dielectric materials ($k_{(SiO_2)}$=3.9 [2], $k_{(Si_3N_4)}$ =7.5 [3]). However, the continuous progress in RFIC in terms of packing density and cost requires MIM capacitors to have higher capacitance density. According to ITRS [4] the required capacitance density for near future devices is in the range of 10 fF/μm^2 and it should be accompanied with a high level of performance (low leakage current density, high breakdown voltage, and high voltage linearity).

The required capacitance density in MIM capacitors can be achieved by employing either thinner insulator or high dielectric constant (k) materials according to the simple parallel plate capacitance equation. The solution of scaling down insulator thickness for the case of current SiO_2 or Si_3N_4 dielectric materials is limited due to limited capacitance density and reliability issues. Therefore, use of high k materials is considered the most promising solution in order to meet the requirements of MIM capacitors in Si RF analog/IC applications. More significantly, in the efforts to keep on the Moore's Law curve, introduction of high k dielectric materials into IC's has already been established. As the traditional SiO_2 gate insulating layer has been slimmed with each new generation, and thus reached a few atomic layer thickness

where even one more tenth of nanometer shrinkage is not possible, a significant innovation was done by using high k oxide material. Tunneling leakage current resulting in increasing power dissipation and heat was a critical issue, but in 2007, Intel successfully demonstrated high volume production of 45 nm high k–metal gate microprocessor chips [5]. The gate oxide dielectric consisted of ~3 nm HfO_2 (with a dielectric constant k = 25) and replaced the previously used SiO_2 (k = 3.9). Moreover, high k dielectrics are of great interest for metal-insulator-metal capacitor applications as well as in mass storage memory devices such as Dynamic Random Access Memory (DRAM), microwave communication devices and other CMOS devices which require a high capacitive coupling.

Introducing a new high k dielectric material faces several challenges. High k dielectrics enable higher capacitance densities, but they generally result in degraded capacitance-voltage linearity and high leakage current density compared to the conventional dielectric materials. This is mostly related to the dielectric properties in the MIM stack such as microstructure, impurities, surface roughness etc. These properties should be simultaneously optimized to have a good dielectric behavior and thus a high performance MIM capacitor. Besides that, one should also consider the whole MIM structure including dielectric/metal electrode interface in order to optimize the MIM capacitor performance. An interface formation between dielectric and metal electrode might degrade the performance of MIM capacitors. Moreover, an integration of new high k dielectric material into standard back end of line (BEOL) of the CMOS technology is challenging. The candidate material might not be compatible with the requirements of the technology and might need specific process conditions. Mostly, BEOL thermal budget of CMOS process (400 °C) is the main constraint

which limits the use of many alternative high k dielectrics since they usually need higher process temperature. It is also very critical to avoid possible cross-contamination so that high k materials can be introduced without disrupting the silicon wafer processing line.

In literature, numerous dielectric materials have been studied concerning the alternative high performance MIM capacitor. The studied dielectric materials have been mostly chosen due to their high bulk k value. Despite the fact that there has been some progress, the status is that no existing dielectric material matches with the requirements entirely. Therefore, some alternative dielectric configurations have been developed to optimize the properties of MIM capacitors, such as stacked or sandwiched multilayer dielectrics. However, to the best of our knowledge, no satisfied MIM structure has been represented by these approaches so far.

In this thesis, **the main aim** is to screen alternative dielectric materials for future MIM capacitor applications. Some alternative dielectric materials are investigated in MIM structure, such as Ce-Al-O, Sr-Ta-O, and $SrTiO_3$. Unlike most of the work related to MIM capacitors, this study considers a feasible integration method of system in package (SiP) rather than integration into BEOL of standard CMOS process since alternative high k materials mostly require high processing temperatures. Integration method of SiP allows us to ignore several constraints of standard CMOS process such as thermal budget. Therefore, the performances of the MIM capacitors are also investigated after applying a high temperature post-deposition annealing process. As one of the concerns with many high k dielectric materials is high leakage current, capacitance density and leakage current of

dielectrics in MIM structures are the most important parameters considered in this thesis. In addition, structural characterization analyses are also performed on the dielectric material itself and the dielectric/metal electrode interface in order to optimize the MIM properties. As an alternative method, different dielectric configurations are utilized. The stacked or sandwiched structure of multilayer dielectrics constituted from $SrTiO_3$/Sr-Ta-O and $SrTiO_3/Al_2O_3$ are investigated for the optimum response in terms of MIM properties and are compared with respect to single $SrTiO_3$ dielectric MIM structures.

1.2 Dissertation Organization

This dissertation is organized into 5 chapters. Chapter 1 gives a general overview on MIM capacitors and the aim of the thesis.

Chapter 2 describes the general properties and the integration options of MIM capacitors. It is followed by an explanation of the drawbacks and the key requirements of MIM capacitors. Particular attention has been given to challenges for scaling in MIM capacitors. The chapter ends with a systematic literature review concerning alternative dielectric materials for MIM capacitor applications.

Chapter 3 presents a brief description of the experimental techniques used for the deposition and the characterization of the dielectric and the electrode layers of MIM capacitor structures studied in this thesis. The utilized instruments and the tool conditions used during the experiments are introduced as well.

Chapter 4 presents the results of the investigated MIM capacitor structures. The chapter includes two parts. In the first part, results for MIM capacitor structures

with single layer dielectric are given. MIM capacitors consisting of Ce-Al-O and Sr-Ta-O as dielectric are investigated in terms of their physical and electrical characteristics. Moreover, a high temperature post-deposition annealing process has been performed and its influence on the performance of the MIM capacitors has been presented. In the second part of the chapter, MIM capacitors including multilayer dielectrics are presented. A combination of dielectric layers constructed from Sr-Ta-O/$SrTiO_3$ and Al_2O_3/$SrTiO_3$ are optimized and characterized for MIM capacitor applications.

Finally, chapter 5 summarizes the results obtained in this thesis and concludes with future work suggestions.

2 Introduction

2.1 MIM Capacitors

With the rapidly growing wireless communication market, the need for high performance RF and AMS integrated circuits has increased significantly. In contrast to digital CMOS integrated circuits, the performance of many RF and AMS ICs are mainly dependent on the performance of passive components [4]. Capacitors can be considered as one of the most commonly used passive components.

The first used capacitor in Si based ICs was based on metal-insulator-silicon (MIS) structure. Afterwards, it was replaced by polysilicon-oxide-polysilicon (double-poly) capacitors due to the better electrical performances of double-poly structures in terms of small capacitance variation. However, the performances of these passive devices fabricated during front end processing degrade especially when used at high RF frequencies. This limitation in quality is primarily due to large resistive loss from the electrodes, and parasitic capacitance due to the silicon substrate [6].

Currently, a metal-insulator-metal (MIM) structure has been favored as a capacitor owing to its low parasitic coupling to the silicon substrate and highly conductive electrodes reducing the contact resistance [7, 8]. In addition, they have some other advantageous properties compared to the other capacitor structures, such as low voltage and temperature coefficients, low leakage current, and ability to withstand higher application voltage [9]. Consequently, MIM capacitors have generated great interest for applications such as radio frequency and analog Si integrated circuits [10].

2.1.1 Integration Concepts of MIM Capacitors

The integration of MIM capacitors can be done with various techniques, including system on chip (SoC) and system in package (SiP) approaches. These approaches have different advantages and limitations. The following parts give a brief overview about these two techniques.

System on Chip Approach

During the last several decades, the SoC approach has been widely used in the consumer electronic industry. SoC is based on the integration of all functions into one single chip. Therefore, its most important advantage is a high level of integration. BEOL integration of MIM capacitors is one of the most common examples of SoC passive integration. Fig. 2.1 shows the generic cross-sectional view of the integration of the MIM capacitor into IHP's high performance 0.13 µm BiCMOS technology with seven Al metallization layers BEOL. The MIM capacitor is integrated between the fifth and the sixth metal layer. The capacitor's bottom electrode is a metal stack consisting of Ti/TiN/AlCu/Ti/TiN, while the capacitor's top plate is a single PVD TiN metal.

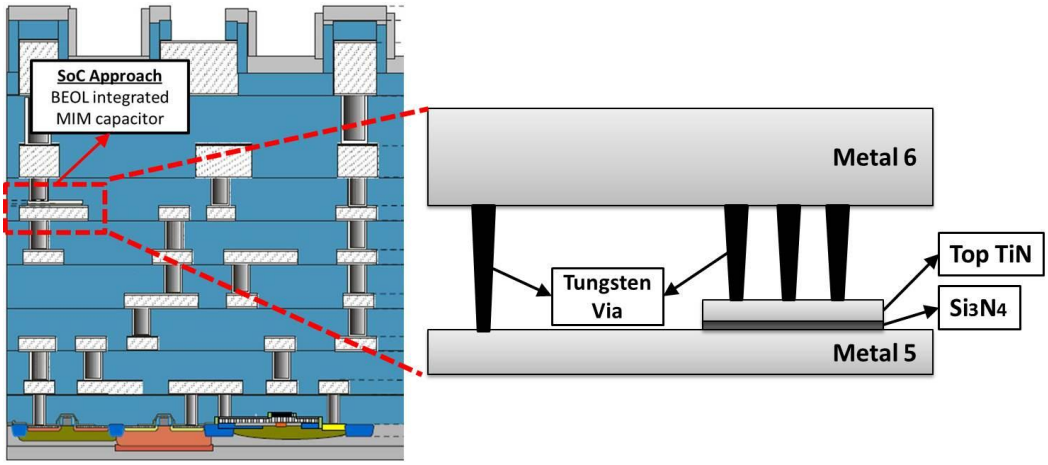

Fig. 2.1 Generic cross-sectional view of IHP's 0.13 µm BiCMOS technology and the integration scheme of MIM capacitor in BEOL.

The dielectric is Si_3N_4 deposited by plasma enhanced chemical vapor deposition (PECVD), at a temperature below 400 °C, which satisfies the thermal budget limitations of the BEOL process. The SoC approach had been widely used before the technology node of CMOS reached the range of few tens of nanometer. The fast shrinking of CMOS technology has a strong benefit to the digital circuit blocks. However, it has become more difficult to integrate any kind of new passive components into these technologies due their high complexity and sensitivity. Therefore, there is a need for new techniques to integrate digital circuits together with high frequency blocks and high quality passive components in next generation communication systems.

System in Package Approach

Recently, with the expectation of increasing complexity and sensitivity of future CMOS devices, SiP is seen as the most convenient integration approach. It introduces the concept of integrating several analog or digital ICs together in a single package. In other words, SiP contains several dies, combined with other passive components on a single substrate.

Fig. 2.2 shows different approaches to realize the SiP concept. As can be seen from the figure, the SiP approach starts from a very basic horizontal placement and by wire or flip chip bonding the chips are assembled to very complex embedded solutions.

Fig. 2.3 shows the comparison of new and old generation SiP approach. The figure seen on the left hand side represents a low density integration of the chips with a horizontal placement on the board while the figure at the right hand side depicts

compact highly integrated chips which can be considered as a stacked SiP approach using both bond wiring and flip-chip techniques. More advanced techniques to achieve higher level integration are being developed such as 3D chip stacking or interposer techniques [4].

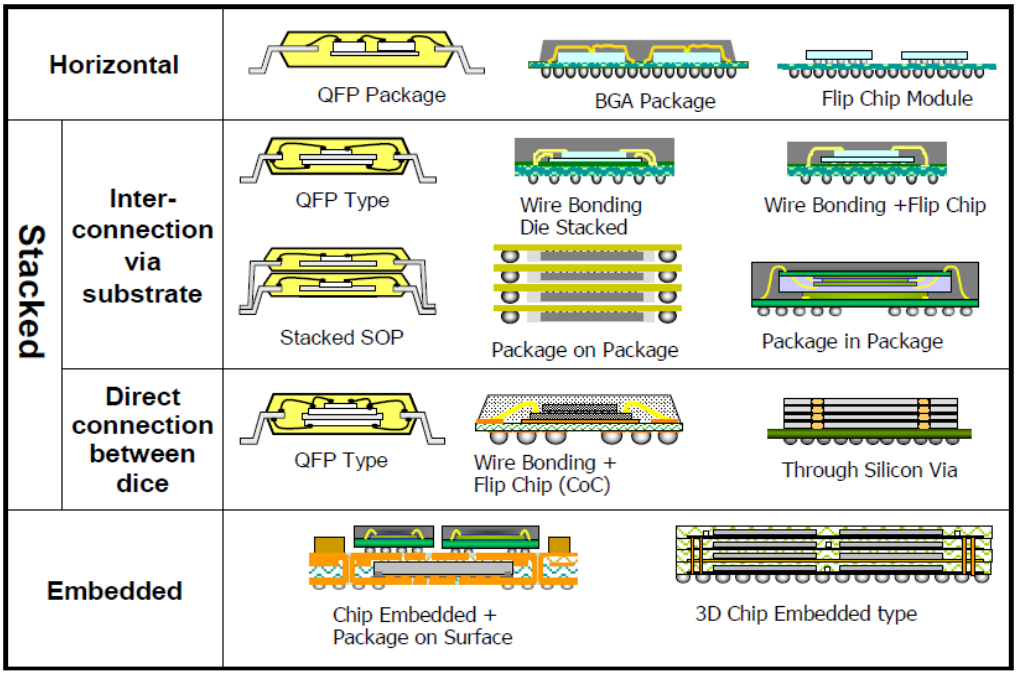

Fig. 2.2 Different techniques of SiP integration [4].

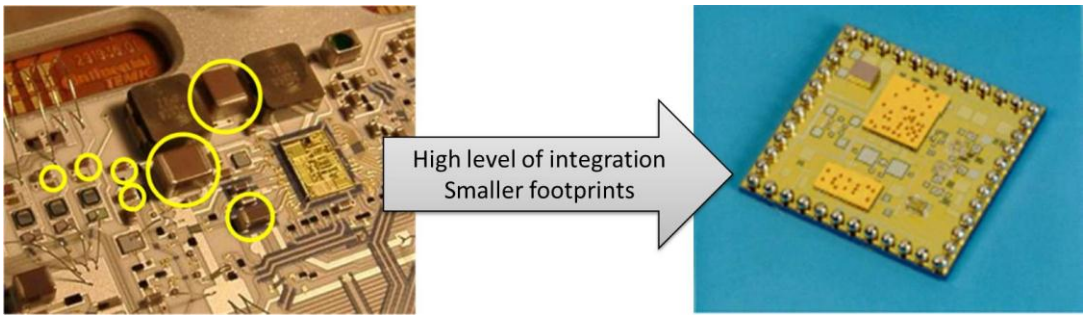

Fig. 2.3 A comparison between old and new types of SiP approaches.

As can be seen from Fig. 2.3, the SiP approach provides the flexibility to develop different technologies independently from each other and therefore, paves the way to develop new processing techniques for passive devices independent from CMOS process limitations. In summary, the SiP approach clearly allows the use of

new alternative CMOS non-compatible materials and different process conditions (i.e high temperature) to improve the performance of MIM capacitors.

2.1.2 Parameters of MIM Capacitors

The simple parallel plate structure of a MIM capacitor is seen in Fig. 2.4. The dielectric film is sandwiched between the bottom and the top metal electrodes. The insulator is usually made of a thin dielectric with a thickness of approximately ~50 nm in the state of the art BiCMOS technologies.

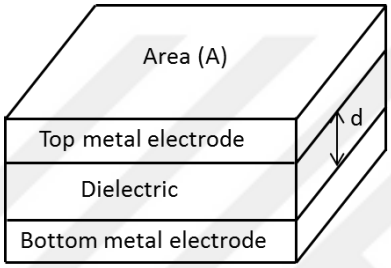

Fig. 2.4 Simple schematic structure of a parallel plate MIM capacitor.

MIM capacitors can be characterized by several physical parameters. The key parameters for MIM capacitors are capacitance density, capacitance-voltage linearity, leakage current density, breakdown voltage and quality factor.

Capacitance Density

As the most important parameter of MIM capacitor, the capacitance density can be estimated by the general formula of the parallel plate capacitors, that is:

$$C = \frac{(k \times \varepsilon_0 \times A)}{d} \qquad \text{Equation 2.1}$$

where k is the dielectric constant (also referred to as the relative permittivity) of the material, ε_0 is the permittivity of free space (8.85 x 10^{-12} F/m), A is the area of the capacitor and d is the thickness of the dielectric. The capacitance density (C/A,

fF/μm^2) shows the capacitance per unit area in MIM devices. The capacitance of a MIM capacitor with parallel electrodes is directly proportional to the active electrode area and the k value of the dielectric material while it is inversely proportional to the dielectric thickness as described by the Equation 2.1.

As capacitance density is a direct function of the dielectric constant, it is important to know how dielectric materials properties could influence the k value. The dielectric constant indicates the ability of a dielectric material to store charge. It is determined by polarizability of a dielectric material when it is exposed to an electrical field. In other words, k value is a measure of the change in a molecule's electron distribution in response to changing electric interactions. The polarizability of a dielectric material depends on several factors including the density of electrons, the crystal structure, and the dopants [11].

In general, atoms with a large ionic radius (e.g. high atomic number) exhibit strong electron dipole response to an external electric field, because there are more electrons to respond to the field. This electronic contribution tends to increase the permittivity of higher atomic number atoms. For example, transition metal oxides typically have higher dielectric constants than the oxides of lighter elements like Si and Al [12]. Therefore, higher density of electrons is preferable for high k value of a dielectric material. In addition, crystallization type of the dielectric material has an enormous effect on the k value of a dielectric. Depending on the location of ions in a crystal structure, the k value is varied. It has been reported on many occasions that the rutile phase of TiO_2 gives a higher k value than the anatase phase of TiO_2 [13]. The enhancement of k value through structural transformation is explained either by

increasing molar polarizability or by decreasing molar volume in the dielectric material according to the Clausius-Mosotti equation [14] which is expressed as follows;

$$k = \frac{1+(8\pi\alpha_m/3V_m)}{1-(4\pi\alpha_m/3V_m)} \quad \text{Equation 2.2}$$

where α_m and V_m are the molar polarizability and the molar volume, respectively.

Apart from the type of crystal structure, k value of oxide dielectric film is strongly dependent on whether the material is amorphous or crystalline. The crystalline films offer much higher dielectric constants than their amorphous counterparts for the dielectrics [15, 16]. This tendency of k value is attributed to the higher density of the crystalline state of the dielectric materials.

Dopants in dielectric materials also impact the overall k value. Impurities like carbon are generally expected to lead to a reduction in the dielectric constant. For example, fluorine or carbon doped silica results in a lower dielectric constant value compared to the pure one. Both fluorine and carbon increase the inter-atomic distances or “free volume” of silica which provides an additional decrease of the dielectric constant [17]. However, it should be noted that there is an exception of intentional doping of high k perovskites which results in a very high dielectric constant [18].

Capacitance Voltage Linearity

Capacitance-voltage linearity of MIM capacitors indicates the dependence of the capacitance variation on the applied bias voltage in MIM devices. For a precise

MIM capacitor, it is essential the capacitance variation with voltage fluctuation to be as small as possible on a chip.

The dependence of capacitance on voltage can be approximated by the second order polynomial equation [19] shown as Equation 2.3;

$$\frac{C(V)}{C_0} = \alpha V^2 + \beta V + 1 \qquad \text{Equation 2.3}$$

where *C(V)* is the capacitance measured at a voltage bias of *V*, C_0 is the capacitance measured at zero bias, while α and β are two fitting parameters called quadratic and linear voltage coefficients of capacitance, respectively. The emphasis on the capacitors is second-order voltage linearity (α value) since it is critical for the dynamic range of analog circuit as highlighted in ITRS 2009.

There have been many papers regarding optimization of the voltage linearity of MIM capacitors. Nevertheless, the physical explanation of the underlying mechanism controlling the α value of MIM capacitors is not completely understood. Several modeling approaches have been studied to clarify the corresponding mechanism [20, 21, 22]. These models generally explain voltage linearity either by a dielectric bulk effect or dielectric/electrode interface effect. Additionally, it has been reported that voltage dependence of capacitance depends on the thickness of dielectric films. Both experimental and theoretical works have shown that the α value is inversely proportional to the dielectric thickness ($\alpha \sim 1/d_{ox}^2$) [23]. This is explained by the higher electrical field of thinner dielectric films at the same applied voltage which results in higher polarization, and thus a higher capacitance variation. For that reason, capacitance density and alpha value are in a trade-off relationship which

makes the simultaneous achievement of large capacitance density and capacitance-voltage linearity difficult. The capacitance variation has also been reported to be dependent on the measured frequency. Alpha values become smaller when the measured frequency increases. This is also related to the reduced polarization by increasing frequency [6]. The charge mobility becomes smaller with increasing frequency which leads to higher relaxation time and a smaller capacitance variation [24]. Another proposed model is reported by Wenger et. al, in which several fundamental physical phenomena have been considered, such as electrostriction, coulomb interaction, and nonlinear electronic polarizability.

According to the model the quadratic voltage coefficient *α* in Equation 2.4 can be identified as:

$$\alpha = \frac{2n_2 n_0}{k_0 d^2} \qquad \text{Equation 2.4}$$

where the coefficient α is dependent on the refractive index n_0, the linear dielectric constant k_0, and the nonlinear refractive index n_2, whereby n_2 strongly depends on k_0 [25].

Leakage Current

Leakage current as another critical parameter of the MIM capacitor specifies the stability of the dielectric material in the device. Leakage current through a MIM capacitor causes an increase in power consumption and if sufficiently high, can be the reason of complete circuit failure.

The measured resistivity of a dielectric material is not an intrinsic property of the material and can be controlled by the crystallinity, purity and stoichiometry of the

material. For example concerning crystallinity of the dielectric, it has been reported that even thicker crystallized dielectric films exhibit a deteriorated leakage current performance compared to its amorphous counterparts [26]. The effect of crystalline structure on degradation of leakage current can be attributed to the grain boundaries in crystalline material. They are known to create a path for electrons, thus, causing a higher leakage current through the dielectric material.

From the dielectric's purity point of view, leakage current through dielectric materials is affected by the number of impurities in the dielectric. This is because they can create defect sites or act as mobile ions in dielectric. Therefore, a lower amount of carbon is desirable for lower leakage current density through dielectric film as proved for HfO_2 for gate dielectric application [27].

A variation from an ideal stoichiometry can also result in a dielectric becoming highly conductive as reported by Kukli *et al.* for TiO_2 [28]. In addition, the work function of metal electrodes, interfacial layers, and surface roughness are also known as determining factors of leakage current in MIM capacitor [6].

Fowler-Nordheim tunneling is one of the important conduction mechanisms. The process is based on tunneling of electrons through a barrier in the presence of a high electric field. This quantum mechanical tunneling process is observed for thin films especially for MOS structures. According to the observations, current in a MIM device can flow through the insulating film mainly by two conduction mechanisms such as Schottky emission and Poole-Frenkel (PF) emission [29]. Schottky emission is based on the electron flow from the Fermi level of electrodes directly into the conduction band of the dielectric due to high electrical field. The interface properties

between dielectric and electrode material are very important for this kind of current mechanism. A high work function electrode material such as Pt is known to reduce leakage following this mechanism. For the case of Poole-Frenkel type of emission, electrons flow through the traps caused by structural defects in dielectric materials. These traps hinder the transport of electrons in the conduction band by drift and diffusion mechanisms and trapping/detrapping of electrons become the dominant processes that control the conduction-electron density in the insulating films [30].

Breakdown Voltage

Breakdown voltage is a parameter which determines the lifetime (or reliability) of MIM devices. In fact, the term is related to dielectric material and indicates the maximum voltage value of the potential difference that the dielectric material can withstand without losing its dielectric properties. Consequently, its determination is done by sweeping the voltage (electric-field) at a specified rate and then recording the field at which one observes an abrupt increase in leakage current through the dielectric. High breakdown voltage (or breakdown strength) of dielectric material is desirable for a highly reliable MIM devices.

In general, high k dielectrics tend to have low breakdown strength. However, the physics behind this tendency is not well understood. Nevertheless, the breakdown in high k dielectrics has been found approximately proportional to $(k)^{-1/2}$ [31]. Moreover, the defect density in dielectric material is known as an essential property concerning the breakdown strength of the material, since defects can cause unreliability as a starting point for electrical failure and breakdown of the oxide. Electrically active defects are defined as atomic configurations which give rise to

electronic states in the band gap of the oxide. Typically these are sites with an excess or deficit of oxygen or impurities in high k oxides [32]. The high k oxides generally show a high intrinsic defect concentration because their bonding cannot relax easily [33]. Therefore, several strategies have been attempted to reduce defect densities in dielectric materials such as processing control and high temperature annealing.

Quality Factor

Quality factor (also known as the inverse of dissipation factor or tanδ) is one of the most important parameters for evaluation of a MIM capacitor. It has a conspicuous impact on the performance of the capacitor.

The theoretical treatment of capacitors tends to assume they are ideal or "perfect" devices, contributing only capacitance to the circuit. However, except for the ones constructed with superconducting materials, all the components in physical devices contain some resistance. These resistances cause losses in energy and are sourced from the dielectric material itself or from the electrode material in MIM capacitors. A MIM capacitor with high quality factor is demanded and indicates a low loss status.

The quality factor (Q), is a dimensionless number and is equal to the capacitor's reactance divided by the capacitor's parasitic resistance as shown in Equation 2.5 [34]. The value of Q changes dramatically with frequency as both reactance and resistance change with frequency.

$$Q = \frac{1}{tan\delta} = \frac{reactance\ of\ the\ capacitor\ in\ ohms}{equivalent\ series\ resistance} \qquad \text{Equation 2.5}$$

Fig. 2.5 shows a typical Q factor with the main parameters influence. The quality factor depends mainly on the value of the capacitor and on losses. But the inductive effect of the electrodes limits its maximum frequency of use.

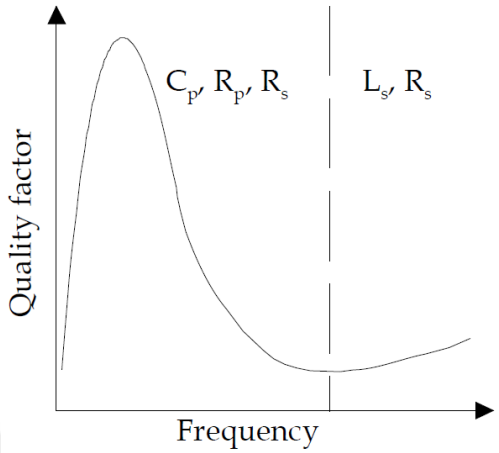

Fig. 2.5 Q factor vs. frequency [34].

The effects of the losses in dielectric materials on the performance of MIM capacitors are well-known, but the phenomenon is not yet well understood. In practice, it has been found that a lower dissipation factor is associated with materials of lower dielectric constant. Higher permittivity materials, which develop this property by high polarization mechanisms, display a higher dissipation factor. For instance, dielectric losses have been studied for some alternative high k dielectrics [35]. According to that, the dielectric losses of all alternative high k materials were at least an order of magnitude higher than the dielectric loss for SiO_2.

2.2 The Challenges in Scaling of MIM Capacitors

The drawback of the current MIM capacitors is the scaling issue. Scaling down in passive MIM capacitors is quite slow compared to the case for transistors, which is about 50 % in length every two years for MOSFETs. Therefore, it is essential to

reduce the capacitor area as the percentage of chip area used by capacitors significantly increases with the scale down of logic parts. If the area occupied by MIM capacitors on the chip could be minimized, this would allow for more compact designs at high speed with improved performance, smaller die size, and lower cost [36].

The need to integrate high density and high quality MIM capacitors in a cost effective way follows the guideline published in the international technology roadmap for semiconductors (ITRS). ITRS envisions how each design parameter of MIM capacitors will scale in future years. According to that, MIM capacitors for RF and AMS applications should have a high capacitance density, low leakage current density, small voltage linearity, and high quality factor. The requirements for the next decade are listed in Table 1. In order to realize future MIM devices, the required parameters should be achieved simultaneously.

Year of production	2012	2016	2020
Capacitance Density ($fF/\mu m^2$)	5	7	10
Voltage Linearity (ppm/V^2)	<100	<100	<100
Leakage Current (A/cm^2) @ ±2V	<1e-8	<1e-8	<1e-8
Q factor (5 GHz for 1pF)	>50	>50	>50

Table 1. Main requirements for high density integrated MIM capacitor according to ITRS by years [4].

The traditional dielectric material for MIM capacitor was SiO_2 because of the excellent insulating properties. But, the capacitance density is only around 1 $fF/\mu m^2$ due to its low k value of 3.9 and far from the value for future MIM capacitors. In order

to fabricate such devices mentioned in Table 1, one can either scale down the thickness of the dielectric materials or use a dielectric with higher k value to increase the capacitance density. However, the leakage current and reliability issues restrict the aggressive thickness down-scaling in the case of SiO_2 [6].

Currently, Si_3N_4 is in use as a dielectric in MIM capacitors owing to its higher k value of 7.5. By this replacement, the capacitance density was improved from the value of ~0.5 to ~2 fF/μm^2 depending on the technology node [37]. Although MIM capacitors with Si_3N_4 show very good leakage and voltage linearity properties, their capacitance values do not meet the values which are presented in ITRS for the coming years (Table 1). Moreover, thickness scaling down of Si_3N_4 is also not a promising method due to leakage and reliability issues.

More recently, as an alternative method, a move from 2 fF/μm^2 to 4 fF/μm^2 has been enabled by stacking of a 2 fF/μm^2 capacitor (with Si_3N_4 as dielectric material) on two metal layers [38]. Although it is convenient from the simple use of conventional dielectric material point of view, the processing of this capacitor structure requires doubling the mask levels and process steps. It should be also added that there is a promising approach for obtaining high capacitance density in MIM capacitors e.g. 3D architecture. In this method, the capacitance density is increased by increased electrode area. Depending on the width and depth of trenches capacitance density increases by a factor of three or higher compared to a standard planar MIM architecture. Benefits aside, the method presents some challenges in terms of processes. Filling high aspect ratio trenches requires high conformity deposition techniques such as Atomic layer deposition. In addition, a very

accurate polishing step is required in order to remove the excess material and to minimize the mismatch on achieved capacitance value [39].

The development in MIM capacitor density integrated with RF CMOS and BiCMOS is summarized in Fig. 2.6 [40]. It has already been emphasized in previous years that high k dielectric materials are the solution concerning the scaling issue in MIM capacitors. They are seen as the viable solutions achieving very high capacitance density with relatively thick films. In fact, HfO_2 [5] and Ta_2O_5 [41] are already in use as high k dielectric materials for transistor and capacitor applications, respectively. New alternative high k dielectrics are still being evaluated for MIM capacitor applications. It could be expected that further development in the processing technology of high k dielectric materials, could push the MIM capacitors to higher densities in near future.

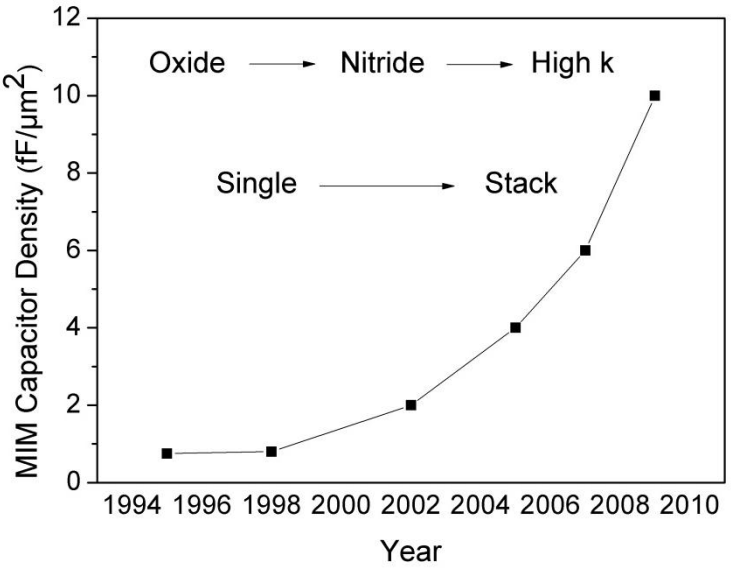

Fig. 2.6 MIM capacitor density plotted as a function of year of introduction [40].

On the other hand, keeping all the key parameters of MIM capacitors in the required range simultaneously by using high k materials is not a straightforward task.

High k dielectrics enable higher capacitance densities, but they generally result in challenging properties such as degraded capacitance-voltage linearity, and high leakage current as mentioned in detail in the previous section [11].

Unlike SiO_2, which is an almost ideal insulator, high k dielectrics usually contain plenty of bulk traps and interface states, especially after electrical stress [42]. These kinds of defects cause instability of devices during operation, which leads to the distortion of performance of MIM capacitors.

Moreover, because of their deposition method, most of the high k dielectric materials
need to be processed at high temperatures. Also, it is known that densification and improvement of crystallinity of dielectric materials occur by applying high temperature processes [43, 44]. Therefore, high temperature process is unavoidable for employing high k materials in MIM capacitor structure. However, one should consider that high temperature processes can lead to a number of problems.

First of all, in terms of CMOS compatibility high temperature applications can be a problem. In standard CMOS technology the BEOL process is limited to a thermal budget of about 400 °C. The high k dielectric process temperatures are generally much higher. It is also noteworthy to mention that the new high k material should not cause any cross contamination. Therefore, their introduction into a standard CMOS process has been limited so far.

Secondly, high temperature processes can degrade the interface quality between the layers of the MIM capacitor stack. In an ideal case, the electrode materials should act as a diffusion barrier against interaction between dielectric and

the underlying substrates. However, a high temperature process might accelerate diffusion of atoms, molecules or ions from one layer into another one and cause a degradation of dielectric and metal electrodes. Oxygen diffusion especially at high temperatures is a well-known problem for high k materials.

In addition to the drawbacks of the high temperature process, it is also essential to prevent the bottom electrode from oxidizing as high k films are always deposited under an ambient of oxidizing atmosphere. For instance, some low k value interfacial layers can be formed between dielectric and metal electrode layers and thus the effective dielectric constant can be reduced. Regardless of what kind of interfacial layer is formed, the overall capacitance that can be achieved with an interfacial layer/high k stack will be lower than that of the capacitance of the high k film alone. The capacitance of two capacitors in series is determined by Equation 2.6.

$$C_{total}^{-1} = \frac{1}{C_1} + \frac{1}{C_2} \qquad \text{Equation 2.6}$$

The overall capacitance of capacitors in series is dominated by the layer with the lowest capacitance, so that dielectric and electrode material interfaces are important in order to control MIM stack capacitance.

Another challenge is related to the composition of the material. Dielectric materials show their high k values for specific compositions of atoms in the components. Especially mixed oxides show their high k values in a very narrow range. Therefore, it is also important for the composition of dielectric to be kept under tight control especially after the thermal treatment.

By considering all the challenging aspects discussed above, development of the future MIM capacitor structures requires detailed physical characterization as well as electrical characterization to optimize the parameters and processing technology. As this thesis covers screening of alternative dielectric materials for MIM capacitor application, a special attention has been also given in order to characterize the samples in terms of their physical properties. Studying the dielectric itself and the interaction of the layers at the interfaces under a varying annealing temperature is of importance.

2.3 Alternative High k Dielectric Materials

High k dielectric material selection

As mentioned in the previous section, high k dielectrics have some challenges to face in order to replace the traditional dielectrics. Compared to gate dielectric application, the number of constraints on high k oxide is fewer for MIM capacitors, because the oxide is not in direct contact with any Si and it must only act as an insulator [45]. In addition, using a SiP integration approach, limitations are less critical, such as process temperatures and cross- contamination. The most important requirement is that alternative high k dielectric materials should possess much higher k values preferably larger than ~25 in order to satisfy the requirements of future MIM capacitor applications. The other important parameters are related to the band gap, morphology and interfacial quality. A high band gap value is preferred in order to limit leakage currents. It must also form a good electrical interface with the metal electrodes in terms of roughness and absence of low k interfacial layer formation [46]. Amorphous dielectric material is very useful, as it helps to cover and reduce

possible leakage paths [47]. Also as few as possible defects such as excess or deficit of oxygen or impurities are desirable in dielectric material [45]. Although, the required properties for an alternative high k dielectric material for MIM capacitor application are very clear, selection of the dielectric material is a challenging issue, as there is a tradeoff relationship between the different desired properties.

Current high k dielectric materials

Numerous alternative high k materials have been investigated to be used not only for MIM capacitors for RF and AMS ICs but also for logic devices, non-volatile memories, DRAMs and low power mixed signal components. The main motivation for the studied dielectric materials is their high k values which have been measured on bulk samples. The comparison of thin film high k dielectrics reported in the literature in terms of their MIM performance is not straightforward due to the different measurement conditions. Nevertheless, the studied alternative dielectric materials can be categorized according to their type such as binary oxides, mixed oxides and perovskite based oxides. In addition, there have also been several different attempts such as using multilayered dielectrics for high k dielectric applications. These alternative high k dielectric types will be briefly introduced with some examples reported in literature in the following parts.

- *Binary Oxide Dielectrics*

There are several binary oxide materials which have been proposed as potential dielectric materials for replacement of the traditional ones. Among them, Al_2O_3 is the most widely studied one [48]. It exhibits excellent insulating behavior due to its large Al_2O_3 band gap of 8.7 eV. However, its relatively low dielectric constant (k

~ 8-10) [6] limits the usage of Al_2O_3 for next generations of high density MIM capacitors.

Ta_2O_5 based MIM capacitors are already in use for current DRAM fabrication owing to their moderately high k value and excellent thermal and chemical stability [49]. Amorphous Ta_2O_5 films exhibit a k value of ~25 [50]. However, deposited Ta_2O_5 films typically exhibit poor leakage performance [51] which will make them difficult to use for future MIM capacitors for RF and AMS applications.

Another important candidate as an alternative dielectric material is HfO_2. It also has a moderate k value of around ~18-25 [52] but is accompanied with a large band gap value of 5.9 eV. Excellent MOS capacitors with this dielectric have been demonstrated [53]. Also its compatibility with semiconductor circuit-processing technology has been proven [54]. Its disadvantage is its low crystallization temperature of 400 °C which can promote grain boundaries within the layers to act as leakage paths and impurity getters during processing [55]. Also oxygen vacancies in this dielectric material [56] can be pronounced as drawbacks as they can cause leakage current through dielectric film.

Among binary oxide dielectrics, there is an exception in the case of the rutile phase of TiO_2 which has a k value as high as 170. However, it has a low band gap value of ~3 eV which worsens the leakage and the breakdown characteristic [57].

ZrO_2 is also one of the most studied binary oxide type dielectric materials. The highest k value of ~46 has been predicted for pure ZrO_2 crystallized to tetragonal

phase [16]. But, the high leakage current makes it inapplicable for MIM capacitors [58].

In summary, binary oxide materials seem not so promising for MIM capacitor applications, as their k values are mostly moderate (max. ~25) [59]. For some cases, the requirement for a capacitance density larger than 5 fF/μm^2 is achieved; however, the leakage current and/or the voltage linearity are much larger than the required limits, due to the trade-off relationship between them [60]. The k values of these kinds of materials tend to vary inversely with the band gap and breakdown strength as shown in Fig. 2.7. It is well-known that narrow band gaps can basically increase the leakage due to a smaller band offset when contacting dielectric material with metal electrode.

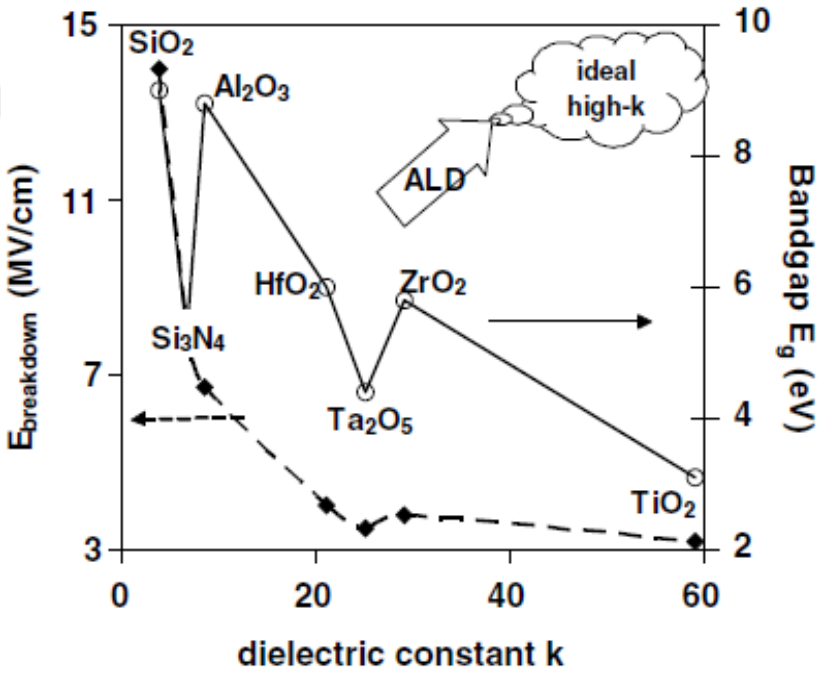

Fig. 2.7 Dielectric constant (k) vs. breakdown strength (MV/cm) and bandgap values (eV) on mostly studied binary oxide materials [61].

- *Mixed Oxide Dielectrics*

The mixed oxide dielectric materials consisting of two binary oxides exhibit superior properties compared to the simple single binary oxides. Therefore, these kinds of complex dielectrics have become dominant materials under active investigation for both gate dielectric and capacitor applications. For example, it was shown that the dielectric constant of Ta_2O_5 increased dramatically by an 8 % substitution of TiO_2 [62]. Also, in another report, it was indicated that, Al doped TiO_2 samples exhibited lower leakage current density than the undoped sample by at least one order of magnitude at ±1 V bias [57]. Additionally, by the incorporation of TiO_2 into the Pr_2O_3 matrix, the water absorption behavior of Pr_2O_3 from air was reported to be suppressed [63]. It was also demonstrated by S. J. Kim *et al.* that 4% lanthanide doping in HfO_2 can improve the two undesired properties of thin dielectric MIM capacitors, higher leakage current, and poor capacitance linearity [19]. Another promising result was obtained by mixing TaO and TiO. Added TaO inside TiO matrix was reported as blocking the TiO crystallization [64]. Therefore, a very promising leakage current of 1.2 x 10^{-8} A/cm^2 at 2 V was reported [64]. As mentioned above with several examples, impressive progresses of binary oxides has been proven by mixing the simple oxides; however, further optimization of this type of dielectrics needs to be considered in order to satisfy all the MIM properties simultaneously.

- *Perovskite based oxide dielectrics*

Recently, dielectric materials which have a perovskite structure have received an increasing attention as they exhibit very high dielectric constant values. Their crystalline structure is ABO_3 where A and B are cations. A representation of atomic

arrangement of a perovskite material is seen in Fig. 2.8. The origin of high dielectric constant of these materials is the mobility of the central ion in the oxygen octahedral [65]. This induces a strong ionic contribution to the whole polarizability. These kinds of materials show ferroelectric properties at temperatures below their Curie point. Below their Curie temperature, the ions shift to create a permanent dipole in the material and a very high dielectric constant. However, the deposition process is more complicated when compared with binaries, due to the need of strict control of the ratio of two cations. Furthermore, most of the perovskite dielectric materials are synthesized at temperatures typically around 600-700 °C [66] which does not agree with the thermal budget of standard CMOS BEOL process.

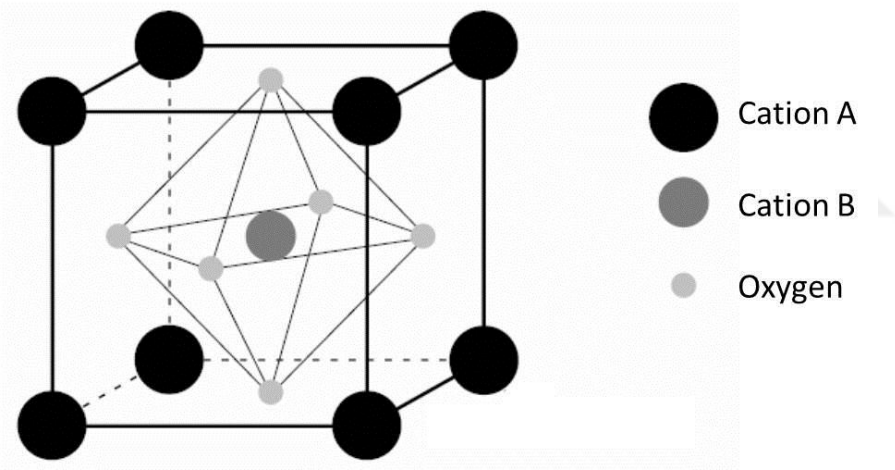

Fig. 2.8 Atomic arrangement of a perovskite material (ABO_3) [67].

$BaHfO_3$ is one of the studied perovskite based dielectrics. It was especially investigated for DRAM application and reported with a low leakage current of around 10^{-8} A/cm^2 accompanied with a k value of 23 [68]. Furthermore, the influence of partial substitution of Hf ions in $BaHfO_3$ by Ti ions on the dielectric constant was studied [69]. The authors reported that the resulting $BaHf_{1-x}Ti_xO_3$ dielectric exhibits a significant gain in k values with respect to $BaHfO_3$.

In another work, $BaTiO_3$ was deposited and after annealing at 500 °C, a k value of 165 was reported [70]. Furthermore, solid solutions of $BaTiO_3$ and $SrTiO_3$ were studied. Barium strontium titanate as a capacitor dielectric was reported to have a maximum capacitance density of 12,5 fF/μm^2 and a moderate leakage current of 4 x 10^{-5} A/cm^2 at 2 V after RTA at 700 ˚C. However, the dielectric constant was found to be highly temperature dependent. Additionally, dielectric constants of about 40 were reported for $BaZrO_3$, and $SrHfO_3$ on TiN substrates for DRAM application [71].

Material	Form	Process Temperature	k value	Reference
$CeAlO_3$	pellet	1600 °C	3000	[75]
$BaTaO_2N$	pellet	1000 °C	450	[76]
$SrTaO_2N$	pellet	1000 °C	400	[76]
$Ba_xSr_{1-x}TiO_3$	film	800 °C	230	[77]
$SrTiO_3$	film	500 °C	150	[78]
$SrTa_2O_6$	film	700 °C	100	[79]
$Sr_2Ta_2O_7$	pellet	1000 °C	80	[80]
BiTaO	film	360 °C	50	[81]
$ZrTiO_4$	pellet	1400 °C	50	[82]
$Sr_2Nb_2O_7$	film	850 °C	48	[83]
Ba_4SrNbO_{15}	pellet	1100 °C	48	[84]
$CoTiO_3$	film	800 °C	45	[85]
TiTaO	film	400 °C	45	[86]
$Sr_5Ta_4O_{15}$	pellet	1300 °C	41	[84]
$Sr_5Nb_4O_{15}$	pellet	1100 °C	40	[84]
$Ce_2Ti_2O_7$	pellet	1200 °C	40	[87]

Table 2. The list of some perovskite based high k dielectric materials reported in the literature.

In addition to these examples, there are even more oxide dielectrics based on perovskite structure explored for dielectric applications. Table 2 shows some more

examples for these type of dielectrics especially those reported with k ≥ 40. Their form during k value measurement and processing temperature information are shown as well. Although they have shown very promising k values either in pellet or thin film form, they require very high processing temperatures as well. The dielectrics used in this thesis were chosen from this table, and indicated with red color. The details about these dielectrics will be introduced in the following parts of this section.

- *Multilayer dielectric stack*

Besides using single dielectric layers, different approaches have been also attempted to optimize MIM properties such as alternative configurations of dielectric materials including stacked, laminated, and sandwiched structures of multilayer dielectrics. The motivation of using different configurations is mainly to combine the material's different good properties to improve the overall electrical characteristic of MIM devices. Indeed, in the literature, several enhancements in performance of MIM capacitors have been reported using these structures. For example, as a critical factor for MIM applications, the capacitance-voltage linearity parameter has been manipulated by stacking dielectrics. S. J. Kim *et al.* showed the use of stacked dielectric layers constituted of HfO_2 and SiO_2 [72]. SiO_2 dielectric with a negative α was used to compensate the oxide (HfO_2) with a positive α. By using a 12 nm HfO_2 /4 nm SiO_2 stack, a very low α value of 14 ppm/V^2 was obtained. However, the low k value of SiO_2 prevented high capacitance values from being reached. In another work done by S. K. Lee et al, $Al_2O_3/HfO_2/Al_2O_3$ sandwiched type of dielectric stack was the focus for MIM application [73]. They observed that as the portion of Al_2O_3 increases the MIM capacitors were found to exhibit strong resistance to hard

dielectric breakdown. Further work confirmed the good electrical properties of combination of ZrO_2 with SiO_2 [74]. The authors showed this combination along with interface engineering and reported a high capacitance density of 8.82 fF/μm^2, an alpha value of 402 ppm/V^2 and a leakage current in the range of 10^{-7} A/cm^2 at 2 V. Also, it was reported that better leakage performance was possible by combining two suitable dielectric materials in the sandwich configured MIM devices. The stack of $ZrO_2/Al_2O_3/ZrO_2$ multilayer dielectric structure was shown to be an improvement in terms of the leakage current compared to single ZrO_2 dielectric MIM capacitor. This behavior was explained by the high band gap value of the additional Al_2O_3 layer [88, 89]. Although the method of using multilayered dielectric systems simply reduces the effective k value, it is still a very promising method in order to achieve the desired properties for future MIM capacitors.

The dielectric materials used in this thesis

As it is mentioned above, no single dielectric material can satisfy all the parameters of future MIM capacitors. Therefore, in this thesis, we focused to the perovskite based dielectrics which can offer the highest k values. $CeAlO_3$ is one of the studied dielectrics in this thesis. Although, it has the highest processing temperature of 1600 °C (Table 2), the reported k value of 3000 for the pellet form of this material is very interesting in terms of future MIM capacitor applications. In addition, $Sr_2Ta_2O_7$ systems were chosen as they have rather lower processing temperatures and still large k values. Also, the limited number of reports about these materials motivated us to further explore them. Moreover, $SrTiO_3$ was used in this thesis owing to its relatively low processing temperature and large enough k value. In

addition to the single dielectrics based on these perovskite based structures, multilayered dielectric configuration was also utilized in order to optimize the MIM parameters. As crystalline structure of a dielectric material is a possible effect for high k value accompanied with poor leakage performance, a thin film $SrTiO_3$ dielectric was combined with $Sr_2Ta_2O_7$ and Al_2O_3 owing to their amorphous structures at the crystallization temperature of $SrTiO_3$. By these stacking methods an improved interface quality is intended in order to have a moderate dielectric constant with sufficiently low leakage current when deposited on a metal electrode. In Fig. 2.9, the dielectrics used in this thesis are shown schematically.

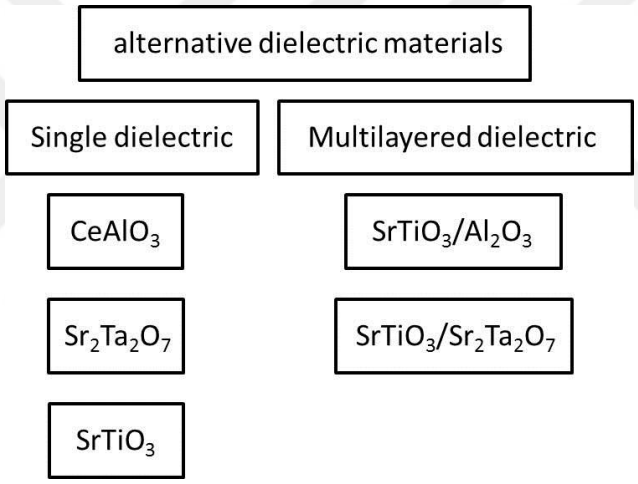

Fig. 2.9 Schematic view of the screened dielectric materials in the thesis.

In the following parts, the general properties of these dielectrics are introduced.

- *$CeAlO_3$*

$CeAlO_3$ is an attractive perovskite-based dielectric candidate for MIM applications due to its high bulk k value of ~3000. $CeAlO_3$ was reported to have tetragonal symmetry by Zachariasen [90], Tanaka [91], and Tas and Akinc [92], but a

rhombohedral symmetry by Roth [93] and Kim et al [94]. The possible origin for the large k value of $CeAlO_3$ has been attributed to its structure of tetragonal centrosymmetric space group I4/mcm at room temperature, which immediately precludes the occurrence of ferroelectricity by Wang et al [95]. On the other hand, in another report, it has been shown that, the unexpectedly large k value of $CeAlO_3$ ceramics maybe explained on the basis of an electrically heterogeneous microstructure containing resistive surface layers (either on the surface of a pellet, individual grains, and/or as a grain boundary phase) and semiconducting grains [96].

Although $CeAlO_3$ has a large bulk k value, this material has been rarely studied for MIM capacitor application so far. This might be due to the fact that, $CeAlO_3$ is difficult to synthesize since Ce valence of +4 is stable in nature [95]. One of the few report about this material, has shown that single crystal $CeAlO_3$ grown by cold crucible technology has a dielectric constant of about 3000 [75]. In another report, the dielectric constant of $CeAlO_3$ was reported to be varied between ~18 at 8 K and ~20 at 300 K [96]. Wang *et al.* reported that $CeAlO_3$ with a tetragonal structure exhibits k > ~600 and tanδ <0.04. They also calculated the optical band gap of this oxide as 3.29 eV and reported it superior than the one of single crystal (2.65 eV) [95]. Yan et al studied Ce-Al-O for use in metal-oxide-semiconductor gate dielectric applications [97]. The amorphous Ce-Al-O film in MOS structures had a dielectric constant of less than 10 and leakage current of 2.74×10^{-3} A cm^{-2}. In another work, a Ce-Al-O system was studied by molecular beam deposition method for investigation of MIM properties [98]. Electrical characterization of Ce-Al-O dielectric film on a TiN electrode was shown, that amorphous $Ce_{0,7}Al_{1,3}O_3$ films reveals a dielectric constant value of about 11 and a leakage current lower than 10^{-4} A/cm^2. Additionally, the

authors observed that there was not any low k interface formation between the Ce-Al-O and the TiN metal electrode.

- *Sr-Ta-O*

Among strontium-bearing oxides, Sr-Ta-O system is one of the most promising mixed oxide dielectric as it shows an improved dielectric constant compared to that of single SrO and Ta_2O_5. Ta_2O_5 has been already used in DRAM application for more than a decade. It exhibits a very good voltage linearity property, but the poor leakage performance and moderately low k value makes it less attractive for MIM application. Therefore, mixing it with SrO exhibits better results.

Different phases of Sr-Ta-O with complex structures have been reported. Instead of a simple perovskite structure, Sr-Ta-O has been demonstrated to contain perovskite building blocks as part of the lattice [99]. Among these systems, $SrTa_2O_6$ and $Sr_2Ta_2O_7$ are the most promising phases due to their k values of 100 [100] and 80 [101], respectively, in their orthorhombic crystal form. It has been also found that the permittivity of $SrTa_2O_6$ grown by MOCVD is not very sensitive to the exact composition of that, and gives flexibility to have composition between Sr/Ta:0.4-0.7. However, at higher Sr content, the k value was observed to be reduced to ~30-40 with the transition to perovskite phase. The amorphous structure of this dielectric exhibited a k value of ~40 and a very low leakage current. No significant change on the k value was observed within the wide range of composition for amorphous structures [79].

In another work, $SrTa_2O_6$ was deposited by plasma enhanced atomic layer deposition [100]. As MIM characteristic on Pt/$SrTa_2O_6$/Pt it was reported that after

annealing at 600 °C, a leakage current of 3 x 10^{-8} A/cm^2 was accompanied with a k value of 40.

Also, in the work about MOCVD-grown Sr-Ta-O, the main electrical measurement results were compared with the other most known dielectrics [81]. As seen in Fig. 2.10, Sr-Ta-O dielectric films in that work had rather lower leakage levels compared to the levels typically reported for thin layers of Ta_2O_5, Al_2O_3, HfO_2, and ZrO_2.

In addition, a chemical preparation of Sr-Ta-O has been performed. The structural characterization on the obtained film showed that a new phase had been identified as a cation-deficient, simple cubic perovskite structure having the formula $Sr_xTa_xO_3$ (x=0.85). The dielectric constant and tan δ values were observed to be 16 and 0.04, respectively [99].

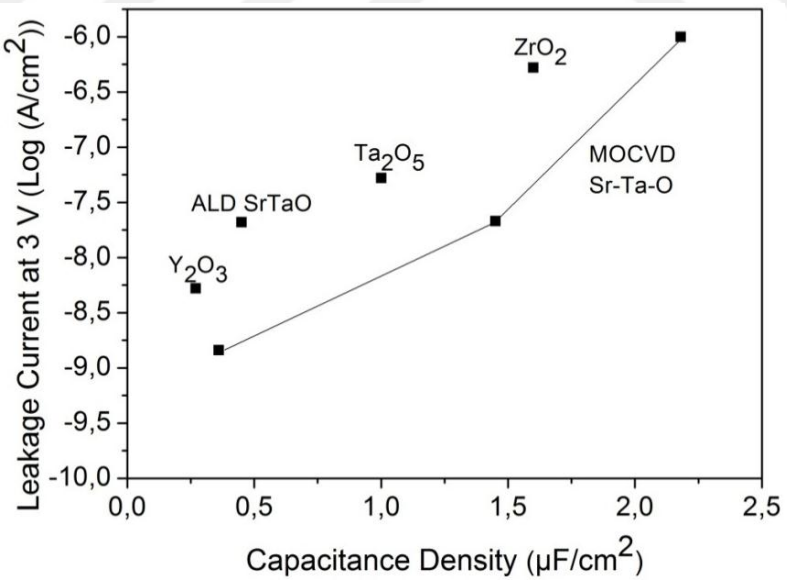

Fig. 2.10 Leakage current density measured at 3V through SrTaO (MOCVD-grown) MIM capacitor, plotted as a function of capacitance density; data from the literature included [81].

- *$SrTiO_3$*

$SrTiO_3$ is one of the most promising candidates with a cubic perovskite type structure and has been widely examined for DRAM, MOS and MIM capacitor applications. At room temperature the cubic unit cell consists of a central Ti^{4+} ion, which is octahedrally coordinated by 6 O^{-2} ions. At the corners of the cube Sr^{2+} ions are situated. The major advantage of strontium titanate ($SrTiO_3$) dielectric is its high k value (reachable to 300). On the other hand, the band gap of $SrTiO_3$ is relatively small (~3.2 eV), and thus the structures with this dielectric often suffer from high leakage currents.

In the literature, many different deposition methods have been reported to grow $SrTiO_3$ films. For instance, M. Popovici *et al.* have studied ALD-grown $SrTiO_3$ in Pt/STO/TiN MIM capacitor structure. The extracted dielectric constant value was 18 for the as-grown film while it was 181 when it is crystalline after RTA at 600 °C. However the leakage was observed as 10^{-4} A/cm^2 for crystalline $SrTiO_3$. F. M. Pontes et al reported a spin coating method for $SrTiO_3$ [102]. For a 600 nm thick dielectric, a k value of 475 and dissipation factor of 0.050 had been reported. This was higher than the value for $SrTiO_3$ sintered ceramic (~300) [103]. On the other hand, Hofman et al, have shown that using a sol gel process, 600 nm thickness of $SrTiO_3$ exhibits dielectric constant and dissipation factor values of up to 200 and 0.04, respectively [104]. In another report, $SrTiO_3$ deposition has been done by PVD technique. Very high capacitance density of 44 fF/μm^2 and a small alpha value of 54 ppm/V^2 at 2 GHz were simultaneously achieved using a TaN/$SrTiO_3$/TaN MIM configuration [78].

In another report $SrTiO_3/ZrO_2$ bilayer was studied. By combining the two high k materials with opposite quadratic voltage coefficient of capacitance, a high performance MIM capacitor was obtained. They reported α and capacitance density as -60 ppm/V^2 and 11.5 fF/μm^2, respectively, while the leakage current was 3.5 x 10^{-8} A/cm^2 at 2 V [105]. In [106], the capacitance voltage linearity of MIM structures was enhanced using $SrTiO_3/Y_2O_3$ dielectric stack. The authors observed that an increase in the Y_2O_3 thickness in the stack leads to an improvement in the voltage linearity, while maintaining an overall capacitance density greater than 10 fF/μm^2. Additionally, $SrTiO_3/Al_2O_3/SrTiO_3$ laminate structure was proposed as a dielectric stack. The corresponding authors mentioned a very promising result for capacitance density as 19.13 fF/μm^2, alpha of 610 ppm/V^2, and a low leakage current of 5 x 10^{-9} A/cm^2 [107].

3 Experimental Methods

3.1 Deposition Methods of Dielectric and Electrode Materials

In this thesis, atomic vapor deposition (AVD) and atomic layer deposition (ALD) techniques are used for deposition of the dielectric materials, while sputtering-physical vapor deposition (PVD) technique is utilized for deposition of the electrode materials (TaN and TiN). For the completion of MIM stacks, top metal Au dot electrodes are deposited on dielectric materials by resistive thermal evaporation technique. In the following paragraphs of this chapter, brief information about basics of the used deposition techniques is given.

Atomic Vapor Deposition

Atomic Vapor deposition (AVD) is also known as a pulsed injection MOCVD (metal organic chemical vapor deposition) method combining basic operation of conventional MOCVD and ALD processes. The technique is based on sequential injection of micro-liters amounts of solution of metal organic chemical precursor into an evaporator through a high speed micro-electro valve. The injection rate is controlled simply by two parameters of frequency and valve aperture time [108].

The advantages of this technique over the classical CVD method are that the thickness of the layer, coating stoichiometry and the growth rate can be controlled precisely (digital growth) due to easy control of precursor flux. In contrast to conventional MOCVD and ALD, heated bubblers for precursors are not used in this technique. Therefore, deterioration of precursors and a change in deposition quality

over time is prevented. Precursors are stored at room temperature right until injection into the vaporizer, thus, the requirements on the precursor in terms of volatility and stability are not as critical.

Atomic Layer Deposition

Atomic layer deposition (ALD) is a chemical gas phase thin film deposition method. In this technique, the film is grown through sequential saturative surface reactions that are realized by pulsing the two (or more) precursors into the reactor alternately, one at a time, separated by purging or evacuation steps.

Owing to the saturative reactions, the film growth is self-limiting in this technique. This gives the method a number of advantages such as, accurate and simple thickness control, large area capability, excellent conformality, and capability to produce sharp interfaces [109]. It is also straightforward to tailor film composition at an atomic layer level. The method is well suited for the preparation of multicomponent and multilayer materials due to the fact that process temperature windows are often reasonably wide so that binary processes are easy to combine. The major drawback of ALD is the low deposition rate which is a direct consequence of the stepwise film growth where in most processes only a fraction of a monolayer is deposited in one cycle. Deposition rates are typically in the range of 100-300 nm/hour.

Physical Vapor Deposition

There are several types of physical vapor deposition techniques namely, reactive sputtering, evaporation, metal sputtering deposition and oxidation, and pulsed laser deposition. Sputtering mechanism of PVD technique is the most widely

used method for depositing various metallic films. It involves such a mechanism that atoms or molecules are ejected from a target material by high-energy particle bombardment so that the ejected atoms or molecules can condense on a substrate as a thin film. For the evaporation type of the technique, the source material is evaporated in a vacuum. The vacuum allows vapor particles to travel directly to the target object (substrate), where they condense back to a solid state.

3.2 Physical Characterization Techniques

In this section, a short overview about the structural characterization techniques used for dielectric and electrode materials of MIM capacitors is presented.

3.2.1 X-Ray Diffractometry

Microstructure of the dielectric materials and the metal electrodes of the MIM capacitors were characterized by means of X-Ray Diffractometry (XRD).

In this technique, a monochromatic X-Ray beam is directed toward the sample at an angle of θ as illustrated in Fig. 3.1. The interaction of the incoming X-ray beam with the sample produces constructive interference only if conditions satisfy Bragg's Law shown in Equation 3.1;

$$n\lambda = 2dsin\theta \qquad \text{Equation 3.1}$$

where, n is an integer, λ is the wavelength of electromagnetic radiation, d is the lattice spacing in crystalline samples and θ is the diffraction angle.

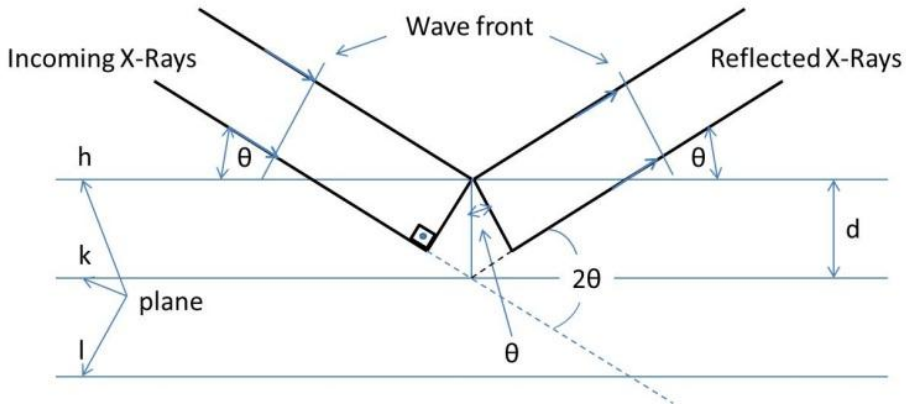

Fig. 3.1 Diagram of Bragg's Law.

As X-Ray beams have wavelengths in the order of angstroms, in the range of typical inter-atomic distances in crystalline solids, X-Ray beams can be diffracted from the repeating patterns of atoms that are characteristic of crystalline materials. The diffracted X-rays are then detected, processed and counted. By scanning the sample through a range of 2θ angles, all possible diffraction directions of the lattice should be attained.

In this work, XRD measurements were obtained with an RIGAKU DMAX 1500 diffractometer using a Cu Kα monochromatic radiation (λ=0.154 nm) source. The experimental data was collected in the angular range of 2θ = 20–60° with an increment of 0.04° and a counting time of 1 s per data point.

3.2.2 X-Ray Photoelectron Spectroscopy

The X-Ray photoelectron spectroscopy (XPS) method was used to determine the surface composition of elements in the dielectric materials and to receive information about the oxidation state of surface and sub-surface atoms on the dielectric and the electrode materials.

The sample is positioned in an ultra-high vacuum chamber and irradiated with an X-Ray photon beam. The interaction of an X-Ray photon with a sample leads to the ejection of photoelectrons, as shown schematically in Fig. 3.2. As illustrated in the diagram, the X-Ray photon interacts with an electron in the K shell, causing the emission of a 1s photoelectron and the resulting K shell vacancy is filled by an electron from a higher level which can lead to either X-Ray fluorescence, or the radiationless de-excitation process of Auger emissions. The determination of the kinetic energy of the photoelectron is the basis of experimental XPS. The kinetic energy of the photoelectron is given by Equation 3.2;

$$E_K = h\nu - E_B - \varphi \qquad \text{Equation 3.2}$$

where $h\nu$ is the photon energy of the X-Ray source, E_B is the binding energy of the atomic orbital from which the electron originates, φ is the spectrometer work function (the work function is the lowest energy an electron must overcome in order to escape from the surface and be detected). Since each element has a unique set of binding energies, XPS is used to identify and determine the concentration of the elements at the surface.

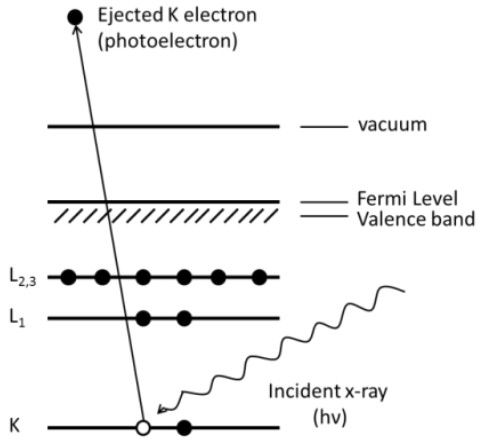

Fig. 3.2 Schematic view of the photoemission process [110].

In this thesis, all XPS measurements were acquired using a Physical Electronics (PHI) Model 5600 XPS system. The system uses an Al Kα source (hv=1486.8 eV) and is equipped with a mono-chromator. Ejected photoelectrons were detected by a hemispherical analyzer that provided high sensitivity and resolution. All high resolution spectra were collected with pass energy of 29.35 eV while surface spectra were obtained with pass energy of 59 eV. The step size and time/step were chosen to be 0.025 eV and 100 ms, respectively. The charge correction on the samples was done by setting C1s line to 284.6 eV. The data acquired from the instrument was processed using Multipak software provided by the instrument manufacturer. Surface elemental compositions were calculated from subtracting the background peak areas by Shirley method. Sensitivity factors used to calculate the relative atomic percentages were provided by the manufacturer. The database of sensitivity factor is based upon empirical peak area values relative to F1s line corrected for the system's transmission function. The ion sputter profiling was performed on the area of 3 x 3 mm^2 of sample with a 1 keV Ar^+ ion beam.

3.2.3 Time of Flight Secondary Ion Mass Spectroscopy

Time of flight mass spectroscopy (ToF-SIMS) method was used to investigate depth profile of the MIM stacks and any diffusion phenomena of ions between the layers of the MIM structure, particularly after the post-deposition annealing processes.

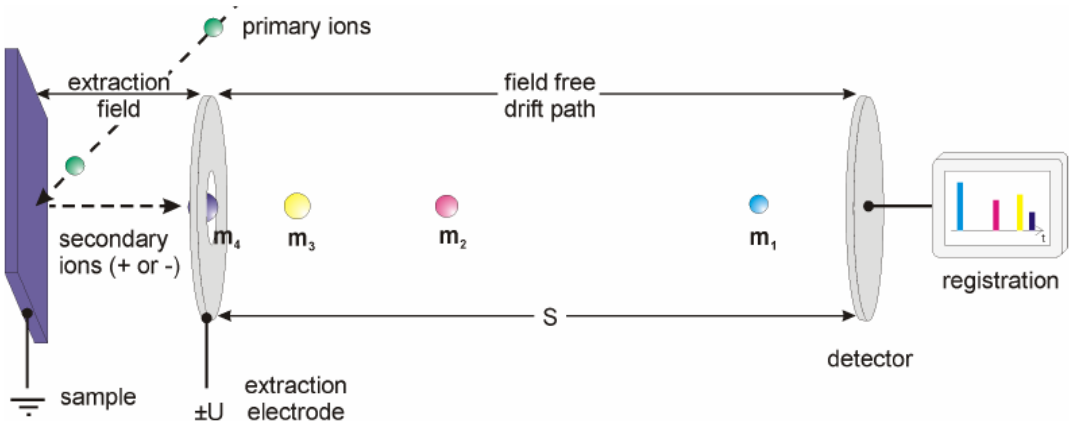

Fig. 3.3 Schematic view of the Tof-SIMS process [111].

The Tof-SIMS technique is based on the sputtering of the sample. A pulsed primary ion beam, such as Ga^+ or Bi^+ with a high energy of 25 keV, bombard the sample to remove and ionize species from the surface of the sample by transferring the energy of the incident ion beam to the atoms. The resulting secondary ions include monoatomic and polyatomic particles of the samples. Secondary ions then fly toward the mass spectrometer with the same kinetic energy due to a given potential for acceleration resulting in ions of different mass to charge (m/q) ratio to have different velocities as shown in Fig. 3.3. Ions with lower mass have higher flight velocity than those with higher mass. Thus they will reach the secondary-ion detector earlier. As a result, the mass separation is obtained in the flight time from the sample surface to the detector. The flight time (t_f) of various ions is measured and related to the m/q ratio as shown in Equation 3.3;

$$\frac{m}{q} = \frac{2Vt_f{}^2}{L^2} \qquad \text{Equation 3.3}$$

where L is the flight distance from the sample to the detector, and V is the potential drop [112]. Since the m/q is solely a function of the t_f, fragments with different mass can be identified.

Secondary ions are registered either by digitizing their current transient at the detector output (low mass resolution) or by registration of their arrival times at the detector (high mass resolution).

In this work, the measurements were acquired using a ToF-SIMS 5 spectrometer (IONTOF GmbH, Münster, Germany). It was equipped with a 25 keV bismuth ion analysis source (Bi^+) and a 0.2-2.0 keV Cs^+/O_2^+ sputtering source. The sputtering ion beam of Cs^+ ion with 0.5 keV energy was rastered over a 300 x 300 μm^2 area under an incident angle of 45 degree. The pulsed analysis beam of Bi^+ ion was rastered over a 100 x 100 μm^2 area at the center of sputter craters during data acquisition. Negative ions were detected as Cs is a strong electron donor.

3.2.4 Transmission Electron Microscopy

In order to image the morphology, thicknesses and interfaces of the MIM layers, transmission electron microscopy (TEM) technique was applied.

In this technique, a well-focused high energy (few hundred keV) electron beam travels through a very thin sample. As the electrons are transmitted through a sample, many interactions between them and the specimen occur. Depending on the density of the sample, some of the electrons are scattered and disappear from the beam. At the bottom of the microscope the unscattered electrons hit a fluorescent screen, which gives rise to a "shadow image" of the specimen with its different parts

displayed in varied darkness according to their density. The image can be photographed with a camera.

The technique is similar to the light microscope, but its imaging capability is at much higher resolution, due to the very small wavelength of the electrons with high energy. Therefore, it is possible to image even a single column of atoms.

In this thesis, a Philips CM 200 was operated with electron beam energy of 200 keV. The cross-sections of the samples were prepared by mechanical polishing. The final thinning was performed by Ar^+ ion polishing with 2 keV for 20 minutes.

3.2.5 Scanning Electron Microscopy

Cross-sectional images of deposited MIM stacks were also obtained by Scanning Electron Microscopy (SEM) owing to its easy sample preparation method. By this technique, conformity, surface morphology and thickness of the layers of MIM structures were investigated.

In this technique, an electron beam is focused on a spot volume of the specimen, resulting in the transfer of energy to the spot. These bombarding electrons emit electrons from the specimen. The emitted electrons, also known as secondary electrons, are attracted and collected by a positively biased grid or detector, and then translated into a signal.

Secondary electron images can be obtained on materials for identifying surface features. For most of the instruments, the practical limit is of ~5 nm. Despite the significant depth of penetration of the incident electron beam (e.g. 0.5-5 μm), the

emitted electrons come from mean depths of 50 nm-0.5 μm depending on the density of the material. Hence the technique is sensitive to the near-surface region.

In this thesis, A Hitachi S 4500 SEM was used. Surface topography differences between the layers of MIM capacitor stacks are imaged by secondary electrons released from the surface.

3.3 Electrical Characterization Techniques

3.3.1 Capacitance-Voltage Measurements

As the most important property of MIM capacitors, capacitances versus voltage (C-V) measurements were performed. By sweeping the bias voltage, capacitance density is measured, thus extraction of the k value and alpha coefficient is possible.

In this thesis, C–V measurements were performed in serial mode by using two top Au dot electrodes with an Agilent 4294A precision impedance analyzer. Therefore, the measured equivalent capacitance was multiplied by 2 for determining one of the capacitance connected in series. The simplified setup is illustrated in Fig. 3.4 schematically. The measurements were performed at a frequency of 100 kHz with AC-amplitude of 0.1 V. The bias voltage was varied between -3 and 3 V.

The extraction of k values was done by the simple capacitance equation (Equation. 2.1) using the capacitance density value measured at bias voltage of 0 V, and thickness of the dielectric obtained by TEM image.

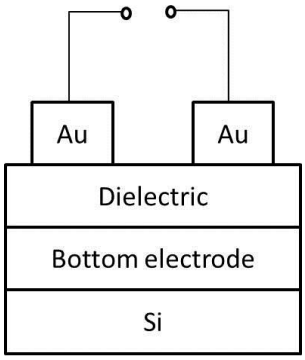

Fig. 3.4 Schematic view of the setup for the C-V measurement.

3.3.2 Current-Voltage Measurements

In order to measure leakage current density through MIM layer, current versus voltage (J-V) measurements were performed. The setup used for this measurement is seen schematically in Fig. 3.5.

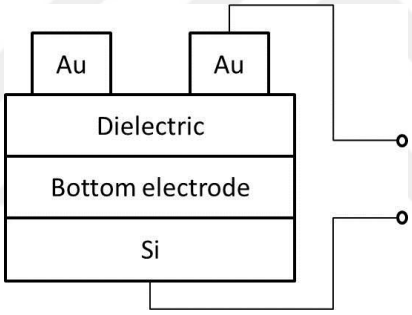

Fig. 3.5 Schematic view of the setup for the J-V measurement.

In this thesis, the measurements were performed by a HP 4140 ampermeter, which has a direct current (DC) current resolution in picoampere (pA) range. The DC leakage current was measured by sweeping the applied voltage typically from – 3 to 3 V at room temperature.

4 Results and Discussions

In this thesis, the work is mainly categorized into two parts according to the configuration of dielectric layers in alternative MIM capacitor structures namely, single layer dielectric and multilayer dielectric MIM capacitors as already shown schematically in Fig. 2.9. The corresponding results are presented in the following parts of this chapter.

4.1 MIM Capacitors with Single Layer Dielectric

For the single dielectric MIM capacitor structure, three different alternative high k dielectrics were investigated namely, Ce-Al-O, Sr-Ta-O and $SrTiO_3$. As $SrTiO_3$ was also studied with multilayered dielectric configurations, the single dielectric $SrTiO_3$ MIM capacitor findings are included to the multilayered dielectric part (Chapter 4.2) in order to see the effect clearly. Therefore, in this part, the structural and electrical properties of Ce-Al-O, and Sr-Ta-O dielectric materials in MIM capacitors are discussed, sequentially.

4.1.1 MIM Capacitors with Ce-Al-O

As mentioned in section 2.3, $CeAlO_3$ is a promising dielectric material for MIM capacitor due to its high bulk k value. However, there are not many studies in the literature concerning its usage for MIM capacitor application. In this chapter, MOCVD deposited thin film Ce-Al-O is investigated as a part of the single dielectric configuration for the MIM capacitors. Several precursor injection ratios are used in order to vary the stoichiometry in the dielectric film. The as-deposited dielectric films in MIM capacitors are compared in terms of their k values and leakage current

densities. Their microstructure analyses are also performed. In addition, the effect of post-deposition annealing process on deposited dielectric films, on electrode layers and on MIM properties are presented. Lastly, the conclusions about the whole treatment on single Ce-Al-O based MIM capacitor will be discussed.

4.1.1.1 Experimental Details

Depositions of dielectric film were carried out on Si (100) substrate, covered with 70 nm TiN bottom electrode grown by PVD technique.

Dielectric Ce-Al-O thin films with a thickness of 30-40 nm were deposited at 400 °C by pulsed injection MOCVD technique. Ce-Al-O depositions were carried out using mixtures of Ce and Al precursors in separate solutions: 0.05 M $Ce(^{i}PrCp)_3$ and 0.05 M $Al(NEt_2)_3$. Main solvent for precursors was dry toluene. Precursors were delivered into the vaporizer by a simultaneous injection of solutions using two separate electromagnetic injectors. Ar was used as a carrier gas for vapor transportation to the hot substrate where vapor decomposes and the growth of the layer occurs. O_2 was added as an oxidant. The process pressure was kept at 1 mbar.

In order to complete the MIM structures, deposition of Au top electrode with a thickness of ~150 nm and area of $3x10^{-3}$ cm^2 was done on Ce-Al-O layers using a shadow mask at room temperature. The schematic diagram of the prepared MIM structures is shown in Fig. 4.1.

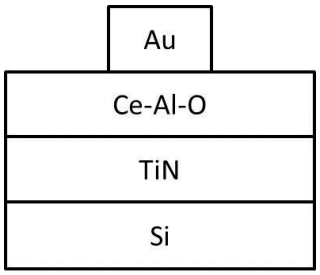

Fig. 4.1 Schematic view of the investigated Ce-Al-O MIM capacitor stack.

For the investigation of the effect of annealing temperature on the dielectric and on the bottom electrode stack, just before the Au top electrode deposition, the annealing process was performed at 600 °C and 850 °C in N_2 ambient for 1 min using the RTA equipment. After the annealing process, the top electrode deposition was performed for electrical measurements.

4.1.1.2 Characteristics of As-Deposited MIM Capacitors

In order to vary the composition of Ce-Al-O films, several injection ratios of Ce to Al precursors (Ce:Al) have been used such as Ce:Al=1:1.7; 1:1.4; 1:1; 1.7:1; 2.5:1. The corresponding dielectric constants of the films were extracted from C-V measurements. In Fig. 4.2, the plot shows the dielectric constant dependence of Ce-Al-O films as a function of injected Ce to Al precursor ratio.

As evidenced from Fig. 4.2, a dielectric constant of 20 is obtained if more Al is injected into the samples (Ce:Al=1:1.7). Although this k value is higher by roughly a factor of two than the one reported for MBD-grown Ce-Al-O [98], it is still very far from the values for $CeAlO_3$ crystals [75]. It is seen that as the injected precursor ratio of Ce to Al increases, k value further decreases to the value of 8.

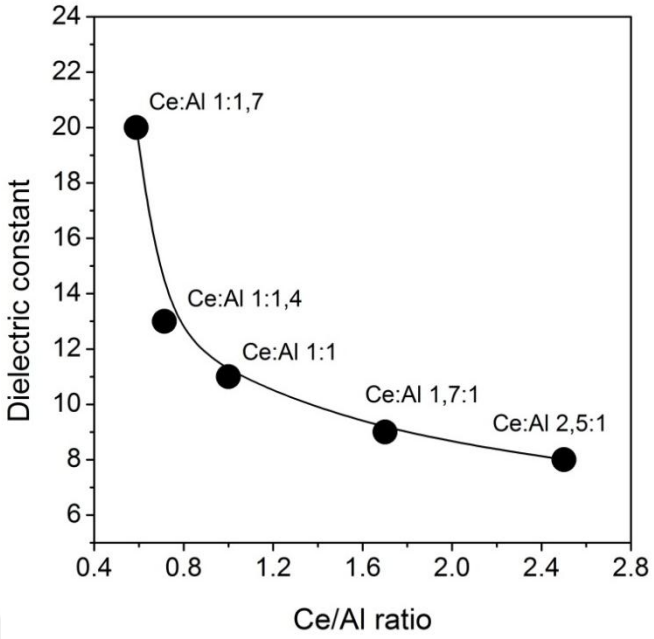

Fig. 4.2 Dielectric constants of as-deposited Ce-Al-O MIM capacitors as a function of injected Ce:Al precursors ratio.

The leakage current density measurements on Ce-Al-O films grown with different injection ratio of Ce to Al precursors have been performed and the results are shown in Fig. 4.3.

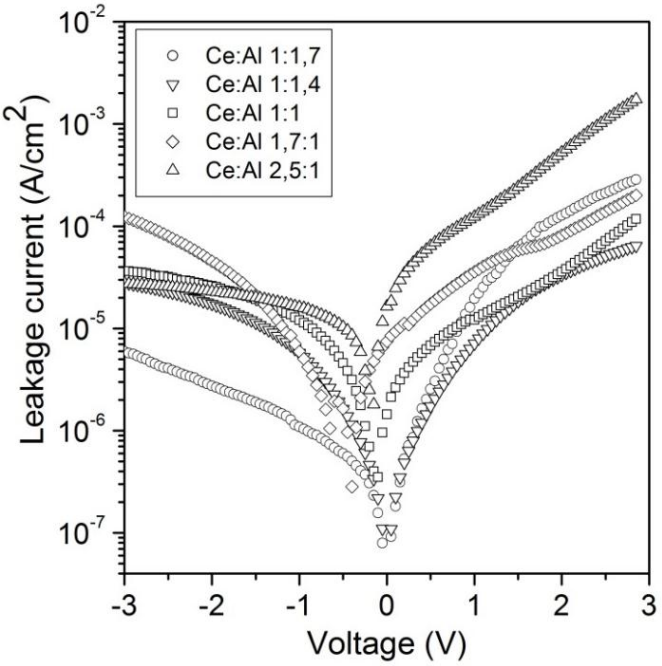

Fig. 4.3 Leakage current densities of Ce-Al-O based MIM capacitors prepared with different Ce:Al precursors injection ratios.

As seen from the figure, leakage current values of ~10^{-5} A/cm^2 can be obtained at -2 V. In addition, the leakage current density values are observed to be slightly dependent on Al content in the oxide films. The samples with more Al content tend to have around one order of magnitude lower leakage current densities. This effect might be attributed to difference of the band gaps of Al_2O_3 (8.7 eV) [11] and CeO_2 (3.2 eV) [113].

On the other hand, for the positive bias voltage, the effect of injection ratio on leakage current densities seems not simple, as the leakage current at positive biases are leaded by the interface between the dielectric and the bottom metal electrode. The reason for this kind of observation may be the different interface statuses induced by different composition of dielectric material.

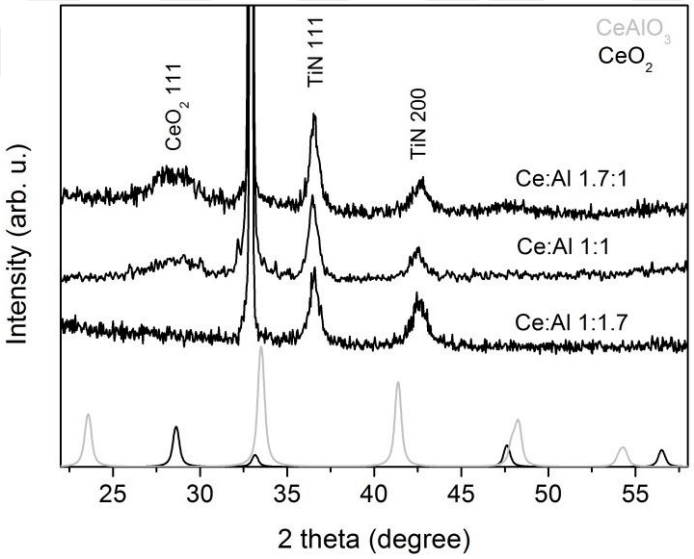

Fig. 4.4 XRD patterns of Ce-Al-O thin films grown with different injected Ce:Al ratios. (On the bottom of the figure, the gray line corresponds to the reference data of $CeAlO_3$, while the black line is for CeO_2 reference).

In order to investigate the microstructure of the films deposited with different stoichiometry, XRD measurements were performed. Fig. 4.4 shows XRD patterns for the films representing high, low, and equal cases of the ratio of Ce to Al precursor.

Also, $CeAlO_3$ and CeO_2 powder diffraction data are plotted at the bottom of the figure as a reference. It is seen that the dielectric film is amorphous if it is Al rich (Ce:Al=1:1.7) as there is no observation of corresponding diffraction peaks. Only, crystalline structure of Si as substrate and TiN as bottom metal electrode has been obtained for this composition. On the other hand, crystallization in dielectric film have been observed for the Ce rich case (Ce:Al=1.7:1). However, it confirms a phase separation of CeO_2 instead of $CeAlO_3$ formation as the corresponding diffraction peak of CeO_2 (111) appear at around 2θ of 29°. The other observed diffraction peaks are related to the cubic orientation of PVD-grown TiN and to the Si substrate.

4.1.1.3 Characteristics of Annealed MIM Capacitors

In order to investigate if post-deposition annealing at high temperatures enhances $CeAlO_3$ crystallization in the dielectric film, thus, giving a high k value, two different annealing temperatures, namely, 600 °C and 850 °C were applied to the samples in which the dielectric layers were deposited with different precursor injection ratio. Since the results of the annealing are similar for all the films (except the injection ratio of Ce:Al=1:1), only one of the used injection ratios of Ce to Al precursor's (Ce:Al=1:1.4) characterization results are presented here in detail for the investigation of annealing effect.

In order to understand the annealing effect on microstructure of the films XRD measurements were performed. In Fig. 4.5, XRD measurement results of annealed samples grown with Ce:Al ratio of 1:1.4 are shown. The XRD patterns include those annealed at 600 °C and 850 °C together with the as-deposited stack for better comparison. The simulated spectra of powder CeO_2 and $CeAlO_3$ diffraction patterns

have been also shown on the bottom of the figure as a reference. According to the measurements, it is revealed that the annealing of the samples does not lead the dielectric to form crystalline structure of $CeAlO_3$ for both of the annealing temperatures. The dielectric film remains in its amorphous state until 850 °C. At 850 °C, a small peak observed at around 28° might be due to the CeO_2 crystallization. On the other hand, when the annealing is applied at 600 °C, the peaks related to the crystalline TiN disappear and new diffraction peaks are observed. The new peaks are consistent with the rutile phase of TiO_2 [57].

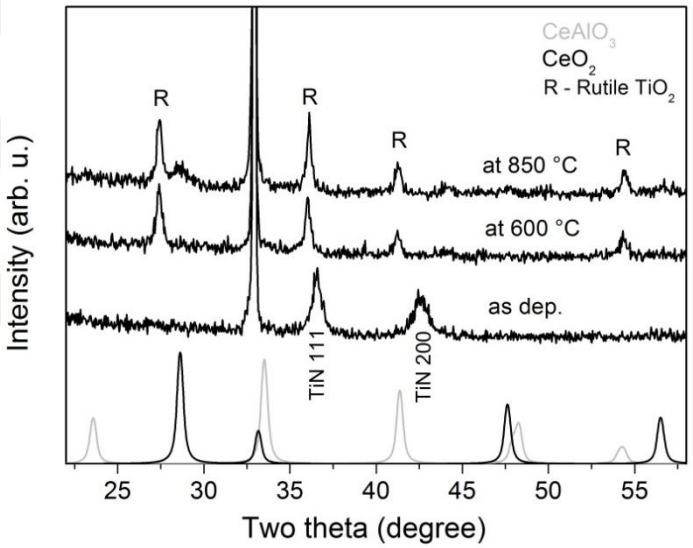

Fig. 4.5 XRD patterns of Ce-Al-O films grown with the injected Ce:Al ratio of 1:1.4, for as-deposited and annealed status. (On the bottom of the figure, the gray line corresponds to the reference data of $CeAlO_3$, while the black line is for CeO_2 and R refers to rutile phase of TiO_2)

As a complementary technique, XPS has been used in order to provide information about the chemical states of constituent atoms on the surfaces of the samples. Fig. 4.6 shows the XPS spectra of Ce3d transition for the samples grown with Ce:Al ratio of 1:1.4 and treated at different annealing temperatures. As seen from the figures, the measured Ce3d spectra (shown with black lines) vary as a function of the annealing temperature.

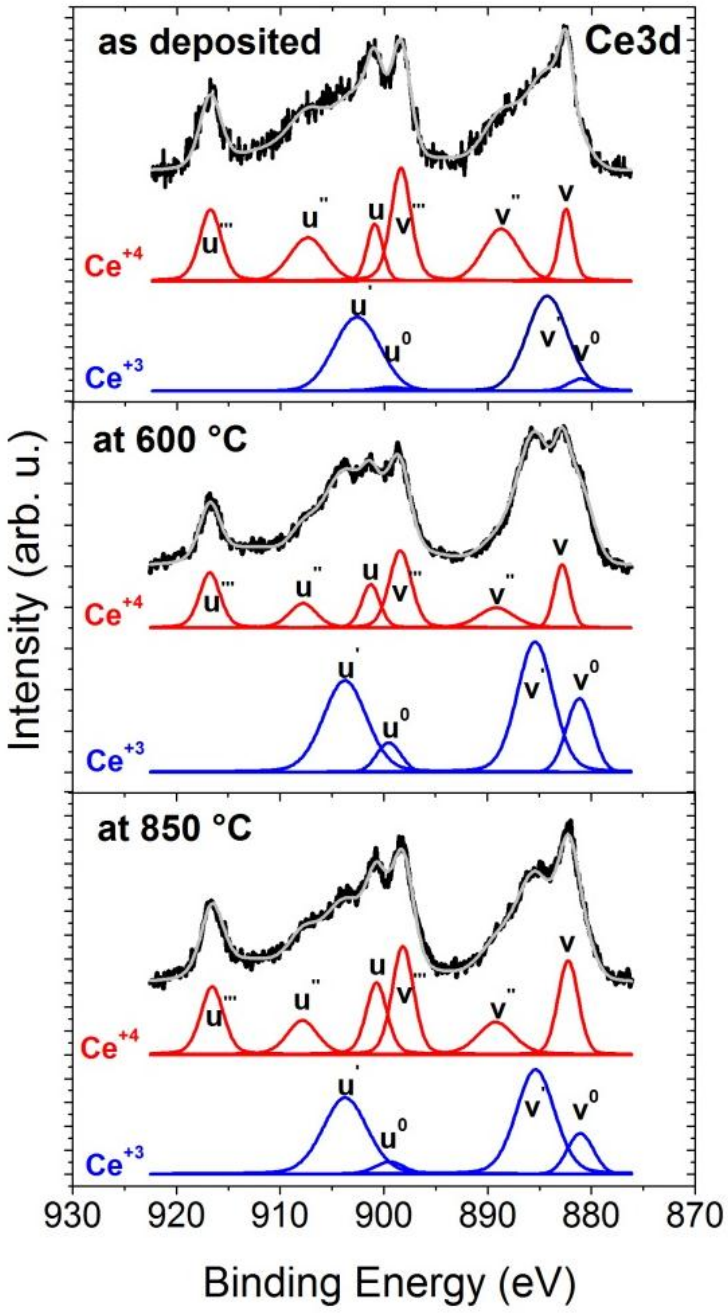

Fig. 4.6 XPS spectra of Ce3d on the dielectric films: as-deposited, annealed at 600 °C and 850 °C. (The black lines indicate the measured Ce3d spectra and the gray lines correspond to sum of the fitted curves. Each Ce3d spectra were fitted for Ce^{+3} (blue lines) and Ce^{+4} (red lines)).

According to the Ce3d spectra, the dielectric films seem to include Ce^{+4} on the surfaces due to the distinct feature at around 917.1 eV which is characteristic of this oxidation state and it has no interference with Ce^{+3} [114]. The existence of this distinctive peak has been ascribed to CeO_2. In order to see the tendency of formation of Ce^{+4} (assigned as CeO_2) and Ce^{+3} (assigned as mixture oxide) on the samples induced by annealing, curve fittings have been applied to the XPS spectra. The assignments of the structures in Ce3d spectra are seen with the same nomenclature used by Burrough *et al.* [115]. The Ce^{+4} state has been fitted with 6 specific peaks (shown with red lines) in agreement with the data reported in the literature [116]. The corresponding six peaks for the as-deposited samples are found at about 917.1(u'''), 908.1(u''), 901.4 (u), 898.7(v'''), 889.3(v''), and 883.1(v) eV. The remaining 4 main peaks (u´, u^0, v´, v^0) are attributed to Ce^{+3} in mixed oxide and shown with blue lines. Also, small shake up satellite structures are detected and associated with Ce^{+3} [117].

Fig. 4.7 a) and b) show O1s and Ti2p XPS spectra for the Ce-Al-O film (grown with 1:1.4) treated at different annealing temperatures, respectively. The O1s spectra (Fig. 4.7 a)) obtained on as deposited sample has been fitted using 4 peaks which are attributed to surface contamination, Al_2O_3, $CeAlO_3$ and CeO_2.

By annealing process at 600 °C and 850 °C, the surface contamination has been observed to be vanished. However, for these annealed samples, there had to be a new peak (shown with green line) located between $CeAlO_3$ and CeO_2 and this peak has been attributed to TiO_2 on the surface of the sample. The obtained Ti2p spectra (Fig. 4.7 b)) from the samples confirm TiO_2 [118] on the surface of the annealed samples.

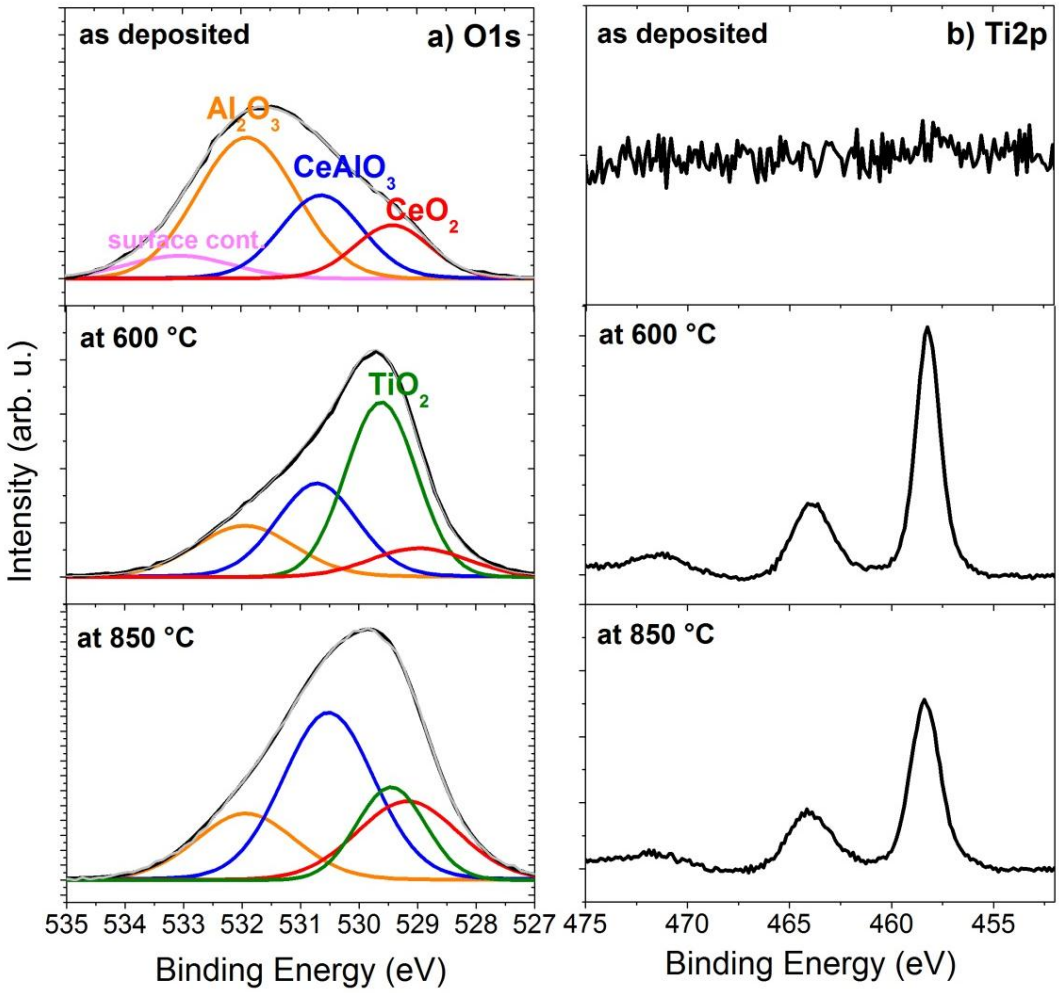

Fig. 4.7 The high resolution XPS spectra on the dielectric films: as-deposited, annealed at 600 °C and 850 °C , a) O1s, b) Ti2p transition region.

For further investigation of the formation of Ce^{+4} on the samples semi-quantitatively, Fig. 4.8 is plotted by taking the sum of the individual spectral weights of cerium states on the fitted spectra of Ce3d and O1s [119]. The relative percentages of Ce^{+4} % in the total Ce3d spectrum and in the total O1s spectrum are seen in the figure. It has been shown the same tendency for the Ce^{+4} percentage on the surface of the samples by these two fitting methods. It is revealed that the as-deposited Ce-Al-O dielectric film on TiN electrodes is non-stoichiometric on the surface. Annealing at 600 °C increases the contribution from Ce^{+3} (mixed oxide)

slightly, but annealing at 850 °C gives rise to CeO_2 formation (increase in Ce^{+4} %) again.

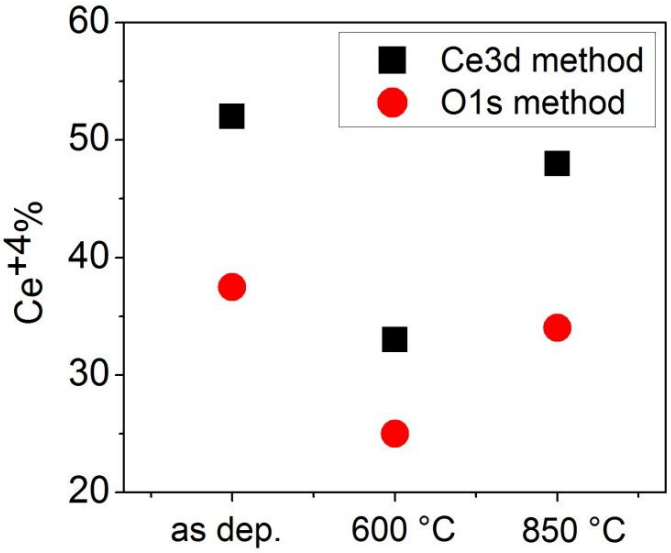

Fig. 4.8 Relative percentages of Ce^{+4} to the total Ce3d spectra obtained on as-deposited, and annealed $Ce_xAl_yO_z$/TiN/Si stacks by two different fitting methods.

ToF-SIMS measurements were performed in order to investigate inter-diffusion of the atoms by the annealing process. Fig. 4.9 shows depth profiles of ^{30}Si, Al, ^{18}O, TiN fragments before and after the annealing process on Ce-Al-O/TiN/Si stacks. TiN profile indicates that the diffusion into the dielectric layer takes place if the annealing process is applied. The diffusion seems to be reached up to the top-surface of the samples annealed at 600 °C and 850 °C as also obtained by XPS. However, XPS analysis (not shown here) on top of the surface of the annealed samples did not reveal the existence of N1s. Since both XRD and XPS results proved the existence of TiO_2 on the annealed samples, the observation of TiN signal on top of the surface by ToF-SIMS measurement has been attributed to the superposition of TiN with ^{46}TiO in this technique.

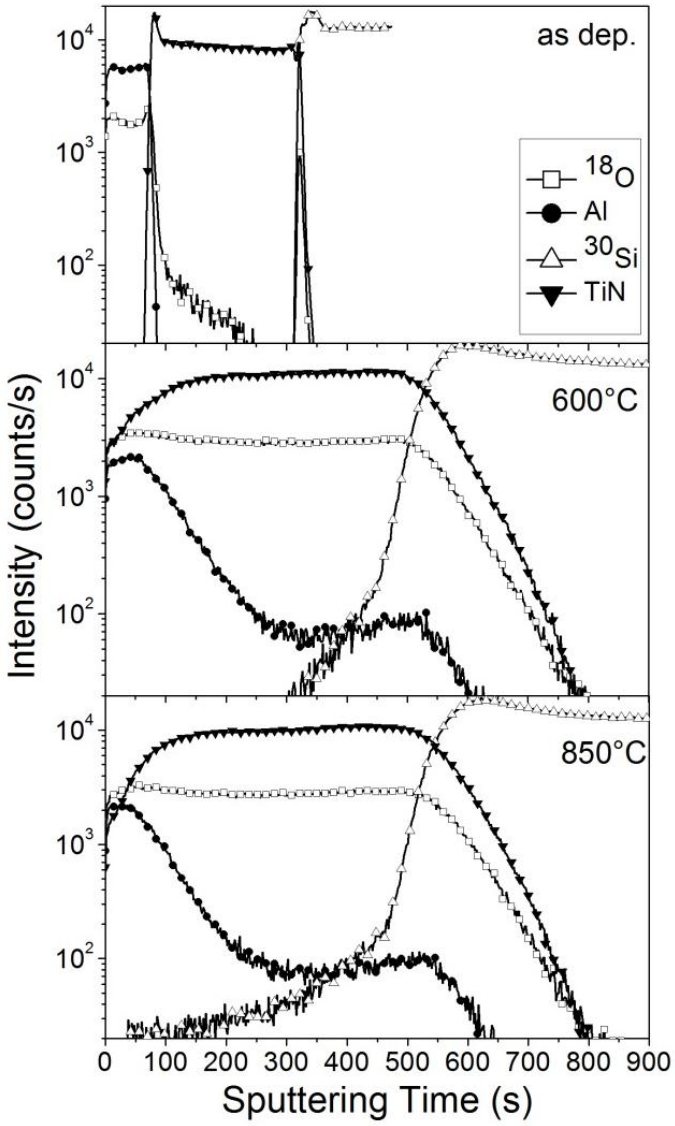

Fig. 4.9 ToF-SIMS depth profiles of Ce-Al-O/TiN/Si stacks:as-deposited, annealed at 600 °C and 850 °C.

The ^{18}O profiles obviously show that the TiN electrodes are oxidized by annealing at 600 °C. As the reaction in dielectric is $CeO_2+Al_2O_3=CeAlO_3+1/2O_2$, the reason of oxidation of metal electrode can be attributed to the oxygen which is generated by the reaction. Al is also observed slightly diffused out through metal electrode. On the other hand, it has been shown that even small amount of oxygen impurity in nitrogen annealing atmosphere can cause oxidation of TiN [120]. Therefore, the source of the ^{18}O signal increase in the annealed samples might be

due to a possible oxygen contamination in N_2 annealing atmosphere. It is known that titanium oxides are thermodynamically more favorable than TiN [121].

In summary, the annealing process on the samples with different Ce:Al precursor ratios did not reveal the formation of $CeAlO_3$ crystal and caused degradation of the bottom electrode. Therefore the electrical measurement using these samples was not considered.

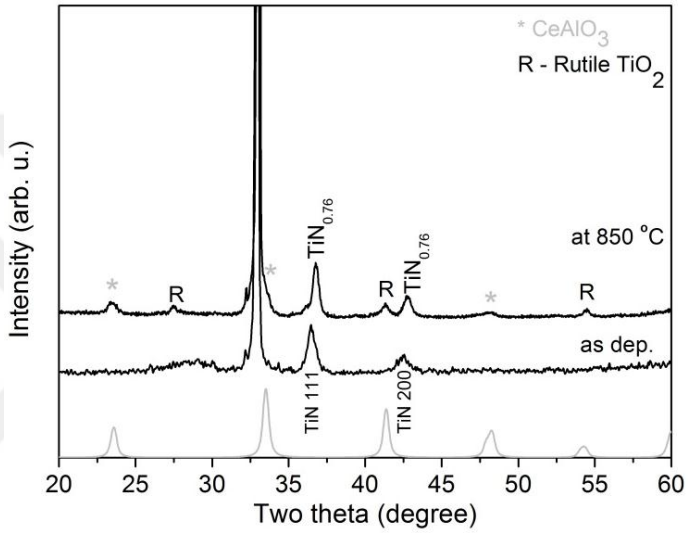

Fig. 4.10 XRD patterns of as-deposited and annealed Ce-Al-O films. (on the bottom of the figure, $CeAlO_3$ reference data is seen with gray line, while R refers to rutile phase of TiO_2)

On the other hand, for the injected precursor ratio of 1:1, formation of crystalline $CeAlO_3$ films is achieved after the annealing process at 850 °C. The corresponding XRD patterns of this sample and as-deposited sample are shown in Fig. 4.10.

In this case, the diffraction peaks of crystalline $CeAlO_3$ are visible after annealing at 850 °C, but the rutile phase of TiO_2 is also obtained. Nevertheless, the intensities of the diffraction peaks are significantly lower compared to the case of

Ce:Al=1:1.4. This can be related to the fact that the TiN bottom electrode is only partially destroyed by the annealing and the reflections of TiN in the XRD plot have not completely vanished, but shifted to the higher two theta values. The signals at 36.8 and 42.7 are attributed to the nitrogen deficient $TiN_{0.76}$ structures. The XRD results are correlated with the SEM analysis of the samples shown in Fig. 4.11 a) and b) for the annealed (at 850 °C) samples grown with Ce to Al precursor ratio of 1:1.4 and 1:1, respectively. The cross-sectional SEM images of the samples imply the damage done to the TiN electrode as well as to the $CeAlO_3$ layer.

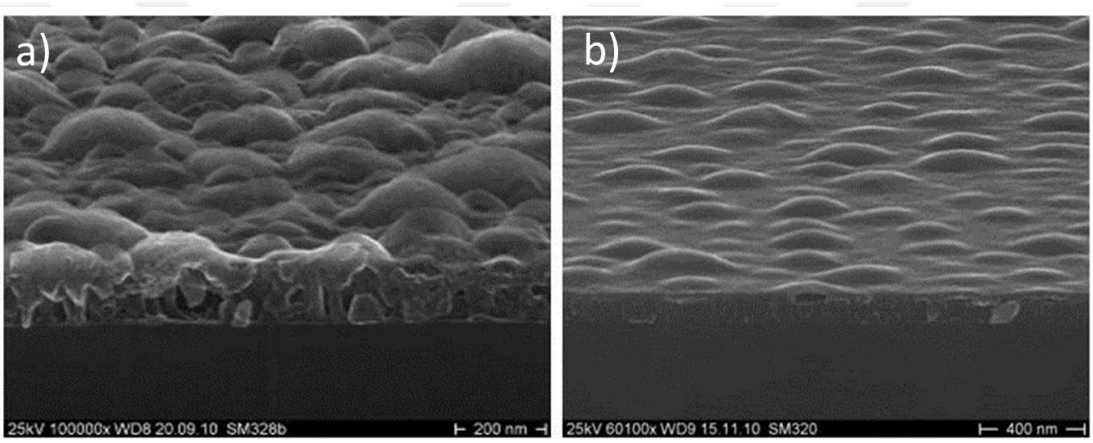

Fig. 4.11 SEM image on the CeAlO/TiN/Si (annealed at 850 °C) stacks in which Ce-Al-O deposited using precursor injection ratio of a) Ce:Al=1:1.4, b) Ce:Al=1:1.

By the formation of crystalline $CeAlO_3$ in dielectric film, k value is observed to be improved from 11 to 60, but the leakage current density worsens to 10^{-3} A/cm^2 range at -2 V as shown in Fig. 4.12. Crystallization in the dielectric and partial degradation in the bottom electrode are attributed as the reason of high leakage current through the MIM stack.

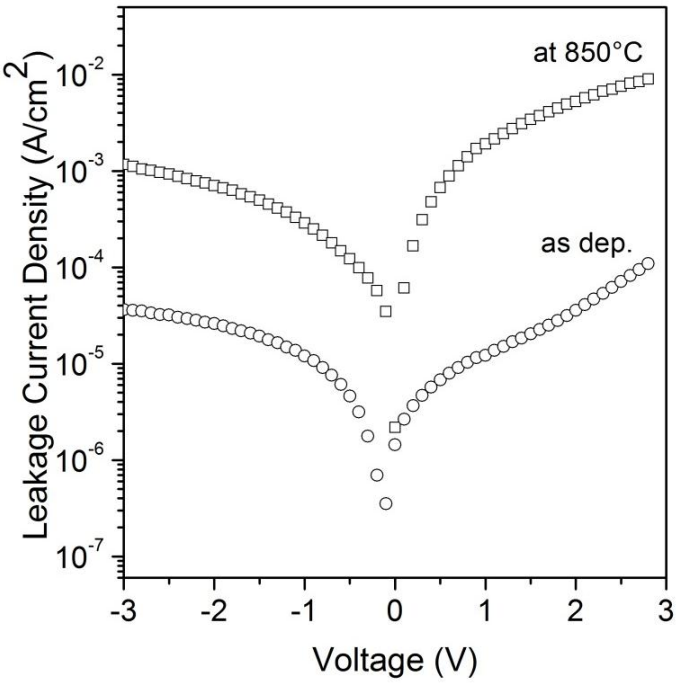

Fig. 4.12 Leakage current density of annealed Ce-Al-O samples (black solid lines) obtained with injected Ce:Al ratio equal to 1:1. The dotted line represents the leakage current density of as-deposited samples.

4.1.1.4 Summary & Conclusions

Ce-Al-O dielectric films were deposited on TiN electrode using pulsed injection MOCVD method at 400 °C. Different stoichiometry on the deposited dielectric film was obtained using different precursor ratios of Ce:Al. As-deposited Al rich Ce-Al-O films were amorphous and exhibited a k value of 20 with leakage current densities of ~10^{-5} A/cm^2. On the other hand, as-deposited cerium rich films were found to have crystalline CeO_2 phase separation and have much lower k values with higher leakage current densities than aluminum rich dielectric films.

In order to crystallize the dielectric film in the form of $CeAlO_3$ and thus obtain a high k value, high temperature annealing at 600 °C and 850 °C were applied to the samples. Among the samples deposited with different stoichiometry, the annealing lead to the formation of $CeAlO_3$ crystallization only for the precursor ratio of

Ce:Al=1:1. By crystallization in dielectric film k value was increased from 11 to 60. However, the structures were observed to be partially degraded at high annealing temperatures and exhibited higher leakage current densities. On the other hand, for the other Ce to Al precursor ratios, no $CeAlO_3$ crystallization in dielectric films was observed at all. The high temperature annealing process caused oxidation of the bottom electrode.

4.1.2 MIM Capacitors with Sr-Ta-O

Single Sr-Ta-O MIM capacitor performance is presented in this section as it is one of the promising perovskite based dielectrics in terms of its high dielectric constant. The AVD-grown Sr-Ta-O dielectric was characterized for its general MIM properties and structural properties. In addition, the annealing effect investigation is presented in this part. First, the experimental details concerning the deposition of the layers and annealing conditions are given. Afterwards, the as-deposited films characteristics, and annealing effect results are discussed in terms of electrical and physical properties. Finally, all the results on single Sr-Ta-O MIM capacitors are summarized.

4.1.2.1 Experimental Details

TaN(40 nm)/TiN(110 nm)/Ti(20 nm) bottom electrode stacks were deposited using PVD technique on Si (100) p-type substrate.

Sr-Ta-O dielectric films with thickness of ~70 nm were deposited on TaN layer of electrode stack using AVD technique. For the deposition of Sr-Ta-O films, a bis[pentakis(ethoxy)dimethylaminoethoxy)tantalum] strontium precursor, dissolved in octane, was used. The principle of AVD was based on repetitive injections of

microdoses (~3 µl) of solution of a volatile metal-organic precursor, flash evaporation at 200 °C, vapor transport by a carrier gas (Ar), and oxidant-assisted (O_2) decomposition on a hot substrate (400 °C).

In order to evaluate the electrical properties, Au top electrode stack with a thickness of ~150 nm and area of $3x10^{-3}$ cm^2 was deposited on Sr-Ta-O layer using a shadow mask at room temperature. The prepared MIM stack is seen in Fig. 4.13 schematically.

Fig. 4.13 The schematic view of the investigated single Sr-Ta-O MIM capacitor stack.

For the investigation of the effect of annealing temperature on dielectric and bottom electrode stack, just before the top electrode stack (Au) deposition, the annealing process was performed at 500 °C, 700 °C and 900 °C using the RTA equipment in N_2 ambient for 15 s. After applying annealing processes, the top electrode deposition was done.

4.1.2.2 Characteristics of As-Deposited MIM Capacitors

Microstructure examination of the as-deposited Sr-Ta-O dielectric on the electrode stack (TaN/TiN/Ti) on Si substrate was done by using XRD. In Fig. 4.14, XRD pattern of the as-deposited sample is presented. As seen in the figure, the

crystalline structure of TaN, TiN, Ti and Si substrate have been observed. In contrast, there is no diffraction peak concerning Sr-Ta-O dielectric which indicates the as-deposited Sr-Ta-O dielectric film has amorphous structure at 400 °C.

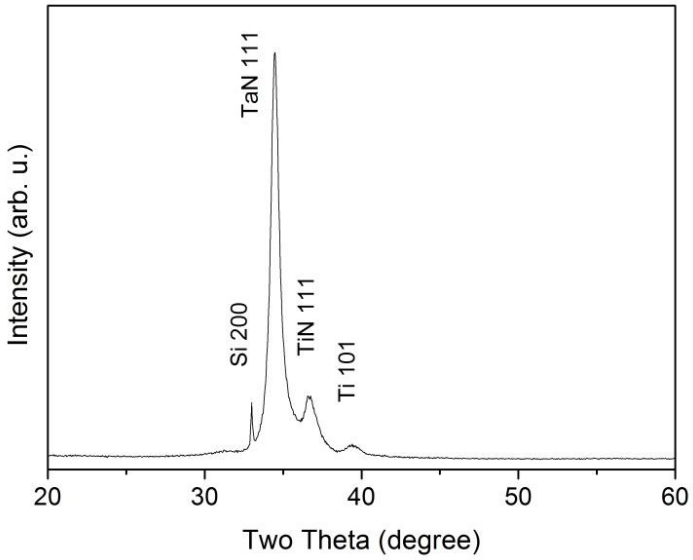

Fig. 4.14 XRD pattern of the as-deposited stack of Sr-Ta-O/TaN/TiN/Ti/Si.

In order to check chemical bonding on AVD-grown Sr-Ta-O film, XPS measurement was performed. The survey XPS spectrum recorded for the as-deposited SrTaO/TaN/TiN/Ti/Si is shown in Fig. 4.15. Since XPS is a surface sensitive technique, all the photoelectrons that reached the analyzer of XPS instrument, came from the top few nm of Sr-Ta-O dielectric film. Except the line at around ~285 eV, all the observed peaks can be attributed to photoelectrons emitted from constituent element core levels of Sr-Ta-O dielectric film. The line found at around ~285 eV is assigned to the C1s core level, which arises from adventitious hydrocarbons due to exposure of the sample to air.

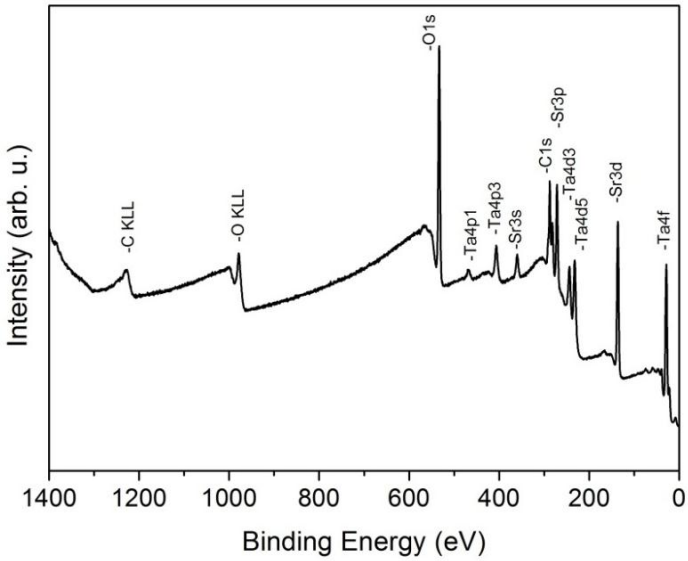

Fig. 4.15 XPS survey spectra of the as-deposited stack of Sr-Ta-O/TaN/TiN/Ti/Si.

The main transition regions for the constituent elements of Sr-Ta-O were investigated using high resolution settings. Fig. 4.16 a), b), and c) represent the high resolution XPS measurement at the transition region of Sr3d, Ta4f and O1s lines, respectively.

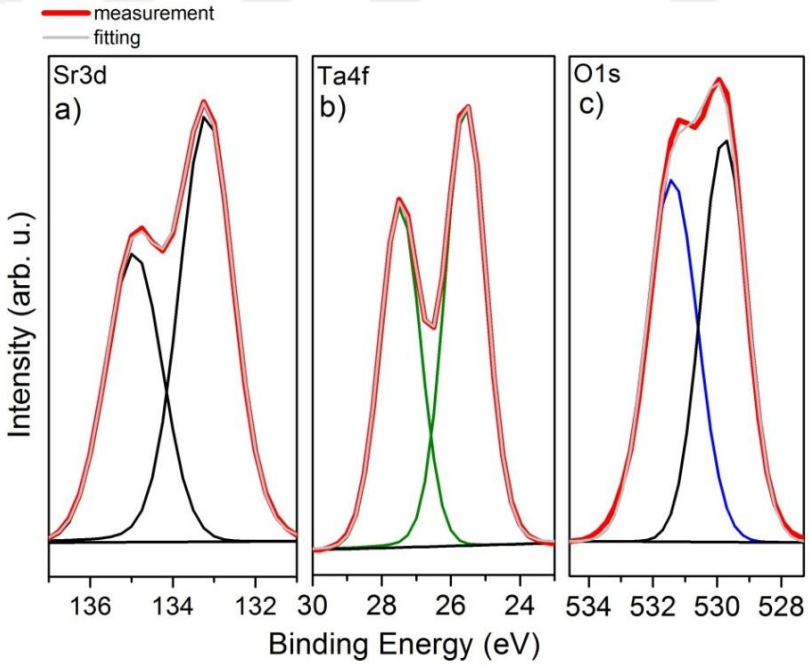

Fig. 4.16 High resolution fitted XPS spectra on Sr-Ta-O/TaN/TiN/Ti/Si, a) Sr3d doublet, b) Ta4f doublet, and c) O1s line.

Both Sr3d and Ta4f exhibit doublets due to spin-orbit splitting. The peaks reveal narrow symmetrical lines and are well fitted to unique chemical states. The detailed fitting parameters are shown in Table 3.

	$Ta4f_{7/2}$	$Ta4f_{5/2}$	$Sr3d_{5/2}$	$Sr3d_{3/2}$	O1s (oxide)	O1s (cont.)
Position (eV)	25.7	27.6	133.2	134.9	530	531.5
FWHM (eV)	1.40	1.40	1.60	1.60	1.55	1.9
Area ratio %	1.35		1.5			
Peak Splitting (eV)	1.9		1.75			

Table 3. Fitted XPS parameters of all the elements of Sr-Ta-O films.

On the other hand, for O1s, two different chemical states have been observed. Besides the spectral component related to mixed oxide dielectric at 530 eV, the peak at 531.5 eV is attributed to surface OH- groups as well as adsorbed water due to the interaction of the oxide surface with water vapor in air. The binding energy positions of Sr3d, Ta4f, and O1s (for the mixture oxide) lines are well matched with the report by Atuchin *et al.* [122], confirming that the dielectric has a composition of $Sr_2Ta_2O_7$.

The main electrical characteristic of the as-deposited case of single Sr-Ta-O MIM capacitor showed that k value was 15, and the leakage current density was around 10^{-8} A/cm^2 at 3 V as shown in Fig. 4.17 and Fig. 4.18, respectively.

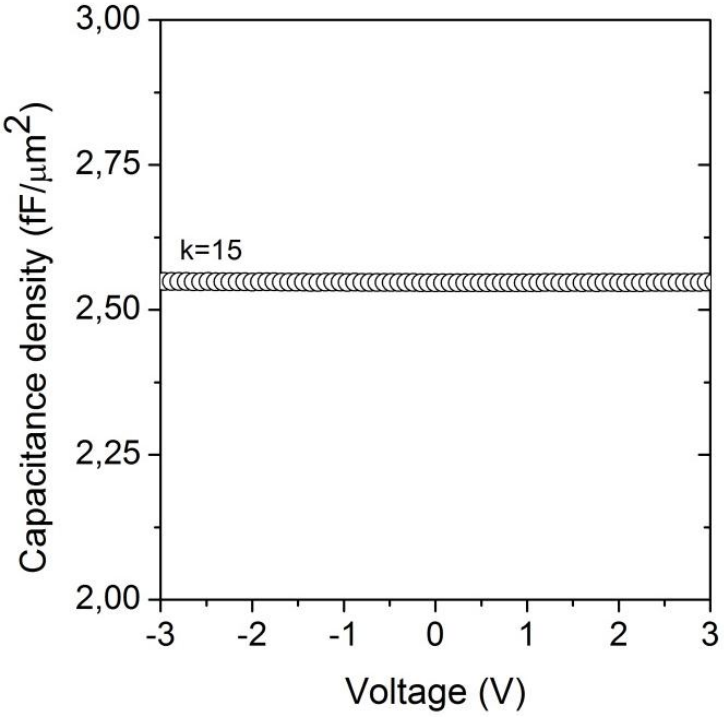

Fig. 4.17 Capacitance density vs. voltage curve with extracted k value for as-deposited status of Au/Sr-Ta-O/TaN MIM capacitor.

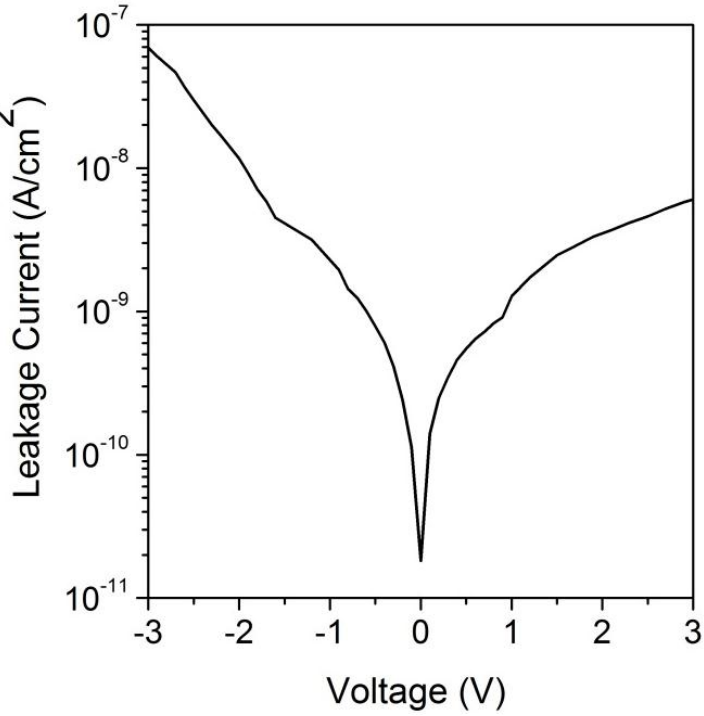

Fig. 4.18 Leakage current density vs. applied voltage on Au/Sr-Ta-O/TaN MIM capacitor.

4.1.2.3 Characteristics of Annealed MIM capacitors

In order to improve the electrical properties of the as-deposited sample, a RTA process has been applied to the samples. Three different annealing temperatures, namely, 500 °C, 700 °C, and 900 °C, have been used. For the main electrical characteristics of MIM capacitors, C-V and J-V measurements were performed. The capacitance-voltage measurements with extracted dielectric constants (k) and leakage current density measurements are shown in Fig. 4.19 and Fig. 4.20, respectively. From 500 °C to 700 °C, k value is observed to be a little larger, while it increased from 20 to 50 by the increase from 700 °C to 900 °C annealing temperature (Fig. 4.19). However, the leakage current also increases continuously by several orders of magnitude as the annealing temperature increases (Fig. 4.20).

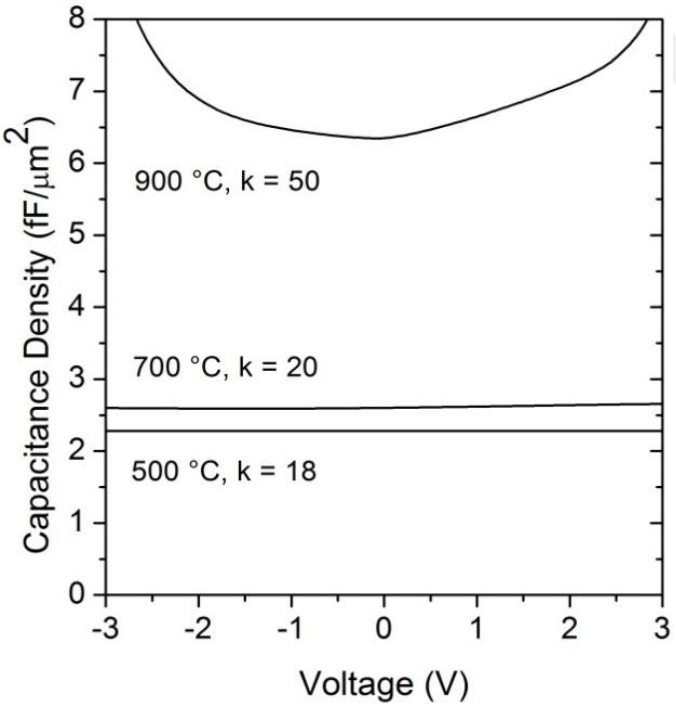

Fig. 4.19 Capacitance density vs. voltage curves with extracted k values for Sr-Ta-O MIM capacitor annealed at different temperatures.

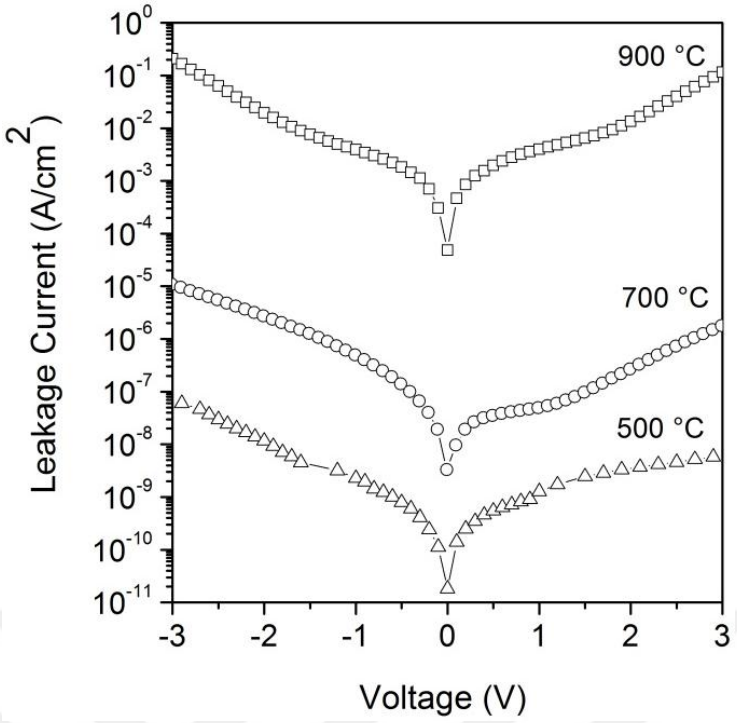

Fig. 4.20 Leakage current density vs. voltage curves measured after applying different annealing temperatures.

In order to understand the microstructural change as a function of annealing temperature XRD measurement was performed. The XRD pattern shown in Fig. 4.21 indicates that Sr-Ta-O is still in amorphous state at 500 °C and starts to crystallize at 700 °C. The Sr-Ta-O system tends to form complex structures containing perovskite building blocks [123, 124, 125]. Rodriguez *et al.* reported the observation of a metastable simple cubic perovskite-type structure in thin Sr-Ta-O films annealed at 800 °C [99]. However, many structural modifications of the cubic perovskite structure are also known for oxynitrides. $SrTaO_2N$ crystallizes in a cubic perovskite structure [126]. The observed diffraction peaks agree well with the formation of polycrystalline $SrTaO_2N$ structure. The rapid increase in k value between 700 °C and 900 °C (Fig. 4.19) can be attributed to the crystallization of the dielectric. In addition, it is revealed that the most prominent peak at 500 °C, representing the TaN electrode, vanishes at

higher annealing temperatures. Instead, peaks indicating a formation of binary compound of Ta_5Si_3 appeared. It is confirmed by the report in which it is explained that silicide formation is completed between 700 °C and 900 °C [127]. These results imply that the degradation of the TaN electrode is caused by chemical interaction between Ta and Si. In addition to the crystallization of the dielectric, the degradation of TaN electrode also has an effect on increase of leakage current, due to the change in work function. In contrast to TaN, TiN diffraction peak intensifies, becomes sharper, which indicates the continuing crystallization of the layer by the annealing process. The results also emphasize that the TiN electrode can resist at higher temperature annealing process compared to TaN electrode.

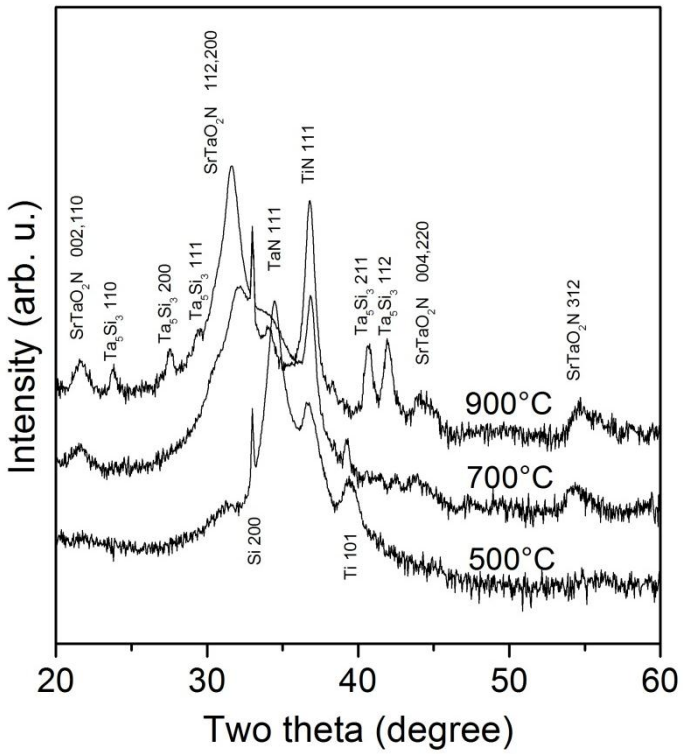

Fig. 4.21 XRD patterns of the annealed stacks of Sr-Ta-O/TaN/TiN/Ti/Si at 500 °C, 700 °C and 900 °C.

In order to study diffusion phenomena between the layers by annealing process, ToF-SIMS depth profile measurements were performed as seen in Fig.

4.22. The depth profiles show the fragment of TaN, TiN, ^{30}Si, and Ti throughout the film from top of the dielectric layer to the Si substrate as a function of annealing temperature. It is observed that the contribution of TaN fragment in the dielectric film increases with increasing annealing temperature. High annealing temperature degrades the TaN barrier and causes the diffusion of N into the dielectric layer for 700 °C and 900 °C (Fig. 4.22). This result confirms the crystallization in dielectric as $SrTaO_2N$ and deficiency of TaN (111) peak for 700 °C and 900 °C annealing process which are found from XRD measurements (Fig. 4.21).

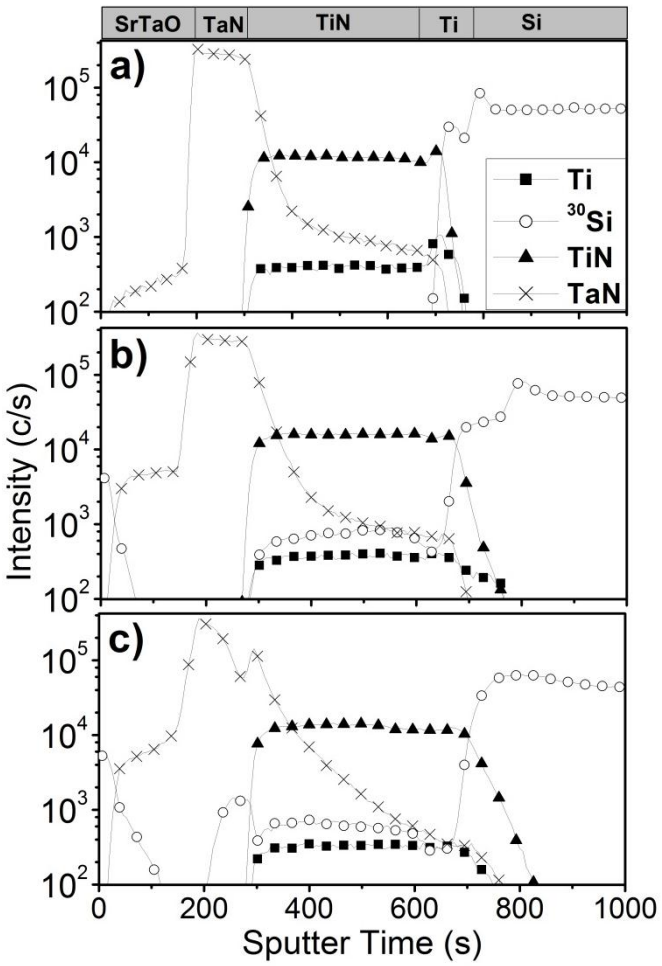

Fig. 4.22 Tof-SIMS depth profile of annealed stacks of Sr-Ta-O/TaN/TiN/Ti/Si at (a) 500 °C, (b) 700 °C and (c) 900 °C.

As the profile of ^{30}Si is followed, it is visible that Si diffuses out from the substrate through the TiN layer and segregates on the top surface of the dielectric layer at 700 °C and at 900 °C. For 900 °C, it is additionally observed that Si segregates at a depth where TaN layer already exists. This segregation of Si is reflected also in the TaN profile as a second peak since the sputtering rate is updated due to the new compound formation. This effect points out a chemical interaction between Ta in the TaN layer and segregated Si, which confirms the observation of Ta_5Si_3 compound in XRD results.

At the interface region between TiN and Si, small humps are observed for ^{30}Si, TiN and Ti profiles for the sample annealed at 500 °C, due to the different sputter rates of the distinctive layers. At 900 °C, these humps have completely vanished because of the extended interfacial layer due to diffusion. This extended interface is also the reason for the disappearance of the metallic Ti peak with increasing annealing temperature obtained from XRD measurement.

In order to understand the reaction between Ta in TaN and diffused-out Si at the interface region, sputter-XPS was performed. The spectra (Fig. 4.23 a), b), and c)) were obtained after Ar^+ ion beam sputtering on the samples and correspond to the depth where Si segregation at the interface between TaN and TiN layers is observed.

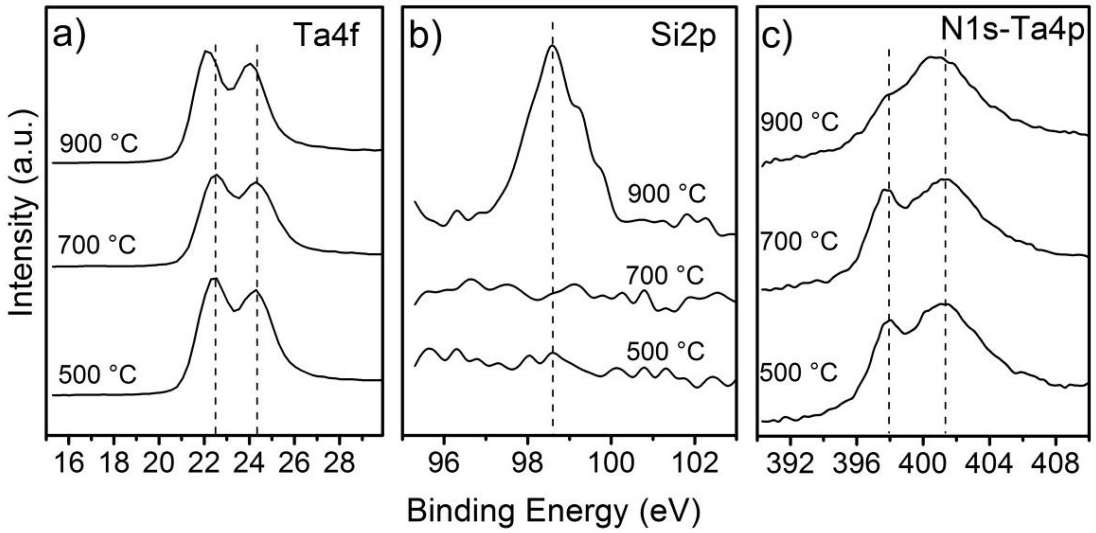

Fig. 4.23 XPS spectra corresponding a depth where Si segregation is observed between TaN and TiN electrode layer, (a) Ta4f, (b) Si2p and (c) N1s–$Ta4p_{3/2}$.

It is revealed that after annealing at 500 °C and 700 °C, $Ta4f_{7/2}$ peak position does not change and remains at 22.5 eV which agrees with the Ta_2N phase (Fig. 4.23 a)) [128, 129]. After annealing at 900 °C, 0.5 eV energy shift towards lower binding energy is observed. This chemical shift has been correlated with the corresponding Si2p spectra (Fig. 4.23 b)) observed at 98.6 eV for 900 °C and it matches well with Ta_5Si_3 formation [130]. Regarding the electro-negativity difference between N and Si (3.0 and 1.9 respectively), Ta4f chemical shift towards lower binding energy is reasonable due to the formation of Ta_5Si_3. Fig. 4.23 c) shows N1s and $Ta4p_{3/2}$ analysis region. For samples annealed at 500 °C and 700 °C, N1s peak is observed at 397.9 eV distinctively which is consistent with Ta_2N [131]. However for the sample annealed at 900 °C, N1s peak decreases in intensity and becomes slightly indistinct due to Ta_5Si_3 formation. In addition a slight shift to lower binding energy for $Ta4p_{3/2}$ is visible and coherent with Ta_5Si_3 formation by annealing at 900 °C.

Cross-sectional SEM images of the samples annealed at different temperatures are shown in Fig. 4.24. The morphology of the dielectric seems to be amorphous for 500 °C while it is modified for 700 °C and 900 °C due to the crystallization. The image of the stack annealed at 700 °C exhibits that the crystallization in dielectric film starts at the SrTaO/TaN interface region. These findings support the thesis that the crystallization in dielectric occurs due to the degradation of TaN electrode and following N diffusion into dielectric layer caused by annealing. The observed ongoing crystallization of dielectric between 700 °C and 900 °C is also consistent with the drastic increase in k value observed for these temperatures. In addition, the layer observed on top of the dielectric as different contrast for the image of 900 °C may be associated with ToF-SIMS depth profiles, in which Si diffusion towards the top of dielectric surface increases with increasing annealing temperature is shown (Fig. 4.22). XPS measurement on the surface of the sample annealed at 900 °C revealed that the Si2p binding energy is at around 102.0 eV which confirms an oxidized state of Si.

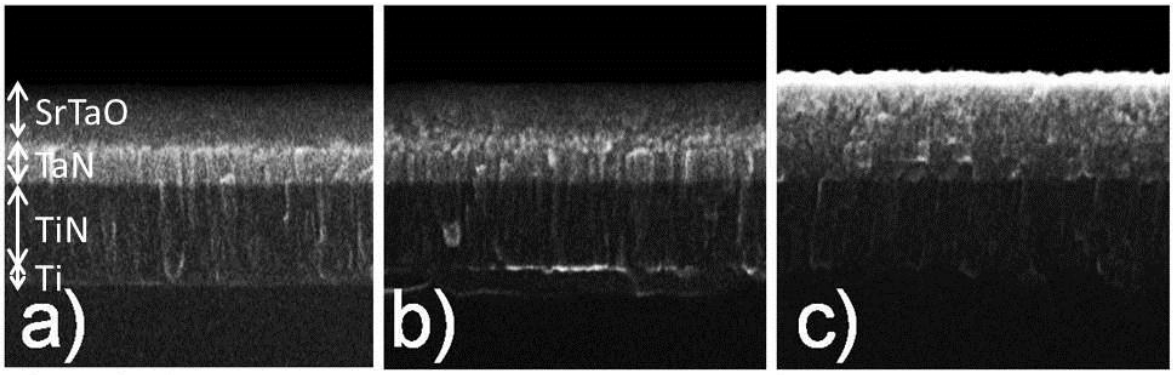

Fig. 4.24 Cross-sectional SEM images of annealed stacks of Sr-Ta-O/TaN/TiN/Ti/Si at a) 500 °C, b) 700 °C and c) 900 °C.

4.1.2.4 Summary & Conclusions

Sr-Ta-O dielectric films were deposited on TaN/TiN/Ti/Si substrate using AVD method at 400 °C. The MIM structure was completed by deposition of the Au top electrode on the Sr-Ta-O layer. In order to investigate the annealing effect, three different annealing temperatures, namely 500 °C, 700 °C, 900 °C were applied to the samples before top electrode deposition.

XRD measurement on as-deposited Sr-Ta-O dielectric on bottom electrode showed that the dielectric has an amorphous microstructure. It has a composition of $Sr_2Ta_2O_7$ according to the chemical states of the constituent elements measured by XPS. The electrical response of the as-deposited case of MIM structure showed a k value of around 18 accompanied with a leakage current of around 10^{-8} A/cm^2.

By the thermal treatment on the single Sr-Ta-O MIM capacitor, the dielectric film was observed to be crystallized at 700 °C starting from the interface region between Sr-Ta-O and TaN layers. XRD measurements exhibited that the crystallization in dielectric occurred in the form of $SrTaO_2N$. N diffused out into the dielectric layer due to the degradation of TaN bottom electrode at high annealing temperatures as proved by Tof-SIMS measurement.

The crystallization in the dielectric layer improved the dielectric constant of the film from 18 to 50. However, the annealing at 700 °C and 900 °C caused higher leakage current. The increase of the leakage current density was explained in terms of crystallization of dielectric, degradation of TaN electrode material and out-diffusion of Si from the substrate. It was also concluded that the TiN electrode can survived at higher temperature annealing process compared to TaN electrode.

4.2 MIM Capacitors with Multilayer Dielectric

Multilayer dielectric configuration is a very promising method for MIM capacitors, as it allows one to tailor useful properties of different materials, most importantly high permittivity and low conductivity. This section presents multilayer dielectrics consisting of $SrTiO_3$/SrTaO and $SrTiO_3/Al_2O_3$. $SrTiO_3$ was used as high k source in these structures, while SrTaO and Al_2O_3 are utilized for improving the interfacial properties and thus lower leakage current. Optimization of these alternative dielectric configurations has been performed to reach the ideal properties of MIM capacitors. In order to see the effect of additional layers in a MIM stack, the results for a single $SrTiO_3$ MIM capacitor are also included.

4.2.1 MIM Capacitors with $SrTiO_3$/Sr-Ta-O

The stacked configurations of dielectrics consisted of $SrTiO_3$/Sr-Ta-O for MIM capacitors are presented in this part.

In order to improve $SrTiO_3$ single layer dielectric MIM capacitor properties, SrTaO additional layer was used with asymmetric bilayered structures in MIM structures. As $Sr_2Ta_2O_7$ has a moderate k value (~20) and amorphous structure at the crystallization temperature of $SrTiO_3$ (550 °C) the multilayer dielectric constructed by $Sr_2Ta_2O_7/SrTiO_3$ is very promising for MIM capacitors. However, so far, no report concerning the combination of these materials has been published in the literature. In this thesis, the electrical and physical characteristics of multilayer dielectric MIM capacitors constituted of SrTaO and $SrTiO_3$ are systematically investigated for the first time. A comparative study is presented in terms of the effect using sequences of dielectrics in multilayer dielectric structures for MIM capacitor application.

Firstly, the experimental details about the preparation of the stacks are given, and then the results concerning the optimization of the multilayered dielectric MIM capacitor stack are discussed in detail. All the results concerning $SrTiO_3$-SrTaO multilayer dielectric MIM capacitor are summarized in the conclusions part of this section.

4.2.1.1 Experimental Details

Multilayer bottom electrode of TaN/TiN/Ti was prepared by PVD sputtering technique on 200 mm Si(100).

As a dielectric layer 50 nm $SrTiO_3$ was deposited on TaN electrode using ALD technique in Pulsar 2000 reactor at 250 °C. $(1,2,4\text{-tertiarybutyl-Cp})_2Sr$ (from SAFC) and $Ti(OMe)_4$ were used as the metal precursors and H_2O was used as the oxidizing agent.

The details about the AVD technique for SrTaO were already described in the single SrTaO dielectric MIM section (chapter 4, section 4.1.2.1).

The completion of MIM stack was done by Au dot top electrode with a thickness of ~150 nm and area of $3x10^{-3}$ cm^2 which was deposited using shadow mask evaporation technique on top of dielectric material.

All the prepared stacks are annealed at 550 °C in nitrogen ambient for 10 min.

4.2.1.2 Optimization of the MIM stack

SrTaO thickness optimization

In order to optimize the thickness of additional SrTaO layer in bidielectric MIM stack, different thicknesses of SrTaO were deposited on top of TaN bottom electrode layer using AVD technique. Single $SrTiO_3$ MIM capacitor was also prepared and used as reference sample. All the prepared stacks are described in Fig. 4.25. In the stacks, the $SrTiO_3$ thickness is fixed at 50 nm and combined with 3 different SrTaO thicknesses of 0, 3, 6 and 9 nm.

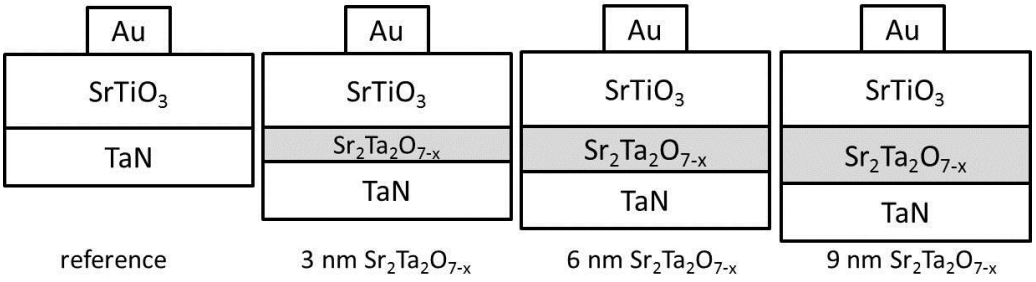

Fig. 4.25 Schematic structures of the prepared multilayer dielectric MIM capacitor consisted of $SrTiO_3$-SrTaO as dielectric stack using different SrTaO thicknesses: 0 (reference), 3, 6 and 9 nm.

As $SrTiO_3$ is the main dielectric material and expected to be the source of high capacitance density in the proposed MIM capacitors, annealing processes are applied at 550 °C for the crystallization of $SrTiO_3$ layers. Fig. 4.26 shows the XRD pattern, recorded after the annealing process of the pure $SrTiO_3$ structure (reference) as well as the bilayered $SrTiO_3$-SrTaO (9 nm) film on the bottom metal electrode stack. It is seen that both the $SrTiO_3$ films are crystallized in the cubic perovskite phase, while the $Sr_2Ta_2O_{7-x}$ film remains amorphous as expected. Typical crystallization temperature of strontium tantalate is 700-800 °C, as shown by Regnery *et al.* [79].

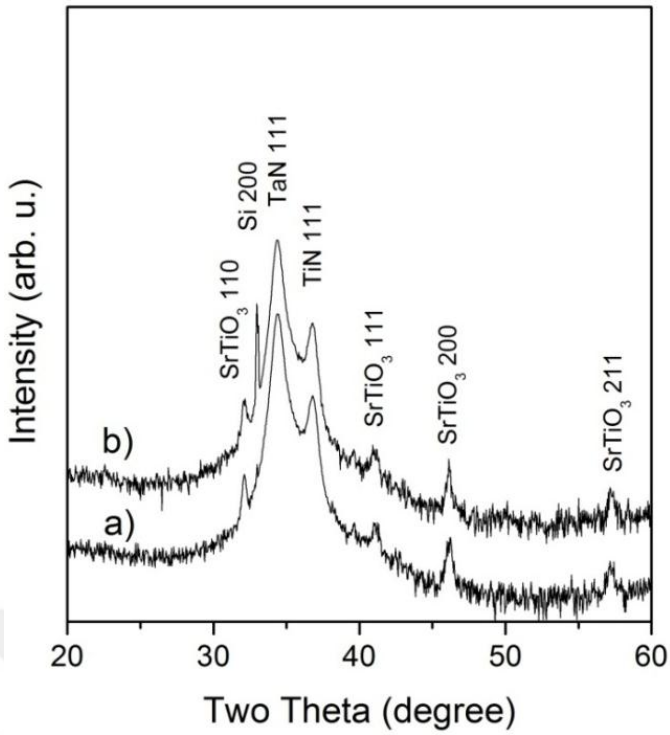

Fig. 4.26 XRD patterns of samples after annealing process: a) reference sample ($Si/TiN/TaN/SrTiO_3$), b) 9 nm $Sr_2Ta_2O_{7-x}$ deposited sample ($Si/TiN/TaN/Sr_2Ta_2O_{7-x}/SrTiO_3$).

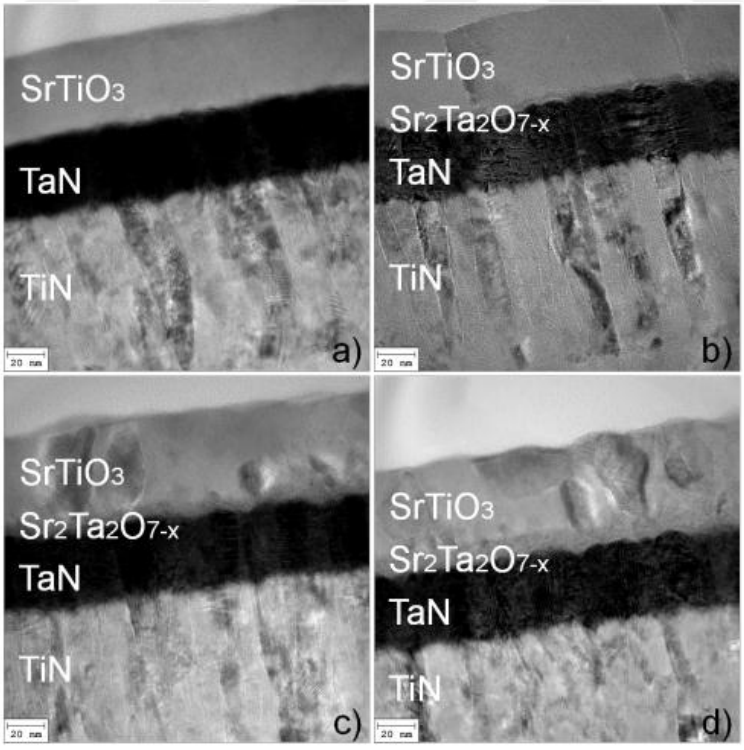

Fig. 4.27 Cross-sectional TEM images of samples after annealing process: a) reference sample: ($TiN/TaN/SrTiO_3$), b) 3nm $Sr_2Ta_2O_{7-x}$, c) 6 nm $Sr_2Ta_2O_{7-x}$, d) 9 nm $Sr_2Ta_2O_{7-x}$ deposited sample: ($TiN/TaN/Sr_2Ta_2O_{7-x}/SrTiO_3$)

Cross-sectional TEM images of the bilayered dielectrics with 3 nm, 6 nm and 9 nm $Sr_2Ta_2O_{7-x}$ layers as well as the one with single $SrTiO_3$ dielectric on bottom electrode stacks are shown in Fig. 4.27. The amorphous character of the $Sr_2Ta_2O_{7-x}$ interlayer after the annealing step is visible for each stack. Although the TiN/TaN bottom electrode stack has a high roughness, even the 3 nm thick $Sr_2Ta_2O_{7-x}$ layer covers the electrode surface uniformly due to the advantage of AVD technique. In addition, there are not any visible interfacial layers between $Sr_2Ta_2O_{7-x}$ and TaN layers.

Electrical measurements were performed on the TaN/$Sr_2Ta_2O_{7-x}$/ $SrTiO_3$/Au MIM capacitors. The extracted C_0 values and the effective k values as a function of additional SrTaO thickness are shown in Fig. 4.28. The single $SrTiO_3$ dielectric MIM capacitor provides a k value of 95 and high capacitance density of 17 fF/μm^2. With increasing thickness of the underlying $Sr_2Ta_2O_{7-x}$ layer, the capacitance density is reduced to 9 fF/μm^2.

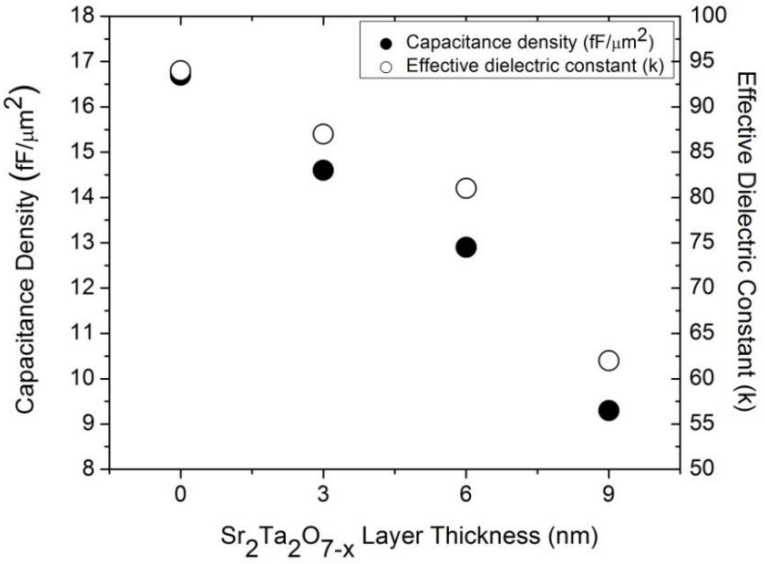

Fig. 4.28 Capacitance density (solid circle) and effective dielectric constant (open circle) vs. thickness of $Sr_2Ta_2O_{7-x}$ layer in the bilayered $Sr_2Ta_2O_{7-x}$/$SrTiO_3$ dielectric MIM capacitors.

Due to the lower k-value of 20 of the amorphous $Sr_2Ta_2O_{7-x}$ film, the effective dielectric constant of the insulating bilayer is reduced to 62 for the 9 nm $Sr_2Ta_2O_{7-x}$/50 nm $SrTiO_3$ stack. The total capacitance C_{total}, and consequently the effective k value are defined by the lowest k value of $Sr_2Ta_2O_{7-x}$ according to the equation for capacitors connected in series:

$$C_{total} = \frac{C_{SrTiO_3} \times C_{Sr_2Ta_2O_{7-x}}}{C_{SrTiO_3} + C_{Sr_2Ta_2O_{7-x}}} \qquad \text{Equation 4.1}$$

where, C_{SrTiO_3} and $C_{Sr_2Ta_2O_{7-x}}$ are the contributions of $SrTiO_3$ and $Sr_2Ta_2O_{7-x}$, respectively.

Fig. 4.29 presents the typical J-V characteristics of the MIM capacitors with 3, 6 and 9 nm additional SrTaO layer.

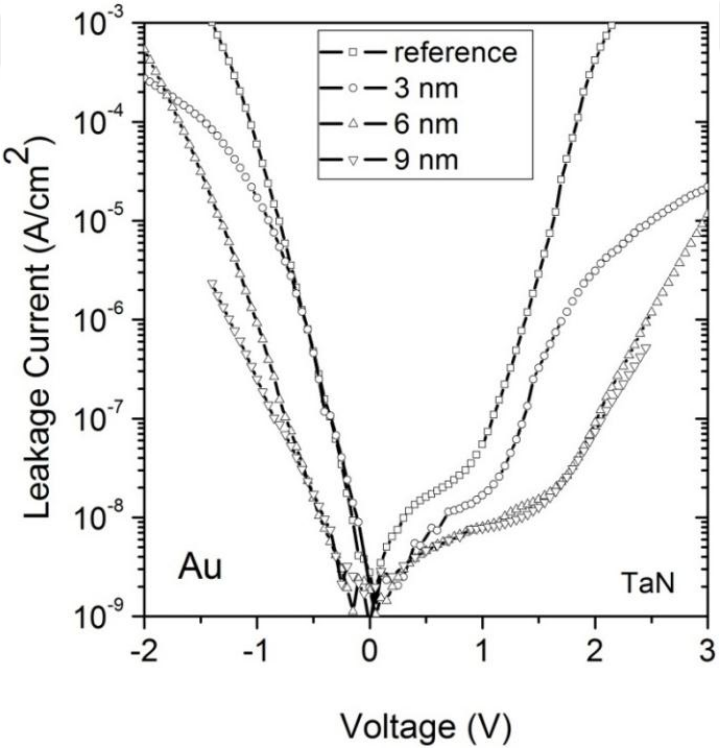

Fig. 4.29 Leakage current density vs. bias voltage measurement on single $SrTiO_3$ and bilayered dielectric MIM capacitors with varied thickness of $Sr_2Ta_2O_{7-x}$.

The leakage current density of the single layer $SrTiO_3$ (50 nm) MIM capacitor is 4 x 10^{-4} A/cm^2 at 2 V. This leakage value can be drastically reduced to 8 x 10^{-8} A/cm^2 by introducing a 6 nm thick $Sr_2Ta_2O_{7-x}$ layer underneath the $SrTiO_3$ films. Such low leakage currents are most likely attributed the incorporations of thin amorphous $Sr_2Ta_2O_{7-x}$ layers. Slow oxygen diffusion through Sr-Ta-O matrix improves the interface properties. However, the further increase of the $Sr_2Ta_2O_{7-x}$ thickness does not improve the leakage current density further for the bilayered dielectric MIM capacitors.

Interfacial reactions which occur at metal/insulator interfaces can affect the electrical performance of MIM capacitors [132, 133]. The reactive TaN electrodes can interact with the dielectric, creating defect states within the dielectric, and thus increase the leakage current density [134]. In order to study the interfacial characteristic of the metal/dielectric (TaN/$Sr_2Ta_2O_{7-x}$) interface, XPS depth profiles were obtained by performing a low energy Ar^+ ion sputtering process. Fig. 4.30 illustrates the distribution of elements of strontium and nitrogen across the particular layers of interest (TaN/$Sr_2Ta_2O_{7-x}$/$SrTiO_3$) for the investigation of dielectric/metal interface. The cross-over points of strontium and nitrogen profiles have been utilized as a representative point for the TaN/$Sr_2Ta_2O_{7-x}$ interface [135] shown detailed in the inset figure of Fig. 4.30. It is visible that as the thickness of $Sr_2Ta_2O_{7-x}$ increases, the sputtering time to reach to the interface increases (141 min. for 3 nm $Sr_2Ta_2O_{7-x}$; 148 min. for 6 nm $Sr_2Ta_2O_{7-x}$; 152 min. for 9 nm $Sr_2Ta_2O_{7-x}$). The sputtering rate was determined using $SrTiO_3$ films of known thickness and found to be about 0.4 nm/ min. Fig. 4.31 demonstrates the photoelectron spectra (Ta4f, N1s, Sr3d, O1s) taken from each sample at the interface region between TaN/$Sr_2Ta_2O_{7-x}$ as it is indicated in the

depth profile (Fig. 4.30) by the vertical lines. The spectra of each element obviously declare that there is no visible change in the binding energies at the interface between TaN/$Sr_2Ta_2O_{7-x}$ for different thicknesses of $Sr_2Ta_2O_{7-x}$ which indicates that dielectric/metal interfaces are identical.

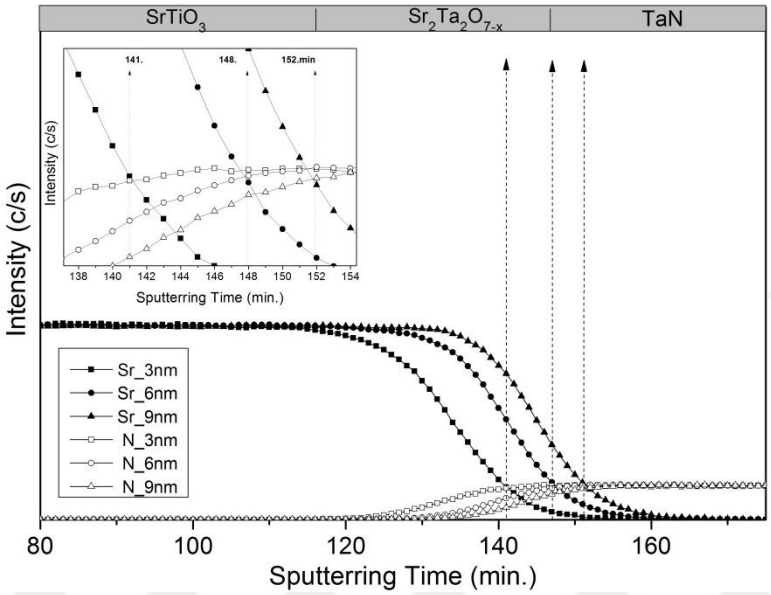

Fig. 4.30 XPS depth profiles for strontium and nitrogen (inset figure: zoom in version of strontium and nitrogen profile at the interface region).

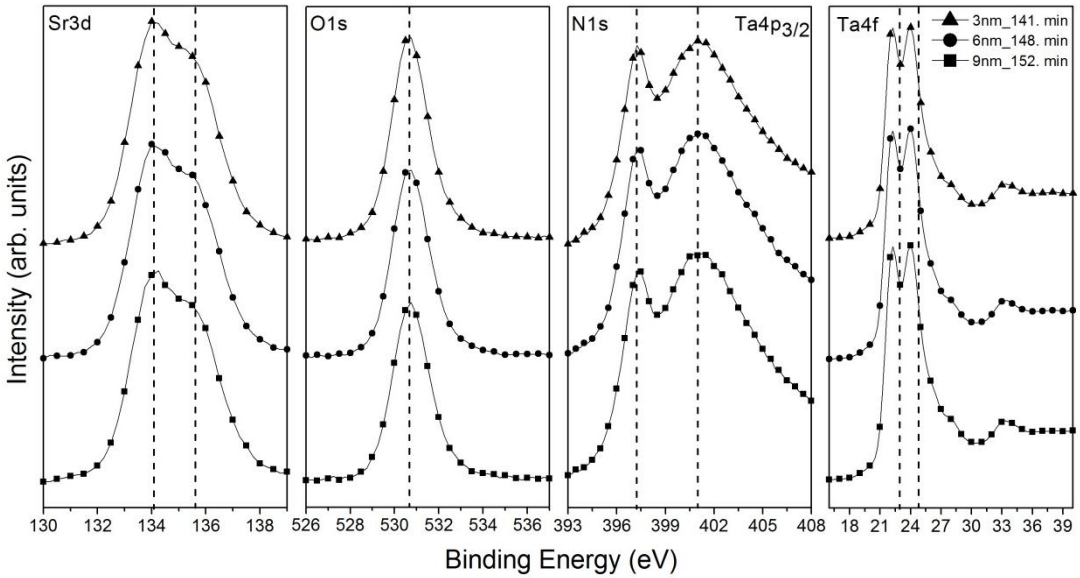

Fig. 4.31 XPS spectra (Sr3d, Ta4f, O2s, N1s) for each sample obtained from corresponding cross- sections as representative of $Sr_2Ta_2O_{7-x}$/TaN interface (141 min. for 3 nm, 148 min. for 6 nm, 152 min. for 9nm $Sr_2Ta_2O_{7-x}$ deposited bilayered $Sr_2Ta_2O_{7-x}$/$SrTiO_3$ dielectric MIM capacitors).

According to the results on TaN bottom/SrTaO/$SrTiO_3$/Au top electrode configuration, the optimized bilayered dielectric system constructed by 6 nm SrTaO and 50 nm $SrTiO_3$ provides the optimum results in terms of capacitance density and leakage current.

Optimization of deposition sequences of dielectric layers

In the second part of this section, influences of deposition sequences of dielectric materials on the main MIM properties are presented. As the thickness of additional SrTaO layer is optimized as 6 nm, an opposite sequence of dielectrics has been prepared for 6 nm and compared with the previous results. The studied bilayered MIM stacks for this part of the thesis are seen schematically in Fig. 4.32.

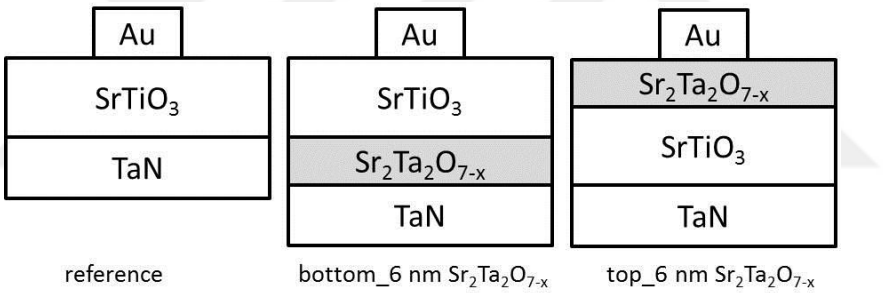

Fig. 4.32 Schematic of the prepared multilayer dielectric MIM capacitor consisted of $SrTiO_3$-SrTaO as dielectric using different sequences of deposition of dielectrics.

After the post-deposition annealing process at 550 °C, XRD measurement was performed. The corresponding result on the sample with additional 6 nm SrTaO on top is shown together with single $SrTiO_3$ reference sample in Fig. 4.33. It is seen that the $SrTiO_3$ film is crystalline, while $Sr_2Ta_2O_7$ remains in its amorphous state by this opposite sequence of dielectrics.

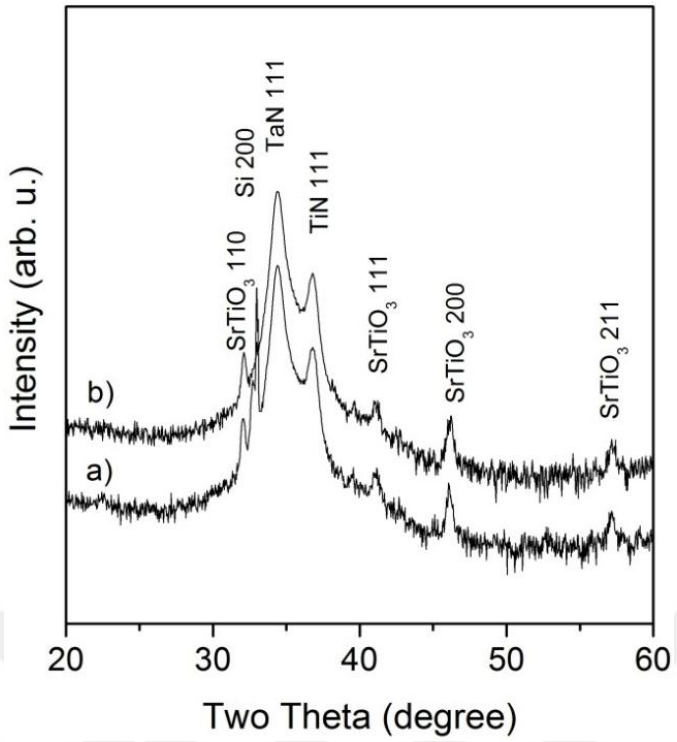

Fig. 4.33 XRD pattern of the sample with a) 6 nm SrTaO deposited on top b) single $SrTiO_3$ on bottom electrode stack (reference sample).

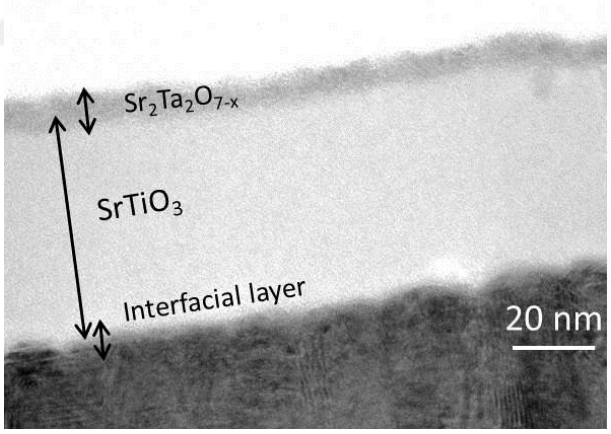

Fig. 4.34 Cross-sectional TEM images of 6 nm $Sr_2Ta_2O_{7-x}$ on $SrTiO_3$/TaN after annealing process.

A cross-sectional TEM image of the stack is seen in Fig. 4.34. The 6 nm additional SrTaO layer is clearly visible on 50 nm of $SrTiO_3$ layer. In addition, between $SrTiO_3$ and bottom TaN electrode around ~1-2 nm of interfacial layer can be observed faintly, probably due to the oxidized bottom electrode.

The C-V measurement on the samples with opposite deposition sequence of dielectric stack is seen in Fig. 4.35 with the extracted effective k values. The measurement result on single $SrTiO_3$ dielectric MIM capacitor is also added to the plot. As seen in the figure, with additional 6 nm SrTaO the capacitance density is reduced. However, the top and bottom deposition of 6 nm of SrTaO resulted in different capacitance densities and thus different effective k values. Bottom deposition of SrTaO resulted in a capacitance density of 13.3 fF/μm^2 while the top deposition of SrTaO gave a capacitance density of 11.6 fF/μm^2. The difference is attributed to additional interfacial layer formation between $SrTiO_3$ and TaN for the top deposition case of SrTaO. This interface has been shown to be prevented when SrTaO deposited under $SrTiO_3$, on top of TaN bottom electrode (Fig. 4.27 (c)). Nevertheless, the capacitance density values obtained by this bilayered dielectric configuration are still acceptable for future MIM capacitors.

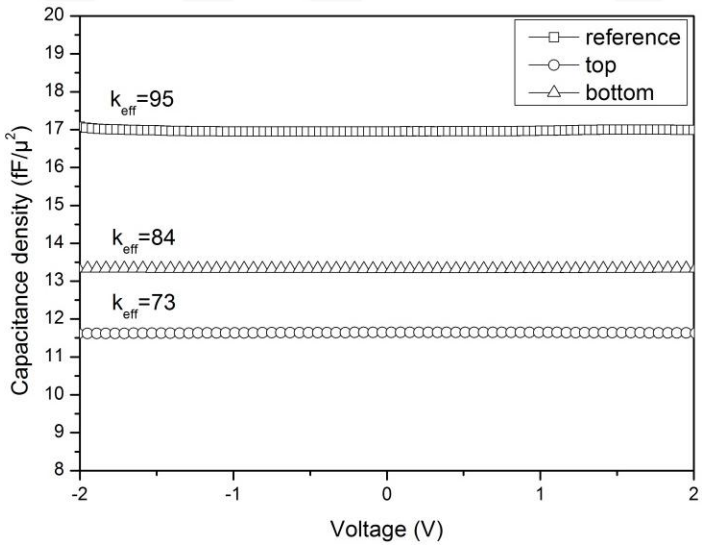

Fig. 4.35 Capacitance density vs. applied voltage for the samples with opposite deposition sequence (SrTaO deposition on top or bottom of $SrTiO_3$) and reference sample.

The comparisons of leakage current density measurements on the MIM capacitor stacks are seen in Fig. 4.36. At negative bias voltage the leakage current is

observed clearly to be controlled by the top electrode/dielectric interface. It is seen that SrTaO deposition between Au top electrode and $SrTiO_3$ dielectric improves the leakage current for several orders of magnitude for the case of top injection. This effect can be explained both by the higher band gap of SrTaO and by its amorphous structure which prevents the creation of an electron path. On the other hand, the leakage current at positive bias voltages was observed to be the same until to the applied bias voltage of ~2 V and is 2.10^{-8} A/cm^2. The effect of additional SrTaO thickness is visible at bias voltages higher than 2 V. The sample with a top deposition of SrTaO (6 nm) layer shows better leakage current by around one order of magnitude at bias voltages higher than 2 V.

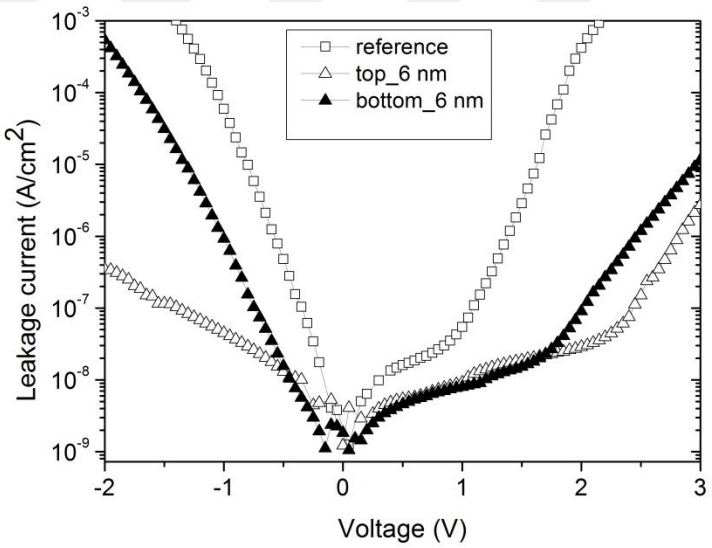

Fig. 4.36 Leakage current density versus bias voltage measurement on single $SrTiO_3$ and bilayered dielectric MIM capacitors with varied thickness of $Sr_2Ta_2O_{7-x}$.

4.2.1.3 Summary & Conclusions

A combination of $SrTiO_3$-SrTaO is studied for multilayer dielectric MIM capacitor. Although single $SrTiO_3$ (50 nm) MIM capacitor gave excellent capacitance density of around 17 fF/µm^2 owing to its high k value of ~95, the leakage current

density was obtained to be very high (~ 10^{-2} A/cm^2). The additional SrTaO on top of TaN electrode obviously improved the leakage with cost of reduced capacitance density. Nevertheless, the thickness of SrTaO is optimized in multilayer dielectric MIM capacitor for 6 nm with very promising leakage current and capacitance density values of 10^{-8} A/cm^2 and 13 fF/μm^2, respectively. Additionally, the deposition sequence of dielectric layers are investigated in terms of main MIM capacitor properties. 6 nm SrTaO was deposited in the opposite way, between top Au electrode and $SrTiO_3$. The results have proved the significance of the sequences of dielectrics in multilayer dielectric MIM capacitor. The capacitance density obtained was around 2 fF/μm^2 higher for bottom deposition of SrTaO than that of top deposition. The reason for this difference is attributed to worse interfacial status between $SrTiO_3$ and TaN electrode compared to SrTaO/TaN electrode. A TEM image has shown around 1-2 nm interface layer formation between $SrTiO_3$ and TaN bottom electrode. From the leakage current point of view, the effect of sequence of dielectric stack has shown that top deposition of SrTaO in the dielectric stack proves one order of magnitude better leakage current values at bias voltages higher than 2 V.

4.2.2 MIM Capacitors with $SrTiO_3/Al_2O_3$

This section of the thesis covers the studies concerning the combination of $SrTiO_3$ and Al_2O_3 as a dielectric layer for alternative MIM capacitor structure.

As Al_2O_3 has an amorphous matrix at the crystallization temperature of $SrTiO_3$ (~ 550 °C) and it exhibits a rather large band gap value of 8.7 eV, a multilayer dielectric constituted of $SrTiO_3$ and Al_2O_3 is a good candidate for future MIM capacitors.

Before the optimization of the multilayer dielectric system single $SrTiO_3$ dielectric is optimized for its ideal composition and response. Afterwards, multilayer dielectric layer MIM capacitor optimization on different electrodes is performed in a systematic way. Firstly the experimental details about the deposition of the MIM stacks are given in the experimental details part. Afterwards, the characteristics of the prepared stacks are given according to the used electrode. Finally, all the results are summarized.

4.2.2.1 Experimental Details

The MIM capacitors were fabricated on Si (100) substrate. TaN and TiN were used as bottom electrode and deposited using PVD technique.

Thin films of $SrTiO_3$ as well as of Al_2O_3 were deposited by ALD in an ASM Pulsar® 200 type reactor at 250 °C using $(1,2,4\text{-tertiarybutyl-Cp})_2Sr$ + $Ti(OMe)_4$ and $Al(CH_3)_3$ metal precursors. O_3 was added as the oxidizing agent. Composition of the $SrTiO_3$ films was controlled by changing the cycle ratios of the SrO and TiO_2 deposition steps.

Post deposition annealing processes were done in nitrogen ambient for 5 min.

In order to evaluate the electrical properties, Au top electrode stack with a thickness of ~150 nm and area of $3x10^{-3}$ cm^2 was deposited through shadow mask evaporation at room temperature.

4.2.2.2 Characterization Results

The characterization results on the MIM capacitor stacks are categorized according to the used bottom electrode. Firstly, the results on TaN electrode are given and then the results on TiN electrode are discussed.

On TaN bottom electrode

Before investigation of the MIM capacitor structure with multilayer dielectric, a MIM capacitor with single $SrTiO_3$ dielectric was investigated for its optimum characteristics.

In order to reach the right composition of $SrTiO_3$, different injection ratios of Sr to Ti precursors were used. All the Sr-Ti-O layers with thicknesses of 50 nm were deposited on PVD-grown TaN bottom electrode. In Fig. 4.37, the prepared single Sr-Ti-O MIM capacitor stacks are illustrated schematically.

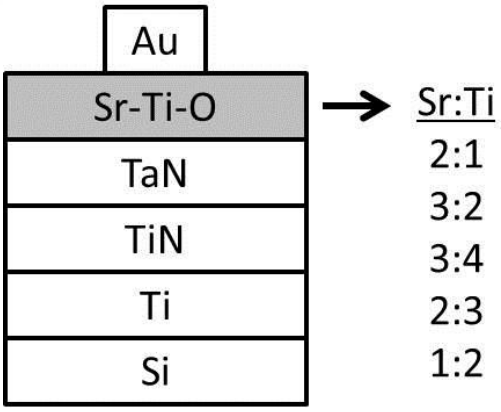

Fig. 4.37 Schematic view of the single Sr-Ti-O MIM capacitors in which Sr-Ti-O layers were deposited with different injection ratios of precursors.

After applying an annealing process at 600 °C, for the investigation of the microstructure of the deposited Sr-Ti-O dielectric films with different precursor ratios,

XRD measurements were performed as seen in Fig. 4.38. The reference XRD data obtained on the powdered $SrTiO_3$ sample is also seen on the bottom of the figure.

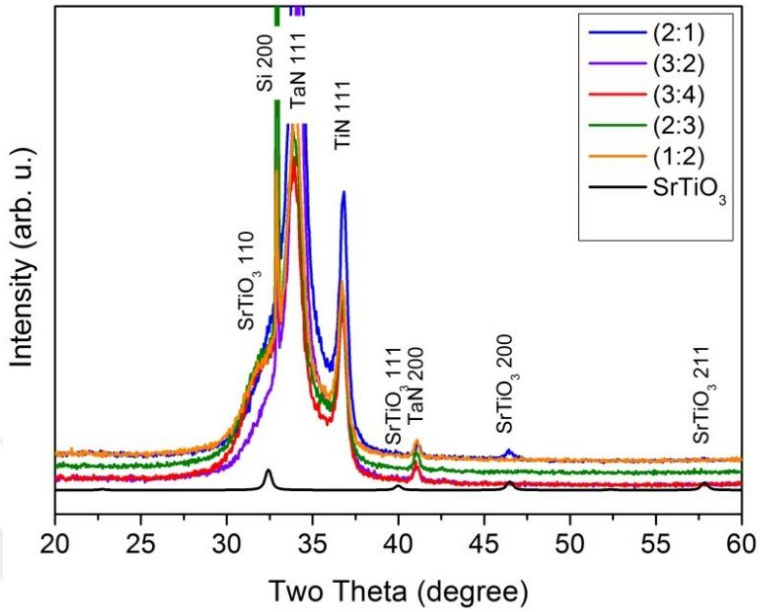

Fig. 4.38 XRD patterns of Sr-Ti-O films deposited with different injection ratio of precursors. (black line on the bottom indicates a reference data obtained from powder $SrTiO_3$ sample)

According to XRD measurements, all the deposited dielectric films on TaN electrodes are obtained as crystalline structure due to the common shoulder peak observed at around 32.5°. Only for the case of injection ratio of 2:1 an additional diffraction peak is observed at around 47° corresponding to $SrTiO_3$ 200 orientation.

The C-V measurements and the extracted k values are seen in Fig. 4.39, for each injection ratio of precursors. The highest k value obtained was 30, for the 2:1 ratio. Although it is the highest k value among the other samples, it is still far from the expected value (~100) for crystalline $SrTiO_3$ films. This low k value can be attributed to interfacial layer formation between the dielectric and TaN bottom electrode.

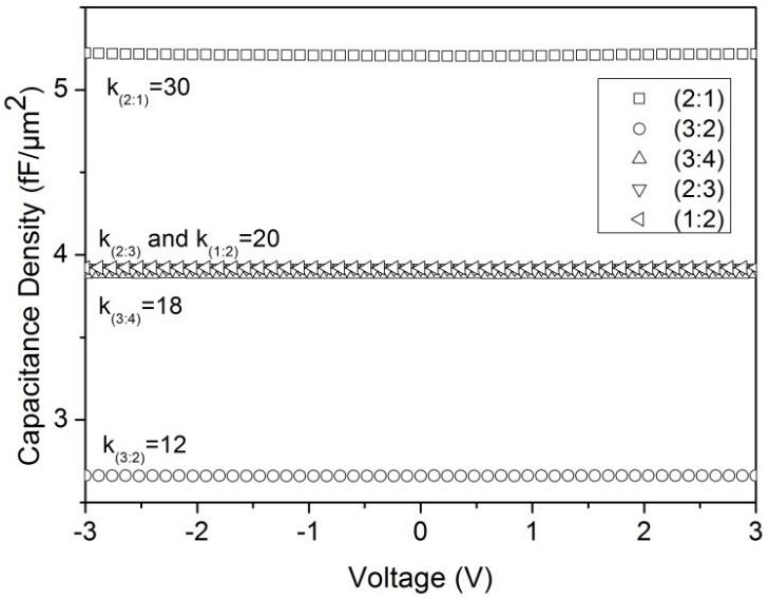

Fig. 4.39 Capacitance density vs. bias voltage for Sr-Ti-O films deposited with different injection ratio of precursors.

In order to investigate the interface properties of this stack (Sr:Ti=2:1) sputtering XPS measurement was performed. Fig. 4.40 shows XPS spectra of Ta4f transition region after periodical (every 10 min) Ar^+ ion beam sputtering processes for the sample deposited with 2:1 precursors injection ratio. In this case the dielectric thickness was 30 nm. Until the 30th min. of sputtering there is no peak related to Ta4f. Only small peaks corresponding to Sr4s (~39 eV), Sr4p (~21 eV) and O2s (~23 eV) are visible. At the 40th min. of sputtering, the Ta4f splitting peaks start to appear at 26.3–28.2 eV which corresponds to oxidized tantalum ions [136] at the interface. The peaks observed after 50 min. sputtering at 22.4–24 eV are due to the tantalum nitride bottom electrode [136].

In addition to sputtering XPS, a cross-sectional TEM image was obtained from $SrTiO_3$/TaN stack as seen in Fig. 4.41. As different contrasts represent different materials in the TEM images, an interfacial layer with a thickness of about 10 nm

between $SrTiO_3$ and TaN layers is also confirmed by this technique. The interfacial layer is attributed to the origin of the reduced k-value (~30) of $SrTiO_3$ [137].

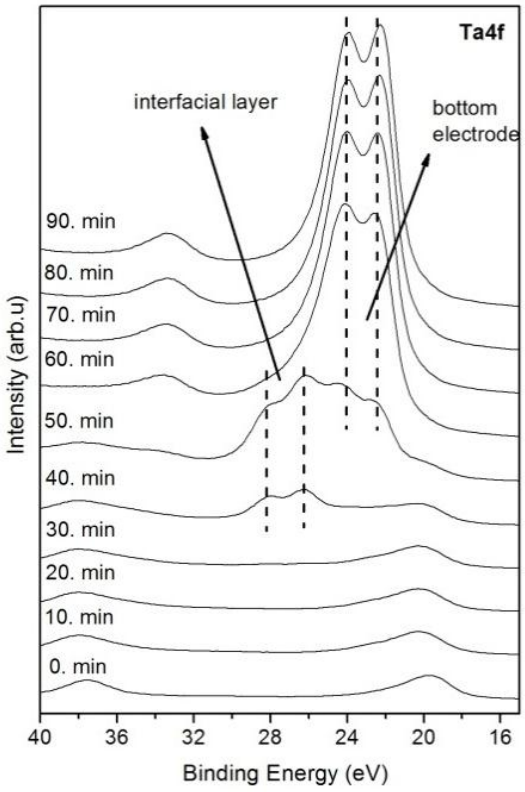

Fig. 4.40 XPS spectra in Ta4f transition region obtained on 30 nm Sr-Ti-O films deposited with 2:1 precursors injection ratio on TaN bottom electrode.

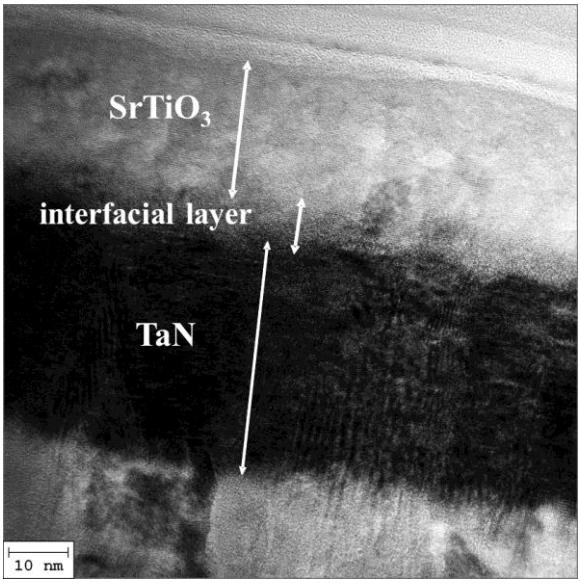

Fig. 4.41 Cross-sectional TEM image obtained on $SrTiO_3$ films deposited with 2:1 precursors injection ratio on TaN bottom electrode.

The leakage characteristic of the MIM stack (with single $SrTiO_3$ deposited with 2:1) is seen in Fig. 4.42. It is seen that very high leakage current values exist especially at bias voltages higher than 1 V, as expected from a crystal $SrTiO_3$ dielectric. In fact, it could exhibit even worse values in terms of leakage but in this case we have seen the positive effect of interfacial layer formation. The higher band gap interfacial layer helped to lower leakage current compared to the one without an interface layer.

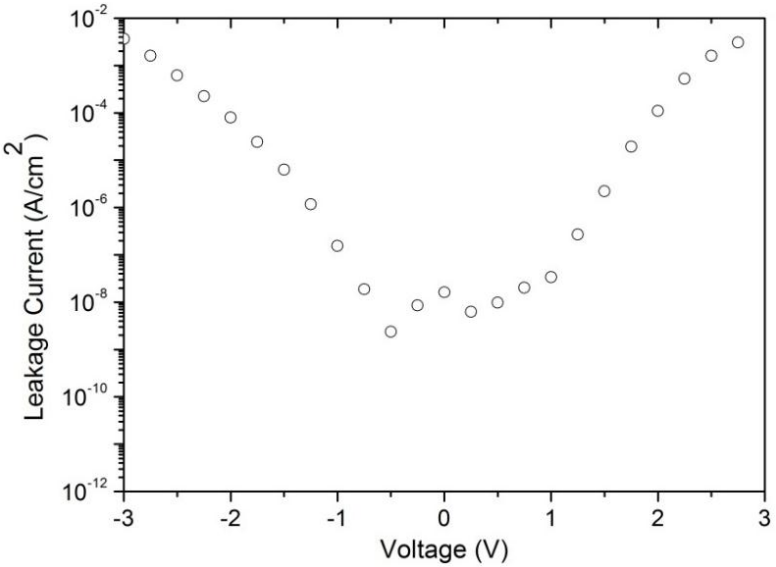

Fig. 4.42 Leakage current density vs. bias voltage on Au/$SrTiO_3$/TaN MIM capacitor.

Nevertheless, $SrTiO_3$ is optimized in terms of injection ratio of the precursors in order to reach the right composition. Further enhancement at the interface region between dielectric and electrode layer is expected by adding Al_2O_3 dielectric layers to the MIM stack. Al_2O_3 layers are added into the MIM stack using a sandwich configuration as schematically shown in Fig. 4.43. As the best k value was obtained using the 2:1 injection ratio of the precursors, $SrTiO_3$ was deposited by ALD technique using the same ratio. In order to optimize the dielectric stack, 50 nm

$SrTiO_3$ layers were combined with two different thicknesses of 2 and 4 nm of Al_2O_3 in the MIM capacitor stacks.

After annealing the stacks at 600 °C with the aim of crystallization of $SrTiO_3$, XRD measurements were performed to understand the microstructure of the layers. Fig. 4.44 shows that the XRD pattern obtained on a sample with 4 nm Al_2O_3 (shown as black line) exhibited no diffraction peaks for both $SrTiO_3$, and Al_2O_3 layers, indicating they both have an amorphous structure after annealing at 600 °C. The crystallization of $SrTiO_3$ was prevented at this temperature by the additional Al_2O_3 layers in the stack. Therefore, further annealing was applied to the sample at 700 °C. At this temperature crystallization in $SrTiO_3$ layer is slightly visible as the corresponding diffraction peak at 32.5 ° appeared as shown with a red line in the XRD spectra. However, the obvious shifting and lower intensity of TaN 111 peak indicates a degradation on TaN bottom electrode at 700 °C.

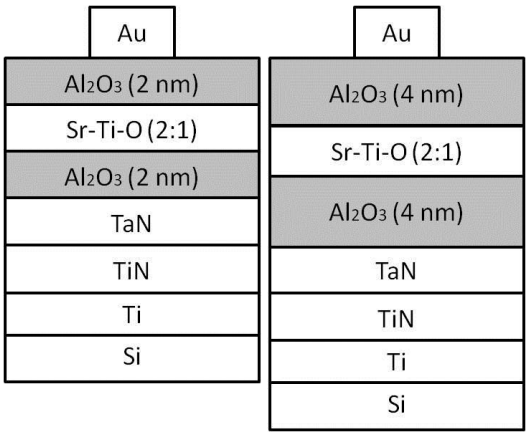

Fig. 4.43 Schematic view of the samples prepared by sandwiched multilayer dielectric coonfiguration of $Al_2O_3/SrTiO_3/Al_2O_3$ on TaN electrode for two different thickness of Al_2O_3: 2 and 4 nm.

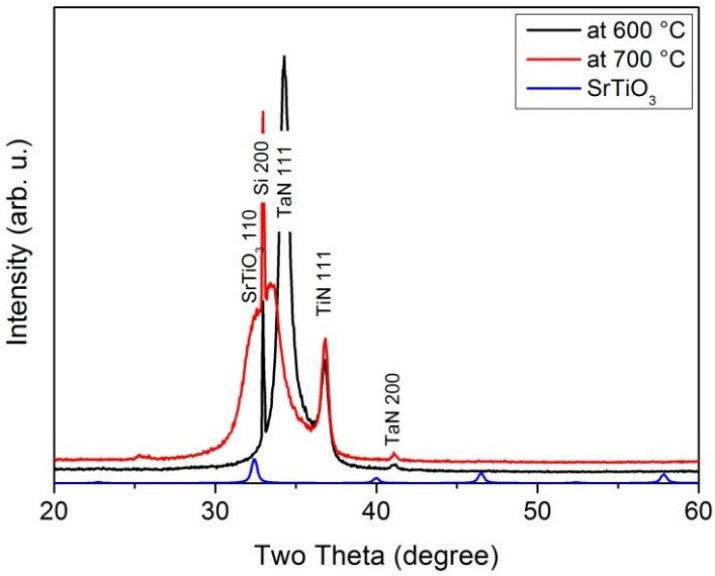

Fig. 4.44 XRD patterns of multilayer dielectric MIM capacitor of Au/Al_2O_3(4nm)/ $SrTiO_3$/ Al_2O_3(4nm)/ TaN annealed at 600 °C and 700 °C. (on the bottom of the figure blue line refers to powder $SrTiO_3$ reference XRD data)

The capacitance density measurements and the extracted k values of these multilayer dielectric MIM stacks are seen in Fig. 4.45. The calculated effective k values also confirm the amorphous structure of $SrTiO_3$ after annealing at 600 °C and were found as 14 and 10 for the sample with 2 and 4 nm additional Al_2O_3 layers, respectively. Higher annealing temperature (700 °C) increased the k value from 10 to 22 for the sample with additional 4 nm Al_2O_3 layers, but it is still too low. This can be the reason of partial crystallization in the $SrTiO_3$ dielectric film sandwiched between amorphous Al_2O_3 layers.

In terms of leakage characteristics, the sample with 2 nm Al_2O_3 layers has a leakage current of around ~10^{-5} A/cm^2 while the sample with 4 nm Al_2O_3 layers has a leakage of around ~10^{-7} A/cm^2 at 3 V bias voltages as shown in Fig. 4.46. These results confirm the trend that sandwiched type configuration of the dielectrics works. Since for the both cases (2 and 4 nm Al_2O_3) $SrTiO_3$ remained in amorphous state, it can be proved that minimum 4 nm additional Al_2O_3 layers are needed in order to

have low leakage current values through the MIM stack. The increment of leakage current of a few order of magnitude is also visible for the sample with 4 nm Al_2O_3 annealed at 700 °C due to increasing crystallinity as already proved by XRD measurements.

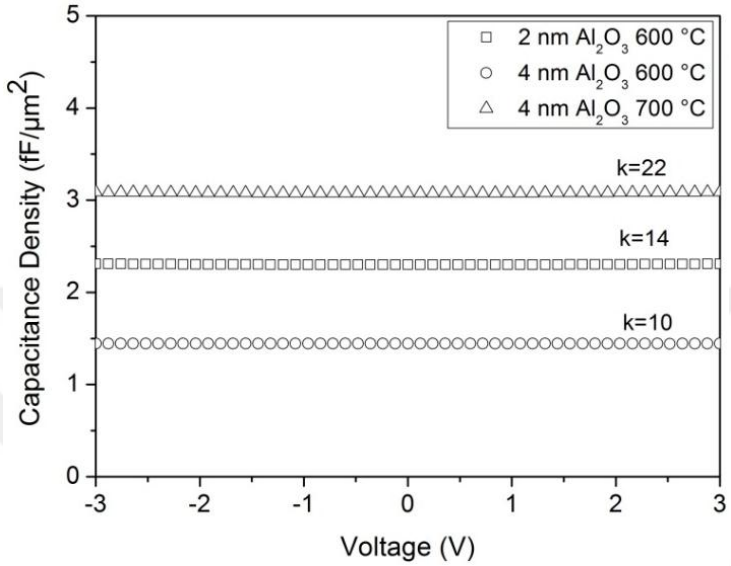

Fig. 4.45 C-V measurements and extracted k values on the samples of Al_2O_3(2 nm)/$SrTiO_3$/Al_2O_3(2 nm) annealed at 600 °C and on Al_2O_3(4 nm)/$SrTiO_3$/Al_2O_3(4 nm) annealed at 600 °C and 700 °C.

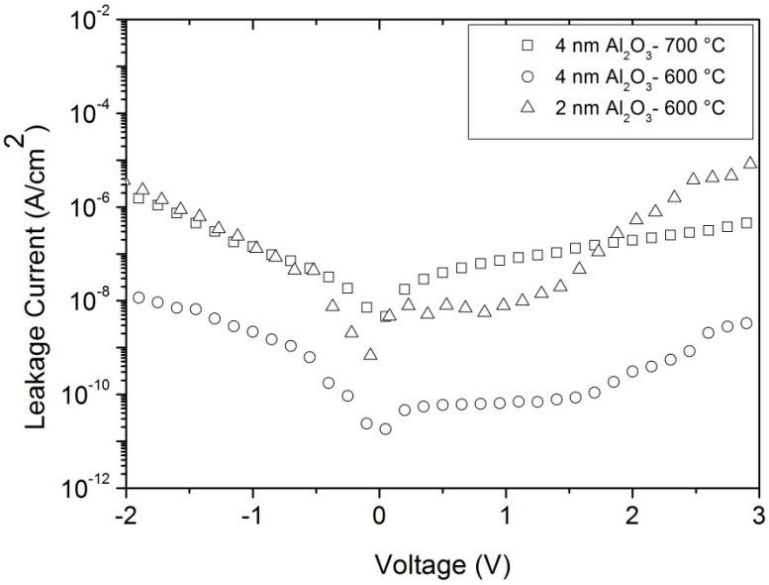

Fig. 4.46 Leakage current densities on the samples of Al_2O_3(2 nm)/$SrTiO_3$/Al_2O_3(2 nm) annealed at 600 °C and Al_2O_3(4 nm)/$SrTiO_3$/Al_2O_3(4 nm) annealed at 600 °C and 700 °C.

On TiN bottom electrode

Due to the interface layer formation between $SrTiO_3$ and TaN bottom electrode, the second part of this chapter covers the investigation of $SrTiO_3$-Al_2O_3 multilayer dielectric on TiN bottom electrode. Before the investigation of the effect of additional Al_2O_3 layer, a single $SrTiO_3$ layer was deposited on TiN electrode as a reference MIM capacitor. Fig. 4.47 shows the capacitance density measurement result on the sample which was annealed at 600 °C. It is seen that it has a k value of 100 for 50 nm thickness of $SrTiO_3$. However, the leakage current shown in Fig. 4.48 is in the range of 10^{-2} A/cm^2 at 3 V due to crystalline structure of $SrTiO_3$ as proved by XRD technique (not shown here).

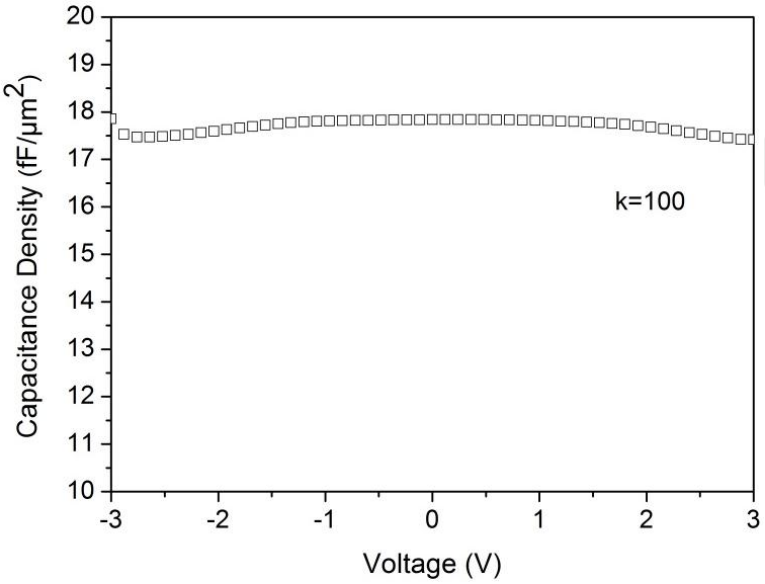

Fig. 4.47 Capacitance density vs. voltage with the extracted k value on Au/$SrTiO_3$/TiN MIM capacitor.

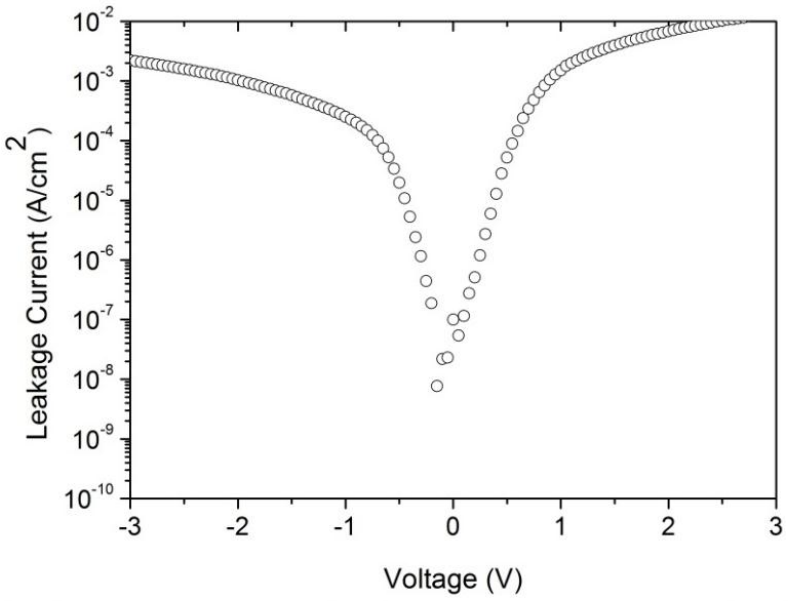

Fig. 4.48 Leakage current density vs. voltage on Au/$SrTiO_3$/TiN MIM capacitor.

The higher k value (~100) of $SrTiO_3$ compared to the case with TaN electrode is attributed to the good interface properties between $SrTiO_3$ and TiN bottom electrode. Fig. 4.49 presents a cross-sectional TEM image of a $SrTiO_3$ (30 nm)/TiN sample. The crystalline structure of $SrTiO_3$ is clearly seen in the image. It also exhibits a very sharp interface between $SrTiO_3$ and TiN and no interfacial layer formation.

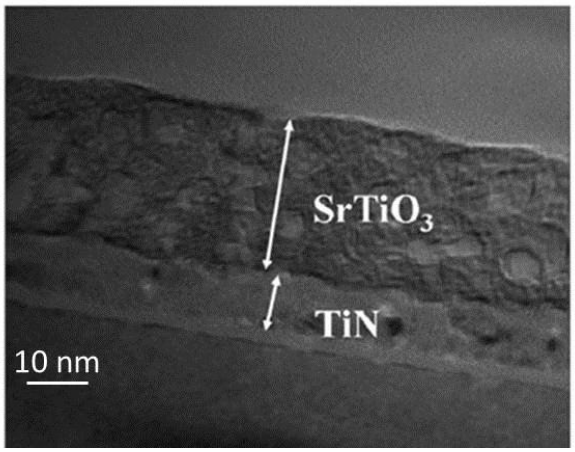

Fig. 4.49 Cross-sectional TEM image on $SrTiO_3$/TiN.

In order to investigate the sandwiched configuration of 50 nm of $SrTiO_3$ with additional Al_2O_3 layers on TiN bottom electrode, two different thickness of 2 and 4 nm for Al_2O_3 layer were used in the MIM stacks as shown schematically in Fig. 4.50. For the crystallization of $SrTiO_3$, an annealing process was applied at 600 °C.

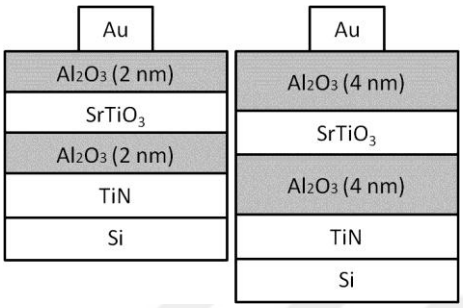

Fig. 4.50 Schematic view of the samples prepared by sandwiched multilayer dielectric coonfiguration of $Al_2O_3/SrTiO_3/Al_2O_3$ on TiN electrode for two different thickness of Al_2O_3: 2 and 4 nm.

In order to investigate whether the $SrTiO_3$ dielectric is crystallized, XRD measurements were performed on the sandwiched stacks. However, as seen in Fig. 4.51, no diffraction peaks have been observed except the peak belonging to Si substrate. This shows that $SrTiO_3$ in the sandwiched configuration remained in its amorphous state after annealing process at 600 °C.

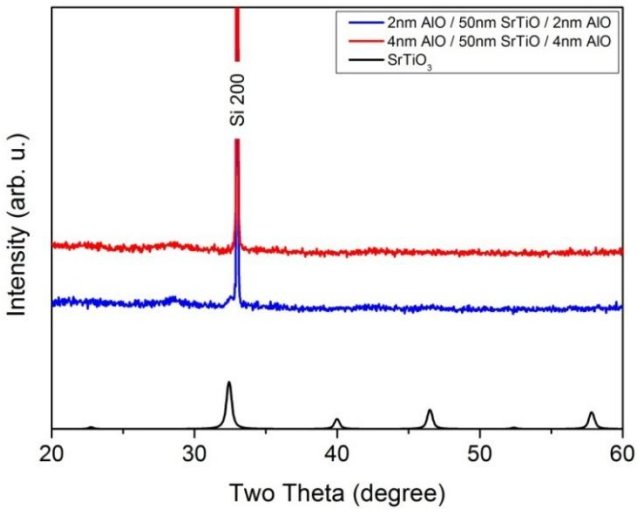

Fig. 4.51 XRD pattern of multilayer dielectric MIM capacitors of $Au/Al_2O_3/SrTiO_3/Al_2O_3/TiN$ with different thickness of Al_2O_3:2 and 4 nm.

The capacitance density measurement results are also in agreement with the amorphous structure of $SrTiO_3$ in the MIM stacks. As seen in Fig. 4.52, the extracted k values are 10 and 11 for the samples with 2 and 4 nm additional Al_2O_3 layers, respectively.

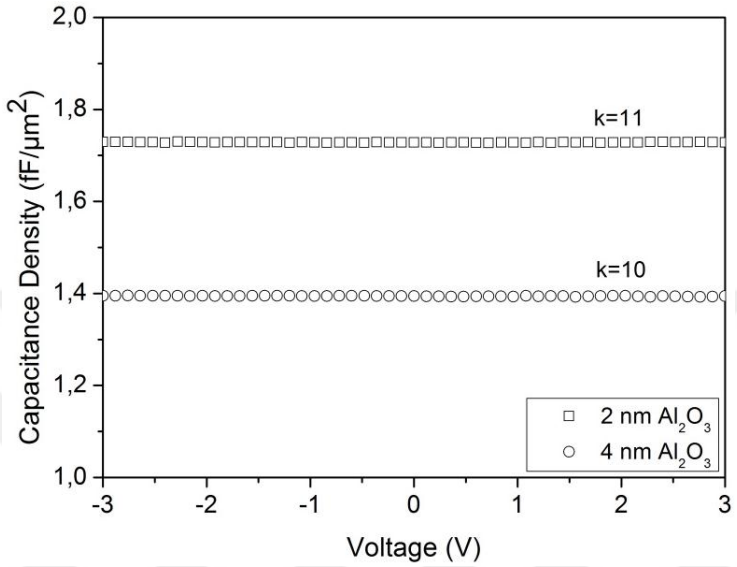

Fig. 4.52 C-V measurements with extracted k values on multilayer dielectric MIM capacitor of $Au/Al_2O_3/SrTiO_3/Al_2O_3/TiN$ with different thickness of Al_2O_3: 2 and 4 nm.

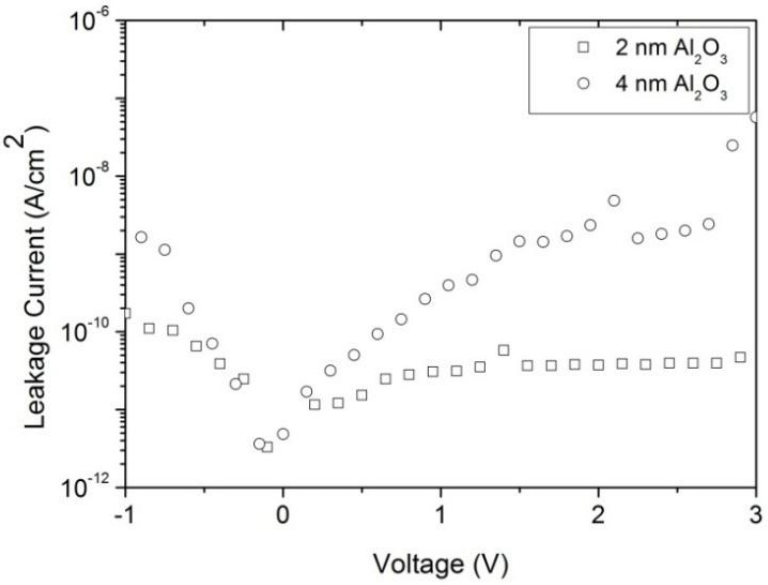

Fig. 4.53 Leakage current density measurements on multilayer dielectric MIM capacitor of $Au/Al_2O_3/SrTiO_3/Al_2O_3/TiN$ with different thickness of Al_2O_3: 2 and 4 nm.

The leakage current density measurement exhibits very good values in the range of 10^{-10} A/cm^2 especially on the sample with 4 nm additional Al_2O_3 layers (Fig. 4.53). However, this good leakage cannot be only attributed the effect of additional Al_2O_3 layer in MIM stack. The amorphous structure of $SrTiO_3$ is also responsible.

In order to further investigate the crystallization behavior dependence of $SrTiO_3$ on the sequences of dielectric layers in MIM structures, different stacks of dielectrics are deposited as seen in Fig. 4.54, schematically. Al_2O_3 layers were deposited for two different thicknesses (2 and 4 nm) once on top of bottom TiN electrode and also on of 50 nm $SrTiO_3$ dielectric layer.

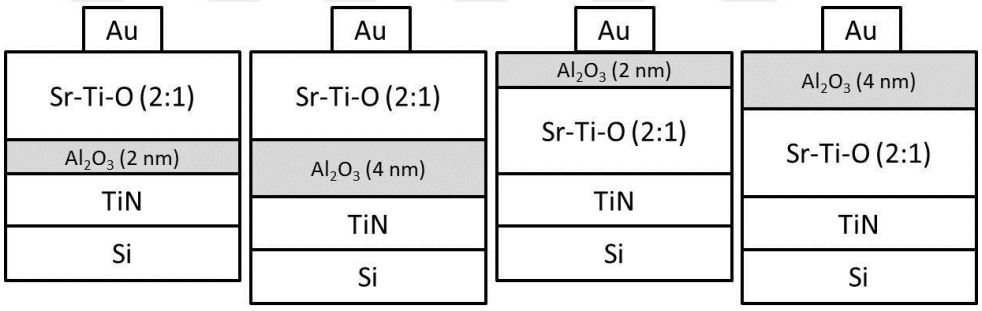

Fig. 4.54 Schematic view of the stacked dielectrics MIM capacitors for different sequences of dielectric layers and for different thickness of Al_2O_3 (2 and 4 nm) on TiN electrode.

After annealing at 600 °C, XRD measurement results on these samples are shown in Fig. 4.55. It has been proven that in all the dielectric stacks the $SrTiO_3$ is crystallized independently on the sequence of the dielectric layers. In addition, it is observed that the crystallization degree in $SrTiO_3$ is slightly higher for the case of $SrTiO_3$ right deposited on TiN, as the corresponding diffraction peaks are observed to be more intensive (Fig. 4.55, yellow and blue lines).

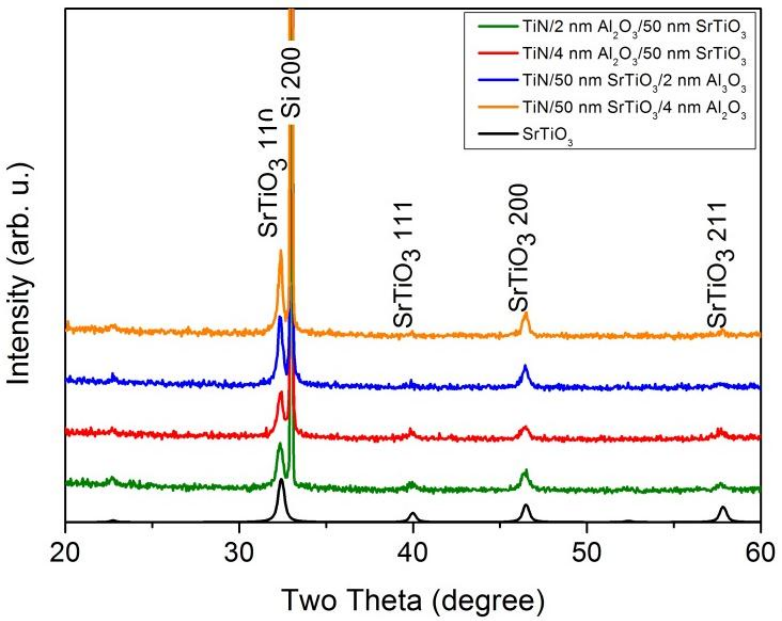

Fig. 4.55 XRD pattern on the stacked dielectric MIM capacitors with different deposition sequences for dielectrics and for different thickness of Al_2O_3 layers.

By considering this tendency of increasing crystallinity of the samples grown in the order of Al_2O_3/$SrTiO_3$/TiN, the next set of samples for sandwiched configuration is prepared in the opposite way. The Al_2O_3 layer is sandwiched between 25 nm thick $SrTiO_3$ layers for two different thicknesses of 4 and 6 nm as schematically seen in Fig. 4.56.

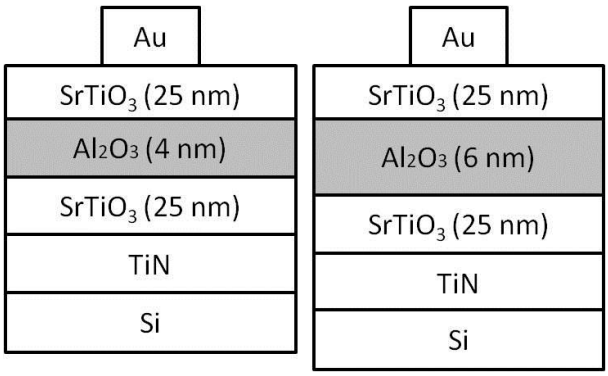

Fig. 4.56 Schematic view of the sample multilayer dielectric MIM capacitors of Au/$SrTiO_3$/Al_2O_3/ $SrTiO_3$/TiN electrode for different thickness of Al_2O_3 layer: 4 and 6nm.

After annealing at 600 °C, as seen in Fig. 4.57, XRD measurements on these samples show the crystalline structure of $SrTiO_3$ layers. However, it is not possible to confirm if both $SrTiO_3$ layers are crystalline using the XRD technique.

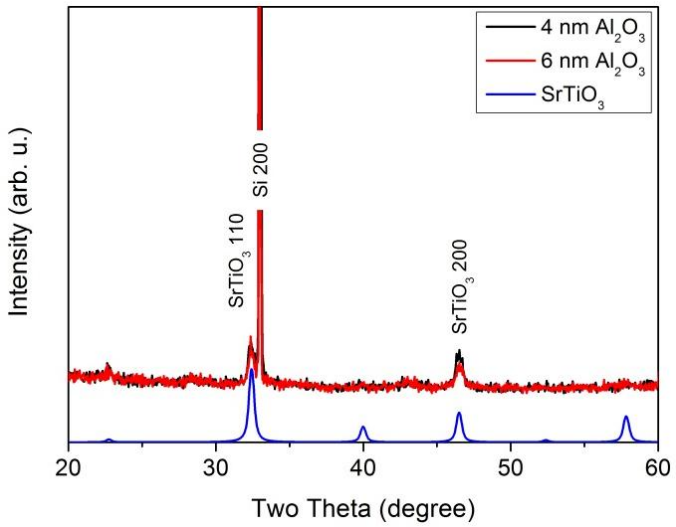

Fig. 4.57 XRD patterns of the multilayer dielectric stack of $SrTiO_3/Al_2O_3/SrTiO_3$ on TiN electrode for different thickness of Al_2O_3 layer: 4 and 6nm.

Fig. 4.58 a) and b) show high resolution TEM images obtained from the samples with 4 and 6 nm additional Al_2O_3 layer, respectively. Indeed, as seen in the images, there is a difference in terms of microstructure of the bottom and top $SrTiO_3$ layers. Especially for the sample with 6 nm Al_2O_3 layers, the top $SrTiO_3$ layer looks crystalline while the bottom $SrTiO_3$ layer is more amorphous.

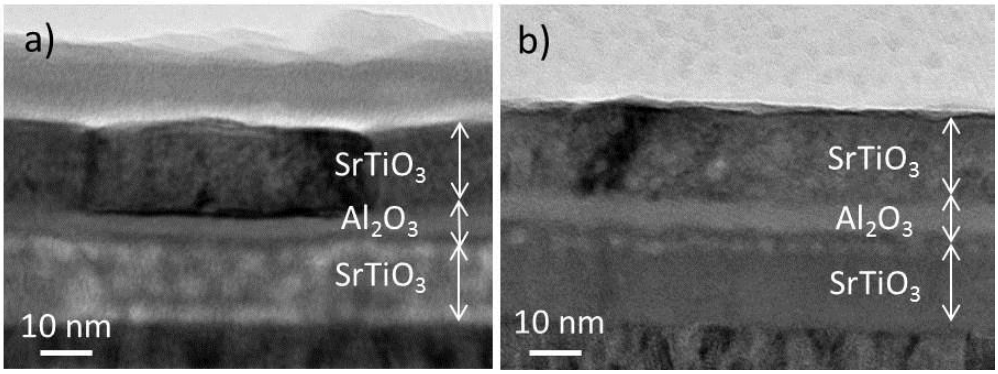

Fig. 4.58 Cross-sectional TEM images of the multilayer dielectric stack of $SrTiO_3/Al_2O_3/SrTiO_3$ on TiN electrode for different thickness of Al_2O_3 layer: a) 4 nm, b) 6 nm.

In order to have both $SrTiO_3$ layers in crystalline state, a two-step annealing process at 600 °C was applied. Firstly, bottom $SrTiO_3$ was deposited and then the annealing process was applied. After the Al_2O_3 and top $SrTiO_3$ deposition one more annealing process was applied to the samples. In order to observe the microstructure of bottom $SrTiO_3$, XRD measurements were performed after each annealing process. The corresponding XRD measurement results of the sample with 4 and 6 nm Al_2O_3 layers are shown in Fig. 4.59 a) and b), respectively. It can be seen that bottom $SrTiO_3$ is successfully crystallized by the two-step annealing approach. However the 110 orientation is not observed for the bottom $SrTiO_3$ layer.

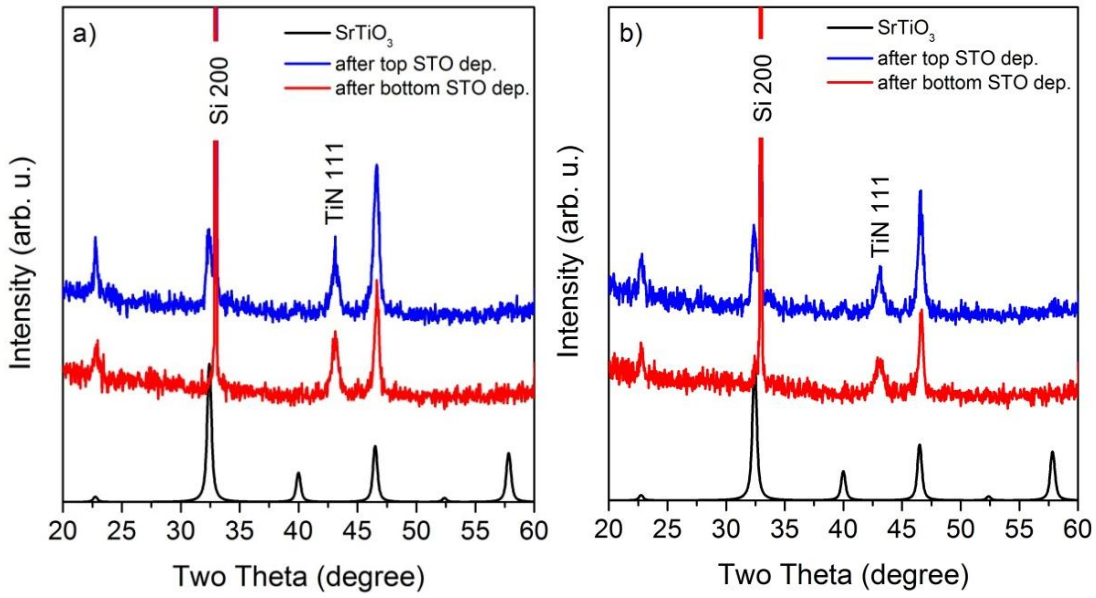

Fig. 4.59 XRD patterns of the multilayer dielectric stack of $SrTiO_3/Al_2O_3/SrTiO_3$ on TiN after bottom and top $SrTiO_3$ deposition a) 4 nm Al_2O_3 in the stack b) 6 nm Al_2O_3 in the stack.

The C-V measurement results on the two step annealed samples show that the k values are improved to the values of 33 for the sample with 4 nm Al_2O_3 layers, owing to the crystalline structure of $SrTiO_3$ layers as seen in Fig. 4.60. However, it is still far from the value of a fully crystalline $SrTiO_3$ dielectric film. In addition a very

promising low leakage current of 1.10^{-8} A/cm^2 is obtained at a 3 V bias voltage for both of the samples as shown in Fig. 4.61. Such a low leakage is attributed to the intermediate amorphous Al_2O_3 layer which terminates the continuous crystal growth of $SrTiO_3$, thereby eliminating the grain boundary channels extending from one electrode to the other, which is responsible for the reduced conductivity [138]. In addition, the ALD technique can achieve stoichiometric dielectric films [139] due to the saturative chemisorbtion of sequential cycles of precursor's vapors which likely enhance dielectric performance.

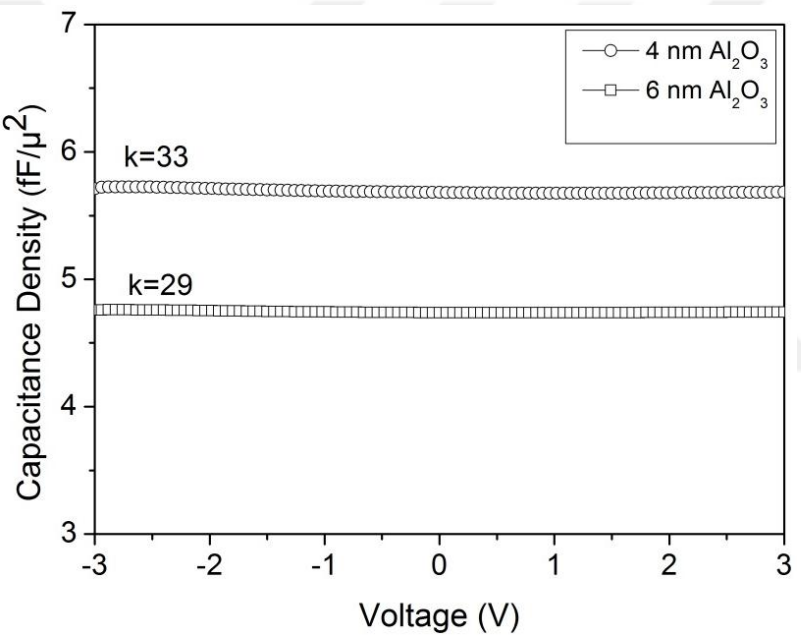

Fig. 4.60 C-V measurements with extracted k values on multilayer dielectric MIM capacitor of Au/$SrTiO_3$/Al_2O_3/$SrTiO_3$/TiN with different thickness of Al_2O_3 layers: 4 and 6nm.

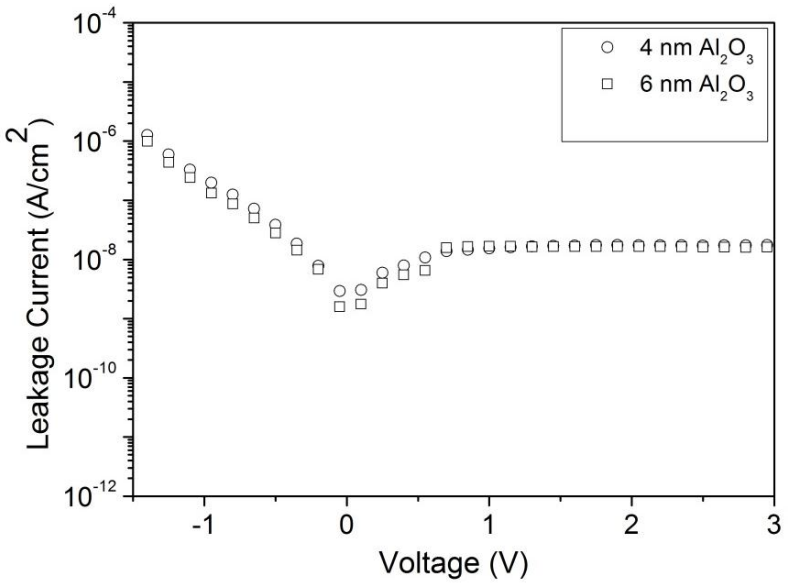

Fig. 4.61 Leakage current density measurements on multilayer dielectric MIM capacitor of Au/$SrTiO_3$/Al_2O_3/$SrTiO_3$/TiN with different thickness of Al_2O_3 layers: 4 and 6nm

In order to investigate the interfacial properties between the layers, a TEM image was obtained for the sample which includes 6 nm Al_2O_3 layer between $SrTiO_3$ dielectric layers (Fig. 4.62). Indeed, the high magnification TEM image on sample with 6nm Al_2O_3 shows that there is an interfacial layer formation between the bottom $SrTiO_3$ and Al_2O_3 layers as the contrast is observed to be different from the rest Al_2O_3 layer.

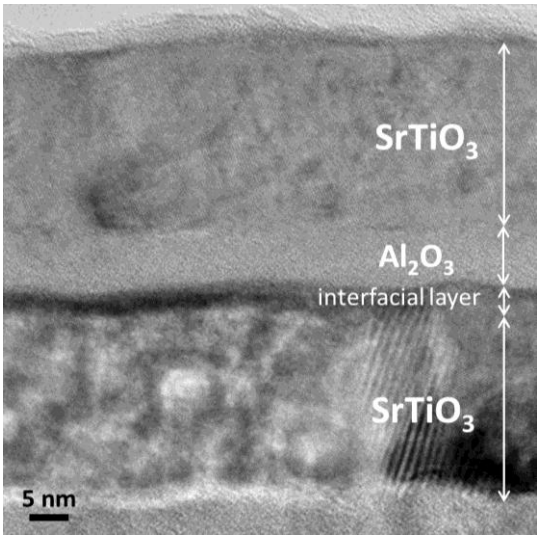

Fig. 4.62 Cross-sectional TEM image on $SrTiO_3$/Al_2O_3(6nm)/$SrTiO_3$/TiN stack.

Analysis of the diffusion of atoms between the layers after the annealing process was studied by sputtering ToF-SIMS technique. Fig. 4.63 shows the depth profile of the representative positive ions for each layer of the whole MIM stack such as Sr^+, Al_2^+, Ti^+, and SiO^+. All the profiles of the investigated fragments are obtained to be as expected through the depth of the stack, except SiO^+. It is clearly seen that there is contribution of SiO^+ at the interface region between Al_2O_3 and bottom $SrTiO_3$ layer. As the Al_2^+ and SiO^+ intensities get lower simultaneously, this interface can be attributed likely to be composed from Al-O-Si.

For better understanding the composition and chemical state of the elements at this interface region, the sputtering XPS method was utilized. Corresponding spectra were analyzed after 70 min of Ar sputtering which corresponds to the depth for the interfacial layer formation.

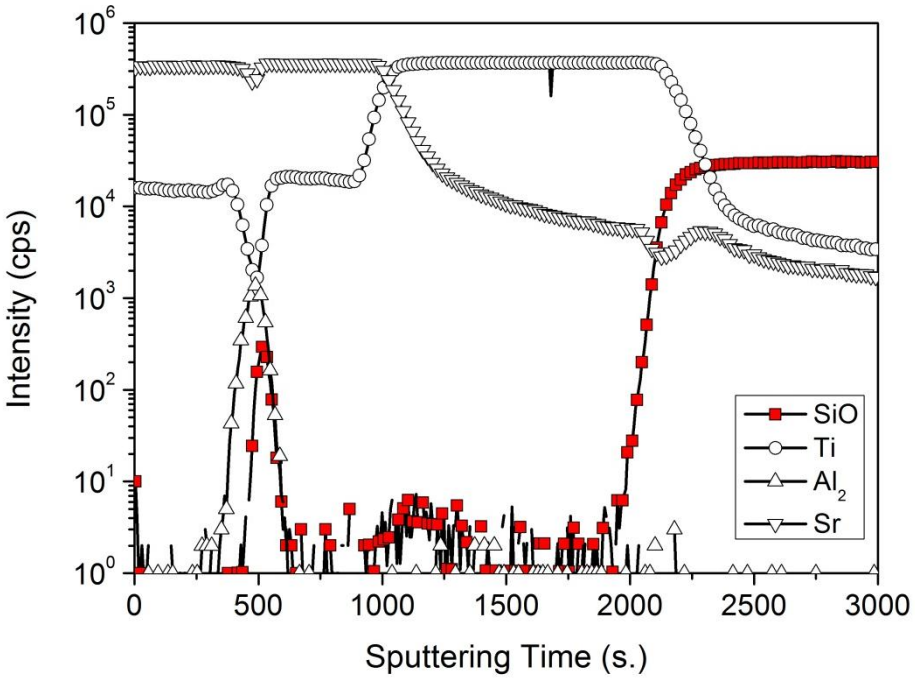

Fig. 4.63 ToF-SIMS depth profile on $SrTiO_3/Al_2O_3$(6nm)/$SrTiO_3$/TiN stack.

As the chemical shift for Al in Al-O (i.e. Al_2O_3) and (Al-O)-Si coordination is negligibly small, Al2p binding energy was used as an internal reference for charging and set to 74.5 eV as shown in Fig. 4.64 a). The corresponding Si2p peak was observed to be centered at 102.5 eV as shown in Fig. 4.64 b). This peak does not correspond exactly to a fully oxidized state of Si because the chemical shift to metallic silicon is only a 3.1 eV which is much smaller than that of Si^{+4}. The general binding energy shift between metallic silicon and SiO_2 is 4 eV [140]. The lower binding energy of Si2p compared to the peak for Si-oxide at 103.5 eV indicates that Si is bonded to an atom that has a lower electronegativity than oxygen, namely, aluminum. Thus, the peaks can be attributed to either aluminum silicate, some other Al-O-Si compound or SiO_2-Al_2O_3 mixture [141]. In addition it can be concluded that the interfacial layer of silicate is amorphous at 600 °C as there is no observed peak visible in the XRD pattern. In reference [142], it was also observed that this interface layer remains in amorphous state up to 600 °C.

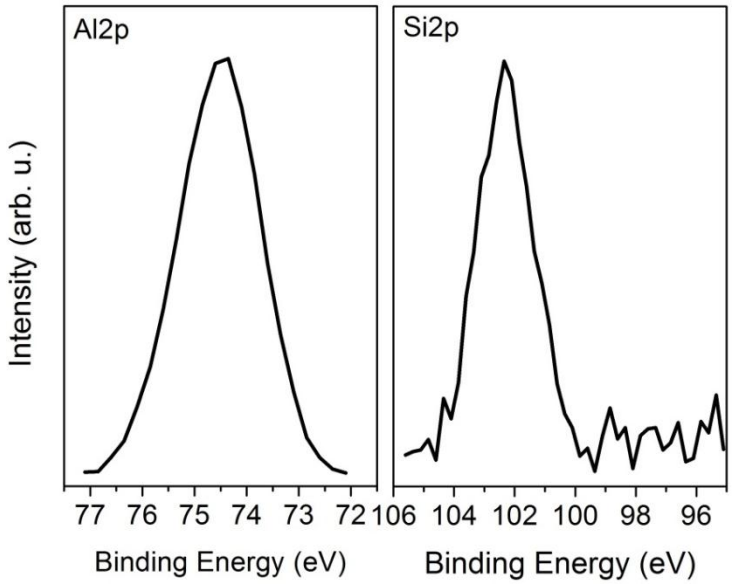

Fig. 4.64 XPS spectra of Al2p and Si2p at the interface region between Al_2O_3 and bottom $SrTiO_3$ in $SrTiO_3/Al_2O_3$(6nm)/$SrTiO_3$/TiN stack: gray line indicates measurement while black line is fitting result.

4.2.2.3 Summary & Conclusions

Single $SrTiO_3$ dielectric on TaN bottom electrode has been deposited using different precursor injection ratios. According to the extracted k values from C-V measurements of the dielectric films, the best ratio has been found to be 2:1, and the corresponding k value of the dielectric was ~30. As this k value is lower than the expected one (~100) for a crystalline $SrTiO_3$ dielectric, interface analysis has been done. According to sputtering XPS and a cross- sectional TEM image of the corresponding stack, it has been proven that ~10 nm of interfacial layer of oxidized tantalum is formed. The low effective k value is attributed to this low k value interface formation. For the combination of dielectrics $SrTiO_3$ and Al_2O_3 on TaN electrode using sandwiched configuration exhibited that $SrTiO_3$ was not able to crystallize when it is deposited between two amorphous Al_2O_3 layers. Therefore, the k value of the sandwiched configuration of multilayer dielectric MIM capacitor did not show high values.

In the second part of the chapter, TiN bottom electrode was used. Single $SrTiO_3$ MIM capacitor using TiN bottom electrode showed an excellent k value of ~95. This has been correlated with the sharp interface between $SrTiO_3$ and TiN electrode. However, the leakage current of this single dielectric MIM stack showed very high values. The sandwiched configuration of $SrTiO_3$ between Al_2O_3 layers on TiN bottom electrode was faced with the same problem of non-crystallization by annealing at 600 °C. Therefore another set has been prepared. It has been proven that the grade of crystallization of $SrTiO_3$ is higher when it is deposited right on top of crystalline TiN electrode, instead of on top of amorphous Al_2O_3 layer. Therefore, the

stacking sequence of $SrTiO_3/Al_2O_3/SrTiO_3$ has been investigated. Indeed, this configuration proved the crystallization of $SrTiO_3$, if two step annealing is applied. Although very low leakage current of 1.10^{-8} A/cm^2 has been achieved, k value was around 33 for this configuration of dielectrics. By interfacial analysis, it has been observed that the bottom interface between Al_2O_3 and bottom $SrTiO_3$ layer degraded after the annealing steps. Si has been observed to be diffused out from the substrate and segregated between Al_2O_3 and bottom $SrTiO_3$ layer. According to XPS analysis, an Al-O-Si compound formation is observed. As the dielectric films were deposited and annealed by repeated heating cycles, the lower $Al_2O_3/SrTiO_3$ interface was subjected to more heating cycles than the upper interface. This has resulted in the observed degradation in the bottom interface.

5 Summary and Future Works

In this thesis, alternative dielectrics such as Ce-Al-O, Sr-Ta-O, $SrTiO_3$ are investigated for future MIM capacitor applications. The properties of MIM capacitors with these dielectrics have been investigated systematically, including the electrical and physical characteristics. Moreover, the influence of the post-deposition annealing treatment and the metal electrodes on the performance of MIM capacitors has been studied. As single dielectric MIM capacitor mostly faces tradeoffs between capacitance density and leakage current, the main properties of the MIM stacks are also optimized using multilayer dielectric configurations. $SrTiO_3$ was used as the source of high k value in the multilayer dielectric MIM capacitors. Its combination with Al_2O_3 and SrTaO was investigated as these dielectric materials possess rather high band gap values and amorphous structures at the crystallization temperature of $SrTiO_3$. The important findings and conclusions obtained in this study can be summarized as following:

1. Ce-Al-O dielectric films deposited using pulsed injection MOCVD on TiN electrode were investigated for the first time for MIM capacitor application. Several injection ratios of precursors were used for deposition of the dielectric layer. Analysis on these samples showed that as-deposited Al rich Ce-Al-O films were amorphous and exhibited a k value of 20 with leakage current densities of about 10^{-4} A/cm^2 at 2 V. On the other hand, as-deposited cerium rich Ce-Al-O films were found to have crystalline CeO_2 phase separation and had much lower k values with higher leakage current densities than aluminum rich dielectric films. Moreover, their electrical and physical properties were investigated after high temperature annealing at 600 °C and

850 °C. It was shown that the annealing process did not lead to $CeAlO_3$ formation and degraded the electrode and dielectric layers for almost for all of the samples. Only, the dielectric deposited with an injection ratio of Ce:Al=1:1 was observed to result in crystalline structure in the form of $CeAlO_3$ at 850 °C. By the crystallization of the dielectric film the k value was increased from 11 to 60. However, the structures were partially degraded at high annealing temperatures and exhibited much higher leakage current densities. In summary, CeAlO dielectric was shown to be a non-convenient candidate for the application of MIM capacitors.

2. A MIM capacitor with SrTaO dielectric deposited using MOCVD on TaN electrode was studied in terms of its electrical and physical properties. The influence of annealing on the electrical and structural properties of the MIM capacitors was studied. XRD measurement showed that as-deposited SrTaO dielectric has an amorphous microstructure. Composition of the dielectric was proved to be $Sr_2Ta_2O_7$, according to the chemical states of the constituent elements measured by XPS. The electrical response of the as-deposited case of MIM structure showed a k value of around 18 accompanied with a leakage current of around 10^{-8} A/cm^2 at 2 V. By thermal treatment of the single SrTaO MIM capacitor structure, the dielectric film was observed to be crystallized at 700 °C. XRD measurements exhibited that the crystallization in dielectric occurred in the form of $SrTaO_2N$. N diffused into the dielectric layer due to the degradation of TaN bottom electrode at high annealing temperatures as proved by Tof-SIMS measurement. The crystallization in the dielectric layer improved the dielectric constant of the film from 18 to 50. However, the annealing at 700 °C and 900 °C caused higher leakage current.

3. A combination of $SrTiO_3$-SrTaO was studied for multilayer dielectric MIM capacitor structure. In order to see the effect of SrTaO, single $SrTiO_3$ MIM capacitor was used as reference sample. Although the single $SrTiO_3$ (50 nm) MIM capacitor gave an excellent high k value of ~95, a very high leakage current was obtained (~10^{-4} A/cm^2) for the MIM capacitor application. The additional SrTaO layer on top of the TaN bottom electrode obviously improved the leakage current while keeping high capacitance density. The thickness of SrTaO was optimized in the multilayer dielectric MIM capacitor as 6 nm with a very promising leakage current and effective k value of 8.10^{-8} A/cm^2 and 81, respectively. Additionally, the deposition sequence of dielectric layers of SrTaO and $SrTiO_3$ were investigated in terms of main MIM capacitor properties. 6 nm SrTaO was also deposited in the opposite way, between top Au electrode and $SrTiO_3$. The results proved the significance of the sequences of dielectrics in multilayer dielectric MIM capacitor. The capacitance density was about 2 fF/μm^2 higher for the case of bottom deposition of SrTaO than that of top deposition. The reason for this difference was attributed to a degraded interface between $SrTiO_3$ and TaN electrode compared to that between SrTaO and TaN electrode. TEM investigation of the sample SrTaO/$SrTiO_3$/TaN showed an approximately 1-2 nm interface layer formation between the $SrTiO_3$ and the TaN bottom electrode. From the leakage point of view, it was observed that SrTaO deposition on $SrTiO_3$ in the dielectric stack showed one order of magnitude better leakage current values at bias voltages higher than 2 V.

4. Single $SrTiO_3$ dielectric on TaN bottom electrode was deposited using different precursor injection ratio. According to the extracted k values from C-V measurements of the dielectric films, the best ratio was found to be 2:1, and the

corresponding k value was ~30. As this k value is lower than the expected one (~100) for a crystalline $SrTiO_3$ dielectric, interface analysis was performed. According to sputtering XPS and cross-sectional TEM images of the corresponding stack, it was proved that about 10 nm of interfacial layer of oxidized tantalum was formed. For the combination of dielectrics of $SrTiO_3$ and Al_2O_3 on TaN electrode using a sandwiched configuration it was shown that $SrTiO_3$ was not able to crystallize when it was deposited between two amorphous Al_2O_3 layers. Therefore, the k value of the sandwiched configuration of multilayer dielectric MIM capacitor was very low. If, TiN bottom electrode was used, single $SrTiO_3$ MIM capacitor showed excellent k value of ~95. This was correlated with the sharp interface between $SrTiO_3$ and TiN electrode. However, the leakage current of this single dielectric MIM stack showed very high values. The sandwiched configuration of $SrTiO_3$ between Al_2O_3 layers on TiN bottom electrode faced the same problem of non-crystallization by annealing at 600 °C. Therefore another set of samples were prepared. It was proved that $SrTiO_3$ was becoming more crystallized when it is deposited right on top of crystalline TiN electrode, instead of deposition on top of an amorphous Al_2O_3 layer. Therefore, $SrTiO_3/Al_2O_3/SrTiO_3$ was investigated. Indeed, this configuration proved the crystallization of $SrTiO_3$, if two step annealing was applied. Although very nice leakage current of 1.10^{-8} A/cm^2 was achieved, k value was around 33 in this configuration. By interfacial analysis, it was observed that the bottom interface between Al_2O_3 and bottom $SrTiO_3$ degraded after the annealing step. Si was observed to be diffused out from the substrate and segregated between Al_2O_3 and bottom $SrTiO_3$. According to XPS analysis, an Al-O-Si compound formation was

confirmed. The degradation in the bottom interface was attributed to exposure of bottom interface to two annealing steps.

Fig. 5.1 summarizes the main electrical properties of all the MIM capacitors investigated in this thesis. As seen in the figure, leakage current through most of the MIM capacitors increases with increasing k value of the dielectrics. Nevertheless, multilayer dielectric MIM capacitor constituted of $SrTiO_3$ and SrTaO as dielectric, and TaN as bottom electrode material is out of this trend and exhibits high k value of around 80 accompanied with low leakage current in the range of 10^{-8} A/cm^2 as seen in the figure. This result is very promising as this kind of dielectric material is investigated for the first time for MIM capacitor application.

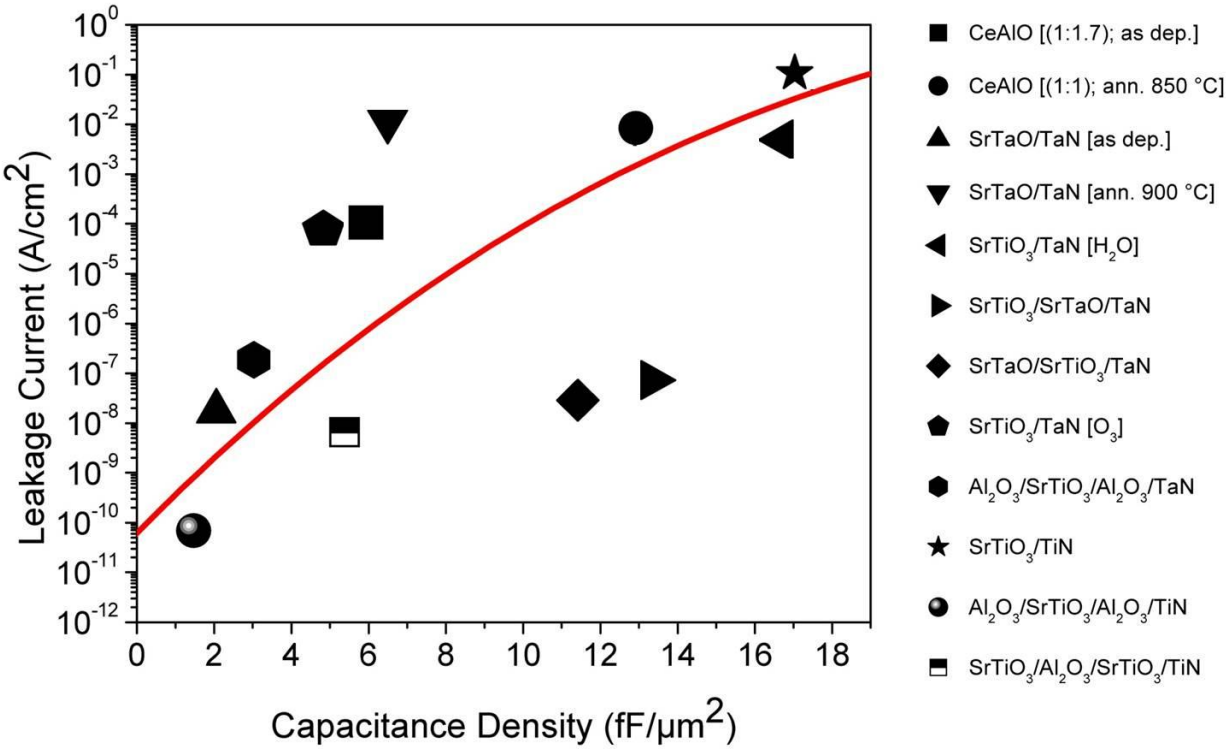

Fig. 5.1 Leakage current density vs. k value obtained from all the MIM capacitors studied in this thesis.

In order to show better comparison, Table 4 shows both the main electrical results out of these structure and 2020 ITRS requirements for MIM capacitor applications. The promising characteristics obtained for multilayer dielectric ($SrTiO_3$-SrTaO) MIM capacitor suggest that this dielectric system has a potential to be a good candidate for future MIM capacitor applications.

	Capacitance Density ($fF/\mu m^2$)	Leakage Current (A/cm^2) at 2V
ITRS for 2020	10	< 1e-8
$SrTiO_3$/SrTaO	13.5	5e-8
SrTaO/$SrTiO_3$	11.5	3e-8

Table 4. Comparison of the main properties of Au/SrTaO-SrTiO/TaN multidielectric MIM capacitor and ITRS requirements for 2020.

In conclusion, the main trade off for high k dielectrics is between high capacitance density and low leakage current. Using multilayered dielectric stacks results in very promising parameters by improving the properties between the dielectric and electrode interface. However, one should add that the integration of this potential dielectric is impossible under BEOL CMOS due to its high annealing temperature and possible cross-contamination issue. Nevertheless, as defined in the ITRS several other components are also getting complex structure for simple integration by the enormous growth of microelectronics. Although some moderately high k dielectrics are already introduced, this is only the very beginning. The available high k oxides are only applicable for the current or next technology node. In the future, significant improvements have to be made to meet the stringent demands of subsequent technology generations. We believe that through a combination of integration methods innovation and engineering skills the issues could be

successfully overcome, thereby paving the way for high k implementation into MIM capacitor.

Future Works

Further investigation on the MIM capacitor with multilayer dielectric of $SrTiO_3$-SrTaO would be interesting, as the first attempt exhibited very promising characteristics. The studies should focus on the improvement of the quality of each dielectric layer as well as interfacial properties both between dielectric/electrode and dielectric/dielectric. Nondestructive methods of hard-XPS can be utilized for interface analysis. In addition, analysis of different suitable electrode material with high work function and robust interface with this dielectric system can be studied as the bottom electrode material has a significant effect on the performance of MIM capacitor.

Due to the need for high annealing temperature processes for obtaining high k values, different annealing environments would also be interesting to analyze.

The leakage current can be decreased by using a thin amorphous Al_2O_3 layer between $SrTiO_3$ dielectric and electrode materials. However, the obtainable capacitance density could not be as high due to the prevented crystallization of $SrTiO_3$ layers by additional Al_2O_3 layers. Other deposition processes could be used in order to overcome this problem. Also, investigation of the corresponding leakage mechanism and breakdown voltage are of interest.

The preliminary Q factor tests of the fabricated MIM capacitors have been performed at low frequencies range. More accurate Q factor measurement can be done at higher frequencies. However, these kinds of high frequency tests can only be

done using test structures with special pad configurations. Therefore, test structures with a ground-signal-ground (GSG) type of pad configurations can be designed and used for characterization of Q factor of the MIM capacitors at high frequencies.

List of Abbreviations

AC- alternative current

ALD- atomic layer deposition

AMS- analog mixed signal

AVD- atomic vapor deposition

BEOL- back end of line

BiCMOS- bipolar complementary metal oxide semiconductor

CMOS- complementary metal oxide semiconductor

C-V- capacitance versus voltage

CVD- chemical vapor deposition

DC- direct current

DRAM- dynamic random access memory

IC- integrated circuits

ITRS- international technology roadmap for semiconductor

J-V- current versus voltage

MIS- metal-insulator-silicon

MIM- metal-insulator-metal

MOCVD- metal organic chemical vapor deposition

MOS- metal oxide semiconductor

MOSFET- metal oxide semiconductor field effect transistor

PECVD- plasma enhanced chemical vapor deposition

PVD- physical vapor deposition

RF- radio frequency

RFIC- radio frequency integrated circuits

RTA- rapid thermal annealing

SEM- scanning electron microscopy

SiP- system in package

SoC- system on chip

TEM- transmission electron microscopy

ToF-SIMS- time of flight secondary ion mass spectroscopy

XPS- x-ray photoelectron spectroscopy

XRD- x-ray diffractometry

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List of Publications and Conferences

Journals

1) “Investigations of thermal annealing effects on electrical and structural properties of MIM capacitor with SrTaO”, **C. Baristiran Kaynak**, M. Lukosius, I. Costina, B. Tillack, Ch. Wenger, G. Ruhl, S. Rushworth, Microelectronic Engineering, vol. 87, pp. 2561-2564, 2010.
2) “Enhanced leakage current behaviour of $Sr_2Ta_2O_{7-x}/SrTiO_3$ bilayer dielectrics for metal-insulator-metal capacitors”, **C. Baristiran Kaynak**, M. Lukosius, I. Costina, B. Tillack, Ch. Wenger, G. Ruhl, T. Blomberg, Thin Solid Films, vol. 519, pp. 5734-5739, 2011.
3) “Single $SrTiO_3$ and $Al_2O_3/SrTiO_3/Al_2O_3$ based MIM capacitors: Impact of the bottom electrode material”, **C. Baristiran Kaynak**, M. Lukosius, B. Tillack, Ch. Wenger, T. Blomberg, G. Ruhl, Microelectronic Engineering, vol. 88, pp. 1521–1524, 2011.
4) “$Ce_xAl_yO_z$/TiN stack analysis for Metal-Insulator-Metal applications: Effect of annealing and the metal electrode deposition method”, **C. Baristiran Kaynak**, M. Lukosius, B. Tillack, Ch. Wenger, A, Abrutis, M. Skapas, Thin Solid Films, vol. 520, pp. 4518-4522, 2012.
5) “Atomic Vapor Depositions of Ti-Ta-O thin Films for Metal-Insulator-Metal applications”, M. Lukosius, **C. Baristiran Kaynak**, Ch. Wenger, G. Ruhl, S. Rushwoth, P. Baumann, Thin Solid Films , vol. 519, no. 11, pp. 3831-3834, 2011.

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Conferences & Symposiums

16) “Characterization of Sr-Ta-O based on spectroscopic techniques”, **C. Baristiran Kaynak**, M. Lukosius, I. Costina, C. Wenger, C. Borschel, C. Ronning, Synthesis, Processing and Characterization of Nanoscale Multi Functional Oxide Films II, European Materials Research Society, Spring Meeting, Strasbourg, France, 2009. *(poster presentation)*

17) “Ti/Sr-Ta-O/TaN MIM Capacitors”, **C. Baristiran Kaynak**, M. Lukosius, Ch. Wenger, I. Costina, G. Ruhl, Deutsche Physikalische Gesellschaft Spring Meeting, Dresden, Germany, 2009. *(oral presentation)*

18) “Electrical and structural characteristics of Sr-Ta-O/$SrTiO_3$ based M-I-M capacitors”, **C. Baristiran Kaynak**, M. Lukosius, B. Tillack, Ch. Wenger, G.

Ruhl, T. Blomberg, Deutsche Physikalische Gesellschaft Spring Meeting, Regensburg, Germany, 2010. *(oral presentation)*

19) “Enhanced leakage current behaviour of $Sr_2Ta_2O_{7-x}/SrTiO_3$ bilayer dielectrics for metal.insulator-metal capacitors”, **C. Baristiran Kaynak**, M. Lukosius, I. Costina, B. Tillack, Ch. Wenger, G. Ruhl, T. Blomberg, European Materials Research Society, Spring Meeting, Strasburg, France, 7 June- 11 June, 2010. *(poster presentation)*

20) “Single $SrTiO_3$ and $Al_2O_3/SrTiO_3/Al_2O_3$ based MIM capacitors: Impact of the bottom electrode material”, **C. Baristiran Kaynak**, M. Lukosius, B. Tillack, Ch. Wenger, T. Blomberg, G. Ruhl, 17th Conference on "Insulating Films on Semiconductors" Grenoble, France, June 21-24, 2011. *(poster presentation)*

21) “$Ce_xAl_yO_z$/TiN stack analysis for Metal-Insulator-Metal applications: Effect of annealing and the metal electrode deposition method”, **C. Baristiran Kaynak**, M. Lukosius, B. Tillack, Ch. Wenger, A. Abrutis, M. Skapas, European Materials Research Society, Spring Meeting, Nice, France, May 9 - 13, 2011. *(poster presentation)*