CROSS-COUPLED CMOS VOLTAGE CONTROLLED OSCILLATORS OPERATING IN THE X-BAND

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCE
OF BILKENT UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR
THE DEGREE OF
MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

By
Can Soygür
June 2023

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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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June 2023

Voltage controlled oscillators (VCOs) are electronic devices whose oscillation frequencies can be tuned by applying an external control input. A widely preferred topology is the cross-coupled VCO topology, which offers easy implementation inside integrated circuits. VCO designers take certain performance metrics into account for their designs, with the most prominent ones being the frequency tuning range and the output phase noise. These two metrics often require trading off from one another; as introducing more networks for tunability increases the overall noise within the device. With the aim of observing this trade-off between the tuning range and phase noise, four VCOs have been designed and fabricated in a single die with a 0.18 μm CMOS process. They are designed to operate in the X-band, at almost the same oscillation frequencies, to allow for easier comparison. Each VCO in the IC offers either more tunability with more tuning circuits or better phase noise performance with simpler circuits. Measurement results verify this hypothesis; a decrease in output phase noise is observed in the tested VCOs that contained simpler tuning network. With center frequencies of oscillation at approximately 12 GHz in the VCOs, tuning ranges as high as 25% are achieved in the VCO with most tunability, while phase noises as low as -106 dBm/Hz (at a 1 MHz offset) were achieved in the one with no tunability.

Keywords: Voltage controlled oscillator, VCO, CMOS, cross-coupled, tuning range, phase noise.

ÖZET

X-BANDINDA ÇALIŞAN ÇAPRAZ BAĞLI CMOS GERİLİM KONTROLLÜ OSİLATÖRLER

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Haziran 2023

Gerilim kontrollü osilatörler (GKO'lar) salınım frekansları dışarıdan sağlanan bir kontrol girdisi ile ayarlanabilen elektronik aygıtlardır. Entegre devrelere kolay uyarlanabilirlik sunması açısından yaygın olarak tercih edilen topolojilerden biri çapraz bağlı GKO topolojisidir. GKO tasarımcıları tasarımları için belirli performans kriterlerini, en öne çıkanları frekans ayarlama aralığı ve çıktı faz gürültüsü olmak üzere, dikkate alırlar. Bu iki kriter çoğu zaman bir diğerinden ödün verilmesini gerekli kılar; ayarlanabilirlik açısından daha fazla devre eklenmesi cihaz içerisindeki toplam gürültüyü arttırır. Ayarlama aralığı ve faz gürültüsü arasındaki bu dengeyi gözlemleyebilmek adına 0.18 μm CMOS proseste üretilmiş tek bir çip içerisinde dört farklı GKO tasarlandı ve üretildi. Daha kolay karşılaştırma yapılabilmesi için hepsi X-bandında ve neredeyse aynı salınım frekansında çalışacak şekilde tasarlandı. Çip içerisindeki her GKO ya daha fazla ayarlanabilirlik için daha karmaşık ayarlama devreleri ya da daha iyi faz gürültüsü performansı için daha sade devreler sunmaktadır. Ölçüm sonuçları bu hipotezi doğrular niteliktedir; test edilen GKO'lardaki ayarlama devrelerinin sadeleşmesinin çıktı faz gürültüsünün azalmasına yol açtığı gözlemlenmiştir. GKO'ların merkez salınım frekansları yaklaşık 12 GHz olup en fazla ayarlanabilir GKO'da %25 ayarlama aralığına erişilmiş olunup ayarlanabilirliği olmayanda ise -106 dBm/Hz (1 MHz ofsette) faz gürültüsüne erişilmiştir.

Anahtar sözcükler: Gerilim kontrollü osilatör, GKO, CMOS, çapraz bağlı, ayarlama aralığı, faz gürültüsü.

Acknowledgement

I would like to thank and express my gratitude to my advisor Prof. Abdullah Atalar for his support and guidance throughout my graduate studies. His way of teaching and enthusiasm had made me interested in microelectronics when I was an undergraduate student. His knowledge has taught me a lot and inspired me in the last three years. It was an invaluable experience for me to work with him.

I would also like to thank Prof. Ekmel Özbay and Prof. Ali Bozbey for reviewing this thesis and participating in the thesis committee.

I am especially grateful to my friends Derin Erkan for assisting me with lab-related works many times and Mehmet Halit Öztürk for helping me with the wire bonds on my dies. It was thanks to their help and practical knowledge that the final parts of this thesis were completed successfully.

I would like to thank Derin again, along with Baha Erim Uzunoğlu and Sobhan Gholami for their friendship and all the fun times we had in the office. I am so glad to know them, and wish them the best for their future endeavors.

My special thanks are for my long-time friends Süleyman Taylan Topaloğlu, Doğa Gürgünoğlu, Onur Özder, Ali Bahadır Alga, Ceyhun Emre Öztürk, Alper Umut Uçar, Ömer Deveer, Mustafa Bay, Onur Kağan Çoşkun, Berat Aydın, Osman Gülüzade, Baturay Sağlam and Onat Dalmaz, whom I have known for years in my time at Bilkent and endured all difficulties with. They are the best.

I sincerely and wholeheartedly thank my mother Fatoş Betül Sevgican, my father Kazım Hakan Soygür and my sister Sera Soygür, along with the rest of my family. Their unconditional love has supported me throughout my life and brought me to where I am now.

My final and deeply thanks are for my significant other Selen Ünal, who have always been there for me with love, kindness, joy and empathy. Her support and encouragement have always helped me while working on this thesis, even at the most difficult times. I feel so lucky to have her in my life.

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Chapter 1

Introduction

Electronic oscillators are devices that generate a waveform at their output without any input. They are widely used in applications such as clock generation for digital circuits, carrier signal generation, within phase-locked loops, and in any other application where a steady and reliable periodic signal is needed [1, 2].

Oscillators can be modeled as an amplifier and a resonator (frequency selective network) connected in a positive feedback loop, as shown in Fig. 1.1. The initial input signal v_{in} represents the noise present in the circuit, as no external input signals are provided. It is amplified, frequency selected, then fed back into the loop, and amplified again. Thus, the output signal v_{out} grows over time at a particular frequency [2].

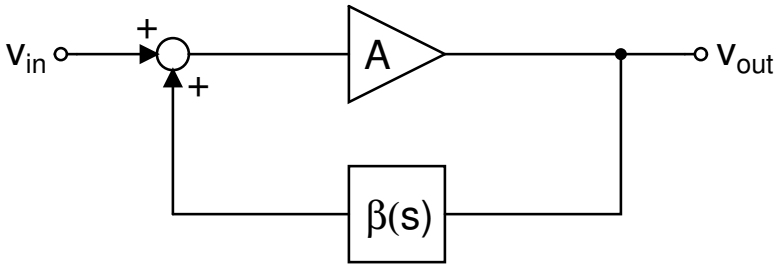


Figure 1.1: Feedback diagram of an oscillator

Closed loop gain of the system, given in Eq. 1.1, elaborates this phenomenon mathematically. If the denominator of the closed-loop gain is zero at any frequency, the system may oscillate. The conditions necessary for oscillation are called *Barkhausen criteria*, which state that loop gain should have unity magnitude ($|A\beta(s)| = 1$) and multiples of 360° phase shift ($\angle A\beta(s) = 2\pi k,\ k \in \{0, 1, 2, ...\}$) [2].

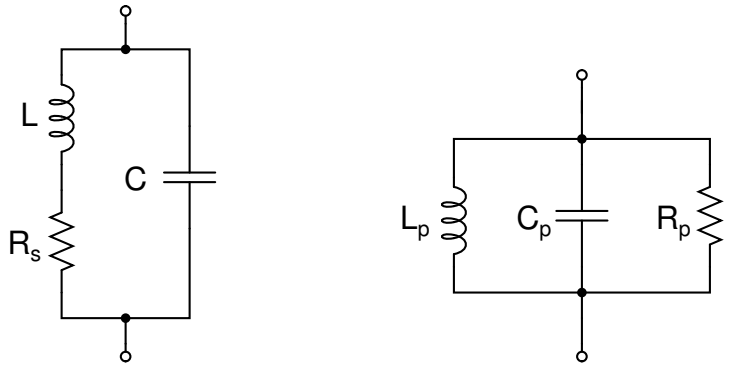
$$\frac{v_{out}}{v_{in}} = \frac{A}{1 - A\beta(s)} \tag{1.1}$$

Similar to many other electronic devices, oscillators can be realized in an integrated circuit instead of being constructed with discrete components. This allows for much smaller form factors, so that the overall device can be realized as a microchip, or as only a part of a microchip with many other components. CMOS processes allow easy fabrication of two types of oscillators: LC oscillators (a type of harmonic oscillator) and ring oscillators (a type of relaxation oscillator) [1]. The main focus of this thesis is the design and fabrication of a cross-coupled LC tank oscillator with a CMOS process.

1.1 Cross-Coupled CMOS Oscillators

A cross-coupled oscillator has a simple and robust topology that makes it an attractive choice in many applications. It consists of two amplifier stages connected to each other in a positive feedback loop. On their own, each introduces a 180° phase shift between their inputs and outputs. Although they cannot oscillate on their own in this manner, together they can produce a 360° phase shift. If the gain is also sufficient, both Barkhausen criteria are satisfied, and an oscillation can be sustained [3].

LC tanks form the frequency selective network in a cross-coupled topology, thus it is beneficial to examine them. An LC tank can be modeled as an inductor and a capacitor connected in parallel, with a series resistance accompanying the inductor. For easier calculations, this network can be converted to three equivalent parallel components, as shown in Fig. 1.2. The new values of the tank components are $C_p = C$, $L_p = (1+1/Q^2)L$, and $R_p = (1+Q^2)R_s$, where Q is the inductor quality factor at the resonance frequency. (The latter two can be derived from Eq. 2.2, which is discussed in Chapter 2. They can also be approximated as $L_p \approx L$ and $R_p \approx Q^2 R_s$, but only if Q is sufficiently large, which is not always the case in ICs.) The resonance frequency of an LC tank is given in Eq. 1.2 [1].



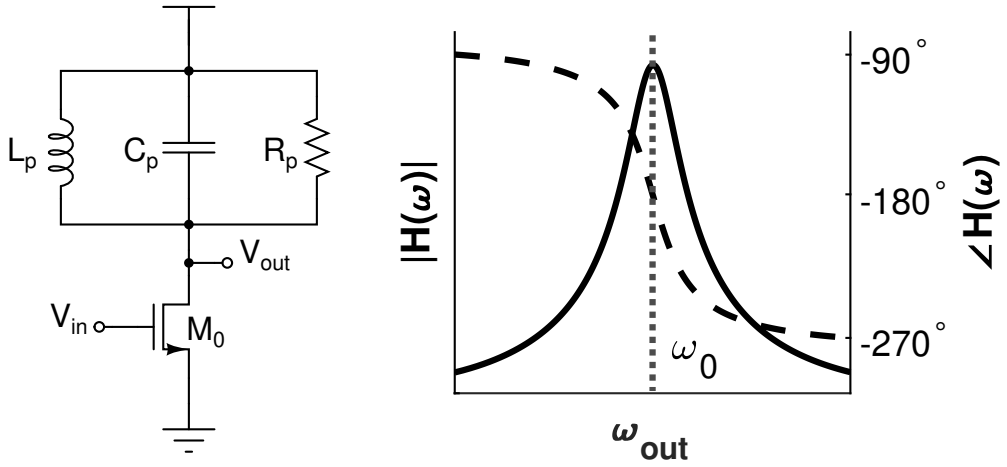
(a) LC tank (b) with parallel components

Figure 1.2: LC tank model and its equivalent circuit with parallel components

$$\omega_0 = \frac{1}{\sqrt{L_p C_p}}$$
$$f_0 = \frac{1}{2\pi\sqrt{L_p C_p}} \tag{1.2}$$

(The parallel LC tank in Fig. 1.2b can be thought of as representing all inductive, capacitive, and resistive components within an integrated circuit. As parasitics are introduced due to substrate couplings, metal tracks, and other factors; they begin to contribute to the overall resonance frequency of an oscillator.)

Using this LC tank, a frequency-tuned amplifier can be built, as shown in Fig. 1.3. This amplifier would produce a gain of $g_m R_p$ and a frequency shift of 180°, insufficient to produce an oscillation when fed to itself. However, using a duplicate of it and connecting them in a feedback loop, as shown in Fig. 1.4, would produce a gain of $(g_m R_p)^2$ (assuming that M_0 and M_1 transistors are identical) and a total phase shift of 360°. If $(g_m R_p)^2 \geq 1$, the circuit will oscillate. The frequency of oscillation is again given by Eq. 1.2 [1, 3].



(a) Tuned amplifier (b) Gain response

Figure 1.3: A single tuned amplifier and its gain response

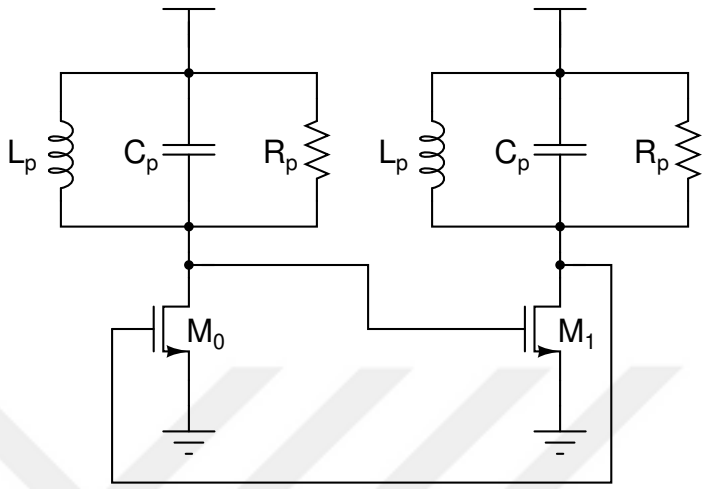
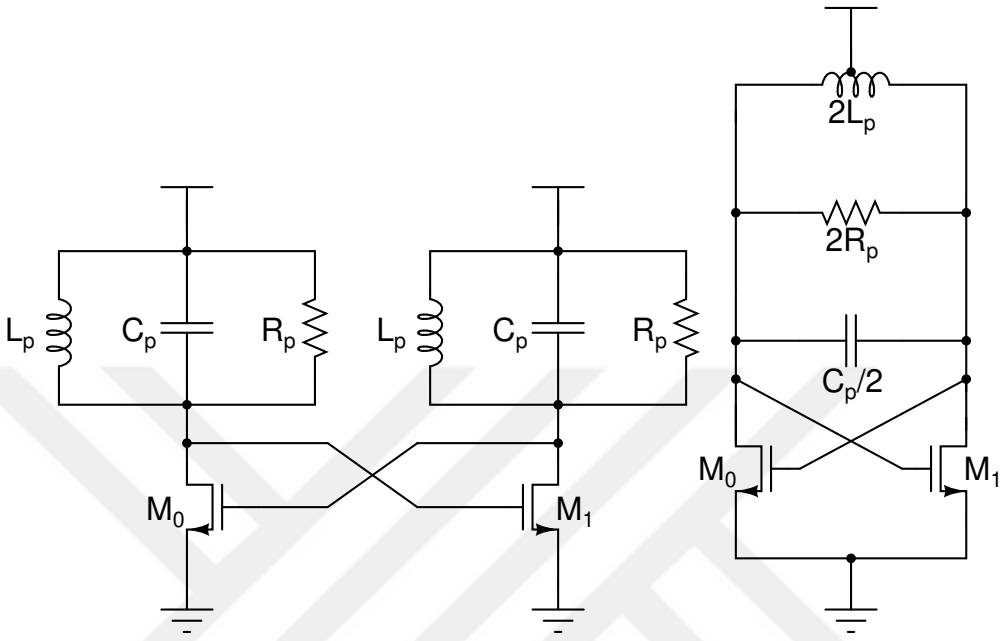


Figure 1.4: Two tuned amplifiers in feedback loop, forming an oscillator

The drain-to-gate connections in this circuit can be denoted in a simpler manner, and the components of the LC tanks can be simplified, as shown in Fig. 1.5. However, it should be noted that merging the L_p inductors into a single $2L_p$ inductor is only valid if there is no coupling between them. Otherwise, mutual coupling should be taken into account, and the total inductance may reach $4L_p$ if the coupling is perfect. Therefore, the designer should compensate for this effect by changing the inductor parameters accordingly. A tail bias using a current source could also be added to reduce supply sensitivity of the device, as in Fig. 1.6, at the cost of the magnitude of the output swing [3]. (To achieve maximum output swing and reduce the number of components, a tail bias is not included in our designs.)



(a) Simplified connection (b) Simplified tank

Figure 1.5: Simple cross-coupled oscillator topology

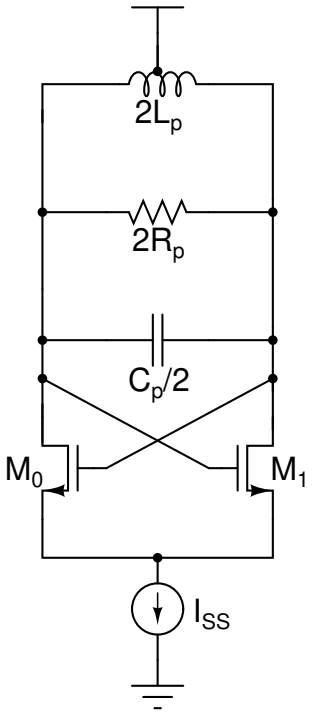


Figure 1.6: Cross-coupled oscillator with a tail bias

Although most cross-coupled oscillators are designed according to the topologies in Fig. 1.5b or Fig. 1.6, one can build a cross-coupled oscillator using both NMOS and PMOS types of transistors. Called a *complementary cross-coupled oscillator* and presented in Fig. 1.7, it offers several advantages. First of all, it provides a common mode output of $V_{DD}/2$ (unlike the previous ones that swing around V_{DD}), allowing for easier tuning of varactors present in the frequency selective network. Furthermore, it doubles the output swing. These come at the cost of adding two PMOS devices that are at least double the size of NMOS devices, consuming chip area and adding additional capacitance to the network due to their gates [3].

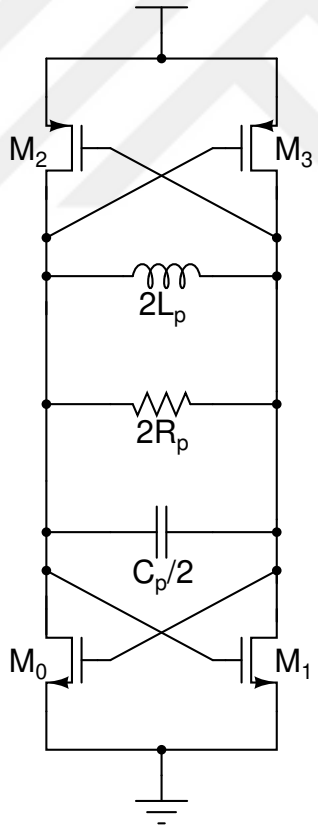


Figure 1.7: Complementary cross-coupled oscillator topology

Our main focus in this section was on the cross-coupled topology itself. However, what makes an oscillator a *voltage controlled oscillator (VCO)* is the tunability aspect of its frequency selective network. For VCOs that use an LC tank circuit, this means altering the capacitance or inductance of the tank by applying a control voltage. The most common method of doing so is using varactors, devices that vary their capacitance with respect to DC voltage applied between their terminals. They are constructed using MOSFET devices in integrated circuits (though varactor diodes are used in discrete designs). Other methods mostly consist of connecting or disconnecting capacitors/inductors through switches, allowing discrete tuning of a VCO [3].

1.2 Performance Metrics

Performance of a VCO can be quantified using a series of performance metrics. These metrics are important design considerations that IC designers aim to optimize [1, 2]:

- **Center frequency** (f_c): Center frequency of oscillation. Measured in GHz.
- **Tuning range** (TR): Measure of tunability for a VCO, given either as a range (in GHz) or as a percentage with respect to the center frequency. (Described further in Sec. 1.2.1.)
- **Output amplitude** (P_{out}): Power amplitude of the signal at the output. Measured in dBm.
- **Power dissipation** (P_{DC}): DC input power consumed by the oscillator to sustain the operation. Measured in mW.
- **Phase noise** ($\mathcal{L}(\Delta f)$): Random fluctuations in output frequency (or phase). Measured in dBc/Hz at a particular frequency offset. (Described in further detail in Sec. 1.2.2.)

- Tuning sensitivity (K_{VCO}): Variation in oscillation frequency in accordance with the applied control voltage. Given in MHz/V. It is usually not constant and depends on the tuning hardware, such as varactors.

- Frequency stability: Changes in the oscillation frequency due to changes in temperature. Measured in ppm/°C.
  ("ppm" stands for "parts per million"; in this context, it means the ratio between the variation and the center frequency. e.g., 5 ppm variation at 10 GHz oscillation frequency means 50kHz shifts from this frequency.)

- Harmonic power (G): Output power of harmonics with respect to the fundamental frequency during oscillation. Measured in dBc.

- Supply and common-mode rejection: The noise sensitivity of an oscillator determines how well it rejects noise caused by the supply or by itself. Measured in dB.

- Frequency pulling (f_{pull}): Amount of change in the output frequency caused by variation in load impedance. Measured in MHz at a particular VSWR value (e.g., 1.75:1 VSWR).

- Frequency pushing (f_{push}): Amount of change in the oscillation frequency caused by the change in the supply voltage. Measured in MHz/V.

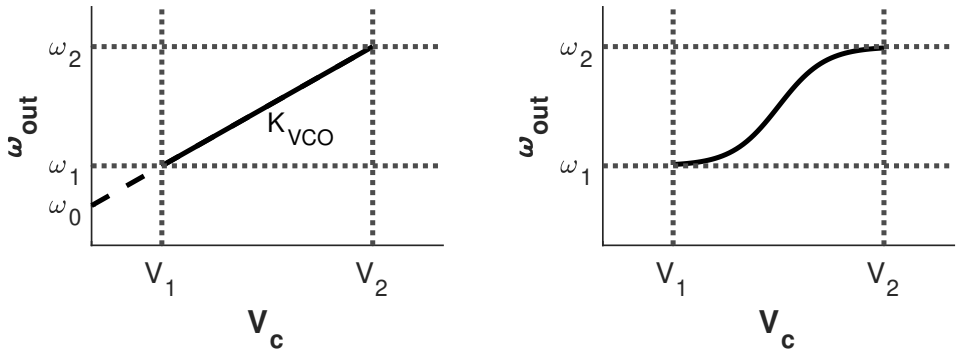
The bold elements are the metrics we took into account while designing our on-chip VCOs, while the ones also underlined are the main metrics that varied between our designs. These metrics, namely *tuning range* and *phase noise* are elaborated in the subsections Sec. 1.2.1 and Sec. 1.2.2 below, followed by a more generalized metric called *figure of merit (FoM)* in Sec. 1.2.3. (It should also be noted that although we did not directly design for it, we simulated the frequency pulling and frequency pushing metrics for our devices.)

1.2.1 Tuning Range

The tuning range defines the variation in the oscillation frequency with respect to the center frequency in a VCO. It is determined by a designer's choice of range (so that the VCO satisfies the requirements of an application), as well as process and operation temperature variations. The latter set a requirement for VCOs to have sufficient ranges so that they can oscillate at the desired frequency [1].

An elaboration of the tuning range concept is shown below in Fig. 1.8. K_{VCO} represents tuning sensitivity (or gain). The tuning range is defined as the frequency range in which a VCO can be tuned, which is $\omega_2 - \omega_1$. In realistic cases, tuning is never completely linear; yet depending on the linearity, the output frequency can be estimated, as shown in Eq. 1.3 [1].

$$\omega_{out} = \omega_0 + K_{VCO} \times V_c \tag{1.3}$$



(a) Constant K_{VCO} (b) Variable K_{VCO}

Figure 1.8: Example output frequency plot wrt. input control voltage V_c

1.2.2 Phase Noise

Theoretically, the output spectrum of an ideal oscillator would only consist of a delta function at the oscillation frequency. In reality, this spectrum is a broad and continuous distribution with its peak at the oscillation frequency, yet its vicinity has non-zero amplitude values. Therefore, it can be expressed as Eq. 1.4, showing that the amplitude and phase of the output signal vary over time. (The first results in amplitude noise, which is negligible compared to phase noise.) Phase and frequency of the output are strongly related as shown in Eq. 1.5 [3, 4].

$$v_{out} = A(t) \times cos(\omega_0 t + \phi(t)) \tag{1.4}$$

$$\omega(t) = \omega_0 + \frac{d\phi(t)}{dt} \tag{1.5}$$

This phenomenon is caused by random fluctuations arising from intrinsic sources such as thermal noise and various extrinsic noise sources. Furthermore, harmonics and intermodulation products may appear as spikes in this distribution, as shown in Fig. 1.9 [2, 4, 3].

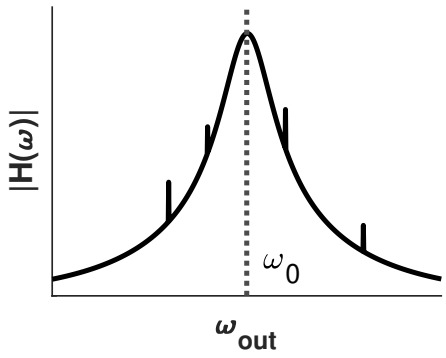


Figure 1.9: Example output spectrum denoting phase noise

Phase noise is characterized as the ratio of the single sideband (SSB) noise power at an offset Δf per unit bandwidth (Hz), to the power of the main oscillation frequency (which can be referred to as the carrier signal). In other words, the ratio of noise power to carrier power, as expressed in Eq. 1.6 [2, 4].

$$\mathcal{L}(\Delta f) = \frac{P_n}{P_c} = P_{n\ [\text{dBm/Hz}]} - P_{c\ [\text{dBm}]}\ [\text{dBc/Hz}] \tag{1.6}$$

1.2.3 Figure of Merit (FoM)

A special metric taking into account the center frequency, phase noise (with measurement offset), and power dissipation, thus summarizing the overall performance of an oscillator, is called the *figure of merit* and abbreviated as FoM. Its relation is given in Eq. 1.7 and is expressed in dBc/Hz. Its variant *figure of merit with tuning range*, abbreviated as FoM_T, additionally takes into account the tuning range metric to assess the performance of VCOs. Given in Eq. 1.8, its unit is dBc/Hz [3].

$$FoM = \mathcal{L}(\Delta f) - 20\log(\frac{f_c}{\Delta f}) + 10\log(P_{DC})\ [\text{dBc/Hz}] \tag{1.7}$$

$$FoM_T = FoM - 20\log(\frac{TR_{\%}}{10})\ [\text{dBc/Hz}] \tag{1.8}$$

1.3 Literature Review

The work in contemporary literature consists of VCO designs that aim to excel in certain performance metrics (the same metrics mentioned in Sec. 1.2). While some intend good performance in certain center frequencies, others aim for wider tuning ranges. Others may target an exceptional phase noise performance or lower power consumption. Aiming for any one of these affects the performance in other metrics. Ergo, the works present in the literature defend a certain design by testing it and comparing its metrics with others' designs. (Almost all papers also make generic comparisons in terms of FoM and FoM_T.)

The work presented in [5] has given inspiration about both the general topology and the coarse tuning mechanism of our VCO devices. In the work, the authors have used the complementary cross-coupled topology in their VCO, without a tail bias, and utilized a 3-bit switched capacitor array for coarse tuning. The latter choice has given them 8 different switching combinations. Combined with the varactors in their VCO that allow for continuous tuning, they achieve a wide tuning range of 51.7% at the center frequency of 2.4 GHz and -123.8 dBc/Hz phase noise at 1MHz offset from this center frequency. Their design is built with a 0.18 μm CMOS process. Although their design operates mostly in the S-band, we confirmed that the topology is also useful in the X-band.

Another interesting work that caught our attention was [6]. Built-in a 0.18 μm CMOS process, the authors' VCO design uses an ordinary cross-coupled architecture, without PMOS devices or tail biases. However, they have chosen to utilize a custom-built inductor (which is actually a transformer; with two separate windings) that is switchable. A switch connects or severs a connection between two halves of the secondary winding. When turned on, the secondary winding completes a closed loop and drains the energy coming from the primary winding, effectively dropping its inductance value. When turned off, the primary winding acts as an ordinary monolithic inductor, with a higher inductance. The authors have also added inverters to the secondary winding, connected to another switch, so that when that switch is turned on, the secondary winding boosts the primary,

thus yielding an even higher inductance. With these three modes of operation, combined with the varactors, they achieve a wide tuning range of 38.8% at the center frequency of 24.7 GHz, operating in the K band. An overall average of -122.3 dBc/Hz phase noise at a 10MHz offset is also achieved.

A work that follows a different approach is [7], where the authors have built a complementary cross-coupled oscillator (not tunable) in 0.25 μm CMOS process, with a tail bias at the end. Their device oscillates at 1.8 GHz in the L band. By varying its tail bias and supply voltage, they aim to find an optimum point between phase noise performance and power consumption of the device. They present such a point, with -121 dBc/Hz phase noise at 600kHz offset from oscillation frequency, while the device consumes 6 mW of power. Moreover, the authors present another set of measurements at the end with a cross-coupled oscillator using only NMOS devices, confirming the superior phase noise performance of complementary cross-coupled devices, which encouraged us to design our VCOs in this manner.

One work that uses a more contemporary technology is presented in [8], which uses a 45 nm CMOS process. The authors designed their cross-coupled VCO to operate at the center frequency of 16GHz, in the Ku band. Their proposed topology utilizes two different switched capacitor arrays, a 6-bit one for mid-tuning and a 3-bit one for coarse tuning purposes, along with varactors for continuous tuning. Ultimately, a tuning range of 37.5% and a phase noise performance of -110 dBc/Hz at 1 MHz offset have been achieved.

One last academic work worth mentioning is [9], in which the authors present a mm-wave cross-coupled oscillator (not tunable) designed in a 65 nm CMOS process. Through the use of inductors and transmission lines in conjunction, along with buffer-feedback and negative resistance tank networks, they have achieved an oscillation frequency of 82.4 GHz and a phase noise performance of -112 dBm/Hz at 10MHz offset. Since their device operates in the W band, their design and methodology are much different from the other works reviewed in the course of this thesis. Operating in this frequency band requires extensive usage of microwave design techniques, even on smaller length scales inside an

integrated circuit. Nevertheless, the authors' way of designing the output common source buffer with a $\Lambda 4$ transmission line has given the idea of designing the buffers of our devices with RF-choke inductors instead of resistors or CMOS inverters, unlike most others' works.

It is beneficial to review some commercial products along with academic work. Datasheets [10, 11] present two off-the-shelf VCOs, designed to oscillate at 1–2.3 GHz band (L and S-bands) and 8–16 GHz band (X and Ku-bands), respectively. These correspond to 1.65 GHz and 12 GHz center frequencies with 79% and 67% tuning ranges. As for their phase noise performances; the first VCO offers -101 dBc/Hz output phase noise (at a 10 kHz offset) while the latter one offers -94 dBc/Hz (at a 100 kHz offset). However, it should be noted that these VCOs are not designed with power consumption concerns; while the first requires a 12 V DC bias, the latter requires both a 5 V and a -1.7 V DC bias to operate. Maximum tuning voltages are in scale with this; 24 V and 15 V respectively. Combined with the fact that they both come with packages that take a certain amount of space on PCBs, it is understandable for researchers to pursue VCOs with much smaller form factors and that can operate with lower supply voltages.

Although the works and products presented above establish only a small portion of all research in the literature related to the design of cross-coupled VCOs, we intended to mention the most closely related ones to our work. These aforementioned works, along with many others, provided useful information on how to approach the task of building VCOs.

1.4 Motivation

The motivation of this thesis is to design, simulate, manufacture, and test different VCO designs that meet certain performance criteria. While maintaining a certain quality that would make our VCOs comparable with the work present in the literature, the main aim is to observe the trade-off between tunability and phase noise of a VCO. Widening the tuning range of a VCO requires more sophisticated control circuitry. Since it is known that one major source of noise is the very components in a circuit, lowering the phase noise may necessitate simpler circuitry with fewer components. The work presented in this thesis aims to observe how much it impacts to sacrifice tuning range to improve phase noise performance. For this purpose, we designed four VCOs intended to operate in the X-band (8-12 GHz, with 10 GHz center frequency) and with varying tuning ranges, with the expectation of observing different phase noise performances from each.

(In Chapter 2, the previous motivation of this thesis is presented where custom on-chip inductors are designed with the aim of understanding how their inductances and quality factors are affected by varying their design parameters.)

1.5 Thesis Outline

This chapter, Chapter 1, introduces the reader to the topic and purpose of the thesis, which is the design and testing of integrated RF VCOs. Chapter 2 elaborates how on-chip inductors are custom-designed and simulated, which was our previous work before deciding to design VCOs. Chapter 3 discusses how our complementary cross-coupled VCOs are designed, drawn, simulated, and fabricated at the end. Chapter 4 presents our measurement results with an actual fabricated IC under test. Chapter 5 reviews the work done throughout the thesis and argues what future work can be done.

Chapter 2

Design of Monolithic Inductors

The aim of this thesis prior to designing on-chip VCOs was to design on-chip monolithic inductors with different design parameters and compare their performance metrics with respect to the said parameters. Because monolithic inductors are crucial components for the operation of our VCOs (which utilize LC tank resonators), it is beneficial to present the process and results of this research for informing the reader about the principles of designing and simulating these components.

Inductors are passive circuit elements that conserve the flow of current by electromagnetic means. These components store energy in a magnetic field when a current flows through them. They could be thought of as components that oppose the change in current and thus, generate an electromotive force (EMF) as a result. Therefore, their I-V characteristics can be expressed as shown in Eq. 2.1 [12]. Some of their applications include switching regulators, filters, and oscillators.

$$v_L(t) = L\frac{di_L(t)}{dt} \tag{2.1}$$

Inductors are often realized by wrapping an insulated wire around a coil and are mostly used as discrete components. However, it is also possible to realize an inductor inside an integrated circuit. These inductors are called monolithic (or integrated) inductors and are made from metal tracks inside an IC [13].

2.1 Monolithic Inductors

Monolithic inductors provide lower inductance (L) and lower quality factor (Q) values compared to their discrete counterparts, which is due to their manufacturing process. Realization in an IC allows for smaller surface areas, shorter lengths, and fewer number of turns. When combined with the fact that silicon substrates are weakly diamagnetic materials (thus can be considered equivalent to an air core), resulting inductances are on the order of nano henries (or even picohenries). The latter reason also causes the quality factor to be on the order of 1-20, depending on the design parameters of an inductor [13].

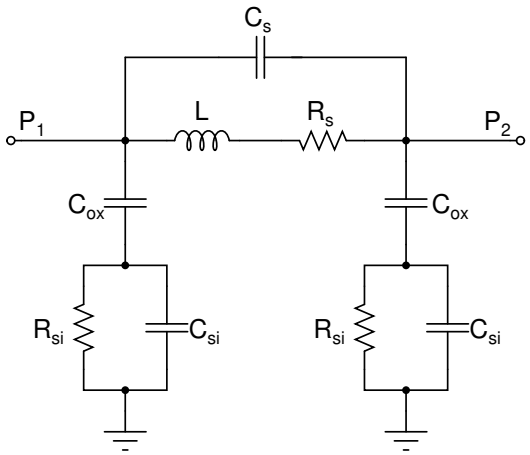
The most common type of monolithic inductors used in ICs are spiral inductors. Due to the mutual coupling between turns in the spirals, it yields better performance compared to straight metal tracks [13]. (Although meander tracks are sometimes used [14].)

Depending on how their metal tracks are looped, they can be categorized into *asymmetric spiral inductors* and *symmetric spiral inductors* [13]. The types of symmetric inductors of interest are symmetric spiral inductors. Unlike their asymmetrical counterparts, they can be utilized in differential circuits and thus are less susceptible to noise. Their symmetric layout allows designers to add a center tap if necessary. Moreover, the differential mode of operation yields higher inductance and Q-factors compared to the single-ended operation.

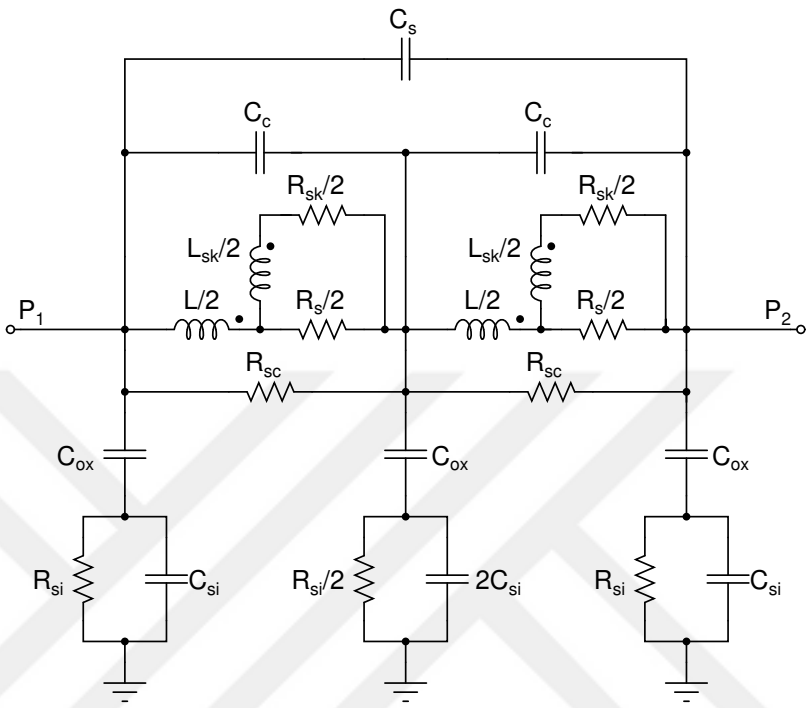
2.1.1 Modeling

Monolithic inductors are much harder to model than polysilicon resistors or parallel plate capacitors. Their models are highly process-dependent and require extensive information about their geometry, layout, and metal layers [13]. Although EDA tools often use more sophisticated models for design and simulation purposes [15], there exist simpler models too.

Two most common on-chip inductor models are Π-type circuits which are constructed to model the inductance L and most of the loss mechanisms in monolithic inductors. They are shown in Fig. 2.1 and include metal track resistances R_s, feedthrough capacitance C_s, metal-substrate couplings C_{ox} (due to oxide in between) and silicon substrate losses C_{sub} and R_{sub}. Common issues with the single-Π model in Fig. 2.1a are that its parameters are dependent on frequency and its insufficiency for modeling some types of losses in higher frequencies, whereas the double-Π model in Fig. 2.1b has frequency-independent parameters and models phenomenon such as skin and proximity effects. The first is modeled by L_{sk} and R_{sk}, while the latter is modeled by mutual couplings between the inductors (denoted by dots on the inductor symbols). Also, metal-metal couplings are modeled with C_c while R_{sc} models the electrical coupling between the oxide capacitances denoted by C_{ox} [14, 15, 16].



(a) Single-Π model



(b) Double-Π model

Figure 2.1: Schematics of on-chip inductor models

2.1.2 Characterization

The three most important characteristics/parameters of a monolithic inductor are its inductance, quality factor, and equivalent series resistance. The quality factor Q of an inductor is directly proportional to its inductance and inversely proportional to its equivalent series resistance. This is consistent with the fact that the quality factor is the ratio of the energy stored in a resonator to the energy dissipated by it in one cycle. It can be directly derived from the real and imaginary parts of an inductor's impedance. Moreover, when nonideal effects like self-resonance are omitted (or the measurement is away from the self-resonance frequency), the quality factor of an inductor can be approximated as described in Eq. 2.2. Inductance L can also be deduced from the impedance for a given frequency, as shown in Eq. 2.3. The resistance R, on the other hand, is simply the real part of the impedance, given in Eq. 2.4 [13, 14].

$$Q = \frac{Im(Z)}{Re(Z)} \approx \frac{\omega L}{R} \tag{2.2}$$

$$L = \frac{Im(Z)}{\omega} = \frac{Im(Z)}{2\pi f} \tag{2.3}$$

$$R = Re(Z) \tag{2.4}$$

As for how the impedance of an inductor could be calculated or measured, one can run s-parameter simulations or carry on s-parameter measurements on the device. After obtaining the required s-parameters for the frequency range, the single-ended or differential impedance can be computed. (It should be noted that Eqs. 2.2 and 2.3 hold for any type of impedance.) Eq. 2.5 gives the single-ended impedance value Z_{se} (where the other port is grounded), whereas Eq. 2.6 gives the differential impedance Z_{diff} [14].

$$\begin{aligned} S_{\text{se}} &= S_{11} - \frac{S_{12}S_{21}}{1 + S_{22}} \\ Z_{\text{se}} &= Z_0 \frac{1 + S_{\text{se}}}{1 - S_{\text{se}}} \end{aligned} \tag{2.5}$$

$$\begin{aligned} S_{\text{diff}} &= \frac{S_{11} - S_{12} - S_{21} + S_{22}}{2} \\ Z_{\text{diff}} &= 2Z_0 \frac{1 + S_{\text{diff}}}{1 - S_{\text{diff}}} \end{aligned} \tag{2.6}$$

2.2 Design and Simulation of Sample Symmetric Inductors

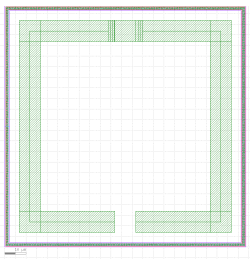
The design of a symmetric spiral inductor takes into account the L and Q values required by the application along with the chip area that the inductor uses. The latter is an important constraint, as inductors are the most chip area-consuming components [13].

In order to observe how the performance of an inductor is affected due to design parameters, we decided to design a series of simple, square-shaped, symmetric spiral inductors. By varying their parameters, we were able to observe how their performances are affected. The parameters suggested to vary are given below in Table 2.1, all of which increase the overall area an inductor consumes as they increase.

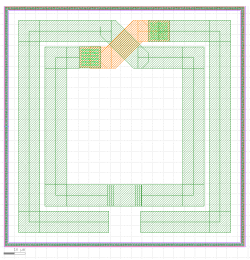
Parameters	Abbreviations
Outer diameter	a (μm)
Number of windings	n
Track width	w (μm)
Track spacing	s (μm)

Table 2.1: Varied inductor parameters and their abbreviations

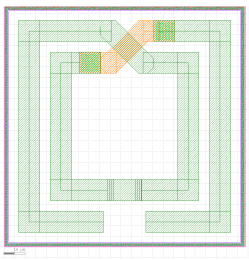
By varying these parameters we developed seven different designs, ranging from Ind 0 to Ind 6, the layouts of which are given in Fig. 2.2. Process development kit (PDK) of XFAB XC06, a 0.6 μm CMOS process, was chosen for this job [17]. The inductor layouts were drawn using the thick top metal layer (METL) and parasitic extraction was performed to extract the inductance along with other capacitive and resistive parasitics. All layouts were drawn using Cadence Virtuoso and extracted using Cadence Assura software. (The legend showing color-layer assignments is given in Fig. B.1. Despite that this legend being made for TSMC's PDK for the following chapters, it can be used to refer to layers drawn in XC06, as the same color-layer matching was used. METL corresponds to METAL3.)



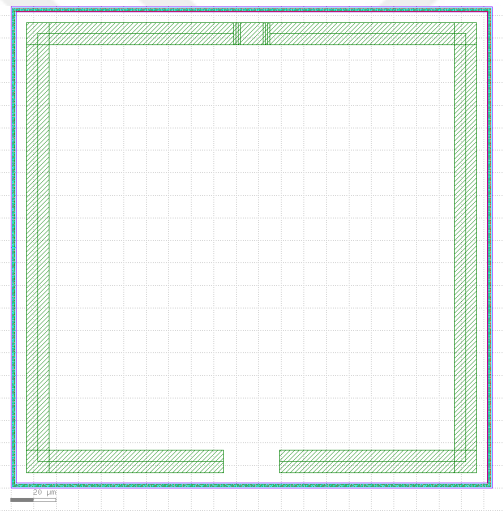
(a) Ind 0 ($\{a, n, w\} = \{100\mu\text{m},\ 1,\ 10\mu\text{m}\}$)



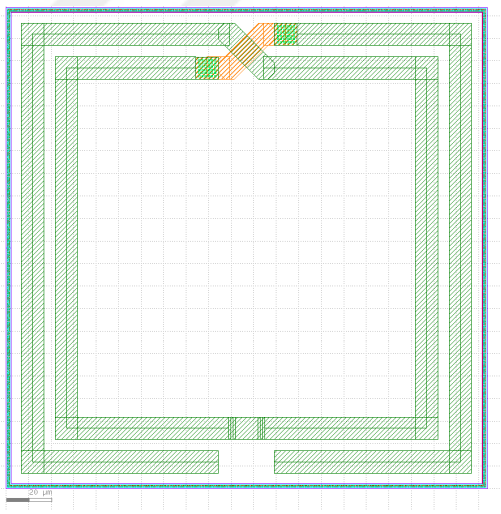
(b) Ind 1 ($\{a, n, w, s\} = \{100\mu\text{m},\ 2,\ 10\mu\text{m},\ 2.5\mu\text{m}\}$)



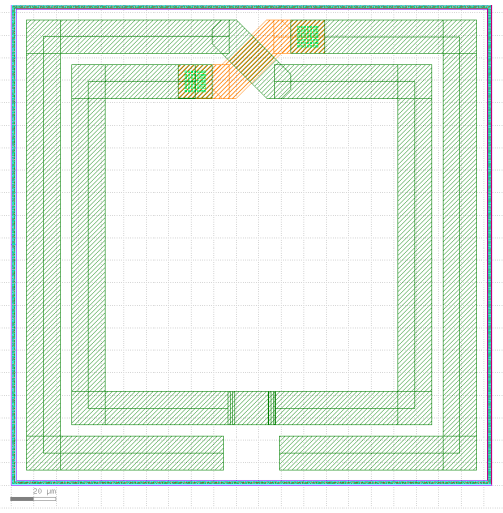
(c) Ind 2 ($\{a, n, w, s\} = \{100\mu\text{m},\ 2,\ 10\mu\text{m},\ 5\mu\text{m}\}$)



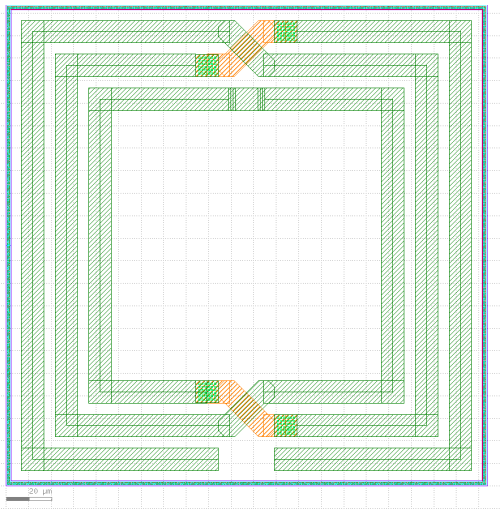
(d) Ind 3 ($\{a, n, w\} = \{200\mu\text{m},\ 1,\ 10\mu\text{m}\}$)



(e) Ind 4 ($\{a, n, w, s\} = \{200\mu\text{m},\ 2,\ 10\mu\text{m},\ 5\mu\text{m}\}$)



(f) Ind 5 ($\{a, n, w, s\} = \{200\mu\text{m},\ 2,\ 15\mu\text{m},\ 5\mu\text{m}\}$)



(g) Ind 6 ($\{a, n, w, s\} = \{200\mu\text{m},\ 3,\ 10\mu\text{m},\ 5\mu\text{m}\}$)

Figure 2.2: Layouts of different inductor designs

After extracting these designs, s-parameter analyses are performed using the Cadence Spectre simulator, and their *differential* impedances are found according to Eq. 2.6; since symmetric inductors are designed to be operated differentially, they yield their best results this way. At the end, to compute their Q-factor, inductance, and resistance; Eqs. 2.2, 2.3 and 2.4 are used, respectively. The results of this simulation are presented in Fig. 2.3, as well as in Table 2.2 for frequencies f=1 and 10 GHz.

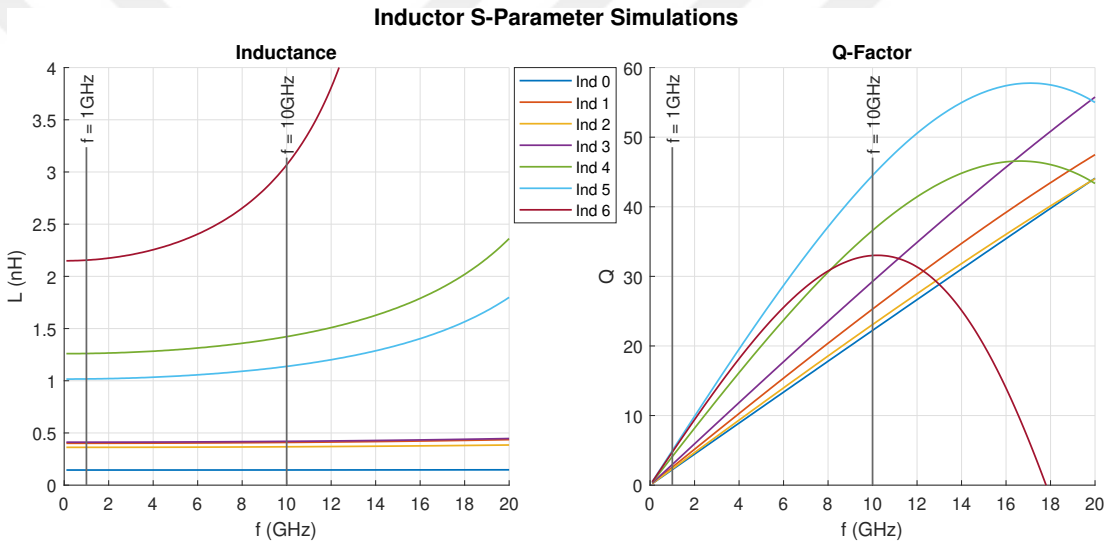


Figure 2.3: Inductance and Q-factor of the inductors wrt. frequency

Ind	Parameters				$f = 1$ GHz			$f = 10$ GHz			f_{sr}
#	a(μm)	n	w(μm)	s(μm)	L(H)	R(Ω)	Q	L(H)	R(Ω)	Q	(GHz)
0	100	1	10	-	145p	408m	2.23	145p	411m	22.2	163
1	100	2	10	2.5	401p	977m	2.58	409p	1.02	25.3	68.7
2	100	2	10	5	362p	972m	2.34	368p	1.00	23.1	80.2
3	200	1	10	-	412p	870m	2.97	420p	901m	29.3	69.4
4	200	2	10	5	1.26n	1.93	4.11	1.42n	2.44	36.6	28.8
5	200	2	15	5	1.02n	1.29	4.96	1.14n	1.61	44.5	29.8
6	200	3	10	5	2.16n	2.85	4.75	3.07n	5.84	33.0	17.8

Table 2.2: Comparison of inductor s-parameter analysis results

In the scope of these results, some comparisons are made with respect to how changing one design parameter (while keeping others the same) affects L, R, Q, and f_{sr}. In addition to these comparisons, we also observe that Q is approximately 10 times higher when the measurement frequency is changed from 1 to 10 GHz, which is expected as described in Eq. 2.2.

- **Outer diameter:** Ind 2 and 4 are compared by varying outer diameter $a = \{100,\ 200\}$ μm. ($n = 2,\ w = 10$ μm, $s = 5$ μm) are kept constant.) An increase in all three metrics L, R, and Q is observed. f_{sr} decreases significantly as a increases. (The same outcomes can be deduced by comparing Ind 0 and 3.)

- **Number of windings:** Ind 3, 4, and 6 are compared by varying numbers of windings $n = \{1,\ 2,\ 3\}$. ($a = 200$ μm, $w = 10$ μm, $s = 5$ μm) are kept constant.) An increase in all three metrics L, R, and Q is observed again. f_{sr} decreases as the number of windings increases.

- **Track width:** Ind 4 and 5 are compared by varying track width $w = \{10,\ 15\}$ μm. ($a = 200$ μm, $n = 2$, $s = 5$ μm) are kept constant.) A decrease in L and R is seen as Q increases. f_{sr} increases slightly.

- **Track spacing:** Ind 1 and 2 are compared by varying the track width $s = \{2.5,\ 5\}$ μm. ($a = 100$ μm, $n = 2$, $w = 10$ μm) are kept constant.) A decrease in L and Q is observed while R remains constant. However, f_{sr} increases.

Chapter 3

Complementary Cross-Coupled VCO Design

The main scope of this thesis is to test different VCO designs quantitatively and observe the trade-off between *the tuning range* and *phase noise* of a VCO. These two properties are important performance metrics for an oscillator, in addition to DC power consumption and the center frequency of oscillation, which are kept constant in this context. For this purpose, we propose four different VCO designs with minimal topological variations. These variations are present in the frequency-selective networks of the VCOs, whereas the other parameters are kept the same to allow for an adequate comparison.

Therefore, four VCO devices will be designed and compared according to both these performance metrics and figure of merits (FoM's), mentioned in Sec. 1.2. (The last VCO design, VCO 3, is actually not tunable, but for the sake of completeness, it will be referred to as a VCO along with the other designs.)

3.1 Device Topology

The proposed VCO designs have a fairly simple structure consisting of two stages. The first stage is the *oscillation stage* where the oscillation is initiated and maintained by a positive feedback loop, whose operation principle is elaborated in the diagram in Fig. 1.1. It is followed by a *buffer stage* that allows the devices to drive a 50 Ω load without any disturbance of the oscillation signal and its frequency. The relation of these stages is shown in Fig. 3.1, along with control inputs and output signals.

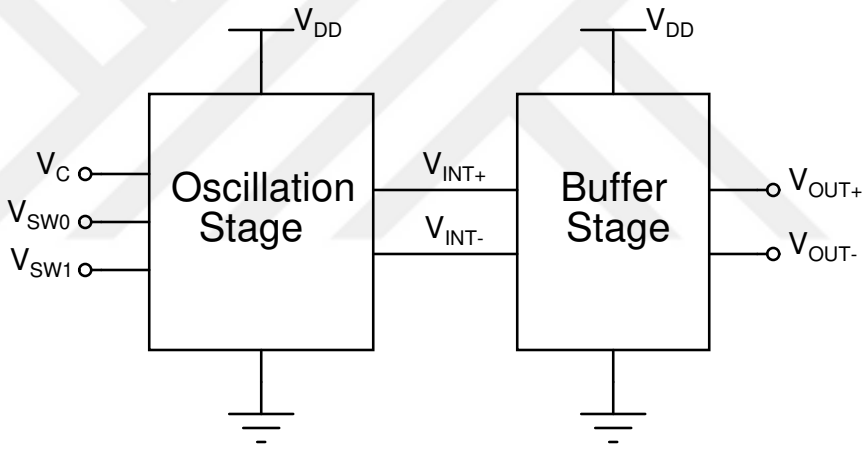


Figure 3.1: Block diagram of the VCOs

Topology-wise, the VCO designs are based on a complementary cross-coupled CMOS structure, which generates two oscillations at its opposite arms. These arms are connected to two buffers that drive the aforementioned loads. Subtraction of the output signals allows us to obtain a differential output signal. The schematic in Fig. 3.2 presents the common topology of four designs. However, the number of control inputs varies between the designs.

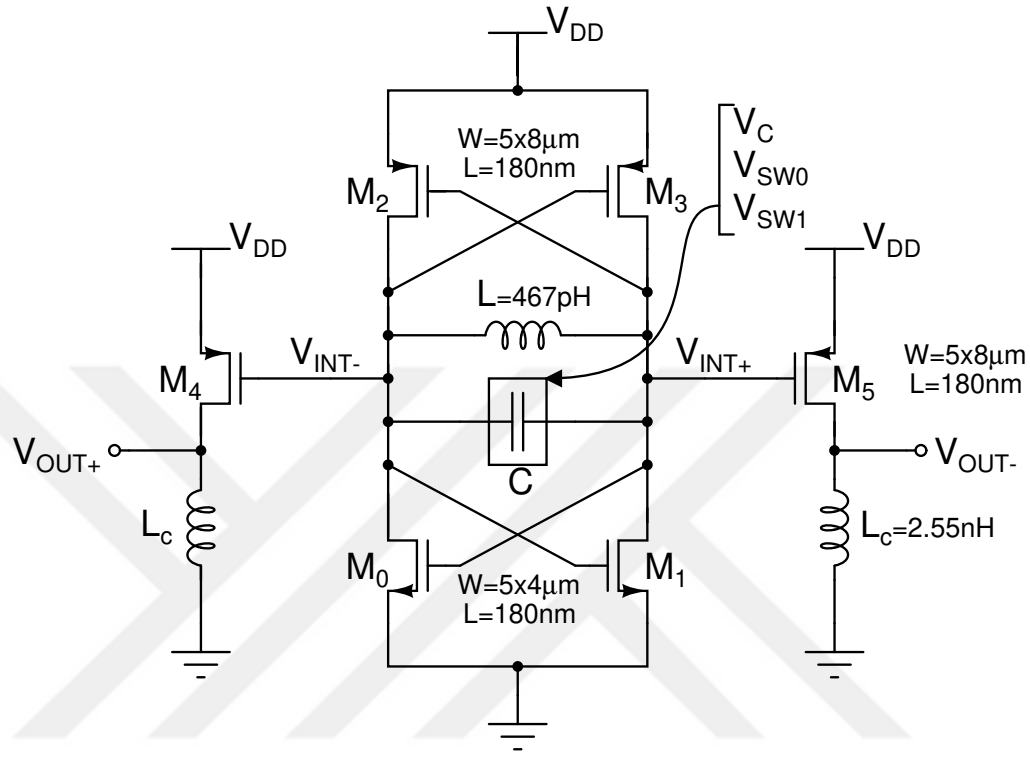


Figure 3.2: Overall schematic of the VCOs

3.1.1 Oscillation Stage

As with all oscillators, this stage consists of an amplifier and a resonator connected in a positive feedback loop. Being fed only a DC supply voltage, the amplifier does not amplify any external signal. Instead, the noise present inside the circuit is amplified at every cycle. The resonator, consisting of an LC circuit, acts as a frequency-selective network (in other words, a filter) that allows the signal to grow in a single frequency. The oscillation grows until the amplifier transistors saturate. Fig. 3.3 shows its topology. This stage cannot drive a 50 Ω load on its own, as connecting a load directly to this stage would increase frequency pulling and many cause unwanted variations in oscillation frequency.

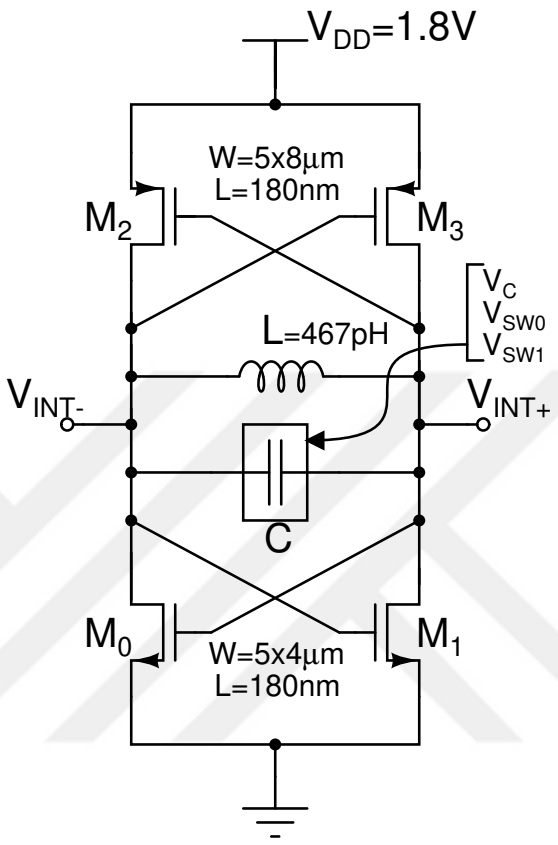


Figure 3.3: Schematic of the oscillation stage

The complementary cross-coupled structure offers several advantages over ordinary cross-coupled VCOs that utilize either NMOS or PMOS amplifiers, as discussed in Sec. 1.1. The use of NMOS and PMOS transistors in its structure allows the oscillation stage to keep its common-mode output signal (DC values of V_{INT+} and V_{INT-}) at approximately half of the supply voltage, without using a current mirror. The common mode signal being kept close to $V_{DD}/2$ yields a better oscillation swing. Furthermore, it eliminates the need to include a DC bias circuit for the buffer stage, since the DC voltage of $V_{DD}/2$ provides a sufficient bias. Therefore, including DC block capacitors is not needed.

Since the resonator contains perhaps the most important components in a VCO, the following subsections discuss how its inductive and capacitive parts are built.

3.1.1.1 Inductor Specifications

The inductive part of the resonator is fairly simple and consists of a single-turn (single-winding) symmetric spiral inductor given in Fig. 3.9. It is generated with the inductor utility provided with TSMC's PDK. The four VCO designs use the same inductor, the parameters of which are given in Table 3.1. Using the s-parameter analysis method, we can compute its inductance and quality factor throughout a frequency band, as shown in Fig. 3.4.

Parameter	Value
Type	Sym. spi. ind.
Shape	Octagon
Outer diameter	360μm
Track width	30μm
Inner radius	110μm
Number of windings	1
Guard ring distance	40μm
Inductance (@10GHz, Diff.)	467pH
Q factor (@10GHz, Diff.)	22.3

Table 3.1: Specifications of the inductor in the oscillation stage

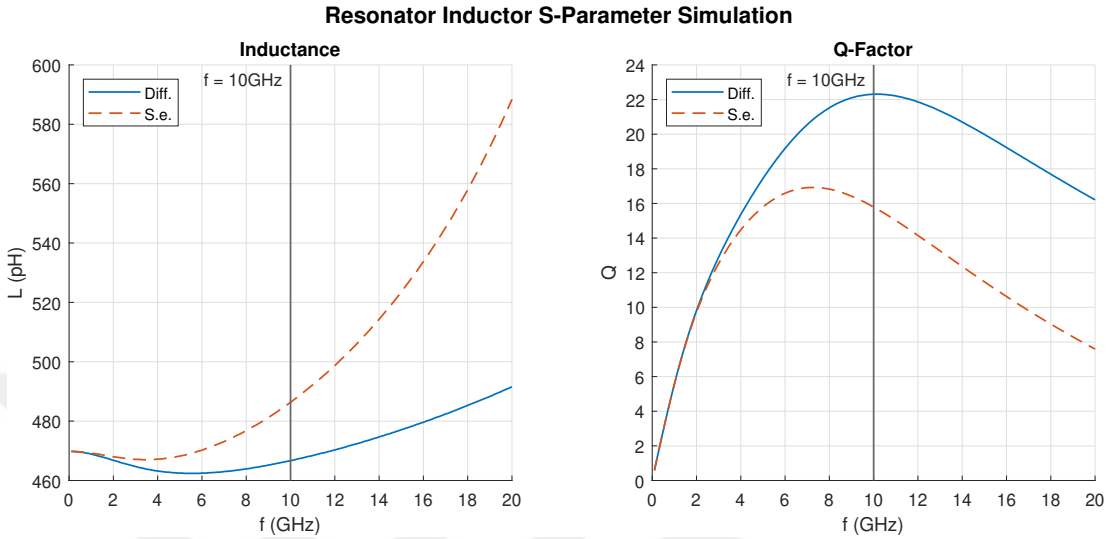
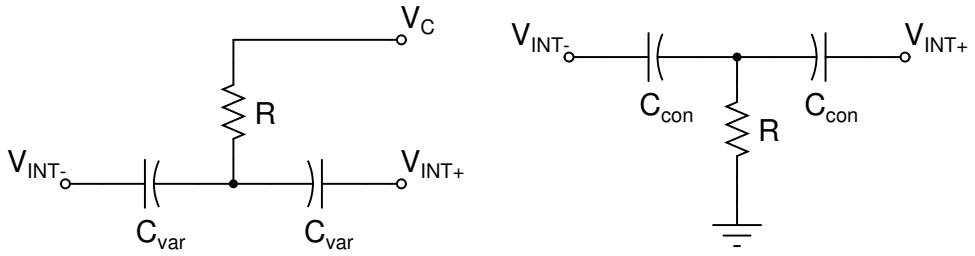


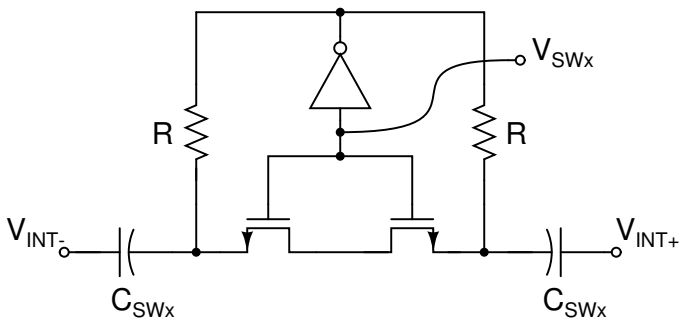
Figure 3.4: Inductance and Q-factor of the inductor in the oscillation stage

3.1.1.2 Capacitor Specifications

The capacitor in Fig. 3.3 does not represent a single capacitor but a combination of varactors, constant capacitors, and switched capacitors that allow tunability for our VCO designs. This is the part that also provides design variation between the four VCO designs. Fig. 3.5 shows general representations (without specific component parameters) of these networks, respectively.



(a) Varactor block (b) Constant capacitor block



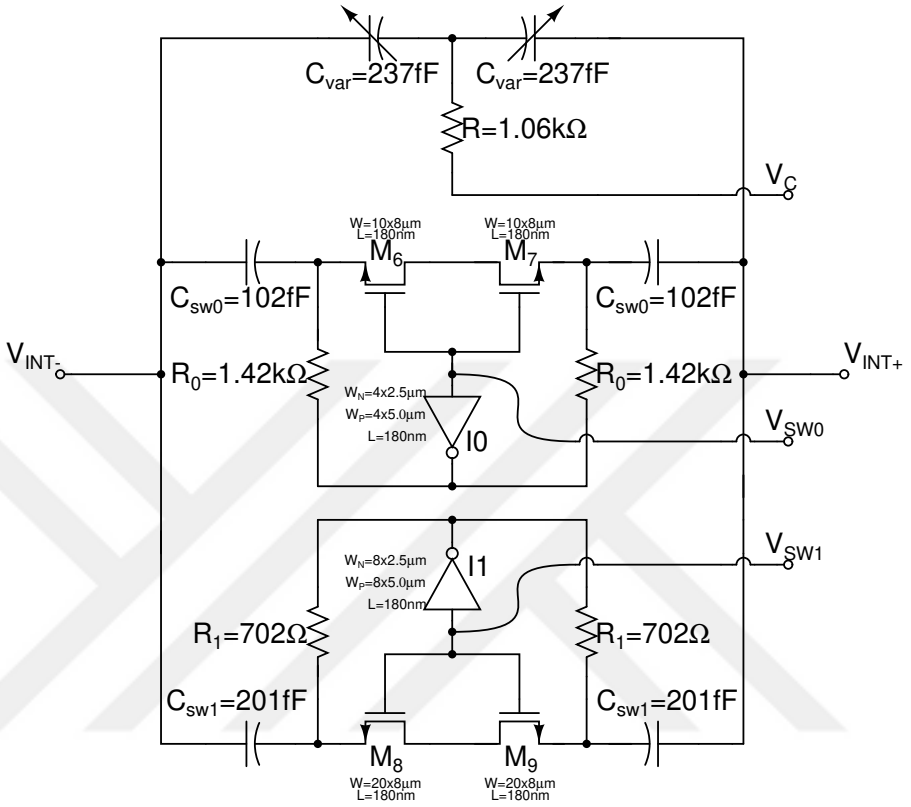
(c) Switched capacitor block

Figure 3.5: Schematics of capacitive network blocks used within VCO resonators

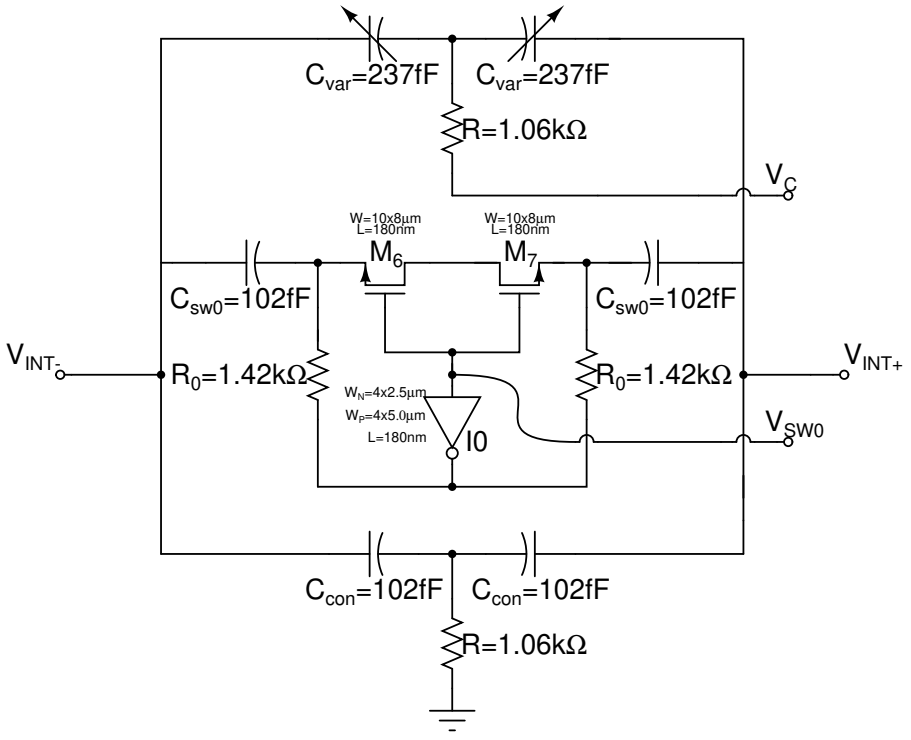
Table 3.2 below presents the combination of these capacitive networks that each VCO uses, with the specific parameters of the capacitors specified. Detailed schematics of the capacitive networks utilized in each VCO are also shown in Fig. 3.6.

VCO #	C_{var}	C_{con}	C_{SW0}	C_{SW1}
0	237fF	-	102fF	201fF
1	237fF	102fF	102fF	-
2	237fF	171fF	-	-
3	-	320fF	-	-

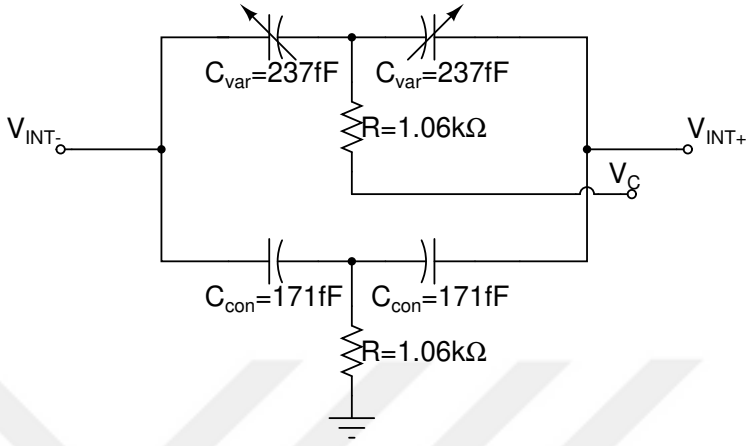
Table 3.2: Parameter values of capacitive networks within each VCO



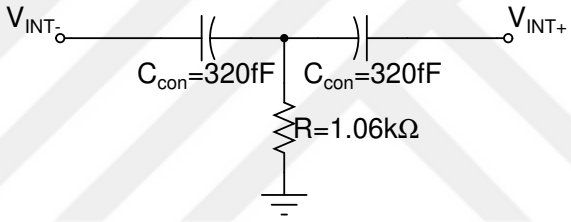
(a) VCO 0 cap. network



(b) VCO 1 cap. network



(c) VCO 2 cap. network



(d) VCO 3 cap. network

Figure 3.6: Detailed capacitive network schematics of the VCO's

3.1.2 Buffer Stage

The oscillation frequency of a VCO is not only dependent on its resonator's LC parameters but on all parasitic components inside the feedback loop. Thus, gate capacitances of amplifiers' transistors and inductances of metal tracks contribute. As a result, a load cannot be directly connected to the oscillation stage without compromising the tuning of the VCOs. Any load capacitance (or inductance) will adjust the oscillation frequency to a new value. To solve this issue, adding a buffer stage between the oscillation stage and the load is necessary, which provides isolation between them. It also provides protection against frequency pulling caused by impedance variations in load. Although gate capacitances of the transistors in the buffer stage contribute to the oscillation frequency; the extent of this contribution is known, and the oscillation stage is designed accordingly.

The buffer stage consists of only a transistor with an RF choke inductor connected to its drain. This structure is repeated for both outputs of the oscillation stage for differential operation. The input of the buffer stage comes from the oscillation stage and is given to the gate of the transistor. The output is taken from the drain.

There are two ways to realize this stage; either with an NMOS transistor or a PMOS transistor. Advantages of realization with NMOS transistors include increased output power with a smaller form factor, whereas, with PMOS transistors, it yields lesser phase noise. For our purposes, this stage is realized with PMOS transistors as shown in Fig. 3.7. The sources are directly connected to the supply and the drains are connected to the choke inductors. The other ends of the inductors are grounded.

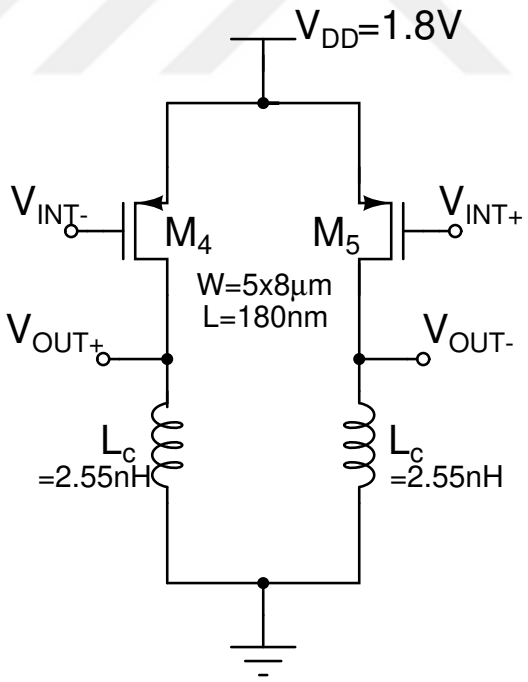


Figure 3.7: Schematic of the buffer stage

The RF choke inductors utilized in this stage are asymmetric spiral inductors, the layouts of which are shown in Fig. 3.12. The inductor utility of TSMC's PDK is again used to generate it, the parameters of which are given in Table 3.3. Its inductance and quality factor can be computed using s-parameter analysis throughout a frequency band, as shown in Fig. 3.8.

Parameter	Value
Type	Asym. spi. ind.
Shape	Octagon
Outer diameter	121μm
Track width	3μm
Track spacing	2μm
Inner radius	30μm
Number of windings	4.25
Guard ring distance	10μm
Inductance (@10GHz, S.E.)	2.55nH
Q factor (@10GHz, S.E.)	10.3

Table 3.3: Specifications of the inductor in the buffer stage

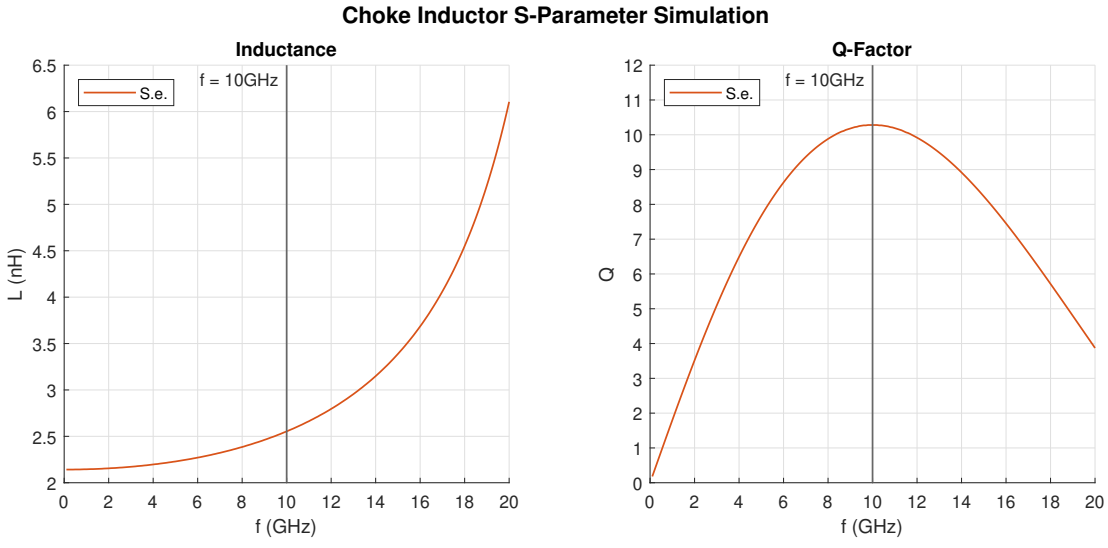


Figure 3.8: Inductance and Q-factor of the inductor in the buffer stage

3.2 Design Layout

Schematic design is followed by its translation to the layout. The layout of an IC is the closest form of abstraction from an actual IC since it features all the component coordinates, interconnections, orientations, and many other features that cannot be included in a schematic. Lithographic layers in an IC layout describe to a foundry how that device should be fabricated.

Since our designs are cross-coupled differential VCOs, all four individual devices have to be designed symmetrically. Maintaining symmetry yields far fewer mismatch issues. (DC devices and connections are excluded from this rule.) During the design, the oscillation stage is built first, and two arms of the buffer stage are placed on both sides. From these sides, final outputs are taken. When individual VCO designs are complete, they are distributed to the four corners of the IC and surrounded by an IO ring, which provides a connection between the IC core and the outside world. Other ends of IO ring elements are connected to pads, on which wire bonds should be made. Details of layout design procedures are discussed in the following subsections. Layouts have been initially drawn with Cadence Virtuoso and rendered again in KLayout software. (All the layouts presented in this section, aside from Fig. 3.14, use the color-layer matching shown in the legend in Fig. B.1.)

3.2.1 Key Components

At the beginning of drawing a VCO layout, the LC resonator inductor is placed first, and its axis of symmetry is taken as the axis of symmetry of the entire VCO device. Its layout is shown in Fig. 3.9. Metal tracks are extended from both ports so that gain transistors, capacitive networks, and buffer transistors can be connected. These metal arms are named V_{INT+} and V_{INT-}, corresponding to intermediate nets (as shown previously in Fig. 3.3).

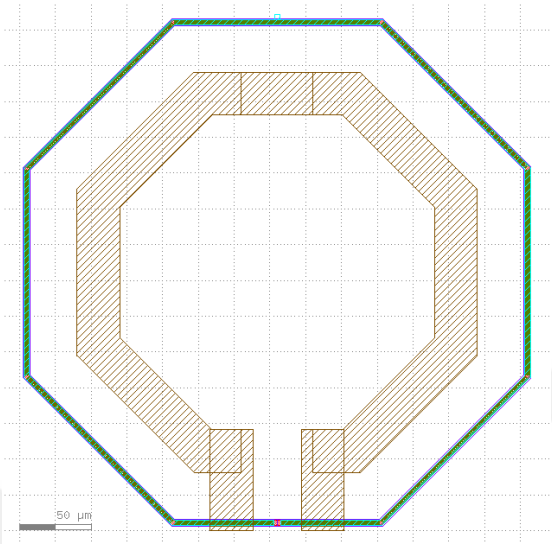


Figure 3.9: Layout of the inductor utilized in the oscillation stage

Gain transistors are placed next, surrounded by the aforementioned metal arms to which drains are connected. Their gates are connected to the opposite arm, forming a cross-couple. Their sources are connected to either V_{DD} or GND, depending on transistor types (as complementary cross-coupled VCO's include both types of transistors). The structure of this gain network is presented in Fig. 3.10.

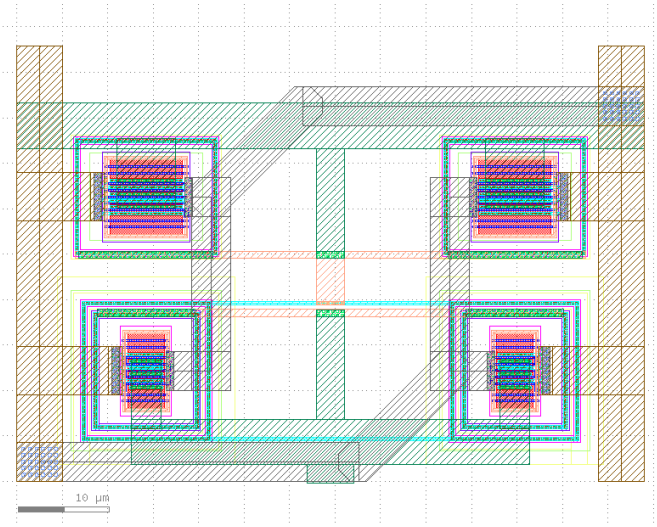
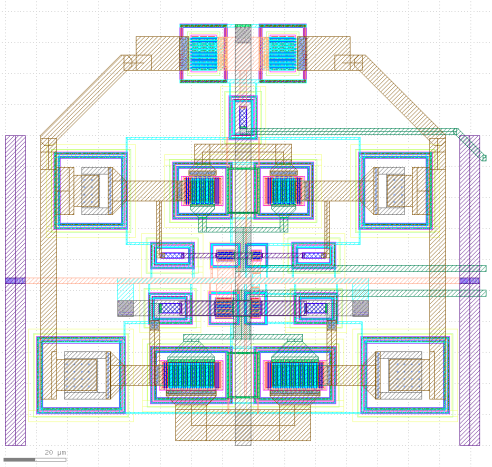
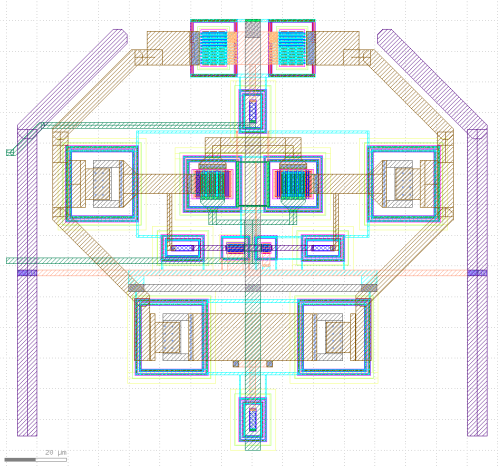


Figure 3.10: Layout of the gain network, consisting of cross-coupled transistors

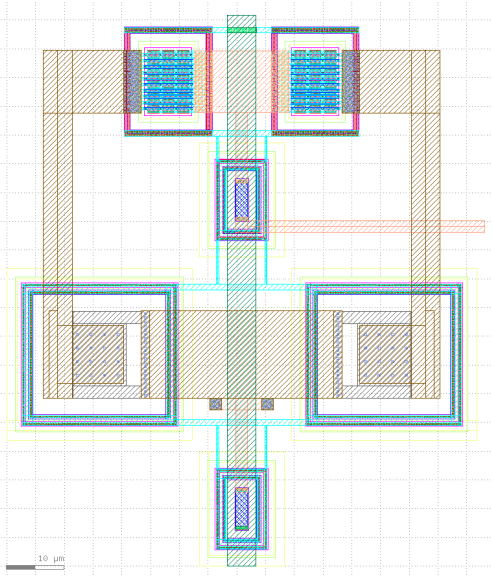
The arms of intermediate networks are extended further down to connect the capacitive networks. The orientation and order of these networks are edited so that the chip area is utilized efficiently. Their layouts are presented in Fig. 3.11 for each VCO.



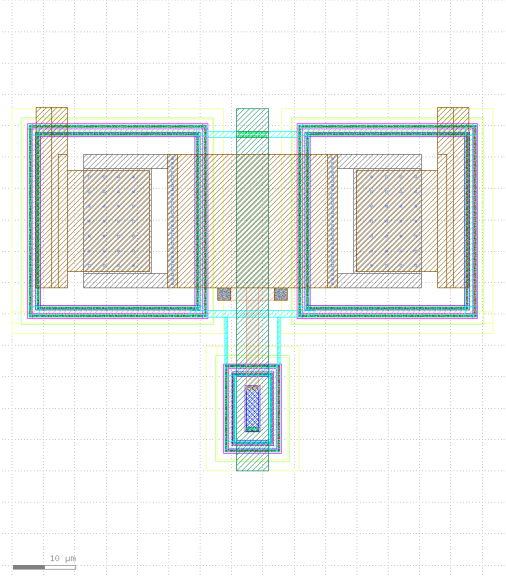
(a) VCO 0 (varactor & two switched cap.)



(b) VCO 1 (varactor, switched cap. & constant cap.)



(c) VCO 2 (varactor & constant cap.)



(d) VCO 3 (constant cap. only)

Figure 3.11: Individual layouts of capacitive networks utilized in each VCO

In the end, buffer transistors are added to the other sides of the metal arms, with their gates connected to them. Their sources are connected to V_{DD}, as they are PMOS devices, whereas their drains are connected to GND through RF choke inductors on either side, as elaborated in Fig. 3.7. The layout of one end of this part is shown in Fig. 3.12. Since the other is its symmetric counterpart, its image is redundant. (One center-tapped symmetric inductor could have been used instead of two inductors, with the center tap connected to the ground. However, this approach proved to be too area-inefficient.)

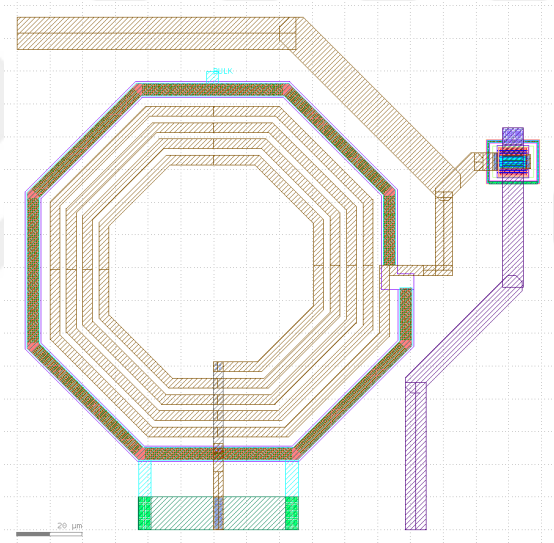


Figure 3.12: Layout of one half of the buffer stage

3.2.2 VCO Devices and IC Core

Using the flow described in Sec. 3.2.1, four VCO devices have been constructed. The first two devices, VCO 0 and VCO 1, consume 390×575 μm^2 chip area; the latter two, VCO 2 and VCO 3, consume 390×530 μm^2. Their finalized layouts are given in Fig. B.2 in Appendix B. The entire layout of the core is given in Fig. 3.13, which takes 1185×1185 μm^2 chip area.

Before moving on to the addition of the IO ring and the bond pads, the empty areas inside the core are filled with dummy capacitors, with both terminals connected to the ground. Doing so allows us to satisfy one of the density requirements dictated by the foundry. In the middle of the IC, a logo composed of top metal is inserted as a fabrication requirement. The logo is chosen as my initials and the month/year when the design is finalized.

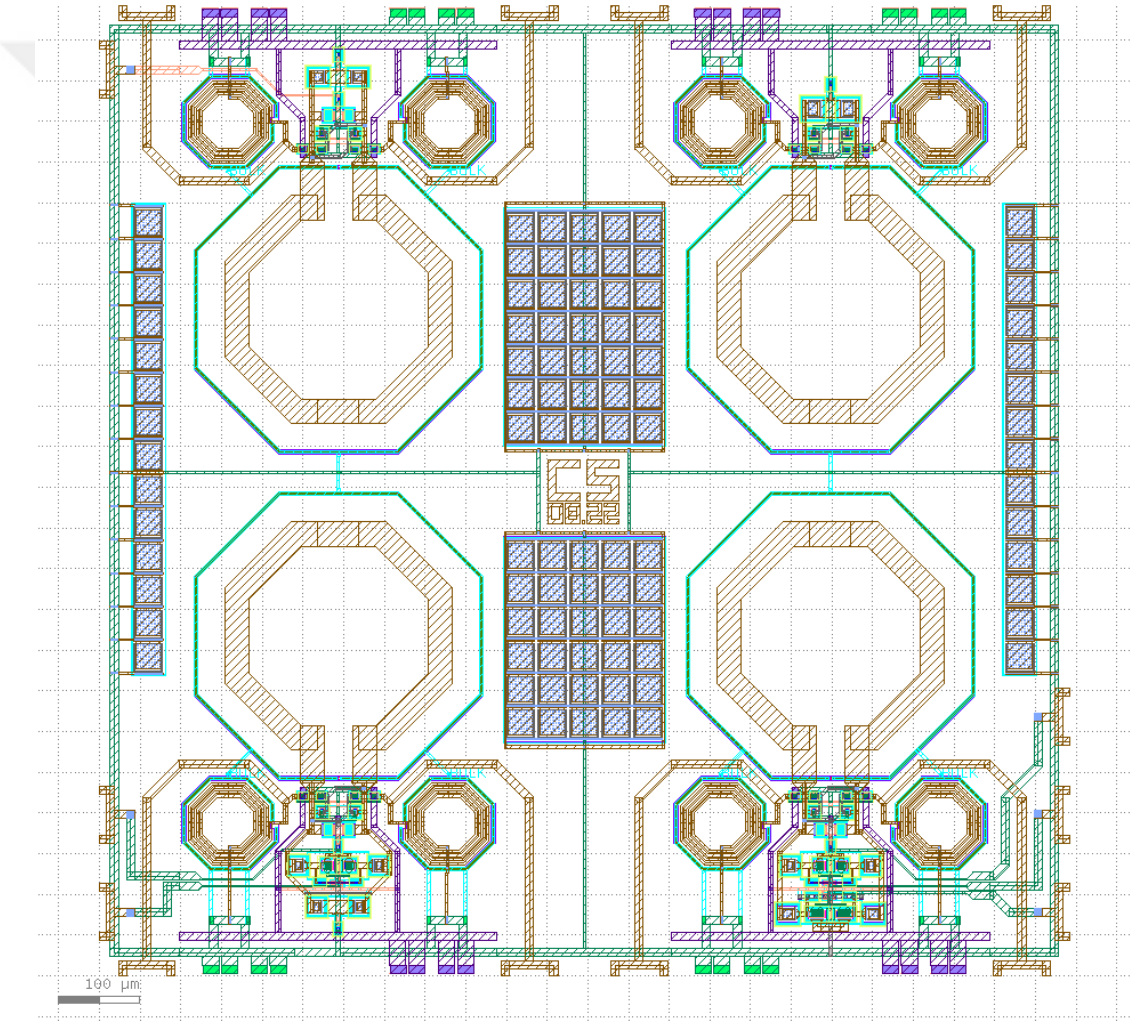


Figure 3.13: Layout of the oscillator IC core

3.2.3 IO Ring and Bond Pads

In order to be able to connect the IC core with the outside world, the IO and pad components need to be inserted. The IC core discussed in Sec. 3.2.2 is surrounded by an IO ring that consists of ring components that connect the analog I/O signals, power, and ground. In between these components, fillers are inserted, which simply fill the gaps between them. Since electrical isolation is important for the performance of each VCO, cutting blocks are inserted between each IO ring section corresponding to different VCOs. Lastly, since our IC only works with $V_{DD} = 1.8$ V supply voltage, clamp blocks are added between the supply and ground blocks so that the supply voltage is clamped above 1.8V, thus adding a level of supply protection.

(Due to requirements set for this 0.18 μm process by TSMC, IO rings cannot be fully composed of analog IO blocks. Therefore, some digital IO ring elements and pads were added according to these preset requirements, with the intention of them being connected to the ground. Nevertheless, they can also be left open, which is what was done during wire bonding..)

In the end, these IO ring blocks are connected to the bond pads. Since the largest sizes of compatible bond pads were 50×100 μm, pairs of pads were utilized for each input or output for easier wire bonding. Low capacitance pads, with 100 fF for each, are used for control inputs and RF outputs. Since they are utilized in pairs, this results in 200 fF for each connection. (Power and ground pads possess a higher capacitance of 300 fF each, 600 fF in total.)

Before finalizing the layout, dummy diffusion and metal layers are added to satisfy their density requirements. The finalized layout of our oscillator IC design is provided in Fig. 3.14, in which the IO ring components and the fillings are rendered. (Layer colors are different from the layouts in previous sections, as this figure was rendered by Europractice.)

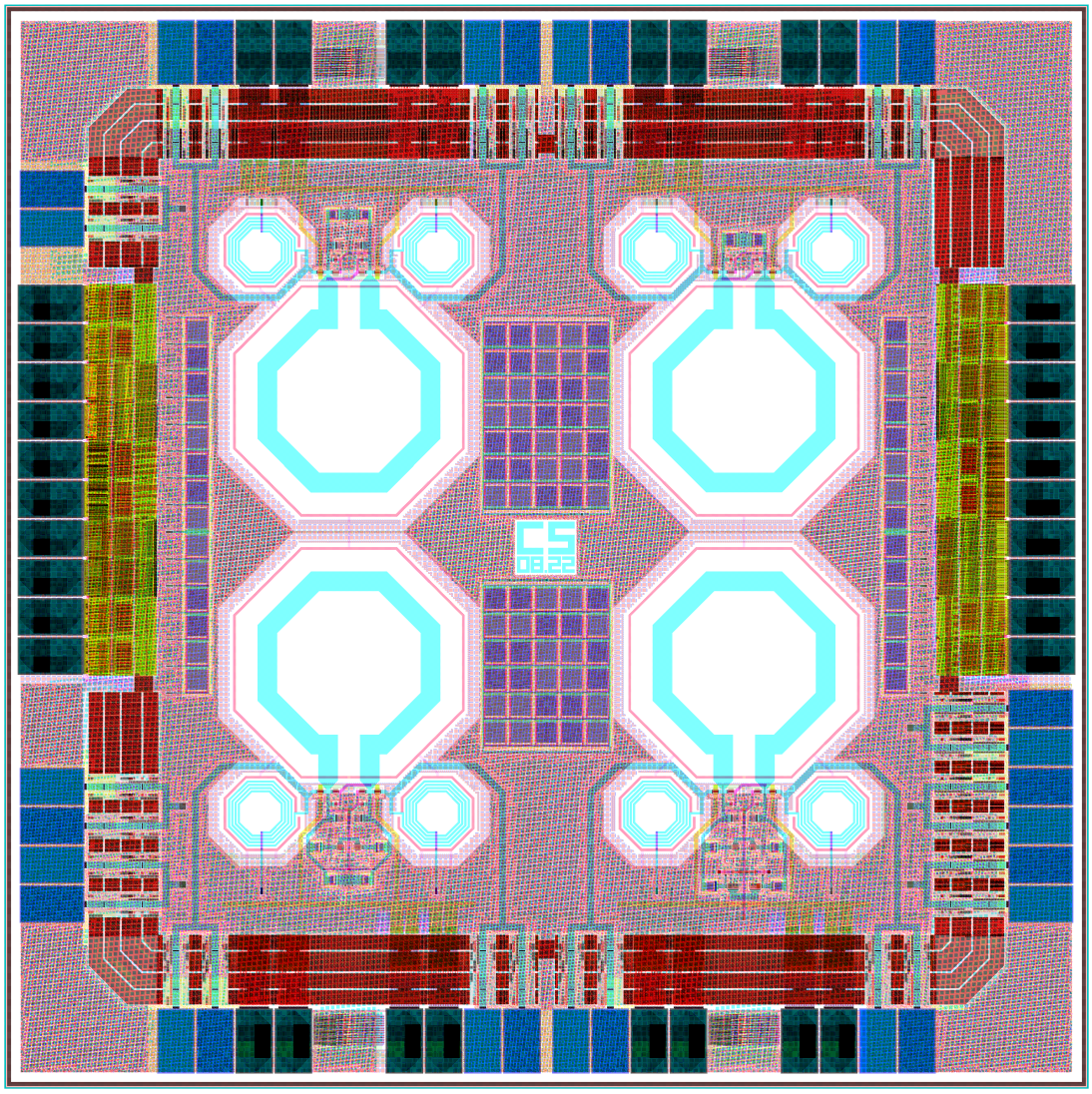


Figure 3.14: Layout of the whole oscillator IC

3.3 Simulation Results

The simulation results of the four different VCOs will be discussed and compared in this section. As mentioned earlier, these four devices vary in tuning range, but in return have improved phase noise properties. All results in this section are obtained from either harmonic balance simulations or noise simulations consecutive to the said harmonic balance simulations. The testbench setup shown in Fig. 3.15 is used. Simulated circuits (shown as the component named "VCO") are post-layout circuits extracted from the layouts (in Sec. 3.2) with Cadence Assura parasitic extraction tool. Simulations themselves are performed using Cadence Spectre simulation software. Due to the test setup mentioned in Chap. 4 having single-ended outputs for each VCO, and measurements in the said chapter are carried out according to this; simulations are also performed on only one of the differential outputs. However, the simulation results of the differential outputs are presented in Appendix A.

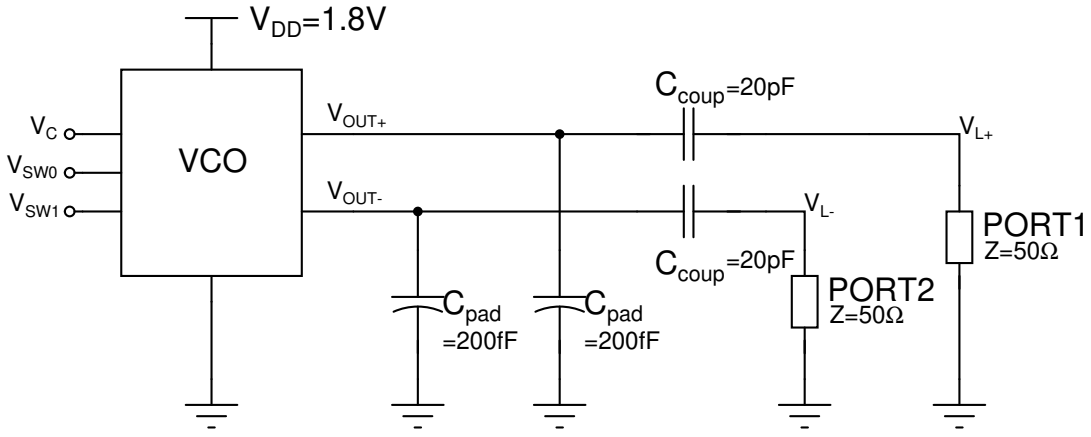


Figure 3.15: Testbench setup used in VCO simulations

3.3.1 Harmonic Balance Analysis

Results in Fig. 3.16 present the frequency coverage of the four VCO devices with respect to the control voltage. Control voltage V_C is the tuning input applied to the varactor inside the LC tanks. Different curves within one graph represent different frequency coverage achieved by turning the switched capacitor networks on and off. (VCO 2 does not utilize any switched capacitor and is based only on a varactor. VCO 3 does not utilize any form of tunable capacitors whatsoever, and is named "VCO" only for the sake of completeness.) The relationship between the control voltage and resulting frequency shows some nonlinearities, especially at the end points of the plots, but it is still monotonic.

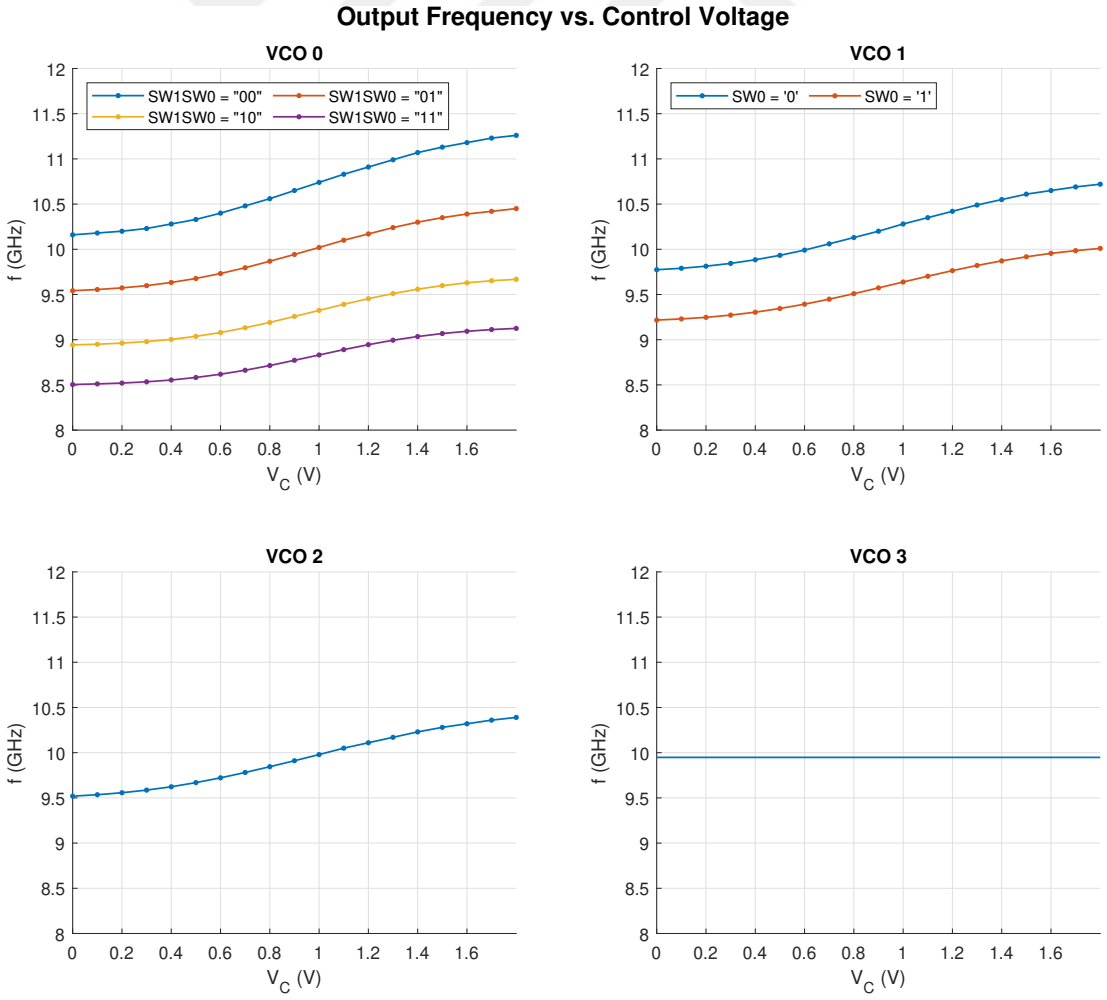


Figure 3.16: Output frequency vs. control voltage simulations

The results in Fig. 3.17 indicate the output power (with 50 Ω load) and the corresponding output frequency at fundamental. As expected, losses introduced by turning on switched capacitors result in lower output power, which is observable for the first two oscillators. This outcome is one of the trade-offs to achieving better frequency coverage. Furthermore, each point in the graphs represents a data point obtained by sweeping control voltage V_C in increments of 100 mV. Therefore, the plots also indirectly show the nonlinearity between the control voltage and the corresponding output frequency. Moreover, the VCOs produce second and third order harmonics, simulation results of which are shown in Table 3.4 for $V_C = \{0, 0.9, 1.8\}$ V and for all switch combinations. The highest harmonic power value for each VCO is indicated.

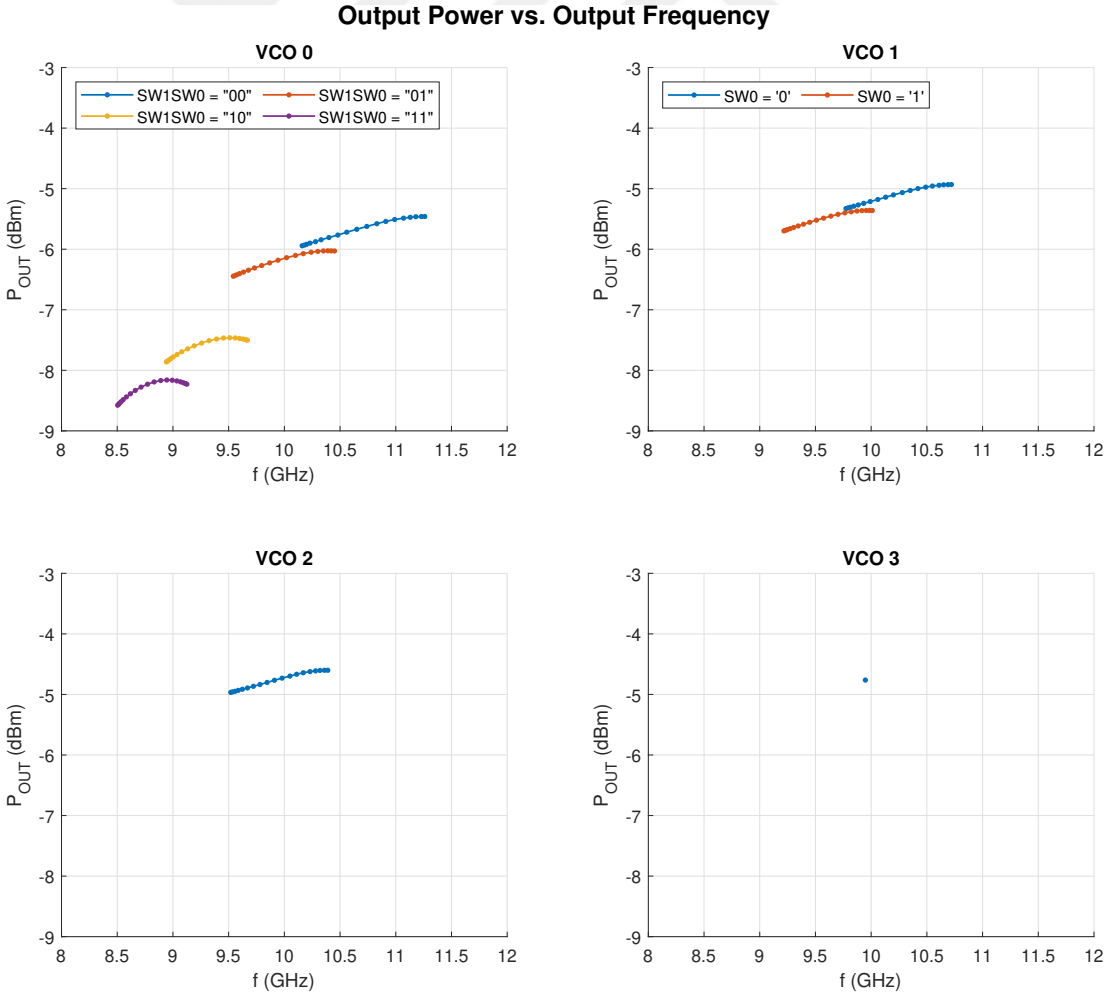


Figure 3.17: Output power vs. output frequency simulations

$SW1SW0$	V_C (V)	f_{out} (GHz)	P_{out} (dBm)	G_2 (dBc)	G_3 (dBc)
	0	10.16	−5.943	−16.36	−24.58
"00"	0.9	10.65	−5.671	−15.39	−24.51
	1.8	11.26	−5.460	**−14.85**	−21.54
	0	9.543	−6.447	−17.46	−26.16
"01"	0.9	9.944	−6.182	−16.62	−26.09
	1.8	10.45	−6.025	−16.33	−23.17
	0	8.942	−7.860	−19.79	−28.94
"10"	0.9	9.257	−7.549	−19.02	−28.58
	1.8	9.668	−7.502	−19.05	−26.07
	0	8.504	−8.575	−20.89	−31.14
"11"	0.9	8.772	−8.229	−20.14	−30.67
	1.8	9.125	−8.231	−20.26	−28.70

(a) VCO 0

$SW0$	V_C (V)	f_{out} (GHz)	P_{out} (dBm)	G_2 (dBc)	G_3 (dBc)
	0	9.774	−5.328	−15.93	−24.47
'0'	0.9	10.20	−5.103	−15.11	−24.41
	1.8	10.72	−4.932	**−14.85**	−21.60
	0	9.217	−5.697	−16.70	−25.73
'1'	0.9	9.573	−5.487	−15.99	−25.68
	1.8	10.01	−5.361	−15.88	−23.19

(b) VCO 1

V_C (V)	f_{out} (GHz)	P_{out} (dBm)	G_2 (dBc)	G_3 (dBc)
0	9.519	−4.966	−16.00	−25.56
0.9	9.911	−4.766	**−15.02**	−26.13
1.8	10.39	−4.601	−15.19	−23.33

(c) VCO 2

f_{out} (GHz)	P_{out} (dBm)	G_2 (dBc)	G_3 (dBc)
9.948	−4.763	**−15.57**	−24.37

(d) VCO 3

Table 3.4: Harmonic power simulations

The data in Tables 3.5 and 3.6 present the results of the frequency pulling and frequency pushing simulations after their respective sweeps have been carried out. To observe the frequency pulling effect, the phase of the load impedance has been varied for $VSWR = 1.75{:}1$. The output frequency with the largest deviation from the ordinary oscillation frequency with 50 Ω load is subtracted from the said ordinary frequency. The overall maximum frequency pulling has been reported for each VCO. As for observing the frequency pushing effect, the supply voltage was varied for $V_{DD} = [1.7, 1.9]$ V with 0.5 V increments. The overall maximum value of derivative of the resulting output frequency vs. supply voltage plot provides the frequency pushing, which has been reported for each VCO. Both simulations are performed for $V_C = \{0, 0.9, 1.8\}$ V and for all switch combinations.

$SW1SW0$	V_C (V)	f_{pull} (MHz)
"00"	0	3.30
	0.9	4.00
	1.8	**7.00**
"01"	0	4.39
	0.9	4.06
	1.8	4.90
"10"	0	4.33
	0.9	4.50
	1.8	2.93
"11"	0	4.59
	0.9	4.94
	1.8	3.62

(a) VCO 0

$SW0$	V_C (V)	f_{pull} (MHz)
'0'	0	3.54
	0.9	2.70
	1.8	**5.30**
'1'	0	3.95
	0.9	3.56
	1.8	3.00

(b) VCO 1

V_C (V)	f_{pull} (MHz)
0	**3.96**
0.9	3.18
1.8	3.80

(c) VCO 2

f_{pull} (MHz)
3.08

(d) VCO 3

Table 3.5: Frequency pulling simulations

$SW1SW0$	V_C (V)	f_{push} (MHz/V)
"00"	0	-147
	0.9	**-542**
	1.8	-368
"01"	0	-121
	0.9	-463
	1.8	-289
"10"	0	-73.8
	0.9	-329
	1.8	-208
"11"	0	-59.5
	0.9	-265
	1.8	-170

(a) VCO 0

$SW0$	V_C (V)	f_{push} (MHz/V)
'0'	0	-143
	0.9	**-471**
	1.8	-326
'1'	0	-126
	0.9	-413
	1.8	-276

(b) VCO 1

V_C (V)	f_{push} (MHz/V)
0	-141
0.9	**-439**
1.8	-335

(c) VCO 2

f_{push} (MHz/V)
-134

(d) VCO 3

Table 3.6: Frequency pushing simulations

3.3.2 Noise Analysis

Followingly, phase noise simulations are performed on all four devices. Plotted relative to the oscillation frequency, the noise performance of each device is shown for all combinations of switched capacitors and for the control voltage inputs $V_C = \{0, 0.9, 1.8\}$ V. To achieve simplicity in the plots and allow for easier comparison, the geometric mean (arithmetic mean on a logarithmic scale) of the results is taken for V_C control input trios and shown as single curves in Fig. 3.18. As can be seen, phase noise performance improves as device complexity and tunability are reduced, which is the main trade-off focused on in this thesis.

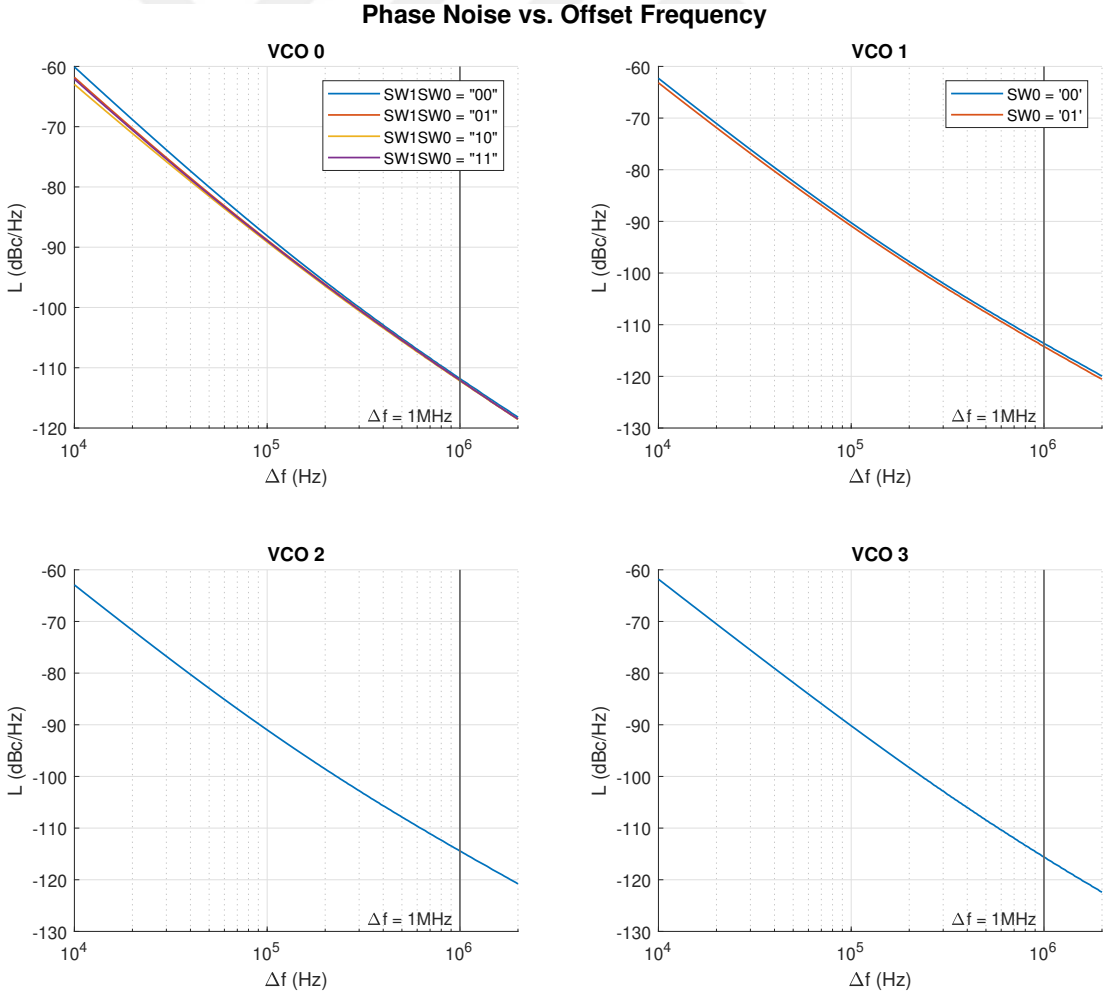


Figure 3.18: Output phase noise vs. offset frequency simulations

3.3.3 Device Performance

The results of these simulations allow us to compute the figure-of-merit and figure-of-merit with tuning range (FoM and FoM_T) parameters for the four VCOs, the formula of which are Eqs. 1.7 and 1.8 respectively. Table 3.7 presents these values, as well as some other metrics mentioned in Sec. 1.2.

VCO #	f_c (GHz)	TR (%)	P_{DC} (mW)	G_2 (dBc)	f_{pull} (MHz) @1.75:1 VSWR	f_{push} (MHz/V)	$\mathcal{L}$ @1MHz (dBc/Hz)	FoM (dBc/Hz)	FoM_T (dBc/Hz)
0	9.882	27.89	14.29	−14.85	7.00	−542	-111.5 ± 3.3	−179.8	−188.8
1	9.969	15.08	14.29	−14.85	5.30	−471	-113.5 ± 3.0	−181.9	−185.5
2	9.955	8.750	14.39	−15.02	3.96	−439	-114.2 ± 2.6	−182.6	−181.4
3	9.948	0	14.21	−15.57	3.08	−134	−115.6	−184.0	-

Table 3.7: Comparison of VCO simulation results

The results show that a center frequency of 10 GHz is achieved for all four devices. Keeping the power consumption the same for all devices as intended at 14.3 mW, it is the tuning range and the phase noise performance that are varied. The widest tuning range achieved is 27.89%, yielding a FoM_T of −188.8 dBc/Hz; whereas the lowest phase noise achieved is −115.6 dBc/Hz at a 1 MHz offset, yielding a FoM of −184.0 dBc/Hz. Moreover, the general maxima of harmonic power, frequency pulling and frequency pushing of all devices have been calculated. It is observed that simpler designs, which are less susceptible to noise, yield less frequency pulling. As for frequency pushing, not adding a tail bias has caused a significant susceptibility to supply variations for all VCOs, but it was a necessary measure to decrease the output phase noise.

3.4 Die Fabrication

The oscillator IC is realized in TSMC 0.18 μm CMOS process [18]. As mentioned priorly, the die surface area is $1660 \times 1660\mu$ m^2. A die micrograph is provided in Fig. 3.19, whereas detailed micrographs of the die are provided in Appendix C. This die will be tested and measurements will be made as described in Chap. 4.

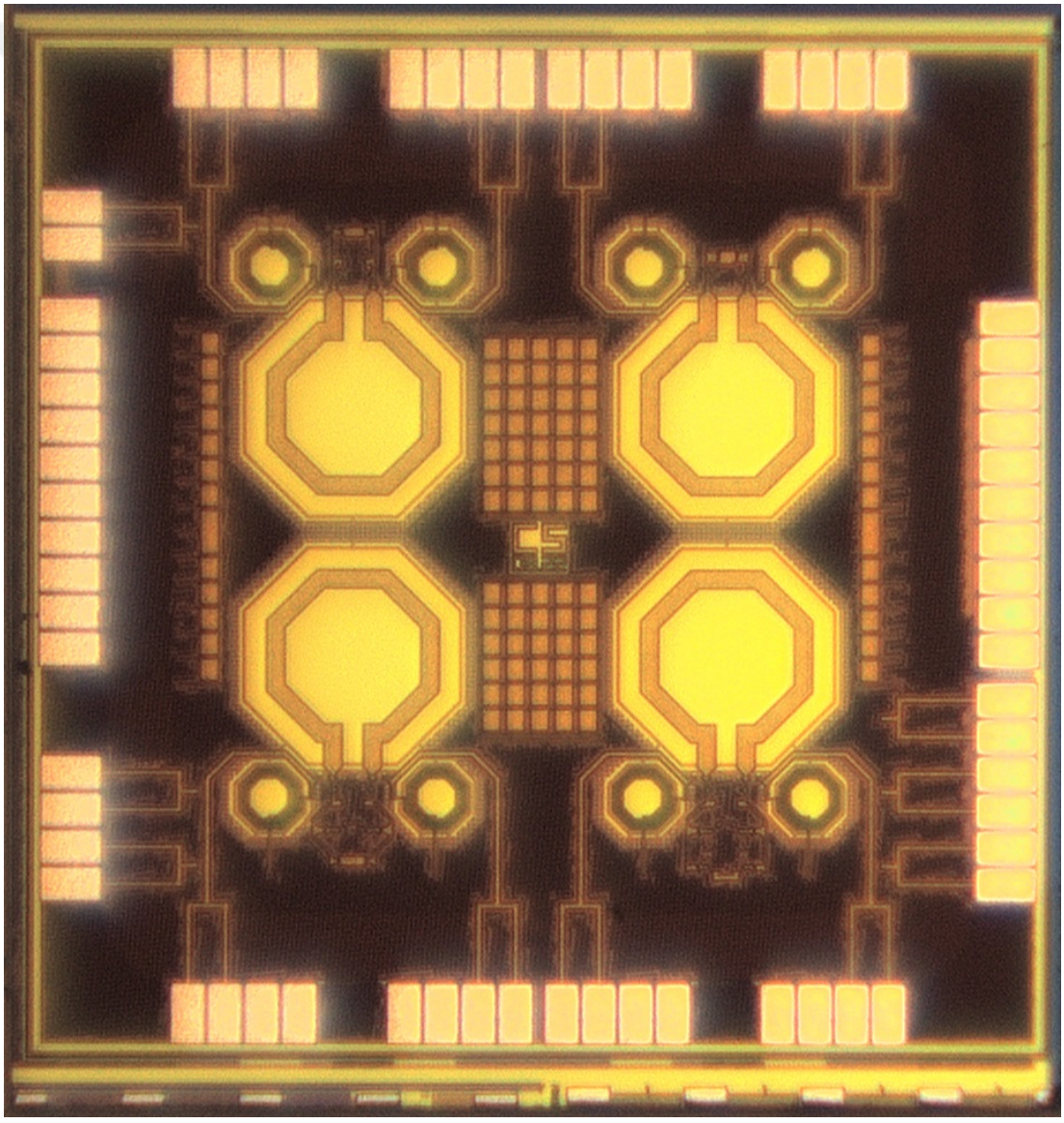


Figure 3.19: Micrograph of the oscillator IC die

Chapter 4

Measurements and Results

After the design and fabrication procedures of the oscillator IC have been completed, the final step in our research is to test the output signal characteristics of the device. An adequate measurement setup was prepared to make measurements with a minimal amount of error and with ease. Results are tabulated, plotted, and presented in the same manner as in Sec. 3.3.

4.1 Measurement Setup

The measurement setup is a system consisting of the IC itself, the test PCB (using Rogers 4350B substrate [19]) on which it will be wire bonded, an aluminum shielding box to protect the test PCB from outside interference, and a control PCB for managing DC inputs (power and control) with ease. Two DC power supplies provide the DC inputs to the control PCB whereas a spectrum analyzer is utilized to measure the outputs from the test PCB. Though briefly summarized in this section, extensive details about the design and implementation of each of the measurement setup elements are covered in Appendix D. A simplified schematic of this setup is given in Fig. 4.1.

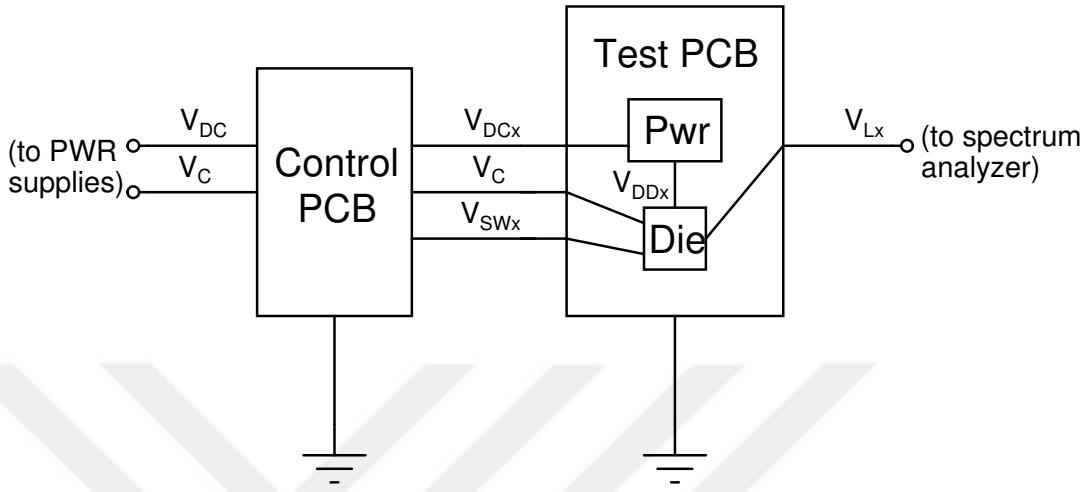


Figure 4.1: Overall schematic of the measurement setup

The first step of the preparation involves the oscillator IC being glued to the test PCB with epoxy and electrically connected to it via gold wire bonds. As using a package would cause additional parasitic components that would hinder the operation of the IC, the chip-on-board (COB) approach was followed instead. The used gold wire has 25 μm thickness so that wire bonds are made on two bond pads on the IC. The empty bond pads belong to the digital IO ring components; they were intended to be either grounded or left open. (The reason for this is elaborated in Sec. 3.2.3 in detail; there must be some digital IO components in the IO ring as a design rule set by TSMC.) An image of the die after the successful completion of these two procedures is given in Fig. 4.2.

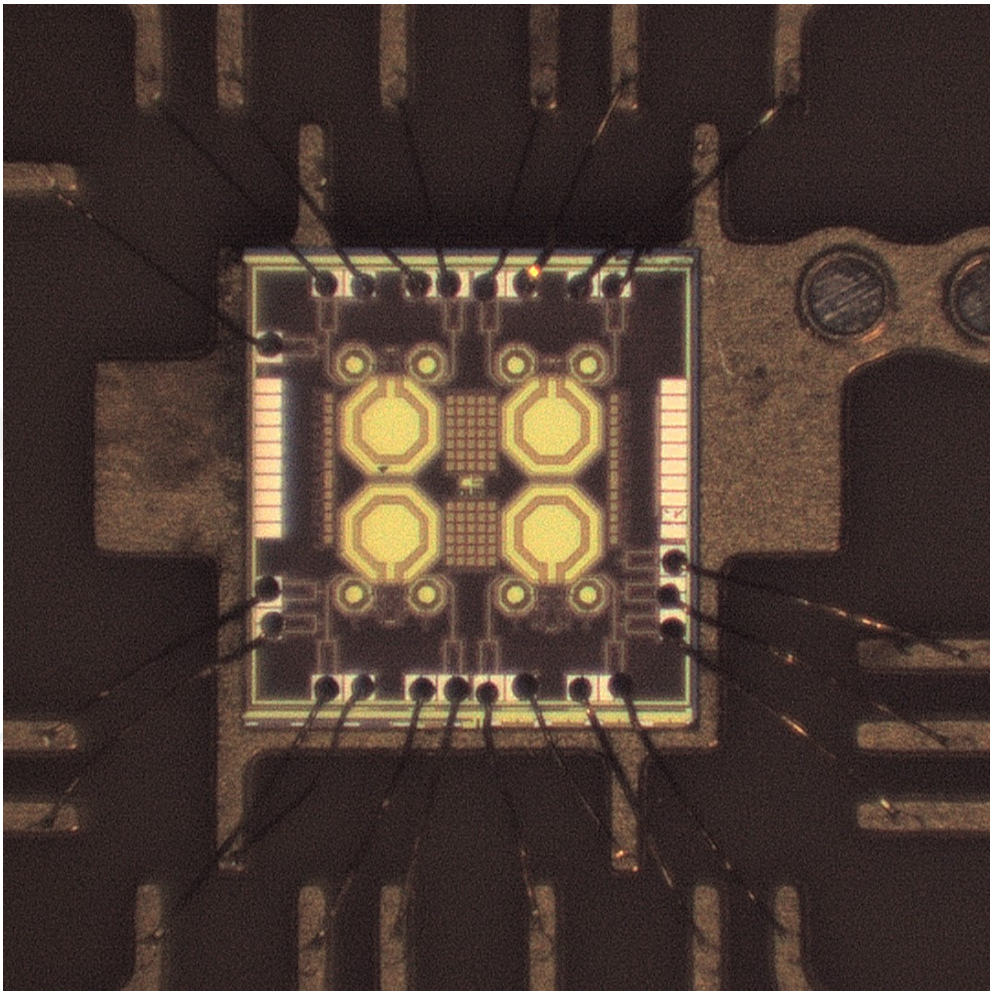
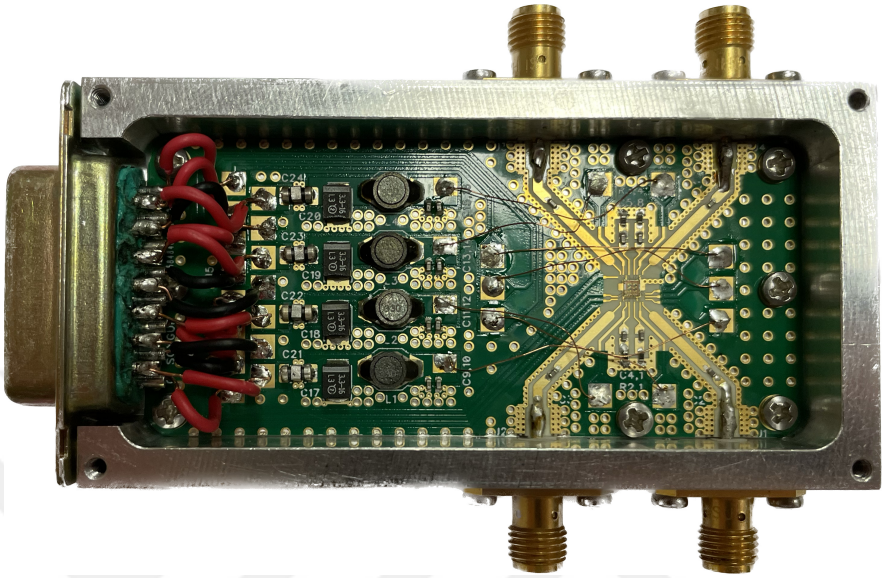


Figure 4.2: Micrograph of wire bond connections between the die and the test PCB

The test PCB with the oscillator IC, after its components were soldered, is placed inside the aluminum box, as shown in Fig. 4.3. This box provides DC control and power inputs with a 15-pin D-Sub connector while using SMA ports for the outputs. While the power inputs are met with a power circuitry consisting of feedthrough capacitors, decoupling capacitors, and RF choke inductors; control inputs are fed directly into the PCB. RF outputs are carried to the SMA connectors through 50 Ω transmission lines and decoupling capacitors. One of each differential output pair is terminated with 51 Ω load resistors.

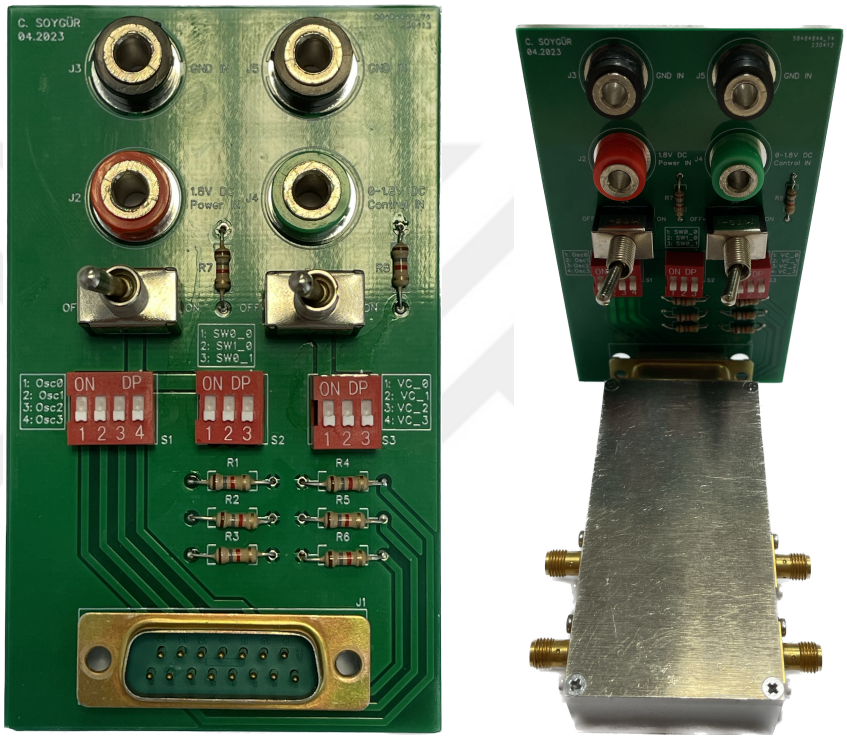


(a) Lid open

(b) Lid closed

Figure 4.3: Test PCB with the aluminum box it is placed in

The other end of the D-Sub connector is connected to a control PCB which allows for easy management of DC inputs through a series of switches so that the user can select which of the oscillators to operate and which control inputs to provide. The control PCB, along with the aluminum box, is shown in Fig. 4.4.



(a) Unconnected (b) Connected

Figure 4.4: Control PCB, with how it is connected to the box shown

This whole system (consisting of the test PCB, the aluminum box, and the control PCB) is connected to two HP E3616A DC power supplies (one providing DC power and switched capacitor inputs, another providing DC varactor control inputs) and an HP 8536A spectrum analyzer as shown in Fig. 4.5.

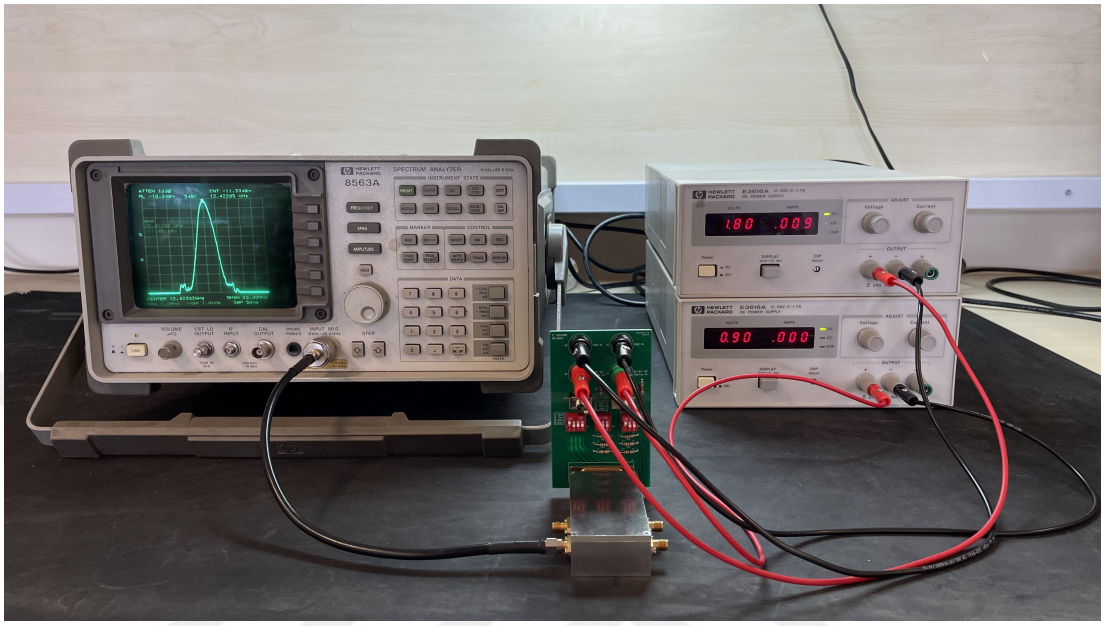


Figure 4.5: Measurement setup for testing the oscillator IC

4.2 Measurement Results

Output spectral measurements of four VCOs in the oscillator IC are presented in this section. These measurements consist of oscillation frequency (with respect to control inputs), output power, and phase noise measurements; presented in Figs. 4.6, 4.7, and 4.8 respectively.

4.2.1 Spectral Analysis

The first set of measurements aims to determine *the output power at each oscillation frequency* and *which control inputs correspond to these frequencies*. Since the combination of control inputs applied to the system is known, we can deduce which output frequencies and powers correspond to them, as the spectrum analyzer can measure both. Then the output power and the corresponding frequencies can be matched.

To be able to capture the peaks of output signals with ease when control inputs are varied, the spectrum analyzer is set to a sufficiently large span of 4 GHz and a resolution bandwidth of 1 MHz. To further make the frequency measurements more accurate, the built-in frequency counter feature of the analyzer is enabled.

The plots in Fig. 4.6 present the frequency of oscillation corresponding to the DC control inputs applied. While the x-axis corresponds to the varactor control voltage V_C, different curves represent different switched capacitor control inputs.

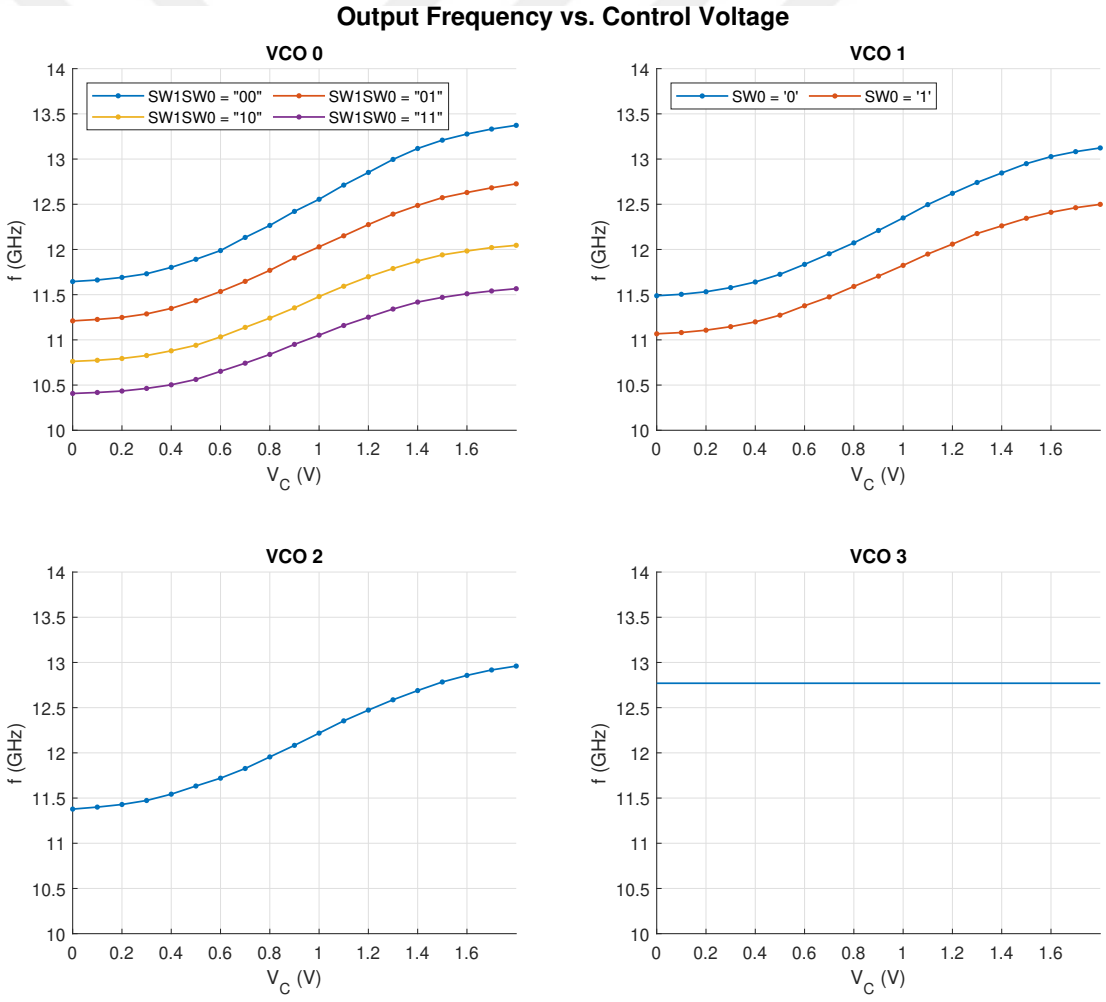


Figure 4.6: Output frequency vs. control voltage measurements

Plots in Fig. 4.7 present the output power with respect to the output frequency. Again, different curves in each graph correspond to different switched capacitor inputs, whereas each data point corresponds to 0.1 V increments of varactor control voltage V_C (the latter correspond to the same data points in Fig. 4.6).

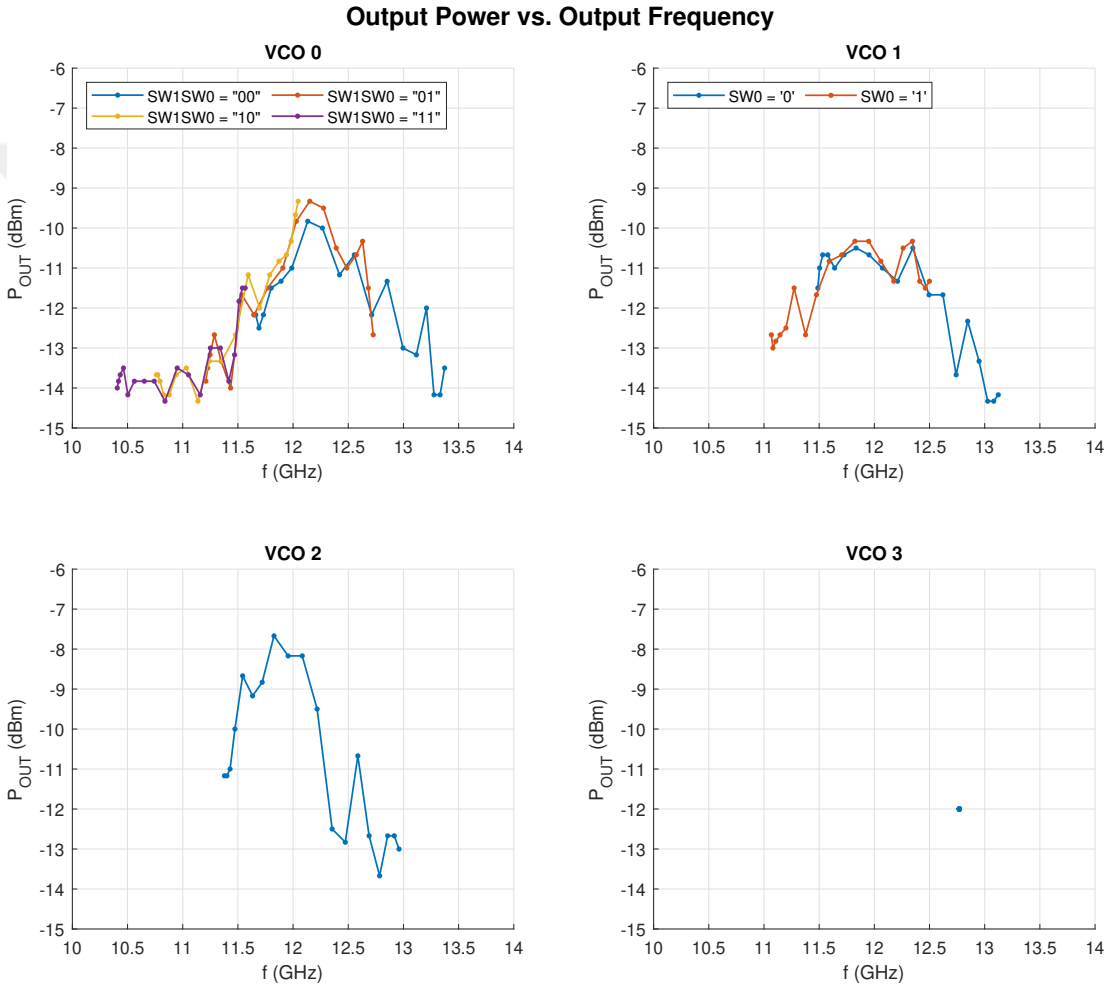


Figure 4.7: Output power vs. output frequency measurements

4.2.2 Noise Analysis

The last set of measurements aims to measure the phase noise components residing within the output signal. As elaborated in Sec. 1.2.2, phase noise is, in theory, measured per unit bandwidth. However, in reality, the available resolution bandwidth of spectrum analyzers is much larger. As such, most analyzers (including ours) include a noise marker feature that converts the bandwidth to a unit bandwidth of 1 Hz. Combined with the delta (difference) marker setting that allows us to subtract it from carrier power, we can directly measure the phase noise at certain frequency offsets. This requires a sufficient dynamic range in the spectrum analyzer so that both the carrier and the offset can be measured at the same time [20]. During the measurements the resolution bandwidth was set to 10 kHz, whereas the video bandwidth was set to 1 kHz. This yielded a noise floor as low as -86 dBm, corresponding to -126 dBm/Hz at unit bandwidth. All spectra were viewed in a 3 MHz span. (Our spectrum analyzer does not possess a built-in phase noise analysis mode, which allows for automatic offset changing and plotting. Nevertheless, manually measuring phase noise is available more often in spectrum analyzers.)

The last set of plots, in Fig. 4.8, presents the phase noise present in the output with respect to certain offset frequencies in dBc/Hz. (In fact, these measurements also include amplitude noise, but it is insignificant compared to phase noise levels [20].) The offset frequencies are relative to the carrier frequency (frequency of oscillation) and are measured with the offset frequencies increasing in a logarithmic manner. As such, plots are on a semi-log scale. Measurements are carried out for $V_C = \{0, 0.9, 1.8\}$ V and for all combinations of switched capacitors. To allow for a simpler representation of results, the geometric average of the plot corresponding to V_C trios is taken (this is equivalent to taking the arithmetic average of plots in logarithmic scale, as phase noise measurements are represented in dBc/Hz).

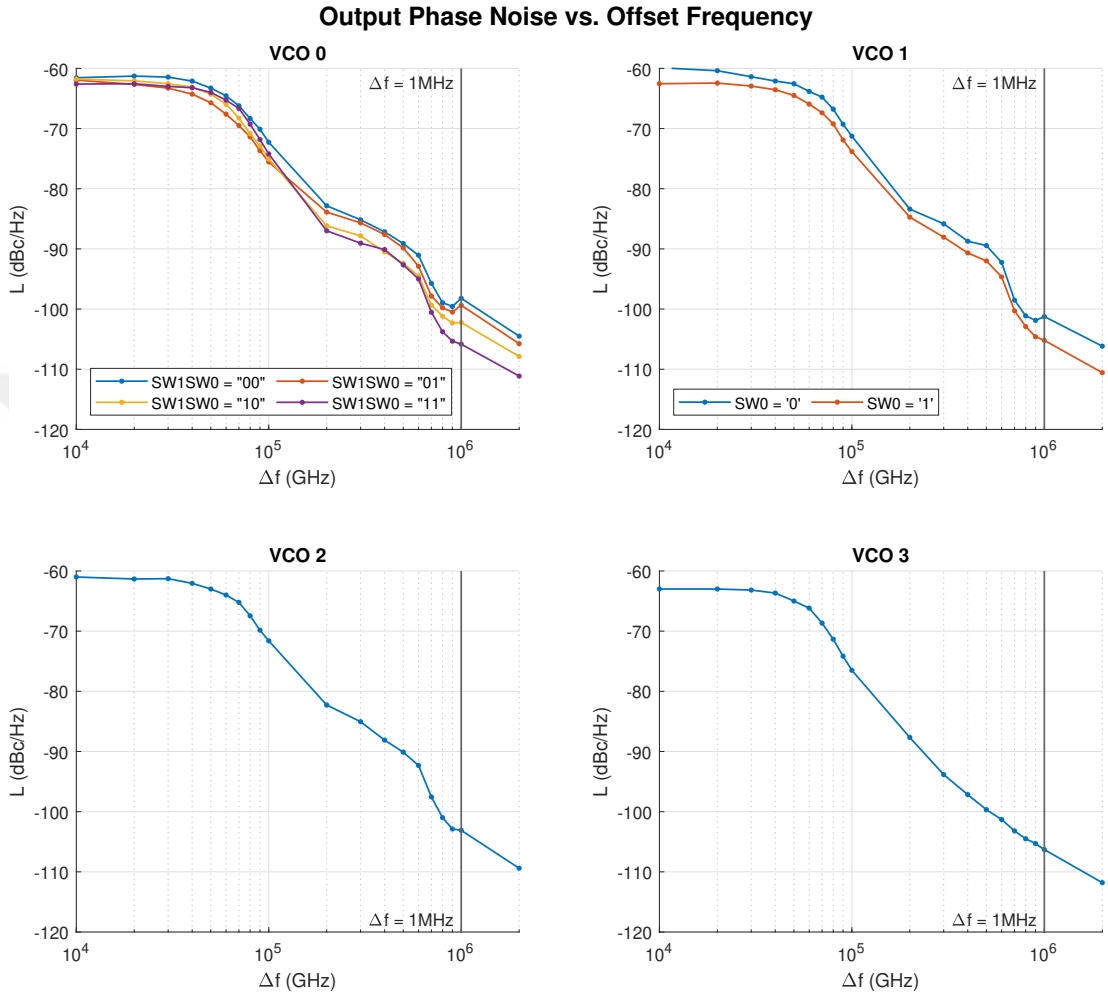


Figure 4.8: Output phase noise vs. offset frequency measurements

4.2.3 Device Performance

Using these measurement results we can compute the figure-of-merit and figure-of-merit with tuning range (FoM and FoM_T) values for the four oscillator devices, the formula of which are given in Eqs. 1.7 and 1.8. Table 4.1 presents these values along with other metrics mentioned in Sec. 1.2.

VCO #	f_c (GHz)	TR (%)	P_{DC} (mW)	$\mathcal{L}$ @1MHz (dBc/Hz)	FoM (dBc/Hz)	FoM_T (dBc/Hz)
0	11.89	24.95	18.0	-98.9 ± 10.6	-167.9	-175.8
1	12.10	17.00	18.0	-101.3 ± 7.5	-170.4	-175.0
2	12.17	13.00	16.2	-102.0 ± 6.5	-171.6	-173.9
3	12.77	0	16.2	-106.3	-176.3	-

Table 4.1: Comparison of VCO measurement results

The measurement results indicate that the center frequencies of the devices vary from each other. The power consumptions of the devices are almost identical as expected, which is 17 mW on average. The highest achieved tuning range is 24.95%, while the best phase noise performance is -106.3 dBc/Hz at a 1 MHz offset.

4.3 Comparison with Simulation Results and Remarks

Measurement results in Sec. 4.2, albeit indicate that all four VCOs within the oscillator IC work, show differences with the simulated results in Sec. 3.3. The main nonconformities between the simulations and measurements are:

- **Oscillation frequencies are slightly higher than expected.** Although all devices were intended to oscillate at approximately 10 GHz center frequency in the X-band, they oscillate at the center frequencies of approximately 12 GHz, except for VCO 3 which oscillates at 12.8 GHz. Thus, the devices oscillate between the end of the X-band and the beginning of the Ku-band.

- **Output powers are lesser than expected.** Despite the simulated output powers, the measured results indicate 5 to 10 dBm less output power.

- **Somewhat higher DC power consumption than anticipated.** VCOs consume 2 to 4 mW more DC power than expected.
- **More phase noise is present at the output than predicted.** Measured phase noises at 1 MHz offset are approximately 10 dBc/Hz more powerful compared to the simulations.

Therefore, major issues with the realized ICs are higher oscillation frequencies that cannot cover the intended center frequency of 10 GHz and the inability to deliver the expected level of power to the outputs. The other two issues are somewhat expected, as realistic circuits tend to consume more power and produce more noise than their simulated counterparts. The first two, possible causes are listed below:

- **Parasitic extractor might have overestimated parasitic L's and C's inside the VCOs.** Higher than expected oscillation frequencies may indicate that the total L and C values the gain transistors see are less than expected, resulting in higher-frequency oscillations. The parasitic extractor may have computed higher parasitic values than there are present in the device.
- **Unaccounted voltage drops might be present between the IC pads and power rails in the IC core.** Lowering the supply voltage causes an increase in the oscillation frequency and a decrease in the output power before the oscillation completely ceases. If there is an unknown voltage drop somewhere inside the IC, it might be causing the device to receive less power. IC bond pads and IO ring blocks could not be included in the simulation as their models are not present (they were provided to us as black boxes.)
- **Dummy fills utilized throughout the IC may cause shifts in resonance frequencies and output power leaks.** Simulating all the dummy diffusions, metals, and capacitors require tremendous amounts of simulation time, and thus could not be performed. In spite of not expecting them to cause significant performance issues, this could be the case.

Chapter 5

Conclusion

Electronic oscillators are devices that find many uses in today's applications. Most of them require some sort of control input to be able to vary their output frequencies. If this input is in the form of a DC voltage, they are called voltage-controlled oscillators, or in short, VCOs. They need to satisfy certain performance criteria depending on the needs of an application. Most commonly considered criteria are tuning range, which quantifies how much the output frequency can possibly be tuned, and phase noise, which describes how much undesired variations are present in the output spectrum aside from the oscillation frequency. In this thesis, four oscillator devices are designed and fabricated in a 0.18 μm CMOS process to assess the compromise when shooting for either of these metrics. A wide tuning range necessitates complex tuning circuitry within the resonator of a VCO, whereas lowering phase noise requires fewer noise sources in a VCO, forcing designers to simplify their designs instead.

Before shifting the focus of this thesis to VCOs, our aim was to design custom on-chip monolithic inductors with good quality factors and observe how changing their design parameters changes their inductances and quality factors at particular frequencies. This work provided insight into how on-chip inductors operate and what performance should be expected from them. (At this part of the thesis, PDK of a 0.6 μm CMOS process was used instead.)

Four integrated oscillator devices designed in the scope of this thesis include identical circuitry except for the capacitive parts of their LC resonators. While the first device (VCO 0) includes the most complex capacitive network where two switched capacitor blocks and a varactor block are present, the last device (VCO 3) only utilizes a single constant capacitor block. Ergo, while the first device aims for the best tunability, the last one aims for the best phase noise performance. (Although VCO 3 is not technically a VCO, for easier referencing and avoiding confusion, it is referred to as a "VCO" throughout this thesis.)

All devices were intended to operate in the X-band, at a center frequency of 10 GHz, and they are optimized according to their pre- and post-layout simulation results. After these simulations, the designed IC was fabricated, and dies were received, which were then tested with a measurement setup suitable for this purpose. The measured results were promising, but there were two main differences that were predicted differently by the simulations: Variations in oscillation frequency, as they leak into the Ku-band (hence an increase in center frequencies); and lower-than-expected output power results.

All four oscillators in the IC operating successfully and oscillating close to the intended center frequency suggest that the work done is overall successful. Future work regarding this oscillator IC should involve understanding why this variation in the simulated and actual results occurs and how it can be mitigated. Understanding the cause of these encountered problems would allow us to design better VCOs that excel in both tunability and phase noise performance. After countering these issues, any future work can be done which utilizes these integrated VCOs within larger devices such as modulators, PLLs, clock generators, transmitters, and any other electronics that require an integrated RF VCO.

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Appendix A

Differential Output Simulation Results

The results of the output power with respect to the frequency, when simulated with a differential output, are given in this chapter. As expected, the resulting output can deliver twice as much power compared to a single-ended simulation (as presented in Fig. 3.17). In other words, this results in a 6 dBm increase in output power. The results of this simulation are shown in Fig. A.1. As for harmonic powers, odd harmonics experience the usual 6 dBm increase in power. Even harmonics, on the other hand, get damped when subtracted from each other. This shows the efficiency of differential topologies against even harmonics. The results of these are shown in Table A.1.

Naturally, the frequency of oscillation does not get affected when measured from one or two outputs, since its results are the same as in Fig. 3.16. Phase noise results do not vary either, and its results are the same as shown in Fig. 3.18. (Since both ends of a differential output have the same phase noise, the signal-to-noise ratio between the carrier and the offset remains the same.)

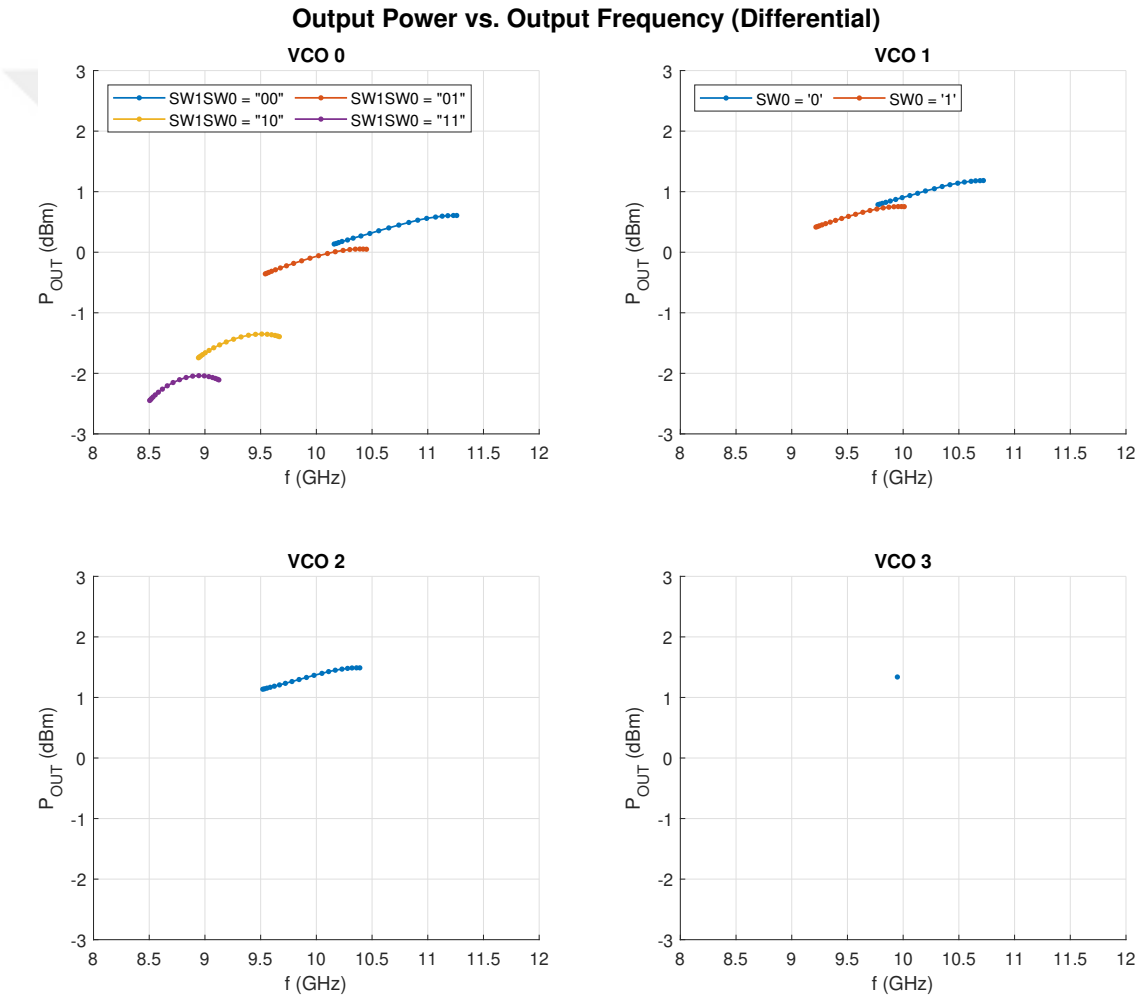


Figure A.1: Differential output power vs. output frequency simulations

$SW1SW0$	V_C (V)	f_{out} (GHz)	P_{out} (dBm)	G_2 (dBc)	G_3 (dBc)
"00"	0	10.16	0.1353	−53.81	−24.80
	0.9	10.65	0.4016	−55.35	−24.91
	1.8	11.26	0.6069	−60.70	**−21.81**
"01"	0	9.543	−0.3578	−51.58	−26.37
	0.9	9.944	−0.0978	−52.17	−26.35
	1.8	10.45	0.0529	−53.82	−23.34
"10"	0	8.942	−1.742	−49.69	−29.13
	0.9	9.257	−1.436	−49.63	−28.80
	1.8	9.668	−1.392	−50.14	−26.17
"11"	0	8.504	−2.446	−49.80	−31.27
	0.9	8.772	−2.105	−49.54	−30.88
	1.8	9.125	−2.110	−49.96	−28.85

(a) VCO 0

$SW0$	V_C (V)	f_{out} (GHz)	P_{out} (dBm)	G_2 (dBc)	G_3 (dBc)
'0'	0	9.774	0.7856	−43.95	−24.73
	0.9	10.20	1.012	−43.24	−24.80
	1.8	10.72	1.184	−42.54	**−21.86**
'1'	0	9.217	0.4155	−44.66	−25.79
	0.9	9.774	0.6264	−44.15	−25.89
	1.8	10.01	0.7529	−43.75	−23.93

(b) VCO 1

V_C (V)	f_{out} (GHz)	P_{out} (dBm)	G_2 (dBc)	G_3 (dBc)
0	9.519	1.136	−50.86	−25.87
0.9	9.913	1.330	−51.20	−26.56
1.8	10.39	1.489	−52.03	**−23.61**

(c) VCO 2

f_{out} (GHz)	P_{out} (dBm)	G_2 (dBc)	G_3 (dBc)
9.948	1.338	−48.97	**−24.67**

(d) VCO 3

Table A.1: Differential harmonic power simulations

Appendix B

Layout Drawings

In this chapter full layout drawings of our VCO designs are given in Fig. B.2 in order to provide the reader with the details of the VCO topologies. A layer legend is provided in Fig. B.1.

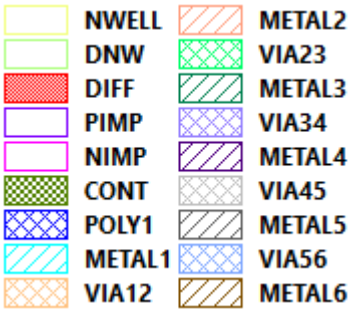
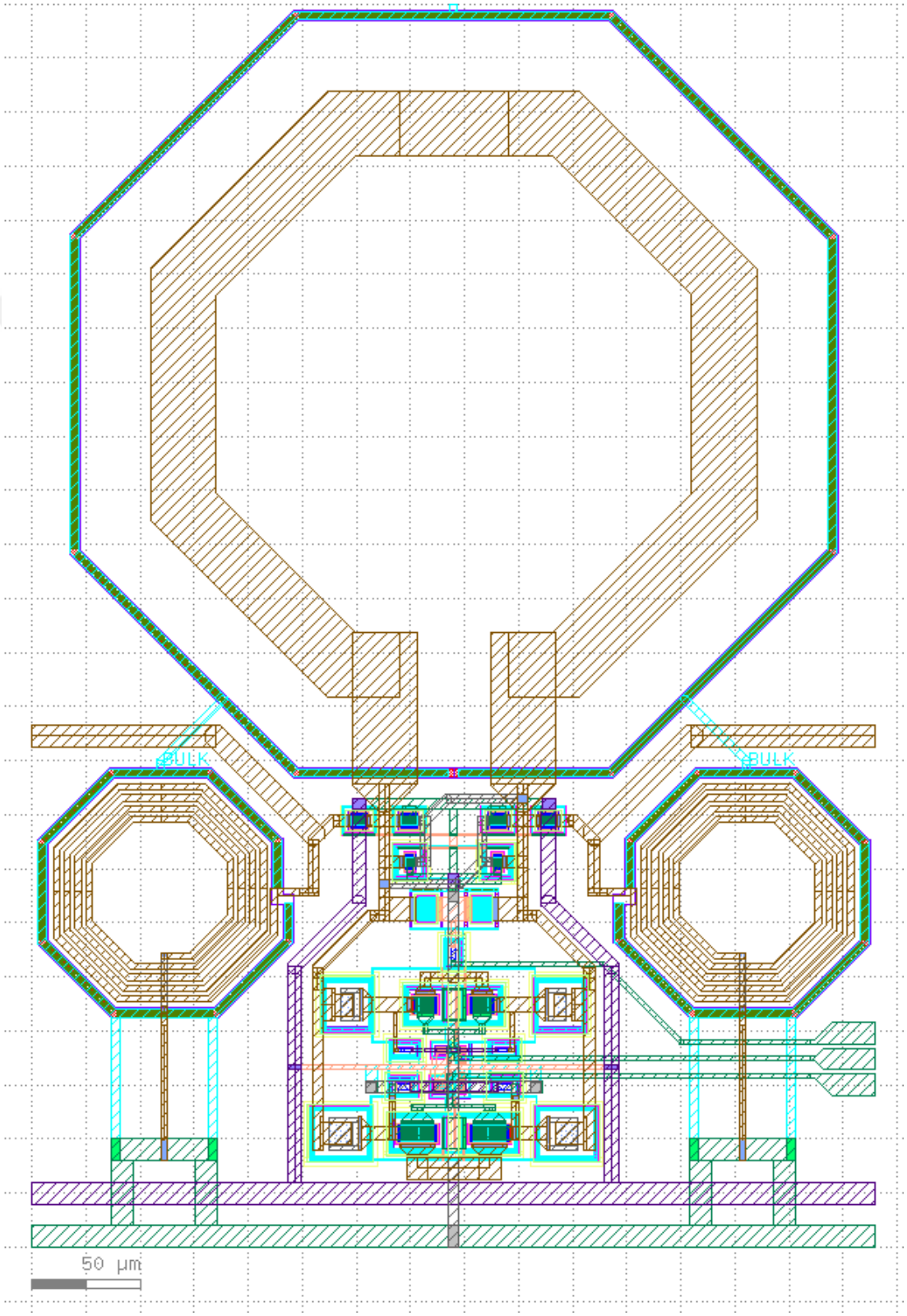
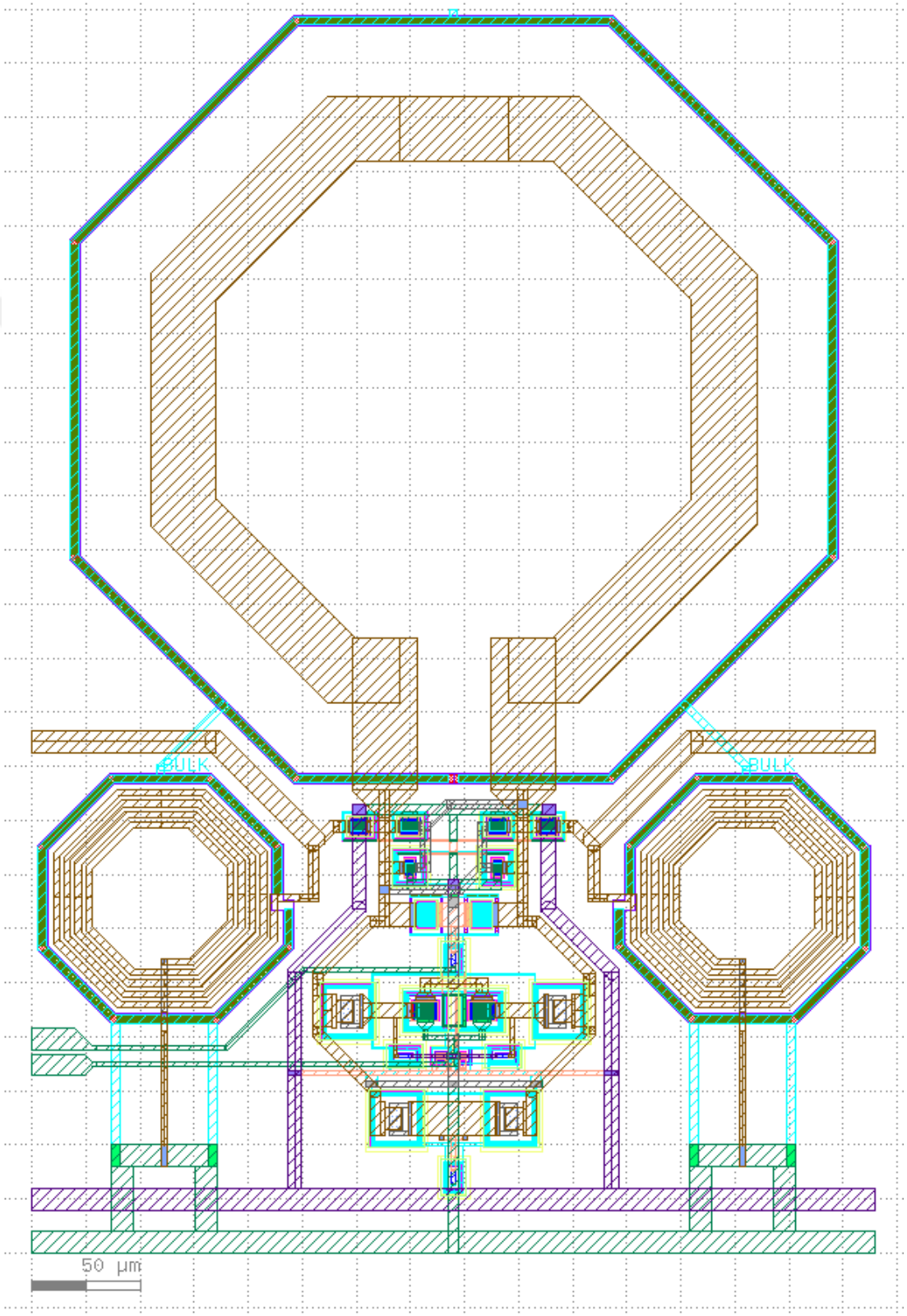


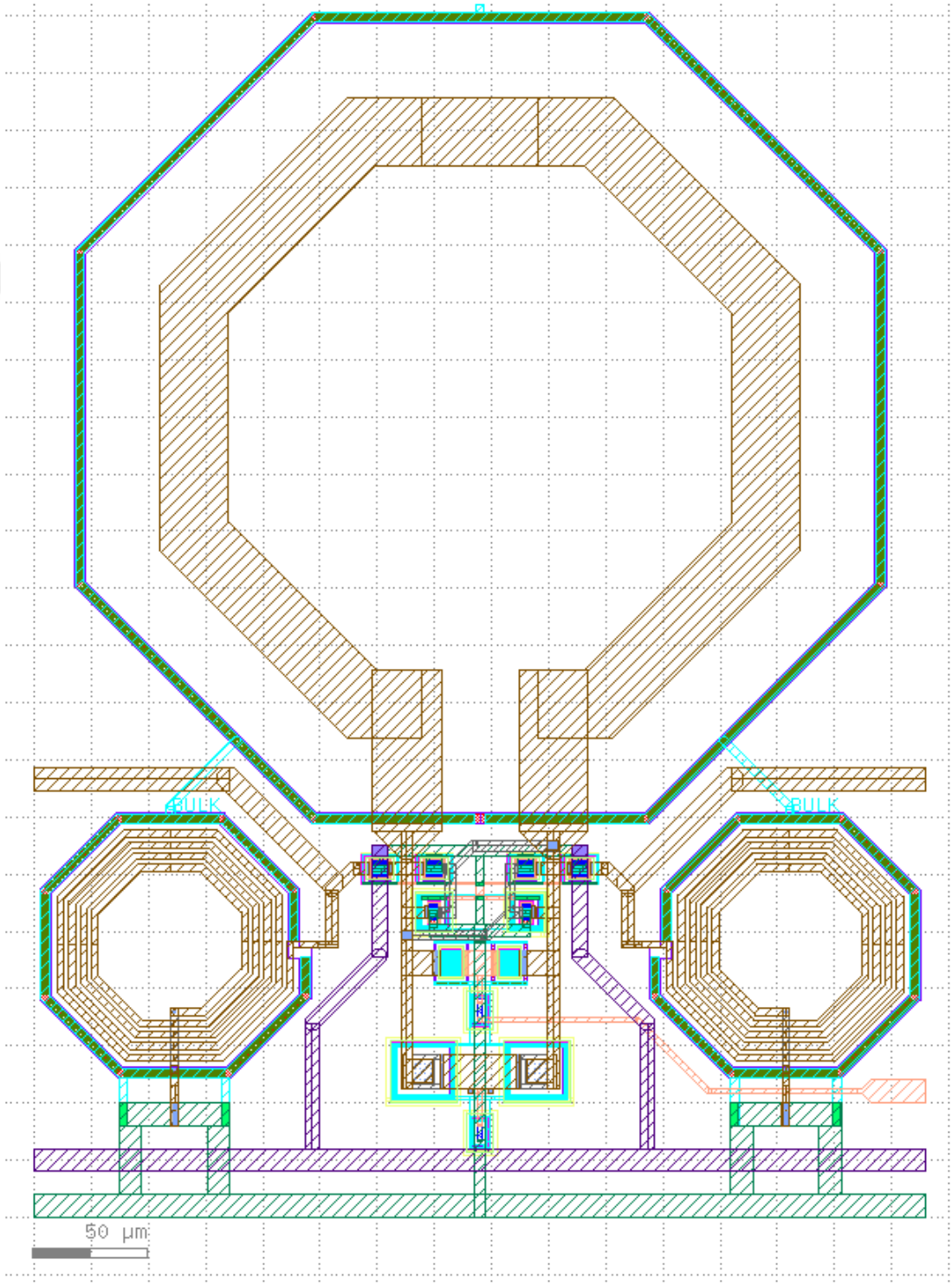
Figure B.1: Legend indicating pattern-layer correspondence in layouts



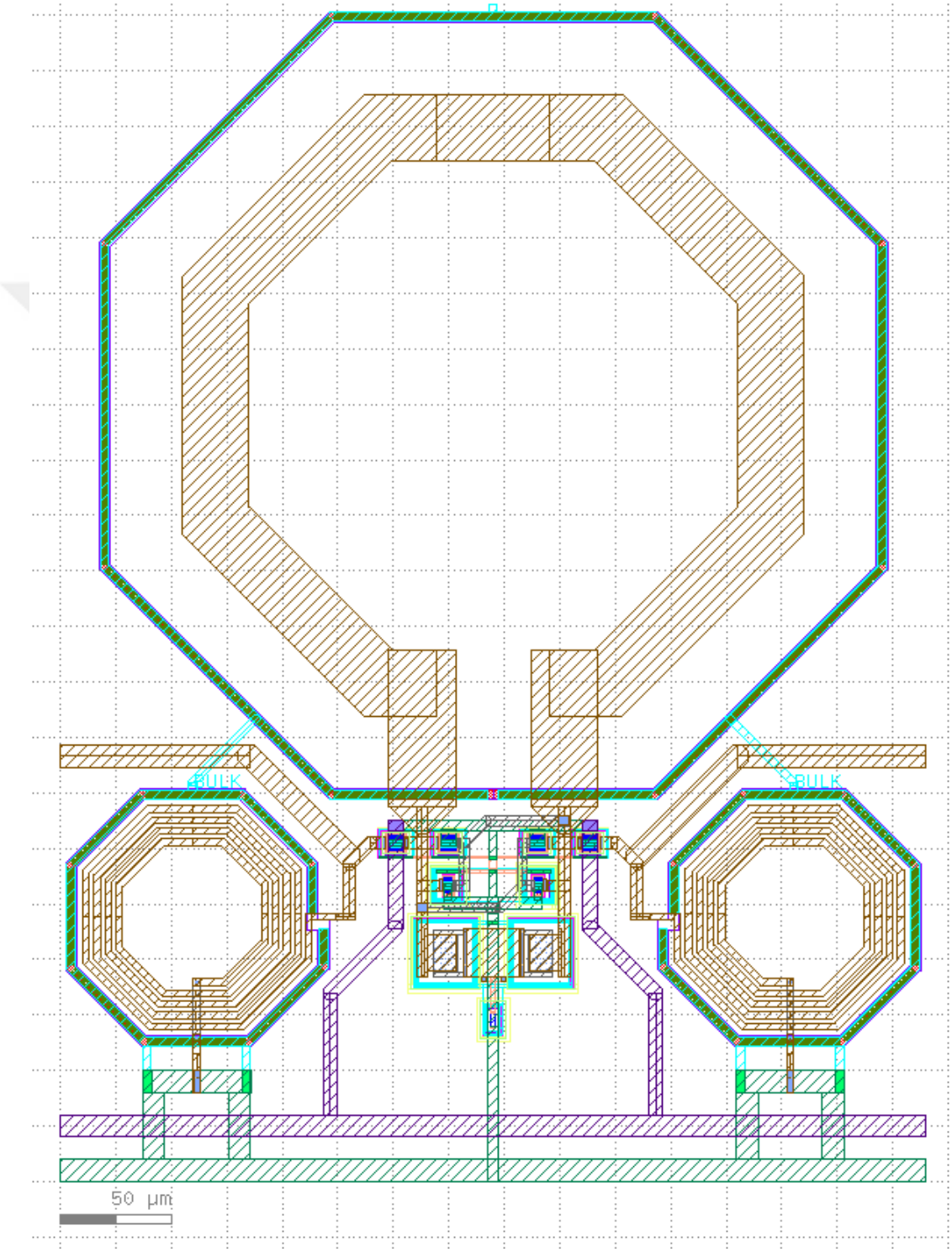
(a) VCO 0 layout



(b) VCO 1 layout



(c) VCO 2 layout



(d) VCO 3 layout

Figure B.2: Individual layouts of the VCOs

Appendix C

Detailed Die Micrographs

In this chapter, detailed and zoomed-in images of VCO devices are provided to let the reader examine them in detail. First, a clearer image of the IC, with its core in the focus, is presented in Fig. C.1. Next, the micrographs of each individual VCO are provided in Fig. C.2.

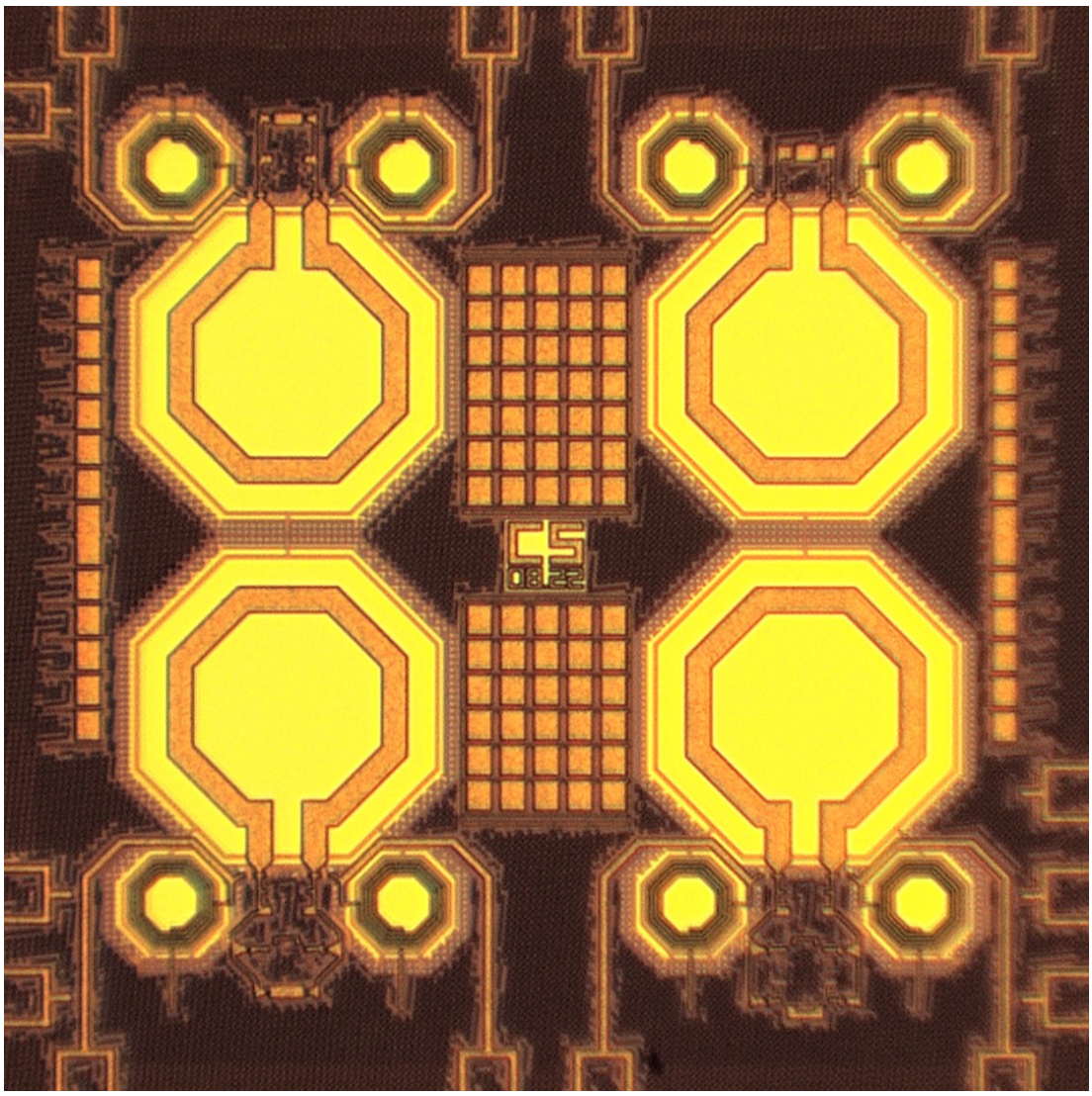
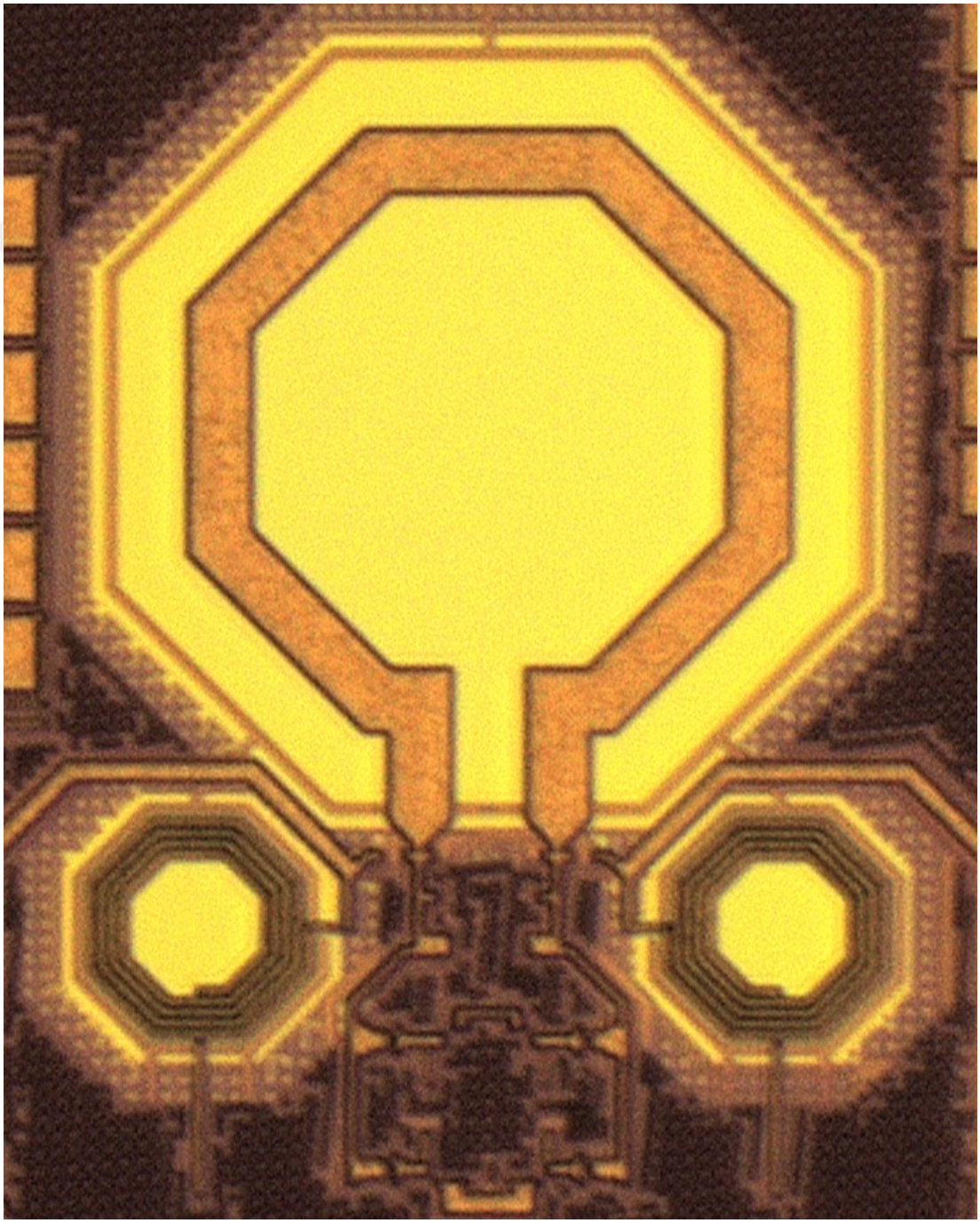
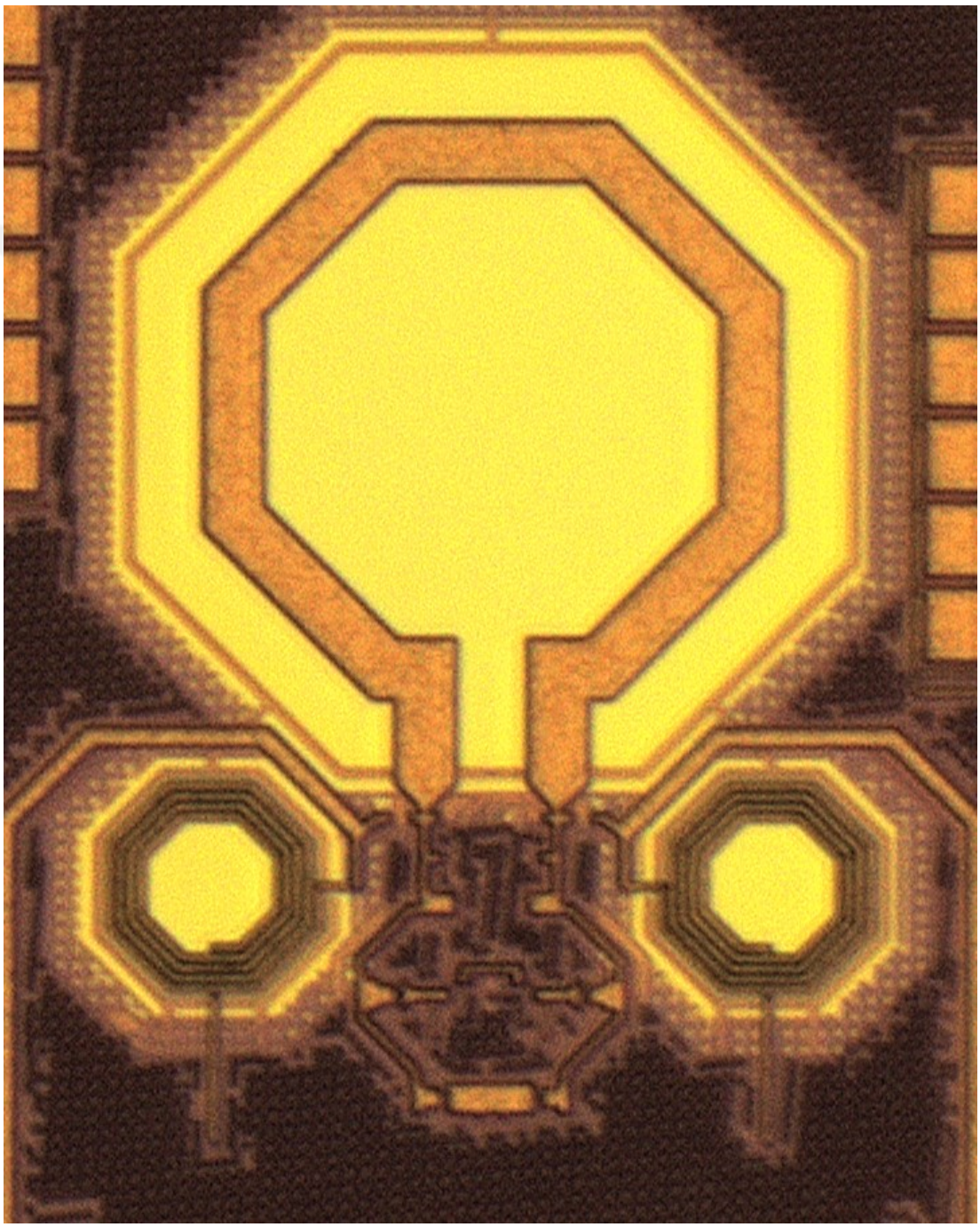


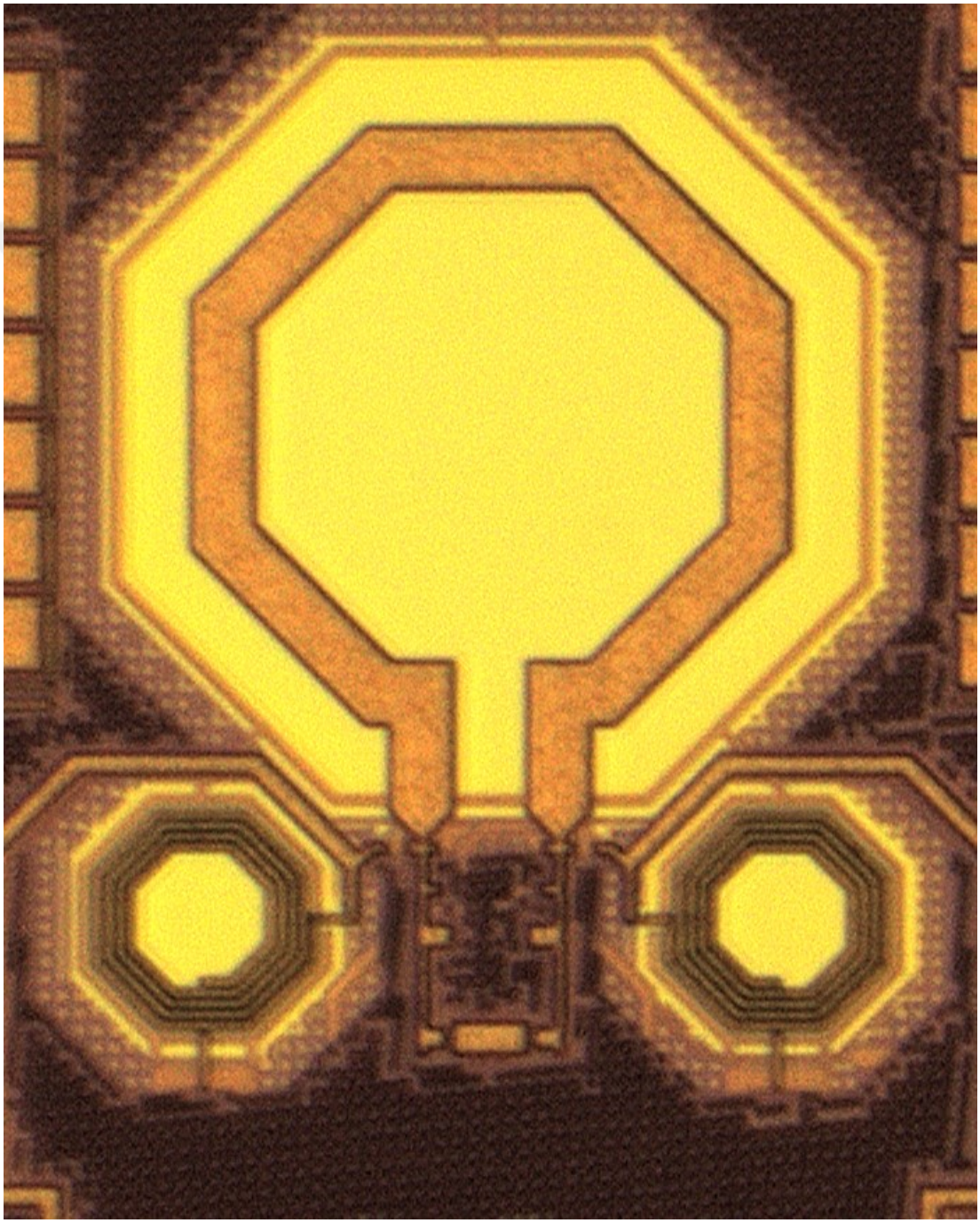
Figure C.1: Micrograph of the IC core (without the IO ring and pads)



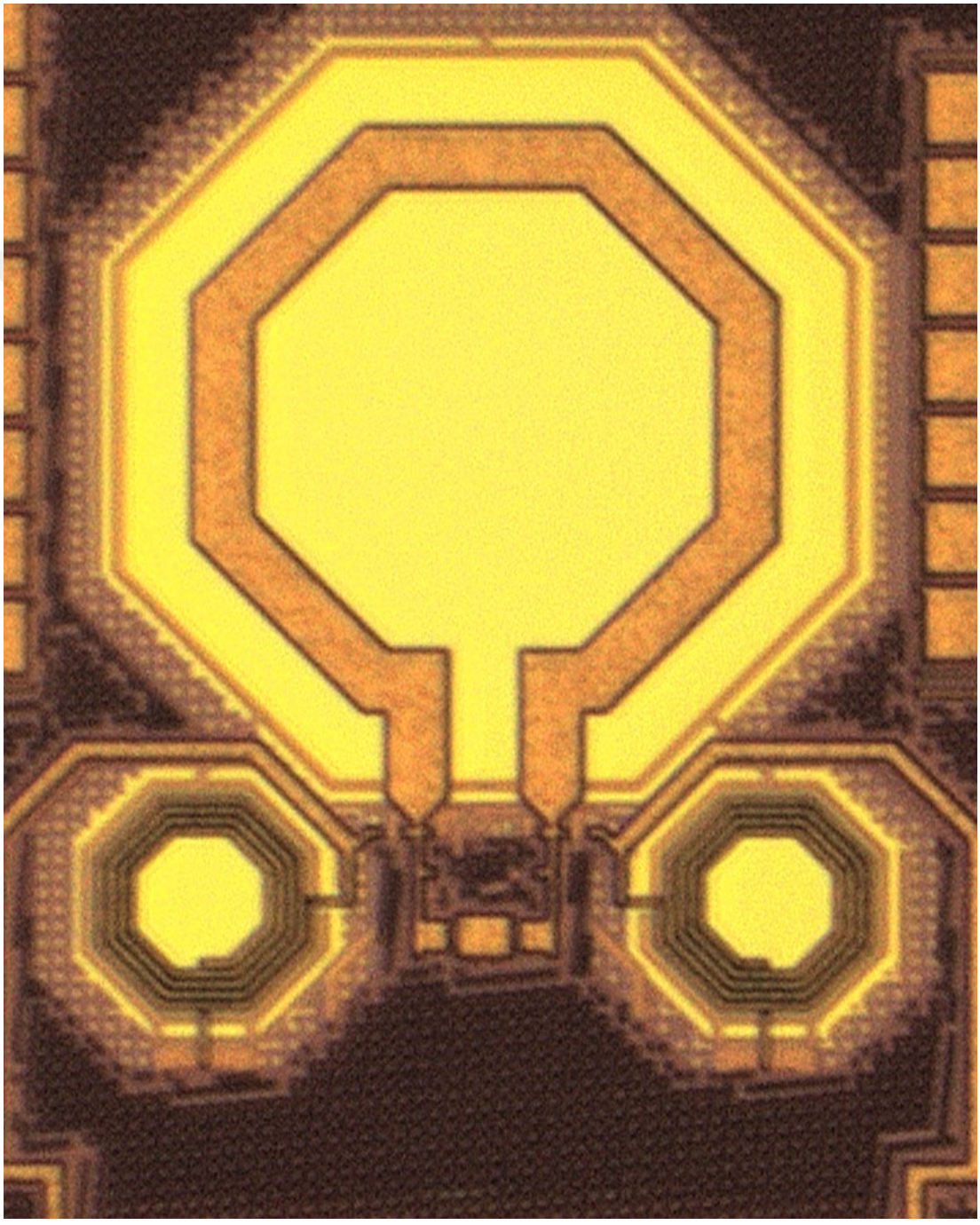
(a) VCO 0 micrograph



(b) VCO 1 micrograph



(c) VCO 2 micrograph



(d) VCO 3 micrograph

Figure C.2: Individual micrographs of the VCO's

Appendix D

Measurement Setup Preparation

This chapter aims to elaborate the complete details of how the measurement setup was prepared, which was briefly summarized in Chap. 4, Sec. 4.1.

D.1 Test PCB

A test PCB had to be designed to test the oscillator IC. We concluded that packaging the die would yield intolerable amounts of parasitic elements for the frequency range within which the device works. Thus, we have decided to follow the chip-on-board (COB) approach and designed a PCB on which the die could be epoxied and wire bonded. As such, the PCB has tiny 6 mil wide gold pads on which wire bonding is possible. In the middle of these bond pads, a large square pad with 70 mil width was placed to epoxy the die. The bonding diagram that shows how these connections should be made is provided in Fig. D.1.

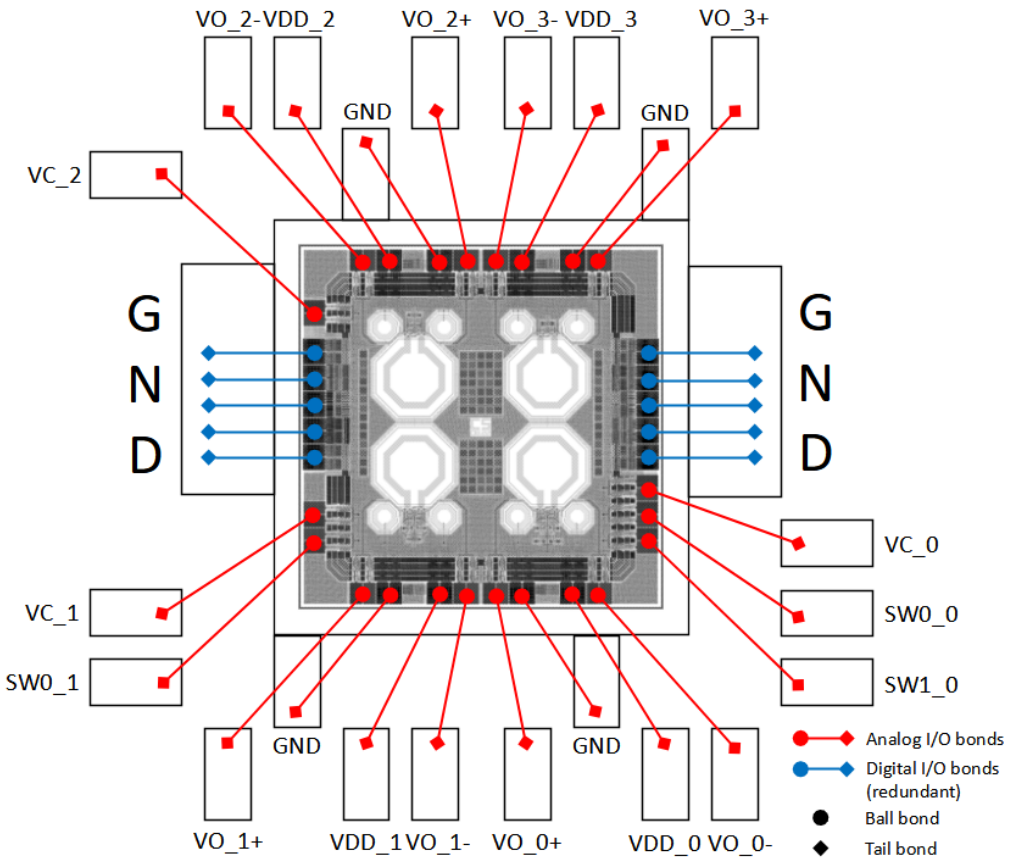


Figure D.1: Bonding diagram of the oscillator IC

Before starting the design, a suitable material for the PCB substrate had to be chosen. This choice was going to determine the widths of the RF transmission lines in our circuit. For our purposes, Rogers 4350B is an adequate choice. It provides a dielectric constant of $\varepsilon_r = 3.66$ and a dissipation factor of $DF = 0.0037$ (at 10 GHz, 23°C) [19].

Next, the appropriate transmission line widths must be determined to provide a 50 Ω path to four RF outputs of oscillators within the IC. Using AWR TX-Line utility, the microstrip line width has been determined as 42.4 mil (a line with no ground plane near its vicinity, at 10 GHz), and the coplanar waveguide width has been determined as 39.1 mil (a line with ground planes on both sides; ground plane distances are 20 mils, at 10 GHz). The final width for the lines has been determined as 40 mil.

For the ease of making measurements with a single-input spectrum analyzer, only one end of differential outputs of each oscillator is taken and connected to a panel-mounted SMA connector. The other ends are terminated with 51 Ω resistors. All outputs are filtered from DC components using 20 fF coupling capacitors.

DC control inputs of VCOs 1 and 2 are directly carried from the PCB input port to the die inputs without any elements in between. Due to design limitations, three input signals of VCO 0 are carried with jumper wires before being connected to the die.

Since four VCO's within the IC have isolated power inputs of their own, four different input networks for providing power have been placed on the PCB with feedthrough capacitors of 2.2 nF, decoupling capacitors of 3.3 μF, RF chokes of 33 μH and bypass capacitors of 10 nF and 100 pF. After the bypass capacitors, the input powers are carried with jumper cables to the die, due to the design limitations of a single-sided PCB.

All DC control and power inputs are provided to the test PCB from a D-Sub DB-15 connector. The other end is connected to the aforementioned control PCB, which manages the switchings between DC power and control inputs.

Schematic and layout images, as well as photographs of the fabricated test PCB are provided below. The test PCB schematic is provided in Fig. D.2, with its reference-value pairs of components shown in Table D.1; while its layout is provided in Fig. D.3. Top and bottom photographs of a test PCB without its components are given in Fig. D.4, while one with its components soldered (except for the D-Sub and SMA connectors) is given in Fig. D.5.

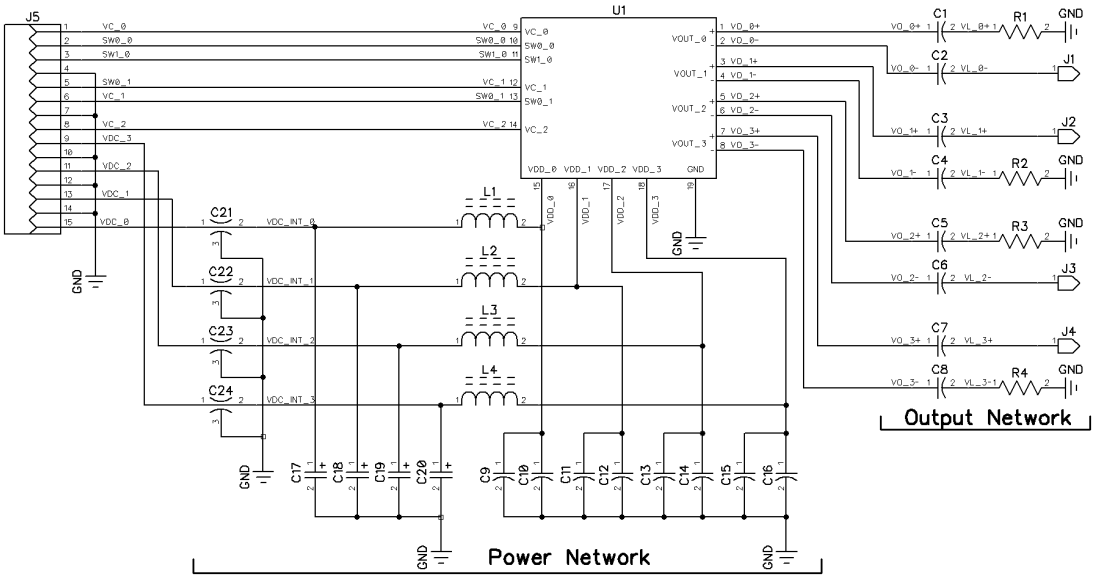
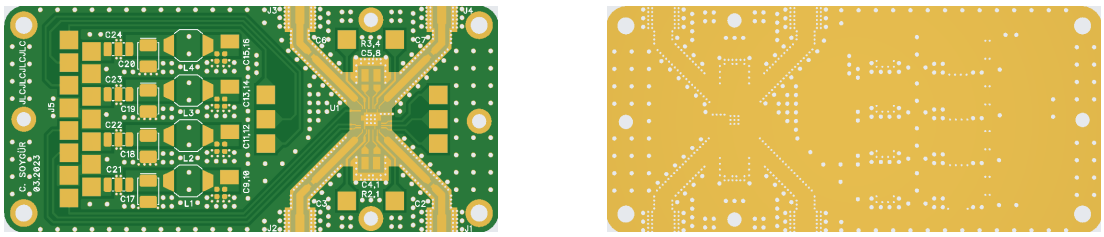


Figure D.2: Schematic of the test PCB

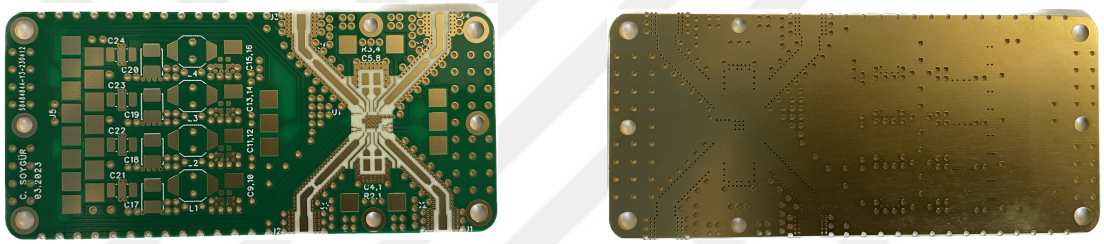
Ref. Designations	Values
U1	Osc. Die
R{1,2,3,4}	50Ω (SMD 402)
C{1,2,3,4,5,6,7,8}	20pF (SMD 402)
C{9,11,13,15}	1nF (SMD 402)
C{10,12,14,16}	150pF (SMD 402)
C{17,18,19,20}	3.3μF (SMD Tant. Case-B)
C{21,22,23,24}	2.2nF (SMD 1206, 3-term.)
L{1,2,3,4}	33μH (SMD SDR6603)
J{1,2,3,4}	SMA Con. (Panel Mnt.)
J5	D-Sub Con. (DB15F)

Table D.1: List of components in the test PCB



(a) Top view (b) Bottom view

Figure D.3: Layout of the test PCB



(a) Top side (b) Bottom side

Figure D.4: Test PCB before its components are soldered on

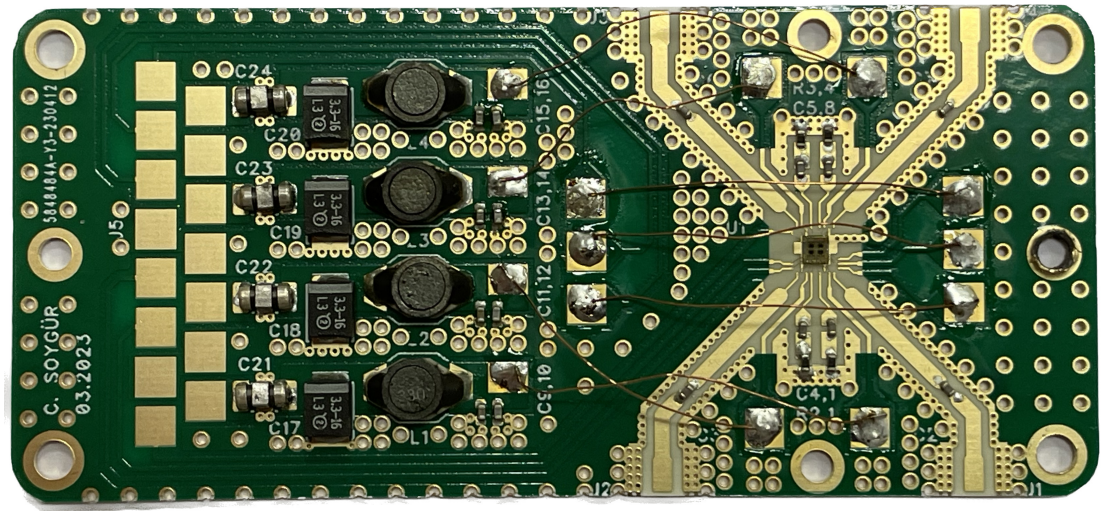
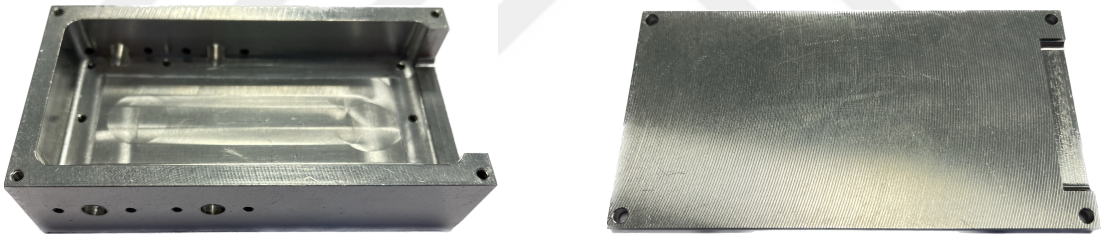


Figure D.5: Test PCB with its components soldered on

D.2 Shielding Box

A custom-made aluminum box has been utilized to provide shielding for the oscillator IC and its test PCB. It has an interior cavity to place the test PCB and cutouts for inputs (through the DB-15 connector) and outputs (through panel mount SMA connectors). It has been manufactured by processing an aluminum prism with dimensions of $78 \times 40 \times 19\text{mm}^3$ using a CNC (computer numerical control) machine. A cavity with 10mm depth and 4mm thickness was cut from the prism, creating a space to place the test PCB. Following this, cutouts for the ports have been added to their respective places to provide outside connection for the PCB. Another short aluminum prism with dimensions $78 \times 40 \times 3.2\text{mm}^3$ is utilized as a lid for the box. The images of the shielding box and lid are given separately in Fig. D.6 whereas Fig. D.7 show them together.



(a) Body of the box (b) Lid of the box

Figure D.6: Body and lid of the shielding box separated

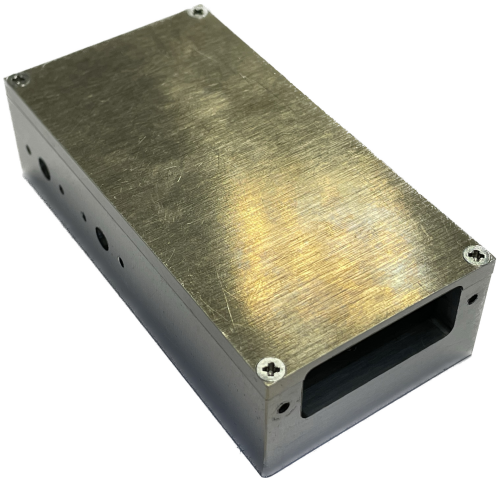


Figure D.7: Empty shielding box with its lid closed

D.3 Control PCB

All four VCOs in the IC have their own separate DC power and control inputs with separate input pins on the D-Sub connector. Nevertheless, all inputs have the same parameters (1.8 V power inputs, 0 or 1.8 V discrete switching inputs and 0 to 1.8 V continuous tuning inputs). This led to the idea of designing a simple control PCB that handles switching operations between inputs during tests of each four oscillators, instead of manually switching via jumper wires between each test.

The PCB takes the DC power input and the tuning control input from two sets of banana sockets. Both sockets are connected to DC power supplies; the first is set to 1.8V, whereas the latter is tuned in the range 0, 1.8V. Each input then arrives at a toggle switch that toggles between them and ground (the latter is connected through 1.8kΩ resistors). Followingly, DC power input arrives to a 4-input and a 3-input DIP switch; while the first turns the power on or off for VCO's the second turns on or off the switched capacitor arrays of VCOs 0 and 1 for coarse tuning. DC control input, on the other hand, arrives at a single 3-input DIP switch that provides control input for VCOs 0, 1 and 2.

The PCB has been fabricated with standard FR4 material. Schematic and layout images, as well as photographs of the fabricated control PCB are provided below. The control PCB schematic is provided in Fig. D.8, with its reference-value pairs of components shown in Table D.2; while its layout is provided in Fig. D.9. Top and bottom photographs of a control PCB without its components are given in Fig. D.10, while one with its components soldered is given in Fig. D.11.

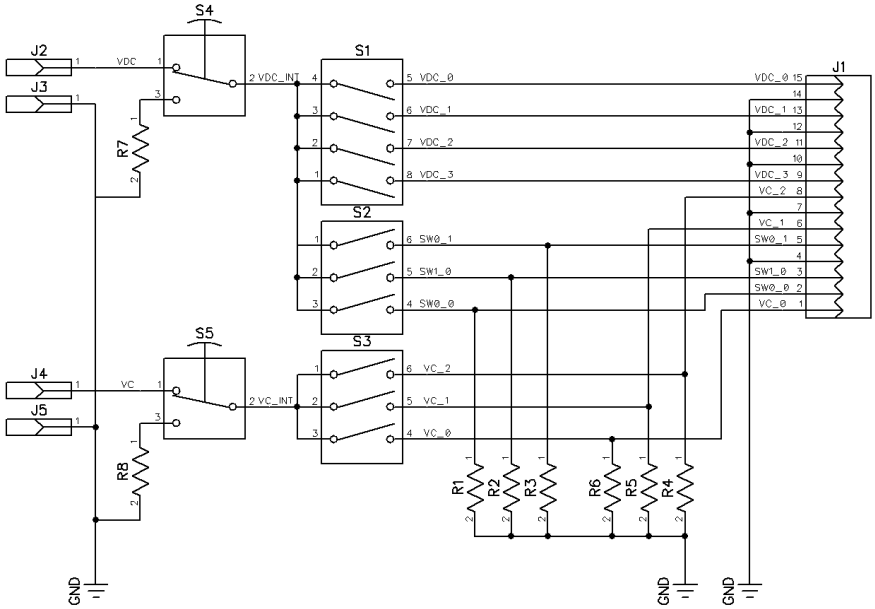
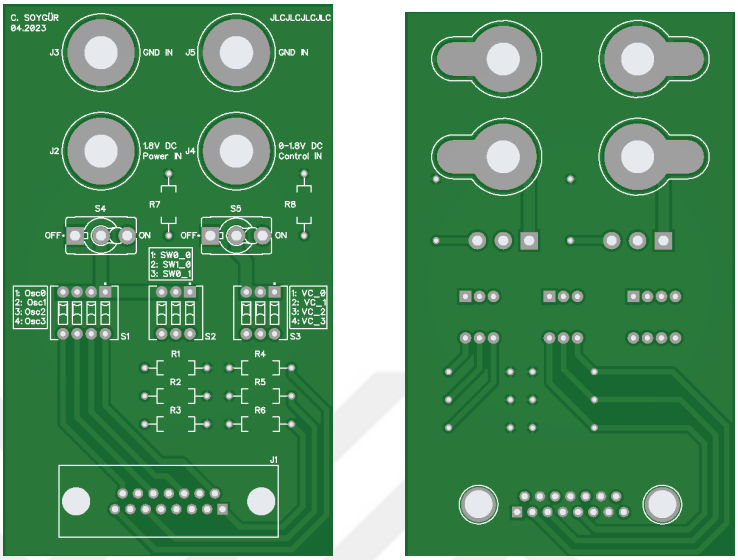


Figure D.8: Schematic of the control PCB

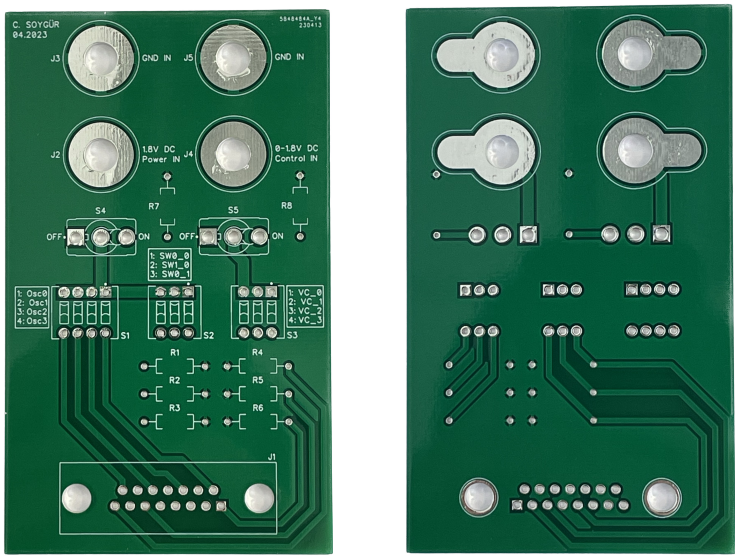
Ref. Designations	Values
R{1,2,3,4,5,6,7,8}	1.8kΩ (TH)
S1	3-Pin Dip Sw. (BD04)
S{2,3}	3-Pin Dip Sw. (BD03)
S{4,5}	Toggle Sw. (ON-OFF)
J1	D-Sub Con. (DB15M)
J{2,3,4,5}	Banana Jack (4mm)

Table D.2: List of components in the control PCB



(a) Top view (b) Bottom view

Figure D.9: Layout of the control PCB



(a) Top side (b) Bottom side

Figure D.10: Control PCB before its components are soldered on

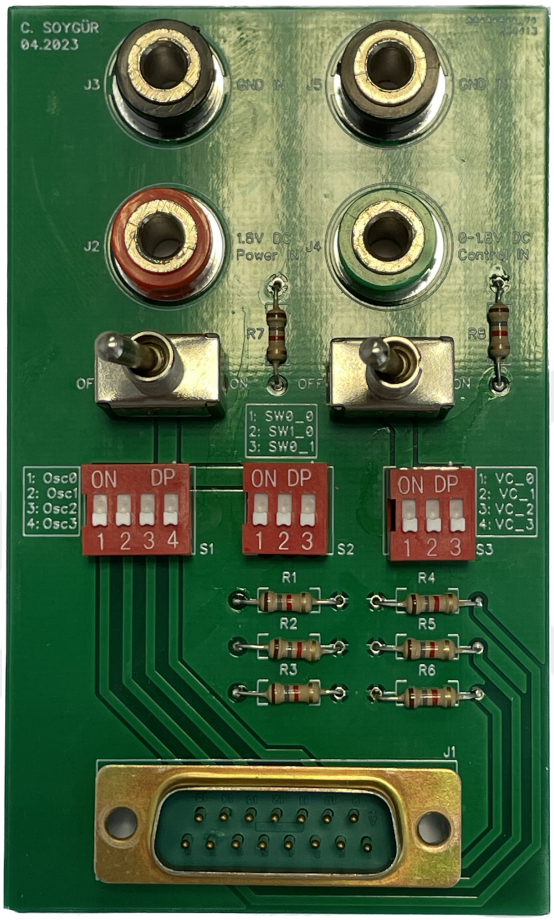


Figure D.11: Control PCB with its components soldered on