

HIGH PERFORMANCE CURRENT CONTROL METHODS FOR VOLTAGE
SOURCE CONVERTERS WITH SATURABLE INDUCTORS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

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IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF DOCTOR OF PHILOSOPHY
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

JUNE 2019

Approval of the thesis:

**HIGH PERFORMANCE CURRENT CONTROL METHODS FOR
VOLTAGE SOURCE CONVERTERS WITH SATURABLE INDUCTORS**

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ABSTRACT

HIGH PERFORMANCE CURRENT CONTROL METHODS FOR VOLTAGE SOURCE CONVERTERS WITH SATURABLE INDUCTORS

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June 2019, 182 pages

Pulse Width Modulated (PWM) Voltage-Source Converters (VSCs) are the building blocks of today's power electronics technology for grid-connected systems. In PWM-VSC systems, utilization of filter inductors with deep saturation characteristics is often advantageous due to improved size, cost, and efficiency. However, with the inclusion of saturable inductors, current control dynamics become nonlinear. The utilization of conventional linear current regulation methods in such nonlinear systems results in significant dynamic performance loss as bandwidth shrinkage and poor steady-state current waveform quality as amplification of low-frequency harmonics. This thesis proposes an Inverse Dynamic Model Based Compensation (IDMBC) method and a Saturation Compensation with Resistive Decoupling (SCRD) method to overcome the performance issues of PWM-VSC systems with conventional linear current regulators. Prior to implementation, the nonlinear VSC system L-R parameters are characterized. Employing the nonlinear system characteristics foreknowledge, the proposed methods linearize the nonlinear plant in the large yielding a fictitious linear plant such that linear controllers perform satisfactorily. These methods can be

applied to single-phase (1P) (half-bridge (HB) and full-bridge (FB)) and multiphase HB and FB VSC systems. In 1P (HB/FB) and multiphase HB systems single-line dynamic parameters are used in the linearization. Unconventionally, in multiphase FB systems the line-to-line nonlinear system model is established and utilized in the linearization. The proposed methods are applied to single-phase and three-phase PWM-VSC grid-connected systems. A thorough dynamic response, parameter mismatch, and steady-state performance assessment of the methods is performed in comparison with conventional methods. Advantageous performance attributes are demonstrated via analyses, simulations, and laboratory experiments.

Keywords: Bandwidth, Current Regulator, Dynamic Response, Inductor Saturation, Harmonic Distortion, Grid Connected Voltage Source Converter, Saturable Inductor

ÖZ

DOYMALI İNDÜKTÖRLÜ GERİLİM KAYNAĞI DÖNÜŞTÜRÜCÜLERDE YÜKSEK BAŞARIMLI AKIM DENETİM YÖNTEMLERİ

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Haziran 2019 , 182 sayfa

Darbe Genişlik Modülasyonlu (DGM) gerilim kaynaklı dönüştürücü (GKD)'ler günümüz şebeke bağlantılı güç elektroniği teknolojilerinin yapı taşıdır. DGM-GKD sistemlerinde derin doyma özellikli filtre indüktörlerinin kullanımı üstün boyut, maliyet ve verim sebebiyle avantajlıdır. Buna rağmen doymalı indükterlerin kullanımıyla akım kontrol dinamikleri doğrusal olmayan hale gelir. Geleneksel doğrusal akım kontrol yöntemlerinin böylesine doğrusal olmayan sistemlerde kullanımı kontrol bant genişliği daralması şeklinde önemli dinamik başarımların kaybı ve düşük frekans harmoniklerin yükselmesi şeklinde kalıcı durum dalga şekli kalitesi bozulması ile sonuçlanır. Bu tez geleneksel doğrusal akım denetleyicili DGM-GKD sistemlerde başarımların sorunlarını çözmek için Ters Dinamik Model Tabanlı Dengeleme (TDMTD) yöntemini ve Direnç Ayrışmalı Doyma Dengelemesi (DADD) yöntemini önerir. Yöntemlerin uygulanmasından önce doğrusal olmayan L-R parametreleri karakterize edilir. Doğrusal olmayan sistem karakteristik ön bilgisiyle önerilen yöntemler sonuçta doğrusal denetleyicilerin başarılı bir şekilde çalışacağı varsayımsal bir doğrusal sistem verecek şekilde doğrusal olmayan sistemi doğrusallaştırır. Bu yöntemler tek faz (1F)

(yarım köprü (YK) ve tam köprü (TK)) ve çok faz YK ve TK GKD sistemlerine uygulanabilir. 1F (YK/TK) ve çok faz YK sistemlerin doğrusallaştırılmasında tek hat parametreleri kullanılır. Sıradışı olarak, çok faz sistemlerde faz arası doğrusal olmayan sistem modeli sistem doğrusallaştırılması için kurulur ve kullanılır. Önerilen yöntemler tek faz ve üç faz şebeke bağlantılı DGM-GKD'lere uygulanmıştır. Yöntemlerin kapsamlı dinamik tepki, parametre sapması ve kalıcı durum başarımlarını değerlendirme geleneksel yöntemlerle karşılaştırmalı olarak yapılmıştır. Yöntemlerin yüksek başarımlarını özellikleri analiz, benzetim ve laboratuvar deneyleriyle doğrulanmıştır.

Anahtar Kelimeler: Akım Denetleyici, Bant Genişliği, İndüktör Doyması, Dinamik Tepki, Doymalı İndüktör, Harmonik Bozunumu, Şebeke Bağlantılı Gerilim Kaynağı Eviriciler



To humanity.

ACKNOWLEDGMENTS

I express my sincerest thanks to my supervisor, Prof. Ahmet M. Hava, for his guidance, support, encouragement, and valuable contributions throughout my graduate education.

I thank my final defence committee Professors Muammer Ermiş, Işık Çadircı, Yakup Özkazanç, and Emine Bostancı.

I would like to express my deepest gratitude to my family Kadir Özkan, Fatma Özkan, and Şadiye Özkan for their support and patience during not only my studies but also throughout all my life.

I would like to express my gratitude to Prof. Emre Tuna and Prof. Fatih Kamışlı for their technical support, infinite patience, and of great importance encouragement throughout my studies and education.

I would like to thank Semih Kavurucu, Eyüp Demirkutlu, and Prof. Hasan Eroğlu for their help and support on my experimental hardware studies, and their encouragement throughout my studies.

I also would like to thank Prof. Nevzat Özay for providing valuable practical engineering insight.

I would also thank Prof. Sinan Erdoğan and Prof. Elçin Kentel Erdoğan for their support and encouragement.

I also would like to thank Prof. Barış Bayram, Prof. Çağatay Candan, and Prof. Umut Orguner for their support throughout my studies.

I would like to express my gratitude to all my friends who stands (and would stand) besides with me when necessary.

I wish to thank Middle East Technical University Department of Electrical and Elec-

tronics Engineering faculty and staff for their help throughout my studies.



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LIST OF ABBREVIATIONS

1P	Single Phase
2L	Two Level
3L	Three Level
3P	Three Phase
3P3W	Three Phase Three Wire
3P4W	Three Phase Four Wire
AD	Active Damping
BW	Bandwidth
CCR	Conventional Current Regulation
CCR3	Three Phase Three Wire Conventional Current Regulation
CLTF	Closed-Loop Transfer Function
DPWM	Discontinuous Pulse Width Modulation
EMI	Electromagnetic Interference
FB	Full Bridge
HB	Half Bridge
HVDC	High Voltage Direct Current
IDM	Inverse Dynamic Model
IDMBC	Inverse Dynamic Model Based Compensation
NPC	Neutral Point Clamped
OLTF	Open-Loop Transfer Function
PI	Proportional Integral
PIR	Proportional Integral Resonant
PR	Proportional Resonant

PV	Photovoltaic
PWM	Pulse Width Modulation
SCRD	Saturation Compensation with Resistive Decoupling
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	Static Synchronous Compensator
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
THD _i	Total Current Harmonic Distortion
VSC	Voltage Source Converter



CHAPTER 1

INTRODUCTION

The engineering field of power electronics is a multidimensional piece of today's technology that eases human life and efficient use of world resources in many aspects. The energy conversion systems employing power electronics span a range of micro-watts of energy harvesting to megawatts of wind turbine applications. Motion control units, storage systems, active filters, power factor correction systems, battery charger systems, and power supply systems are a few more to name. Within this span, voltage-source converters (VSCs) gained popularity due to their advantage of high performance by means of efficiency, cost, and reliability; hence dominated most of the applications. Accordingly, many efforts have been put on the performance improvement in the efficiency increase, volume shrinkage, cost reduction, control attributes, and reliability which made VSCs probably the most investigated subject in the power electronics literature.

The development in the VSC technology expanded basically into four branches. These are semiconductors, converter topology, filter topology, and control/optimization.

With the advancements in the semiconductor technology, pulse width modulation became the industry standard. Hence throughout the study, the term VSC refers to pulse width modulated voltage-source converter. In accordance with the standardization of PWM in VSCs, modulation methods have been developed to improve waveform quality, efficiency, and DC bus voltage utilization, when applicable.

Following the semiconductor technology, converter topologies have evolved. Derived from buck converter, two-level VSC found vast application area. After that, three-level VSC topology was introduced, reducing the output filter size, hence cost.

Further, multilevel topologies arose providing a further reduction in the filter inductor and enabling operation at higher voltages. Topologies with other benefits, such as low leakage current, are developed recently for applications such as photovoltaic VSCs.

Output filter topologies are also developed to mitigate PWM related current harmonics. L, LC, LCL, LCL-LC, LLCL, etc. type filter topologies are developed with distinct attenuation characteristics. The design of these filters is also being developed.

On the other hand, the control and optimization of VSCs are also being investigated. The VSC heatsink, switching frequency, and filters are numerically optimized. Besides, the stationary frame and synchronous frame control architectures are the standard approach in current-controlled VSCs.

1.1 Problem Definition

In grid-connected PWM-VSC systems, utilization of grid interface filters is standard. Although the filter topology may vary, for the time being, the general trend is to use LCL filters, the converter side inductor experience high-frequency PWM pulses in proportion to DC-link voltage. Hence the design of the converter side inductor is an issue most of the times and has a high impact on the size, cost, and efficiency of the converter. Filter inductors with deep saturation characteristics are often advantageous in these aspects. However, with the use of conventional current regulation (CCR) methods, the inductor saturation results in poor steady-state current waveform quality at first. This issue is quite significant for most of VSC applications. For example, the current waveform quality in grid-connected systems is very critical as grid connection standards limits both the individual harmonic injections and requires overall waveform quality to meet predefined total harmonic distortion limits.

The second problem is the dynamic performance loss. The dynamic response performance is a measure of "how a command signal can be tracked in minimal time with minimal error in the physical system". The dynamic response performance is proportional to system closed-loop bandwidth. When saturable inductors are employed, the system inductance(s) change periodically with the inductor current bias level. Hence

the system dynamics change. As a result, the system response to the same step command change with the current bias. This feature of the conventional current regulation methods yields slow system response especially when the inductance is high. As a result, desired control performance can not be attained all the time while the converter is operating.

1.2 Contributions

First of all, this study explains a cost, weight, and energy-efficient implementation of VSC filter inductors, especially converter side inductors, with saturable cores.

The utilization of the saturable cores with conventional current regulation approaches brings problems described in the previous section that appear both in single-phase VSC systems and three-phase VSC systems. Accordingly, this study proposes the saturation compensation with resistive decoupling (SCRD) and inverse dynamic model based compensation (IDMBC) methods for the VSCs employing saturable inductors.

For single-phase controlled VSC systems, the SCRD and IDMBC are developed step by step and their frequency response analyses have been made by means of the command to output and disturbance to output characteristics. These two proposed methods are compared with the conventional approaches and IDMBC method is found to be advantageous when compared to other methods including the SCRD method.

For three-phase three-wire VSC systems, IDMBC method is developed also. In the development, three-phase three-wire VSC is modelled in a two-phase manner. Then, the inverse dynamic model is established accordingly. To comply with the three-phase VSC, two-phase modulation of three-phase VSC is developed also. Moreover, the frequency response analyses have been conducted to show the viability of the proposed technique.

The steady-state and dynamic response characteristics of the proposed methods are investigated in comparison with the existing methods via simulations and experiments. The results show the suitability of the proposed methods for the VSC systems employing saturable inductors.

1.3 The Outline of the Thesis

The organization of the thesis is as follows. In chapter 2, the development of VSC technology is reviewed on a fourfold basis. After that, the inductor technology in VSCs is elaborated and advantages behind the use of saturable inductors are emphasized via design examples.

In chapter 3, state-of-the-art current regulation methods for grid-connected VSCs are reviewed both for single-phase VSCs and three-phase three-wire VSCs. Then the problems that arose with the utilization of the conventional current regulation methods with saturable inductors are identified by means of analyses, simulations, and experiments. These problems are bandwidth shrinkage and waveform quality distortion, and are common both in single-phase and three-phase three-wire VSC systems.

Having the motivation to employ saturable inductors and the issues addressed with conventional current regulation methods, chapter 4 presents two methods: inverse dynamic model based compensation (IDMBC) and saturation compensation with resistive decoupling (SCRD). First, the mathematical development of these two methods are presented. Then the command to output and disturbance to output characteristics of these methods are derived together with the conventional current regulation method and K_p scheduling method. Simulations and experiments have been conducted and consistency between the analyses, simulations, and experiments has been observed. Based on the observations, IDMBC and SCR D methods are found to outperform conventional single-phase current regulation methods. Further, between these two proposed methods, IDMBC method is found to be better than SCR D method by means of disturbance rejection performance.

In chapter 5, due to its disturbance rejection performance, IDMBC method is adapted to three-phase three-wire current-controlled VSC systems. First, the inconsistency of the balanced three-phase system approach in three-phase three-wire VSC systems with saturable inductors is demonstrated. Then, the exact modelling of these systems is performed by means of two phases. After that, the linearization of these systems in the large via the established inverse dynamic model. Based on the plant and its inverse dynamic model, integral compensation is added so that the equivalent

system becomes a decoupled linear one. An active damping scheme is also incorporated in the overall current regulation system to meet system damping requirements. Based on this model conventional synchronous linear current regulation is adapted to yield desired control and waveform quality performance. Furthermore, a two-phase modulation scheme is presented for three-phase three-wire VSC systems. Frequency response analyses by means of the command to output and disturbance to output characteristics have been conducted for the conventional synchronous frame current regulation and the proposed IDMBC methods. After that simulations and experiments are conducted to verify the analyses. It is demonstrated that the proposed IDMBC method outperforms the conventional current regulation architecture both in terms of waveform quality and dynamic response characteristics.

In chapter 6, the thesis is summarized and future research potential is addressed.

It is worth to mention to prevent misconceptions that all the inductances are nonlinear and they are not indicated as a function of time or current for the sake of illustration simplicity except the sections describing conventional current regulation methods (section 3.2.1) which are based on linear inductors.



CHAPTER 2

SATURABLE INDUCTORS AND STATE OF THE ART

2.1 Introduction

This chapter reviews the state-of-the-art PWM-VSC technology on a fourfold basis firstly. After that, as in spite of its simpleness, it is widely known incorrectly, the theory of inductor saturation and the concept of incremental inductance are provided. The benefits of utilization of saturable inductors are presented. In accordance with these benefits, the core materials are reviewed and the superiority of saturable inductors (especially as the converter side inductors) is exemplified via inductor designs. These results demonstrate the viability of the utilization of saturable inductors in VSCs.

2.2 Voltage Source Converters

Voltage source converters are widely utilized in AC-DC and DC-AC power conversion applications of grid-connected energy systems such as active filter, regenerative drive, renewable, STATCOM, storage, battery charger, and uninterruptible power supply (UPS).

Typically in power ratings less than several kW single-phase converters are used. For 1P converters, the topology is commonly configured as full-bridge or as half-bridge. In higher power ratings three-wire three-phase converters or four-wire three-phase converters (consisting of three 1P HBs) are employed. In all cases, two-level converters emphasize low cost and high switching frequency; three-level topologies are favorable in high-efficiency applications [6]. PWM mode of operation is common

and designers select among various PWM switching methods.

In standard low-voltage grid ($230\text{ V}_{\text{RMS}}$ /phase and 50 Hz) tied systems, the converter design involves the well-matured silicon MOSFET and IGBT switches allowing switching in several tens of kHz at several kVA levels, while the switching frequency decreases to several kHz levels in hundreds of kVA rating applications. The energy conversion efficiency, cost, size, regulations (standards), and reliability are usually the major drivers shaping the VSC technology. Accordingly, the technology is enhanced basically in the fields of semiconductor technology, converter topology, PWM/control techniques, and filter topology. In the following, these fields are reviewed.

2.2.1 Semiconductor Technology

With the invention of mercury arc rectifier in 1902, the history of power electronics literally ushered more than 100 years ago. In 1926, thyatron devices had been introduced by GE. After that, magnetic amplifiers come into use. The period wherein these developments took place is considered as the classical era of power electronics [7].

In 1948, with the invention transistor, the solid-state revolution and the modern era of power electronics has begun. Phase controlled thyristors, triacs, gate turn off thyristors gradually emerged. Bipolar junction transistors and MOSFETs became popular due to higher frequency switching capabilities when compared to existing counterparts. With the invention of IGBTs, BJTs disappeared from the market as they require high gate currents. Later, the latching problem of IGBTs was resolved and commercialization of these devices is eased. At the same time, MOSFETs found more area in high-frequency low-voltage applications. In Figure 2.1, the state-of-the-art commercial controlled semiconductors are summarized by means of the device ratings.

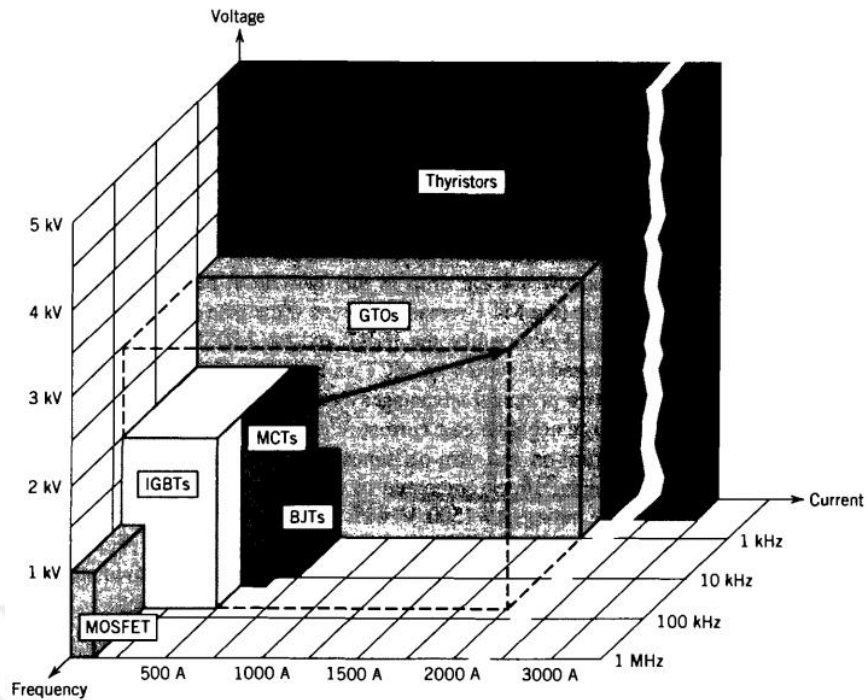


Figure 2.1: Summary of device capabilities [1].

Fast diodes with reduced reverse recovery charge also evolved within the modern era of power electronics. With these advancements, switching frequencies has been considerably increased and the filter size of the power converters normally could be decreased.

Silicon has been the fundamental material for power electronics switch realization until now. However, the introduction of wide bandgap materials seems to change the situation as they are promising in many practical aspects such as high switching frequency, high temperature, and high voltage capabilities [2]. Figure 2.2 shows how the SiC and GaN technologies are advantageous over conventional Si technology. Accordingly, the market share of these new wide bandgap semiconductor technologies is expected to greatly increase with a cumulative annual growth rate of 31 % towards 2023 [2]. It is expected that such improvements in semiconductor technology yielding higher switching frequencies and lower semiconductor losses will reduce overall cost, volume, and increase the energy conversion efficiency.

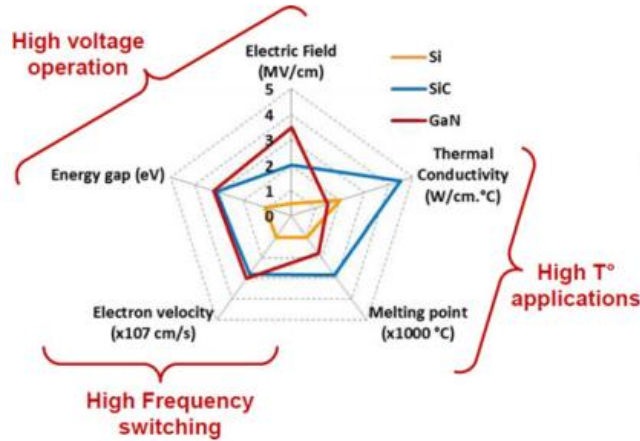


Figure 2.2: Performance comparison of Si, SiC, and GaN material based semiconductors [2].

2.2.2 Converter Topology

Even though the scarcity of the component types employed within the realization of power converters (a controlled switch and a diode), the number of topologies are quite large. Probably, buck, boost (which can be also accounted as an inverse buck), and buck-boost type DC-DC converters constitute the base for most of the invented power converter topologies. Switched capacitor type and Z-source type converters are the other complementary branches of power electronics topology families. Depending on the application requirements, power electronics converter topologies have been evolved from these basic configurations.

Interfacing with high voltage levels, for instance for the case of HVDC applications, multilevel topologies are developed [8] meeting the device ratings and output current waveform quality requirements.

Another branch of application that evolves converter topologies is transformerless photovoltaic inverters. As there is no galvanic isolation in these inverters and the photovoltaic modules are grounded due to safety reasons, there occurs a path for leakage current. In single-phase case, the leakage current is minimized by the introduction of new topologies [9]. For single-phase VSCs, further topologies are invented aiming to solve the intrinsic second-order power oscillation problem also [10]. Microinverters

(or module integrated converters, MIC) are also introduced into photovoltaic market around the beginning of the 21th century and gradually increased their share for distributed maximum power point tracking of the photovoltaic modules. Accordingly, thenceforward, many MIC topologies have been invented [11].

Covering a vast range of applications, the single-phase topology family has been expanding for the last decade. Among a large number of topologies, the basic and representative single-phase topologies are shown in Figure 2.3. In Figure 2.3(a) 1P-HB-VSC, probably the most basic element of single-phase VSCs, is shown. This topology can be conceived as buck or boost converter topology. The advantage of the topology is that there is a solid connection between the neutral and midpoint of the dc-link, hence leakage current problems, especially in PV applications, can be mitigated. The main drawback of the topology is the high current ripple of the filter inductor which is caused by only two-level output voltage. Thus more filtering is required with larger passives.

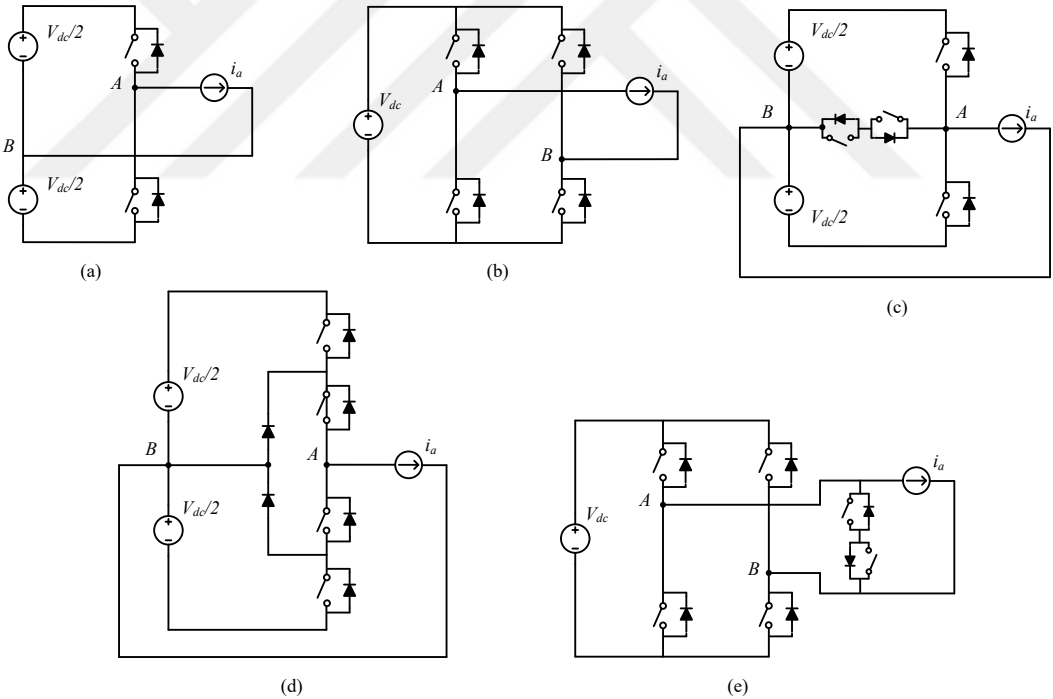


Figure 2.3: Single-phase VSC topologies. (a) 1P-HB-VSC. (b) 1P-FB-VSC. (c) 1P-3L-T-VSC. (d) 1P-3L-NPC-VSC. (e) 1P Heric VSC topology.

In Figure 2.3(b), 1P-FB-VSC topology is illustrated. This topology has three-level

output voltage when unipolar modulation is employed ($V_{dc}, 0, -V_{dc}$) yielding less filtering requirements when compared to 1P-HB-VSC.

Figure 2.3(c) shows the 1P-3L-T-VSC topology. This topology has also three-level output voltage in addition to neutral wire solid connection advantage. However, single-phase application of this topology creates low-frequency stress on the DC-link capacitors.

In Figure 2.3(d) the 1P-3L-NPC-VSC topology is depicted. Three-level output voltage and DC-link stress for single-phase applications is the same as the 1P-3L-T-VSC topology. However, the maximum voltage stresses experienced by the semiconductors is half of the DC-link. Hence, higher DC-link voltages can be reached with this configuration.

1P Heric VSC topology (Figure 2.3(e)) [9] is recently invented to mitigate the leakage current problems in PV systems at the same time conserving high efficiency with three-level outputs and a low number of semiconductors on the current path.

Three-phase VSC topologies, on the other hand, are relatively low in number when compared to single-phase VSC topologies. Here, the term three-phase VSC topologies refers to FB type topologies wherein the star point of the three-phases has no solid connection to the DC-side of the VSC. When there is a connection, the configuration can be called as HB type. The FB and HB discrimination is nothing but the same of three-wire three-phase and four-wire three-phase respectively. When the system is a three-phase HB type (or equivalently called three-phase four-wire type) the system dynamics and control becomes the same that of a single-phase counterpart. Thus the term three-phase within the context of this study corresponds to three-phase full-bridge (or equivalently three-phase three-wire) VSC systems. Figure 2.4 illustrates probably the most favourable 3P VSC topologies in the industrial low voltage applications. In Figure 2.4(a), 3P-2L-VSC topology is illustrated. The low number of switches eases the design and control. Therefore, the topology has become the most preferable topology in most low-voltage applications. Its major disadvantage of the two-level output voltage can be continuously improved with the increasing switching frequencies with the developments in the semiconductor technology, especially in wide bandgap devices.

In Figure 2.4(b) and (c), 3P-3L-T-VSC topology and 3P-3L-NPC-VSC topology are depicted respectively. These topologies have the advantage of the three-level output voltage. However, 3P-3L-T-VSC has less number of semiconductors on the current path as compared to 3P-3L-NPC-VSC topology. On the other hand, 3P-3L-NPC-VSC topology can extend higher voltage applications which is a good choice, for example, today's PV systems with a maximum DC-link voltage of 1.5 kV. Another issue in these three-level VSCs is their more DC-link capacitor requirement than their two-level counterpart [12]. In [13] further three-phase topologies are presented.

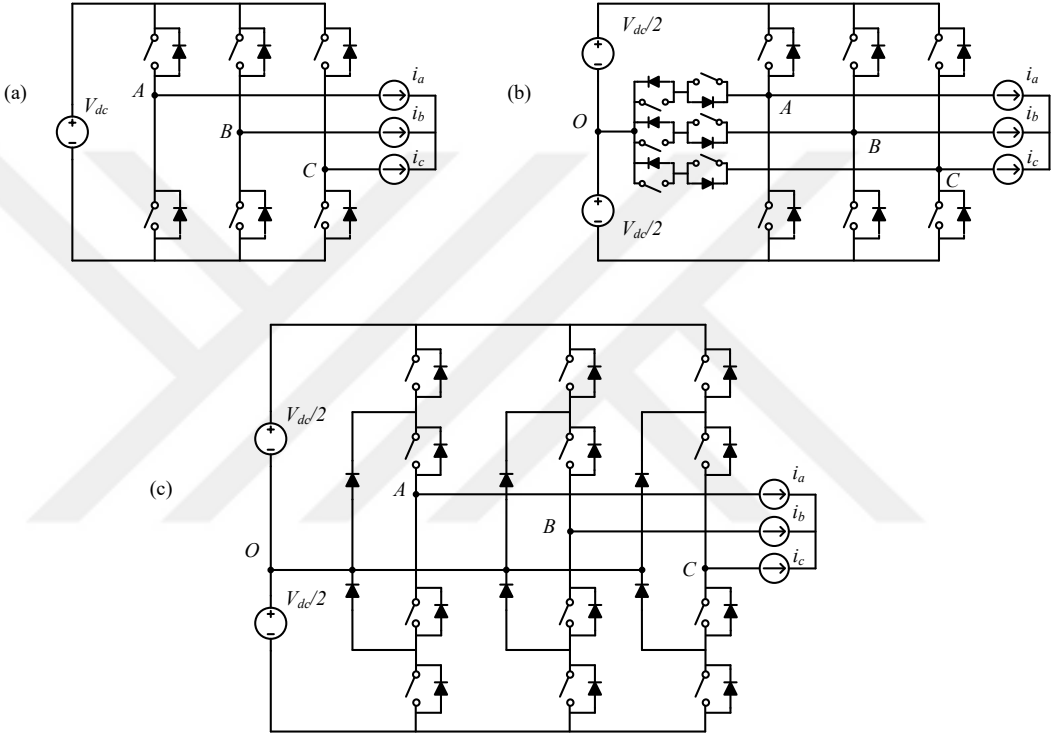


Figure 2.4: Three-phase VSC topologies. (a) 3P-2L-VSC topology. (b) 3P-3L-T-VSC topology. (c) 3P-3L-NPC-VSC topology.

2.2.3 PWM, Control, and Optimization

After the advancement of the semiconductor technology, the techniques that how and when the switches of a VSC are triggered gained great importance. Given a converter topology, the technique how the switching of the semiconductors are performed (or the PWM method) may affect the output voltage spectral characteristics, dc-link cur-

rent spectral characteristics, DC-link voltage utilization, and semiconductor losses greatly. Fixed carrier frequency is customary as the output voltage spectral (hence current spectral) characteristics are fixed. For grid-connected VSCs for example, such fixed spectral prevent resonant excitation of the LCL filter. However, in some applications, hysteresis controllers are still being used [14] and modifications are applied on the method to fix the spectral characteristics. Otherwise, linear current regulation has become the industry standard.

For 1P-FB-VSC topology, given fixed carrier frequency, bipolar and unipolar modulation can be performed with distinct output voltage spectral characteristics [1]. While the most dominant harmonic in the voltage spectrum is at the carrier frequency (f_c) for bipolar modulation, it is at $2f_c$ for unipolar modulation. Such a distinction yields different filtering requirements. Thus, the same VSC hardware requires less passive elements for filtering when unipolar modulation is employed.

Similarly, the effect of PWM technique employed in 3P3W VSC systems determines the DC-link current and output voltage spectral characteristics [12, 15]. The popular PWM techniques are thoroughly analyzed in [16] and characteristic waveforms for generating the final output voltage command are summarized in Figure 2.5. These waveforms are nothing but the scalar implementation of the methods wherein the generation rules are described in [17]. In the figure, sinusoidal PWM (SPWM) represents the raw output voltage command without injecting a zero-sequence voltage to the modulation signal. The linearity range of this simplest form without making use of the zero-sequence signal injection yields limited linearity range for the output voltage command (up to $M_i = 0.785$ where $M_i := \frac{2}{\pi} \frac{V^*}{V_{dc}}$). Other PWM methods shown in Figure 2.5 have a linearity range up to $M_i = 0.907$ [15, 17].

The zero-sequence signal generation of space vector PWM (SVPWM) can be performed by obtaining one of three sinusoidal output voltage reference signals with minimum magnitude and scaling it by 0.5 [17]. With such a zero-sequence injection, the active pulses are centered within a half carrier period in 2L-VSC inverters which yields improved harmonic characteristics [18]. Due to implementation ease, improved harmonic characteristics, and extended voltage linearity SVPWM became popular, especially in 2L-VSC inverter applications.

Centered Space Vector PWM (CSVPWM) is introduced in [19] to center the active vector pulses in the middle of a half carrier cycle to yield better harmonic characteristics in multi-level inverters. In 2L-VSCs the method converges to SVPWM. The zero-sequence signal of this method for 3L-VSCs is obtained in a manner similar to that of SVPWM [15, 18, 19].

Discontinuous PWM (DPWM) methods yield reduced switching losses, therefore switching frequency can be increased. Among them, DPWM1 method clamps the one of reference leg voltages having the highest magnitude to either positive or negative DC rail, so that switching losses can be reduced, especially at unity power factor mode of operation. In DPWM3 method, the reference leg voltage having the intermediate magnitude is clamped to either positive or negative DC link rail depending on the sign of that reference sinusoidal leg voltage.

In DPWMMAX method, the reference leg voltage having the largest value determines the zero-sequence signal such that, this voltage is clamped to the positive DC rail. A similar approach can be adopted for the smallest reference leg voltage to clamp to negative DC rail (DPWMMIN). In DPWMMAX and DPWMMIN methods, loss distribution of the semiconductors is asymmetrical. Moreover, for 3L-VSCs, the utilization of upper and lower DC-bus capacitors become unsymmetrical. Thus, DPWMMAX and DPWMMIN should be used interchangeably in a fundamental cycle.

In [20], a high performance generalized DPWM (GDPWM) method is presented. DPWM1 and DPWM3 methods become the special case of this method and the method has the advantage that it can be adopted to minimize switching losses depending on the displacement angle.

The DC-link stresses of the methods also differ from each other hence while designing the DC-link capacitors, associated characteristics should be taken into consideration [12]. For example, the utilization of DPWM methods requires very large DC-link capacitor size due to clamping of upper (or lower) DC-link capacitors [12].

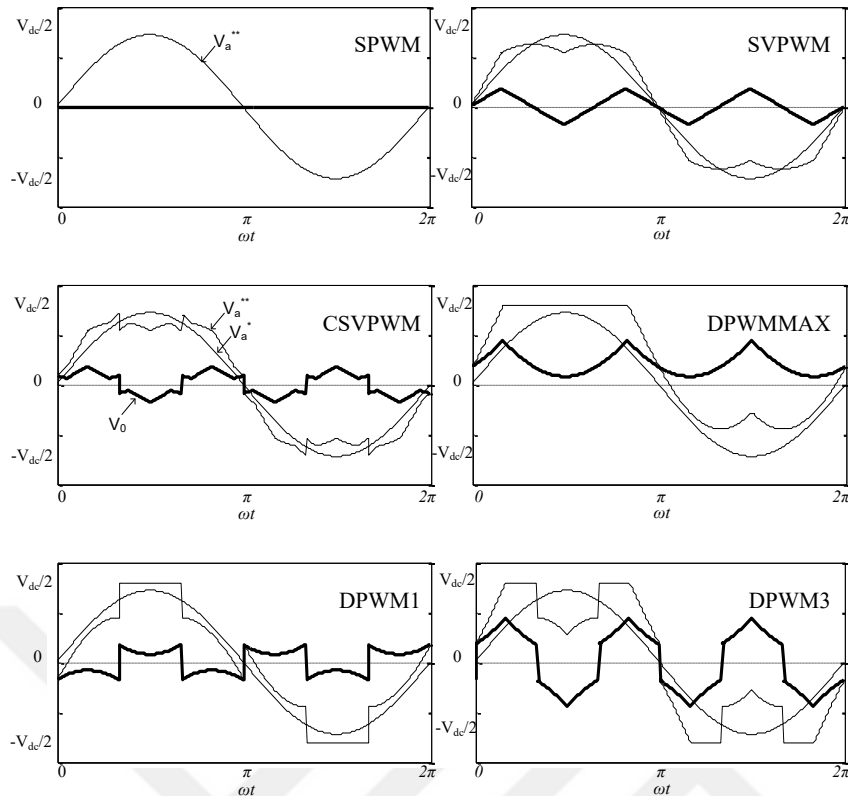


Figure 2.5: Generation of output voltage (V_a^{**}) of popular PWM methods for 3P3W VSC systems with the addition of zero sequence voltage (V_0) to the command voltage (V_a^*) for phase-a.

Without making any hardware modifications, the PWM method employed can greatly improve the VSC performance. Similar performance improvement can be realized via small hardware modifications such as interleaving and selective harmonic elimination methods. Moreover, optimization tools in the design can provide size and cost reduction as well as efficiency improvement. These approaches have a great contribution to today's VSC technology.

2.2.4 Filter Topology

The output of a VSC is composed of rectangular voltage pulses, wherein its harmonic spectrum involves the fundamental frequency and harmonic frequency components. When connected to a load (utility grid, ac machinery, etc.) the fundamental compo-

ment performs the power transfer to/from the load, which is the primary aim of the utilization of VSCs. On the other hand, high-frequency voltage harmonics cause performance degradation. In ac machinery case, the degradation is observed as torque ripple, excessive losses, and converter/machine power rating degradation. In the case of the grid connection of VSCs, harmonic currents give rise to power quality problems as well as power converter derating. Hence, certain standards exist to limit the injected harmonic current to the utility grid. Therefore, in both single-phase and three-phase VSC applications, the converter is interfaced with the grid (or the load) through ripple filter structures to meet grid code compatibility by restraining the total current harmonic distortion (THD_i) and individual harmonics [21]. In contrast to the vastness of the converter topologies, the filter topologies are relatively scarce.

The simplest filter type that can be used in the grid (load) connection is L filter. Such a filter has a PWM voltage to output current attenuation of 20 dB/decade. In spite of the topology simplicity and absence of resonance problems, L filter is not favored in the grid connecting of VSCs due to drawbacks such as high cost, large volume, excessive voltage drop and poor dc-link utilization, and poor dynamic characteristics.

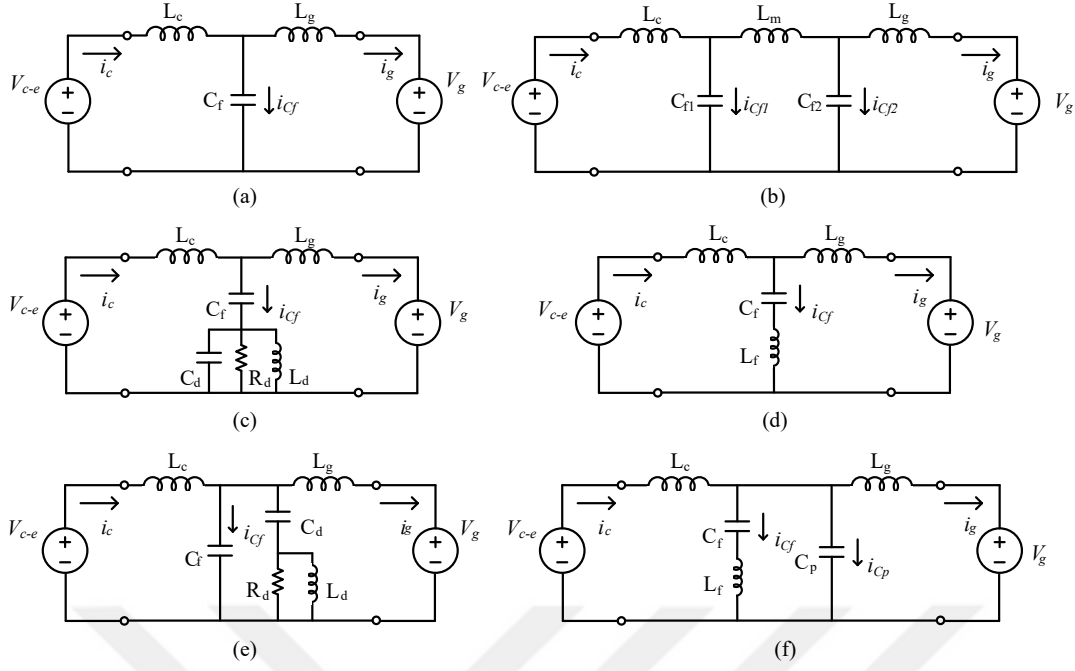


Figure 2.6: VSC output filter structures. (a) LCL filter. (b) Two-stage LCL filter. (c) Series R_d damped LCL filter with RLC damper. (d) LLCL filter. (e) Shunt R_d damped LCL filter with RLC damper. (f) LCL-LC filter.

Figure 2.6 shows the state-of-the-art VSC output filter topologies in a single-phase manner. In Figure 2.6(a) LCL type filter circuit diagram is depicted. This configuration provides an attenuation 60 dB/decade for the PWM harmonics [22]. As a result, less total inductance is required to meet grid standards as compared to L type filter. Therefore LCL filters provide significantly smaller size and reduced cost and improved control dynamics [21, 23–29]. However, due to the resonant poles in the filter transfer function (2.1), a resonant peak occurs in the frequency response hence the closed-loop system is unstable with conventional current regulation techniques. Therefore, the system should be stabilized by active or passive damping methods when grid current feedback is employed.

$$\frac{i_g(s)}{V_{c-e}(s)} = \frac{1}{s^3 L_c L_g C_f + s(L_c + L_g)}. \quad (2.1)$$

In the literature, the stabilization issue is resolved by means of active damping and passive damping methods. In the passive damping methods, a resistor is utilized

usually to damp the resonant spike of the filter. Such an approach results in additional losses and worsened filter characteristics [30]. On the other hand, in the case of active damping methods either capacitor current feedback, artificial active damping resistor, or cancellation of the resonant peak via inverse transfer functions are employed [26, 30–33]. When the converter side current feedback is employed, the current control system becomes inherently stable [30] and further stability margin can be provided via enabling an active damping term as performed in this thesis.

The Figure 2.6(b) shows the two-stage LCL filter. Although the topology has better attenuation characteristics than LCL filter at high frequency, the overall system has increased size, weight, cost, and complexity [22]. Further, regarding (2.2), the system involves two resonant peaks which makes the stabilization complicated.

$$\frac{i_g(s)}{V_{c-e}(s)} = \frac{s^2 C_{f2} L_g + 1}{s^5 L_c L_g L_m C_{f1} C_{f2} + s^3 [L_c L_m C_{f1} + L_g C_{f2} (L_c + L_g)] + s(L_c + L_g)}. \quad (2.2)$$

In Figure 2.6(c) the series damped LCL filter is illustrated with the damping circuit being a parallel RLC circuit. In [21, 34, 35] numerous passive damping topologies are presented. In [26], the series connection of the resistor is found to be efficiency effective method amongst other resistively damped configurations. In [21] and [35], however, the series connection of resistor is modified to this configuration allowing high-frequency current components to flow through the parallel capacitor (C_d) and low-frequency components to flow through the parallel inductor, hence resistive losses are aimed to be cut. The filter transfer function of this topology can be written as

$$\frac{i_g(s)}{V_{c-e}(s)} = \frac{s^2 a + sb + c}{s^5 d + s^4 e + s^3 f + s^2 g + sh} \quad (2.3)$$

where $a = L_d R_d (C_d + C_f)$, $b = L_d$, $c = R_d$, $d = L_c L_g L_d R_d C_f C_d$, $e = L_c L_g L_d C_f$, $f = R_d [L_d (C_f + C_d) (L_c + L_g) + L_c L_g C_f]$, $g = L_d (L_c + L_g)$, and $h = R_d (L_c + L_g)$.

Shown in Figure 2.6(d), Wu et al. proposed LLCL filter topology [36]. The parallel branch, in this case, is composed of series resonant LC circuit. By tuning this reso-

nant circuit to the carrier frequency, it is intended that the most dominant harmonics (around the carrier frequency) flows through the parallel branch. Hence, the grid side inductance (L_g) can be reduced. Regarding the filter transfer function (2.4), it seems, although the attenuation of the topology at the carrier frequency is quite sufficient at the carrier frequency, for higher frequencies LCL filter can exhibit better attenuation as the parallel branch starts to exhibit high impedance as the frequency increases beyond the carrier frequency. Due to resonant poles, the system should be stabilized as in the case of LCL filter topology. In [21] and [37] various passive damping techniques are provided. In [23] active damping method is elaborated for the topology.

$$\frac{i_g(s)}{V_{c-e}(s)} = \frac{s^2 C_f L_f + 1}{s^3 (L_c L_g C_f + L_c L_f C_f + L_g L_f C_f) + s(L_c + L_g)} \quad (2.4)$$

In Figure 2.6(e), parallel RLC damped LCL filter circuit topology is illustrated. As pointed in [21], the topology has low losses (found in [21] approximately 0.03 %). Further, the topology has 60 dB/decade attenuation in the high-frequency region. Hence, such configuration seems favorable among passive damped filters. The filter transfer function can be written as

$$\frac{i_g(s)}{V_{c-e}(s)} = \frac{s^2 a + sb + c}{s^5 d + s^4 e + s^3 f + s^2 g + sh} \quad (2.5)$$

where $a = L_d R_d C_d$, $b = L_d$, $c = R_d$, $d = L_c L_g L_d R_d C_f C_d$, $e = L_c L_g L_d (C_d + C_f)$, $f = R_d [L_d C_d (L_c + L_g) + L_c L_g (C_d + C_f)]$, $g = L_d (L_c + L_g)$, and $h = R_d (L_c + L_g)$.

Considering the LCL and LLCL filter topologies, the topology proposed in [38] (Figure 2.6(f)) provides better attenuation performance. Combining the parallel resonant branch and the parallel capacitor branch the filter has satisfactory attenuation both in the carrier frequency and in the high-frequency region. The filter transfer function of the filter topology can be obtained as in (2.6). Accordingly, the filter has two resonant frequencies, hence the filter suffers from stabilization issues, and increased complexity. In [38], passive damping is applied by series resistor insertion to the C_p hence, the system is stabilized. However, such insertion decreases high-frequency attenuation.

$$\frac{i_g(s)}{V_{c-e}(s)} = \frac{s^2 L_f C_f + 1}{s^5 L_c L_g L_f C_p + s^3 [L_c L_g (C_f + C_p) + C_f L_f (L_c + L_g)] + s(L_c + L_g)}. \quad (2.6)$$

Even a bouquet of filter topologies for VSCs exist, in all topology configurations, the converter side filter inductor experiences the rectangular voltage pulses and carries the load and PWM ripple current such that it is both electrically and magnetically stressed. With the present switching frequency levels, the converter side filter inductors with only several percent values of the base impedance suffice, decreasing the total size and cost of the converter. However, still after the power semiconductors, it is the costliest, lossiest, and largest element in the circuit. In accordance with these considerations, the next sections are devoted to the state-of-the-art converter side filter inductor technology with a focus on saturable inductors.

2.3 Theory of Inductor Saturation

When saturable inductors are employed as output filters, the flux increment ($\delta\lambda$) per current increment (δi) rapidly decreases as the operating current (i_0) magnitude increases. This phenomenon is called the saturation of the magnetic core. In Fig. 2.7, the phenomenon and corresponding inductance-current characteristics for the practical inductor which is made of sendust material as powder alloy are shown. The λ - i characteristics are obtained by subtracting resistive voltage drop from the applied sinusoidal voltage and then integrating the remaining voltage numerically. This inductor is used throughout the paper for obtaining simulation and experimental results. Similar to the linear inductor case, the terminal equation of a saturable inductor can be obtained as in (2.7). Evidently, the incremental inductance of the system decreases as the magnitude of current increases and the system becomes a nonlinear one as

$$v_L = \frac{d\lambda}{dt} = \frac{d\lambda}{di} \frac{di}{dt} = L \frac{di}{dt} \quad (2.7)$$

wherein L is the incremental inductance

$$L \triangleq \lim_{\delta i \rightarrow 0} \frac{\delta \lambda}{\delta i}. \quad (2.8)$$

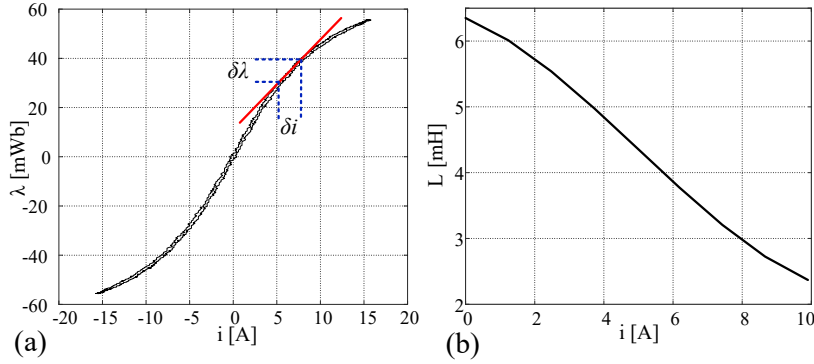


Figure 2.7: Experimental characteristics of the saturable inductor utilized throughout the investigation of this work. (a) λ - i characteristics. (b) L - i characteristics.

With the ESR of the inductor being R , the terminal equation of a saturable inductor is given as

$$v = L \frac{di}{dt} + Ri. \quad (2.9)$$

2.4 State-of-the-Art Inductor Technology in Voltage Source Converters

In the generic LCL filter structure converter side and grid side inductors are usually employed. When the power levels are slightly low, the utility grid impedance (including transformer leakage inductance, feeder inductance etc.) can be exploited as grid side inductor. And as the rating increases to a few kVAs and above the grid side inductors are involved intentionally.

Converter side inductors in the application are designed with fixed (single or multi) gap structures made of ferrite, amorphous steel, etc. material (Figure 2.8(a) and (b)) or with distributed airgap structures made of powder alloys, powder iron etc. (Figure 2.8(c)) [39–41]. The choice is made depending on the availability of the magnetic material, manufacturability, cost, EMC concern, efficiency, size, and weight requirements. Unlike the power modules and capacitors of VSC systems, the inductors are

typically custom made and state-of-the-art grid-connected VSC systems employ a variety of the above-discussed inductor designs. Amongst, inductors made of distributed airgap soft magnetic materials (powder alloys such as sendust, powder iron, etc.) are often favored for their low core loss, high volumetric energy density, and acceptable cost [42, 43]. However, most such inductors have deep magnetic saturation characteristics, especially when made cost-effective [43]. While the magnetic saturation of the inductor is favorable in terms of cost and size reduction, it affects the converter performance characteristics adversely by shrinking the current control bandwidth and generating low order current harmonics. Thus, the inverter current control dynamic performance and steady-state current waveform quality substantially degrade.

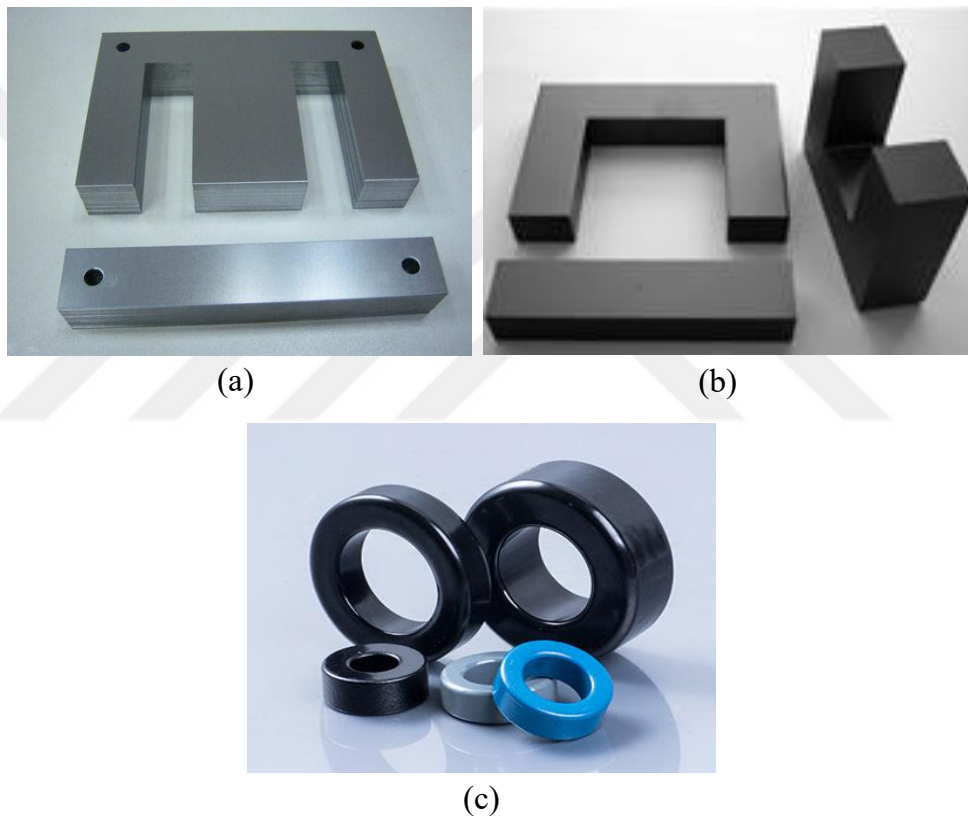


Figure 2.8: State-of-the-art inductor core materials. (a) Air gapped silicon steel laminations. (b) Air gapped ferrites. (c) Distributed gap powder materials.

Throughout the study, the term saturable inductor corresponds to inductors that normally (within the rating range) enter the deep magnetic saturation region (by design, due to cost and filtering advantages).

2.5 Utilization of Saturable Inductors in Voltage Source Converters

In general, in DC-AC power supply and grid-connected VSC applications, the inverter is interfaced with the grid (or the capacitor) with an inductor. The inverter generated pulsating voltage waveforms result in a current waveform which has a commanded (fundamental) frequency main component and the triangular current ripple waveform which has harmonic spectrum PWM ripple at the switching frequency and its multiples. In the application field, such inverter side inductors are designed from a variety of magnetic materials in various geometrical designs depending on a large number of factors. The factors included in the design material and technique are quite variant depending on the application requirement. Power and frequency ratings are primarily important. Then the availability of the magnetic material involves not only economic factors, but geographical limitations also. While in the field of power electronics many basic components essential for the manufacturing of a converter are standardized and vary by limited dimensions by manufacturer, the magnetic components are far from standardization. Power transistors in terms of ratings, packaging, performance characteristics, etc. are quite standard. Similarly, microcontrollers and signal processors are with more or less similar fundamental characteristics. Capacitors are similarly standardized in terms of packaging and material used and main properties. However, inductors are not standardized yet. In general, it is possible to state that at very low switching frequencies and large current (and power) ratings the magnetic design involves silicon steel laminations with thin laminations, typically multi gapped airgap design, and multi-turn windings. For example, applications involving frequencies less than 10 kHz, current levels of hundreds of amperes, involving inductances of several percent or more values, require this solution. As the switching frequency increases to tens of kHz level, then the silicon steel lamination becomes prohibitive due to significantly increasing losses. At such frequencies, the options appear as amorphous steel, nanocrystalline material, powder material etc. Here the winding technique also involves multistranded wires, sheet conductors, etc. While the amorphous material and nanomaterial are designed with airgap, and depending on the inductor ratings, this design may involve multi-gapping technique making the manufacturing more challenging. The powder material, depending on the available geometries and the winding machines may be attractive for mass production cases.

At frequencies above several tens of kHz, the magnetic material becomes mainly powder metal type. Ferrites (also recently nanocrystalline materials) and low loss powder alloys become the choice depending on the application. While the ferrite inductors are built with airgaps (fringing may cause additional losses and increase radiated EMI), in the powder alloys such as Sendust, MPP, FeSi material, the distributed airgap nature of the material is typically of toroidal type and the external field is also well controlled. As a result, the field is well contained for EMC performance purposes also.

To summarize, the powder alloy magnetic material technology, which involves sendust, powder iron, MPP, etc. materials, has applications ranging from several kHz to several hundred kHz and above applications with stable inductance characteristics with minimal temperature and ageing dependency [44]. When using all such materials effectively, the inductor becomes a saturable inductor and the control performance issues arise.

In Figure 2.9, the variation of the L-i characteristic of the utilized magnetic core with respect to number of turns is illustrated which makes the reason behind the utilization of the cores in their saturation region clearer (This curve is obtained from the DC bias curve provided in the datasheet of the core). As shown in the figure, the drastic increase of the inductance with the number of turns ($L = N^2/R$ where L is inductance, N is the number of turns, and R is the reluctance of the core at the excitation level) makes saturation of the inductor favorable. The increase in the inductance is proportional to the number of turns and the decrease in the inductance (as the current increases) is linked with the bias (Ampere-turn) and the core characteristics.

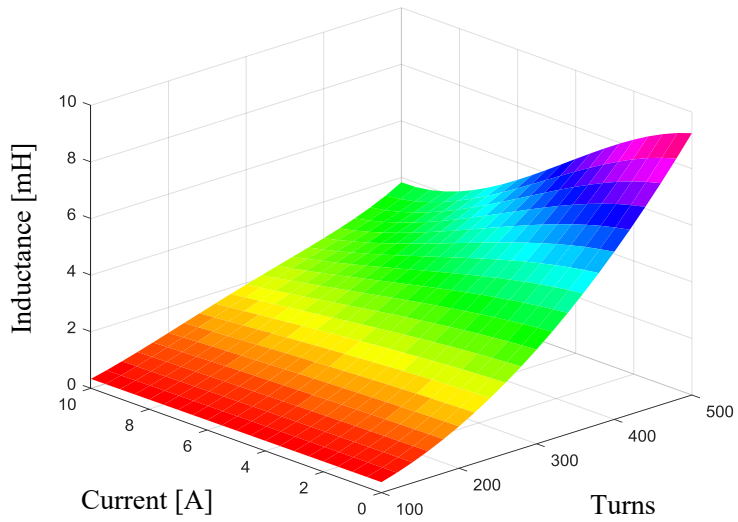


Figure 2.9: Inductance characteristics of a sendust core with respect to turn numbers and current [3].

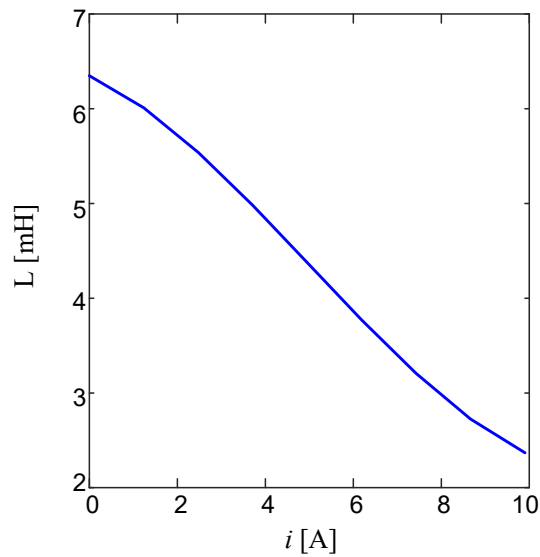


Figure 2.10: Single-phase inductance vs. current characteristics.

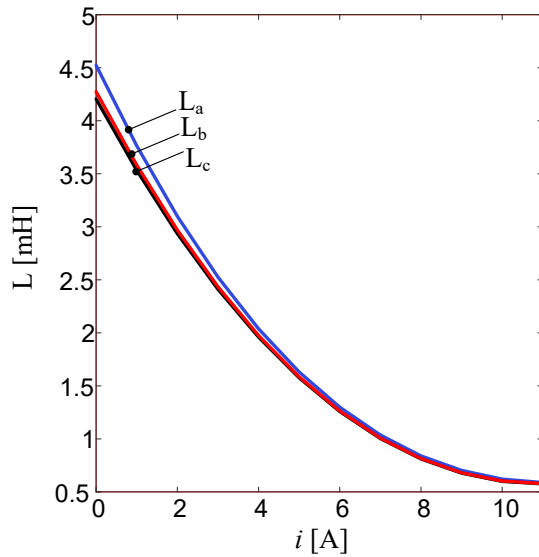


Figure 2.11: Three-phase three-wire inductance vs. current characteristics.

In Figure 2.10 the L - i characteristic of the inductor manufactured for single-phase VSC system experiments is illustrated. In Figure 2.11, the L - i characteristics of the three inductors manufactured for three-phase three-wire experiments are illustrated. The inductance decreases to approximately one-third of the initial value in single-phase case whereas the decrease is to approximately $1/9^{th}$ in three-phase inductors due to balancing effect of the three inductors in 3P3W VSC systems.

2.6 Motivations on the Utilization of Saturable Inductors

The cost, weight, and efficiency benefits of the utilization of saturable inductors may not be apparent in the first sight. Hence, this section aims such a clarification of these benefits.

The practical inductor core materials can be basically classified as laminated silicon steel, ferrite, and powder materials. Depending on the application requirement such as cost, efficiency, and weight, the choice is made. Among the materials, silicon steel exhibits weaknesses in terms of increased core losses due to eddy current losses in spite of the laminated structure [45].

On the other hand, when compared to powder core materials, air-gapped ferrite is the

cheaper solution per weight. Moreover, the inductance characteristics can be made almost linear by adjusting the airgap. However, even if they are not saturated fully, powder materials have advantages over gapped ferrite cores (as well as silicon steel cores as they include air gap also) [4]:

- Powder cores do not have fringing losses whereas gapped ferrite cores suffer excessively these losses.
- Powder cores are inherently fault-tolerant due to their continued inductance characteristics whereas ferrite cores are not.
- Flux capacity of ferrite cores decreases with temperature increase whereas that of powder cores are relatively constant.
- Powder cores exhibit excellent EMI performance whereas gapped ferrite cores do not due to fringing flux, which may be prohibitive in power converters requiring low noise levels.

Therefore, powder core materials are preferable (or at worst comparable when a very cheap design is required) over gapped ferrite in power electronics applications especially in VSCs, more specifically as converter side inductors, even if they not fully saturated. Figure 2.12 exemplifies the permeability vs. DC bias characteristics of an equivalent gapped ferrite and two powder core materials.

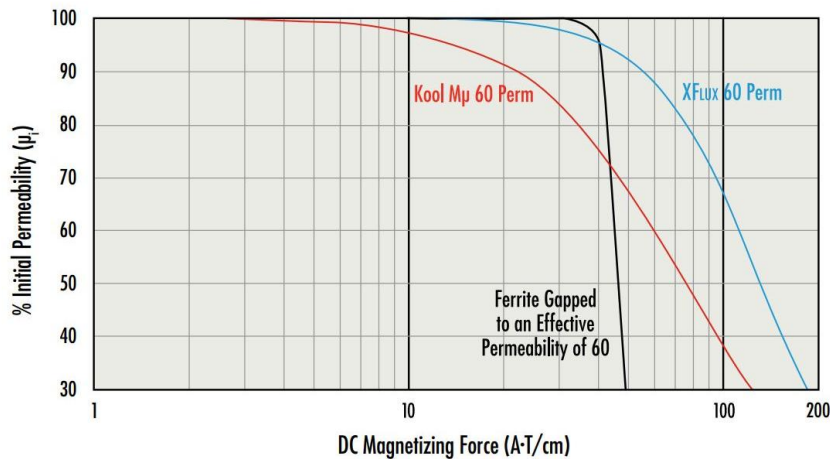


Figure 2.12: Permeability vs. DC bias characteristics of powder materials and gapped ferrite [4].

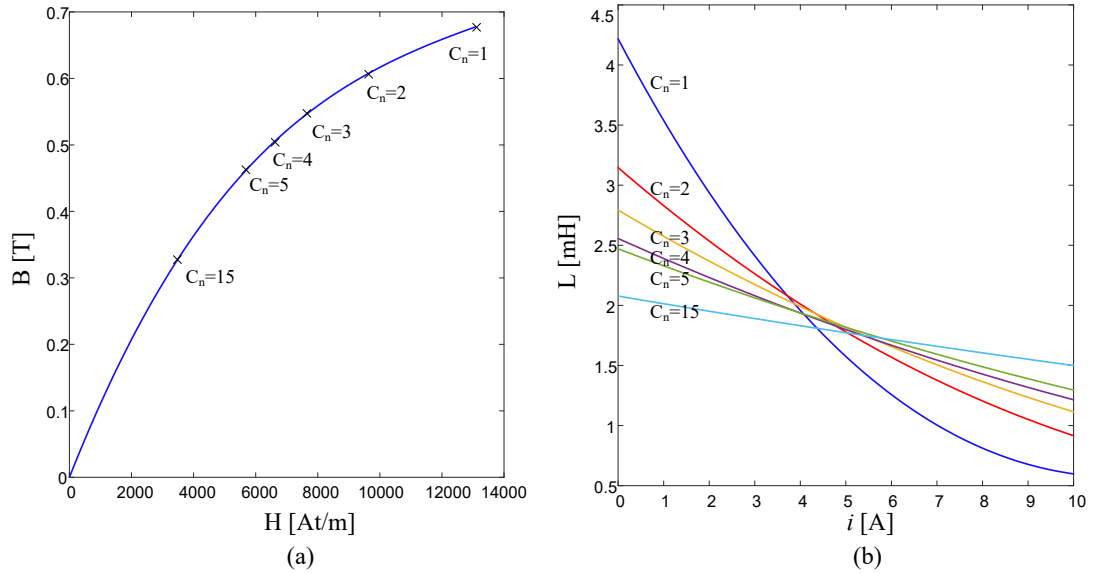


Figure 2.13: The L-i characteristics of the inductors with the same core [5] with various stack numbers and with the same average inductance.

The benefits of utilization of powder cores in their saturation region are quantified via inductor design examples. The designs are performed for the same core (sendust 90μ) [5]. For each design different core numbers are paralleled (stacked) and the number of turns (N) for each stack is adjusted to yield the same average inductance for all designs by making use of the DC-bias curve provided in the core datasheet. The average inductance is 1.95 mH which is the average inductance of the initial single-core design. The rated current is $10 A_{\text{peak}}$ for all designs hence same copper wire can be used for each design. As the window area constraint is not violated for the single core case, it is guaranteed that the constraint will not be violated for higher core numbers with a smaller number of turns than that of single-core design.

In Figure 2.13, the resultant characteristics of the inductor designs are summarized. The characteristics given by the core number 1 ($C_n = 1$) is physically implemented by 150 turns.

The Figure 2.13(a) illustrates the maximum operating point on the B-H curve of each design. It should be noted that as the paralleled core number is doubled, N is not halved but approximately divided by $\sqrt{2}$ to keep the average inductance same. For example for $C_n = 1$, $N = 150$, and for $C_n = 2$, $N = 106$. Therefore, the maximum

operating point reached for each paralleled core number in Figure 2.13(a) does not approach to the linear region instantly. Accordingly, after paralleling 15 cores with approximately 40 turns, the L-i characteristics become almost linear. A conundrum can be led that in practice paralleling of such a number of cores are not preferred due to mechanical implementation issues and instead design is realized via larger cores. In this case, even copper losses may be reduced with the utilization of larger cores in the design, such an approach will increase the required core volume, hence core losses. Thus, paralleling of the same cores constitutes a good basis for comparison of linear and nonlinear inductor designs.

In Figure 2.13(b), the obtained L-i characteristics are illustrated. As the average inductances of these cores are the same, it becomes apparent that using powder cores in a saturated manner yields great reduction in the core material. Furthermore, the copper required in saturable design is slightly less than the linear design as the length of the copper required is approximately linearly proportional to C_n but the reduction in the number of turns is not that much, approximately $N \sim 1/\sqrt{C_n}$. Therefore, the copper cost and losses with the same thickness of wire is more in linear design than of a saturable inductor design.

In Figure 2.14, the inductor losses are illustrated with respect to the stacked core number. In the calculation of losses, 10 A_{peak} 50 Hz sinusoidal fundamental is considered with 2.5 A_{peak-to-peak} ripple component at 20 kHz. The ripple component is taken the same for all designs, with the consideration that each of the designs has the same average inductance.

In the calculation of copper losses, end windings' lengths are assumed constant as the stacked core numbers are increased. Thus, in the figure, a slight decrease in the copper losses as the number of stacked cores is increased from 1 to 2. However, the copper losses increase with further increment of the core number. This increase is simply due to the linear increase of a turn length with C_n whereas the decrease in the turn number is proportional to approximately $\sqrt{C_n}$. Thus the overall length of the turns increases as C_n is increased yielding more copper losses.

In the case of core losses, on the other hand, the core losses are calculated for each flux harmonic component based on the method 3 in [46]. The low-frequency flux

harmonics caused by the saturation and the fundamental frequency due to excitation of the core results in very low core losses (less than 50 mW in total for the first 11 harmonics involving the fundamental) due to high dependency of the core losses to frequency. Accordingly, the majority of the core losses are caused by the high-frequency ripple component in the flux density.

This example calculation of the inductor losses illustrates that the inductor losses increase when more "linear" designs are preferred with the same core magnetic characteristics. Thus, one can conclude that utilizing inductor cores (especially powder cores) as saturable cores is advantageous in terms of efficiency as well as cost, size, and weight.

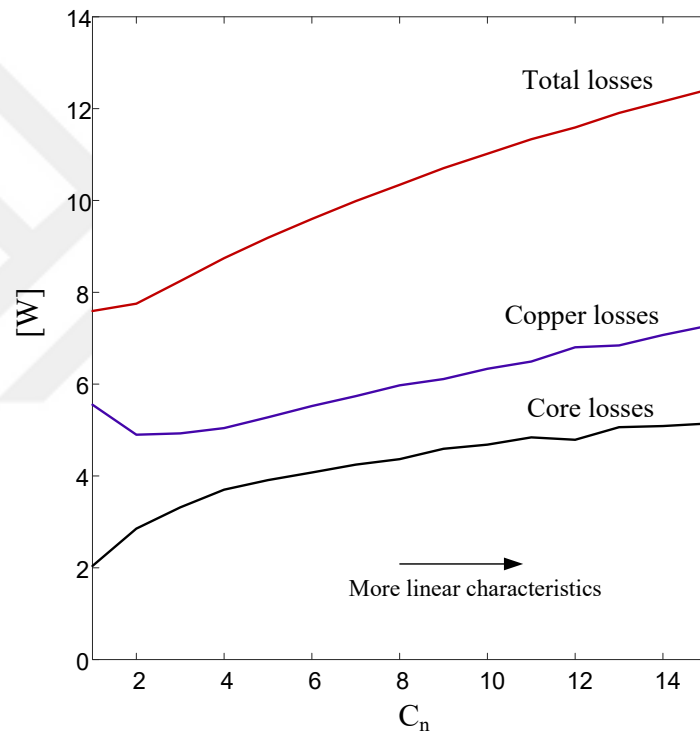


Figure 2.14: Inductor losses with respect to stacked core number yielding the same average inductance.

2.7 Summary

In this chapter, the technological development of VSCs is reviewed. Then, the theory of inductor saturation and the concept of incremental inductance are presented. The

inductor technology in VSCs is also reviewed. Moreover, the motivations with the use of saturable inductors (cost, size, and efficiency improvements) are discussed. These discussions demonstrate that, with the utilization in a saturated manner, the powder core size and cost can be considerably reduced and inductor losses can be cut. In [43] such benefit is demonstrated for a high power application without the waveform quality and bandwidth shrinkage problems addressed. In chapter 3, these issues are clarified both for 1P controlled and 3P3W VSC systems.



CHAPTER 3

VOLTAGE SOURCE CONVERTERS EMPLOYING SATURABLE INDUCTORS

3.1 Introduction

In this chapter, the investigation of conventional linear current control methods and associated problems with the use of saturable inductors is conducted for 1P and 3P3W VSC systems. First, state-of-the-art current controllers for 1P controlled and 3P3W systems are reviewed. Critical implementation issues such as phase-locked loop and disturbance decoupling are discussed. Then, in spite of the simplicity of the understanding and the implementation and the appreciated performance in linear inductors, the drawbacks of conventional linear current controllers with the utilization of saturable (nonlinear) inductors are investigated. Namely, these drawbacks are bandwidth shrinkage and waveform quality distortion which are very critical both for, but not confined only to, 1P controlled and 3P3W VSCs.

3.2 State of the Art

Voltage-source converters (VSCs) are widely utilized in AC-DC and DC-AC power conversion applications of grid-connected energy systems such as active filter, regenerative drive, renewable, statcom, storage, uninterruptible power supply (UPS). Typically in power ratings less than several kW single-phase (1P) converters are used. For 1P converters, the topology is commonly configured as full-bridge (FB) as shown in Figure 3.1(a) or as half-bridge (HB).

In higher power ratings, three-phase four-wire (3P4W) converters (consisting of three

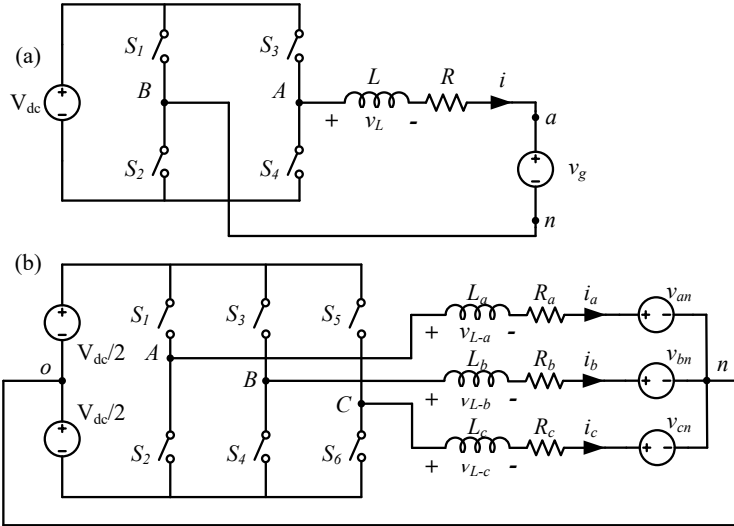


Figure 3.1: Single-phase controlled grid-connected VSC topologies. (a) 1P FB. (b) 3P HB.

1P HBs hence alternatively called 3P HB, see Figure 3.1(b)) are employed. The control of 3P4W VSCs is the same that of 1P VSCs, as each leg voltage (or called pole voltage) directly determines the current of the associated phase. Therefore, by means of control architecture, 3P4W VSCs belong to the category of 1P controlled VSCs. When the $o - n$ connection is removed from the 3P4W VSC system, 3P3W VSC system is obtained. In spite of the simplicity, the outcomes of such a modification are significant. In the first place, zero-sequence voltage can be injected in the VSC output voltage which provides the following benefits. The injection enables better DC-bus utilization conserving the linearity up to 15 % [16]. Furthermore switching losses can be significantly reduced by making use of discontinuous PWM methods, hence switching frequency can be increased. Moreover, the PWM voltage stress of the inductors can be decreased by adjusting the voltage vector sequences within a PWM period. These benefits make 3P3W systems advantageous when applicable. In the second place, the current control of 3P3W VSC systems are distinct from the control of 1P controlled systems which will be discussed in section 3.2.1.

In all cases, two-level converters emphasize low cost and high switching frequency; three-level topologies are favorable in high-efficiency applications [6]. PWM mode of operation is common and designers select among various PWM switching methods.

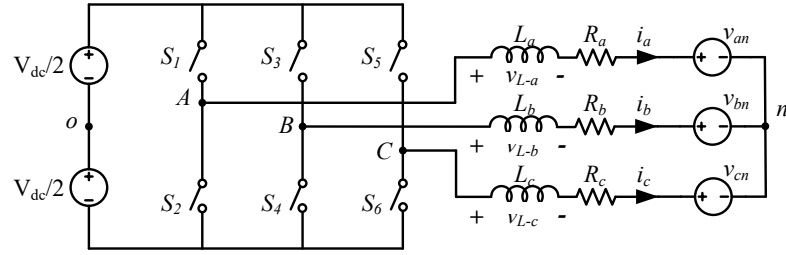


Figure 3.2: Two-level 3P3W grid-connected VSC topology.

In standard low-voltage grid (230 V_{RMS}/phase and 50 Hz) tied systems, the converter design involves the well-matured silicon MOSFET and IGBT switches allowing switching in several tens of kHz at several kVA levels, while the switching frequency decreases to several kHz levels in hundreds of kVA rating applications. In all these applications, the converter is interfaced with the grid (or the load) through LCL ripple filter structures to meet grid code compatibility by restraining the total current harmonic distortion (THD_i) and individual harmonics [21]. The converter side filter inductor experiences the rectangular voltage pulses and carries the load and PWM ripple current such that it is both electrically and magnetically stressed. After the power semiconductors, it is the costliest, lossiest, and largest element in the circuit. With the present switching frequency levels, filter inductors with only several percent values of the base impedance suffice, decreasing the total size and cost of the converter.

Converter side inductors in the application are designed with fixed (single or multi) gap structures made of ferrite, amorphous steel etc. material or with distributed air-gap structures made of powder alloys, powder iron etc. [39–41]. The choice is made depending on the availability of the magnetic material, manufacturability, cost, EMC concern, efficiency, size, and weight requirements. Unlike the power modules and capacitors of VSC systems, the inductors are typically custom made and state-of-the-art grid-connected VSC systems employ a variety of the above-discussed inductor designs. Amongst, inductors made of distributed airgap soft magnetic materials (powder alloys such as sendust, powder iron, etc.) are often favored for their low core loss, high volumetric energy density, and acceptable cost [42, 43]. However, most such inductors have deep magnetic saturation characteristics, especially when made cost-effective [43]. While the magnetic saturation of the inductor is favorable in terms of cost and size reduction, it affects the converter performance characteristics adversely

by shrinking the current control bandwidth and generating low order current harmonics. Thus, the inverter current control dynamic performance and steady-state current waveform quality substantially degrade.

This chapter investigates the 1P (also the investigation is valid for 3P HB VSCs) and 3P3W VSCs with highly saturable inductors in terms of their performance characteristics and proposes an efficient method to overcome the inductor saturation based performance degradation of conventional current regulation (CCR) methods.

3.2.1 Current Regulators for VSC Systems

Current regulation is the standard approach in most VSC applications due to its advantages of high current waveform quality and fast dynamic characteristics. The following are the features of a high-performance current controller [47]:

- No phase and amplitude errors over a wide frequency range
- High dynamic response (small rise and settling time)
- Limited or constant switching frequency to guarantee the safe operation of the semiconductor switches
- Low harmonic content in the output current
- High DC-link voltage utilization
- High disturbance rejection performance
- Stable operation
- High energy conversion efficiency.

In current regulated VSCs, typically linear current controller structures (PI, PI+R) with load voltage decoupling are used. These conventional linear current controllers provide constant switching frequency and hence stationary harmonic spectrum when compared to hysteresis type controllers. This attribute of linear current controllers makes them suitable for grid-connected VSC applications by keeping the resonant

frequency band of the output filter quiet. Furthermore, the safe operation of the semiconductor switches is provided. Therefore these linear controllers are described as conventional current regulators (CCRs) within the context of this thesis. In this section, CCRs are reviewed for 1P controlled and 3P3W VSC systems with linear inductors.

3.2.1.1 Current Regulators for Single-Phase Controlled VSC Systems

Figure 3.3 shows the conventional linear current regulation control block diagram for 1P systems with linear inductors. In the figure, L-R block represents the load having the admittance transfer function of $G_p(s) = (sL + R)^{-1}$, and v_d represents the disturbance voltage ($v_D = v_g + v_{id}$, where v_g is load voltage and v_{id} is inverter generated disturbance due to dead-time, measurement errors, and switch nonidealities). The total time due to feedback signal measurement, computation, and PWM delays of the inverter is represented with a unity gain first order delay function ($G_d(s) = (1 + s\tau_d)^{-1}$, where τ_d is the total equivalent time delay in seconds) [48]. For the basic control loop behavior analysis, as the plant pole (electrical time constant) dominates the control behavior, this delay block is neglected. By decoupling the load voltage and neglecting the delay block, the closed-loop transfer function (CLTF) of the system can be given as (3.1) where $G_c(s)$ is the linear compensator transfer function in s-domain:

$$\frac{I(s)}{I^*(s)} = \frac{G_c(s)}{G_c(s) + sL + R} \quad (3.1)$$

wherein $I(s)$ and $I^*(s)$ denote the s-domain current and current command respectively. The bandwidth (the cutoff frequency of (3.1)) of the overall system can be determined by the linear current controller parameters. As the bandwidth is increased, the ability of the system to track higher frequencies is improved. Therefore, faster response and better harmonic regulation performance can be obtained. Furthermore, higher bandwidth characteristics yield higher disturbance rejection performance [49]. However, in VSCs, bandwidth of the system cannot be increased without bound either due to the carrier frequency (f_c) limitation. For the FB 1P VSC with unipolar modulation under double sampling, the maximum achievable value of the bandwidth (ω_{BW-UL}) is $2\pi f_c/10$ rad/s [50]. Thus, in the controller design this upper should be

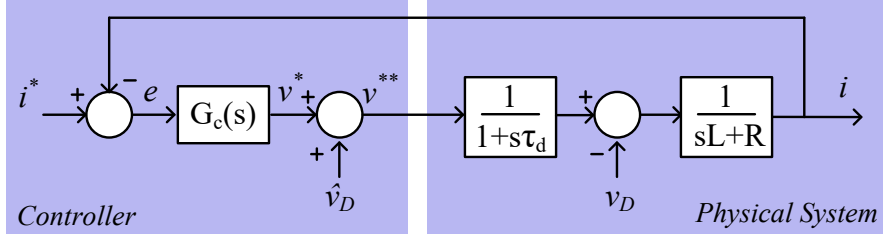


Figure 3.3: Simplified 1P controlled VSC system model and conventional current control block diagram for R-L-E type load.

taken into account which is discussed in the following sections.

The design of $G_c(s)$ for 1P VSCs is a well-known subject. In DC-DC conversion applications, PI controllers are widely used as they exhibit satisfactory performance with high gain for low-frequency signals. This advantage of PI controllers is exploited in AC applications by transferring AC signals to the synchronous reference frame wherein those signals are seen as DC quantities when phase locking is performed accurately. In [51], it was shown that, theoretically identical zero steady-state error performance that of a PI regulator in the synchronous frame for AC signals can be obtained in stationary frame with the use of ideal proportional-resonant (PR) compensation network without the necessity of transforming the stationary frame signals to the synchronous frame. In practice, a damped version of the ideal PR compensator that solves implementation issues such as imperfect realization due to finite precision in digital systems and grid frequency variation is employed [52]. An integral term may be incorporated into the PR controller in order to suppress any low-frequency current harmonics. Similarly, the use of resonant controller can be extended to other harmonics when needed. The generalized form of the transfer function of the PI+R compensator can be formulated as in (3.2) in s-domain

$$G_c(s) = K_p + \frac{K_i}{s} + \sum_{k=1}^n K_{r-k} \frac{2\zeta_k k\omega_e s}{s^2 + 2\zeta_k k\omega_e s + (k\omega_e)^2} \quad (3.2)$$

Herein, K_p (proportional gain) responds to current error instantaneously (and hence determines the bandwidth); K_i (integral gain) term establishes high gain for low-frequency signals; and K_{r-k} (resonant gain) is responsible for steady-state error minimization of k^{th} frequency component ($k\omega_e$, which is $k2\pi50$ rad/s for 50 Hz system).

When designing $G_c(s)$ for constant inductance (linear) systems, it is common practice to cancel the physical system pole (at $s = -R/L$) by setting directly $K_p = \omega_{BW} \times \hat{L}$ and $K_i = \omega_{BW} \times \hat{R}$ [50] where ω_{BW} is the design bandwidth in rad/s, \hat{L} is the estimated inductance, and \hat{R} is the estimated resistance. However, when using highly saturable inductors (resulting in a nonlinear system), and assuming constant inductance and resistance with CCR, the system performance degrades substantially. Such variation of the inductance results in two fundamental issues in 1P VSCs as explained in the section 3.3.

Recently, research has been conducted to solve the inductor saturation based performance loss issues for 1P VSCs. In [53], current regulation performance is restored but the algorithm ensures stability for a limited inductance range. In [54] and [55], proportional control gain scheduling method is proposed to improve the performance. In these studies, the compensator is comprised of proportional gain only without integral and resonant components. Therefore low frequency and fundamental frequency excellence in the current waveform is lost. Another similar approach in [56] is presented for 1P boost converter for power factor correction applications. In all these studies, in addition to the controller structure insufficiency, the equivalent resistor (ESR) of the inductor is neglected. When designing saturable inductors for such applications, the number of turns is usually high as compared to linear inductors, and the ESR is non-negligible. Furthermore, the semiconductor and cable losses also contribute to system dynamics with a resistive effect. Therefore, these methods provide limited performance. In [57], a repetitive control scheme is proposed to reduce low-order harmonics. However, the dynamic performance of repetitive control schemes is limited. Similarly, in the aforementioned studies, bandwidth shrinkage problem is not investigated in depth.

3.2.1.2 Current Regulation in Three-Phase Three-Wire VSC Systems

Similar to the case of 1P VSCs, current control of 3P3W VSC systems is thoroughly studied in the literature. In [58] and [47], it was shown that the stationary frame PI current regulators eventuate significant steady-state error in the output current waveform. As a measure, stationary frame PI current regulator can be modified as a PI+R

controller [58] providing sufficient gain, hence zero steady-state error, at the electrical frequency ω_e . On the other hand synchronous frame aligned with the grid voltage space vector is frequently employed in the field due to its zero steady-state error characteristics that of stationary frame PI+R stationary frame current regulator. Furthermore, the utilization of synchronous frame current control has become industry standard due to its ease of d-axis and q-axis (real/reactive) current control.

The implementation of 3P3W VSC synchronous frame conventional current regulation (CCR3) is based on space vector representation of continuous-time real variables. For a 3P3W VSC system the space vector of a three-phase variable can be described as

$$X_{abc} = \frac{2}{3}(X_a + aX_b + a^2X_c) \quad (3.3)$$

where $a = e^{j\frac{2\pi}{3}}$ and X_a , X_b , and X_c denote instantaneous values of phase variables such as voltages or currents. With such a transformation, three-phase variables can be represented by a single vector rotating with ω_e .

On a synchronously (usually synchronous with the space vector to be transformed) rotating frame (or called dq-frame) the space vector X_{abc} can be represented as DC quantities according to

$$X_{dq} = X_{abc}e^{-j\theta} \quad (3.4)$$

where $\theta = \omega_e t$.

The real and imaginary components of X_{dq} form the d-axis and q-axis components respectively

$$\begin{aligned} X_d &= \text{Re}\{X_{dq}\} \\ X_q &= \text{Im}\{X_{dq}\}. \end{aligned} \quad (3.5)$$

Based on these representations, the synchronous frame current control can be realized via complex variables (X_{dq}) or scalar variables (X_d and X_q) without a change in the performance unless distinct controller parameters are used. In Figure 3.4, these

transformations up to here in this section is visualized for the provision of better insight.

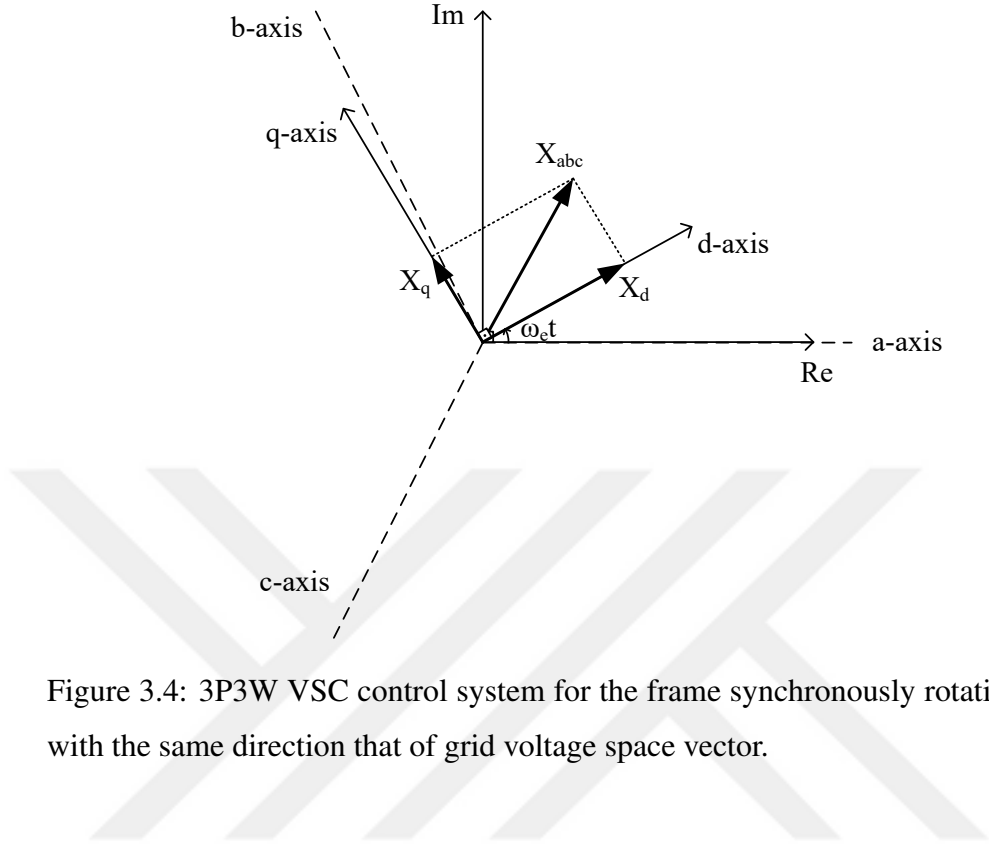


Figure 3.4: 3P3W VSC control system for the frame synchronously rotating with ω_e with the same direction that of grid voltage space vector.

Assuming linear elements and balanced operation, the 3P3W R-L circuit can be described by the state equations as

$$\begin{aligned} v_a &= L \frac{di_a}{dt} + Ri_a \\ v_b &= L \frac{di_b}{dt} + Ri_b \\ v_c &= L \frac{di_c}{dt} + Ri_c. \end{aligned} \quad (3.6)$$

By using (3.3), (3.4), and (3.5); the 3P3W R-L circuit that of Figure 3.2 can be described in dq-frame as

$$\begin{aligned} V_d &= L \frac{di_d}{dt} - \omega Li_q + Ri_d \\ V_q &= L \frac{di_q}{dt} + \omega Li_d + Ri_q \end{aligned} \quad (3.7)$$

with the assumption that the grid voltage and other known disturbances are decoupled. The form of (3.7) describes a cross-coupled control system in which V_d and V_q are the control inputs.

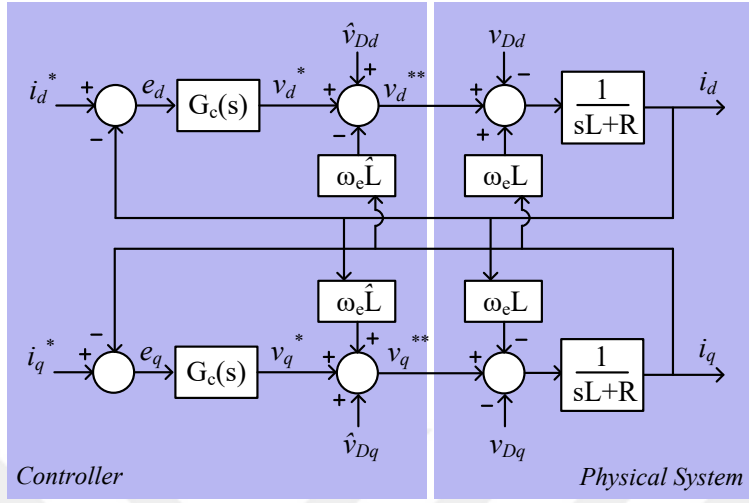


Figure 3.5: 3P3W VSC scalar control system for the frame synchronously rotating with ω_e with the same direction that of grid space vector.

In Figure 3.5, the generic 3P3W VSC control system is illustrated in dq-frame. In the figure, v_{Dd} and \hat{v}_{Dd} denote the projection of disturbance voltage and its estimated value on d-axis (for decoupling purpose) respectively. Similarly, v_{Dq} and \hat{v}_{Dq} denote the projection of disturbance voltage and its estimated value on q-axis respectively. It should be noted that, practically, these disturbance decouplings are performed in the stationary frame and shown in the figure for the sake of consistency. It is also common practice in CCR3 to decouple the cross-coupling terms from the control loop. In the figure, $G_c(s)$ represents the compensator, which is usually a PI controller as the d-axis and q-axis signals are dominantly DC quantities. Assuming the disturbance decoupling (grid voltage, dead-time effect etc.) is performed, and considering Figure 3.5, the 3P3W VSC output voltage command can be obtained as

$$\begin{aligned} V_d^{**}(s) &= [I_d^*(s) - I_d(s)]G_c(s) - \omega \hat{L} I_q(s) \\ V_q^{**}(s) &= [I_q^*(s) - I_q(s)]G_c(s) + \omega \hat{L} I_d(s). \end{aligned} \quad (3.8)$$

When the 3P3W VSC output voltage command is realized by the VSC, the closed-

loop system can be represented as

$$\begin{aligned} [I_d^*(s) - I_d(s)]G_c(s) - \omega\hat{L}I_q(s) &= sLI_d(s) - \omega LI_q(s) \\ [I_q^*(s) - I_q(s)]G_c(s) + \omega\hat{L}I_d(s) &= sLI_q(s) + \omega LI_d(s). \end{aligned} \quad (3.9)$$

When the estimated inductance is equal to the actual inductance ($\hat{L} = L$), the cross-coupling terms are eliminated from the control system and the system becomes fully decoupled as

$$\begin{aligned} [I_d^*(s) - I_d(s)]G_c(s) &= sLI_d(s) \\ [I_q^*(s) - I_q(s)]G_c(s) &= sLI_q(s). \end{aligned} \quad (3.10)$$

Therefore, d-axis (real power component) and q-axis (reactive power component) currents can be controlled independently, which is very similar to the 1P VSC system under DC excitation. These independently controllable d-axis and q-axis systems can be shown as in Figure 3.6. Accordingly, the closed-loop transfer functions of d-axis and q-axis currents can be given by

$$\begin{aligned} \frac{I_d(s)}{I_d^*(s)} &= \frac{G_c(s)}{G_c(s) + sL + R} \\ \frac{I_q(s)}{I_q^*(s)} &= \frac{G_c(s)}{G_c(s) + sL + R}. \end{aligned} \quad (3.11)$$

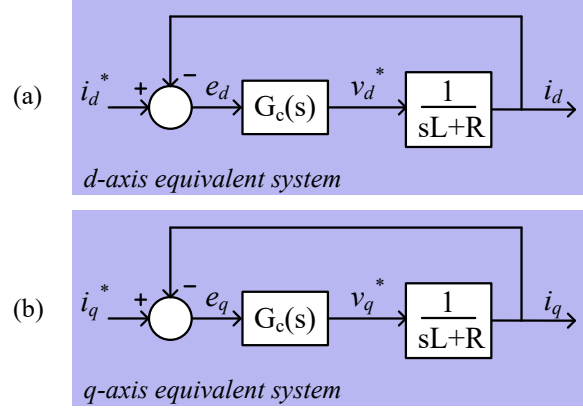


Figure 3.6: 3P3W VSC control system for the frame synchronously rotating with ω_e with the same direction that of grid space vector when the disturbance and cross-coupling decouplings are performed perfectly. (a) d-axis equivalent control system. (b) q-axis equivalent control system.

As the closed-loop control structures that is reached up in (3.11) are the same that of a 1P controlled VSC system, the design rules for $G_c(s)$ are exactly identical to 1P DC current control case for an L-R load. Accordingly, the PI compensator parameters for the realization of $G_c(s)$ can be selected as $K_p = \omega_{BW} \hat{L}$ and $K_i = \omega_{BW} \hat{R}$ as provided in [50].

Another current controller structure for 3P3W VSC systems based on complex vectors is presented in [59], which achieves reducing the cross-coupling effects via feedback rather than decoupling directly. Such an approach is shown to exhibit improved robustness to estimated parameter errors when compared to CCR3. However, when the controller structure is linear as in the case of complex current regulator, the performance degradation is inevitable in the case of inductor saturation occurs.

Recently, for the inductor saturation issues in 3P3W systems, in [60], two-phase modulation is proposed. This study has the disadvantage of lacking the integrator terms in the controller which is a basic requirement for low-frequency controller performance. Besides, the implementation complexity makes the method quite impractical.

In [61], a feed-forwarding approach is adopted to conventional PI type synchronous frame regulators simplifying the approach in [60], and reducing low order harmonics

by 60 %. However, a balanced linear 3P3W system model is utilized in this work which is a quite inaccurate approach.

In spite of the significance of the subject, relevant literature is limited; simple, complete, and effective engineering solutions to the problems due to the utilization of saturable inductors are absent. As a result, conservative designs (involving large inductors with limited saturation and reasonable current control performance) or low-cost designs (highly saturating inductors with poor current control performance) have been employed in the field.

3.2.2 Phase-Locked Loop (PLL)

In order to establish a rotating frame synchronized with the grid voltage, the phase angle θ should be extracted via phase-locked-loop (PLL) which is a state-of-the-art method for detecting the grid phase angle [62]. Even stationary frame controllers accompanied with resonant compensators are used, the grid-voltage angle is essential for precise active/reactive power injection/absorption to/from the utility grid. The implementation of PLL is quite standardized and sufficiently robust both for 1P controlled and 3P3W grid-connected VSC systems. Figure 3.7 summarizes the implementation of the vector PLL. The q-axis component (v_{sq}) of the grid voltage space vector (v_{sabc}) on the estimated dq-coordinate system is subtracted from the reference q-axis component (v_{sq}^*), which is zero when exact alignment of the estimated dq-frame to the desired dq-frame of whose d-axis is aligned with the (v_{sabc}) to obtain the angle error (see Figure 3.8). Such an operation yields quite well results due to the relation

$$v_{sq} = V_m \sin(\theta - \hat{\theta}) \quad (3.12)$$

where V_m is the magnitude of v_{sabc} and for small angles the approximation $\sin(\theta - \hat{\theta}) \approx \theta - \hat{\theta}$ holds thus

$$v_{sq} \approx V_m(\theta - \hat{\theta}). \quad (3.13)$$

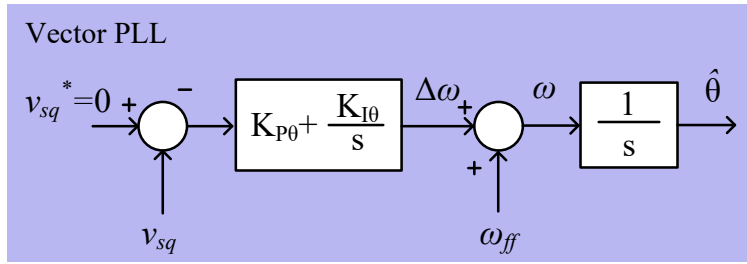


Figure 3.7: Implementation of vector PLL.

Passing through a PI controller the frequency error is obtained and by feed-forwarding the actual grid frequency (ω_{ff}) the corrected frequency is yielded. With the integration of this frequency, the estimated angle of the grid is attained. For single-phase systems, the q-axis voltage can be obtained via the grid-voltage space vector by delaying the single-phase grid voltage by an angle of $\pi/2$ as described in [63]. Further implementation issues on PLL realization and variations are elaborated in [50,63–65].

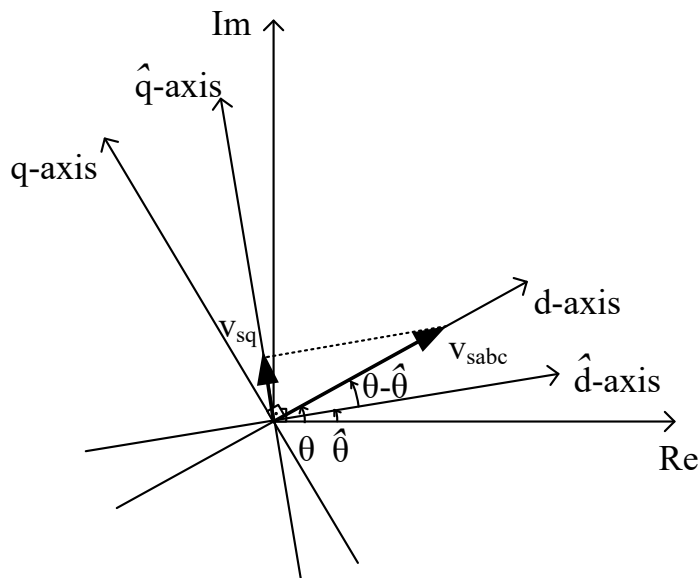


Figure 3.8: Illustration of estimated dq-coordinate system and actual dq-coordinate system to extract the grid voltage phase angle via PLL.

3.3 Problems in Conventional Current Regulation Methods in PWM-VSCs with Saturable Inductors

The VSC systems with linear inductors match suitably with linear current controllers. The modelling of the plant and the design of the controller is a well-known subject yielding satisfactory performance in most applications. However, when the system to be controlled is a nonlinear one, performance degradation is encountered in two fundamental aspects.

The first one of these aspects is the closed-loop system bandwidth. Because of the time-varying characteristics of the plant, the closed-loop frequency response characteristics of the overall control system changes dynamically both in 1P and 3P3W VSCs. Therefore, the bandwidth of the control system changes in time which eventuates in the ineffective utilization of the bandwidth. This issue is called bandwidth shrinkage.

In the second, the current waveform quality degrades with the changing inductance(s) of the system. While the current waveform quality is very critical (especially) in grid-connected VSC systems, conventional linear current regulators in nonlinear plants yield poor current waveform quality. In the following, these two major drawbacks are investigated in depth. Throughout the investigation, these two aspects are considered as a comparison base for the proposed and conventional methods.

3.3.0.1 Bandwidth Shrinkage

For linear minimum phase systems, which involve most of the practical control systems as well as current control systems of power electronics applications, system bandwidth is defined as the frequency range $0 < \omega < \omega_{BW}$ in which the magnitude of the closed-loop does not drop below -3 dB [49]. To visualize, in Figure 3.9 bandwidth of a closed-loop system is illustrated. For an open-loop system, the bandwidth of the system can be determined when the open-loop magnitude is equal to 0 dB which corresponds to -3 dB magnitude of the closed-loop system.

The higher the bandwidth of a closed-loop system corresponds to smaller rise time or

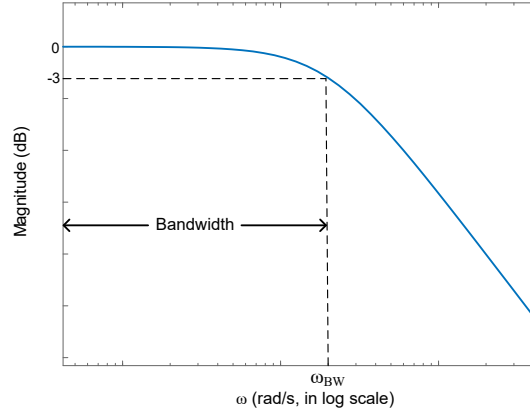


Figure 3.9: Closed-loop system magnitude plot showing the bandwidth of the system.

equivalently faster the response. Furthermore, higher bandwidth increases the waveform quality and provides higher disturbance rejection characteristics. However, the bandwidth of a closed-loop system can not be increased without bound, i.e. to infinity, which corresponds to instantaneous response, due to physical limitations. In power electronics systems, specifically in the current control, the upper bound of the bandwidth is determined by either of carrier frequency, digital controller speed (depends on A/D conversion time, clock frequency, algorithm execution time, and digital controller features such as dedicated hardware increasing the speed of execution etc.), or sensor bandwidth. Accordingly, bandwidth shrinkage issue in 1P controlled and 3P3W VSC systems are elaborated in the following.

Bandwidth Shrinkage in Single-Phase VSC Systems: In saturable inductor applications, depending on the operating current (i_0), the inductance changes. Such a change results in bandwidth shrinkage. This phenomenon can be investigated analytically through the linearization of the nonlinear differential equation (2.9). The nonlinear equation (2.9) can be rewritten as

$$\frac{di}{dt} = f(i, v) = -\frac{R}{L}i + \frac{1}{L}v. \quad (3.14)$$

The small-signal model of (4.18) around the operating point (i_0, v_0) can be represented as

$$\frac{d}{dt}\delta i = A\delta i + B\delta v \quad (3.15)$$

where $\delta i = i - i_0$, $\delta v = v - v_0$. The coefficients A and B can be calculated as in (3.16) and (3.17) respectively.

$$A = \left. \frac{\partial f(i, v)}{\partial i} \right|_{i=i_0, v=v_0} = \frac{-R}{L(i_0)} + \frac{R}{L^2(i_0)} \frac{dL}{di} \Big|_{i=i_0} \quad (3.16)$$

$$B = \left. \frac{\partial f(i, v)}{\partial v} \right|_{i=i_0, v=v_0} = \frac{1}{L(i_0)}. \quad (3.17)$$

The second term on the right-hand side of (3.16) is negligible as compared to the first term. Therefore the linearized model of the plant becomes as

$$\frac{d}{dt} \delta i = -\frac{R}{L(i_0)} \delta i + \frac{1}{L(i_0)} \delta v \quad (3.18)$$

where $\delta i = i - i_0$, $\delta v = v - v_0$. Equipped with a linear compensator G_c , the linearized system have a CLTF as

$$\frac{I(s)}{I^*(s)} = \frac{G_c(s)}{G_c(s) + sL(i_0) + R}. \quad (3.19)$$

The operating point current dependent form of (3.19) reveals that the current regulation performance of the system changes with i_0 ; so does the bandwidth of the system.

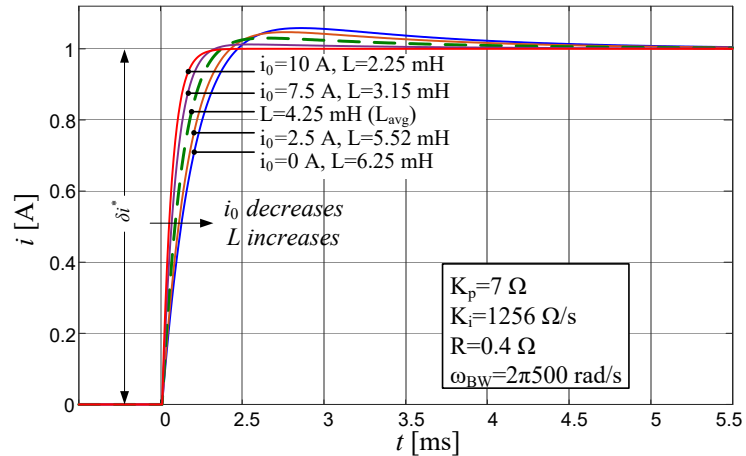


Figure 3.10: Closed-loop current control step response of a saturable inductor to a step current command for various DC-bias currents.

Figure 3.10 shows the results of a closed-loop current-controlled full-bridge converter operating as DC-DC converter and tested for step response by a simulation study. It is showing the current regulation performance at distinct DC operating currents of the saturable inductor with L-i characteristics of Figure 2.7. The compensator is a PI type with $K_p = 7 \Omega$, $K_i = 1256 \Omega/s$ (giving maximum bandwidth of $2\pi 500$ rad/s at $L_{min} = 2.25$ mH). As the system bandwidth decreases at low operating current levels (hence at higher inductance levels), the current tracking performance substantially degrades and rise time of the response considerably increases.

In AC applications, the output current of the VSC varies at the fundamental frequency. Therefore, the bandwidth of the system varies periodically. When the VSC current magnitude is at its maximum rating, the inductance is at its minimum value and the bandwidth of the closed-loop system is at its maximum (ω_{BW-max}). Hence, in order for ω_{BW-max} not to exceed bandwidth upper limit (ω_{BW-UL}) constraint imposed by either of the carrier frequency or the digital controller capabilities (limitation due to A/D conversion time, algorithm execution time etc.), the minimum value of the inductance (L_{min}) should be used when setting the regulator proportional gain (*i.e.* $K_p = \omega_{BW} \times L_{min}$). In accordance, bandwidth of CCR (ω_{BW}^{CCR}) can be approximated as in (3.20), noting that L is the instantaneous incremental inductance

$$\omega_{BW}^{CCR} \approx \frac{\omega_{BW} \times L_{min}}{L}. \quad (3.20)$$

Consistently, the inductance increases to its maximum (L_{max}) and the bandwidth shrinks down to its minimum (ω_{BW-min}) when the current magnitude is zero [55,57]. Figure 3.11 visualizes the bandwidth shrinkage phenomenon in 1P CCR systems employing saturable inductors. As the bandwidth is inversely proportional to the inductance value, the variation is dominantly at the second harmonic of the fundamental frequency. As a result of the bandwidth shrinkage, the current regulation performance of the VSC degrades for constant gain CCRs. When the bandwidth exceeds the (ω_{BW-UL}), the current quality significantly deteriorates.

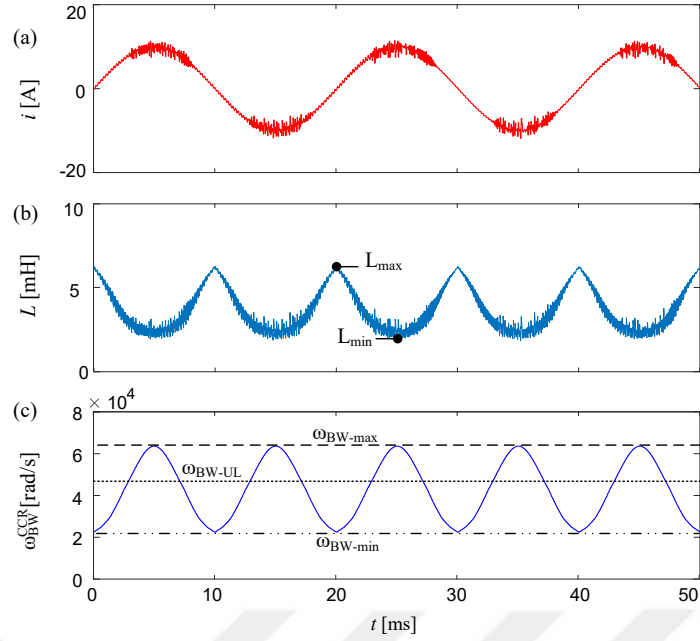


Figure 3.11: Effect of exceeding upper limit of the bandwidth. (a) Inductor current. (b) Inductance variation. (c) Variation of the calculated instantaneous bandwidth with time.

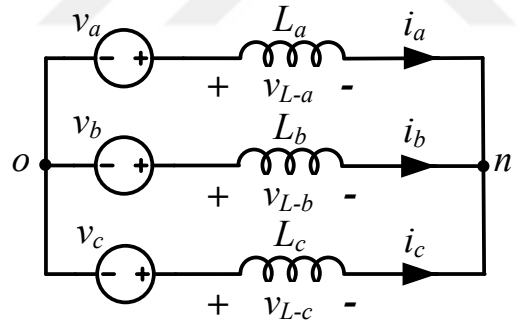


Figure 3.12: Three-phase three-wire current control system model with only inductances and control voltage sources involved for bandwidth shrinkage analysis.

Bandwidth Shrinkage in Three-Phase Three-Wire VSC Systems: In Figure 3.12, the equivalent model of a 3P3W VSC system is illustrated with the basic building blocks, pole control voltage sources and the inductances. The resistances are neglected in order to ease the bandwidth shrinkage analysis. The mathematical model of the system can be obtained as in (3.21) by making use of three mesh equations. It

should be noted the representation is valid whether the inductors are linear or nonlinear and distinct from the conventional representation. However, when the system is balanced these representations become identical. It should be also noted that the rows of (3.21) are linearly dependent.

$$\mathbf{V} = \mathbf{L} \frac{d}{dt} \mathbf{I} \quad (3.21)$$

where $\mathbf{V} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$, $\mathbf{L} = \frac{1}{3} \begin{bmatrix} 2L_a & -L_b & -L_c \\ -L_a & 2L_b & -L_c \\ -L_a & -L_b & 2L_c \end{bmatrix}$, and $\mathbf{I} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$.

The system represented by (3.21) can be transformed to space vector quantities as

$$v_{abc} = \frac{2}{3}(v_a + av_b + a^2v_c) \quad (3.22)$$

where $a = e^{j\frac{2\pi}{3}}$. Inserting (3.21) into (3.22), one can obtain the system equation in terms of currents and the instantaneous inductances as

$$V_{abc} = \frac{2}{3}(L_a \frac{di_a}{dt} + aL_b \frac{di_b}{dt} + a^2L_c \frac{di_c}{dt}). \quad (3.23)$$

In a synchronous reference frame rotating with $\theta = \omega_e t$, the control voltage can be obtained in terms of stationary frame voltage as

$$V_{dq} = V_{abc} e^{-j\theta}. \quad (3.24)$$

Noting that $i_a = \text{Re}\{i_{dq} e^{j\theta}\}$, $i_b = \text{Re}\{i_{dq} a^2 e^{j\theta}\}$, and $i_c = \text{Re}\{i_{dq} a e^{j\theta}\}$ one can represent the 3P3W system in dq frame as

$$V_{dq} = \frac{2}{3} e^{-j\theta} \left[L_a \frac{d}{dt} \text{Re}\{i_{dq} e^{j\theta}\} + aL_b \frac{d}{dt} \text{Re}\{i_{dq} a^2 e^{j\theta}\} + a^2L_c \frac{d}{dt} \text{Re}\{i_{dq} a e^{j\theta}\} \right]. \quad (3.25)$$

Equation (3.25) is equivalent to

$$\begin{aligned}
V_{dq} &= \frac{2}{3}e^{-j\theta} \left[L_a \operatorname{Re} \left\{ \frac{di_{dq}}{dt} e^{j\theta} + j\omega i_{dq} e^{j\theta} \right\} \right. \\
&\quad + aL_b \operatorname{Re} \left\{ \frac{di_{dq}}{dt} a^2 e^{j\theta} + j\omega i_{dq} a^2 e^{j\theta} \right\} \\
&\quad \left. + a^2 L_c \operatorname{Re} \left\{ \frac{di_{dq}}{dt} a e^{j\theta} + j\omega i_{dq} a e^{j\theta} \right\} \right].
\end{aligned} \tag{3.26}$$

The equation (3.26) can be decomposed into its real and imaginary components as

$$\begin{aligned}
V_d &= \operatorname{Re}\{V_{dq}\} \\
&= \frac{2}{3} \left[\cos(\theta)L_a \left\{ \cos(\theta) \frac{di_d}{dt} - \sin(\theta) \frac{di_q}{dt} - \omega i_d \sin(\theta) - \omega i_q \cos(\theta) \right\} \right. \\
&\quad + \cos(\theta - 2\pi/3)L_b \left\{ \cos(\theta - 2\pi/3) \frac{di_d}{dt} - \sin(\theta - 2\pi/3) \frac{di_q}{dt} \right. \\
&\quad \left. - \omega i_d \sin(\theta - 2\pi/3) - \omega i_q \cos(\theta - 2\pi/3) \right\} \\
&\quad + \cos(\theta + 2\pi/3)L_c \left\{ \cos(\theta + 2\pi/3) \frac{di_d}{dt} - \sin(\theta + 2\pi/3) \frac{di_q}{dt} \right. \\
&\quad \left. - \omega i_d \sin(\theta + 2\pi/3) - \omega i_q \cos(\theta + 2\pi/3) \right\} \left. \right]
\end{aligned} \tag{3.27}$$

and

$$\begin{aligned}
V_q &= \operatorname{Im}\{V_{dq}\} \\
&= \frac{2}{3} \left[-\sin(\theta)L_a \left\{ \cos(\theta) \frac{di_d}{dt} - \sin(\theta) \frac{di_q}{dt} - \omega i_d \sin(\theta) - \omega i_q \cos(\theta) \right\} \right. \\
&\quad - \sin(\theta - 2\pi/3)L_b \left\{ \cos(\theta - 2\pi/3) \frac{di_d}{dt} - \sin(\theta - 2\pi/3) \frac{di_q}{dt} \right. \\
&\quad \left. - \omega i_d \sin(\theta - 2\pi/3) - \omega i_q \cos(\theta - 2\pi/3) \right\} \\
&\quad - \sin(\theta + 2\pi/3)L_c \left\{ \cos(\theta + 2\pi/3) \frac{di_d}{dt} - \sin(\theta + 2\pi/3) \frac{di_q}{dt} \right. \\
&\quad \left. - \omega i_d \sin(\theta + 2\pi/3) - \omega i_q \cos(\theta + 2\pi/3) \right\} \left. \right].
\end{aligned} \tag{3.28}$$

This decomposition can be represented in matrix form as

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \mathbf{F}^T(\theta) \mathbf{L}_t \mathbf{F}(\theta) \begin{bmatrix} \frac{di_d}{dt} - \omega i_q \\ \frac{di_q}{dt} + \omega i_d \end{bmatrix} \tag{3.29}$$

where

$$\mathbf{L}_t = \frac{2}{3} \begin{bmatrix} L_a & 0 & 0 \\ 0 & L_b & 0 \\ 0 & 0 & L_c \end{bmatrix}, \text{ and } \mathbf{F}(\theta) = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \cos(\theta - 2\pi/3) & -\sin(\theta - 2\pi/3) \\ \cos(\theta + 2\pi/3) & -\sin(\theta + 2\pi/3) \end{bmatrix}.$$

The system of (3.29) can be represented in s-domain as

$$\begin{bmatrix} V_d(s) \\ V_q(s) \end{bmatrix} = \mathbf{F}^T(\theta) \mathbf{L}_t \mathbf{F}(\theta) \begin{bmatrix} s & -\omega \\ \omega & s \end{bmatrix} \begin{bmatrix} I_d(s) \\ I_q(s) \end{bmatrix}. \quad (3.30)$$

It should be noted that equation (3.30) is generalized form of transforming 3P3W inductance system to dq-frame and when $L_a = L_b = L_c = L$, the transformation becomes the conventional dq-frame linear system representation yielding $V_d = L \frac{di_d}{dt} - \omega Li_q$ and $V_q = L \frac{di_q}{dt} + \omega Li_d$.

Utilizing these outcomes, the current regulation system (3.29) can be represented in s-domain as

$$\left[K_p + \frac{K_i}{s} \right] \begin{bmatrix} I_d^*(s) - I_d(s) \\ I_q^*(s) - I_q(s) \end{bmatrix} = \mathbf{F}^T(\theta) \mathbf{L}_t \mathbf{F}(\theta) \begin{bmatrix} s & -\omega \\ \omega & s \end{bmatrix} \begin{bmatrix} I_d(s) \\ I_q(s) \end{bmatrix}. \quad (3.31)$$

This system can be represented as

$$\left[K_p + \frac{K_i}{s} \right] \begin{bmatrix} I_d^*(s) - I_d(s) \\ I_q^*(s) - I_q(s) \end{bmatrix} = \mathbf{G}_p(s) \begin{bmatrix} I_d(s) \\ I_q(s) \end{bmatrix}. \quad (3.32)$$

$$\text{where } \mathbf{G}_p(s) = \mathbf{F}^T(\theta) \mathbf{L}_t \mathbf{F}(\theta) \begin{bmatrix} s & -\omega \\ \omega & s \end{bmatrix} = \begin{bmatrix} G_{p-11}(s) & G_{p-12}(s) \\ G_{p-21}(s) & G_{p-22}(s) \end{bmatrix}.$$

The system in (3.31) can be rewritten in a standardized manner as

$$\begin{bmatrix} I_d^*(s) \\ I_q^*(s) \end{bmatrix} = \mathbf{G}(s) \begin{bmatrix} I_d(s) \\ I_q(s) \end{bmatrix} \quad (3.33)$$

$$\text{where } \mathbf{G}(s) = \begin{bmatrix} G_{11}(s) & G_{12}(s) \\ G_{21}(s) & G_{22}(s) \end{bmatrix} = \begin{bmatrix} \frac{G_{p-11}(s)}{K_p + K_i/s} + 1 & \frac{G_{p-12}(s)}{K_p + K_i/s} \\ \frac{G_{p-21}(s)}{K_p + K_i/s} & \frac{G_{p-22}(s)}{K_p + K_i/s} + 1 \end{bmatrix}, \text{ or alternatively}$$

the system can be represented as

$$\begin{bmatrix} I_d(s) \\ I_q(s) \end{bmatrix} = \mathbf{H}(s) \begin{bmatrix} I_d^*(s) \\ I_q^*(s) \end{bmatrix} \quad (3.34)$$

wherein $\mathbf{H}(s) = \mathbf{G}(s)^{-1}$.

The transfer function matrix $\mathbf{H}(s)$ is in the form of

$$\mathbf{H}(s) = \begin{bmatrix} H_{11}(s) & H_{12}(s) \\ H_{21}(s) & H_{22}(s) \end{bmatrix} \quad (3.35)$$

where $H_{11}(s) = \frac{G_{22}(s)[K_p+K_i/s]}{G_{11}(s)G_{22}(s)-G_{12}(s)G_{21}(s)}$, $H_{12}(s) = \frac{-G_{12}(s)[K_p+K_i/s]}{G_{11}(s)G_{22}(s)-G_{12}(s)G_{21}(s)}$, $H_{21}(s) = \frac{-G_{21}(s)[K_p+K_i/s]}{G_{11}(s)G_{22}(s)-G_{12}(s)G_{21}(s)}$, and $H_{22}(s) = \frac{G_{11}(s)[K_p+K_i/s]}{G_{11}(s)G_{22}(s)-G_{12}(s)G_{21}(s)}$.

Each of the entries of $\mathbf{H}(s)$ forms a single-input single-output subsystem having specific bandwidths. These bandwidths can be represented by

$$\omega_{\mathbf{BW}} = \begin{bmatrix} \omega_{BW-dd}^{CCR3} & \omega_{BW-dq}^{CCR3} \\ \omega_{BW-qd}^{CCR3} & \omega_{BW-qq}^{CCR3} \end{bmatrix}. \quad (3.36)$$

The upper limit for the control bandwidth (ω_{BW-UL}) sets an upper bound for each of the elements of $\omega_{\mathbf{BW}}$. The cross-coupling bandwidths (ω_{BW-dq}^{CCR3} and ω_{BW-qd}^{CCR3}) are relatively small when compared to d-axis and q-axis self bandwidths (ω_{BW-dd}^{CCR3} and ω_{BW-qq}^{CCR3}). Therefore, the cross-coupling bandwidths do not violate the ω_{BW-UL} constraint. Consequently, the self bandwidths can be used to detect violation of ω_{BW-UL} constraint. In Figure 3.13 the spatial variation of the d-axis and q-axis bandwidths are illustrated for three reference current sets at phase angles of $\theta_0 = 0$, $\theta_0 = \pi/4$, and $\theta_0 = \pi/2$ with respect to the d-axis (or grid voltage space vector). The three-phase inductors having the characteristics given in chapter 2 (see Figure 2.11) are utilized while obtaining the bandwidth characteristics. From the figure, it can be observed that the bandwidths of the d-axis and q-axis currents are both time and displacement angle-dependent as well as the current magnitude.

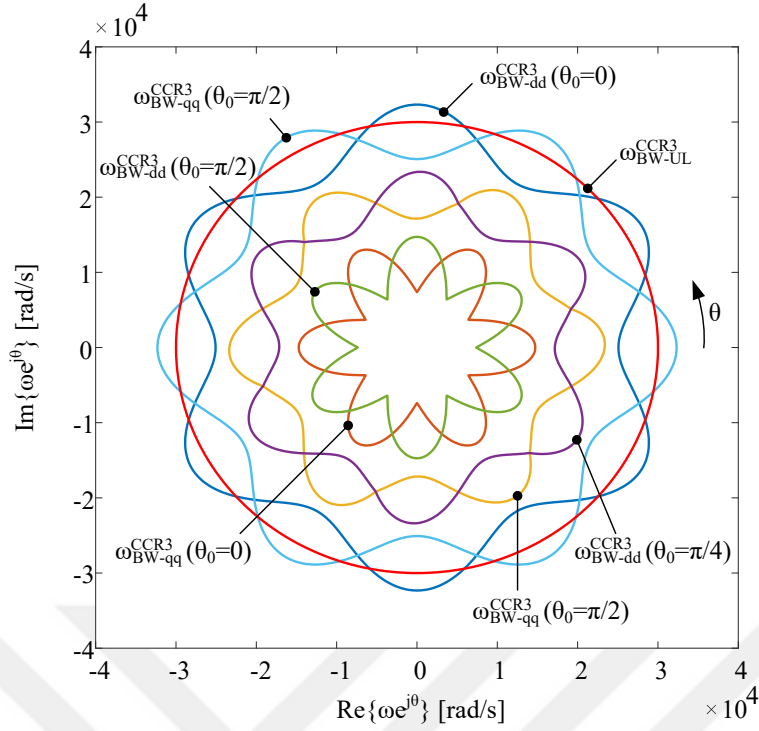


Figure 3.13: Spatial variation of the d-axis and q-axis bandwidths.

The characteristics obtained in the above analyses are demonstrated by closed-loop simulations.

First, K_p is kept small such that the system ω_{BW-UL}^{CCR3} limit is not exceeded (to provide a bandwidth of $2\pi 500$ rad/s when a constant inductance is assumed with an inductance of $450 \mu H$). In Figure 3.14, the current regulation characteristics for this case, when the ω_{BW-UL}^{CCR3} limit is not exceeded. Normally, the current waveforms involve low-frequency harmonics due to inductance variation. However, high-frequency harmonics are non-existent in the current waveforms as the bandwidth limit is not exceeded.

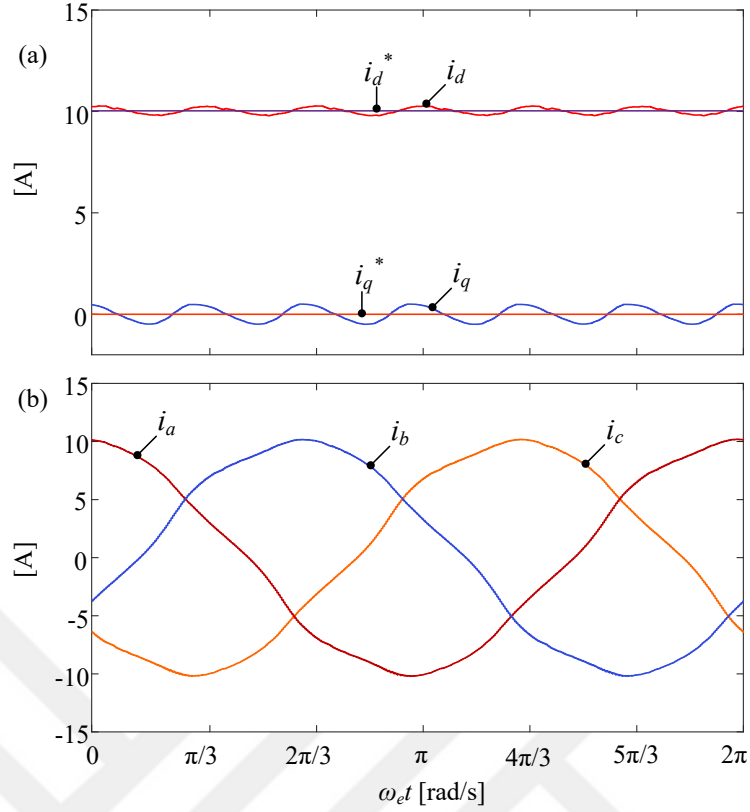


Figure 3.14: Spatial variation of the d-axis and q-axis currents when the bandwidth upper limit is not exceeded. (a) dq-frame currents and current commands. (b) Phase currents.

In Figure 3.15, the simulation waveforms for the case that K_p gain in the stationary frame is increased until the system bandwidth starts to exceed the ω_{BW-UL}^{CCR3} value (corresponds to $K_p = 32 \Omega$). The d-axis current reference is set to 10 A and q-axis current is to zero. In accordance with the bandwidth shrinkage analyses and the resultant bandwidth waveform shown in Figure 3.13, the control problems arise when the d-axis self bandwidth exceeds ω_{BW-UL}^{CCR3} which corresponds to the angle regions near $\frac{\pi}{6} + k\frac{\pi}{3}$ for k is an integer. In Figure 3.16, the dq-frame currents and phase-b current are shown in a zoomed manner. Although the ripple on these waveforms resembles the PWM current ripple, these current ripples are caused by the controller as the bandwidth limit is exceeded. When this limit is exceeded, the controller tries to respond to high-frequency errors that the modulator can not synthesize due to carrier frequency insufficiency. As a result, the output voltage becomes erroneous. Thus,

high-frequency oscillatory currents are encountered.

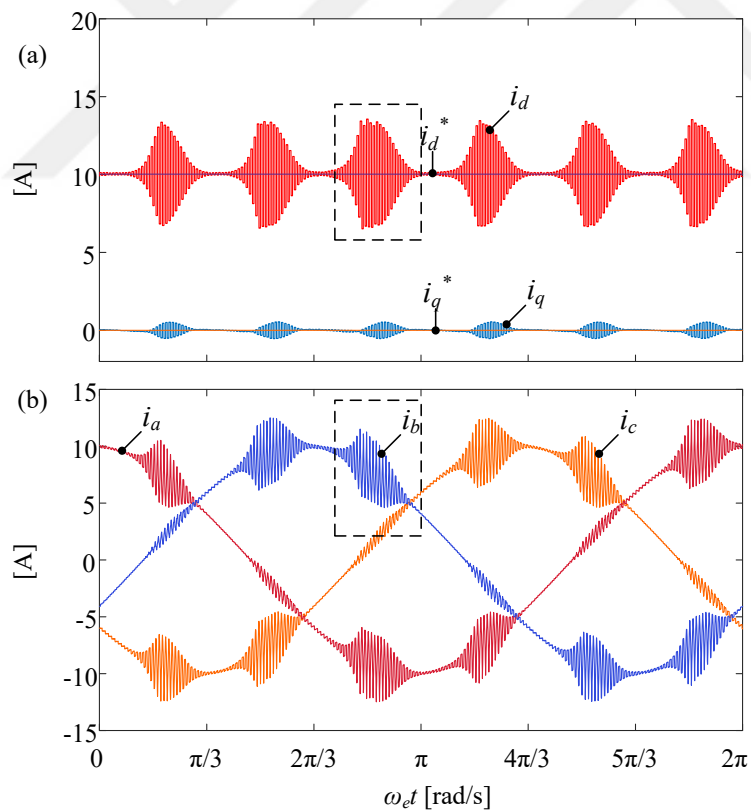


Figure 3.15: Spatial variation of the currents when the bandwidth upper limit is exceeded. (a) dq-frame currents and current commands. (b) Phase currents.

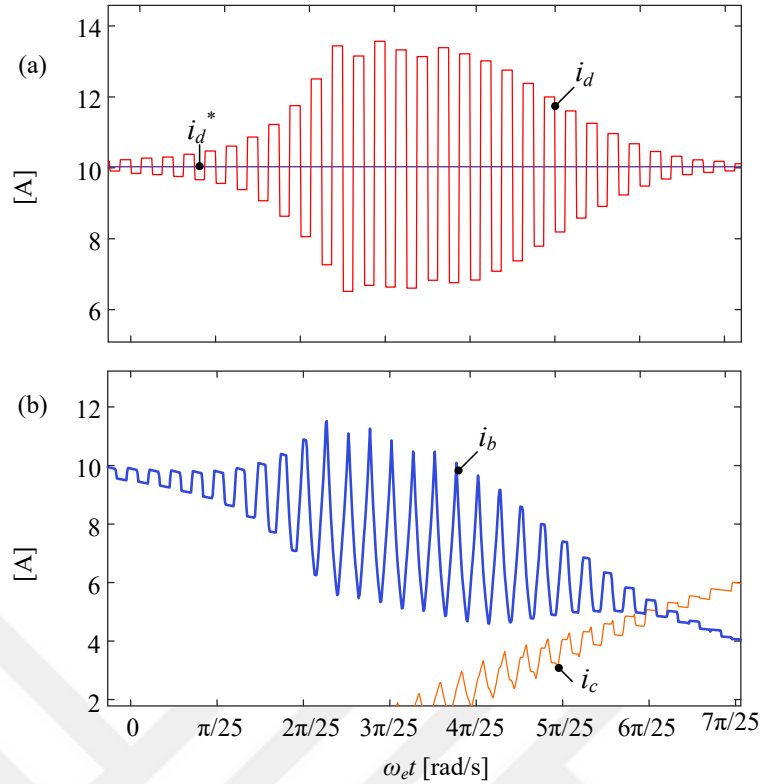


Figure 3.16: Spatial variation of the currents zoomed when the bandwidth upper limit is exceeded. (a) d-axis current and current command. (b) Phase-b current.

3.3.0.2 Waveform Quality

The second eminent problem regarding AC systems with saturable inductors is the generation of low order current harmonics [57], [61]. Inductor current in such systems involves harmonic components in addition to fundamental component even with pure AC voltage excitation at the fundamental frequency. In Figure 3.17, simulation results of such practical L-R circuit (with the inductor being nonlinear, its L-i characteristics as given in Figure 2.10, and with $R = 0.5 \Omega$) under pure sinusoidal voltage excitation are illustrated. From the time-domain waveforms in the figure, it can be observed that the inductance decreases as the current magnitude increases. Accordingly, the current waveform exhibits substantial peaking when the inductance is at its minimum level. Hence the current harmonic spectrum involves prohibitive low order odd harmonics (especially 3^{rd} harmonic). It is remarkable that the magnitude (and ratio to the fundamental) of those low order harmonics are highly dependent on the

excitation voltage and inductance saturation characteristics.

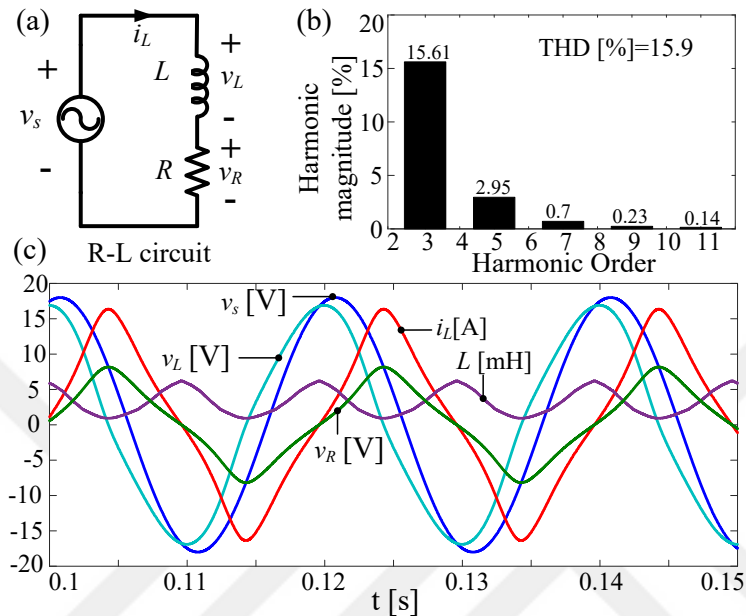


Figure 3.17: Simulation results of 1P AC excitation of saturable inductor. (a) Simulated circuit. (b) Inductor current harmonic spectrum. (c) Simulation waveforms of the simulated variables.

Figure 3.18 shows the experimental current waveform of a 1P conventionally controlled VSC operating in grid-connected mode. Apparently, the current waveform quality is inadmissible as the current THD is 7.32 %. Moreover, the current harmonics are quite above harmonic standards. The most dominant harmonic in the current spectrum is the 3rd harmonic. While a slight amount of these harmonics are caused by disturbances such as grid voltage, the principal source of these harmonics is the controller insufficiency.

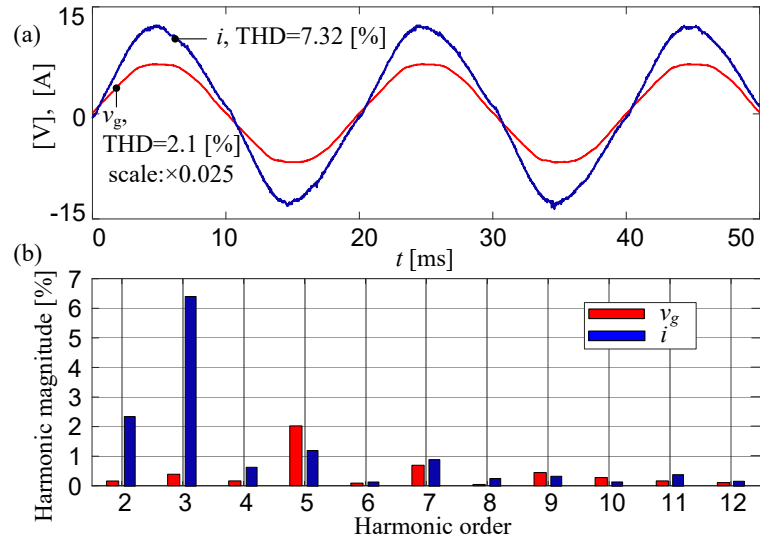


Figure 3.18: Experimental waveforms of a grid-connected VSC system with saturable inductor for conventional current regulation. (a) Voltage and current waveforms. (b) Associated harmonic spectra.

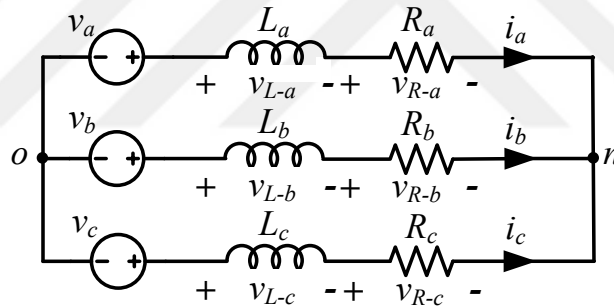


Figure 3.19: Simulated three-phase three-wire R-L-E circuit.

Similar to 1P VSC systems, 3P3W VSC systems suffer from waveform quality problems when saturable inductors are employed. To emphasize the problem, the circuit in Figure 3.19 is simulated. The nonlinear inductors utilized in the simulation have the characteristics given in Figure 2.11. The resistance of the system is 0.5Ω per phase. The system voltage inputs are three balanced sinusoids at 10 V peak value at 50 Hz (see Figure 3.20(a)). In Figure 3.20 associated simulation waveforms are illustrated. Even pure sinusoids are applied to the R-L load, current waveforms involve high harmonic content (THD=8.69 %). As there is no path for zero-sequence

current to flow the voltage and current waveforms significantly deviate from that of 1P controlled. In Figure 3.21, associated current harmonic spectrum is shown for phase-a. When compared to 1P VSC system current harmonics (see Figure 3.17), distinctive attributes can be observed. As the zero-sequence path is absent in 3P3W VSC systems, the zero-sequence harmonics do not flow. Thus only 5th, 7th, and 11th harmonics are existent in the low-frequency region and 3rd and its multiple order harmonics are absent.



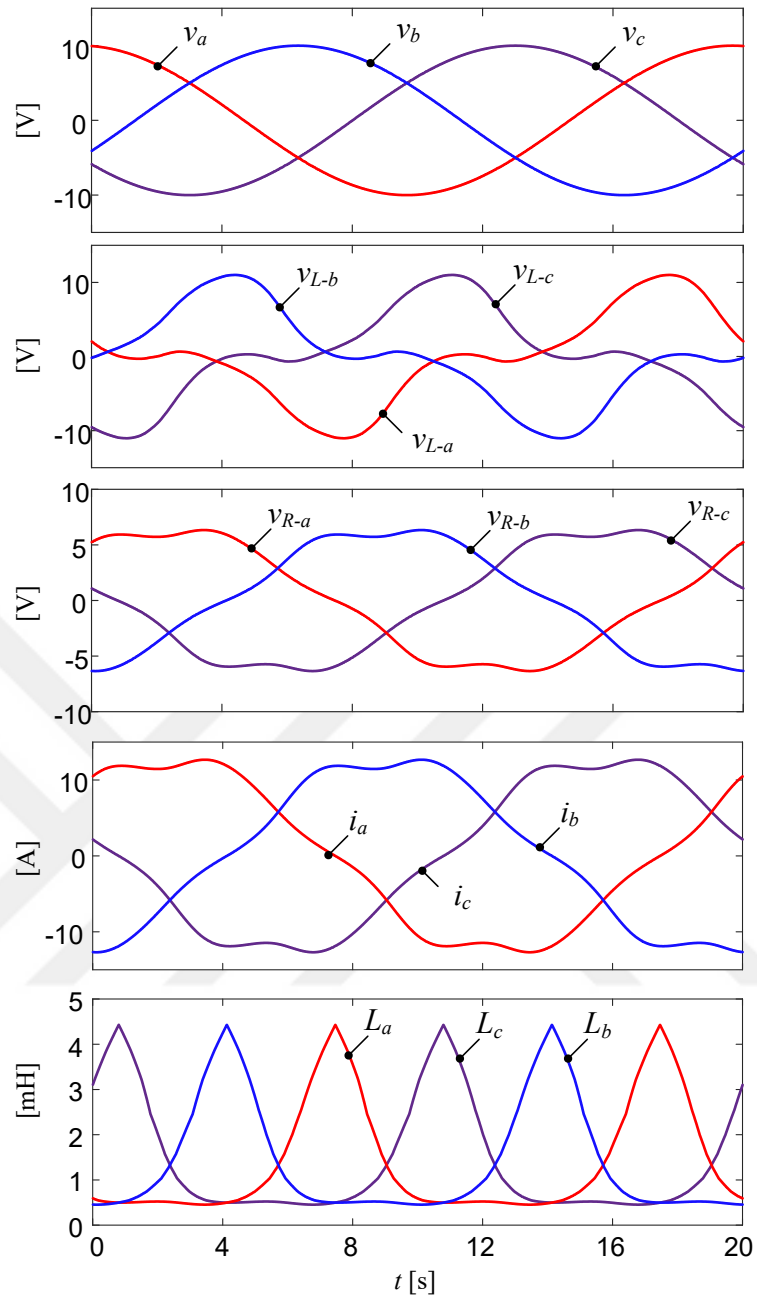


Figure 3.20: Simulation waveforms of AC excitation of 3P3W system with saturable inductors.

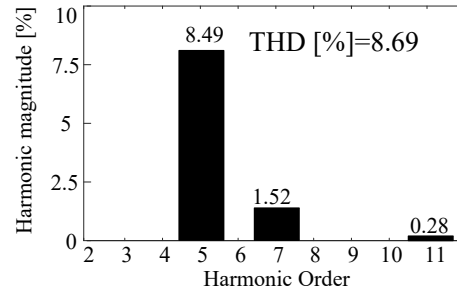


Figure 3.21: Inductor current harmonic spectrum of three-phase three-wire simulated open-loop circuit.

Both for 1P controlled and 3P3W VSC systems, increasing the current control bandwidth may reduce low order harmonics. However, the improvement in this approach is limited as the range of the gains are bounded due to bandwidth upper limit constraint. Furthermore, with such an approach, bandwidth shrinkage issue is still unsolved and limits the usage of available current tracking ability of the converter. Updating K_p in proportion to inductance change (K_p gain scheduling) also does not solve the bandwidth shrinkage and low order harmonics satisfactorily as the resistive voltage drop is in the order of the inductive voltage drop. Furthermore, as the other compensator constituents, especially the resonant term, are not updated, these constituents yield erroneous output for the time-varying plant dynamics.

3.4 Summary

The conventional current control methods for 1P controlled and 3P3W VSC systems are studied in this chapter. The basic controller structures which have become industry standard are summarized. Alternative approaches for VSC systems employing saturable inductors are reviewed. It is shown that the conventional linear controller structures suffer from bandwidth shrinkage and waveform quality problems. These problems are elaborated by means of analyses, simulations, and experiments. After the clarification of the problems in conventionally controlled VSC systems, the next two chapters are dedicated to solve these problems.

CHAPTER 4

INDUCTOR SATURATION COMPENSATION IN SINGLE-PHASE CONTROLLED VOLTAGE SOURCE CONVERTERS

4.1 Introduction

It is shown that the conventional control system in single-phase controlled and three-phase three-wire voltage-source converter systems (shown in Figure 3.3 and 3.5 respectively) exhibit weaknesses of bandwidth shrinkage and low order harmonics when the filter inductor is nonlinear in the previous chapter. To overcome these weaknesses, the inverse dynamic model (IDM) based compensation (IDMBC) method and the saturation compensation with resistive decoupling (SCRD) method is developed in this chapter for single-phase controlled systems. The frequency response and disturbance rejection characteristics of the methods are elaborated in comparison with conventional current regulation and K_p scheduling methods. As these methods require VSC system L-R parameters, associated identification methods are presented afterward. The performance improvement with the proposed methods is shown in comparison with the CCR and K_p scheduling methods by means of simulations firstly. Via simulations, it is also shown that the IDMBC and SCRD methods are parameter mismatch proof, i.e. the performance change is negligible under estimated parameter mismatch. The dynamic response and waveform quality performance improvement with the employment of the IDMBC and SCRD methods are shown via laboratory experiments also. Finally, a conclusive decision among the proposed two methods is reached.

4.2 An Inverse Dynamic Model Based Compensation Method for Inductor Saturation in Single-Phase VSC systems

The method includes two stages; first, the nonlinear plant is compensated in a manner to act as a unity gain system; second, an integral term is incorporated to obtain a fictitious overall equivalent plant consisting of a linear inductor with an inductance of L_{min} .

4.2.1 Inverse Dynamic Model (IDM)

With the load voltage disturbance decoupling performed, the remaining L-R circuit model with saturable inductor described in is nonlinear. IDM is developed to convert this nonlinear system to a linear system with unity-gain and zero-phase. Based on the nonlinear physical system and its IDM can be represented in time-domain as shown in Figure 4.1. Since the system is nonlinear, in this representation, the order of operators is important (unlike the linear systems). With the nonlinear time-domain structure one can write the equivalence of nonlinear state equations as

$$L \frac{di}{dt} + Ri = \hat{L} \frac{du}{dt} + \hat{R}u \quad (4.1)$$

where \hat{L} and \hat{R} are estimated inductance and resistance of the load respectively. When these estimated terms are equal to the actual parameters and the initial states are identical ($i(0) = u(0)$), the equivalence $i(t) = u(t)$ is obtained for $t > 0$. Therefore, the resulting system from the cascade of these two nonlinear systems can be considered as a linear, unity-gain, zero-phase system.

4.2.2 Incorporation of Integral Compensator

The IDM in Figure 4.1 includes derivative operator which can be restrictive due to noise amplification in the control of power electronics. Furthermore, the unity-gain zero-phase equivalent system will have very high bandwidth when linear controllers in the form of (3.2) are employed. This high bandwidth would unnecessarily cre-

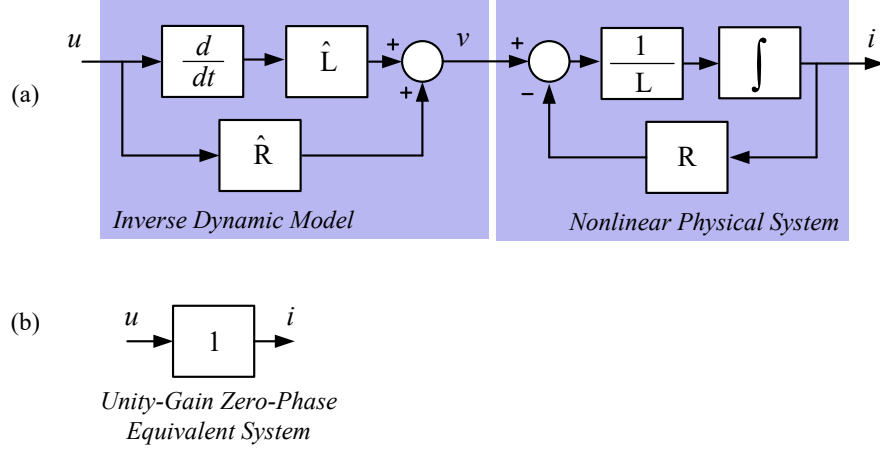


Figure 4.1: Time-domain representation of nonlinear L-R physical system and its IDM. (a) The cascade of IDM and nonlinear physical systems. (b) The equivalent system.

ate significant duty cycle variation stressing the LC filter. Therefore, an integration term with a coefficient of $1/L_{min}$ is incorporated into IDM as shown in Figure 4.2(a). When the integration operator is transferred to IDM side, the simplified time-domain model becomes as in Figure 4.2(b). With such an arrangement, the derivative operator is cancelled by the integration operator, hence possible noise problems are eliminated. With the integration coefficient ($1/L_{min}$), the simplified equivalent model of the system becomes that of a linear inductor with an inductance L_{min} (Figure 4.2(c)).

With these arrangements, the overall closed-loop control scheme becomes as shown in Figure 4.3(a). In the scheme, G_c gives the output signal r ; and when this signal is passed through the nonlinear unified integral IDM block, the command voltage v^* is obtained that will yield approximately desired current in the output of the nonlinear physical system when load voltage decoupling is performed. With the simplification in Figure 4.2, the current error compensator G_c sees a linear system with a constant inductance ($1/sL_{min}$) as shown in Figure 4.3(b). Hence, the CLTF of the system becomes as

$$\frac{I(s)}{I^*(s)} = \frac{G_c(s)}{G_c(s) + sL_{min}}. \quad (4.2)$$

With such simplification, considering the discussion in chapter 3, one can employ

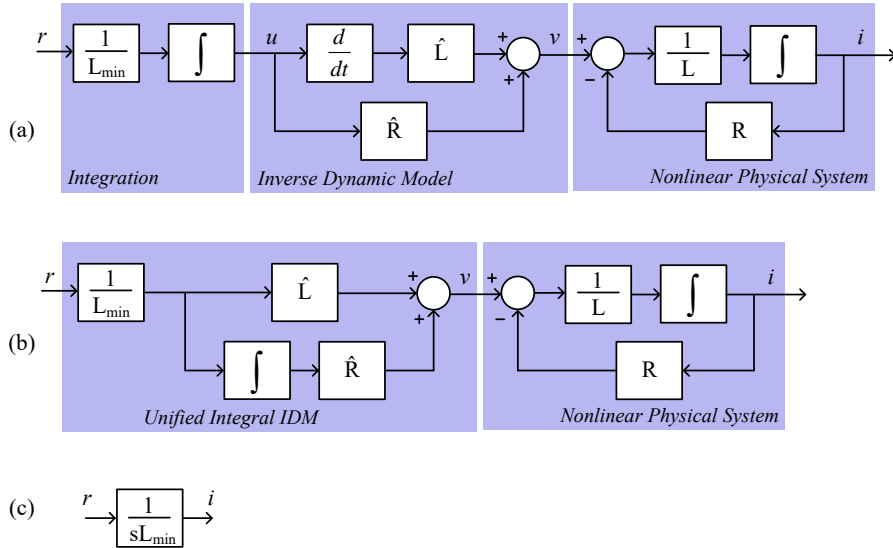


Figure 4.2: Incorporation of integration term (with a coefficient of $1/L_{min}$). (a) The cascade of integration block, IDM, and nonlinear physical systems. (b) The equivalent model when integration is reflected to IDM. (c) Simplified equivalent model.

linear controllers and precisely determine the bandwidth of the overall linear system. The IMDBC method has been developed intuitively with the thought of cancelling the system nonlinearity. However, after the success of the study, the literature search has yielded publications on robotic system trajectory tracking that have similar approaches with feedforwarding the nonlinear system dynamics [66–69]. On the other hand, the proposed method in this paper uses a complete inverse system based on full state feedback which is advantageous in terms of parameter identification errors. To the knowledge of the author, neither this method nor the approaches in [66–69] have been used in power electronics and specifically in the current control of power converters. Note that the approach of nonlinearity cancellation by using the inverse of periodic models (under the name of describing function) is different from what is proposed, which is dynamical and provides high bandwidth [66].

The K_p scheduling method, which provides improved overall performance over CCR, is also benefiting from the inverse gain function by updating the gain in proportion to the inverse of the varying inductance. However, IDMBC does not only involve inverse gain function, but it also manipulates the nonlinear plant and obtains a fictitious linear plant which can be properly controlled by linear compensators such that the

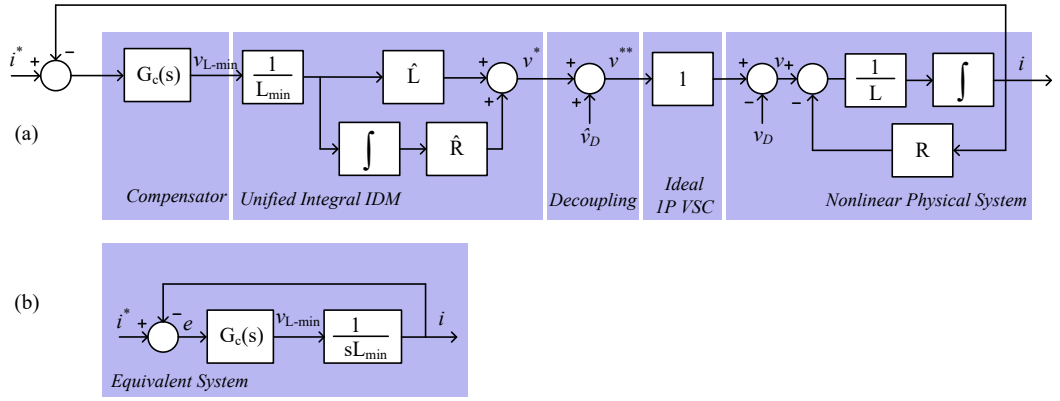


Figure 4.3: The closed-loop implementation of IDMBBC method for 1P VSC system. (a) Overall current regulator architecture. (b) Simplified equivalent representation of the system.

performance is improved. Furthermore, the K_p scheduling method does not affect the output of the resonant controller, thus the performance improvement that of IDMBBC method is not expected in the K_p scheduling method.

4.2.3 Incorporation of Active Damping

Having an equivalent linear current regulation system with a fictitious inductance of L_{min} and based on the system requirements such as dynamic performance and resonance suppression, active damping can be performed via a fictitious damping resistor (R_d) which has been widely utilized in the linear control of power electronics current regulation systems [50]. In Figure 4.4 (a), the control architecture employing active damping is illustrated. This actively damped system reduces to a closed-loop controlled L-R plant as shown in Figure 4.4 (b) with the simplification described in the previous paragraphs. When active damping is performed, the coefficient of the integral compensator should be set as $K_i = \omega_{BW} \times R_d$ for linearized system pole-zero cancellation. In accordance, the CLTF of the system with correctly estimated parameters can be obtained as

$$\frac{I(s)}{I^*(s)} = \frac{G_c(s)}{G_c(s) + sL_{min} + R_d}. \quad (4.3)$$

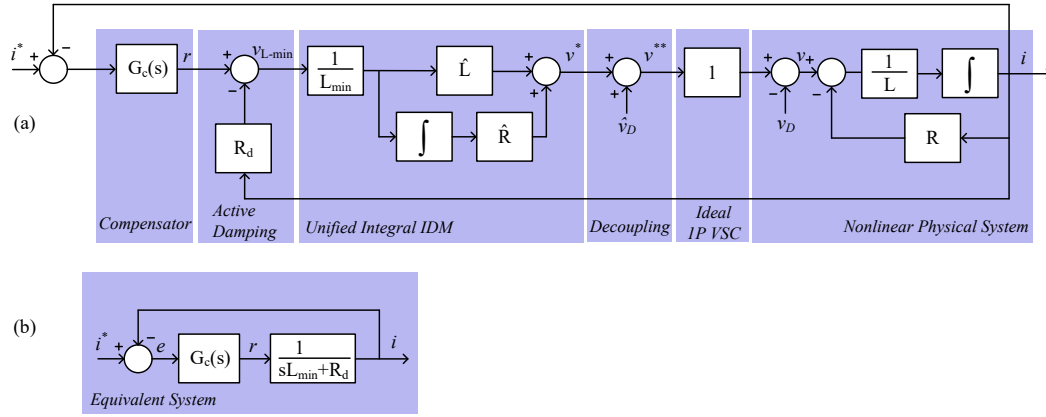


Figure 4.4: The closed-loop implementation of IDMBC method for 1P VSC system with active damping. (a) Overall current regulator architecture. (b) Simplified equivalent representation of the system.

4.3 A Resistive Decoupling Based Inductor Saturation Compensation Method in Single-Phase VSC systems

In this section, the saturation compensation with resistive decoupling (SCRD) method is developed to overcome the poor dynamic response and generation of low order harmonics in the steady-state weaknesses of CCR systems employing nonlinear inductors. With the L-R parameter information in hand, using this approach, a fictitious overall equivalent plant consisting of only a linear inductor with an inductance value of L_{min} is obtained in the end. The method is an adaptation of the feedback linearization approach described in [66] (Chapter 6) and [70] to power electronics applications, specifically to the given VSC system with a saturable inductor. The development of the method is provided in the following discussion.

The VSC output voltage (v^{**}) is composed of the disturbance term (v_D) and the L-R circuit voltage as explained in chapter 3 section 3.2.1.1,

$$v^{**} = L \frac{di}{dt} + Ri + v_D. \quad (4.4)$$

When voltage decoupling is performed, the system can be represented as

$$v^* = L \frac{di}{dt} + Ri + v_D - \hat{v}_D \quad (4.5)$$

where $v^* = v^{**} - \hat{v}_D$. With the a priori parameter data and the measured current, the resistive term can be decoupled as in (4.6). When the estimated/measured parameters are sufficiently close to the actual values, (4.6) simplifies to (4.7) rendering the sole nonlinear inductor characteristic

$$v_L = L \frac{di}{dt} + Ri - \hat{R}i + v_D - \hat{v}_D \quad (4.6)$$

$$v_L = L \frac{di}{dt}. \quad (4.7)$$

Having a reduced system with a nonlinear inductance of the form in (4.7), the system can be linearized by dividing v_L by the instantaneous estimated inductance \hat{L} . This linear model is not only valid in the sense of small-signal (*i.e.* Jacobian linearization), but in large-signal also. Multiplying (4.7) with L_{min} , the minimum inductance value of the varying L, (4.8) is obtained as

$$v_{L-min} = \frac{L_{min}}{\hat{L}} v_L = \frac{L_{min}}{\hat{L}} L \frac{di}{dt} \quad (4.8)$$

where v_{L-min} is the virtual control voltage. When the estimated inductance is equal to actual inductance ($\hat{L} = L$), (4.9) can be obtained as intended; a constant inductance system with an inductance of L_{min} and a control voltage of v_{L-min}

$$v_{L-min} = L_{min} \frac{di}{dt}. \quad (4.9)$$

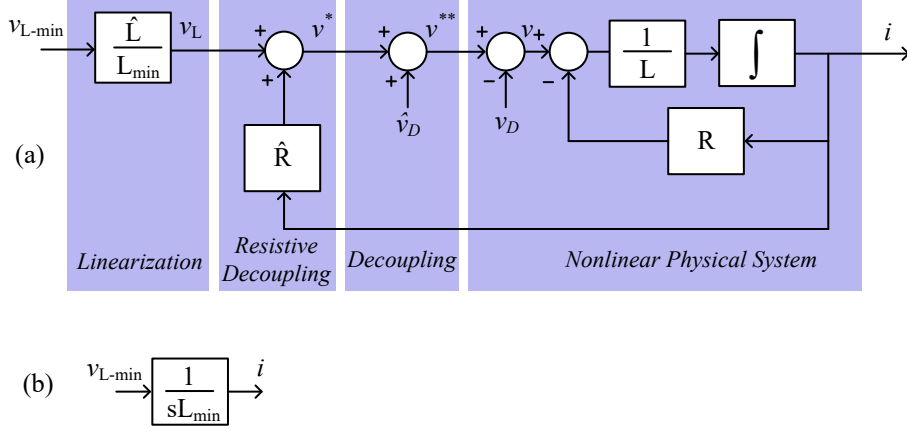


Figure 4.5: Inductor nonlinearity compensation with resistive decoupling. (a) Linearization of nonlinear L-R system with decouplings disclosed. (b) Simplified equivalent linear system.

In Figure 4.5(a), the procedure of reducing the nonlinear L-R system into a linear constant inductance system is summarized. In Figure 4.5(b), the equivalent linear system is illustrated when the estimation of system parameters and decouplings are performed accurately.

With these arrangements, the overall closed-loop control scheme becomes as shown in Figure 4.6(a). In the scheme, $G_c(s)$ provides the output signal v_{L-min} . When this signal is passed through the linearization and decoupling blocks, the VSC output voltage is obtained that will yield approximately the desired current in the output of the nonlinear physical system. With the simplification in Figure 4.5, the current error compensator $G_c(s)$ sees a linear system with a constant inductance ($1/sL_{min}$) as shown in Figure 4.6(b). Consequently, the CLTF of the system becomes as

$$\frac{I(s)}{I^*(s)} = \frac{G_c(s)}{G_c(s) + sL_{min}}. \quad (4.10)$$

With such simplification, considering the discussion in Section II, one can employ linear controllers in the form of (3.2) and precisely determine the bandwidth of the overall linearized system.

Although the resistive decoupling approach seems similar to the concept of active

damping by a virtual resistor which is a frequently employed technique in power electronics, the aim of the method is essentially different. Active damping is employed to increase the damping of an oscillatory control system by adding a virtual resistance from the forward path ($v^* = v_L - i \cdot R_{active}$) where R_{active} is the fictitious damping resistor [50]. On the contrary, resistive decoupling of the proposed method is performed to totally eliminate the system resistance from the control loop ($v^* = v_L + i \cdot \hat{R}$).

The impact of resistive decoupling on control performance enhancement is strong in low power (kW level) VSC applications where the inductor ESR is relatively large and its significance is less in large converters (larger than several tens of kW ratings). In either case, the accompanying inductor nonlinearity cancellation stage is the essential part of the controller for high performance. Thus, the combination of the two techniques yields the best performance and makes the algorithm applicable to a wide power range.

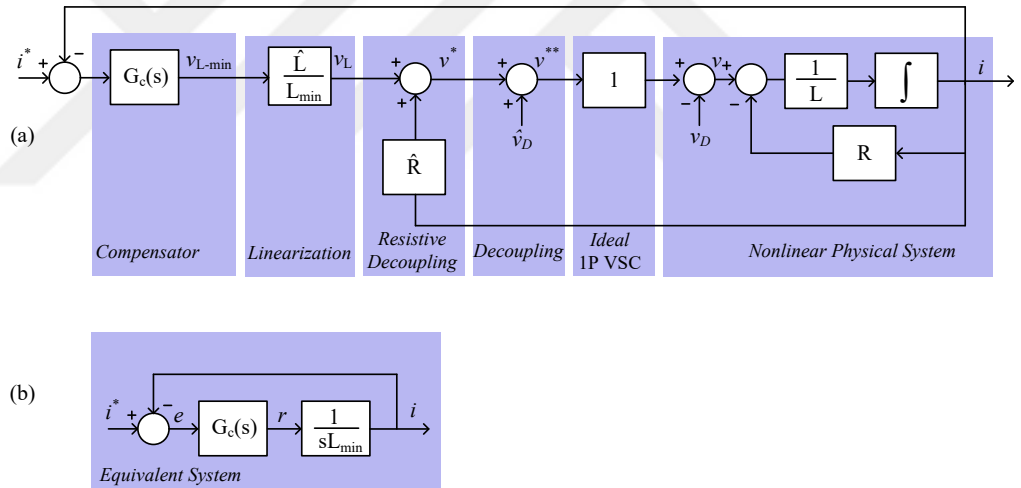


Figure 4.6: The closed-loop implementation of SCR D method for 1P VSC system. (a) Overall current regulator architecture. (b) Simplified equivalent representation of the system.

4.3.1 Incorporation of Active Damping

With the closed-loop control system obtained in Figure 4.6 with a fictitious linear inductor of L_{min} , active damping can be employed in SCR D method as in the

In Figure 4.8, the generic current control system block diagram is shown involving the current command signal (i^*), the system output (i), the load voltage (v), and the disturbance signal (d). The disturbance signal is the difference between the estimated disturbance compensation voltage and the actual disturbance voltage which is given as

$$D \triangleq \hat{v}_D - v_D. \tag{4.12}$$

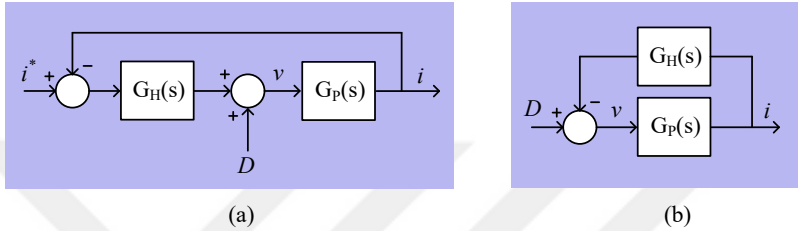


Figure 4.8: Generic control block diagram showing the command current, the output current, and the disturbance signals.

The CCR, K_p scheduling, and SCRD methods can be represented in the form shown in Figure 4.8. It should be noted that $G_P(s)$ is the physical plant transfer function ($1/(sL + R)$) whereas $G_H(s)$ is the overall form of the other system block elements in the overall current regulation system. In the following command to output and disturbance to output analyses, resonant controller term of the compensator is not involved as the contribution to system dynamics is minimal and introduces redundant complexity to analyses.

4.4.1 Command to Output Characteristics

Considering the current control methods in the form of Figure 4.8 with setting the disturbance to zero, command to output characteristics of the methods are obtained. The frequency characteristics of the current control methods are derived in terms of open-loop transfer functions (OLTFs), however, the CLTFs of the methods can be obtained simply by the relation

$$\frac{I(s)}{I^*(s)} = \frac{G_H(s)G_P(s)}{1 + G_H(s)G_P(s)}. \quad (4.13)$$

where the product $G_H(s)G_P(s)$ represents the system OLTF. As elaborated previously, the K_p gain of the CCR should be set in proportion to the minimum inductance $K_p = \omega_{BW} \times L_{min}$ and the K_i gain should be set in proportion to the estimated resistance as $K_i = \omega_{BW} \times \hat{R}$. Then the OLTF of CCR ($G_{OL}^{CCR}(s)$) is obtained as

$$G_{OL}^{CCR}(s) = \frac{s\omega_{BW}L_{min} + \omega_{BW}\hat{R}}{s^2L + sR}. \quad (4.14)$$

In the case of K_p scheduling, K_p gain is set in proportion to the estimated inductance rather than the minimum inductance as $K_p = \omega_{BW} \times \hat{L}$. The setting of the integral gain is the same that of CCR. Therefore, the OLTF of K_p scheduling method ($G_{OL}^{KpSc.}(s)$) can be obtained as

$$G_{OL}^{KpSc.}(s) = \frac{s\omega_{BW}\hat{L} + \omega_{BW}\hat{R}}{s^2L + sR}. \quad (4.15)$$

$$G_{OL}^{IDMBC}(s) = \frac{s^2\omega_{BW}\hat{L}L_{min} + s(\omega_{BW}L_{min}\hat{R} + \omega_{BW}R\hat{L}) + \omega_{BW}R\hat{R}}{s^3LL_{min} + s^2RL_{min}}. \quad (4.16)$$

The K_p and K_i gains of SCRD method are the same that of CCR. However, the OLTF of SCRD method ($G_{OL}^{SCRD}(s)$) is quite distinct which is given as

$$G_{OL}^{SCRD}(s) = \frac{s\omega_{BW}\hat{L}L_{min} + \omega_{BW}\hat{L}\hat{R}}{s^2LL_{min} + s(RL_{min} - \hat{R}L_{min})}. \quad (4.17)$$

Based on the OLTFs of the methods obtained, the magnitude and phase plots of the investigated methods are provided in Figure 4.9 for the maximum and minimum values of the inductance characteristics shown in Figure 4.11(b) for a bandwidth of $2\pi 500$ rad/s. The bandwidth of the CCR (ω_{BW}^{CCR}) shrinks down to approximately one-third of the design bandwidth while the bandwidths of K_p scheduling and SCRD methods are conserved due to their adaptive nature to the inductance change. When the inductor current goes to its maximum, the OLTF of CCR approaches to that of K_p scheduling which implies a time varying command to output frequency response characteristics.

In addition to its time-invariant frequency response characteristics of SCR D method, the high gain characteristic in the low-frequency region as shown in the figure gives better command tracking capability in the low-frequency region. Considering the phase plot in Figure 4.9, the phase margin of CCR (PM^{CCR}) at $L = L_{max}$ is 77.7° . When the inductance is decreased to its minimum value ($L = L_{min}$) the PM^{CCR} increases to 90° , which is the phase margin of K_p scheduling PM^{KpSc} , which is time-invariant with correct estimated parameter values. In addition, the phase margin of SCR D ($PM^{SCR D}$) is 82.4° . Based on these values, it can be concluded that the phase margins of the current controllers are sufficient for stable operation.

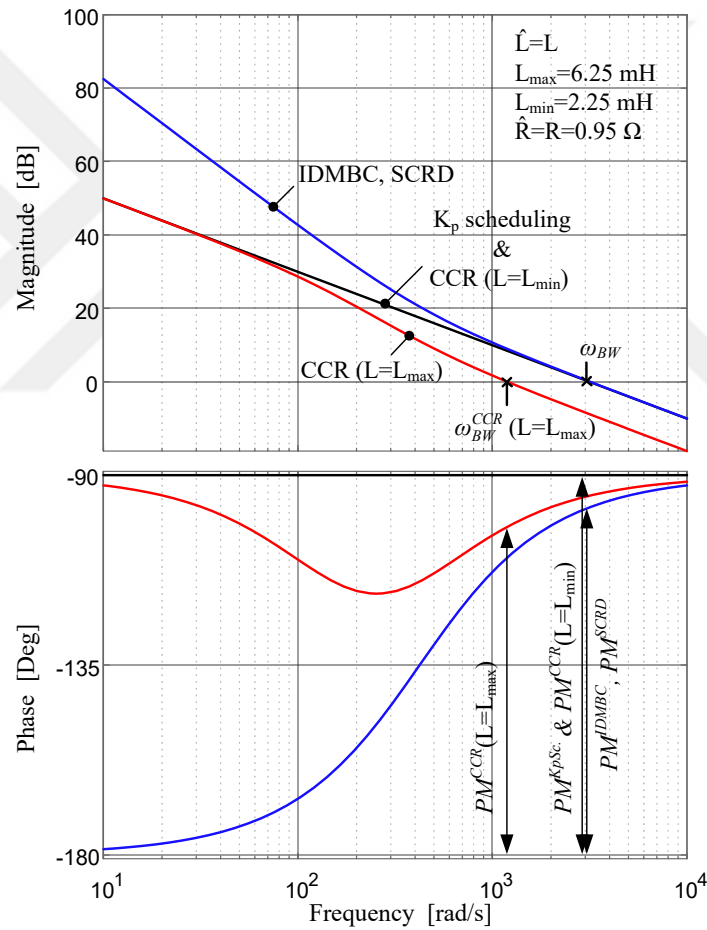


Figure 4.9: Open-loop magnitude and phase responses of CCR, K_p scheduling, and SCR D methods for maximum and minimum inductance cases.

4.4.2 Disturbance Rejection Characteristics

In VSCs, it is common to decouple disturbance effects such as dead-time generated voltage loss, DC-link voltage variation, and the grid voltage. However, the decoupling of those disturbances can be performed neither in infinite precision nor without error due to noise. Thus, some of those disturbance effects leak to the system as described by (4.12) and shown in Figure 4.8(b). In the figure, while the physical plant $G_P(s)$ is the same for all current control methods, $G_H(s)$ is unique to each method. Having these functions, the disturbance to output transfer functions ($F_D(s) \triangleq I(s)/D(s)$) can be obtained by

$$\frac{I(s)}{D(s)} = \frac{G_P(s)}{1 + G_H(s)G_P(s)}. \quad (4.18)$$

Accordingly, the disturbance to output transfer functions are obtained in (4.19), (4.20), (4.21), and (4.22) for CCR, K_p scheduling, IDMBC, and SCR D respectively.

$$F_D^{CCR}(s) = \frac{s}{s^2L + s(\omega_{BW}L_{min} + R) + \omega_{BW}\hat{R}}. \quad (4.19)$$

$$F_D^{KpSc.}(s) = \frac{s}{s^2L + s(\omega_{BW}\hat{L} + R) + \omega_{BW}\hat{R}}. \quad (4.20)$$

$$F_D^{IDMBC}(s) = \frac{as^2}{bs^3 + cs^2 + ds + e}. \quad (4.21)$$

where $a = L_{min}$, $b = LL_{min}$, $c = RL_{min} + \omega_{BW}\hat{L}L_{min}$, $d = \omega_{BW}L_{min}\hat{R} + \omega_{BW}\hat{L}\hat{R}$, and $e = \omega_{BW}\hat{R}^2$.

$$F_D^{SCR D}(s) = \frac{s}{s^2L + s(\omega_{BW}\hat{L} + R - \hat{R}) + \omega_{BW}\hat{R}\hat{L}/L_{min}}. \quad (4.22)$$

In Figure 4.10, the magnitude plots of the disturbance to output transfer functions of the current control methods under investigation are illustrated for the maximum and minimum inductance values of the L-i characteristics shown in Figure 4.11(b) and

problem elaborated in this study, it is used for observing gain, phase, and bandwidth characteristics of the current regulators. Apparently, the motivation behind the use of the frequency response in this kind of system is the relatively slow change of the system dynamics allowing such a use.

4.5 Identification of System Parameters in Single-Phase Controlled VSCs

In the implementation of the SCRDC current control, system resistance and inductance parameters are required [42, 48]. For the identification, the following methods are used.

4.5.1 Resistance Identification

The resistance of the VSC up to the load terminals can be determined by the DC excitation of the VSC at different current levels. With conventional current regulation, the ratio of the DC voltage command difference to VSC current command difference at two operating points (v_1^*, i_1^*) and (v_2^*, i_2^*) yields the identified R value that includes inductor, cable, and VSC semiconductor resistive effects that contribute to system dynamics ($\hat{R} = (v_1^* - v_2^*) / (i_1^* - i_2^*)$) [50]. To increase the signal to noise ratio, the current commands (i_1^*, i_2^*) should be sufficiently large and differ from each other (preferably with opposite polarity).

4.5.2 Inductance Identification

The incremental inductance identification in equation (2.8) involves perturbation around an operating point. Starting from zero current level, the inductor should be DC biased via a current controller to provide the operating point. Then for a specified duration, the current controller is disabled and the inductor is open-loop voltage mode driven such that with sufficient volt-seconds, the current and the flux of the core are incremented, yielding the information to calculate the incremental inductance accurately. This procedure should be repeated for as many points as intended to obtain the L-i curve.

The procedure for the identification in sinusoidal form is as follows: First, the peak of the current command (i_p^*) is set to the current value at which the measurement will take place. With the current controlled, the VSC drives the current to its peak command value, i_p^* . When the current is equal to i_p^* , a voltage perturbation (Δv) is applied for a perturbation time of τ_p with the resistive voltage drop compensation term ($\hat{R} \cdot i$) and inverter disturbance compensation voltage (v_{id}) are feedforwarded). Accordingly, the voltage command to the modulator (as represented in Figs. 3 and 9) can be obtained as $v^{**} = \Delta v + \hat{R} \cdot i + v_{id}$. During this period, the inductor current is not controlled and the applied Δv yields a volt-seconds (flux) increment $\Delta \lambda$ according to

$$\Delta \lambda = \int_{\tau_p} \Delta v dt \approx \Delta v \tau_p. \quad (4.23)$$

The incremental inductance at i_p^* then can be obtained by making use of the calculated flux increment and the measured current increment (Δi) as

$$\hat{L}(i_p^*) = \left. \frac{\Delta \lambda}{\Delta i} \right|_{i_p^*} \approx \left. \frac{\Delta v \tau_p}{\Delta i} \right|_{i_p^*}. \quad (4.24)$$

At the end of the period τ_p , current control of the VSC resumes and brings the current to its set value. Then the i_p^* is incremented and the next identification cycle starts. Repeating the procedure for each predefined current level within the rating range (at distinct cycles), L-i characteristics of a saturable inductor can be obtained in data pairs. In the application, keeping (Δv) sufficiently high, the signal to noise ratio can be kept high to yield accurate inductance value. In the implementation, the measured data pairs can be used directly from a look-up table or the data can be approximated as a polynomial (Figure 4.11(b)).

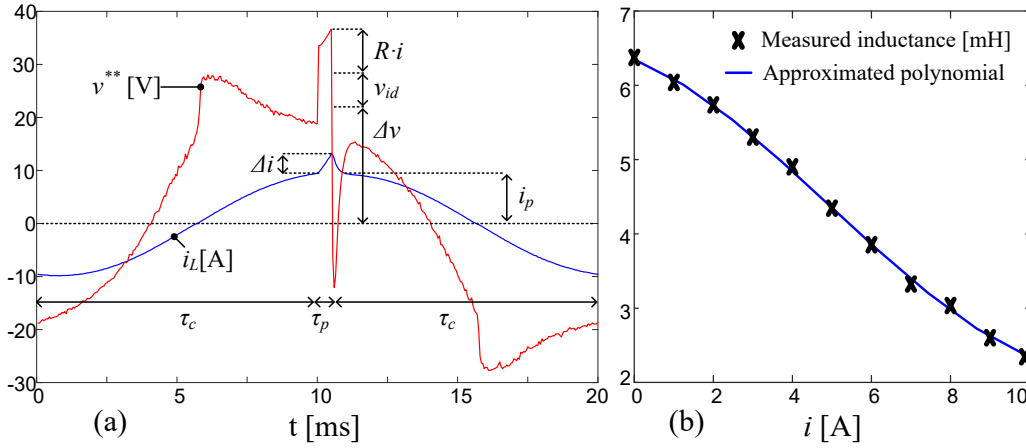


Figure 4.11: Inductance identification waveforms. (a) The voltage command and VSC current for the identification of inductance value at i_p^* . (b) The measured and approximated L-i characteristics of the utilized inductor.

The parameter identification method proposed in this section is utilized during the converter system initialization stage and associated parameter data is embedded in a digital platform to be used in the converter system. In most commercial grid-connected VSCs, the parameters and the controller gains are set in the factory during product initialization and performance tests. Therefore, the offline parameter identification and controller gain tuning approach used in this method are sufficient for most applications. However, with some effort, the proposed approach can be extended to achieve auto-tuning and online parameter identification. Alternative online and offline parameter identification and tuning approaches may be adopted as well along with the control method proposed [55], [71–75].

4.6 Validation of Inductor Saturation Compensation in Single-Phase Controlled VSC Systems via Simulations

In order to evaluate the performances of the IDMBC and SCR D methods, simulations and experiments are conducted for the same hardware and control parameters. CCR and K_p scheduling methods are also accompany to IDMBC and SCR D methods to constitute a basis for the comparison. Accordingly, system configuration information is provided first. Then the dynamic response of the methods is observed to examine

the bandwidth shrinkage issue both for DC, and AC systems. Then AC current waveform quality of the methods is investigated for $2\pi 100$ rad/s and 500 rad/s maximum bandwidth systems. Afterward, the effects of estimated parameter mismatch on the dynamic response and waveform quality are studied.

4.6.1 System Configuration

The system configuration is described by means of system hardware and system control.

4.6.1.1 System Hardware

Simulations and experimental studies are conducted for a 1P FB VSC setup (with 400 V DC-bus voltage) to prove the viability of the proposed control method. A saturable inductor with the $L-i$ characteristics of Figure 4.3(b) is manufactured for a rated current of $10 A_{\text{peak}}$, utilizing a sendust magnetic core [3]. The same inductance characteristics are employed in the simulations also. Results of CCR and K_p scheduling methods accompany these of SCRD and IDMBC methods to form a comparison basis. The simulations and experiments are conveyed in two configurations; inverter terminals short-circuited and grid-connected (Figure 4.12 (a) and (b) respectively).

Both in simulations and experiments, the short-circuited configuration is used for: 1-inductance and resistance parameter identification, 2-DC dynamic response tests, 3-exaggeratedly low bandwidth tests. On the other hand, the grid-connected configuration is used for: 1-AC dynamic response investigation, 2-AC waveform quality investigation. In the grid-connected configuration, a capacitor is inserted between the grid and the inductor to form an LCL filter structure to attenuate the PWM ripple current from the grid [32], while the injected grid current is kept in phase with the grid voltage.

Prior to conducting simulations and experiments testing the performance of the current controllers, characterization of the converter system resistance and saturable inductance were performed via short-circuited VSC experiment (Figure 4.12(a)) by em-

ploying the identification methods provided in section III-c. The associated procedure for parameter identification will be given in the experimental results section.

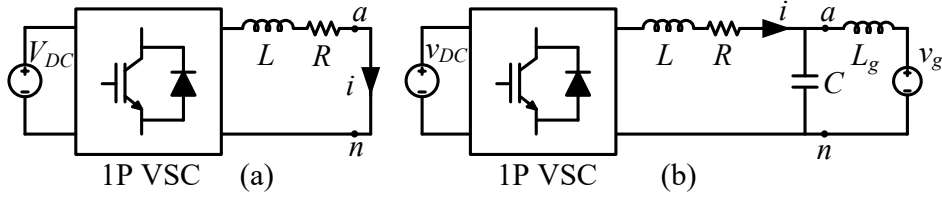


Figure 4.12: (a) VSC+inductor terminals short-circuit configuration. (b) Grid-connected VSC with LCL filter configuration.

In Table-4.1, simulation and experimental setup parameters for the configurations in Figure 4.12 are tabulated.

Table 4.1: Experimental System Parameters

Parameter	Value
DC-link voltage	400 V
Rated current	10 A_{peak}
Grid voltage	230 V_{RMS}
ω_e	$2\pi 50$ rad/s
Power module	PM75RL1A120
f_c	10 kHz
Modulation method	Unipolar
Sampling period (T_s)	50 μs
Inverter dead-time	3 μs
L_{max}/L_{min}	6.25/2.25 mH
R (equivalent resistance)	0.95 Ω
C (LCL filter capacitor)	2.2 μF (2.2 %)

4.6.1.2 System Control

In order to observe the current waveform quality differences among control methods, simulations and experiments are conducted. In the experiments, the discrete-time controller is realized via a 150 MHz floating-point digital signal processor. The interrupt cycle which is $50 \mu s$ provides a double update in a PWM cycle which is $100 \mu s$ (10 kHz). At every interrupt cycle, the controller executes the grid synchronization PLL (single-phase vector PLL method), current control algorithms including anti-windup, software VSC protection, and PWM signal generation. The control scheme in Figure 4.4(a) and 4.7(a) summarizes the continuous-time implementation of the method. The digital implementation can be performed via standard methods such as forward Euler, backward Euler, and Tustin discretization. Amongst, the backward Euler method is utilized for the discretization of the continuous-time controllers.

The experiments and the simulations are conducted at an exaggeratedly low bandwidth of $\omega_{BW} = 2\pi 100$ rad/s (with VSC+inductor terminals short-circuit configuration that of Figure 4.12(a)). All other simulations and experiments are performed for $\omega_{BW} = 2\pi 500$ rad/s (practical bandwidth). In each simulation and experiment, the $G_c(s)$ parameters are adjusted according to the particular bandwidth requirement. As the proportional gain (K_p) determines the bandwidth of the system, it is set to adjust the ω_{BW-max} of the system for distinct experiments at bandwidths of $\omega_{BW} = 2\pi 100$ rad/s and $\omega_{BW} = 2\pi 500$ rad/s and kept constant throughout the associated experiments for CCR, and SCRD methods. In the case of K_p scheduling method, this coefficient is changed in proportion to the varying inductance value dynamically ($K_p = \omega_{BW} \times \hat{L}$). The integral gain is set in proportion to the given design bandwidth for all control methods ($K_i = \omega_{BW} \times \hat{R}$) and kept constant throughout the associated experiments. The value of the resonant controller gain is selected so that the steady-state error at ω_e to be acceptably small ($K_r = 500 \Omega$). The damping term (ζ) of the resonant controller determines the width of resonant frequency band ($\Delta\omega$) to track the fundamental frequency of the command signal in the case of grid frequency deviations. This parameter is set to yield $\Delta\omega$ to be 1 rad/s in accordance with the relation $\Delta\omega = 2\zeta\omega_e$ [76]. In Table 4.2, system controller parameters are given for $\omega_{BW} = 2\pi 100$ and $\omega_{BW} = 2\pi 500$ rad/s of design bandwidth values.

Table 4.2: Current Controller Parameters

$\omega_{BW}(\text{rad/s})$	$K_p(\Omega)$	$K_i(\Omega/s)$	$K_r(\Omega)$
$2\pi 100$	1.4	597	500
$2\pi 500$	7	2984	500

4.6.2 Dynamic Response

Dynamic response of the single-phase VSC system is studied under DC excitation (with VSC+inductor terminals short-circuited) and AC excitation (grid-connected).

4.6.2.1 Dynamic Response at DC Excitation

For the case of DC excitation, simulated dynamic responses of current controllers are given for 1 A (10% of rated peak) step increments in the current command (δi^*) at distinct DC-bias currents (0 to 10 A) in Figure 4.13 for $\omega_{BW} = 2\pi 500$ rad/s. As the simulations are performed at DC operating conditions, the resonant term of the compensator is omitted and K_p and K_i parameters are used for the $\omega_{BW} = 2\pi 500$ rad/s that are listed in Table-4.2. Figure 4.13 shows that with a decrease in the current, the reference tracking performance of CCR decreases as expected. On the other hand, the dynamic performances of IDMBC, SCR, and K_p scheduling methods are conserved when the inductor current decreases (inductance increases) as a result of improvement in the bandwidth.

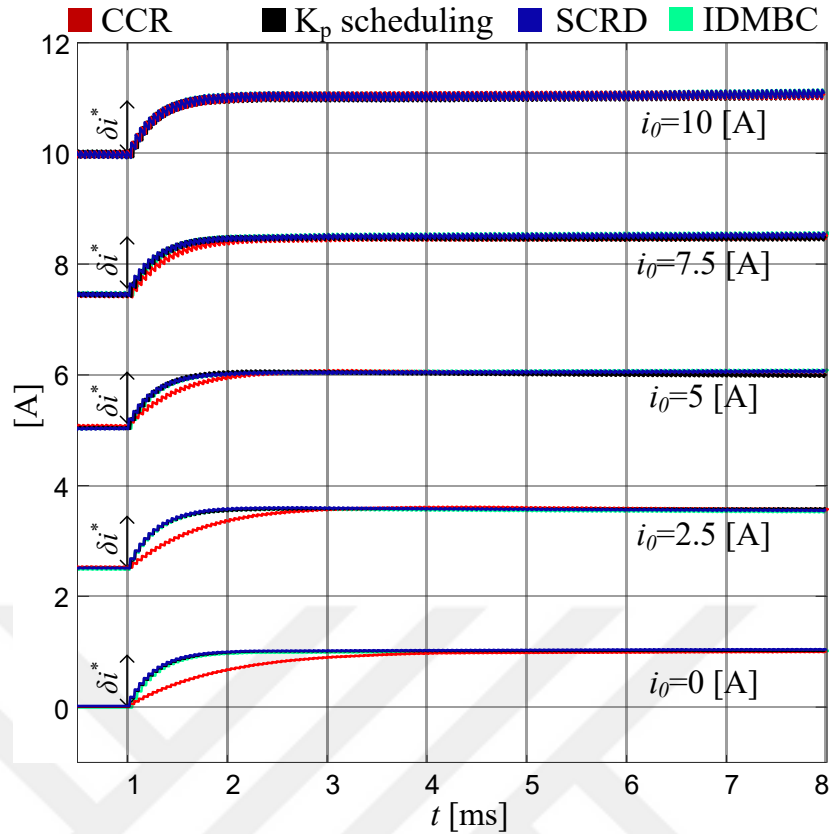


Figure 4.13: Simulated current command step responses of CCR, K_p scheduling, and SCR methods at 0 to 10 A DC-bias levels.

4.6.2.2 Dynamic Response at AC Excitation

In Figure 4.14, the simulated dynamic responses (double sampled converter side inductor currents and associated current errors) of the control methods are illustrated for AC grid-connected system (with harmonic-free grid voltage). The current reference magnitude is incremented by 2 A (20% of rated peak) for the two cases: from 0 to 2 A and from 9 to 11 A (the change is initiated at the peak of the waveform). As the VSC is operated at 50 Hz, the compensator involves resonant term and the overall system has $\omega_{BW} = 2\pi 500$ rad/s. Similar to the DC dynamic response simulations IDMBC, SCR, and K_p scheduling methods perform better than CCR method for 0 to 2 A increment case (the initial slope of the current (di/dt) is higher for IDMBC, SCR and K_p scheduling than CCR). When the increment is from 9 to 11 A (at the peak value of the current), the slope of the current waveforms are same as the bandwidths

of the three methods become the same at the rated current. A very similar dynamic response characteristics of K_p scheduling, IDMBC, and SCR D methods are observed. This is an expected result as the frequency response characteristics of these methods are the same with the same estimated system parameters and active damping resistor value with the actual resistor value.

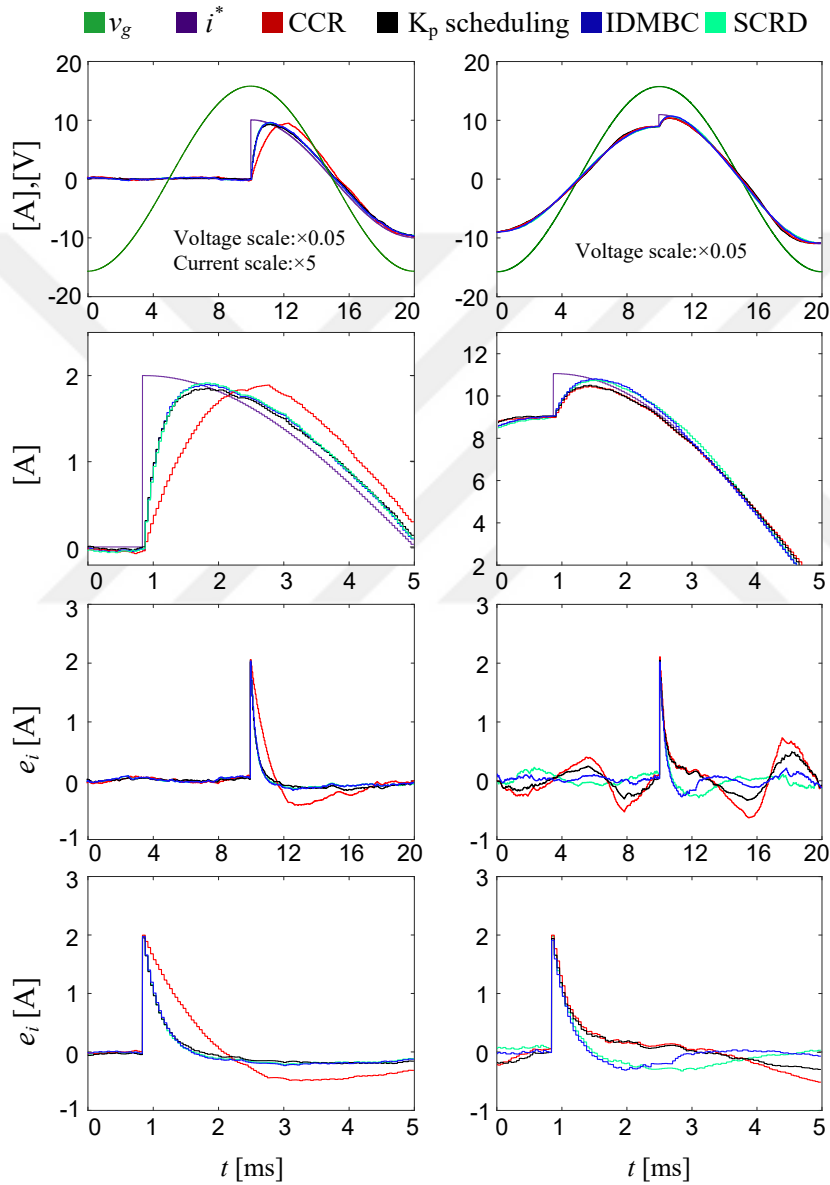


Figure 4.14: Simulated responses of CCR, K_p scheduling, IDMBC, and SCR D methods to a 2 A step change δi^* in the AC current command magnitude: for 0 to 2 A (left) and 9 to 11 A (right).

4.6.3 Waveform Quality

The waveform quality performances of the methods are investigated for exaggeratedly low bandwidth and practical bandwidth. The exaggeratedly low bandwidth is performed for the purpose of observation of pure characteristics of the methods by minimizing the corrective effect of high bandwidth.

4.6.3.1 Exaggeratedly Low Bandwidth

For the purpose of demonstrating the superiority of the IDMBC and the SCRd method, simulations are conducted at a maximum bandwidth of $2\pi 100$ rad/s for the terminal short-circuited configuration in Figure 4.12(a). By omitting the grid connection, it is aimed that the grid induced harmonics are totally eliminated from the measurements (to be studied in the experimental results and performed for simulations also for consistency). Similarly, the purpose of using low bandwidth is to lessen the corrective effect of higher bandwidth on the control methods. Operating with such arrangements, the low-frequency current harmonic content will be solely due to the converter system with a nonlinear inductor. Hence, the current regulation performance differences of the control methods become transparent. With short-circuit configuration, the VSC current command is set as $i^* = 10\sin(2\pi 50t)$ A. To have such a low bandwidth, the gains are set according to Table-4.2 both for CCR, IDMBC and SCRd methods and updated dynamically in proportion to the inductance value for K_p scheduling method as expressed formerly. With such an exaggeratedly low bandwidth, the inductor current clearly deviates from the current command for the cases of CCR and K_p scheduling methods as shown in Figure 4.15. The same figure shows that when the IDMBC and SCRd methods are employed with the same G_c parameters of CCR, the current waveform quality is significantly improved even for such a low bandwidth when compared to other methods. The figure shows that the 3rd harmonic (12.4 % for CCR) is practically eliminated with the application of IDMBC and SCRd. Similarly, other low-frequency harmonics are mitigated considerably and the total harmonic distortion of the current (THD_i) is reduced from 12.8 % to below 1 %.

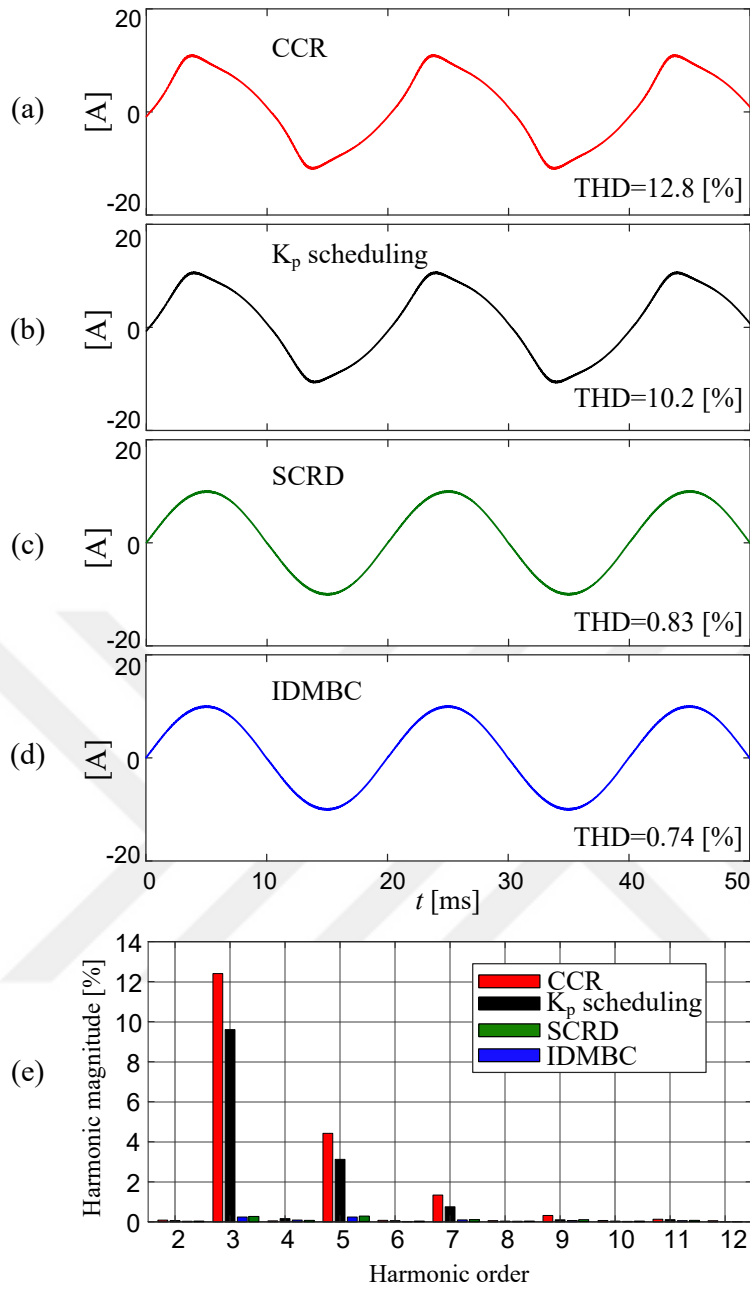


Figure 4.15: Simulated saturable inductor current and associated harmonic spectra of 1P FB VSC for a maximum bandwidth of $2\pi 100$ rad/s when VSC+inductor terminals are short-circuited.

4.6.3.2 Practical Bandwidth

The LCL filtered system configuration in Figure 4.12(b) is used for grid-connected simulations with $\omega_{BW} = 2\pi 500$ rad/s. In a practical grid, the line voltage is polluted with low-frequency harmonics. Thus, the current controller performance is considered under such realistic conditions. For this purpose, in the simulations, the grid voltage waveform with harmonic distortion is considered. In Figure 4.16 the utilized grid voltage waveform and the associated harmonic spectrum are depicted. In the simulations, $50 \mu H$ and $10 m\Omega$ grid side impedance are utilized. The resultant grid current waveforms for CCR, K_p scheduling, IDMBC, and SCRDM methods are illustrated in Figure 4.17. When compared to Figure 4.15, THD_i of CCR and K_p scheduling methods are improved due to the increase in the current control bandwidth (increased K_p in accordance with the table-4.2). On the other hand, in spite of the increase in the bandwidth, an increase in the THD_i of IDMBC and SCRDM can be observed when compared to Figure 4.15 due to grid voltage harmonics. Although the grid voltage harmonics interfere with the system, IDMBC and SCRDM method are still superior to CCR and K_p scheduling methods in terms of current waveform quality.

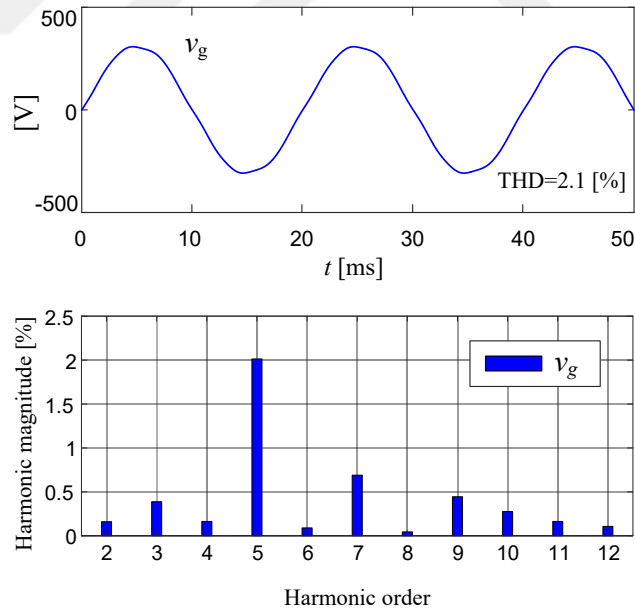


Figure 4.16: Simulated grid voltage, and grid currents of the current control methods of grid-connected 1P FB VSC for $\omega_{BW} = 2\pi 500$ rad/s, and associated harmonic spectra.

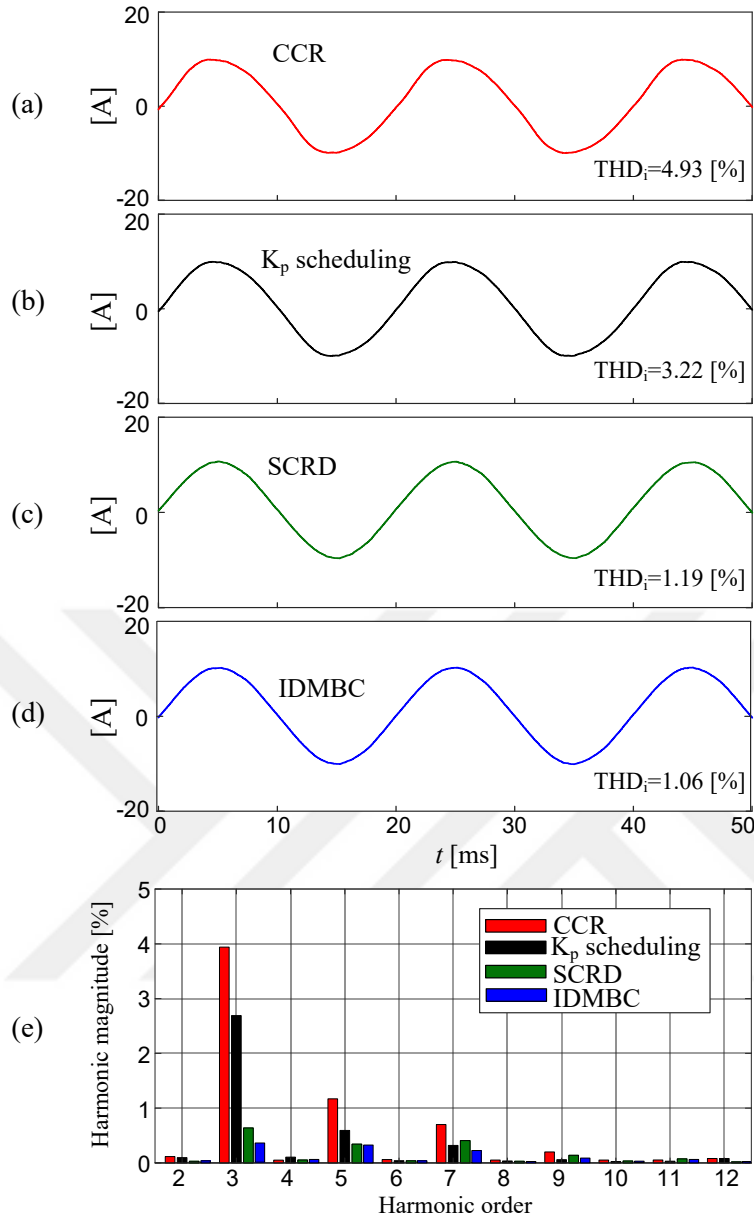


Figure 4.17: Simulated grid voltage, and grid currents of the current control methods of grid-connected 1P FB VSC for $\omega_{BW} = 2\pi 500$ rad/s, and associated harmonic spectra.

4.6.4 Performance Under Parameter Mismatch

In the study so far, it has been assumed that the inductor characteristic and its ESR parameters are precisely known. However, in the field, the parameter estimation method may have an error. Likewise, the parameters may vary due to operating conditions.

This section investigates the parameter sensitivity of the converter performance for both steady-state and dynamics for the proposed IDMBC and SCRD methods. The grid-connected configuration with harmonic-free grid voltage for $\omega_{BW} = 2\pi 500$ rad/s case is simulated. The cases with $\pm 20\%$ under/over estimated inductance and resistance values are utilized in the simulations. Additionally, exact estimation case is kept as a reference. Figure 4.18 illustrates the dynamic performances of the underestimated/overestimated cases of IDMBC method. As the waveforms show, the dynamic response deviation from the nominal parameters case for 0 to 2 A and 9 to 11 A changes in the current command is negligible. A similar conclusion is also reached for SCRD method. In Figure 4.18, the dynamic response current and current error waveforms belonging to the parameter mismatch cases exhibit a slight deviation from that of the perfect parameter estimation case.

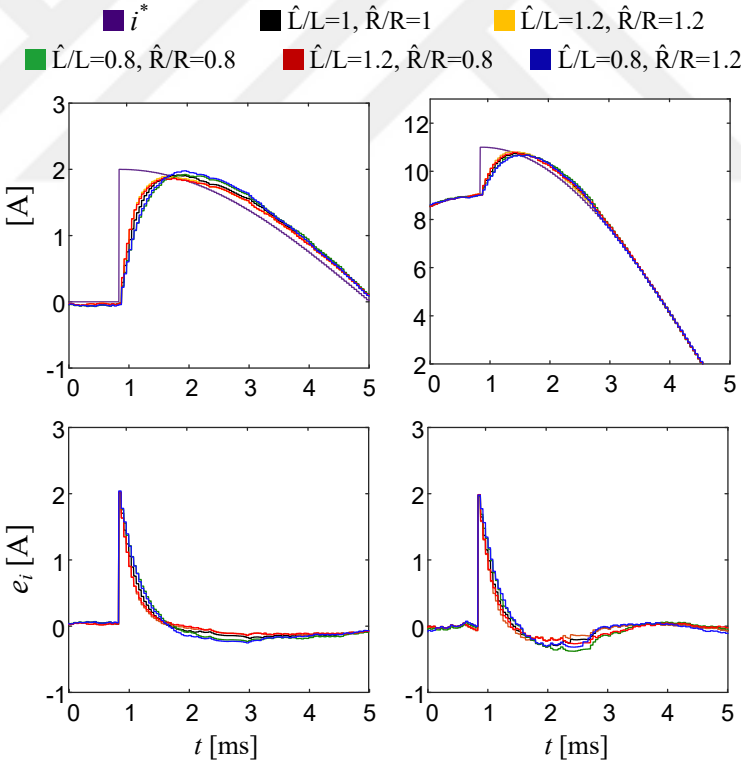


Figure 4.18: Simulated responses of IDMBC method to a 2 A step change δi^* in the AC current command magnitude under parameter mismatch conditions: for 0 to 2 A (left) and 9 to 11 A (right).

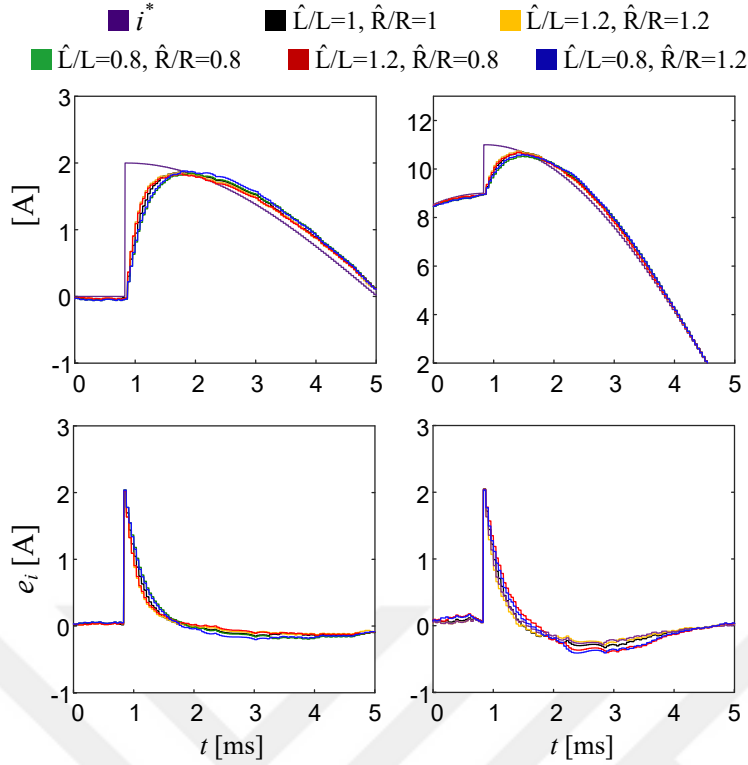


Figure 4.19: Simulated responses of SCR method to a 2 A step change δi^* in the AC current command magnitude under parameter mismatch conditions: for 0 to 2 A (left) and 9 to 11 A (right).

For the steady-state current waveform quality performance of the mismatch cases, THD_i values of the grid are provided in Table-4.3 (10 A_{peak} sinusoidal current command, $\omega_{BW} = 2\pi 500$ rad/s, harmonic-free grid voltage). It is seen that the THD_i performance is best when there is no mismatch between the estimated and actual parameters except the case when $\hat{L}/L = 1.2$ and $\hat{R}/R = 0.8$. For SCR method, the minimum THD_i is observed when $\hat{L}/L = 1.2$ and $\hat{R}/R = 1.2$. For both minimum THD_i points for the methods, the system bandwidth is increased indirectly by increasing the estimated inductance value. Therefore, such an increase is not surprising.

Even for such deviation cases, THD_i of these methods is still better than those of CCR and K_p scheduling methods with exact parameters (with no mismatch under the same simulation parameters: THD_i of CCR is 4.22 %, of K_p scheduling is 2.76 % with harmonic-free grid voltage). These results show that the SCR method preserves its advantage under 20 % parameter mismatch conditions. Since the proposed parameter

estimation method yields estimation accuracy better than 20 %, the SCRD method is considered to be robust to parameter deviations.

Table 4.3: Grid Current THD for Estimated Parameter Mismatch Cases

\hat{L}/L	\hat{R}/R	$THD_i^{IDMBC}[\%]$	$THD_i^{SCRD}[\%]$
1	1	0.84	1.23
1.2	1.2	0.76	1.03
0.8	0.8	1.02	1.64
1.2	0.8	0.68	1.12
0.8	1.2	1.48	1.5

4.7 Validation of Inductor Saturation Compensation in Single-Phase VSC systems via Experiments

In the experiments, the identification of system parameters is performed with the VSC+inductor terminals short-circuited configuration (Figure 4.12(a)) firstly. Afterward, dynamic response and waveform quality performances of the experimental results of the CCR, K_p scheduling, IDMBC, and SCRD methods are examined in the same sequence with the simulation study to confirm its results.

4.7.1 System Configuration

In Fig. 4.20, the experimental setup is illustrated. The VSC DC bus voltage is provided from the 3P isolated AC supply+rectifier configuration. The two legs of a three-phase IGBT power module is utilized to form a 1P-FB-VSC topology. The VSC is interfaced with the 50 Hz, 220 V utility grid through the saturable inductor, filter capacitor and EMI filter in cascade.

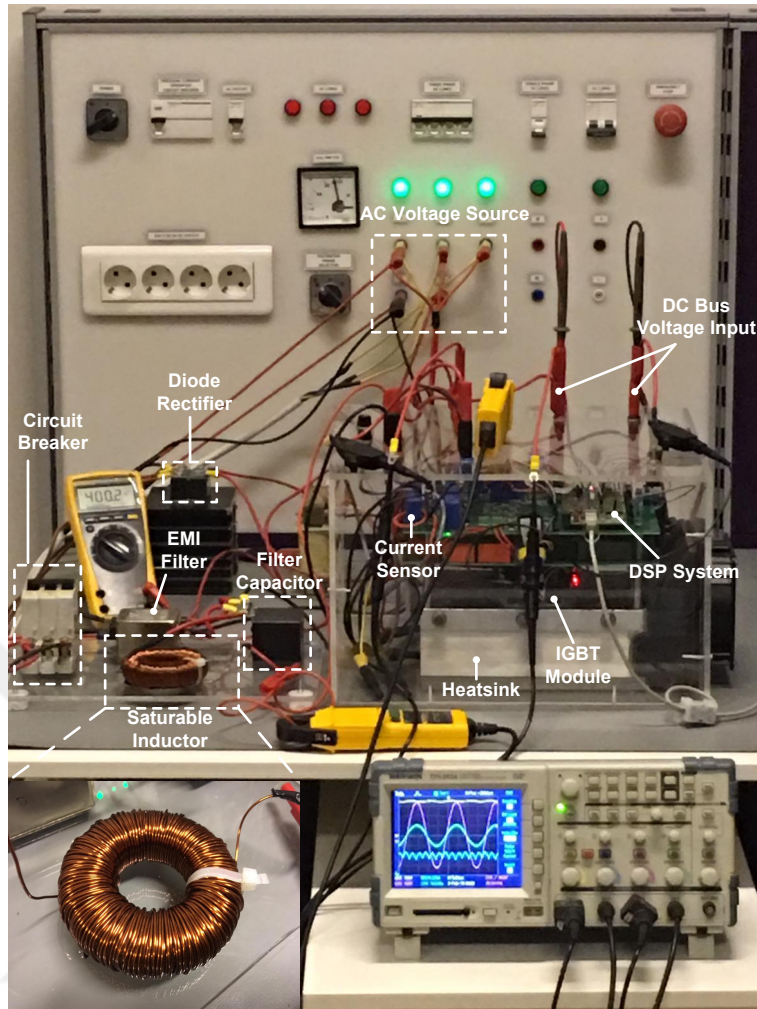


Figure 4.20: Single-phase grid connected VSC setup.

4.7.2 Resistance and Inductance Identification

Based on the identification methods elaborated previously, resistance and inductance identification of the built inductor is performed for the VSC+Inductor terminals short-circuited configuration (Figure 4.12(a)). The resistance of the system is identified by DC excitation of the system at two distinct operating points directly in accordance with the discussion in section 4.5 ($v_1^* = 9.5 \text{ V}$, $v_2^* = -9.5 \text{ V}$, $i_1^* = 10 \text{ A}$, $i_2^* = -10 \text{ A}$, hence $R = 0.95 \Omega$). Then, inductance identification is carried out. A perturbation voltage (Δv) of 20 V is applied to the inductor at the peak of the sinusoidal current (Figure 4.12(a)) while the current magnitude is increased from 0 to 10 A with 1 A intervals at each cycle. The perturbation time is chosen to yield sufficient current

increment (Δi) for accurate measurement as well as keeping Δi sufficiently low to keep small-signal behavior ($\tau_p=350 \mu sec$). Having L-i characteristics in data pairs, the calculation of \hat{L} is performed via a look-up table yielding the characteristic given in Figure 4.12(b).

Prior to parameter identification and all other experiments, the inverter generated disturbance voltage (v_{id} , corresponding to inverter dead-time generated and semiconductors' constant voltage drop losses) was characterized via experiments [1]. Using this disturbance voltage characteristic, the control loop is decoupled from this disturbance throughout the experiments. In the grid-connected configuration, the measured grid voltage is also decoupled from the control loop, as discussed in the theory sections.

4.7.3 Dynamic Response

4.7.3.1 Dynamic Response at DC Excitation

As in the simulations, all three methods are tested for their step function responses at different current levels for the configuration in Figure 4.12(a). The same parameters of the simulations are used in the experiments. In Figure 4.21, the responses of the current control methods to a 1 A step change of current reference (δi^*) are shown. These responses are in high correlation with those of simulations (Figure 4.13). When the DC current level (i_0) is 10 A, all control methods reveal the same dynamic characteristics as they have the same bandwidth ($\omega_{BW} = 2\pi 500 \text{ rad/s}$). The same figure shows that with a decrease in current, the reference tracking ability of CCR decreases. The dynamic performances of IDMBC, SCRd and K_p scheduling methods are retained and the same almost at all DC bias current levels.

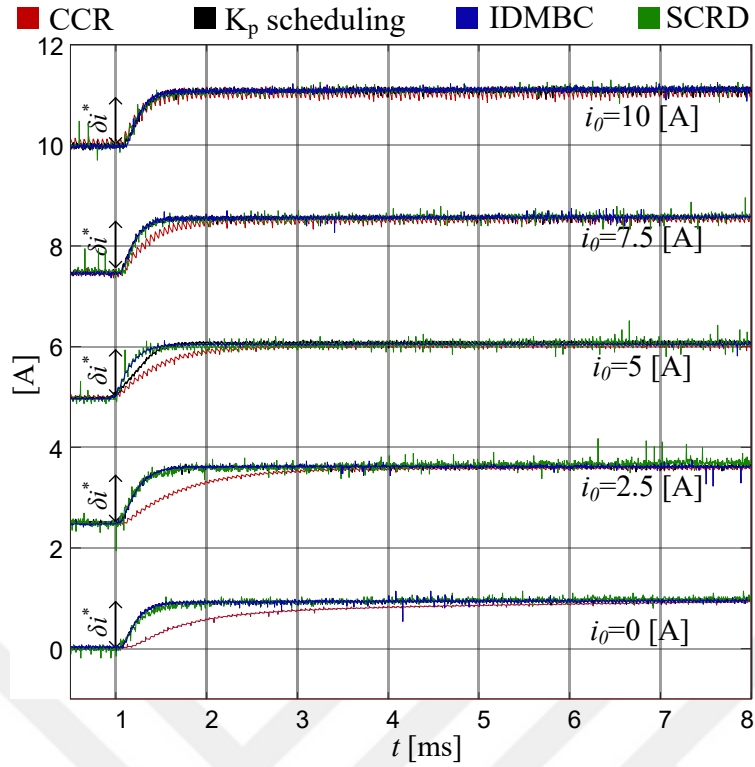


Figure 4.21: Experimental saturable inductor current and associated harmonic spectra of 1P FB VSC for $\omega_{BW} = 2\pi 500$ rad/s when VSC+inductor terminals are short-circuited under DC excitation.

4.7.3.2 Dynamic Response at AC Excitation

Figure 4.22 shows the dynamic response of all the methods for the grid-connected case. In harmony with the simulated results, K_p scheduling, IDMBC, and SCR D methods are superior to CCR for 0 to 2 A current command increase case. When compared with the simulation waveforms in 4.14, it can be concluded that the experimental AC dynamic response waveforms exhibit high consistency with the simulations.

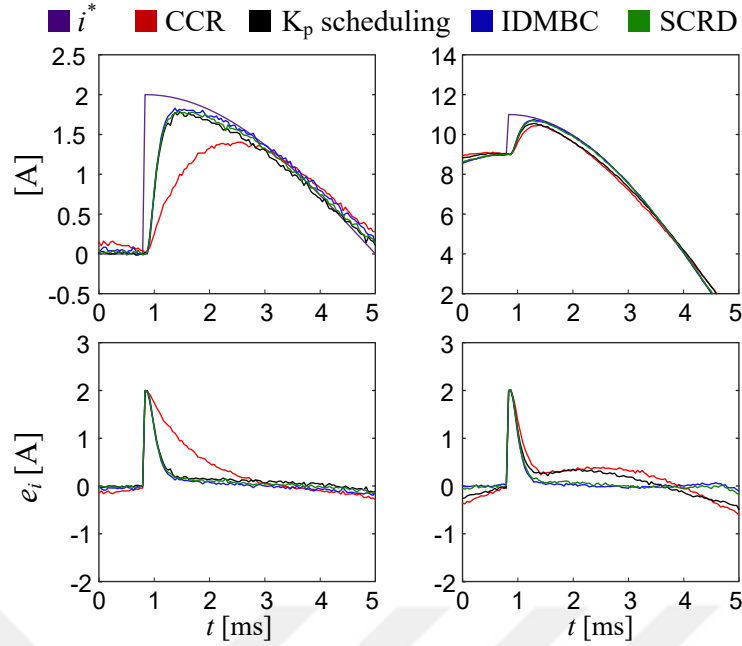


Figure 4.22: Experimental saturable inductor current and associated harmonic spectra of 1P FB VSC for $\omega_{BW} = 2\pi 500$ rad/s when VSC+inductor terminals are short-circuited under AC excitation.

4.7.4 Waveform Quality

4.7.4.1 Exaggeratedly Low Bandwidth

For the short-circuited configuration (Figure 4.12(a)) ω_{BW} of $2\pi 100$ rad/s experiments are conducted for the three methods and the results are shown in Figure 4.23. Having the same parameters, simulation and experimental results are found in high correlation. The inductor current clearly deviates from the sinusoidal reference for the cases of CCR and K_p scheduling methods and conversely, the current quality is significantly improved with IDMBC and SCRD method as shown in Figure 4.23. With the use of the proposed methods, the THD_i is significantly reduced. Additionally, the harmonic spectrum in the same figure shows that with the employment of the SCRD method the low-frequency harmonic content is considerably cleared.

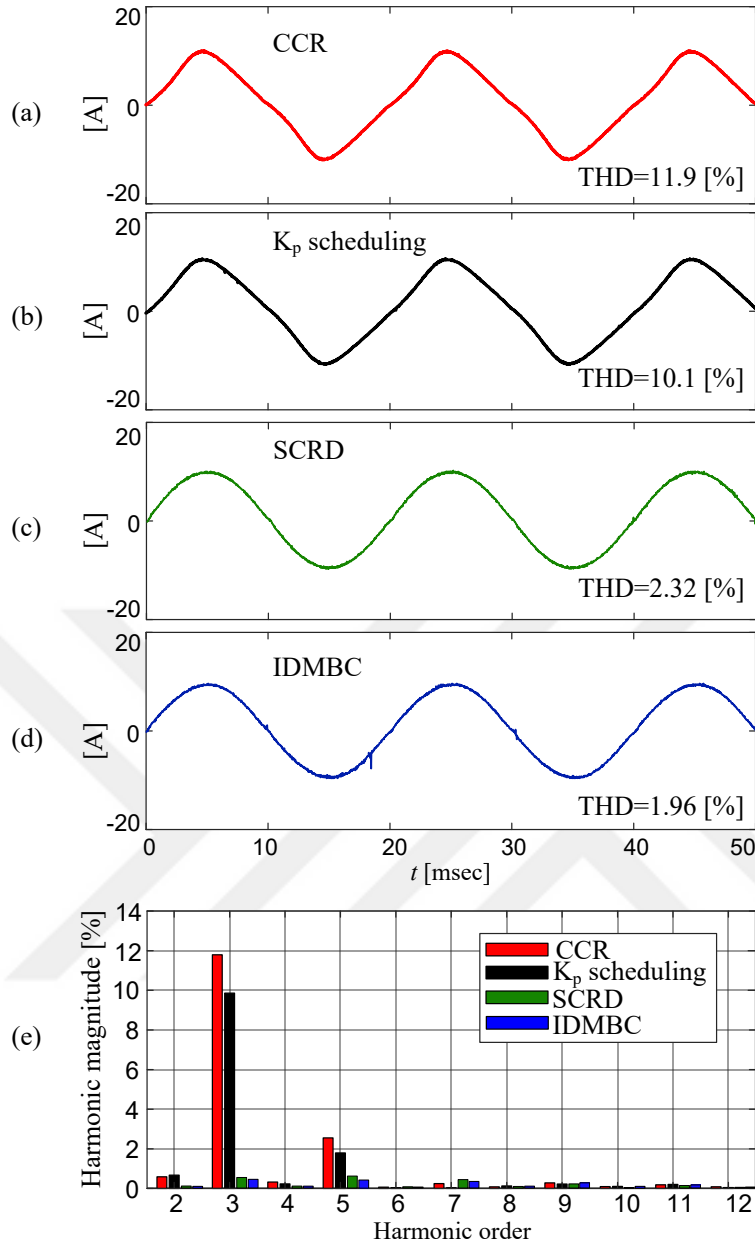


Figure 4.23: Experimental saturable inductor current and associated harmonic spectra of 1P FB VSC for $\omega_{BW} = 2\pi 100$ rad/s when VSC+inductor terminals are short-circuited.

4.7.4.2 Practical Bandwidth

Experiments for the grid-connected system are performed with $\omega_{BW} = 2\pi 500$ rad/s, as simulated. Figure 4.24 illustrates the measured grid voltage, grid currents, and

associated harmonic spectrum. Note that the measured grid voltage is the same as used in the simulations (the simulation voltage waveform was generated based on the measured voltage in order to provide identical conditions for comparison). When compared to simulations, the THD_i of grid currents is slightly higher in the experiments, mostly due to the noise and resolution limitations of current measurement and signal conditioning circuits and inverter nonidealities (although partially compensated via decoupling). Among the methods, the IDMBC and SCR D has the lowest THD_i values (3.43 % and 3.77 % respectively) and the closest method is the K_p scheduling having a THD_i of 4.88 %. Considering this and the harmonic spectrum (especially the 3rd harmonic) of the grid-currents of the methods in Figure 4.24, it can be concluded that IDMBC and SCR D methods are superior to CCR and K_p scheduling methods. On the other hand, it is also possible to further improve the waveform quality by decreasing the active damping of the system, which is elaborated in the next.

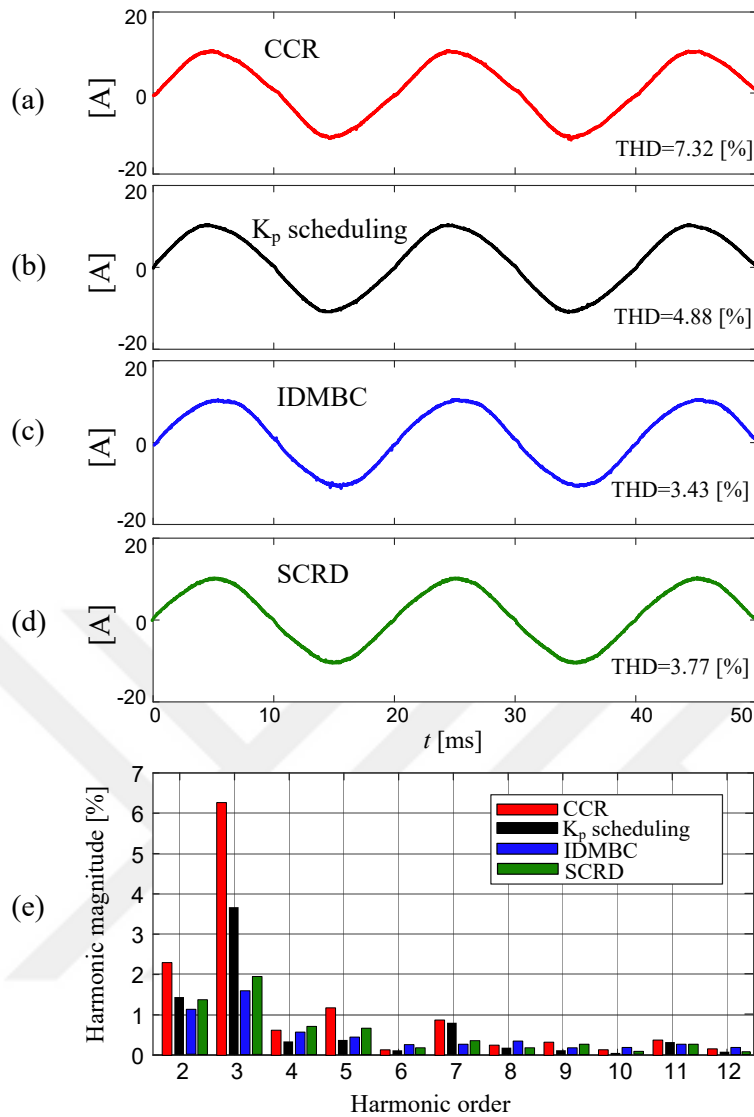


Figure 4.24: Experimental saturable inductor current and associated harmonic spectra of 1P grid-connected FB VSC for $\omega_{BW} = 2\pi 500$ rad/s.

4.7.5 On the Effect of Active Damping

The use of active damping in IDMBC and SCR D methods is to improve the system stability by incorporating an artificial resistor to the control system. Although its existence in the control system does not affect the closed-loop bandwidth, overshoot in the dynamic response is lessened. In this section, the effects of the incorporation of active damping in IDMBC and SCR D methods on the waveform quality is discussed.

In Figure 4.25, the frequency responses of CCR, K_p scheduling, IDMBC, and SCRDM methods are illustrated for the condition that without active damping and minimum system inductance. (Actually, CCR and K_p scheduling methods do not have any active damping configuration as they have already system resistance as a damper.) The frequency responses of the methods for the minimum inductance case were the same when the AD resistance was equal to the actual plant resistance. When AD resistance is set to zero (i.e. when there is no AD), the frequency response of IDMBC and SCRDM methods change duly. When compared to CCR and K_p scheduling referring Figure 4.25, it is seen that the low-frequency gain of the open-loop system is increased in IDMBC and SCRDM methods. Besides, the phase margins of these methods are slightly decreased (from 90 degrees to 75 degrees, but still sufficient for stable operation). Such an increase in the low-frequency band will normally increase the command tracking behaviour at low frequencies. Similarly, the disturbance rejection characteristics of the proposed IDMBC and SCRDM methods are preserved as shown in Figure 4.26. Therefore, a further improvement in the waveform quality is expected in IDMBC and SCRDM methods when the active damping is reduced.

In order to observe the effect of the reduction of the damping, experiments on $2\pi 100$ rad/s VSC+inductor terminals short circuited configuration (Figure 4.12(a)) and $2\pi 100$ rad/s grid-connected configuration (Figure 4.12(b)) are conducted. When compared to their actively damped counterparts in Figure 4.23 and Figure 4.24, the improvement in the waveform quality of the IDMBC and SCRDM methods can be observed due to the low frequency gain improvement in the frequency responses.

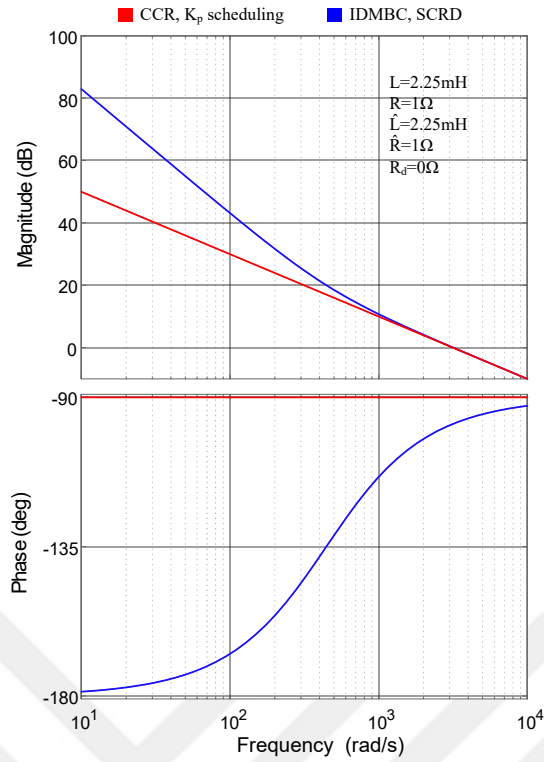


Figure 4.25: Frequency responses of CCR, K_p scheduling, IDMBC, and SCRD methods without active damping.

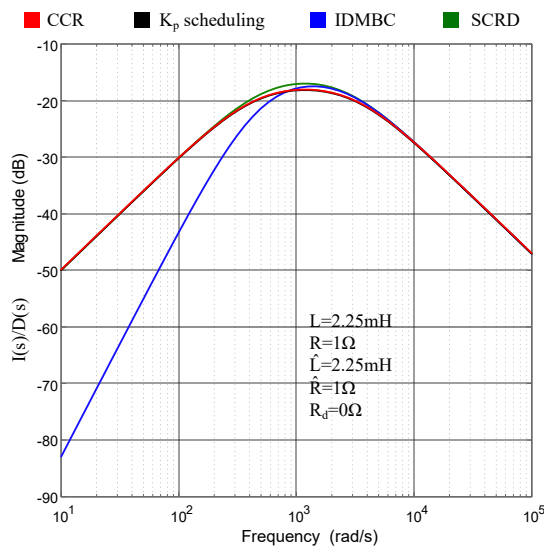


Figure 4.26: Disturbance rejection characteristics of CCR, K_p scheduling, IDMBC, and SCRD methods without active damping.

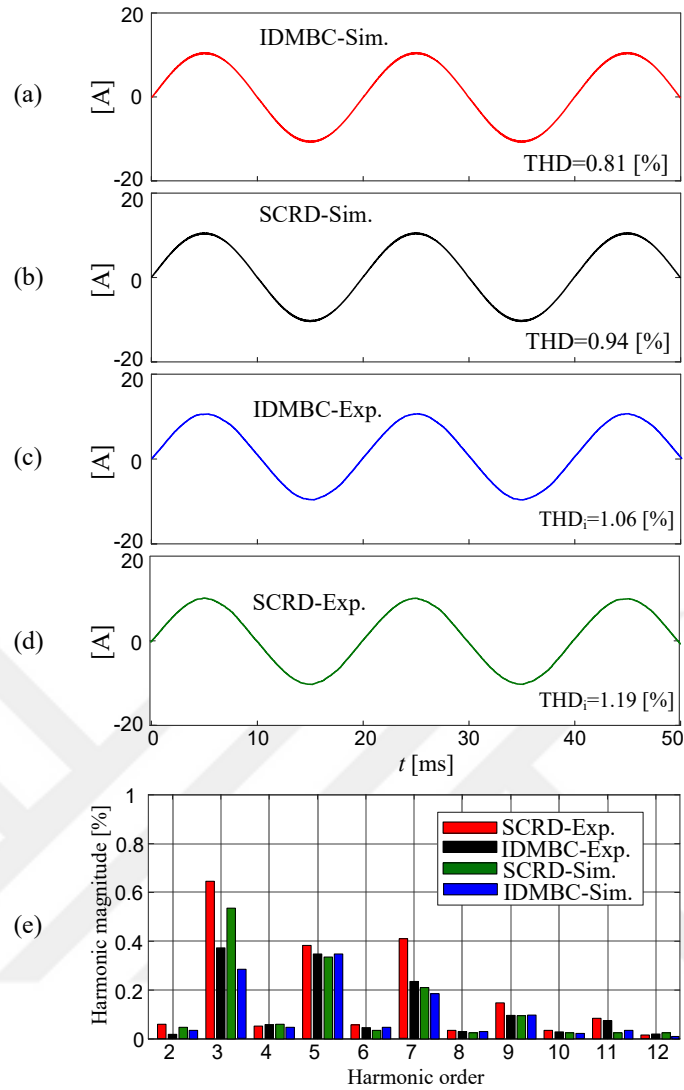


Figure 4.27: Simulation and experimental saturable inductor current waveforms and associated harmonic spectra of 1P FB VSC for $\omega_{BW} = 2\pi 100$ rad/s when VSC+inductor terminals are short-circuited. (a) Simulated IDMBC method. (b) Simulated SCR method. (c) Experimental IDMBC method. (d) Experimental SCR method. (e) Associated harmonic spectra.

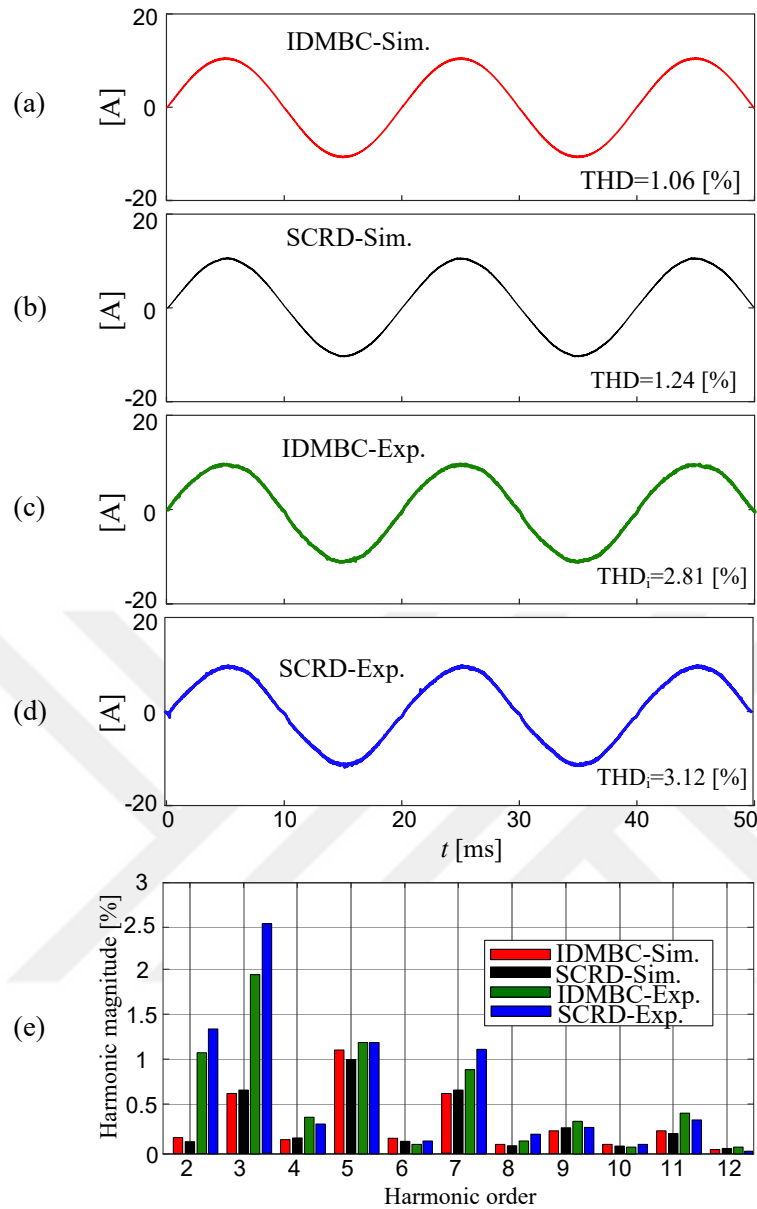


Figure 4.28: Simulation and experimental saturable inductor current waveforms and associated harmonic spectra of 1P FB VSC for $\omega_{BW} = 2\pi 500$ rad/s when VSC+inductor terminals are short-circuited. (a) Simulated IDMBC method. (b) Simulated SCRD method. (c) Experimental IDMBC method. (d) Experimental SCRD method. (e) Associated harmonic spectra.

4.7.6 Performance Assessment of the Methods

Throughout the chapter 4, it is shown by simulation results and experiments that the proposed IDMBC and SCRD methods are superior to CCR and K_p scheduling methods by means of dynamic response, waveform quality, and disturbance characteristics. Although it is easy to infer that the dynamic response performance is linearly proportional to the system bandwidth, the relation of the waveform quality is not very obvious. Therefore, the THD_i values of CCR, K_p scheduling, IDMBC, and SCRD methods are gathered for increasing design bandwidth (up to 2 kHz) experimentally. In Figure 4.29, these data are plotted. As expected, the waveform quality is improved always for all methods as the design bandwidth is increased. However, for a specific BW_{max} value, the proposed methods always exhibit better performance than the CCR and K_p scheduling methods. It is also observed that when AD is not incorporated better waveform quality is obtained.

It is remarkable that between the proposed methods, IDMBC method exhibit slightly better waveform quality characteristics than the proposed SCRD method for the same controller and plant parameters. This is because even though these two methods have the same frequency response characteristics, they have distinct disturbance rejection attributes. The IDMBC method exhibit better disturbance rejection characteristics than SCRD method as discussed in section 4.4.2. Consequently, IDMBC method has lower THD_i values than SCRD method under the same conditions. In Table 4.4, the overall performance attributes of the methods are summarized.

The measured energy conversion efficiency of the VSC for CCR at rated operation is 96.8 % and the inductor maximum temperature is 70 °C wherein the ambient temperature is 25 °C. For the proposed IDMBC and SCRD methods, the efficiency characteristics are very similar and the efficiency is 97.2 % and the maximum inductor temperature is 67 °C. For K_p scheduling similar results that of SCRD is obtained. The improvement with the SCRD is due to reduced low-frequency harmonic content in the current. The grid-connected VSC is operated for several hours for the proposed method without observing a considerable change in the waveform quality. This is due to the superior temperature stability of the sendust core [77] and parameter insensitivity of the method.

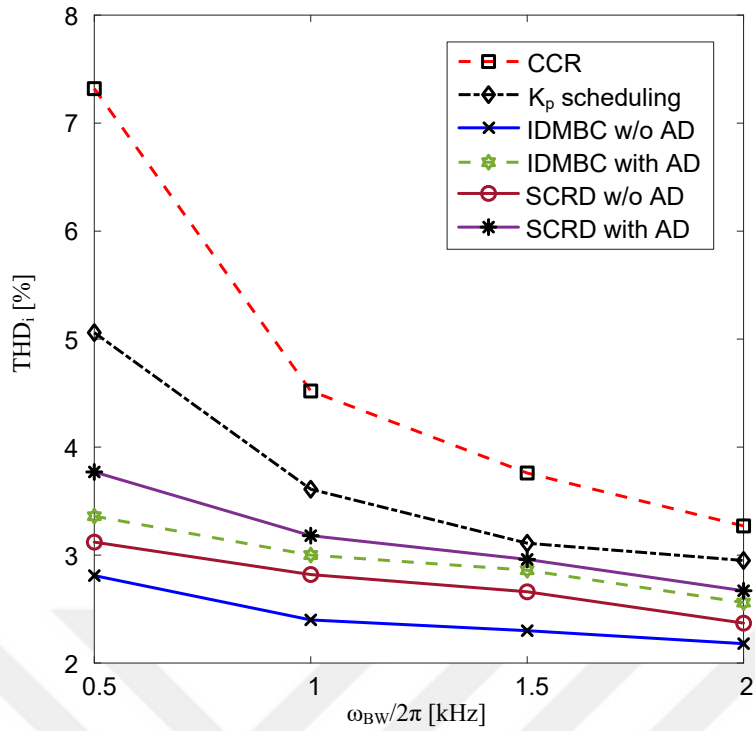


Figure 4.29: Experimental THD_i vs. current control bandwidth of current controllers for 1P VSCs.

Table 4.4: Performance Assessment of Investigated 1P Current Control Methods

Indicator/Method	CCR	K _p Scheduling	IDMBC	SCR D
Dynamic Response	-	++	++	++
Waveform Quality	-	+	+++	+++
Disturbance Rejection	-	+	+++	++

4.7.7 Summary

In this chapter, IDMBC and SCR D methods are presented which were published by the author and his thesis advisor in [78] and [79] respectively. The frequency response and disturbance characteristics of these proposed methods are investigated analytically together with the CCR and the K_p scheduling methods. After that, plant parameter characterization methods are provided as the proposed methods and the K_p

scheduling methods require the dynamic system L-R parameters. The performance improvement with the proposed methods is shown in comparison with the CCR and K_p scheduling methods by means of simulations firstly. A simulation-based parameter mismatch study is also conducted for the IDMBC and SCR D methods showing their robustness to erroneous estimation of the parameters. After that, experimental results indicating the dynamic response and waveform quality performances of the methods with and without active damping cases are presented. It is shown that proposed IDMBC and SCR D methods show high performance over CCR and K_p scheduling methods. Further and final, among the proposed methods it is shown that IDMBC method exhibit better waveform quality characteristics than the SCR D method due to better disturbance rejection characteristics.





CHAPTER 5

INDUCTOR SATURATION COMPENSATION IN THREE-PHASE THREE-WIRE VOLTAGE SOURCE CONVERTERS

5.1 Introduction

In chapter 4, it was shown by simulations and experiments that the proposed IDMBC and SCRD methods overcome the bandwidth shrinkage and the inductor saturation problems in single-phase VSCs employing saturable inductors. Among these, IDMBC method is found slightly better than SCRD method due to its better disturbance rejection characteristics. Hence, for 3P3W systems, IDMBC method is adapted. However, the implementation is not as straightforward as the balanced three-phase approach is not valid when saturable inductors are utilized. Thus, the classical vector control method (or equivalently called CCR3 method within the context of this thesis) can not be used directly. This issue is exposed in this chapter firstly. To be eligible to use of the classical vector control, which is known to be successful in the control of linear balanced 3P3W systems, two-phase model of 3P3W system is established. This model is used to linearize the VSC system in the large by employing the inverse dynamic model of the system. After linearization, the integral compensator is incorporated similar to the single-phase counterpart of IDMBC method. Hence, a linear and symmetrical 3P3W system is attained. Having such a linear system, classical vector control can be utilized with improved performance attributes. After the presentation of the IDMBC method for 3P3W systems, frequency response and disturbance characteristics are investigated analytically. After that, the dynamic response, parameter mismatch, and waveform quality studies via simulations prove the performance improvement with the use of IDMBC method. Finally, experimental results are provided also to show the advantageousness of the proposed IDMBC

method over conventional vector controlled 3P3W VSC system by means of dynamic response and waveform quality.

5.2 The Inconsistency of Symmetrical Linear Three-Phase System Approach in 3P3W VSCs Employing Saturable Inductors

Conventional current controllers are widely employed in almost every area where VSCs exist, independent of the excitation whether it is AC or DC. When the system to be controlled is linear, the controller gains can be calculated such that dynamic response can be predetermined and the waveform quality is satisfactory. Besides, the implementation is quite simple and effective. Therefore, it is very reasonable to utilize these controllers in such a wide-spread manner with linear inductors. On the other hand, in chapter 3, it is shown for both 1P controlled and 3P3W VSC systems that bandwidth shrinkage and waveform quality problems arise with conventional current controllers when saturable inductors are employed. In order to solve these issues, the inconsistency of symmetrical linear three-phase system approach in 3P3W VSCs with saturable inductors is shown in the first place.

From elementary circuit theory lectures to power system analysis, the generic 3P3W system shown in Figure 5.1(a) is analyzed based on the assumption that the voltage potential between the nodes $o - n$ is always zero ($v_{o-n} = 0$), hence a connection between these two nodes (shown in Figure 5.1(a) with dashed line) can be realized without any change in the physical states (voltages and currents) of the lumped elements of the circuit. Such a connection enables one to analyze the 3P3W circuit as a reduced form to single-phase as shown in Figure 5.1(b), in terms of one of the phases of the system, say phase-a. Then the other variables belonging to other phases can be found by adding phase shifts of $2\pi/3$ and $4\pi/3$ to the corresponding states.

While the 3P3W circuit is symmetrical and linear, this approach is adapted well to the current regulation in 3P3W VSC systems. The voltage sources v_a , v_b , and v_c become the control input in VSC control system and the overall system is represented as

$$\begin{aligned}
v_a &= L \frac{di_a}{dt} + Ri_a \\
v_b &= L \frac{di_b}{dt} + Ri_b \\
v_c &= L \frac{di_c}{dt} + Ri_c.
\end{aligned}
\tag{5.1}$$

The overall conventional current regulation process is elaborated in chapter 3 section 3.2.1.2. However, when saturable inductors are employed, the nodes $o - n$ are no equipotential strictly for all time even if balanced pure sinusoidal voltages are applied. That is $v_{o-n} \neq 0$ for most of the time. Therefore, the nodal points $o - n$ can not be connected. This is the fundamental obstacle to the assumption of symmetrical linear 3P3W circuit approach of conventional current control methods. The next section is devoted to exact modelling of 3P3W VSC system to establish a basis for the development of a high-performance current controller when saturable inductors are employed.

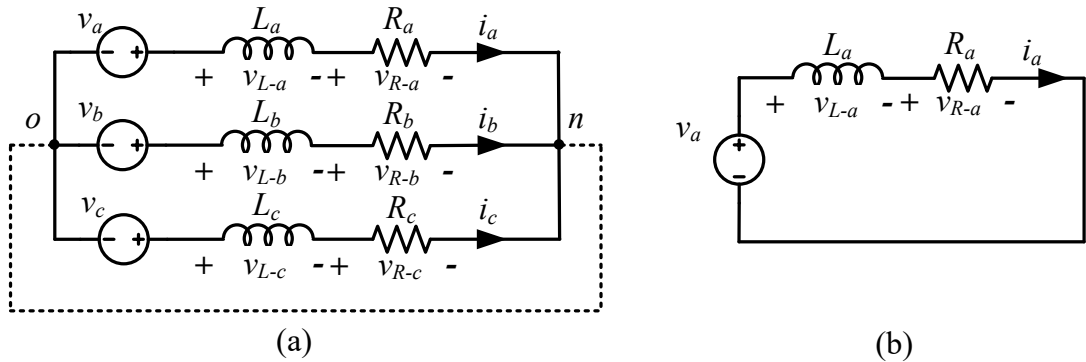


Figure 5.1: Generic circuits for analyzing 3P3W systems. (a) Generic 3P3W circuit. (b) The single-phase representation when the 3P3W system is balanced and linear.

5.3 Two Phase Modelling of 3P3W VSC Systems

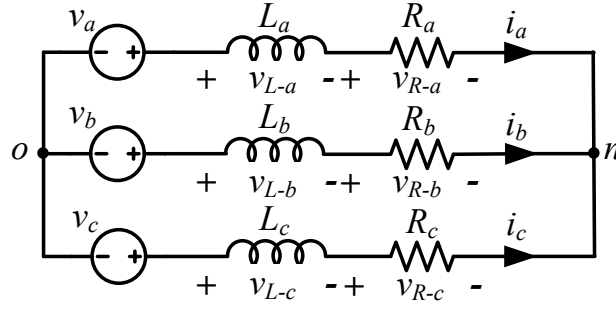


Figure 5.2: Three-phase three-wire R-L-E circuit representing the VSC current regulation system.

Figure 5.2 shows the equivalent 3P3W VSC system for current regulation wherein v_a , v_b , and v_c are the input control voltages provided by the VSC, namely pole voltages. This 3P3W system can be exactly described by the mesh equations

$$\begin{aligned} v_{ab} &= L_a \frac{di_a}{dt} - L_b \frac{di_b}{dt} + R_a i_a - R_b i_b \\ v_{bc} &= L_b \frac{di_b}{dt} - L_c \frac{di_c}{dt} + R_b i_b - R_c i_c \end{aligned} \quad (5.2)$$

where $v_{ab} = v_a - v_b$, $v_{bc} = v_b - v_c$. Utilizing that the sum of the phase currents is zero, $i_a + i_b + i_c = 0$, equation (5.2) can be rewritten as

$$\begin{aligned} v_{ab} &= L_a \frac{di_a}{dt} - L_b \frac{di_b}{dt} + R_a i_a - R_b i_b \\ v_{bc} &= (L_b + L_c) \frac{di_b}{dt} + L_c \frac{di_a}{dt} + (R_b + R_c) i_b + R_c i_a. \end{aligned} \quad (5.3)$$

The equation (5.3) can be written in matrix form as

$$\mathbf{v}_\sigma = \mathbf{L}_\sigma \frac{d}{dt} \mathbf{i}_\sigma + \mathbf{R}_\sigma \mathbf{i}_\sigma \quad (5.4)$$

where $\mathbf{v}_\sigma = \begin{bmatrix} v_{ab} \\ v_{bc} \end{bmatrix}$, $\mathbf{i}_\sigma = \begin{bmatrix} i_a \\ i_b \end{bmatrix}$, $\mathbf{L}_\sigma = \begin{bmatrix} L_a & -L_b \\ L_c & L_b + L_c \end{bmatrix}$, and $\mathbf{R}_\sigma = \begin{bmatrix} R_a & -R_b \\ R_c & R_b + R_c \end{bmatrix}$.

Figure 5.3 illustrates the exact representation of 3P3W nonlinear physical system in terms of control blocks with vector signals. In the next section, this model will be

utilized to linearize the 3P3W VSC system.

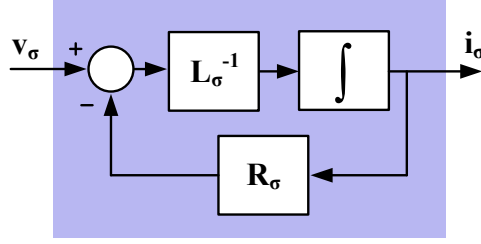


Figure 5.3: Three-phase three-wire system vector block diagram.

5.4 Linearization of 3P3W VSC System in the Large via Inverse Dynamic Model

Having obtained the exact system model for 3P3W systems, the inverse dynamic model of the system can be obtained in a similar manner to 1P controlled VSC systems. The load voltage and known disturbances are assumed decoupled as in the case of 1P controlled VSC systems. IDM is developed to convert this nonlinear system to a linear system with unity-gain and zero-phase. In Figure 5.4(a) the nonlinear physical system and its IDM are shown in cascade. Since the system is nonlinear, in this representation, the order of operators is important (unlike the linear systems). With the nonlinear time-domain structure, one can write the equivalence of nonlinear state equations of the cascaded system as

$$\mathbf{L}_\sigma \frac{d}{dt} \mathbf{i}_\sigma + \mathbf{R}_\sigma \mathbf{i}_\sigma = \hat{\mathbf{L}}_\sigma \frac{d}{dt} \mathbf{u}_\sigma + \hat{\mathbf{R}}_\sigma \mathbf{u}_\sigma \quad (5.5)$$

where $\hat{\mathbf{L}}_\sigma$ and $\hat{\mathbf{R}}_\sigma$ are estimated values of \mathbf{L}_σ and \mathbf{R}_σ respectively. When these estimated terms are equal to the actual parameters and the initial states are identical ($\mathbf{i}_\sigma(0) = \mathbf{u}_\sigma(0)$), the equivalence $\mathbf{i}_\sigma(t) = \mathbf{u}_\sigma(t)$ is obtained for $t > 0$. Therefore, the resulting system from the cascade of these two nonlinear systems can be considered as a linear, unity-gain, zero-phase system as shown in Figure 5.4(b).

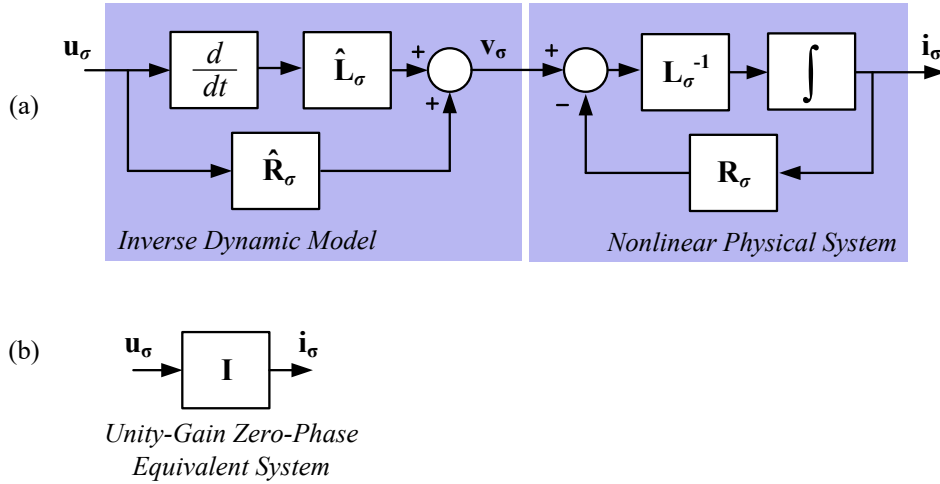


Figure 5.4: Three-phase three-wire system vector block diagram.

5.5 Incorporation of Integral Compensator

The unity-gain zero-phase equivalent system obtained in previous section and shown in Figure 5.4 by making use of IDM has infinite bandwidth. However, the physical realization will exhibit strong deficiencies such as high frequency oscillations and/or tracking error due to physical bandwidth limitations and lack of feedback respectively. Moreover, the derivation in the IDM may amplify high-frequency noise. For these reasons, an integral compensator with a coefficient of $1/L_{\min}$ is cascaded to the IDM as shown in Figure 5.5(a). The integration term can be spread to IDM and cancel the differentiation block as shown in Figure 5.5(b), exterminating the noise amplification problem. Further, the compensated system behaves as a two-input two-output decoupled one as shown in Figure 5.5(c).

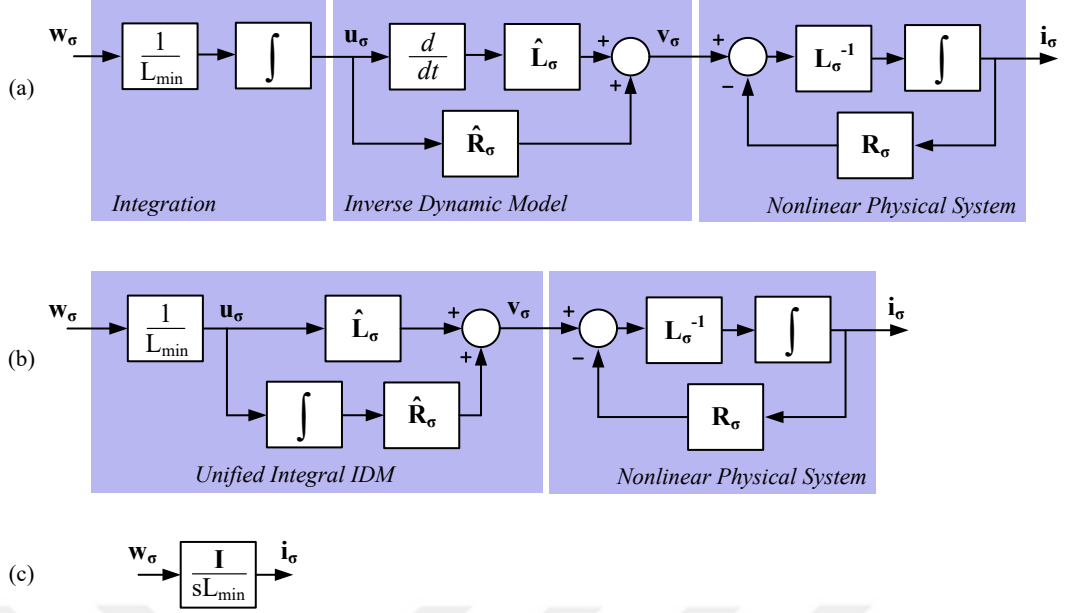


Figure 5.5: Three-phase three-wire system vector block diagram.

5.6 Current Control of 3P3W VSC System with IDMBBC

The linearized overall system shown in Figure 5.5(c) is nothing but two independent phases having the state equation

$$\begin{bmatrix} w_a \\ w_b \end{bmatrix} = \begin{bmatrix} L_{min} & 0 \\ 0 & L_{min} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \end{bmatrix} \quad (5.6)$$

where i_a and i_b are the actual phase currents of the physical system and w_a and w_b are the fictitious input voltages. This system represents obviously two phases of a hypothetical balanced 3P3W VSC circuit such as described by (5.1) which is used in the development of conventional dq-frame current control. Making use of this view on the linearized system, conventional dq-frame current control, or other types of linear controllers can be employed.

In Figure 5.6, the overall closed-loop current control scheme is illustrated in which a conventional synchronous frame controller is employed. The implementation of the synchronous frame controller is shown in complex quantities, easing the illustration, whereas the implementation could have been scalar in the synchronous frame, or

stationary frame resonant type, each providing sufficiently small steady-state error at the fundamental frequency. The IDM based current control shown in the figure operates as follows. The measured current vector $\mathbf{i}_\sigma = [i_a \ i_b]^T$ is fed back to the synchronous frame conversion to its dq-frame space vector representation ($i_{dq} = i_d + ji_q$), wherein only the phase-a and phase-b quantities are sufficient for the conversion as the phase-c current can be derived from the phase-a and phase-b currents ($i_c = -i_a - i_b$). If the phase-c current is measured it can be used directly. The error between the dq-frame current command and the measured current ($e_{dq} = i_{dq}^* - i_{dq}$) is processed by the compensator G_c which usually a PI type. The feed-forward term ($j\omega_e L_{min} i_{dq}$) is added to decouple the cross-coupling of d-axis and q-axis yielding the dq-frame voltage output v_{dq} for the linearized system. This output is converted to stationary frame phase quantities via frame conversion. The output of the frame conversion is three phase quantities (w_a, w_b , and w_c). However, only two of these outputs $\mathbf{w}_\sigma = [w_a \ w_b]^T$ are utilized in the control architecture as the linearized plant is a two-input two-output decoupled one as described by (5.6). Such an approach functions quite well considering the argument that the system (5.6) can be expanded to that of linear, balanced, and decoupled system of equation (5.1) by inserting a third hypothetical equation relating to phase-c. However, the current of phase-c is strictly dependent on phase-a and phase-b currents, hence can not be controlled independently when phase-a and phase-b currents are controlled.

When \mathbf{w}_σ column vector is applied, the output of the unified IDM block becomes the column vector command $\mathbf{v}_\sigma^* = [v_{ab}^* \ v_{bc}^*]^T$ that is the input for the nonlinear physical system line-to-line voltages after the modulation process. However, the state-of-the-art 3P3W VSC technology is built on the independent modulation of each leg and accordingly, high-performance PWM techniques with zero-sequence injection have become wide-spread even if two-phase modulation is possible. Accordingly, the modulator block in Figure 5.6 converts the line-to-line output voltages to three-phase voltages.

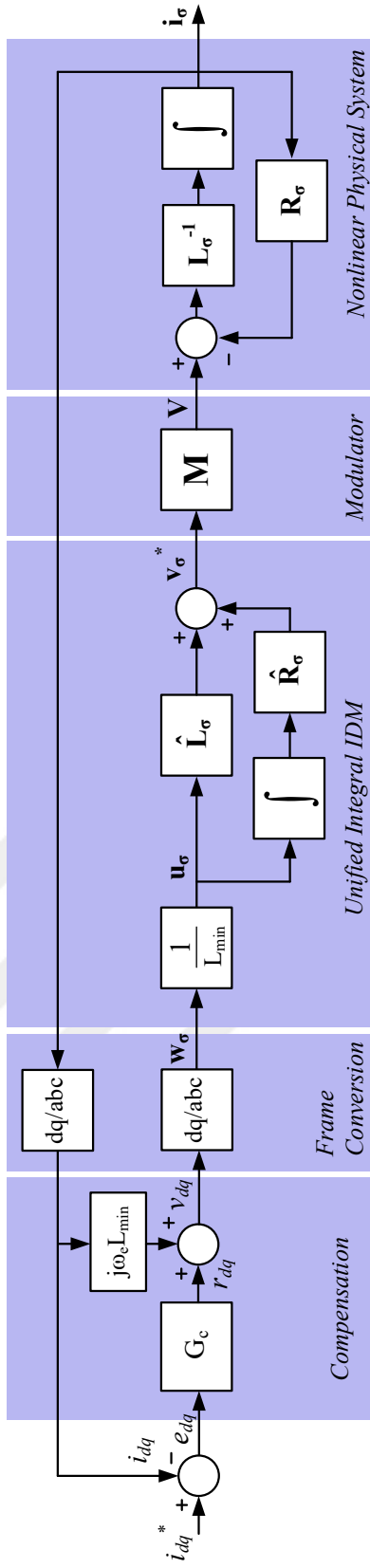


Figure 5.6: Three-phase three-wire nonlinear VSC system linearization and control in synchronous frame.

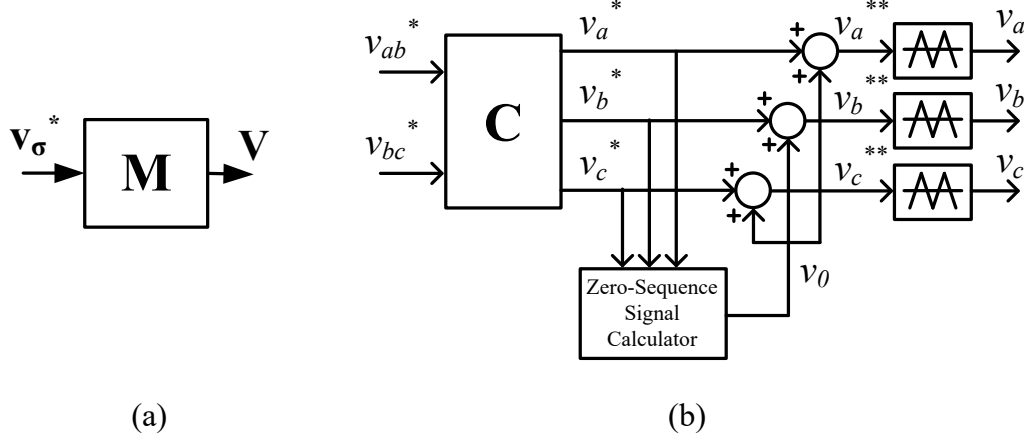


Figure 5.7: Three-phase three-wire system modulator block. (a) Column vector representation. (b) Scalar representation.

In Figure 5.10, the function of the modulator is explained. The Figure 5.10(a) shows the modulator block diagram in a vector input vector output manner. In Figure 5.10(b), the illustration of the modulator is made via scalars. Regarding 5.10(b), the line-to-line voltages provided by the unified integral IDM is converted to phase voltages (v_a^* , v_b^* , and v_c^*) via scalar multiplication by the transformation matrix C .

The matrix C can be deduced from the argument that the phase voltages can be derived from the line-to-line voltages as

$$\begin{aligned}
 v_{ab}^* + v_{ac}^* &= v_a^* - v_b^* + v_a^* - v_c^* = 3v_a^* \\
 v_{ba}^* + v_{bc}^* &= v_b^* - v_a^* + v_b^* - v_c^* = 3v_b^* \\
 v_{ca}^* + v_{cb}^* &= v_c^* - v_a^* + v_c^* - v_b^* = 3v_c^*
 \end{aligned} \tag{5.7}$$

where v_a^* , v_b^* , and v_c^* are the zero-sum phase voltage commands with respect to preferably to the midpoint of the dc-link and their sum includes no zero-sequence component for now, i.e. $v_a^* + v_b^* + v_c^* = 0$. Therefore the following relation can be obtained

$$\begin{aligned}
 v_a^* &= \frac{v_{ab}^* + v_{ac}^*}{3} \\
 v_b^* &= \frac{v_{ba}^* + v_{bc}^*}{3} \\
 v_c^* &= \frac{v_{ca}^* + v_{cb}^*}{3}.
 \end{aligned} \tag{5.8}$$

Rearranging (5.8) and noting that $v_{ab}^* = -v_{ab}^*$, $v_{bc}^* = -v_{cb}^*$, $v_{ca}^* = -v_{ac}^*$ and that $v_{ab}^* + v_{bc}^* + v_{ca}^* = 0$ one can obtain

$$\begin{bmatrix} v_a^* \\ v_b^* \\ v_c^* \end{bmatrix} = \mathbf{C} \begin{bmatrix} v_{ab}^* \\ v_{bc}^* \end{bmatrix} \quad (5.9)$$

$$\text{where } \mathbf{C} = \frac{1}{3} \begin{bmatrix} 2 & 1 \\ -1 & 1 \\ -1 & -2 \end{bmatrix}.$$

After obtaining phase command voltages with no zero-sequence component, zero-sequence voltage is injected in order to improve the overall performance of the VSC. It is worth to emphasize that even if the 3P3W VSC system is a nonlinear one the injection of zero-sequence voltage (v_0) will not create any zero-sequence current as there is no path for the zero-sequence current to flow. Therefore the zero-sequence voltage can be injected to the VSC phase voltages safely.

The generation of the voltage commands upto the triangle comparators (v_a^{**} , v_b^{**} , and v_c^{**}) can be summarized as

$$\begin{bmatrix} v_a^{**} \\ v_b^{**} \\ v_c^{**} \end{bmatrix} = v_0 + \mathbf{C} \begin{bmatrix} v_{ab}^* \\ v_{bc}^* \end{bmatrix}. \quad (5.10)$$

The injection of the zero-sequence voltage can be made among various PWM methods [16,17] depending on the performance criteria. Having obtained the zero-sequence signal injected voltage commands for the inverter legs, one can generate the pulse patterns and hence the VSC output voltage for each leg with respect to the midpoint of the dc-link (v_a , v_b , and v_c). Although these voltages are with respect to the midpoint of the dc-link, the 3P3W load sees line-to-line voltages, which are the same of the elements of \mathbf{v}_σ^* when imperfect decoupling of the disturbance sources and VSC nonlinearity is acceptably suppressed.

5.7 Incorporation of Active Damping

Active damping for the 3P3W VSC current control system in Figure 5.6 is implemented in stationary frame. The overall actively damped system is shown in Figure 5.8(a). When the estimated system parameters are sufficiently correct, the unified integral IDM and the nonlinear physical system yields a constant inductance two input two output system, with an inductance of L_{min} in a decoupled manner as discussed in section 5.5. Then, in dq-frame employing complex variables, the overall system becomes to the one shown in Figure 5.8(b). Furthermore, in Figure 5.8(c), the resultant equivalent system is illustrated after cross-coupling decoupling is achieved. This system is nothing but the same of the case in single-phase actively damped linearized systems except that the state variables are complex and DC quantities. Thus, the closed-loop current control system can be represented by the linear relation in s-domain

$$\frac{I_{dq}(s)}{I_{dq}^*(s)} = \frac{G_c(s)}{G_c(s) + sL_{min} + R_d} \quad (5.11)$$

where $I_{dq}(s)$ and I_{dq}^* denote the s-domain values of synchronous frame complex valued current and current command.

The implementation of the compensator G_c is the same of single-phase systems, except for the need a resonant controller component depending on the frame that the compensation takes place. For a synchronous frame rotating at ω_e typically a PI compensator is employed. The coefficients of the PI controller is selected in a similar manner to that of single-phase VSC systems. To repeat, $K_p = \omega_{BW} \times L_{min}$, $K_i = \omega_{BW} \times R_d$. Accordingly, the open-loop system transfer function becomes a first-order one of ω_{BW}/s which has a bandwidth of ω_{BW} . The value of ω_{BW} can be selected freely depending on the design constraints, such as waveform quality, dynamic response requirement, and bandwidth upper limit.

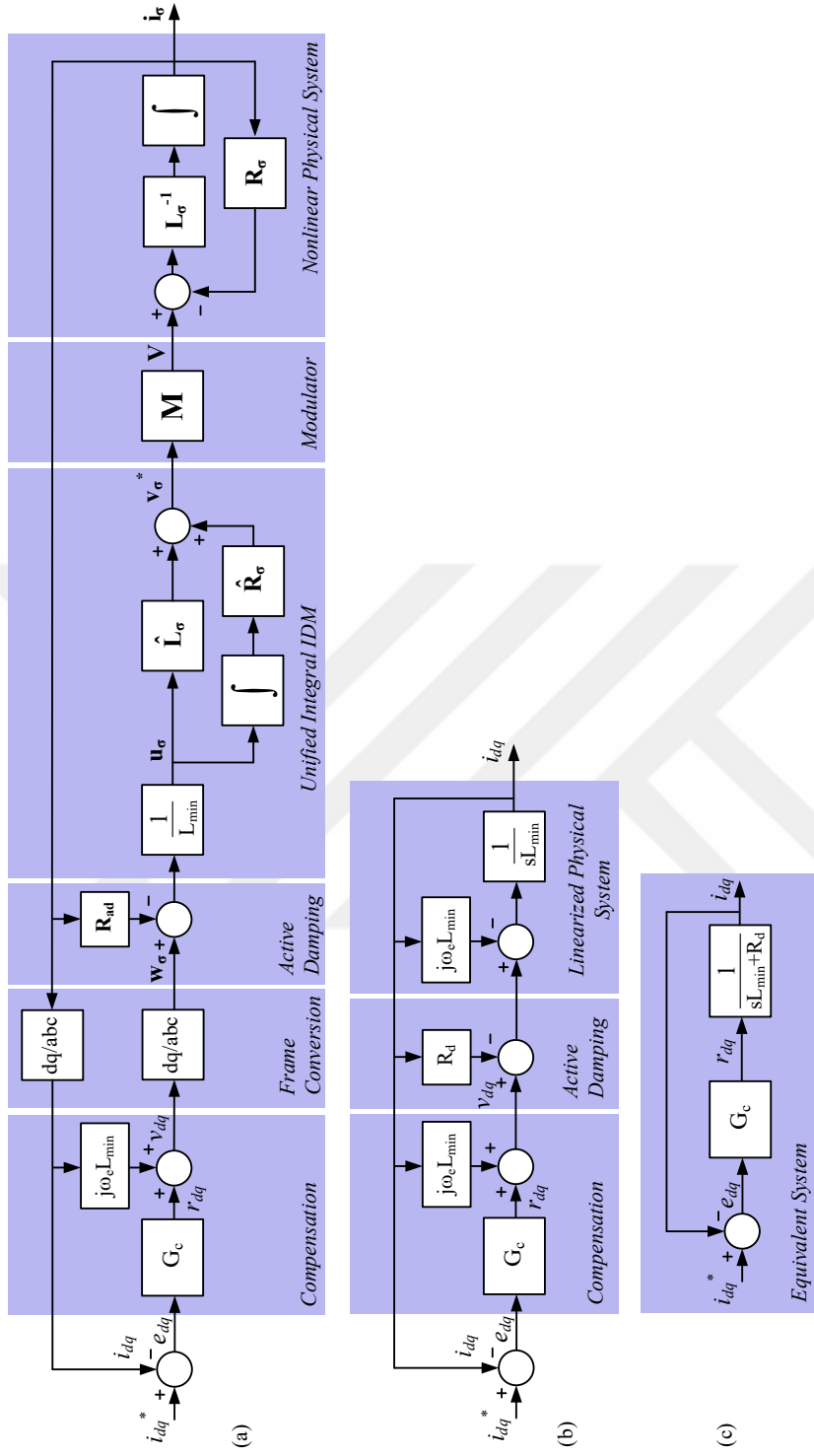


Figure 5.8: Incorporation of active damping in IDM based 3P3W system control. (a) The overall implementation of IDMB method with active damping in dq-frame. (b) The reduced system in dq-frame when the unified IDM and the nonlinear physical system are merged with correct estimated parameters. (c) The equivalent system of the reduced system when cross-coupling decoupling is performed.

5.8 Frequency Response Characteristics of CCR3 and IDMBC Method in 3P3W VSC Systems

In this section, the frequency response characteristics of the CCR3 and IDMBC methods are elaborated. The investigation consists of command to output and disturbance to output characterizations. The investigation is conducted in dq-frame for command to output characteristics. This is to observe the dynamic response characteristics of the dq-frame currents to the dq-frame current commands. In the part of the disturbance to output frequency response investigation, the analyses went on the stationary frame as the physical disturbance source and the output currents are both in the stationary frame. Similar to the single-phase analyses, the VSC system is assumed to operate at a steady-state where the inductance variation is dominated by the fundamental frequency large-signal and small magnitude command/disturbance applied, hence the responses of the controllers are analyzed accordingly.

In Figure 5.9, the equivalent control block diagrams for CCR3 and IDMBC methods are illustrated. In the figure, \mathbf{L}_σ^{-1} denotes the inverse of the two-phase representation of instantaneous inductance matrix \mathbf{L}_σ which is as defined in (5.4). Similarly, \mathbf{R}_σ denotes two-phase representation of instantaneous resistances of the nonlinear physical VSC system. The $\hat{\mathbf{L}}_\sigma$ and $\hat{\mathbf{R}}_\sigma$ denote the estimated values of \mathbf{L}_σ and \mathbf{R}_σ respectively. In the figure, disturbance and its compensation are also illustrated. The disturbance effects are represented as a size two vector in line to line manner (\mathbf{v}_D) here whereas the decoupling of these disturbances is performed in line quantities as in the case of 1P controlled VSCs (as described in chapter 3). In 3P3W VSCs, the disturbance voltage is mainly composed of the load voltage (or grid voltage) and the VSC generated disturbance voltage which can be described by

$$\mathbf{v}_D = \mathbf{v}_{g-\sigma} + \mathbf{v}_{id-\sigma} \quad (5.12)$$

where $\mathbf{v}_{g-\sigma}$ is load voltage and $\mathbf{v}_{id-\sigma}$ is inverter generated disturbance due to dead-time, measurement errors, and switch nonidealities represented in line-to-line manner, i.e. $\mathbf{v}_{g-\sigma} = [(v_{an} - v_{bn}) (v_{bn} - v_{cn})]^T$ where the phase to neutral point load voltages are as shown in Figure 3.2. The other component of the disturbance voltage can be expressed in a similar manner as $\mathbf{v}_{id-\sigma} = [(v_{id-a} - v_{id-b}) (v_{id-b} - v_{id-c})]^T$ wherein

v_{id-a} , v_{id-b} , and v_{id-c} denote the inverter generated disturbance voltage of leg a, b, and c respectively. The same convention is valid for the estimated disturbance voltage $\hat{\mathbf{v}}_{\mathbf{D}}$. Furthermore, the disturbance signal can be represented as a voltage column vector as

$$\mathbf{d}_{\sigma} = \begin{bmatrix} d_{ab} \\ d_{bc} \end{bmatrix} \quad (5.13)$$

where d_{ab} and d_{bc} are line-to-line representations of disturbance signals ($\mathbf{d}_{\sigma} = \hat{\mathbf{v}}_{\mathbf{D}} - \mathbf{v}_{\mathbf{D}}$).

In Figure 5.9 the compensator structure is illustrated in complex vector structure for the sake of reducing illustration complexity. However, the implementation of this space vector controller is equivalent to the scalar implementation which is described in section 3.2.1.2.

In Figure 5.10, the generic representation of current-controlled closed-loop VSC system is illustrated. In this representation, the dq-frame variables are transformed into stationary frame. For CCR method, these transformations can be simply described as

$$\begin{aligned} \mathbf{v}_{\mathbf{dq}} &= \mathbf{H}(\theta)^{-1} \mathbf{v}_{\sigma} \\ \mathbf{i}_{\mathbf{dq}} &= \mathbf{T}(\theta)^{-1} \mathbf{i}_{\sigma} \end{aligned} \quad (5.14)$$

wherein

$$\mathbf{T}(\theta) = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \cos(\theta - 2\pi/3) & -\sin(\theta - 2\pi/3) \end{bmatrix} \text{ and } \mathbf{H}(\theta) = \mathbf{T}(\theta) - \mathbf{T}(\theta - 2\pi/3).$$

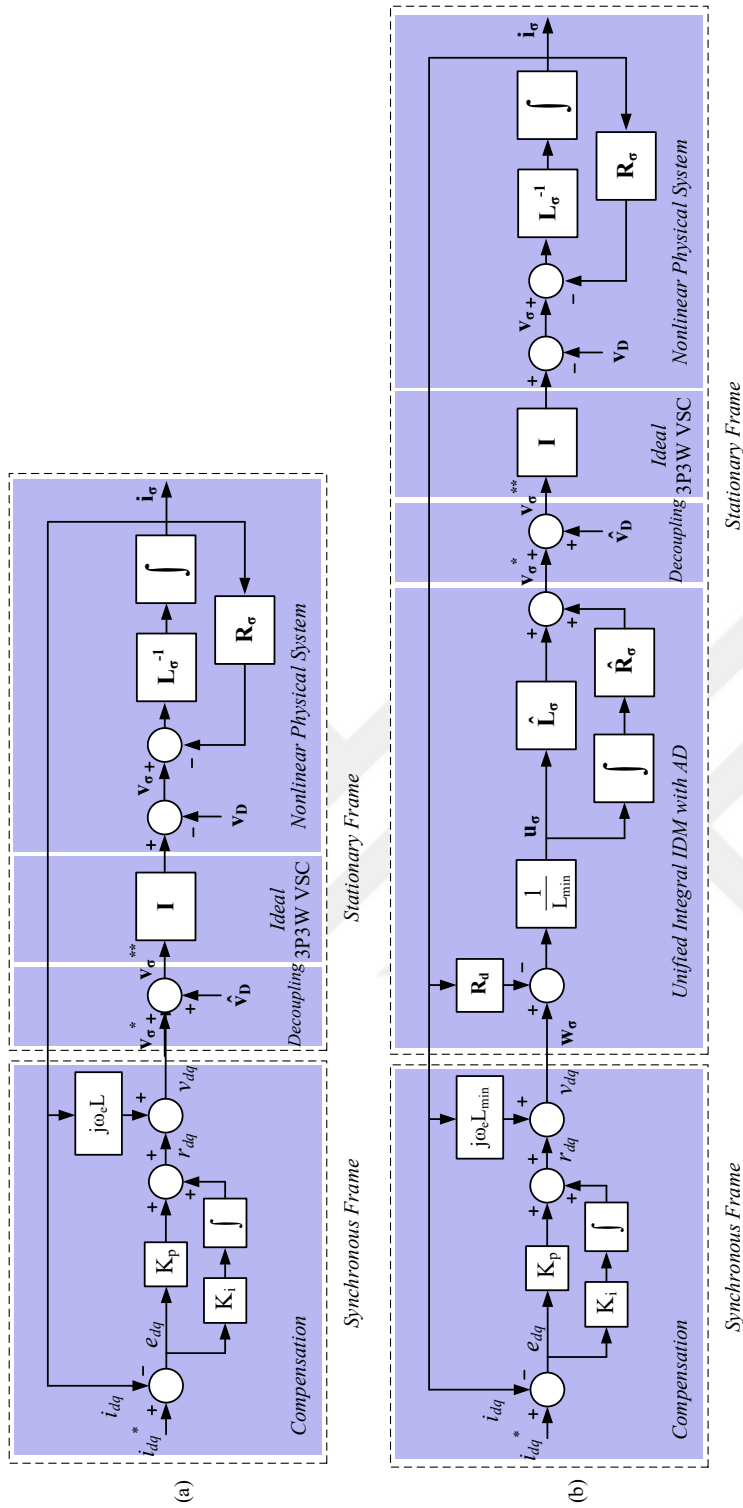


Figure 5.9: Control block diagram representation involving of 3P3W VSC system for CCR3 and IDMBC methods for frequency response analyses. (a) Equivalent closed-loop control block diagram pertaining CCR3 method. (b) Equivalent closed-loop control block diagram pertaining IDMBC method for 3P3W VSC systems.

For IDMBC method the transformation for converting variables into stationary frame can be described by

$$\begin{aligned} \mathbf{v}_{dq} &= \mathbf{T}(\theta)^{-1} \mathbf{w}_\sigma \\ \mathbf{i}_{dq} &= \mathbf{T}(\theta)^{-1} \mathbf{i}_\sigma. \end{aligned} \quad (5.15)$$

The stationary frame representation is utilized for disturbance to output analyses of CCR3 and IDMBC methods.

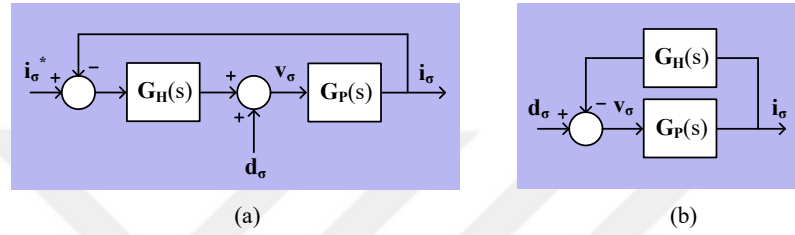


Figure 5.10: Generic control block diagram for 3P3W VSC systems showing the command current, the output current, and the disturbance in stationary frame as column vectors.

In Figure 5.11, the generic current control system block diagram is shown involving the current command signal ($\mathbf{i}_{dq}^* = [i_d^* \ i_q^*]^T$), the system output ($\mathbf{i}_{dq} = [i_d \ i_q]^T$), the applied (R-L) load voltage ($\mathbf{v}_{dq} = [v_d \ v_q]^T$), and the disturbance signal (\mathbf{d}_{dq}). In the case of 3P3W VSCs under study, the disturbance signal is the difference between the estimated disturbance compensation voltage and the actual disturbance voltage which is given by

$$\mathbf{d}_{dq} = \hat{\mathbf{v}}_{D-dq} - \mathbf{v}_{D-dq} \quad (5.16)$$

where $\hat{\mathbf{v}}_{D-dq}$ and \mathbf{v}_{D-dq} are the synchronous frame representations of the estimated and actual disturbance. It should be noted that $\mathbf{G}_{P-dq}(s)$ is the physical plant transfer function matrix whereas $\mathbf{G}_{H-dq}(s)$ is the overall unified form of the other system blocks in the overall current regulation system.

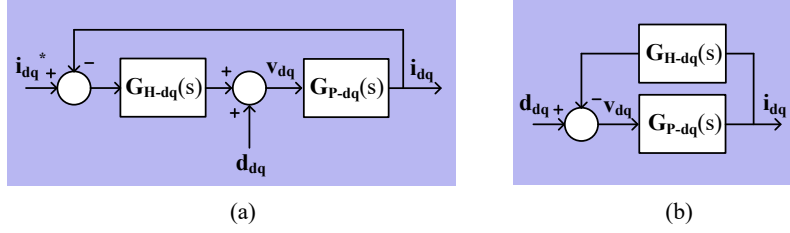


Figure 5.11: Generic control block diagram for 3P3W VSC systems showing the command current, the output current, and the disturbance in dq-frame as column vectors.

The closed-loop CCR3 and IDMBC current control methods for 3P3W VSC systems can be represented in stationary and synchronous frames as shown in Figures 5.10 and 5.11 respectively. Between these, the synchronous frame representation based command to output analyses is made.

5.8.1 Command to Output Characteristics

In order to obtain the command to output characteristics of the CCR3 and IDMBC methods, the equations representing the system dynamics are first described in the stationary frame and then transformed into synchronously rotating dq-frame. For this purpose, the system equation of CCR3 method is derived firstly. In accordance with the conventions and Figure 5.9(a) the closed-loop system dynamics for CCR3 method can be described in terms of line to line quantities as

$$\mathbf{L}_\sigma \frac{d}{dt} \mathbf{i}_\sigma = -\mathbf{R}_\sigma \mathbf{i}_\sigma + \mathbf{v}_\sigma^* + \hat{\mathbf{v}}_D - \mathbf{v}_D. \quad (5.17)$$

Here the control input is implicitly denoted as \mathbf{v}_σ . However, this signal is first generated in the synchronous frame and then transformed to the stationary frame as discussed previously. In order to perform frequency response analyses in dq-frame, all the stationary frame variables can be expressed in dq-frame as

$$\mathbf{L}_\sigma \frac{d}{dt} (\mathbf{T}(\theta) \mathbf{i}_{dq}) = -\mathbf{R}_\sigma \mathbf{T}(\theta) \mathbf{i}_{dq} + \mathbf{H}(\theta) \mathbf{v}_{dq} + \mathbf{T}(\theta) \mathbf{d}_{dq} \quad (5.18)$$

by using the stationary frame to synchronous frame conversion rules $\mathbf{i}_\sigma = \mathbf{T}(\theta)\mathbf{i}_{dq}$, $\hat{\mathbf{v}}_D - \mathbf{v}_D = \mathbf{T}(\theta)\mathbf{d}_{dq}$ and $\mathbf{v}_\sigma^* = \mathbf{H}(\theta)\mathbf{v}_{dq}$. Here it should be noted that the voltage transformation is distinct from the current transformation due to the fact that the two-phase stationary frame current variables are phase quantities whereas the voltage variables are line-to-line quantities.

Expanding the derivative term one can obtain

$$\mathbf{L}_\sigma[\omega\mathbf{P}(\theta)\mathbf{i}_{dq} + \mathbf{T}(\theta)\frac{d}{dt}\mathbf{i}_{dq}] = -\mathbf{R}_\sigma\mathbf{T}(\theta)\mathbf{i}_{dq} + \mathbf{H}(\theta)\mathbf{v}_{dq} + \mathbf{T}(\theta)\mathbf{d}_{dq} \quad (5.19)$$

where $\mathbf{P}(\theta) = \mathbf{T}(\theta + \frac{\pi}{2})$. Assuming slowly changing θ with respect to investigated system dynamics, (5.19) can be represented in s-domain as

$$\mathbf{L}_\sigma[\omega\mathbf{P}(\theta)\mathbf{i}_{dq}(s) + s\mathbf{T}(\theta)\mathbf{i}_{dq}(s)] = -\mathbf{R}_\sigma\mathbf{T}(\theta)\mathbf{i}_{dq}(s) + \mathbf{H}(\theta)\mathbf{v}_{dq}(s) + \mathbf{T}(\theta)\mathbf{d}_{dq}(s). \quad (5.20)$$

Until here, the output of the synchronous frame compensation \mathbf{v}_{dq} is kept implicit. It can be expressed explicitly in s-domain as

$$\mathbf{v}_{dq}(s) = \mathbf{K}_c(s)[\mathbf{i}_{dq}^*(s) - \mathbf{i}_{dq}(s)] + \mathbf{W}_d\mathbf{i}_{dq}(s) \quad (5.21)$$

where $\mathbf{K}_c(s)$ and \mathbf{W}_d are compensation and cross-coupling decoupling matrices respectively which are $\mathbf{K}_c(s) = \begin{bmatrix} K_p + K_i/s & 0 \\ 0 & K_p + K_i/s \end{bmatrix}$ and $\mathbf{W}_d = \begin{bmatrix} 0 & -\omega L \\ \omega L & 0 \end{bmatrix}$. Here it should be noted that when the 3P3W VSC system is linear, the decoupling matrix \mathbf{W}_d is as described, employing the constant phase inductance L in its structure. However, when the system is nonlinear this matrix becomes indeterminate because of that the instantaneous inductance of each phase is distinct from each other, which is an another drawback of the CCR3 method. However, in the analyses of CCR3 method for the nonlinear inductance case, the minimum value of the phase inductances L_{min} is utilized explaining the form of \mathbf{W}_d .

Combining (5.20) and (5.21) the overall closed-loop system employing CCR3 method can be described in s-domain by

$$\begin{aligned} \mathbf{L}_\sigma[\omega\mathbf{P}(\theta)\mathbf{i}_{dq}(s) + s\mathbf{T}(\theta)\mathbf{i}_{dq}(s)] = \\ - \mathbf{R}_\sigma\mathbf{T}(\theta)\mathbf{i}_{dq}(s) + \mathbf{H}(\theta)\{\mathbf{K}_c(s)[\mathbf{i}_{dq}^*(s) - \mathbf{i}_{dq}(s)] + \mathbf{W}_d\mathbf{i}_{dq}(s)\} + \mathbf{T}(\theta)\mathbf{d}_{dq}(s). \end{aligned} \quad (5.22)$$

The equation (5.22) can be rewritten in a more standardized form for command to output and disturbance to output frequency response analyses as

$$\mathbf{i}_{dq}(s) = \mathbf{G}_{OL-dq}^{CCR3}(s)[\mathbf{i}_{dq}^*(s) - \mathbf{i}_{dq}(s)] + \mathbf{G}_D^{CCR3}(s)\mathbf{d}_{dq}(s) \quad (5.23)$$

where $\mathbf{G}_{OL-dq}^{CCR3}(s) = \{\mathbf{L}_\sigma[\omega\mathbf{P}(\theta) + s\mathbf{T}(\theta)] + \mathbf{R}_\sigma\mathbf{T}(\theta) - \mathbf{H}(\theta)\mathbf{W}_d\}^{-1}\mathbf{H}(\theta)\mathbf{K}_c(s)$ and $\mathbf{G}_D^{CCR3}(s) = \{\mathbf{L}_\sigma[\omega\mathbf{P}(\theta) + s\mathbf{T}(\theta)] + \mathbf{R}_\sigma\mathbf{T}(\theta) - \mathbf{H}(\theta)\mathbf{W}_d\}^{-1}\mathbf{T}(\theta)$. Here $\mathbf{G}_{OL-dq}^{CCR3}(s)$ is the command to output open-loop transfer function matrix in dq-frame. On the other hand, the disturbance to output matrix of CCR3 method can be obtained by

$$\mathbf{F}_D^{CCR3}(s) = [\mathbf{I} + \mathbf{G}_{OL-dq}^{CCR3}(s)]^{-1}\mathbf{G}_D^{CCR3}(s). \quad (5.24)$$

The system transfer function of IDMBC method for 3P3W system can be established similarly. The initial governing equation is the same that of CCR3 given by (5.17). However, this time the control input \mathbf{v}_σ^* is determined by the synchronous frame compensator and stationary frame IDMBC method. Considering Figure 5.9, the system dynamics (5.17) can be expanded for IDMBC method in stationary frame as

$$\frac{\hat{\mathbf{L}}_\sigma}{L_{min}} \frac{d}{dt} \int_0^t [\mathbf{w}_\sigma - \mathbf{R}_d\mathbf{i}_\sigma] d\tau + \frac{\hat{\mathbf{R}}_\sigma}{L_{min}} \int_0^t [\mathbf{w}_\sigma - \mathbf{R}_d\mathbf{i}_\sigma] d\tau = \mathbf{L}_\sigma \frac{d}{dt} \mathbf{i}_\sigma + \mathbf{R}_\sigma \mathbf{i}_\sigma + \mathbf{v}_D - \hat{\mathbf{v}}_D \quad (5.25)$$

which can be rewritten as

$$\int_0^t \frac{\hat{\mathbf{L}}_\sigma}{L_{min}} \frac{d}{d\tau} [\mathbf{w}_\sigma - \mathbf{R}_d\mathbf{i}_\sigma] - \mathbf{L}_\sigma \frac{d^2}{d\tau^2} \mathbf{i}_\sigma + \frac{\hat{\mathbf{R}}_\sigma}{L_{min}} [\mathbf{w}_\sigma - \mathbf{R}_d\mathbf{i}_\sigma] - \mathbf{R}_\sigma \frac{d}{d\tau} \mathbf{i}_\sigma d\tau = \mathbf{v}_D - \hat{\mathbf{v}}_D. \quad (5.26)$$

When the variables are transformed to the synchronous dq-frame the equation (5.26)

becomes

$$\int_0^t \left\{ \frac{\hat{\mathbf{L}}_\sigma}{L_{min}} \frac{d}{d\tau} [\mathbf{T}(\theta) \mathbf{v}_{dq} - \mathbf{R}_d \mathbf{T}(\theta) \mathbf{i}_{dq}] - \mathbf{L}_\sigma \frac{d^2}{d\tau^2} [\mathbf{T}(\theta) \mathbf{i}_{dq}] + \frac{\hat{\mathbf{R}}_\sigma}{L_{min}} [\mathbf{T}(\theta) \mathbf{v}_{dq} - \mathbf{R}_d \mathbf{T}(\theta) \mathbf{i}_{dq}] - \mathbf{R}_\sigma \frac{d}{d\tau} [\mathbf{T}(\theta) \mathbf{i}_{dq}] \right\} d\tau = -\mathbf{T}(\theta) \mathbf{d}_{dq}. \quad (5.27)$$

Here it should be noted that the voltage transformation from dq-frame to stationary frame is also made by the phase transformation matrix $\mathbf{T}(\theta)$ instead of line-to-line transformation matrix $\mathbf{H}(\theta)$ due to the designed linearization architecture ($\mathbf{w}_\sigma = \mathbf{T}(\theta) \mathbf{v}_{dq}$). One can rewrite (5.27) equivalently as

$$\frac{\hat{\mathbf{L}}_\sigma}{L_{min}} \frac{d}{dt} [\mathbf{T}(\theta) \mathbf{v}_{dq} - \mathbf{R}_d \mathbf{T}(\theta) \mathbf{i}_{dq}] - \mathbf{L}_\sigma \frac{d^2}{dt^2} [\mathbf{T}(\theta) \mathbf{i}_{dq}] + \frac{\hat{\mathbf{R}}_\sigma}{L_{min}} [\mathbf{T}(\theta) \mathbf{v}_{dq} - \mathbf{R}_d \mathbf{T}(\theta) \mathbf{i}_{dq}] - \mathbf{R}_\sigma \frac{d}{dt} [\mathbf{T}(\theta) \mathbf{i}_{dq}] = -\frac{d}{dt} [\mathbf{T}(\theta) \mathbf{d}_{dq}]. \quad (5.28)$$

Expanding the derivative terms (5.28) can be written as

$$\begin{aligned} & \frac{\hat{\mathbf{L}}_\sigma}{L_{min}} \left\{ [\omega \mathbf{P}(\theta) \mathbf{v}_{dq} + \mathbf{T}(\theta) \frac{d}{dt} \mathbf{v}_{dq}] - \mathbf{R}_d [\omega \mathbf{P}(\theta) \mathbf{i}_{dq} + \mathbf{T}(\theta) \frac{d}{dt} \mathbf{i}_{dq}] \right\} \\ & - \mathbf{L}_\sigma [-\omega^2 \mathbf{T}(\theta) \mathbf{i}_{dq} + \omega \mathbf{P}(\theta) \mathbf{i}_{dq} + \mathbf{T}(\theta) \mathbf{i}_{dq} \frac{d^2}{dt^2} i_{dq}] + \frac{\hat{\mathbf{R}}_\sigma}{L_{min}} [\mathbf{T}(\theta) \mathbf{v}_{dq} - \mathbf{R}_d \mathbf{T}(\theta) \mathbf{i}_{dq}] \\ & - \mathbf{R}_\sigma [\omega \mathbf{P}(\theta) \mathbf{i}_{dq} + \mathbf{T}(\theta) \frac{d}{dt} \mathbf{i}_{dq}] = -[\omega \mathbf{P}(\theta) \mathbf{d}_{dq} + \mathbf{T}(\theta) \frac{d}{dt} \mathbf{d}_{dq}]. \end{aligned} \quad (5.29)$$

Considering the spatial terms vary slowly with respect to the investigated system dynamics, one can represent (5.29) in s-domain in a grid angle-dependent form as

$$\begin{aligned} & \frac{\hat{\mathbf{L}}_\sigma}{L_{min}} [\mathbf{X}(\theta, s) \mathbf{v}_{dq}(s) - \mathbf{R}_d \mathbf{X}(\theta, s) \mathbf{i}_{dq}(s)] - \mathbf{L}_\sigma \mathbf{Y}(\theta, s) \mathbf{i}_{dq}(s) \\ & + \frac{\hat{\mathbf{R}}_\sigma}{L_{min}} [\mathbf{T}(\theta) \mathbf{v}_{dq} - \mathbf{R}_d \mathbf{T}(\theta) \mathbf{i}_{dq}] - \mathbf{R}_\sigma \mathbf{X}(\theta, s) \mathbf{i}_{dq}(s) = -\mathbf{X}(\theta, s) \mathbf{d}_{dq}(s). \end{aligned} \quad (5.30)$$

wherein $\mathbf{X}(\theta, s) = \omega \mathbf{P}(\theta) + s \mathbf{T}(\theta)$ and $\mathbf{Y}(\theta, s) = -\omega^2 \mathbf{T}(\theta) + 2\omega s \mathbf{P}(\theta) + s^2 \mathbf{T}(\theta)$.

This equation can be represented in a more compact form as

$$\mathbf{i}_{dq}(s) = \mathbf{G}_{OL-dq}^{IDMBC}(s)[\mathbf{i}_{dq}^*(s) - \mathbf{i}_{dq}(s)] + \mathbf{G}_{D-dq}^{IDMBC}(s)\mathbf{d}_{dq}(s) \quad (5.31)$$

where $\mathbf{G}_{OL}^{IDMBC-dq}(s) = \left[\left\{ \frac{\hat{L}_\sigma}{L_{min}} \mathbf{R}_d \mathbf{X}(\theta, s) + \mathbf{L}_\sigma \mathbf{Y}(\theta, s) + \frac{\hat{R}_\sigma}{L_{min}} \mathbf{R}_d \mathbf{T}(\theta) \mathbf{R}_\sigma \mathbf{X}(\theta, s) \right\} - \left\{ \frac{\hat{L}_\sigma}{L_{min}} \mathbf{X}(\theta, s) + \frac{\hat{R}_\sigma}{L_{min}} \mathbf{T}(\theta) \right\} \mathbf{W}_d \right]^{-1} \left[\frac{\hat{L}_\sigma}{L_{min}} \mathbf{X}(\theta, s) + \frac{\hat{R}_\sigma}{L_{min}} \mathbf{T}(\theta) \right] \mathbf{K}_c(s)$ and

$$\mathbf{G}_D^{IDMBC-dq}(s) = \left[\left\{ \frac{\hat{L}_\sigma}{L_{min}} \mathbf{R}_d \mathbf{X}(\theta, s) + \mathbf{L}_\sigma \mathbf{Y}(\theta, s) + \frac{\hat{R}_\sigma}{L_{min}} \mathbf{R}_d \mathbf{T}(\theta) \mathbf{R}_\sigma \mathbf{X}(\theta, s) \right\} - \left\{ \frac{\hat{L}_\sigma}{L_{min}} \mathbf{X}(\theta, s) + \frac{\hat{R}_\sigma}{L_{min}} \mathbf{T}(\theta) \right\} \mathbf{W}_d \right]^{-1} \mathbf{X}(\theta, s).$$

Here $\mathbf{G}_{OL-dq}^{IDMBC}(s)$ is the command to output open-loop transfer function matrix of IDMBC method. It should be noted that in these equations the cross-coupling decoupling matrix employs the minimum inductance value as the linearized system have an inductance of L_{min} which is hence described by

$$\mathbf{W}_d = \begin{bmatrix} 0 & -\omega L_{min} \\ \omega L_{min} & 0 \end{bmatrix}. \quad (5.32)$$

On the other hand, the disturbance to output matrix of IDMBC method can be obtained by

$$\mathbf{F}_{D-dq}^{IDMBC}(s) = [\mathbf{I} + \mathbf{G}_{OL-dq}^{IDMBC}(s)]^{-1} \mathbf{G}_{D-dq}^{IDMBC}(s). \quad (5.33)$$

Command to output frequency response characteristics of the CCR3 and IDMBC methods for 3P3W systems are investigated on a phase angle-dependent form that is obtained in the derivations. For this purpose, the disturbance signal is set to zero for both methods. Accordingly, the open-loop control system in dq-frame reduces down to two-input two-output system characterized by $\mathbf{G}_{OL-dq}^{CCR3}(s)$ and $\mathbf{G}_{OL-dq}^{IDMBC}(s)$ matrices respectively which are obtained formerly.

In order to verify the frequency response characteristics obtained, linear phase inductors with equal inductance case is considered initially. The estimated parameters are taken equal to actual parameters both for linear and nonlinear system studies. In Figure 5.12 the linear and balanced 3P3W VSC system d-axis to d-axis and q-axis to q-axis frequency response (also called self-frequency response within the context

of this thesis) characteristics of CCR3 and IDMBC control methods are illustrated. The K_p and K_i gains are tuned to provide $2\pi 500$ rad/s of bandwidth for a VSC system having per-phase resistance and inductance values of 0.5Ω and $500 \mu H$ respectively. Active damping resistance for IDMBC method is selected the same as the phase resistance $\mathbf{R}_d = \text{diag}[0.5 \ 0.5]$. When the 3P3W VSC system is linear and balanced, the open-loop system transfer function matrices of both CCR3 and IDMBC methods are expected to be comprised of only diagonal elements and the cross-coupling elements to be ideally zero when cross-coupling decoupling is performed accurately.

It can be observed from the magnitude plot of the self-frequency response characteristics in Figure 5.12 that both for CCR3 and IDMBC methods the system bandwidth obtained from the frequency response characteristics are the same of the design bandwidth. It should be noted that even the phase angle-dependent s-domain transfer functions are employed, these magnitude and phase plots are phase angle independent due to linear and balanced system characteristics.

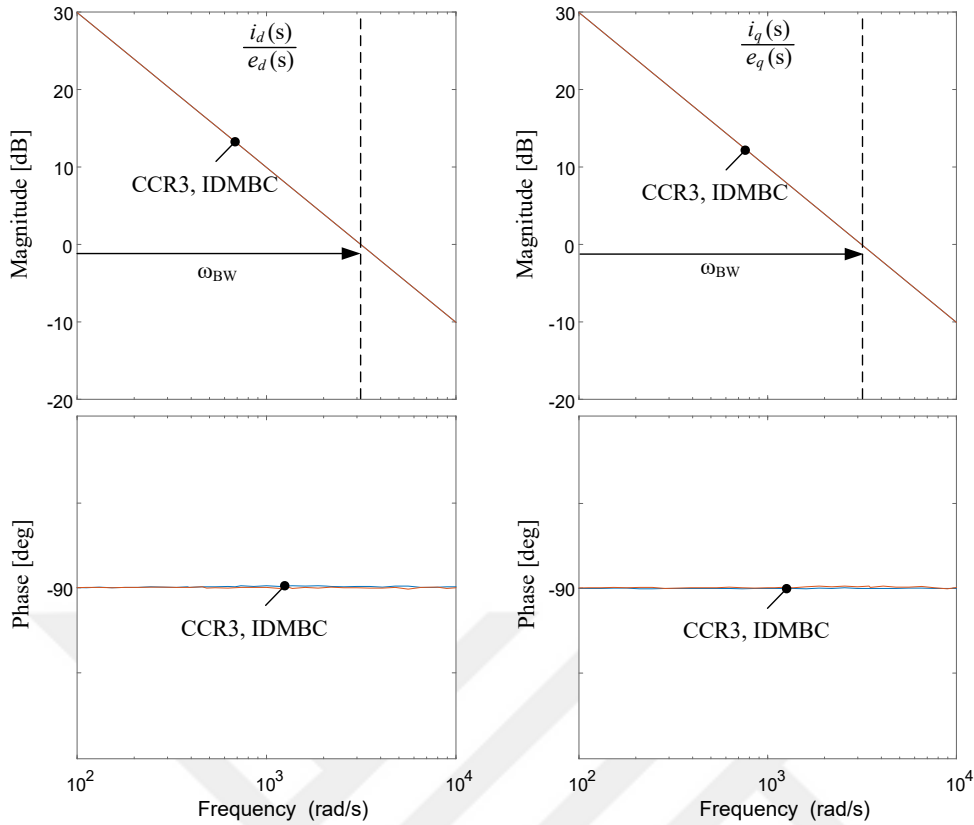


Figure 5.12: D-axis to d-axis and q-axis to q-axis open loop magnitude and phase characteristics of the frequency responses of CCR3 and IDMBC methods for balanced 3P3W linear VSC system case. These plots are phase angle independent due to linear and balanced operation.

In Figure 5.13 the magnitude and phase responses of the cross-coupling constituents of the open-loop frequency responses are illustrated. As the cross-coupling term due to derivation on the space vector rotation is time-invariant in the linear and balanced case the addition the cross-coupling decoupling terms, which is denoted by W_d , converts the system into a decoupled one. Therefore, the cross-coupling magnitude plots become nearly zero as shown in the figure and the phase plots meaningless which is as expected.

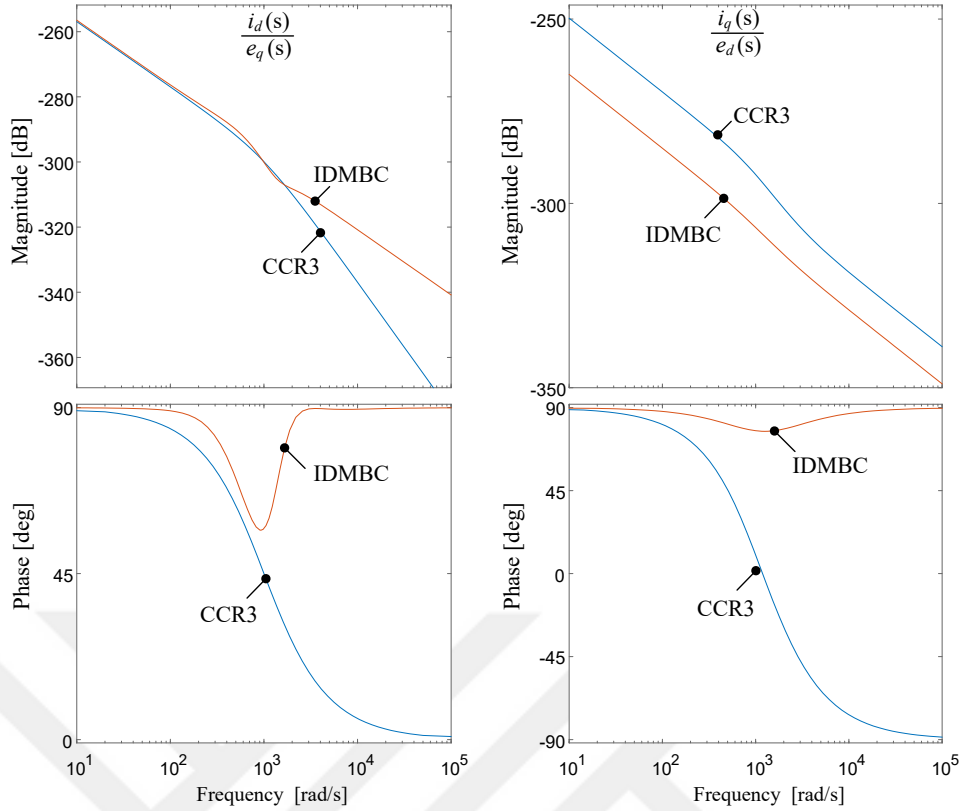


Figure 5.13: q-axis to d-axis and d-axis to q-axis (cross-coupled) open loop magnitude and phase characteristics of the frequency responses of CCR3 and IDMBC methods for balanced 3P3W linear VSC system case.

In order to investigate the command to output characteristics nonlinear 3P3W VSC systems, the nonlinear inductor characteristics given in Figure 2.11 are employed. The system per-phase resistance is taken as 0.5Ω . With nonlinear inductors, the tuning procedure of conventional current controllers are indeterminate. However, the bandwidth upper limit still constraints the controller design and in a practical design should this constraint should be taken into account. Therefore a design considering the minimum inductance value per-phase will guarantee the safe operation of the VSC, without exceeding the bandwidth upper limit constraint. But inevitably bandwidth shrinkage will take place as discussed formerly. Similarly, the cross-coupling decoupling matrix \mathbf{W}_d is indeterminate in CCR3 method when the VSC system is a nonlinear one with the use of saturable inductors. However, minimum inductance value is utilized in order to provide decoupling even if it is not fully decoupled as

shown in the following paragraphs. Thus, this matrix can be set for CCR3 method as

$$\mathbf{W}_d = \begin{bmatrix} 0 & -\omega L_{min} \\ \omega L_{min} & 0 \end{bmatrix}. \quad (5.34)$$

In Figure 5.14, the magnitude and phase plots of self-transfer function of the open-loop frequency response of the CCR3 method is illustrated. The d-axis and q-axis self bandwidths shrink considerably from the design bandwidth as one can interpret from the figure. The bandwidth shrinkage is more in q-axis whereas it is less in d-axis as the current command is provided in the d-axis ($\theta_0 = 0$ rad/s). These characteristics is in harmony with the bandwidth shrinkage study in chapter 3.

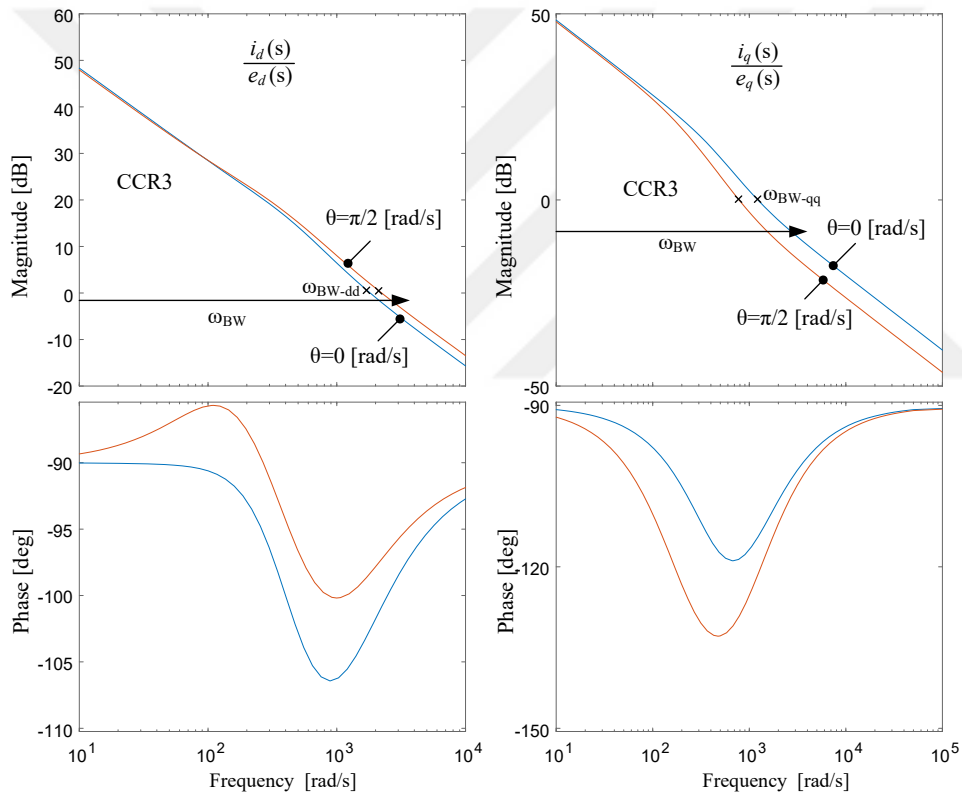


Figure 5.14: d-axis to d-axis and q-axis to q-axis open loop magnitude and phase characteristics of the frequency responses of CCR3 method for nonlinear inductor case.

In Figure 5.15, the magnitude and phase responses of cross-coupling terms of the open-loop transfer function of CCR3 method is illustrated. Even if decoupling per-

formed, the exact decoupling is not achieved when the system is a nonlinear one. When the system was a linear and balanced one the d-axis and q-axis could be decoupled from each other hence the cross-coupling open-loop frequency response magnitude was nearly zero (refer to Figure 5.13). This coupling of the d-axis and q-axis dependent to each other which is especially taken into account for the transient response of the current.

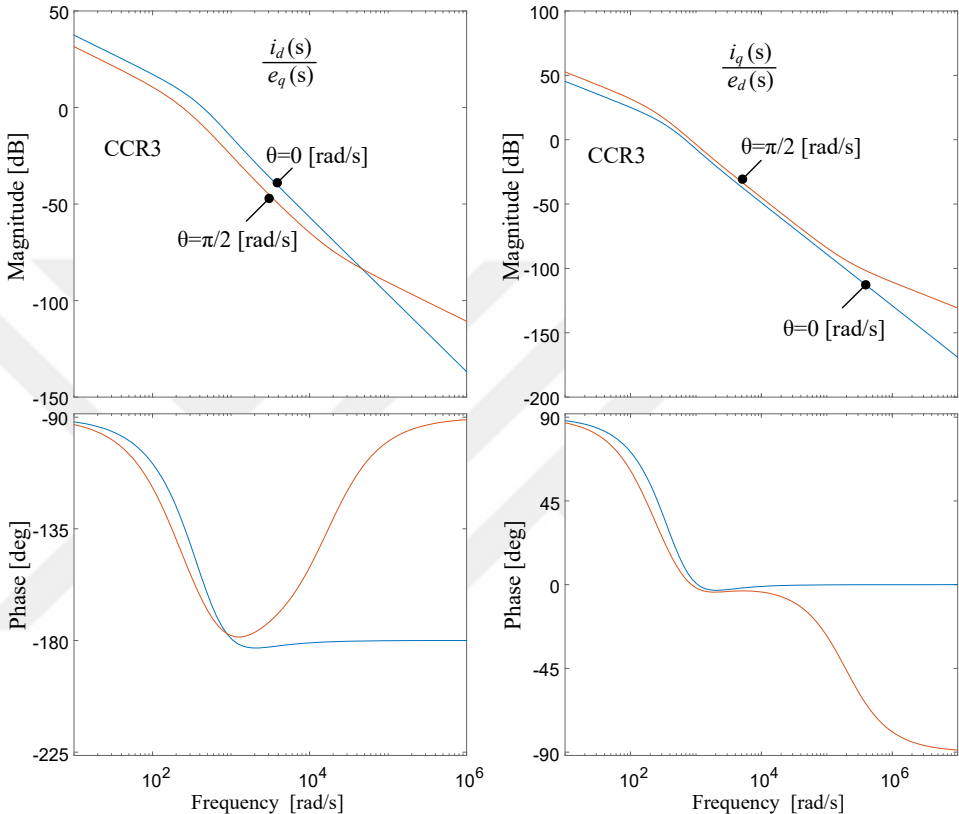


Figure 5.15: q-axis to d-axis and d-axis to q-axis open loop magnitude and phase characteristics of the frequency responses of CCR3 method for nonlinear inductor case.

In the case of IDMBC method for 3P3W VSC systems employing saturable inductors, the open-loop frequency response magnitude response is the same as that of linear systems. This is basically due to the linearization of the system. The system self bandwidths do not change with changing inductances and the cross-coupling of the system in dq-frame can be fully decoupled. In Figures 5.16 and 5.17 the magnitude and phase responses of self frequency response characteristics and cross-coupling

frequency characteristics are illustrated respectively for $\theta = 0$ and $\theta = \pi/2$. These plots confirm the linear and balanced like characteristics of the proposed IDMBC method.

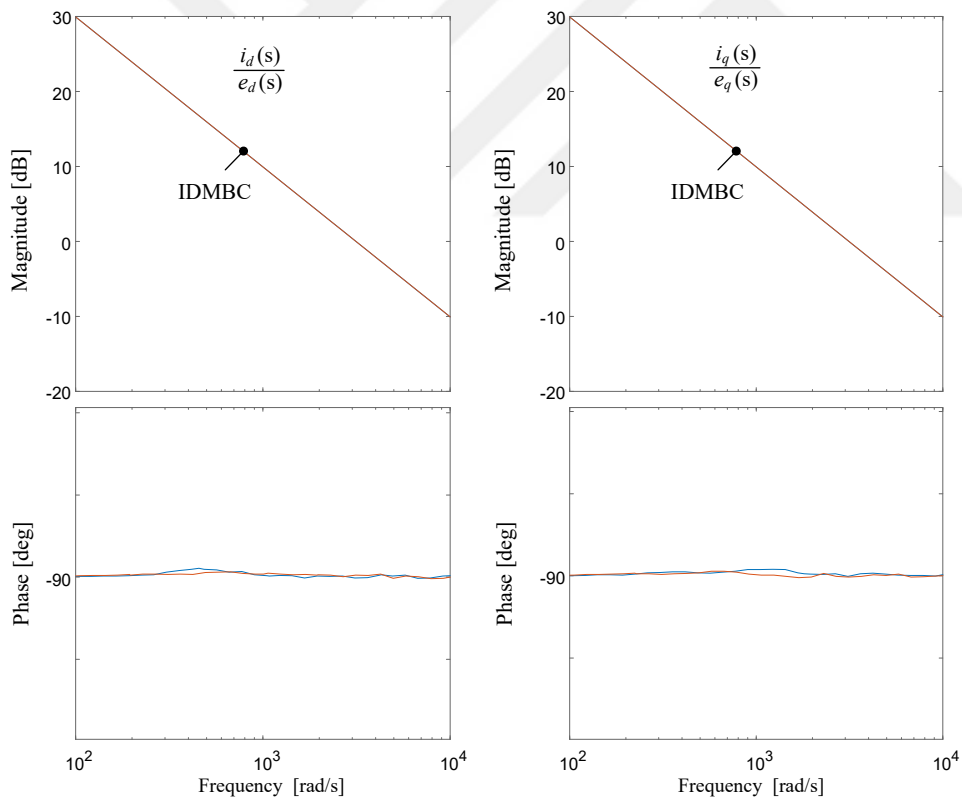


Figure 5.16: d-axis to d-axis and q-axis to q-axis open loop magnitude and phase characteristics of the frequency responses of IDMBC method for nonlinear inductor case.

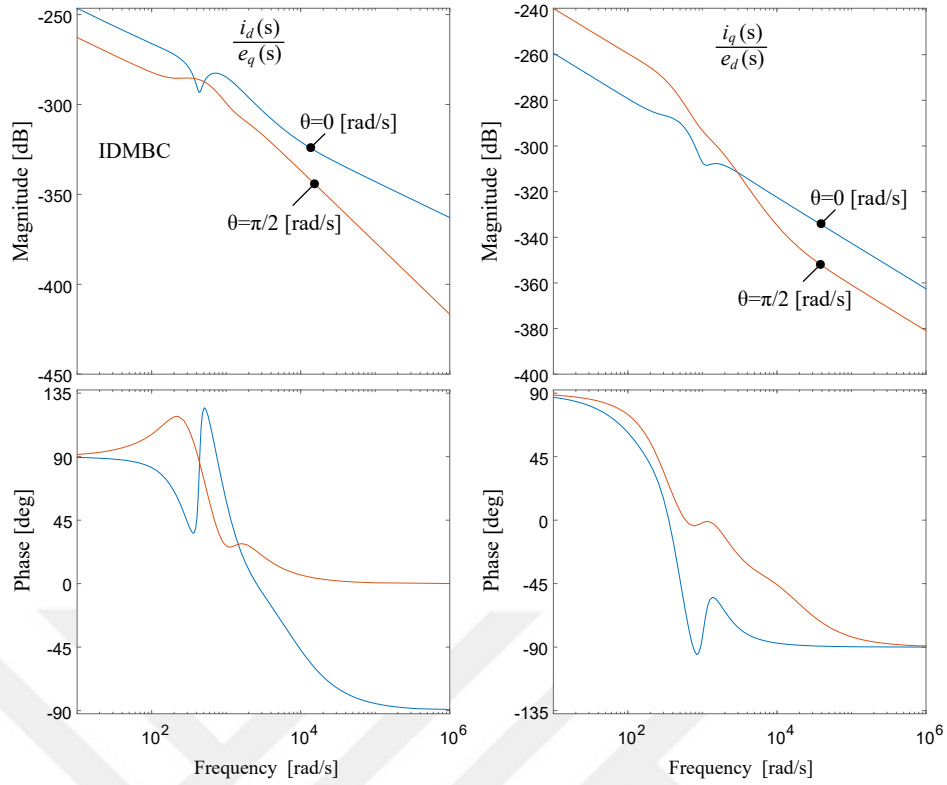


Figure 5.17: q-axis to d-axis and d-axis to q-axis (cross-coupled) open loop magnitude and phase characteristics of the frequency responses of IDMBC methods non-linear inductor case.

5.8.2 Disturbance Rejection Characteristics of IDMBC Method in 3P3W VSC System

Disturbance to output frequency response characteristics of the CCR3 and IDMBC methods for 3P3W systems are investigated in the stationary frame. Accordingly, the disturbance rejection functions of CCR3 and IDMBC methods are obtained firstly.

Starting from the stationary frame system equations (5.17) and (5.26) for CCR3 and IDMBC methods respectively, applying dq-frame to synchronous frame transformations described in (5.14) and (5.15) to the synchronous frame controller output, and setting the command signal to zero, one can write the disturbance and output relation in s-domain as in equations (5.35) and (5.36) for CCR3 and IDMBC methods respectively.

$$\mathbf{d}_\sigma(s) = \left[[s\mathbf{L}_\sigma + \mathbf{R}_\sigma] - \mathbf{H}(\theta)[\mathbf{W}_d - \mathbf{K}_c(s)]\mathbf{T}(\theta)^{-1} \right] \mathbf{i}_\sigma(s). \quad (5.35)$$

$$\mathbf{d}_\sigma(s) = \left[[s\mathbf{L}_\sigma + \mathbf{R}_\sigma] - \frac{1}{sL_{min}} \{ [s\hat{\mathbf{L}}_\sigma + \hat{\mathbf{R}}_\sigma]\mathbf{T}(\theta)[\mathbf{W}_d - \mathbf{K}_c(s)]\mathbf{T}(\theta)^{-1} - \mathbf{R}_d \} \right] \mathbf{i}_\sigma(s). \quad (5.36)$$

Therefore, disturbance to output two-input two-output system can be characterized by $\mathbf{F}_D^{\text{CCR3}}(s)$ and $\mathbf{F}_D^{\text{IDMBC}}(s)$ matrices respectively. These matrices can be simply written as

$$\mathbf{F}_D^{\text{CCR3}}(s) = \left[[s\mathbf{L}_\sigma + \mathbf{R}_\sigma] - \mathbf{H}(\theta)[\mathbf{W}_d - \mathbf{K}_c(s)]\mathbf{T}(\theta)^{-1} \right]^{-1}. \quad (5.37)$$

$$\mathbf{F}_D^{\text{IDMBC}}(s) = \left[[s\mathbf{L}_\sigma + \mathbf{R}_\sigma] - \frac{1}{sL_{min}} \{ [s\hat{\mathbf{L}}_\sigma + \hat{\mathbf{R}}_\sigma]\mathbf{T}(\theta)[\mathbf{W}_d - \mathbf{K}_c(s)]\mathbf{T}(\theta)^{-1} - \mathbf{R}_d \} \right]^{-1}. \quad (5.38)$$

The frequency domain magnitude characteristics described by (5.37) and (5.38) are investigated for the VSC system and controller parameters which are utilized in the command to output characterization (subsection 5.8.1).

In Figure 5.18, the disturbance to output magnitude plots of CCR3 and IDMBC methods are shown on the same graph for all the elements of $\mathbf{F}_D^{\text{CCR3}}(s)$ and $\mathbf{F}_D^{\text{IDMBC}}(s)$ matrices. These plots show that the magnitude of the disturbance to output transfer function of IDMBC method always lies below the disturbance to output transfer function of CCR3 method. Hence, one can conclude that disturbance rejection performance of IDMBC method is superior to CCR3 method which was the case of 1P controlled VSC systems also.

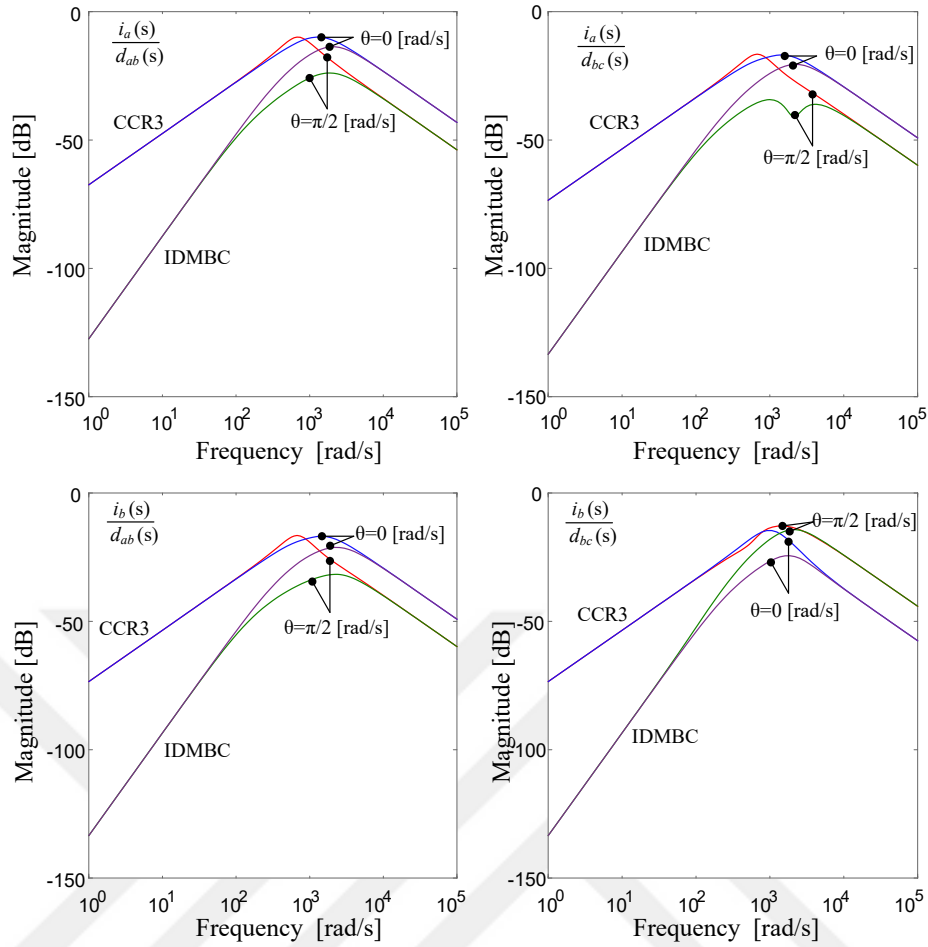


Figure 5.18: Disturbance rejection function magnitude plots of CCR3 and IDMBC methods for nonlinear inductor case at two different angles.

5.9 Validation of Inductor Saturation Compensation in 3P3W VSC Systems via Simulations

In this section, the proposed IDMBC method for 3P3W VSC system simulation results are presented in comparison with that of CCR3 method. The current regulator attributes are investigated by means of dynamic response and steady-state waveform quality. Accordingly, the simulated system configurations by means of hardware and control structure are provided.

5.9.1 Simulated System Configuration

Simulations are conducted to observe and compare the performances of the CCR and IDMBC methods for 3P3W VSC systems. Accordingly, system configuration information is provided by means of system hardware and system control.

5.9.1.1 Simulated System Hardware

Simulations studies are conducted for 3P3W VSC setup (with 350 V DC-bus voltage) to prove the viability of the proposed IDMBC control method. Saturable inductors with the $L-i$ characteristics of Figure 2.11 are employed as converter side inductors. The filter capacitor is selected to be $2.2 \mu F$ connected in a wye configuration. The grid side inductor is selected to be $2 mH$. The LCL filter provides sufficient PWM harmonic attenuation even for the minimum inductance value of the converter side inductor within the design constraints provided [80]. The overall hardware configuration is as shown in Figure 5.19. The parameters related to the simulated hardware configuration in this figure is tabulated in Table-5.1. These parameters are also the same for experimental studies that will be elaborated.

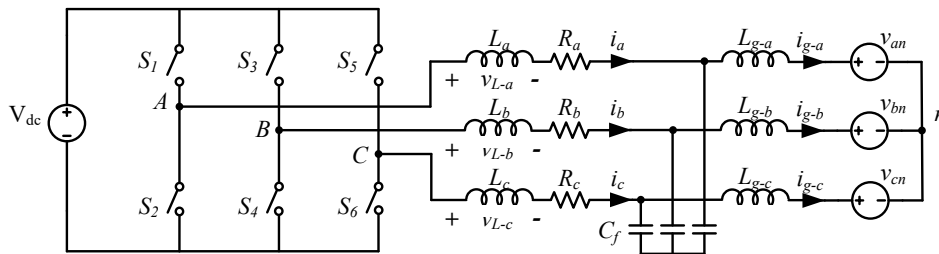


Figure 5.19: 3P3W VSC system hardware configuration for performance investigation of CCR3 and IDMBC methods.

5.9.1.2 System Control

The 3P3W VSC system simulations are performed both for CCR3 and IDMBC methods. The error compensator is a synchronous frame PI controller. This controller is implemented in a scalar manner which is described in Figure 3.5. The cross-coupling

Table 5.1: Simulated and Experimental System Parameters for 3P3W VSC System

Parameter	Value
DC-link voltage	350 V
Rated current	10 A_{peak} /phase
Grid voltage	115 V_{RMS} /phase
ω_e	$2\pi 50$ rad/s
Power module	PM75RL1A120
f_c	10 kHz
Modulation method	SVPWM
Sampling period (T_s)	50 μs
Inverter dead-time	3 μs
L_{max}/L_{min} (converter side)	4.45/0.5 mH
L_g (grid side)	2 mH
R (converter side equivalent resistance/phase)	0.5 Ω
C_f (LCL filter capacitor)	2.2 μF (2.2 %)

decoupling is performed as the same for both controllers, based on L_{min} . Figure 5.9 summarizes the implementation of the two current control methods in a closed-loop manner. During the simulations, SVPWM method is employed to efficiently utilize the DC-link voltage and to have reduced ripple current. Moreover, such utilization of SVPWM method proves the compatibility of zero-sequence voltage injection in 3P3W VSC systems with nonlinear inductors. The zero-sequence signal of SVPWM is generated by selecting the minimum voltage command magnitude of the three phases, multiplying by 0.5 and adding to each of the three-phase voltage command [81]. The synchronous frame PI controllers (for d-axis and q-axis) are tuned to provide a bandwidth of $2\pi 500$ rad/s both for CCR3 and IDMBBC methods. Accordingly, the PI gains are tuned similar to 1P VSCs, $K_p = \omega_{BW} L_{min}$ and $K_i = \omega_{BW} \hat{R}$. Simulation results are obtained as the synchronous frame compensator gains are kept the same for each test. With these specifications, dynamic response and waveform quality performances of the current control methods are investigated.

5.9.2 Dynamic Response

The dynamic response characteristics of a current regulator are one of the figure of merits to evaluate and compare the controller performances. The dynamic response performance indicates the system bandwidth also. Therefore the dynamic response simulation results provided for CCR3 and IDMBC method here also show the system bandwidth characteristics. The simulations are performed by providing 1 A step changes on d-axis and q-axis current commands within the ratings of the converter. Accordingly, the d-axis and q-axis currents are observed. When the excitation on one axis, the other axis current command is set to zero.

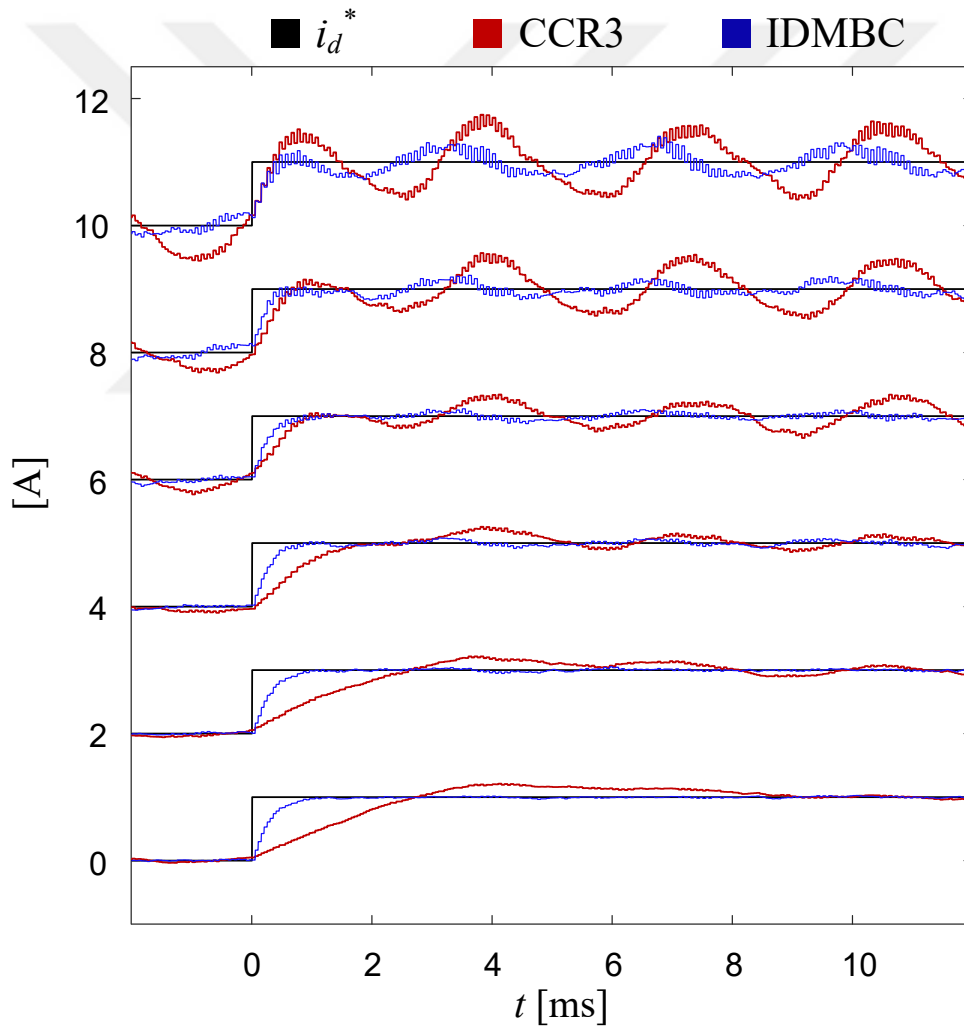


Figure 5.20: Simulated d-axis step responses of CCR3 and IDMBC methods at various d-axis DC-bias currents. Note that q-axis current command is set to zero.

In Figure 5.20, the d-axis current command and currents are illustrated for CCR3 and IDMBC methods. As the q-axis currents are set to zero they are not illustrated in the figure. The response (or rise) time to a 1 A step increase of the CCR3 method is highly dependent on the current bias as discussed in chapter 3. When the current DC-bias is zero, the rise time is approximately 3-4 ms whereas when the d-axis current DC-bias level is 10 A, the rise time of the CCR3 method is around 1 ms. This phenomenon shows the bandwidth shrinkage issue similar to the case that of 1P controlled VSCs under DC excitation.

5.9.3 Waveform Quality

The CCR3 and IDMBC methods are simulated in order to observe and compare the waveform quality performances of the systems at steady-state. First, the results related to CCR3 method are presented and then that of IDMBC. Eventually, a conclusion has been reached in terms of steady-state waveform quality.

In Figure 5.21, the steady-state converter side current, voltage command signal, zero-sequence signal, and zero-sequence added voltage command signal (the signal provided to triangle comparator) of phase-a of CCR3 method are illustrated. Although the command voltage resembles a pure sinusoid, the converter side current includes not only PWM current ripple but also low-order control-fixable harmonics.

In Figure 5.22, the grid current and converter side inductance change are illustrated. As filtered by the LCL filter, almost all PWM caused high-frequency harmonics are cleared and there remain low-order harmonics. At full current, the inductance decreases almost to $1/9^{th}$ of its zero current value as expected.

In Figure 5.23, the space vector representations of the converter side and grid side currents are illustrated for CCR3 method. In the same graphs, current command space vector is also plotted to constitute reference. Although the deviation from the current command is not very explicit in the converter side space vector plot, the deviation is more clear in the case of the grid current waveform.

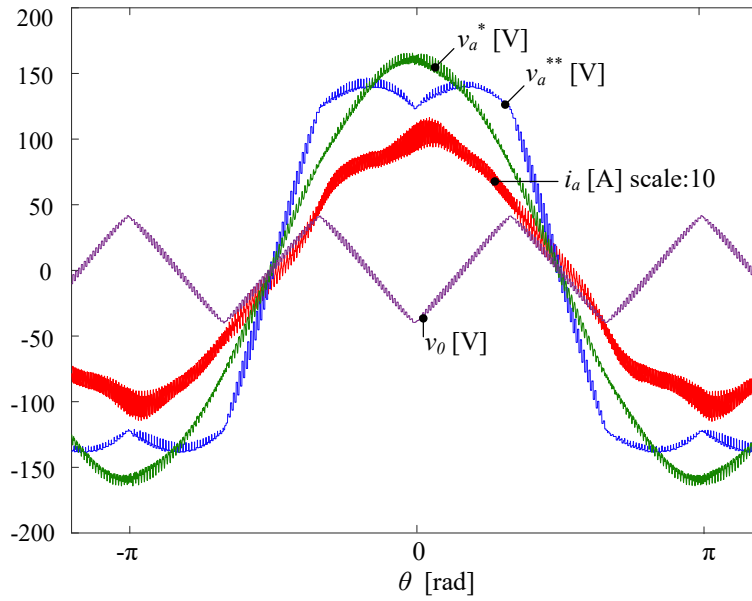


Figure 5.21: Simulated steady-state converter side current, voltage command signal, zero-sequence signal, and zero-sequence added voltage command signal of phase-a of CCR3 method.

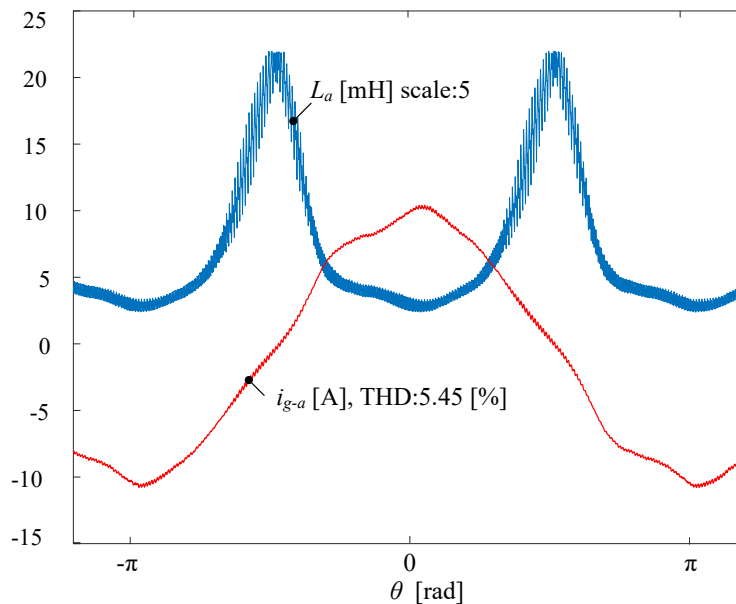


Figure 5.22: Simulated steady-state grid current and inductance variation of phase-a of CCR3 method.

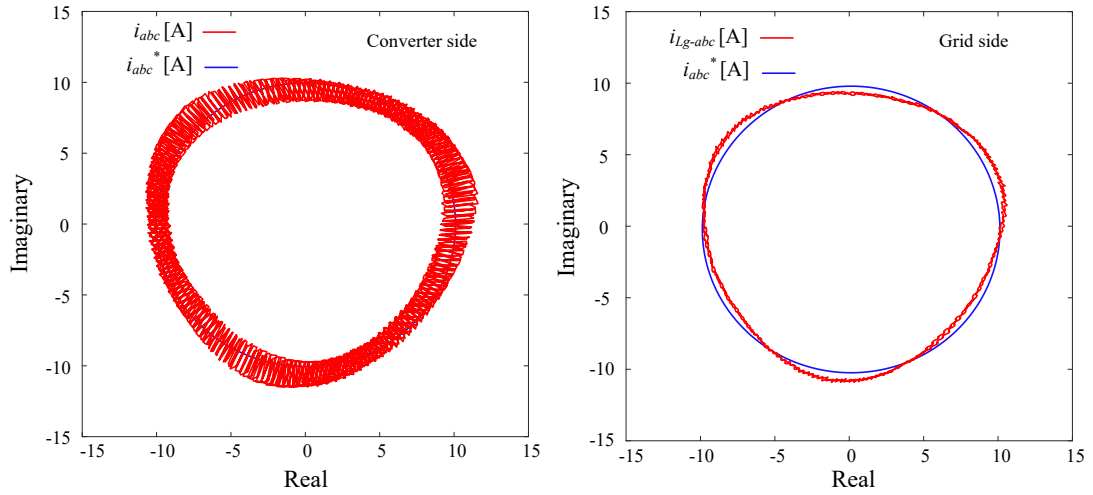


Figure 5.23: Simulated spatial variations of the converter side current and grid current of CCR3 method on the complex plane.

When the current control technique is changed to IDMBC, the steady-state converter side current, voltage command signal, zero-sequence signal, and zero-sequence added voltage command signal waveforms of phase-a become as shown in Figure 5.24. With the application of the IDMBC method, the improvement can be seen in the converter side current waveform as compared to the converter side current waveform of CCR3 method shown in Figure 5.21 even if these waveforms contain PWM current ripple.

In Figure 5.25, the phase-a converter side inductance variation and the grid side current waveform are illustrated. When compared to 5.22, one can observe the current waveform quality improvement with the employment of IDMBC method. To quantify, the current waveform THD is reduced from 5.45 % to 1.82 %.

In Figure 5.26, the spatial variations of the converter side current and grid current of IDMBC method are illustrated in the complex plane in terms of space vectors. The converter side current space vector involves PWM current ripple harmonics in the plot. However, the grid current is nearly the same as the reference current as compared to that of CCR3, verifying the suitability of the IDMBC method.

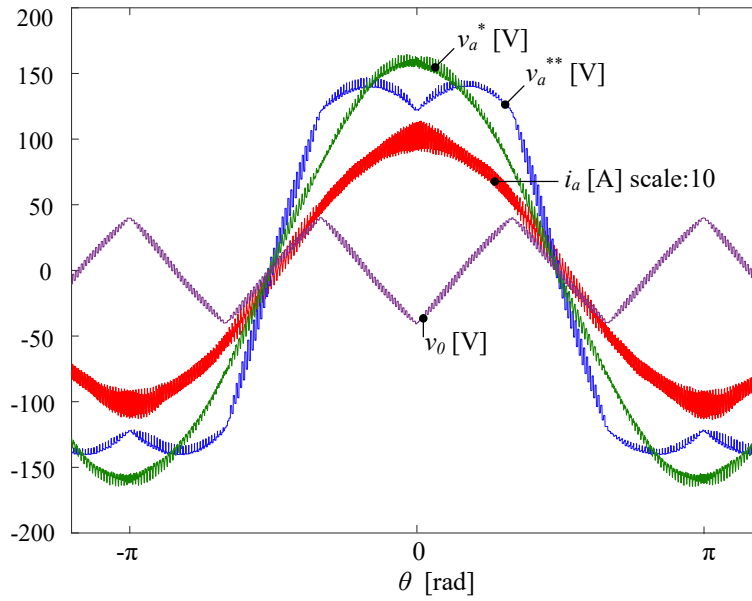


Figure 5.24: Simulated steady-state converter side current, voltage command signal, zero-sequence signal, and zero-sequence added voltage command signal of phase-a of IDMBC method.

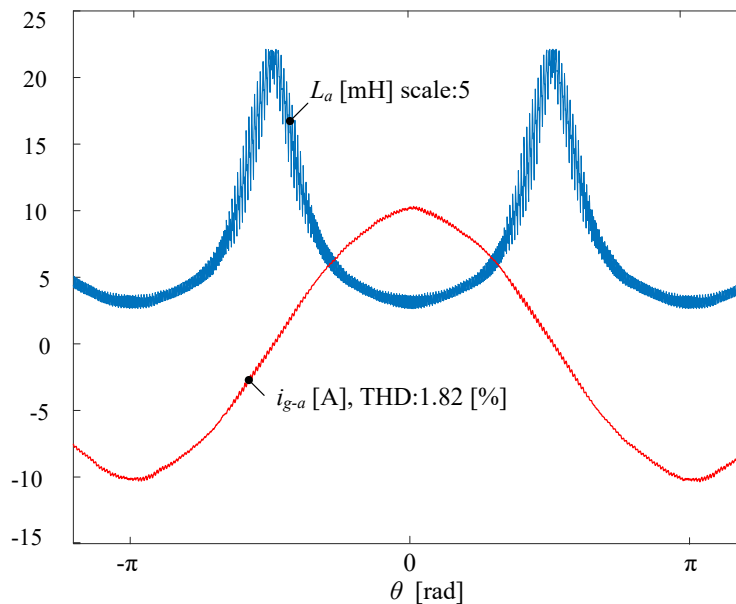


Figure 5.25: Simulated steady-state grid current and inductance variation of phase-a of IDMBC method.

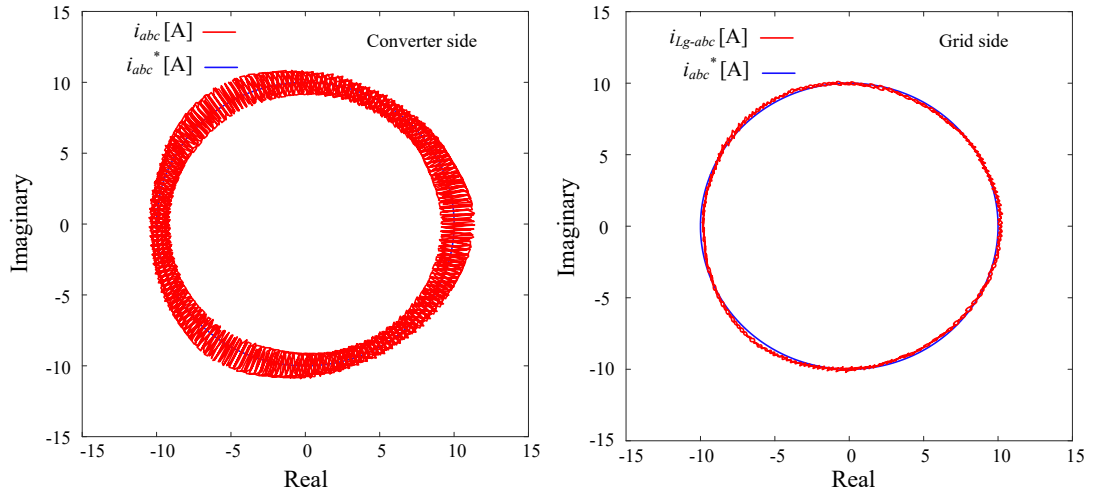


Figure 5.26: Simulated spatial variations of the converter side current and grid current of IDMBC method on the complex plane.

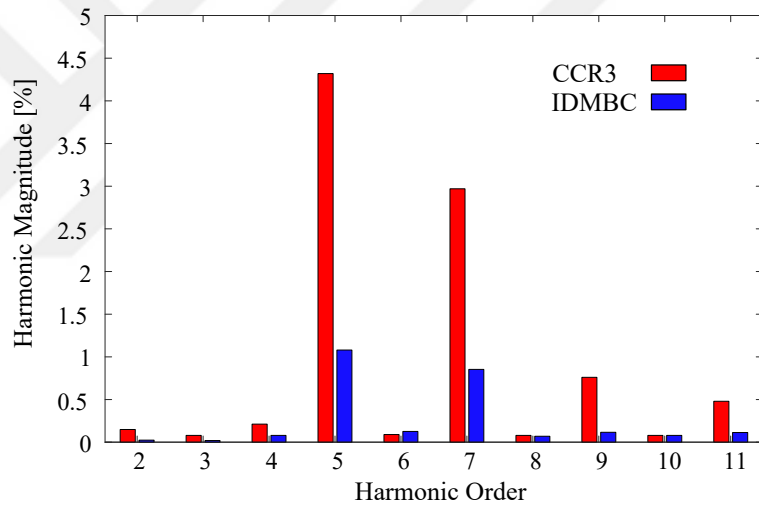


Figure 5.27: Simulated harmonic spectra of the phase currents of CCR3 and IDMBC methods near low frequency region.

In Figure 5.27, the harmonic spectrum of the CCR3 and IDMBC methods near low-frequency region is illustrated. Based on the spectrum, the most dominant harmonics can be observed to be 5^{th} and 7^{th} . Unlike the case that of 1P controlled VSCs, 3^{rd} order harmonics are nearly nonexistent as there is no path for zero-sequence currents to flow. Only a slight magnitude of 3^{rd} and its multiples take place in the spectrum which flows in a balanced manner. Especially 9^{th} harmonic is considerable in CCR3

method. However this harmonic vanishes in the case of IDMBC method. Similarly, in the case of the two most dominant low-frequency harmonics, the IDMBC method outperforms the conventional current regulation method. This makes the IDMBC method preferable by means of current waveform quality.

5.10 Validation of Inductor Saturation Compensation in 3P3W VSC Systems via Experiments

5.10.1 System Configuration

In order to observe and compare the dynamic response and steady-state performances of CCR3 and IDMBC methods, experiments are conducted. VSC+inductor terminals short-circuited and grid-connected configurations are employed for dynamic response and steady-state performance observation. The dynamic response performance of the methods is investigated via VSC+inductor terminals short-circuited configuration to eliminate the grid interaction and hence observe in a noise-free manner. Then the performance is verified via grid-connected experiments. In Figure 5.28 the VSC+inductor terminals short-circuited and grid-connected configurations are illustrated.

In VSC+inductor terminals short-circuited configuration, the experimental parameters kept the same that are tabulated in Table-5.1. In the grid-connected experiments the AC grid voltage is stepped down to $155 V_{1-n-RMS}$ via three single-phase transformers connected in a wye-wye configuration. Considering the system dynamics, for example in the synchronization, the DC-link voltage is slightly kept higher (480 V). Figure 5.29 shows this three-phase grid-connected VSC setup. The transformer leakage inductance is 0.25 mH. Additional filter inductors as grid side have been inserted also to form grid side inductances ($L_{g-a}, L_{g-b}, L_{g-c}$) together with the transformer leakage inductance.

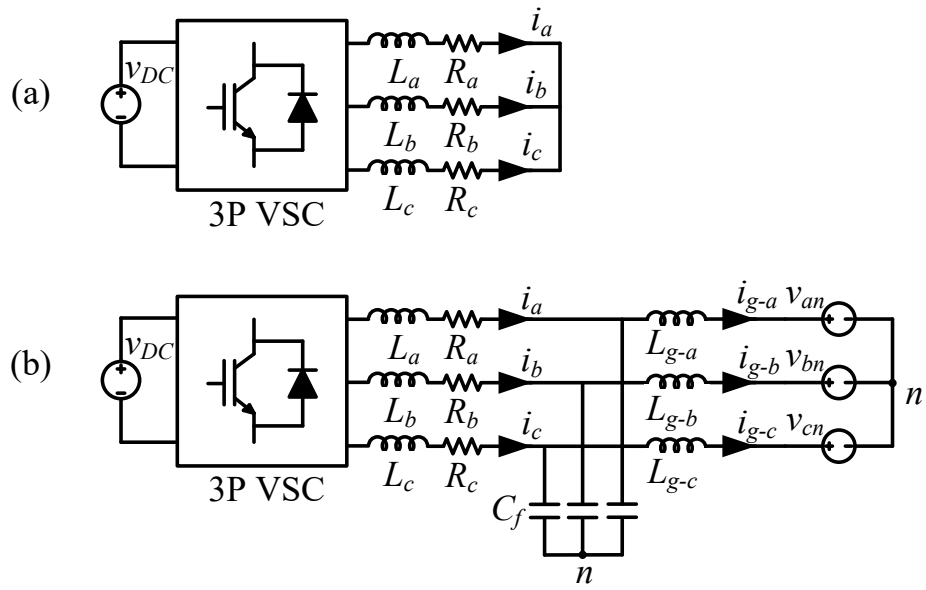


Figure 5.28: Equivalent experimental configurations. (a) VSC+inductor terminals short-circuited configuration. (b) Grid-connected configuration.

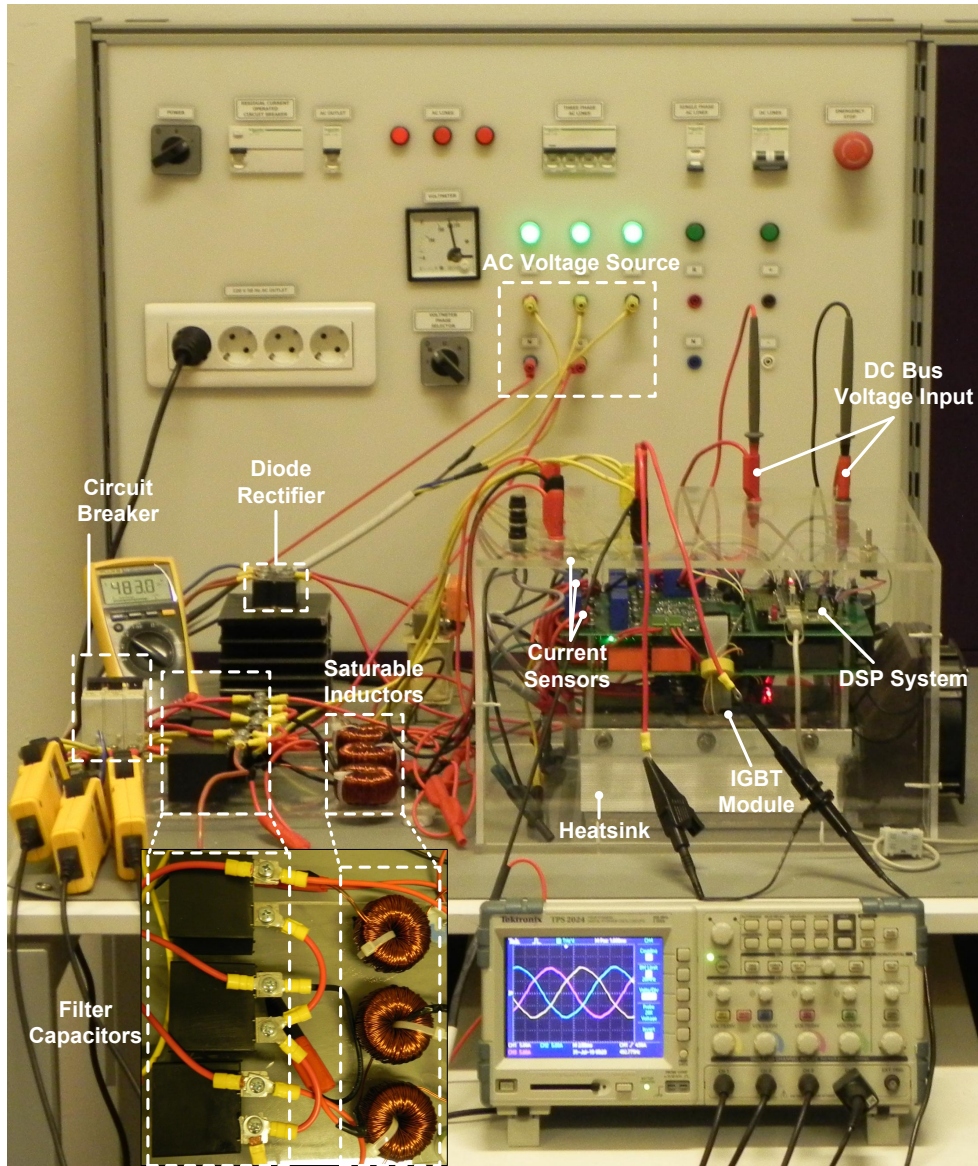


Figure 5.29: Three-phase grid-connected VSC setup.

5.10.2 Dynamic Response

In order to observe and compare the dynamic response performances of the CCR3 and IDMBC methods, 1 A step changes are applied to the d-axis current reference for both methods. To mitigate the grid voltage disturbance, the test is realized for VSC+inductor terminals are short-circuited configuration. The associated dynamic response waveforms are illustrated in Figure 5.30. Based on this figure, one can observe that the results are very similar to the one obtained in the simulations (Figure

5.20). When the d-axis current is zero, the rise time of the d-axis current is quite long in CCR3 method when compared that of IDMBC method even if the associated PI controller parameters are the same aiming the same bandwidth. This is due to the bandwidth shrinkage phenomenon in conventional current regulation as described in section 3.3.0.1. It should be noted that for these dynamic response experiments with distinct d-axis current offsets, the q-axis current is set to zero.

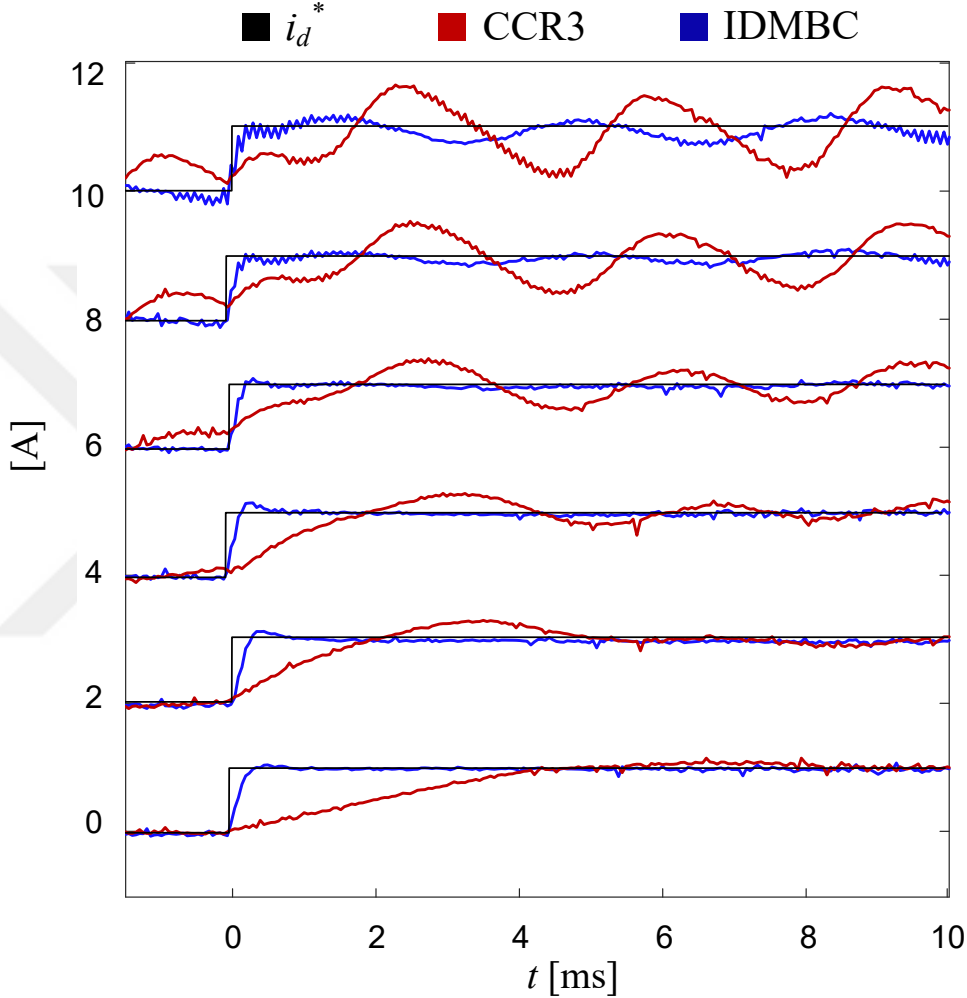


Figure 5.30: Experimental d-axis step responses of CCR3 and IDMBC methods at various d-axis DC-bias currents. Note that q-axis current is set to zero.

When the d-axis current offset is increased, the rise time of CCR3 method starts to decrease while the dynamic response characteristics of the IDMBC method is the same which is initially designed to be. When the d-axis current offset level starts to increase further low-frequency components (6^{th} harmonic) starts to appear especially

in the CCR3 d-axis current. The reason for this problem is the system nonlinearity caused 5th and 7th harmonics in the stationary frame which will be presented in the waveform quality study. Based on the dynamic response waveforms obtained, the superiority of the IDMBC method over CCR3 method is verified experimentally as proposed by analyses and simulations.

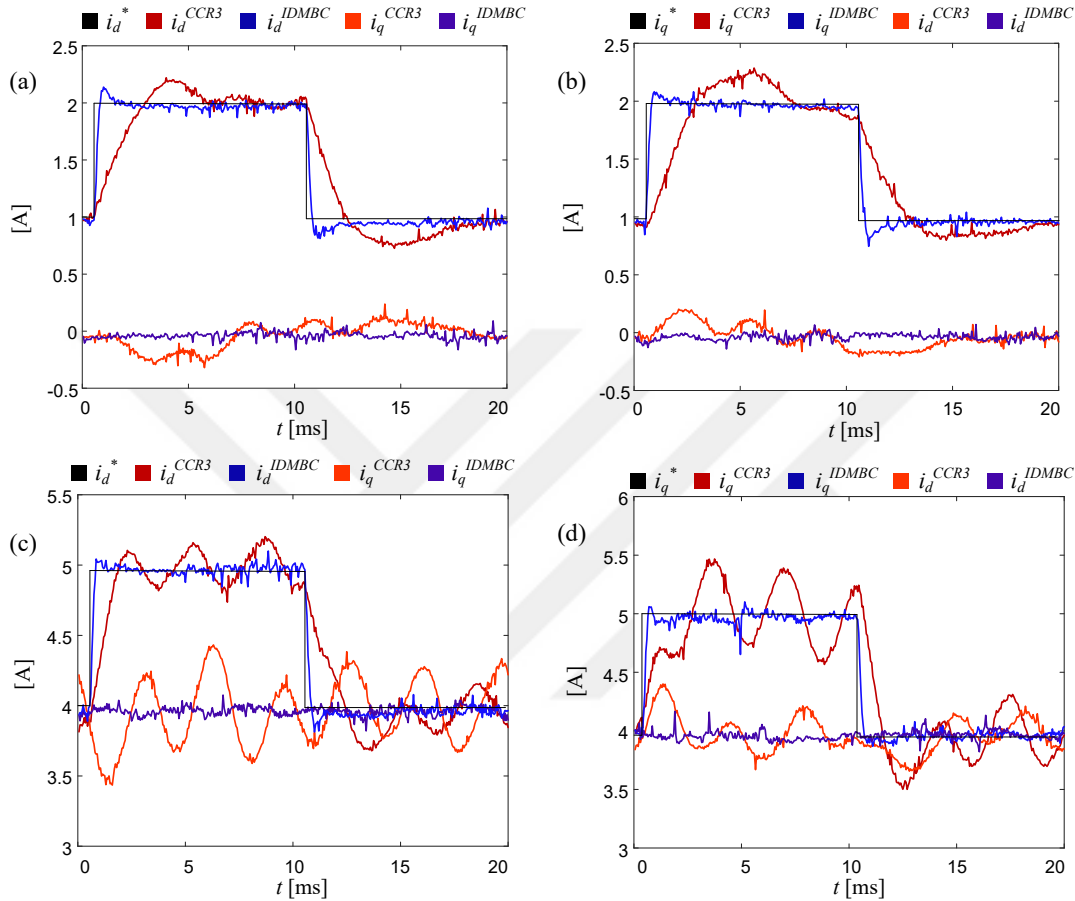


Figure 5.31: Experimental d-axis (or q-axis) step responses of CCR3 and IDMBC methods at various d-axis and q-axis DC-bias currents. (a) $i_d^* = 1A \rightarrow 2A \rightarrow 1A$ while $i_q^* = 0A$. (b) $i_d^* = 1A \rightarrow 2A \rightarrow 1A$ while $i_q^* = 0A$. (c) $i_d^* = 4A \rightarrow 5A \rightarrow 4A$ while $i_q^* = 4A$. (d) $i_d^* = 4A \rightarrow 5A \rightarrow 4A$ while $i_q^* = 4A$.

In Figure 5.31, d-axis and q-axis dynamic response waveforms are illustrated for two DC-bias current sets. In Figure 5.31(a) it is shown that the d-axis current command is increased from 1 A to 2 A while the q-axis command is kept 0 A. Besides illustration of dynamic response characteristics, the figure shows how perfectly the d-axis and the q-axis dynamics are decoupled from each other. For CCR3 method, it was discussed

that the rise time is quite long to consider the dynamic response a poor one. Besides, it should be observed that the q-axis current is not stationary but it deviates from its reference value indicating the imperfect decoupling of the CCR3 method. When the d-axis and q-axis currents are interchanged (Figure 5.31(b)) the same phenomena again appears in a similar way but distinct in sign with a reasoning that the cross-coupling terms have opposite signs. On the other, for both Figure 5.31(a) and (b), the IDMBC method exhibits superior cross-coupling decoupling performance as well as dynamic characteristics.

In Figure 5.31(c) and (d), the DC-bias level on both axes are set to 4 A. Then the d-axis (for Figure 5.31(c)) and the q-axis (for Figure 5.31(d)) current commands are increased to and decreased from 5 A. In these cases, even the 6th order harmonic blurs the decoupling effect it can be still identified that the decoupling is imperfect when the rise and fall regions of the waveforms are considered. Similar to the cases of Figure 5.31(a) and (b), the cases of Figure 5.31(c) and (d) illustrates the superiority of IDMBC method by means of dynamic response and cross-coupling decoupling performances. In the next, the waveform quality performances of the CCR3 and IDMBC methods are evaluated.

5.10.3 Waveform Quality

The waveform quality investigation of 3P3W VSC is performed both VSC+inductor terminals short-circuited and grid-connected configurations. The system parameters specified in Table-5.1 are utilized in the experiments. The inductor L-i characteristics are the same in Figure 2.11 The maximum bandwidth is designed to be $2\pi 500$ rad/s for both configurations.

In Figure 5.32, VSC+inductor terminals short-circuited inductor current waveforms are illustrated for CCR3 and IDMBC methods. The effect of the grid voltage in this configuration is minimal. The current THD of CCR3 method is 7.28 % whereas it is 2.28 % for IDMBC method. These waveform quality between the CCR3 and IDMBC methods are so much that they can be clearly seen just from the figure without THD calculation.

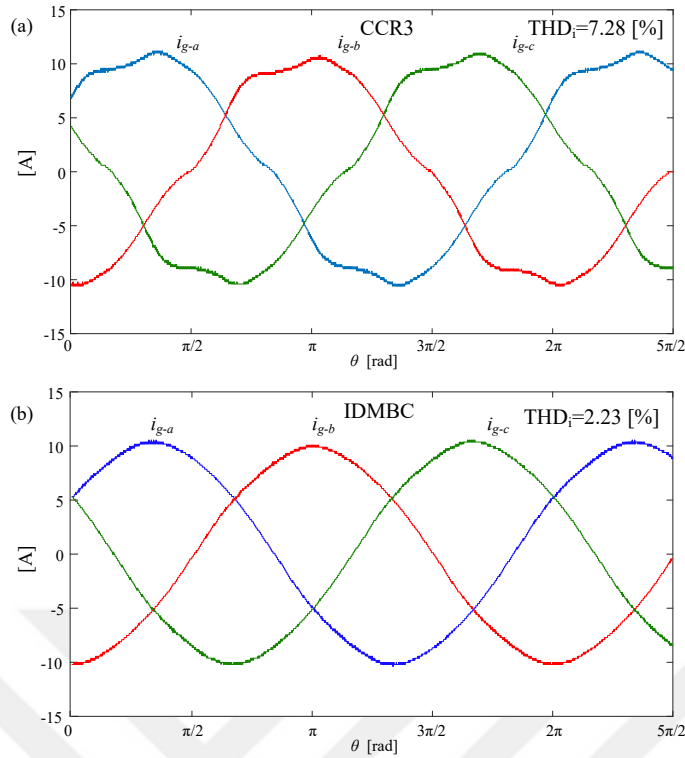


Figure 5.32: Experimental inductor currents of the three phases of CCR3 and IDMBC methods for the VSC+inductor terminals short-circuited configuration at full load. (a) Inductor currents of the three-phases for CCR3 method. (b) Inductor currents of the three-phases for IDMBC method.

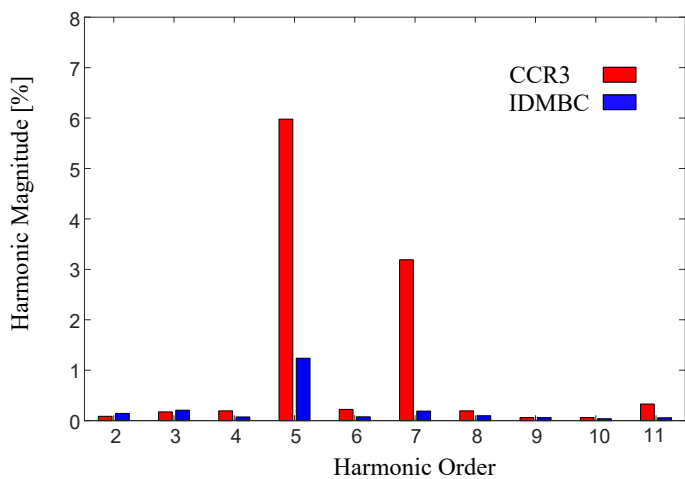


Figure 5.33: Experimental harmonic spectrum of the CCR3 and IDMBC methods near low frequency region for the VSC+inductor terminals short-circuited configuration.

In Figure 5.33, the low-frequency region harmonic spectra of the inductor currents of CCR3 and IDMBC methods are illustrated for VSC+inductor terminals short-circuited configuration (The harmonic spectra of Figure 5.32). For this configuration, the harmonic spectrum of IDMBC involves around 1 % of 5th harmonic. However, the CCR3 method has detrimental 5th and 7th harmonics.

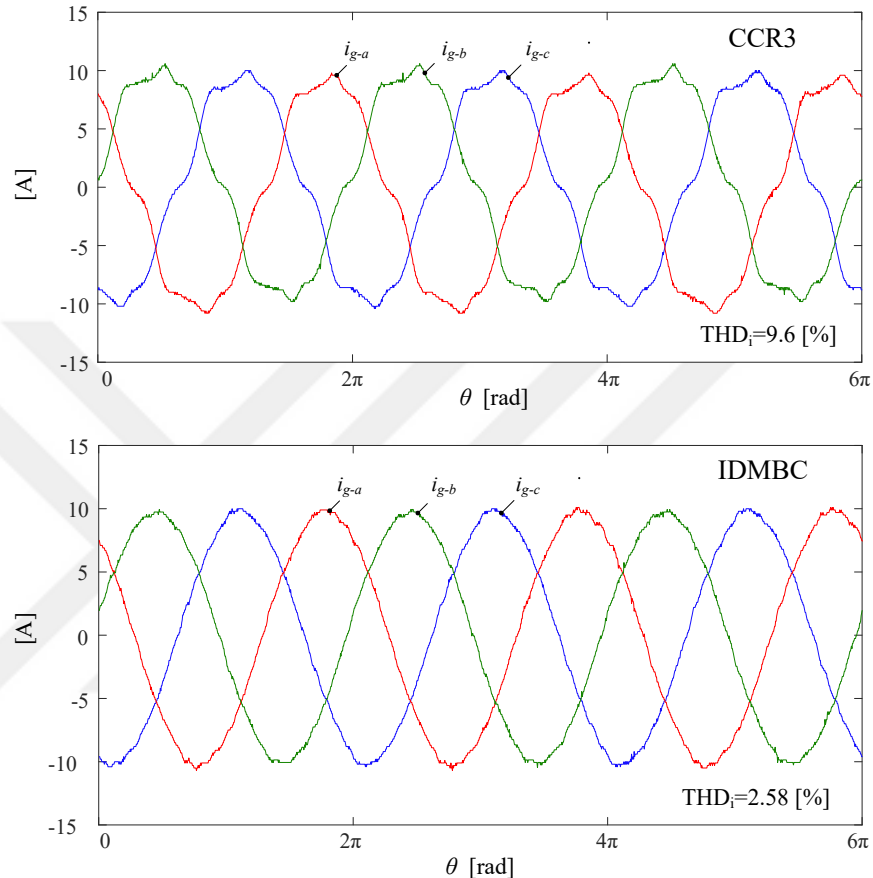


Figure 5.34: Experimental grid currents of the CCR3 and IDMBC methods for zero displacement angle at full load ($i_d^* = 10$ A, $i_q^* = 0$ A). (a) Grid currents of the three phases for CCR3 method. (b) Grid currents of the three phases for IDMBC method.

Following the VSC+inductor terminals short-circuited case, the grid-connected configuration is elaborated. Having synchronized via three-phase PLL and grid voltage decoupled, the grid current waveforms for zero displacement angle operation at full load (corresponding to $i_d^* = 10$ A, $i_q^* = 0$ A) is shown in Figure 5.34. The THD_i value for CCR3 method is measured to be 9.6 % and the THD_i value of IDMBC method is measured to be 2.58 %. The measured THD_i values in the grid-connected

configuration are slightly greater than their VSC+inductor terminals short-circuited configuration counterparts. Imperfectly decoupled grid voltage and higher PWM ripple current (and its distorting effect via control loop) can be listed as the reasons of such distinction.

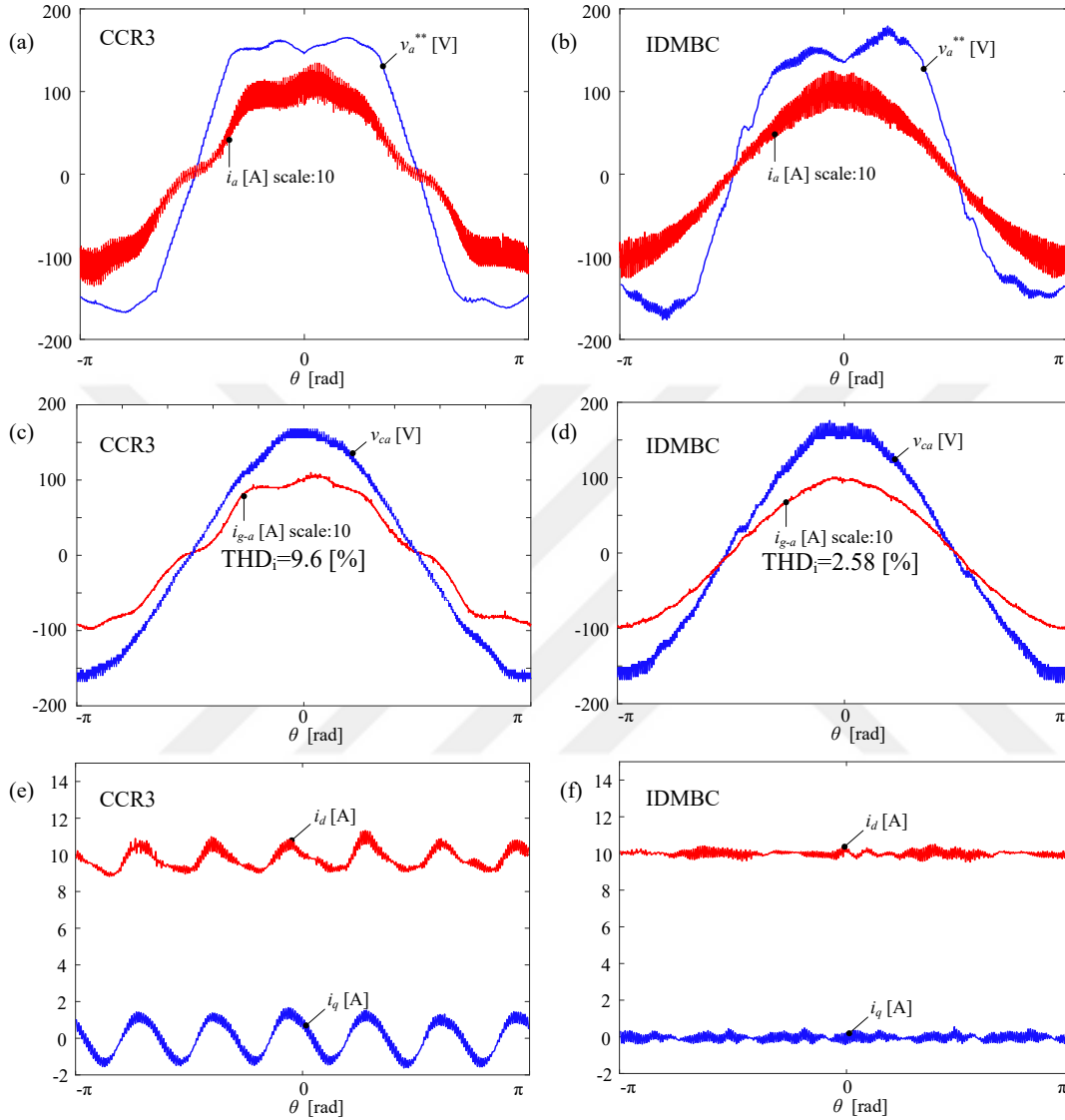


Figure 5.35: Experimental grid-connected 3P3W VSC waveforms for CCR3 and IDMBC methods at full load, zero displacement angle, and steady-state. (a) SVPWM output voltage command and converter side current for CCR3 method. (b) SVPWM output voltage command and converter side current for IDMBC method. (c) Output filter capacitor voltage and grid current for CCR3 method. (d) Output filter capacitor voltage and grid current for IDMBC method. (e) d-axis and q-axis currents for CCR3 method. (f) d-axis and q-axis currents for IDMBC method.

In Figure 5.35 the grid-connected 3P3W VSC system critical waveforms are illustrated at full load, zero displacement angle, and steady-state conditions. In Figure 5.35(a) and (b), the VSC output voltage, which belongs to SVPWM currently, and converter side phase-a inductor currents are depicted for CCR3 and IDMBC methods respectively. In Figure 5.35(c) and (d), the capacitor voltage and the grid current is shown for CCR3 and IDMBC methods respectively. The grid current waveforms show the effectiveness of the IDMBC method, while it can be inferred that CCR3 method can not be used in grid-connected applications for the current system parameters as the THD_i limit is exceeded that is set by the standards (5 % at most for this application at full load according to for instance IEEE 519).

In Figure 5.36, the harmonic spectra belonging to the grid currents shown in Figure 5.35 (and grid currents also shown in Figure 5.34) are illustrated. In the spectra, the zero-sequence current harmonics are minimal as there is no return path for these harmonics to flow. However, for CCR3 method, the 5th and the 7th harmonics flow in a considerable amount making the CCR3 method inhibitive for grid-connected applications with the current parameters. On the other hand, the IDMBC method provides acceptably low 5th and the 7th harmonic current magnitudes. Therefore, the IDMBC method can be employed in grid-connected applications with current control and circuit parameters.

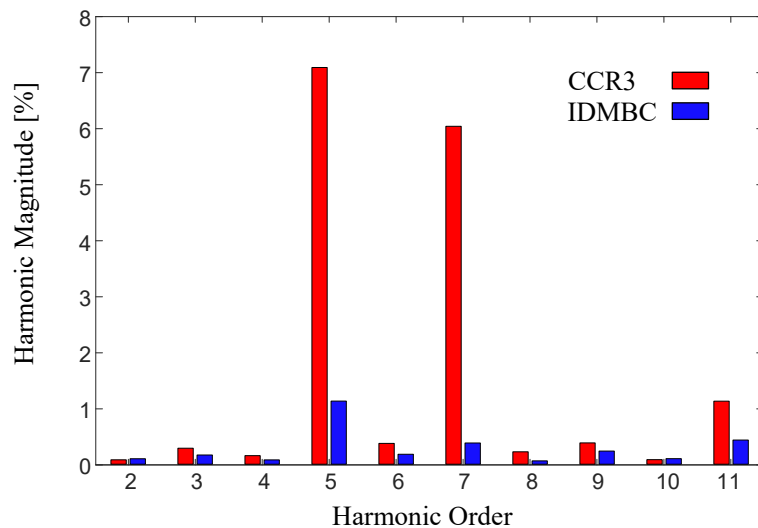


Figure 5.36: Experimental grid-connected system grid side current low frequency region harmonic spectrum for CCR3 and IDMBC methods with $\omega_{BW} = 2\pi 500$ rad/s.

In single-phase VSCs, it was shown that the system design bandwidth may improve grid-current waveform quality. Generally, it can be inferred that the higher the bandwidth of the system, the lower the harmonic distortion. In 3P3W VSC systems, the result is similar. In Figure 5.37, the THD_i and bandwidth relation is plotted for VSC+inductor terminals short-circuited and grid-connected configurations. Based on this experimental plot, it can be observed that the THD_i decreases with increased system bandwidth in general. For CCR3 method, the decrease is sharper while the decrease in the THD_i with the bandwidth increase is not that much for IDMBC method. However, the THD_i of IDMBC is always lower than the upper bound of the standard specifications. On the other hand, the CCR3 method is inapplicable for grid-connection even if the bandwidth is increased to 1.5 kHz.

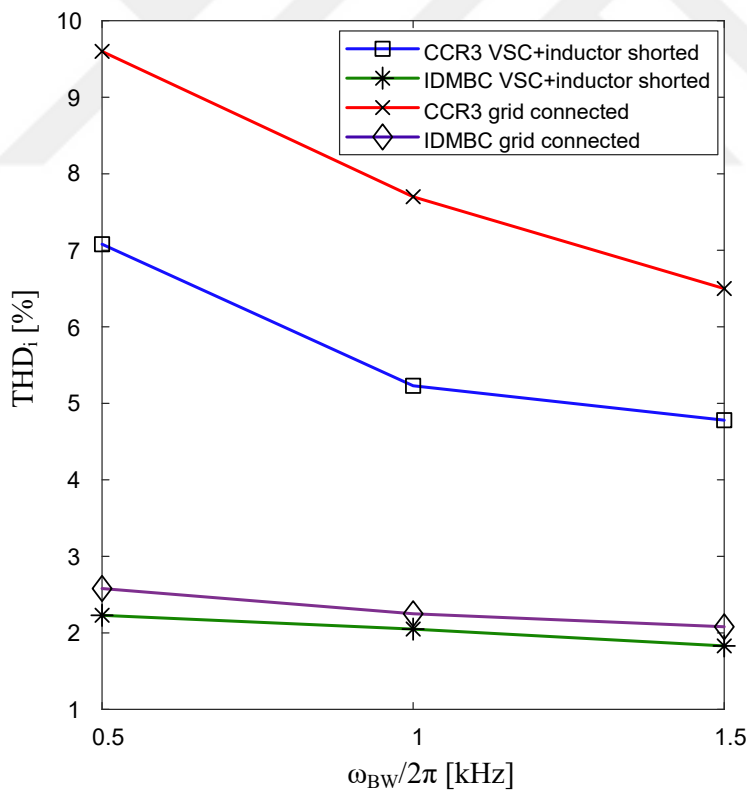


Figure 5.37: Experimental THD_i vs. current control bandwidth of CCR3 and IDMBC current control methods.

5.11 Summary

In this chapter, the IDMBC method is presented. First, it is shown that the balanced 3P3W VSC system approach of conventional current regulation is not valid when saturable inductors are employed. To be eligible to use the classical vector control, which is the industry standard in the control of linear balanced 3P3W systems, two-phase modelling of 3P3W system is performed. With this approach, the 3P3W VSC system is represented in a two-input two-output system manner to obtain correct system representation with independent state variables. After that, the inverse dynamic model of the nonlinear system is established so that the system becomes a unity-gain zero-phase one. An integral compensator and active damping schemes are incorporated to the linearized system so that a fictitious plant is obtained which behaves as a linear and balanced R-L load VSC system. Therefore, linear compensators can perform satisfactorily with desired control features within the design constraints. Accordingly, appropriate transformation for two-phase vector control is established. Furthermore, a two-phase modulation scheme is developed to enable the utilization of line-to-line voltage commands to obtain desired switching signals.

Following the establishment of the theory, frequency response characteristics of the CCR3 method and IDMBC methods are obtained by means of command to output and disturbance to output transfer functions. The magnitude and phase plots of command to output transfer functions verify analytically the bandwidth shrinkage drawback in CCR3 method. On the other hand, the IDMBC method preserves its bandwidth with changing system parameters. Furthermore, with disturbance to output frequency response characteristics, it is shown that the IDMBC method outperforms the CCR3 method in terms of disturbance rejection attributes.

Simulations are conducted to verify the analyses made, and to perform an assessment on the dynamic response and waveform quality aspects. The results obtained from the simulations of CCR3 and IDMBC methods show that the bandwidth of IDMBC method remains constant while the bandwidth of CCR3 method changes periodically, as in the case of 1P controlled VSC systems, with changing system parameters. Besides, the current quality of IDMBC method is far better than that of CCR3 method under same system and compensator parameters. These aspects of IDMBC method

make it highly preferable solution for bandwidth shrinkage and waveform quality issues of conventionally controlled current regulation systems with saturable inductors.



CHAPTER 6

CONCLUSION

Covering a wide range of application fields in large volumes, VSCs constitute the backbone of the industry. Therefore, reaching excellence in the VSC technology is (and should be) the main purpose by means of cost and volume reduction and energy-conversion efficiency enhancement at the same time performing a reliable operation. In accordance with such an objective, the VSC technology is developed and improved by means of semiconductor technology, PWM and control/optimization algorithms, output filter topology, and converter topology throughout the last half-century. The advancements in these branches have been quite rapid. While this is the circumstance, this thesis focused on the VSCs that employ saturable inductors, especially as the converter side inductors. Within the direction of this focus, the following outcomes are attained.

The state-of-the-art VSC technology is reviewed. This revision covered the semiconductor technology and its great impact on the VSC technology at first. Then, the establishment of advanced PWM, control, and optimization strategies are discussed. Furthermore, it is emphasized that with the aim of reducing the filter size, converter cost, and filter losses; converter and filter topologies expanded with an increase in the number of application types and requirements.

While the fundamental aim in the development of increasing the output voltage level and exploring new filter topology types is to reduce the filter size, cost, and filtering losses; such improvements are achieved in this thesis via the employment of saturable inductors, especially as converter side inductors. Accordingly, the theory of inductor saturation and the concept of incremental inductance are reviewed. The inductor technology in VSCs is also reviewed. Moreover, the motivations with the use of

saturable inductors (cost, size, and efficiency improvements) are discussed and exemplified. These discussions and associated outcomes demonstrated that utilization of the inductor in a saturated manner with dedicated core types, the core size and cost can be considerably reduced and inductor losses can be cut which are all desirable features for a VSC. It is also demonstrated that powder core materials are a very good candidate for saturable inductor cores with low core losses, smooth roll-off curves, great temperature stability, and ageing-proof features.

However, the improvements that can be gained with the use of saturable inductors do not come for free. Bandwidth shrinkage and waveform quality distortion are the fundamental issues in both single-phase and three-phase VSCs that arise with the utilization of saturable inductors with conventional current regulators. Accordingly, these regulators are reviewed both for single-phase and three-phase VSC systems and the problems are identified/demonstrated by means of analyses, simulations, and experiments. Based on the simulations and experiments, it is observed and can be inferred also that the current waveform distortion problems are not caused by the high-frequency PWM ripple due to decreased inductance value(s). Rather, the current waveform distortion problem is caused mainly by the low-frequency harmonics. Therefore, the conclusion that the waveform quality problem can be solved by control techniques is reached.

For single-phase VSC systems, the IDMBC method is developed first. The method employs the IDM of the system to yield a unity-gain zero-phase system. Further, the integral compensator is involved in this unity-gain zero-phase system to yield a fictitious plant with constant inductance. After that, the SCRD method is presented that decouples the resistive effects in the first place and then ending up with a fictitious constant inductance plant similarly. Having constant inductance plants, conventional current control techniques are incorporated which perform well with constant inductance systems.

Frequency response analyses on the command to output and disturbance to output are performed to compare the presented and existing techniques. Based on the command to output analyses, the proposed IDMBC and SCRD methods are found to be superior to CCR and K_p scheduling methods. However, the IDMBC method and SCRD

methods exhibit exactly the same characteristics by means of command to output characteristics as they both convert the nonlinear L-R plant into a constant inductance plant. Nevertheless, these two methods differ in disturbance to output characteristics. Based on these characteristics, IDMBC method is found to exhibit better disturbance mitigation features than SCR method. Therefore, the conclusion has been reached that IDMBC method is superior to other methods.

As the IDMBC and SCR methods require system parameters, L-R parameter identification methods are presented. The effect of parameter mismatch is also studied and it is observed that even a 20 % parameter mismatch with the presented methods performs better than CCR and K_p scheduling techniques.

The performance improvement with the proposed methods for single-phase VSCs is shown in comparison with the CCR and K_p scheduling methods by means of simulations. After that, experimental results indicating the dynamic response and waveform quality performances of the methods are provided. It is shown that proposed IDMBC and SCR methods have high performance over CCR and K_p scheduling methods and that IDMBC method exhibits better waveform quality characteristics than the SCR method due to better disturbance rejection characteristics. The current THD is approximately halved with the employment of the presented techniques when compared to single-phase CCR method for the same conditions. For a practical bandwidth of $2\pi 500$ rad/s the current THD values for CCR, SCR, and IDMBC methods are found to be 7.32 %, 3.77 %, and 3.43 % respectively. The results concerning the analyses, simulations, and experiments comply with each other and although they are specific to the overall system parameters, they provide a general insight into the performance of the presented techniques.

Having found the IDMBC method superior to other methods, it is generalized to perform for more than one phases. The generalization is demonstrated for 3P3W VSC systems. For this purpose, 3P3W VSC is modelled in a two-phase manner as the classical linear and symmetrical approach does not represent 3P3W VSC systems employing saturable inductors mathematically. Based on the two-phase modelling of the system, the inverse dynamic model is established. Accordingly, appropriate transformation for two-phase vector control is established. Furthermore, a two-phase

modulation scheme is developed to enable the utilization of line-to-line voltage commands to obtain desired switching signals.

Following the establishment of the theory, frequency response characteristics of the CCR3 method and IDMBC methods are obtained by means of command to output and disturbance to output transfer functions. The magnitude and phase plots of command to output transfer functions verify analytically the bandwidth shrinkage drawback in CCR3 method. On the other hand, the IDMBC method preserves its bandwidth with changing system parameters. Furthermore, with disturbance to output frequency response characteristics, it is shown that the IDMBC method outperforms the CCR3 method in terms of disturbance rejection features. The steady-state and dynamic response characteristics of the proposed methods are investigated in comparison with the existing methods via simulations and experiments. With high correlation to the analyses, the results show the suitability and superiority of the IDMBC method for the VSC systems employing saturable inductors. The improvement in the current quality is found more than the case of single-phase VSC. The grid-connected current THD is reduced from 9.6 % to 2.58 % for a practical bandwidth of $2\pi 500$ rad/s with the employment of IDMBC method. Such improvement can be attributed to that the 3P3W VSC systems may tolerate deeper saturation levels than 1P VSCs due to the balancing effect of the other phases.

As future work, saturable inductors can be employed as grid side inductors as well as converter side inductors. Such an approach may further improve the VSC performance by means of cost, size, and efficiency. Furthermore, distinct feedback configurations may be involved and associated control approaches may be established. Another application of saturable inductors can be distinct filter types. Further, online and robust parameter estimation methods can be elaborated to accompany the presented techniques in this study. It should also be noted that, the application of the use of saturable inductors may be extended to DC-DC and AC-AC converters as the basic power conversion rules applies to these methods in a similar manner that of the VSCs elaborated in this thesis. The current state of the investigation on saturable inductors and the aforementioned further research potential are expected to increase the utilization of the saturable inductors in the industry.

Considering the wide-spread and large-volume applications of current-controlled VSCs, the cost, size, and efficiency improvements that can be provided by the utilization of saturable inductors are quite significant. Therefore, this thesis work is expected to improve better utilization of world resources.





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ACADEMIC EXPERIENCE

Year	Place	Enrollment
2009 - 2018	METU Electrical and Electronics Engineering	Research Assistant

MEMBERSHIP/POSITIONS

1. 2010- IEEE Student Membership

RESEARCH INTERESTS

Power Converter Control

Power Converter Design

Grid-Connected Voltage Source Converters

FOREIGN LANGUAGES

Turkish (Native)

English (Advanced)

German (Basic)

PUBLICATIONS

Thesis

1. Z. Özkan, “Leakage Current and Energy Efficiency Analyses of Single Phase Grid Connected Multi-kVA Transformerless Photovoltaic Inverters,” M.Sc. Thesis, Middle East Technical University, Dept. of Electrical and Electronics Eng., Ankara, February 2012.

Patents

1. Z. Özkan “Dc/ac inverter to convert dc current/voltage to ac current/voltage”, US 2014/0078802 A1, 2014.

Journals

1. Z. Özkan and A. M. Hava, “Classification of grid connected transformerless PV inverters with a focus on the leakage current characteristics and extension of topology families,” J. Power Electron., vol. 15, no. 1, pp. 256–267, Jan. 2015.

2. Z. Özkan and A. M. Hava, "Current Control of Single-Phase VSC Systems with Inductor Saturation Using Inverse Dynamic Model-Based Compensation," *IEEE Transactions on Industrial Electronics*, vol. 66, pp. 9268–9277, Dec 2019.
3. Z. Özkan and A. M. Hava, "Inductor Saturation Compensation with Resistive Decoupling for Single-Phase Controlled VSC Systems," *IEEE Transactions on Power Electronics*, Early Access, 2019.

International Conference Papers

1. Z. Özkan and A. M. Hava, "Output ripple performance evaluation and comparison of 2L-VSI and 3L-VSI considering the spectral characteristics," 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Seoul, Korea, June 2015, pp. 397-404.
2. Z. Özkan and A. M. Hava, "DC-bus ripple current characterization of three-phase 2/3L-VSIs considering the spectral characteristics," 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Seoul, Korea, June 2015, pp. 667-674.
3. Z. Özkan, A. M. Hava, "Three-Phase Inverter Topologies for Grid-Connected Photovoltaic Systems," *IEEE-IPEC 2014 Conference*, May 2014, Hiroshima, Japan, pp. 498-505.
4. Z. Özkan, A. M. Hava, "Energy Conversion Efficiency of Single-Phase Transformerless PV Inverters," *ELECO 2013, 8th International Conference on Electrical and Electronics Engineering*, 28-30 November 2013, Bursa, Turkey.
5. Z. Özkan, A. M. Hava, "A Survey and Extension of High Efficiency Grid Connected Transformerless Solar Inverters with Focus on Leakage Current Characteristics," *IEEE-ECCE 2012 Conference*, September 2012, Raleigh, North Carolina, USA, pp. 3453-3460.
6. Z. Özkan, A. M. Hava, "Leakage Current Analysis of Grid Connected Transformerless Solar Inverters with Zero Vector Isolation," *IEEE-ECCE 2011 Conference*,

September 2011, Phoenix, Arizona, USA, pp. 2460-2466.

7. N. O. Çetin, Z. Özkan, O. B. Tör, “Arbitrage Opportunities between Energy, Bilateral Contracts and Ancillary Service Markets” 7th International Conference on Electrical and Electronics Engineering (ELECO 2011), 1-4 December 2011, Bursa, Turkey.

National Conference Papers

1. Z. Özkan, A.M. Hava, “Şebeke Bağlantılı 3-Faz FV Evirici Topolojilerinin Başarımlarının Değerlendirilmesi, / Performance Evaluation of Three-Phase Grid-Connected PV Inverter Topologies” YEKSEM 2013, Yenilenebilir Enerji Kaynakları Sempozyumu, 3-6 Ekim 2013, KKTC.

2. Z. Özkan, A.M. Hava, “Güç Elektroniği Dönüştürücülerinin Yarıiletken Veriyapılarına Dayalı Verim Hesaplama Yöntemi / Power Electronic Converter Efficiency Calculation Method Based on Semiconductor Datasheets,” ELECO 2012, Elektrik-Elektronik-Bilgisayar Mühendisliği Sempozyumu, 2-5 Aralık 2012, Bursa, pp. 460-464.

3. Z. Özkan, A.M. Hava, “Şebeke Bağlantılı Tek Fazlı Güneş Enerjisi Sistemlerinin Evirici Yapıları / Inverter Structures of Single-Phase Grid-Connected Solar Energy Systems” 3e Electrotech Magazine, no. 201, March 2011, pp. 78-84.

4. Z. Özkan, A.M. Hava, “Yüksek Verimli Trafosuz Güneş Eviricisi Yapıları / Highly Efficient Transformerless Solar Inverter Topologies” ELECO 2010, Elektrik-Elektronik-Bilgisayar Mühendisliği Sempozyumu, 2-5 Aralık 2010, Bursa, pp. 41-45.