RADIATION-AWARE ANALOG CIRCUIT AND LAYOUT DESIGN VIA AUTOMATED SIMULATION ENVIRONMENT

by

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ABSTRACT

RADIATION-AWARE ANALOG CIRCUIT AND LAYOUT DESIGN VIA AUTOMATED SIMULATION ENVIRONMENT

In today's world, there is an exciting increase in space research and applications due to new areas of interest such as space exploration and mining. Due to this interest, reliability of electronic circuits that work in the space environment has become a great concern for engineers and electronic circuit designers. In order to solve this problem, there are mainly two topics to handle, which are detecting the vulnerable areas of the circuits in the presence of radiation and radiation-hardening of circuits. In terms of the former topic, there have been some simulation applications and few commercial CAD tools. However, they are mostly standalone and hard to access. For this purpose, RadiSPICE is developed as a simple but useful tool to help engineers and designers in terms of radiation simulation. The tool is capable of running Monte Carlo simulations for permanent or temporary radiation events and creating sensitivity tables of the circuit on the circuit level. Furthermore, it is extended to simulate radiation effects including the substrate effect on the layout level. In order to show the performance of the tool, some analog and digital circuits were built and tested to observe the effects of radiation.

ÖZET

OTOMATİK SİMÜLASYON ORTAMI İLE RADYASYONA DUYARLI ANALOG DEVRE VE YERLEŞİM TASARIMI

Günümüz dünyasında, uzay keşfi ve madenciliği gibi yeni ilgi alanlarının ortaya çıkmasıyla birlikte uzay araştırmaları ve uygulamaları büyük bir ivme kazanmıştır. Bu artan ilgi nedeniyle, uzay ortamında çalışan elektronik devrelerin güvenilirliği, mühendisler ve devre tasarımcıları için önemli bir endişe kaynağı haline gelmiştir. Bu sorunu çözmek için ele alınması gereken iki ana konu bulunmaktadır: radyasyon etkisine karşı devrelerin hassas bölgelerinin tespiti ve devrelerin radyasyona karşı dayanıklı hale getirilmesi. İlk konuya çözüm olması amacıyla, bazı simülasyon uygulamaları ve birkaç ticari CAD aracı bulunmaktadır. Ancak, bu araçlar genellikle tek başına çalışmakta olup, güvenlik gibi nedenlerden dolayı erişim zorluğu yaşanabilmektedir. Bu ihtiyacı karşılamak amacıyla, mühendisler ve tasarımcılar için radyasyon simülasyonu konusunda yardımcı olabilecek basit ama etkili bir araç olan RadiSPICE geliştirilmiştir. Bu araç, kalıcı veya geçici radyasyon ışınımı olayları için Monte Carlo simülasyonları gerçekleştirebilir ve devre seviyesinde duyarlılık tabloları oluşturabilir. Ayrıca, aracın bir uzantısı, yerleşim düzeyinde substrat etkisini de dahil ederek radyasyon ışınımı etkilerini simüle edebilme özelliğine sahiptir. Aracın etkinliğini örneklemek için analog ve dijital devreler inşa edilip, radyasyon etkileri gözlemlenmiştir.

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LIST OF SYMBOLS

I	Current
R	Resistance
Si	Silicon
SiO_2	Silicon Oxide
V	Voltage
V_{GS}	Gate-to-Source Voltage
V_{th}	Threshold Voltage
σ	Standard Deviation

LIST OF ACRONYMS/ABBREVIATIONS

3D	Three Dimensions
BGR	Bandgap Reference Circuit
BSIM	Berkeley Short-channel IGFET Model
CMOS	Complementary Metal Oxide Semiconductor
MET	Multi Event Transient
SEE	Single Event Effect
SET	Single Event Transient
TID	Total Ionizing Dose

1. INTRODUCTION

Advancements in technology, especially in terms of space technologies, have paved the way for new explorations, advanced satellites and obtaining critical knowledge about the beginning of life. In this topic, electronic devices have crucial significance more than ever since they are amongst the primary tools used in these applications. However, there is a concerning problem that needs to be handled when the topic is the performance of electronic devices in space: radiation.

Radiation is simply the transmission of energy or particles from a source in space environment [1]. There are many highly energetic particles in space, such as protons and electrons, due to several factors such as the charge trapped in the magnetosphere, solar radiation and cosmic radiation [2]. While electronic devices are working in space, these charged particles may affect their performance and stability. Furthermore, it can be said that this effect can cause a temporary or permanent change in the performance parameters of the devices, which may lead to a catastrophic failure. An example could be the demise of the first communication satellite, Telstar-1. Telstar-1 had a catastrophic failure just after the launch caused by high-energy electrons in the radiation belts due to an exoatmospheric nuclear weapon test that was performed before [3].

The minimum dimensions of CMOS processes are getting smaller and smaller every year, which is a critical matter in terms of radiation effects, as smaller transistors are more sensitive to radiation. In this context, it is worth bearing in mind that while highly energetic particles have been mentioned to be harmful to electronic devices in space, as devices shrink, they become more susceptible to radiation effects overall. It comes to a point that even particles with lower energy can damage the circuitry, causing malfunctions, which raises concerns even more for the effects of radiation on sensitive systems.

Regarding radiation effects, it can be said that they are mainly divided into two parts which are Total Ionizing Dose (TID) and Single Event Effect (SEE) or Single Event Transient (SET) [4–6]. Single Event Effect (SEE) is a temporary effect, caused by a single highly energized particle hitting the circuit [7]. It can also be called Single Event Transient (SET) since it doesn't change any transistor parameter but rather it leads to an instant charge rising at nodes, temporarily altering the performance of the circuit. In contrast, Total Ionizing Dose (TID) is a permanent effect caused by the cumulative charge transfer of multiple particles hitting the circuit over a long time period. This cumulative effect causes charges to get captured in the $Si - SiO_2$ layer of transistors, which can alter transistor parameters such as threshold voltage.

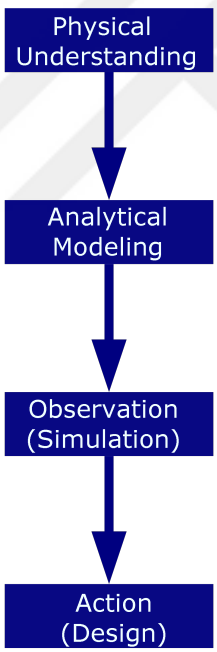


Figure 1.1: Steps of the reliability-aware design [1].

Similar to reliability-aware circuit design, radiation-aware circuit design also consists of four steps which are physical understanding, modeling, observation, and action, which can be seen in Figure 1.1 [1].

In terms of the first step, physical understanding, it can be said that radiation effects on electronic circuits have been investigated for many years which has allowed engineers to understand the accurate mechanism behind it. After this step, there is the modeling step, which means simulating the effect of radioactive particles on the performance of a circuit. With respect to this topic, there have been many successful radiation event models in the literature [8–10]. Furthermore, it is worth noting that there are also some models focusing on one effect such as SET [11] and TID [12–14] focused models.

After the steps of physical understanding and modeling are completed, the next step is observation, which means accurately showing the effects of radiation in a simulation environment utilizing the models from the previous step. In this topic, there have been efficient examples in the literature [15–19].

After conducting a detailed research on the literature, it can be said that many of the radiation effect simulations are focused on applications that are specific to each individual case. Furthermore, there are several commercial tools in the electronics industry, but they are hard to access because of cost and security reasons. In this context, the proposed tool RadiSPICE is an easy-access and easy-to-use, automated simulation tool that can help solve this problem. The tool has the features of conducting many statistical radiation simulations in a few seconds, performing simulations within a wide range of temperatures, which can be selected in the user interface and sensitivity analysis, which is very useful for revealing vulnerable areas of the circuit in the presence of radiation. In addition to the circuit level simulations, the tool has another part which operates in the Cadence environment, and it is capable of performing radiation simulations on substrate level and generating heatmaps for showing sensitive areas of the circuit. Demonstrations of these features on analog and digital circuits can be seen in the following sections.

2. BACKGROUND

As mentioned before, the radiation effect is primarily divided into two topics: TID and SET. Moreover, a helpful illustration can be seen in Figure 2.1, which shows the cross-sectional view of a transistor in the presence of radiation.

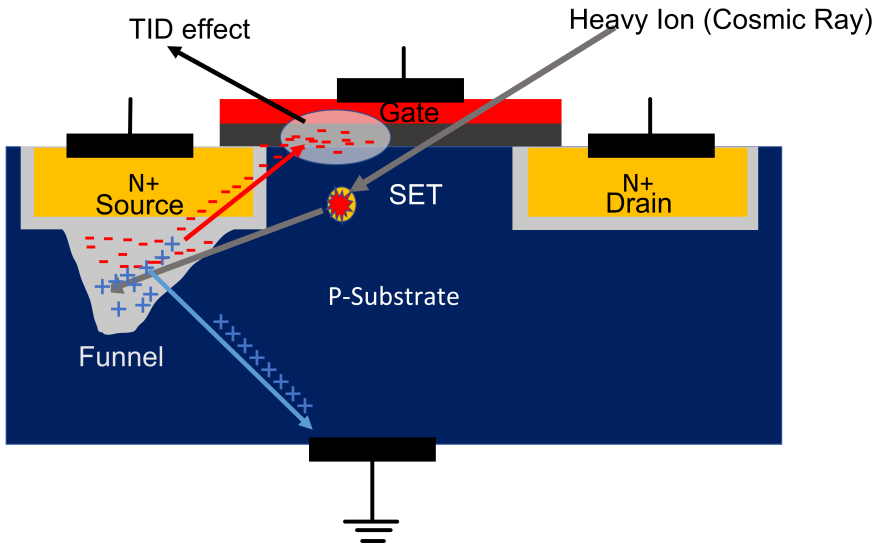


Figure 2.1: Illustration for the radiation effect on a transistor [1].

2.1. Total Ionizing Dose

Total Ionizing Dose (TID) can be simply defined as the cumulative effect of multiple highly energized particles, and it causes a permanent change in the parameters of transistors. Furthermore, it can be said that these ionized charges cause the generation of electron-hole pairs while they are passing through the substrate [1]. In addition, charges getting captured by the traps that already exist in the $Si - SiO_2$ interface can cause a shift in the threshold voltage of the transistor [20]. Due to this shift, circuit performance parameters can change significantly [19, 21].

2.2. Single Event Effect

Single Event Effect (SET) can be defined as the temporary change in a circuit caused by a single charged particle. Moreover, this effect is primarily caused by cosmic rays, including high-energy protons and heavy particles [22]. A helpful visualization of this effect can be seen in Figure 2.1. The principle behind the SET effect is that a single heavily charged particle hits the circuit and transfers a portion of its charge to the circuit. In addition, this charge affects mostly off-transistors and may lead to an increase in leakage currents or node voltages [3]. Since this effect is temporary, it is also called "soft error", meaning that most circuits can recover from that effect on their own. However, the timing of the event is critical since with the specific timing, it can alter the circuit's transient response drastically, which may lead to failures in logic circuits such as comparators [23–28]. A common method for simulating this effect is using a double-exponential current pulse, which can be seen in Figure 2.2 [29].

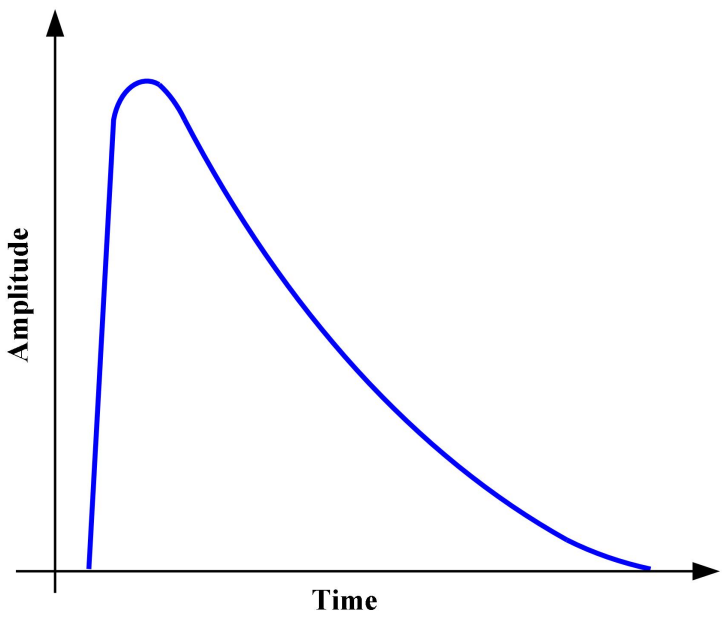


Figure 2.2: Double-Exponential Current Pulse used for simulating the SET effect [1].

The calculation formula for the amplitude of the double-exponential current pulse can be expressed as

$$Q_{tot} = I_{peak} \left[t_1 + t_2 + (td_2 - td_1) - t_1 e^{-(td_2 - td_1)/td_1} \right], \tag{2.1}$$

where t_{d1} is the onset of the rise current, t_{d2} is the onset of the fall current, t_1 is the rise time constant, t_2 is the fall time constant, I_{peak} is the peak current amplitude, and Q_{tot} is the total charge delivered by the current pulse [11]. Furthermore, the value of the transferred charge can be estimated as a Gaussian distribution where $\mu = 0.25\ pC,\ \sigma = 0.02\ pC$. During the simulation tests in the following sections, the rise time is chosen as 1 ns, while the fall time is chosen as four times slower than the rise time [23].

2.3. Substrate Modeling

Substrate modeling is an important topic in terms of simulating radiation effects since charged particles interact with the substrate of the transistors when they hit the circuit. In this topic, there have been many studies in which a significant number focused on combining multiple substrate effects into a single substrate resistance, which simplifies things very well, especially in terms of running simulations [30–34].

After interpreting the papers, including the comparisons of multiple and single substrate resistance networks, it was decided that the substrate mesh for representing the wells of the transistors would be built using a 1-R substrate resistance network. The reason for this decision is that the substrate resistance effect is negligible at low frequencies and the approximation is well enough for obtaining a critical simulation speed boost, especially when hundreds of simulations are needed to be performed [33].

3. A RADIATION SIMULATION SOFTWARE: RADISPICE

3.1. Circuit Level Simulations

RadiSPICE [35] is built on MATLAB® using the App Designer tool which helped design a user-friendly interface that can be used by anyone with a related or unrelated background. Furthermore, the tool is fully integrated with SPICE, and HSPICE® is used as a circuit simulator, and CosmosScope® is used to view the waveform of the output. The user interface and the features of the tool can be seen in Figure 3.1 and the working principle of the tool for both Single Event Effect (SET) and Total Ionizing Dose (TID) can be seen in Figure 3.2. As it can be clearly seen in the figure, TID is simulated using voltage sources, and SET is simulated using double-exponential current pulses.

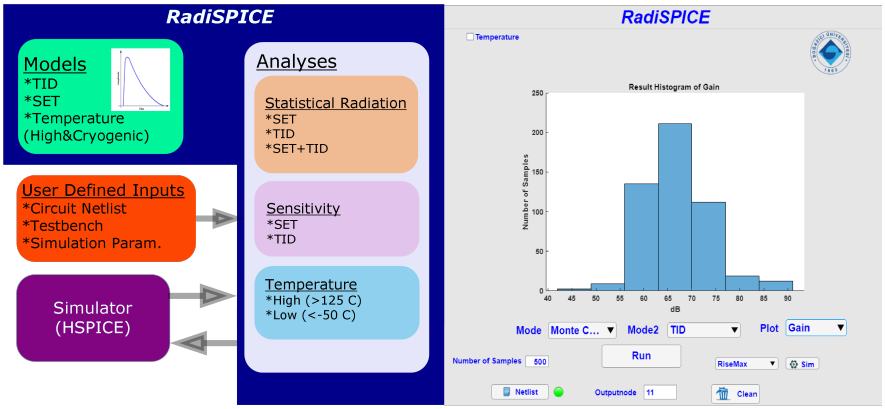


Figure 3.1: The overall layout and user interface design of RadiSPICE [1].

RadiSPICE takes the netlist of the design-under-test (DUT) circuit and arranges it in a way to conduct overall simulations for the TID and SET effects or sensitivity simulations in which individual transistors or nodes are tested for TID or SET radiation effects, respectively.

As overall simulations should include randomness to make them more realistic, it is done using the Monte Carlo method. Furthermore, it is worth noting that the temperature of the simulation environment can be changed in the user interface, which allows the user to run high temperature or cryogenic simulations. Therefore, the user just needs to select the temperature, the number of simulation points, and the simulation type, which can be SET, TID, or both effects combined.

One thing that should be considered is that RadiSPICE is capable of conducting radiation effects under extreme conditions as long as specific models are provided to the tool as it includes the BSIM models in default settings which are suitable for temperatures between -55 °C and -125 °C [36].

In terms of Single Event Effect (SET) simulation, as mentioned before, the user can set the simulation temperature and the number of simulation points and then select SET simulation type in which many Monte Carlo simulations are executed in the background. To simulate the overall SET effect in real life, the tool adds double-exponential current pulses with random amplitudes and event durations in a predefined range to all nodes in the circuit as it is shown in Figure 3.2. Moreover, a useful feature is that the tool has a scope option which can be used to observe the output waveform.

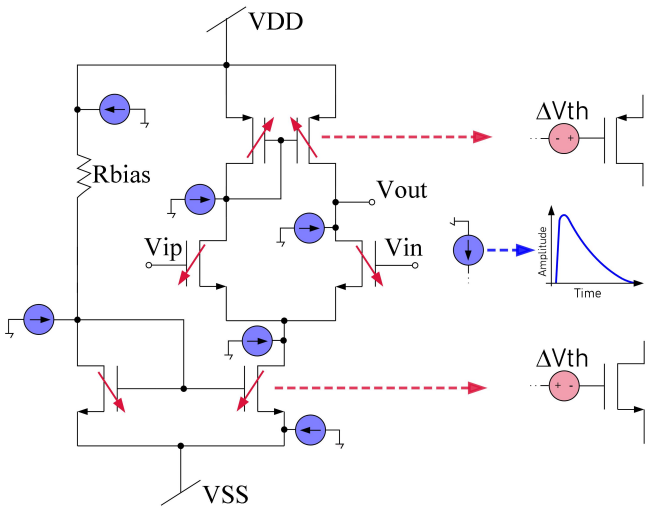


Figure 3.2: Modified schematic for the radiation simulations [1].

In order to test and observe the Single Event Effect, a D-latch circuit has been designed and tested by using RadiSPICE and the circuit can be seen in Figure 3.3. By looking at the results in Figure 3.4 which shows before and after the SET effect, it is clear that the SET effect can cause a glitch or bit flip at the output.

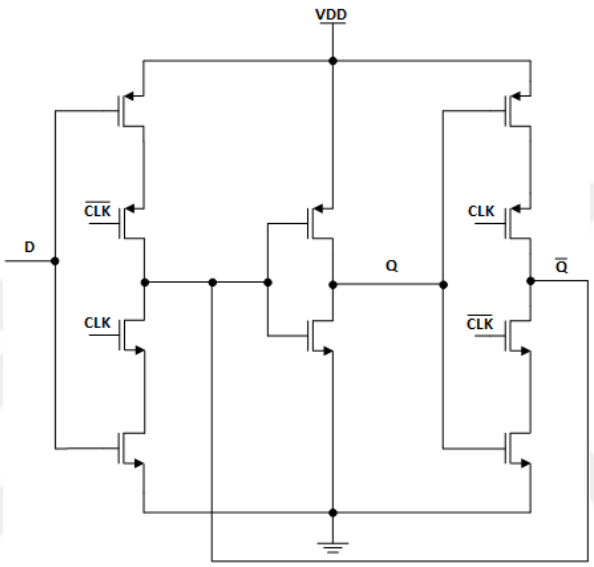


Figure 3.3: Schematic of the D-latch circuit [1].

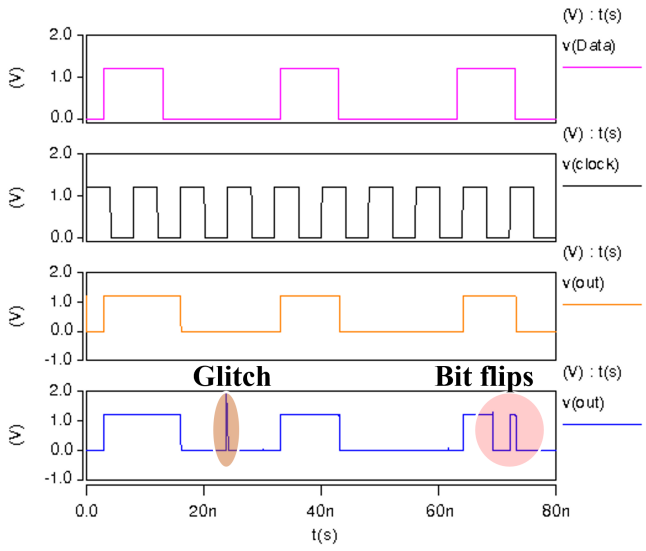


Figure 3.4: Transient simulation output before and after the SET effect [1].

On the other hand, since the TID effect is responsible for permanent changes in the transistor, a DC voltage source is used to emulate the permanent change in threshold voltage which can be seen in Figure 3.2. Furthermore, it should be noted that the DC voltage value of the voltage source is changed for each case in the Monte Carlo analysis. Finally, in order to observe the Total Ionizing Dose effect on the circuit, circuit performance parameters such as Gain and Power are represented on a histogram plot inside the tool.

In terms of radiation sensitivity, the sensitivity analysis for the SET effect focuses on each node individually by adding only one double-exponential current pulse to the specific node and measures the voltage change at the output after the simulation is completed. Likewise, the sensitivity analysis for the TID effect focuses on each transistor individually by adding one DC voltage source to the specific transistor and measures the performance parameters of the circuit after the simulation. In the end, a sensitivity table is created which has a different structure for different cases.

For instance, the sensitivity table for the TID effect on amplifiers shows gain change and output voltage change while transistors are sorted according to the relative sensitivity parameter which is created by giving 100 percent to the transistor that is responsible for the largest gain change and comparing the other transistors' values to the largest value. On the other hand, the sensitivity table for the TID effect on Bandgap circuits shows the current and output voltage change parameters while relative sensitivity is calculated based on current change values. Moreover, the sensitivity table for Logic circuits shows offset change percentage and calculates relative sensitivity based on this parameter.

Continuing with the next step which is testing overall TID effect and TID sensitivity, a folded cascode amplifier is built as it can be seen in Figure 3.5. After selecting the simulation count as 500 and selecting the TID option in the tool, the tool successfully measured gain, power and gain bandwidth product which can be seen in different histograms.

By looking at Figure 3.6, it can be said that gain changes critically which is because of the TID effect. After that, TID sensitivity simulation is completed and results are shown in Table 3.1 which clearly indicates that M3 and M4 transistors are responsible for the largest change in gain.

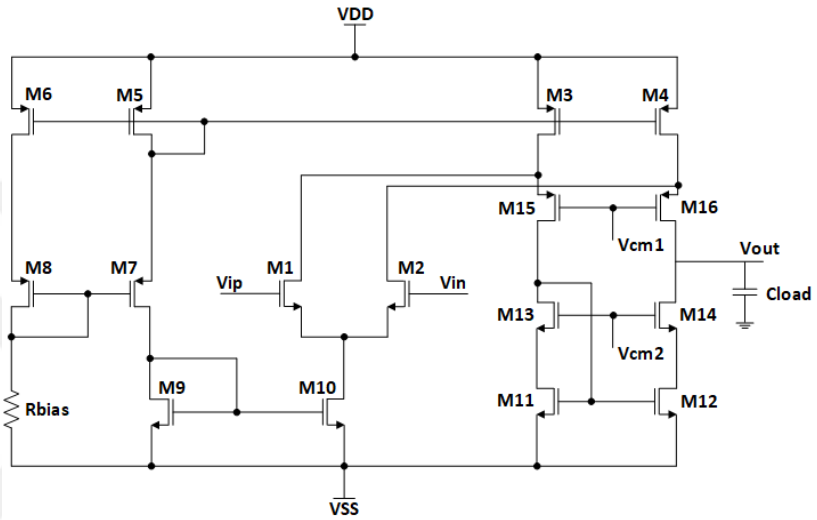


Figure 3.5: Schematic of the Folded Cascode Amplifier [1].

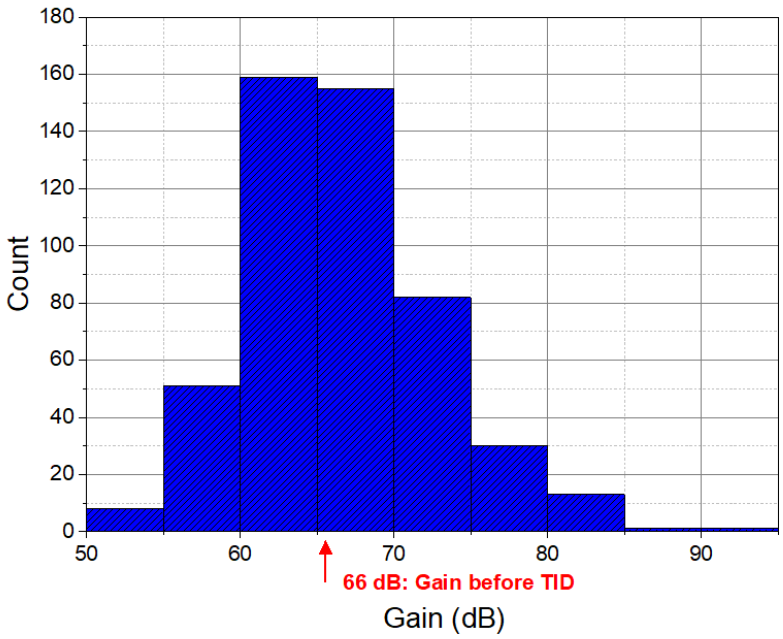


Figure 3.6: TID Sensitivity Histogram showing the gain change [1].

Table 3.1: TID Sensitivity Table of the FCA [1].

Transistor	Relative Sensitivity	Gain Change (%)	Output Voltage Change (%)
M3	100	6.10	0.022
M4	83.44	5.09	0.026
M11	72.73	4.44	0.015
M10	61.65	3.76	1.356
M9	33.09	2.02	1.377
M16	26.41	1.61	0.361
M12	22.67	1.38	0.002
M6	18.99	1.16	2.326
M5	13.93	0.85	2.319
M13	10.15	0.62	0.001
M2	3.25	0.20	2.025
M1	2.27	0.14	2.026
M15	0.61	0.03	0.355
M14	0.07	0.004	0.0001
M8	0.05	0.003	0.010
M7	0.03	0.002	0.003

In the following sections, we focus on two circuit topologies in order to test all features of RadiSPICE and show how to use it for radiation-hardened circuit design. Selected topologies are a bandgap reference circuit and a comparator.

3.1.1. Bandgap Reference Circuits

Bandgap reference circuits are critical blocks in electronic circuit design since they are responsible for providing stable bias currents and reference voltages.

It is very important because of the fact that bias currents and reference voltages are assumed stable while designing many circuits, and errors in reference circuits can lead to a catastrophic failure in the main circuit.

Although there are different topology examples for reference circuits, they are commonly self-biased and have multiple operating points. An example topology can be seen in Figure 3.7 which has two operating points [37]. Firstly, there could be enough current flow in two branches which leads to the formation of the loop in which the voltage drop on the resistor is equal to the V_{GS} of M_1. In this situation, operating point becomes the point A as in Figure 3.7 (b). Moreover, there is another case named *zero current condition* where there aren't any current flows in both branches which means the voltage drop on the resistor and the V_{GS} of M_1 are both zero volts. Operating point B is an undesired condition and it can be caused by many factors including the radiation effect. In this topic, startup circuits are utilized in order to prevent the circuit from operating at the point B [37].

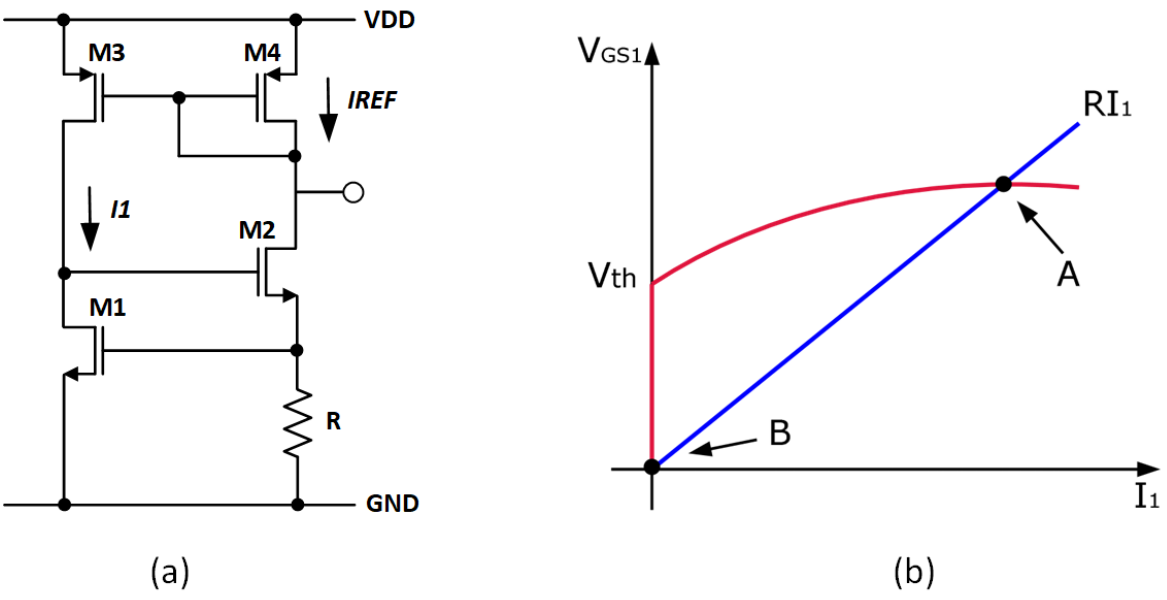


Figure 3.7: A self-biased current reference circuit example: (a) schematic of the circuit, and (b) graph of operating points [1].

In terms of startup circuits, it can be said that they are mainly divided into two types which are dynamic startup circuits and static startup circuits. The working principle of dynamic startup circuits is that they are active only at the power-up of the circuit at the beginning. After that, they don't work actively which means they don't consume any power which is a desired feature. In contrast, static startup circuits are known for non-stop monitoring of the circuit. They intervene if the currents in some branches lead to the operating point B, "Zero Current Condition". Although they are very helpful for stable circuit operation, they have one major disadvantage which is high power consumption because of the fact that they are always active. Hence, they are usually utilized when stability and reliability is the most important parameter in the design process such as radiation-hardened circuit design.

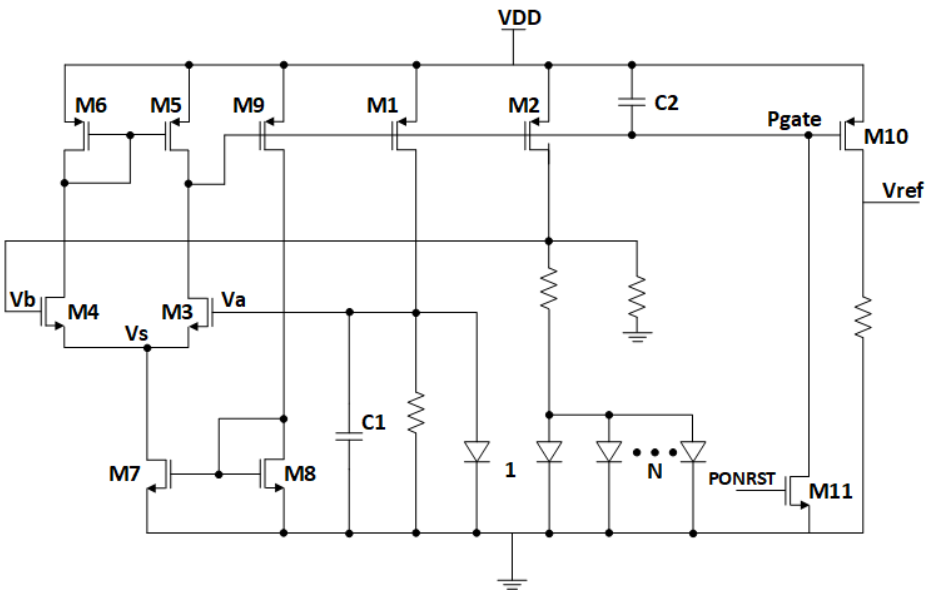


Figure 3.8: An example for low-voltage bandgap reference circuits [1].

In order to show radiation effects on bandgap reference circuits and the difference between dynamic and static startup circuits, a commonly used self-biased bandgap reference circuit [38] is built using the 180 nm CMOS process and then tested with RadiSPICE. The schematic of the circuit can be seen in Figure 3.8 and the working principle of this circuit is that there is a differential amplifier on the left side which makes sure that the voltages at the point "Va" and the point "Vb" are equal.

Furthermore, it creates the loop which is crucial for a reference voltage to appear at the "Vref" node.

At the right bottom of the schematic, we can see the M11 startup transistor with the gate signal named "PONRST" which is the power-on reset signal. This signal is responsible for pulling down the gates of the current mirror transistors which starts the loop and prevents the circuit from operating at "Zero Current Condition". After that, the signal becomes low and stays at that value while the main circuit is actively working which provides a stable reference voltage at the "Vref" node.

Initially, the Single Event Transient effect is tested on this reference circuit by using RadiSPICE. Looking at Figure 3.9, it is clear that Vref goes to zero after the radiation effect, which is a catastrophic failure. The reason for this failure is that a negatively charged particle hits the node "Va", then the voltage at this node goes to negative values causing the output voltage to go to the maximum value which is the positive supply voltage. Because of this, bias currents go to zero which leads to the "Zero Current Condition". Other examples can be seen in [39–41].

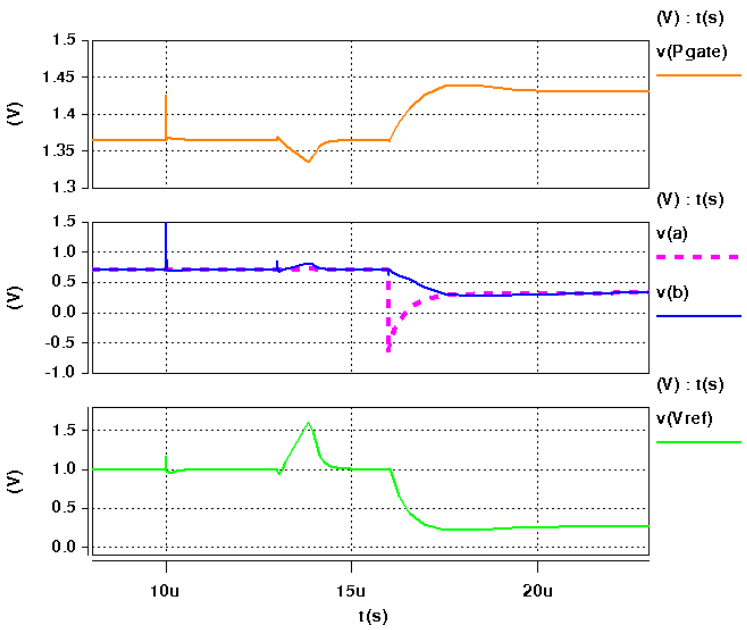


Figure 3.9: Output graph of the bandgap circuit showing a catastrophic failure [1].

The next step is testing the TID sensitivity of the bandgap reference circuit which can be seen in Table 3.2. Looking at the table, we can see the sensitivity of the transistors based on current and output voltage change. Furthermore, it can be said that M2 and M10 are the most sensitive transistors in terms of output voltage change and M2 is the most sensitive transistor in terms of current change. Furthermore, looking at the table carefully, it is worth noting that transistors which have negative current sensitivity are critical for failure possibility since a decrease in the bias current caused by negatively charged particles can lead to the "Zero Current Condition".

Table 3.2: TID sensitivity table of the simulated bandgap circuit [1].

Transistor	Relative Sensitivity	Current Change (%)	Output Voltage Change (%)
M2	100	-4.21	-12.32
M5	82.3	-3.47	-3.21
M3	82.1	-3.46	-3.2
M4	81.6	3.44	3.17
M6	81.1	3.42	3.15
M1	80.6	3.4	3.13
M9	0.93	0.04	0.04
M8	0.73	0.03	0.03
M7	0.64	-0.02	-0.02
M10	0.03	-0.001	9.3

The results of the first tests clearly indicate that a dynamic startup is not enough in order to prevent the catastrophic failure caused by the Single Event Transient effect. In the second test, the dynamic startup circuit is changed with a static startup circuit and the same tests are conducted again in the same conditions. The schematic of the new circuit can be seen in Figure 3.10 and the results can be seen in Figure 3.11.

Looking at the results reveals that the static startup circuit solves the problem by interfering since static startup circuits constantly monitor the circuit for the changes in the bias current. Finally, it is clear that the startup circuits have a critical effect on bandgap reference circuits in terms of the Single Event Transient effect.

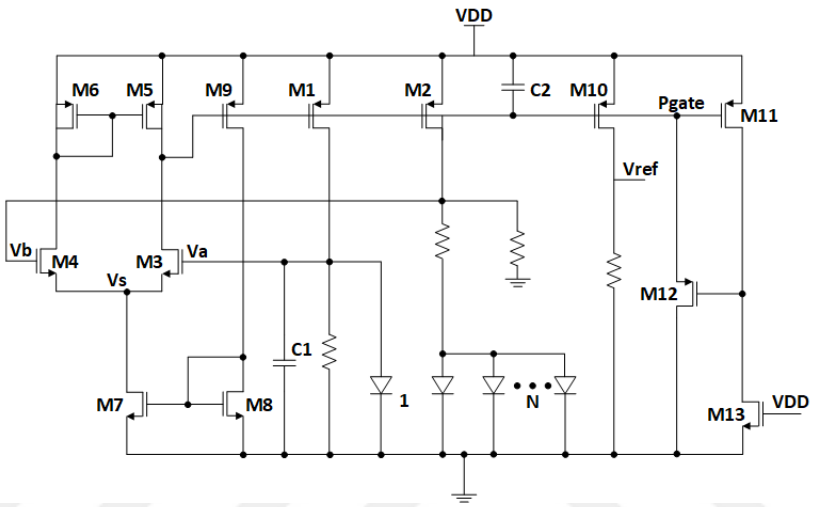


Figure 3.10: New bandgap reference circuit where the dynamic startup circuit is changed with a static one [1].

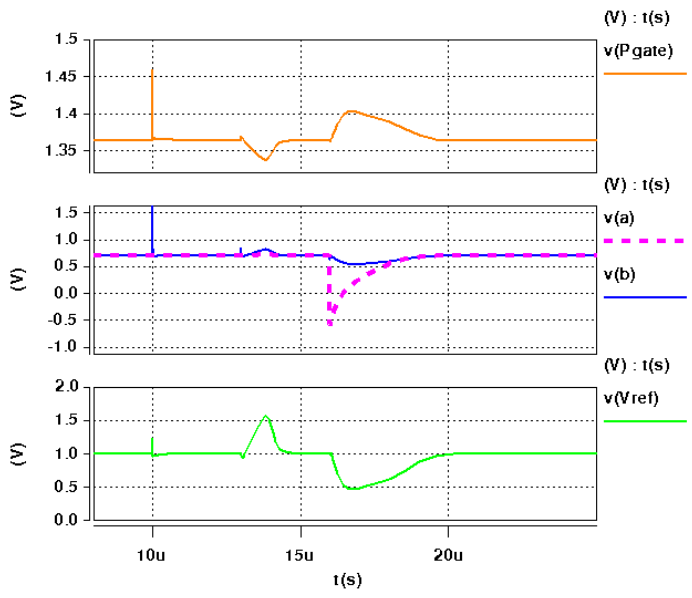


Figure 3.11: Output graph of the second test verifying the advantage of using the static startup circuits [1].

Another case is when a bandgap reference circuit gets hit by not a single but multiple charged particles causing a permanent effect which is called TID effect. In order to observe this effect, a TID simulation is carried out by utilizing RadiSPICE and the results can be seen in Figure 3.12. The result histogram reveals that the output voltage can change critically due to the TID effect with $\sigma = 0.313$ V, which is crucial knowledge that would help electronic designers in order to improve the radiation robustness of the circuit.

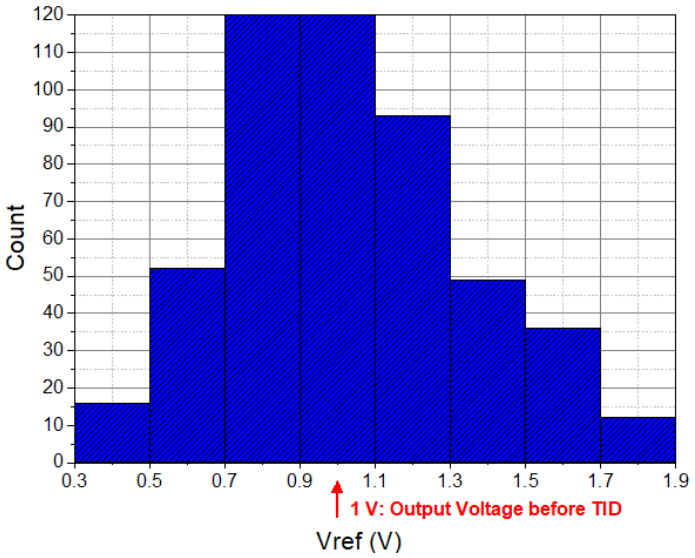


Figure 3.12: Output voltage histogram of the bandgap reference circuit after TID effect [1].

3.1.2. Comparators

Moving on with examples, the second test group consists of two comparator circuits which are built in 65 nm process and tested for radiation effects via RadiSPICE.

The first comparator is called the "CMOS Static Latched Comparator" [42], and the schematic of the circuit can be seen in Figure 3.13. The working principle of this comparator is that it includes two cross-coupled pairs which are responsible for maintaining the latched voltage while the clock is low.

As usual, the output becomes high when V_{in} is bigger than V_{ref} and vice versa. After conducting the TID test via RadiSPICE, it can be seen that the permanent effect of radiation on the transistors can lead to a critical offset which is not acceptable. The result histogram can be seen in Figure 3.14 in which $\sigma = 26.9$ mV.

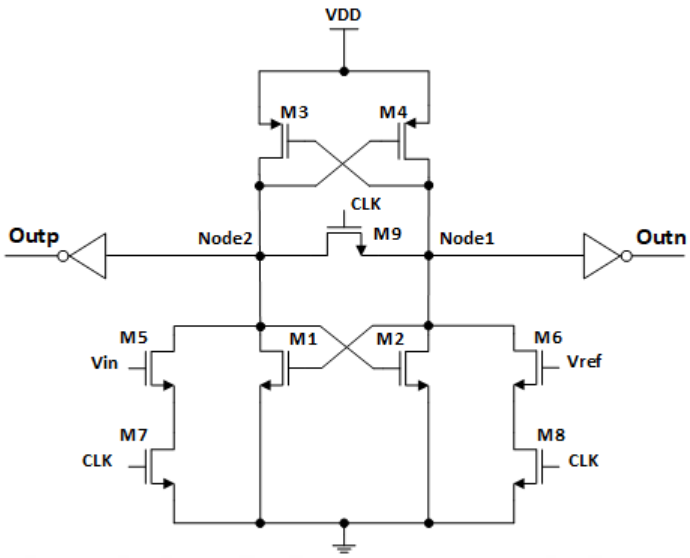


Figure 3.13: Schematic of the CMOS Static Latched Comparator [1].

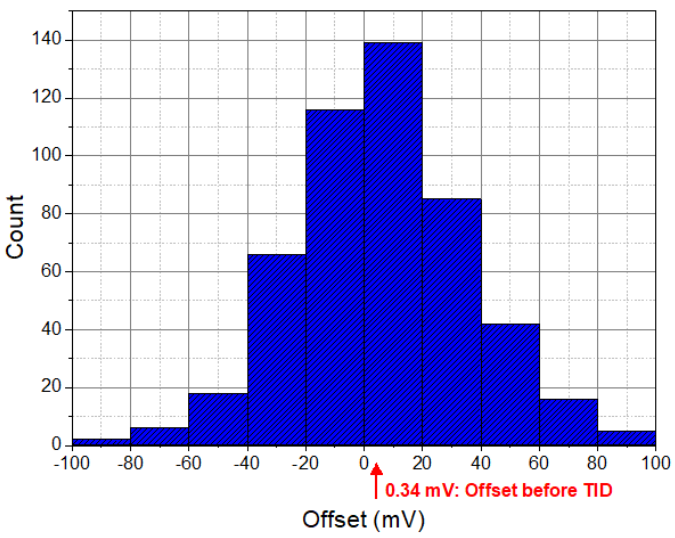


Figure 3.14: Offset histogram showing the TID effect on the comparator [1].

Another test that was done on this comparator is a SET test that is useful for observing the effect of radiation in transient analysis. Results can be seen in Figure 3.15 and it is clear that even a single charged particle can create false pulses in the output node which is crucial especially considering the difference between V_{in} and V_{ref} is not very small.

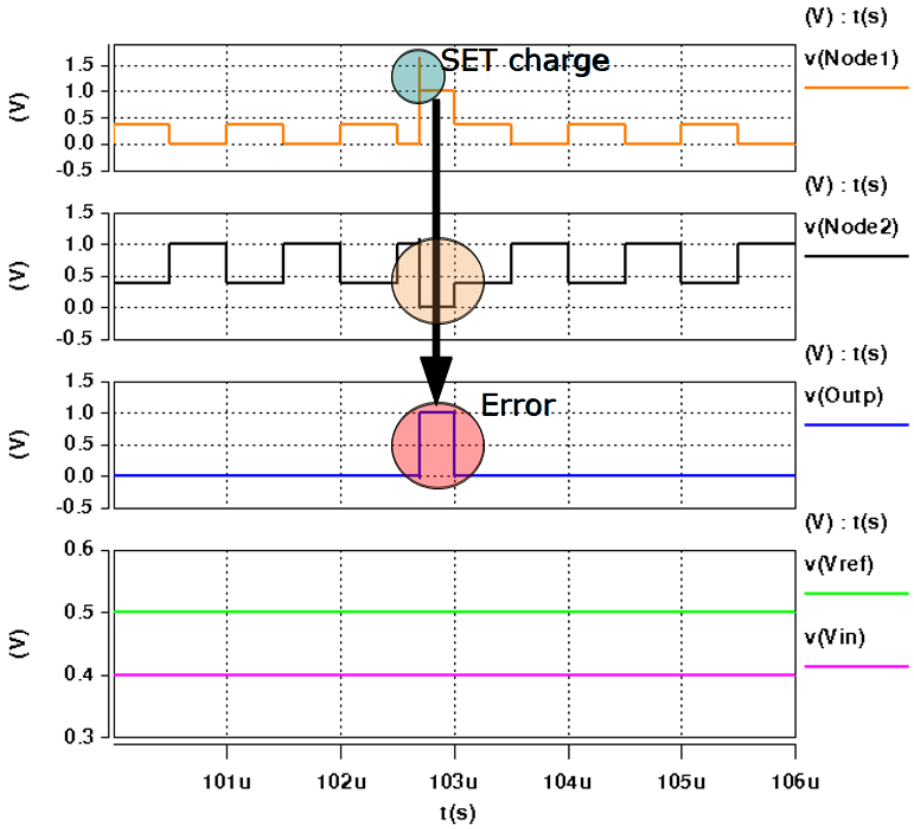


Figure 3.15: Transient graph of the SET test [1].

The second comparator is the "CMOS Dynamic Latched Comparator", which is commonly known as the "Strong Arm Latch Comparator" [43]. The schematic of the circuit can be seen in Figure 3.16 and it has two cross-coupled pairs in order to maintain the latched voltage, similar to the CMOS Static Latched Comparator. However, this time the circuit maintains the latched voltage while the clock is high. After building the circuit using 65 nm CMOS process and verifying that it works as expected, the TID test is conducted on the comparator via RadiSPICE.

The results can be seen in Figure 3.17 and again the crucial effects of TID can be seen on the offset histogram where $\sigma = 14.7$ mV. Looking at the results of both comparators, it can be said that the CMOS Strong Arm Latch Comparator is more robust against the TID effect while the offset change is still not acceptable for stable operation.

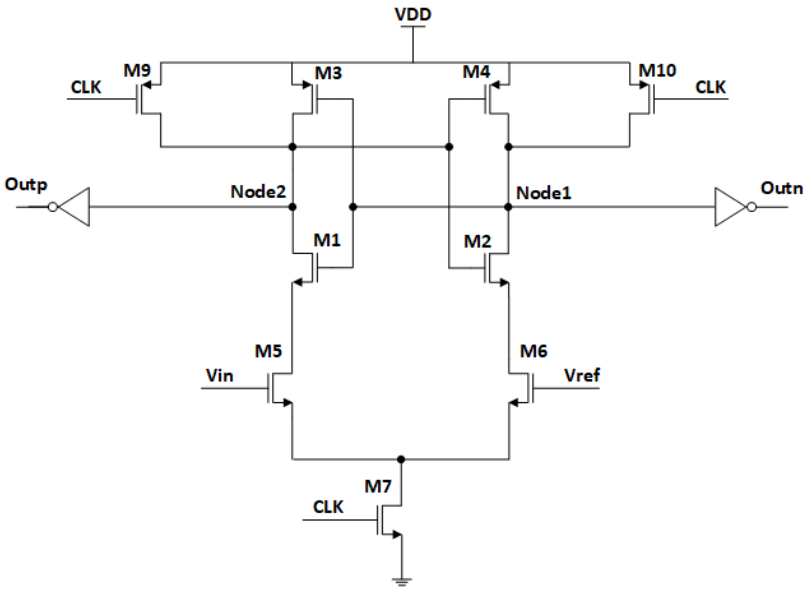


Figure 3.16: Schematic of the Strong Arm Latch Comparator [1].

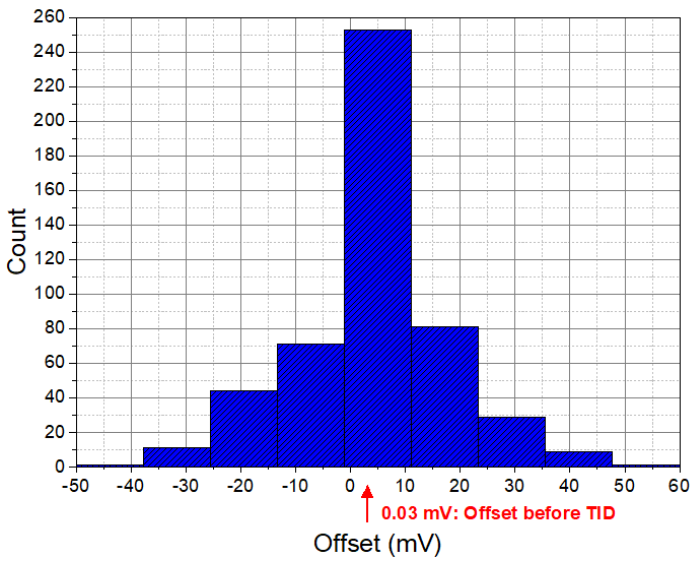


Figure 3.17: TID effect on the Strong Arm Latch Comparator offset [1].

Again, a SET test is conducted on the second comparator and the results can be seen in Figure 3.18. The graph verifies that the Strong Arm Latch Comparator is also sensitive to the SET effect similar to the first comparator. Another point worth noting is that since SET is known to affect especially off-transistors and there is no static current in the Strong Arm Latch Comparator, the error in the graph is an expected result [1].

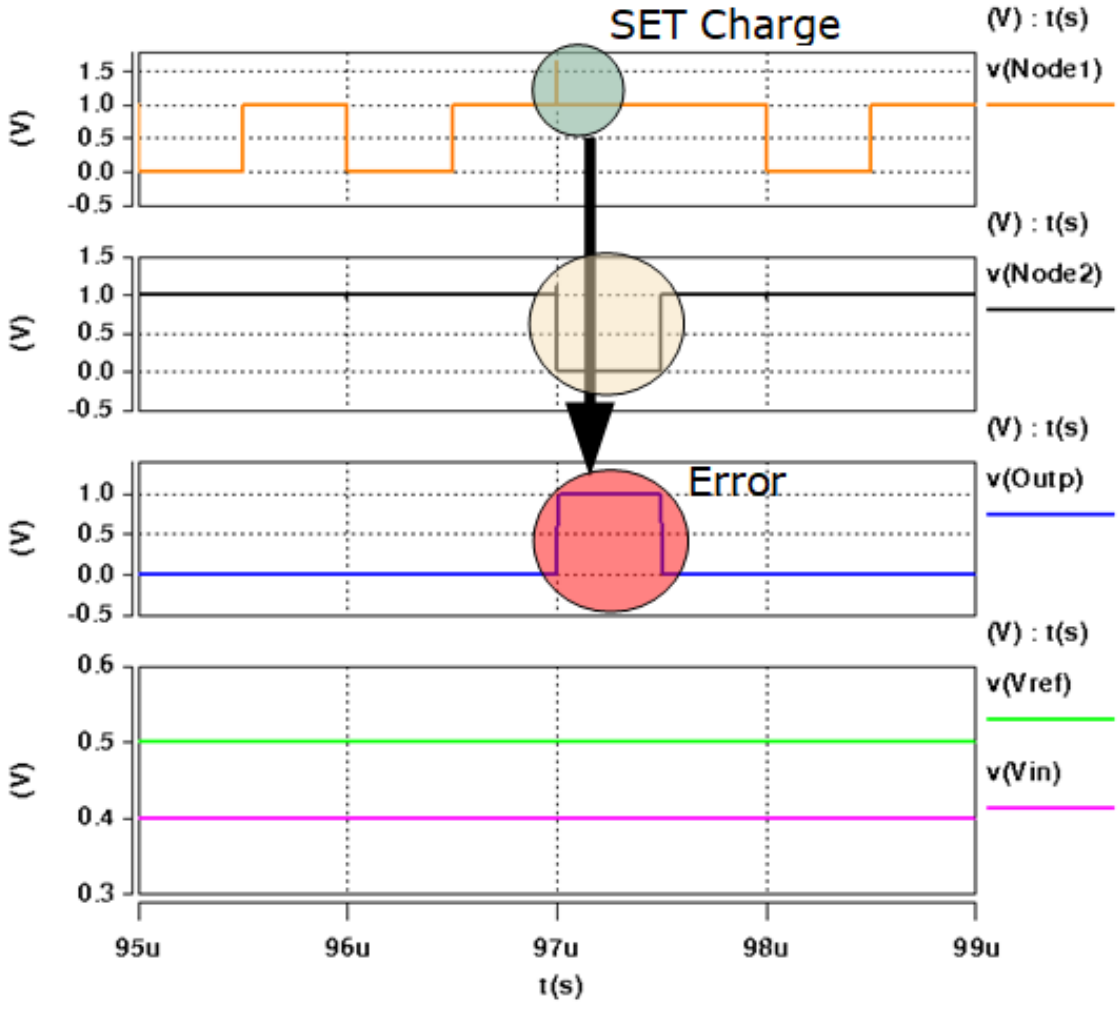


Figure 3.18: Transient graph showing SET effect on the Strong Arm Latch Comparator [1].

Finally, the sensitivity tables of the two comparators can be seen in Table 3.3 and Table 3.4. These tables show the offset change in the second column in which polarity is critical since it may represent a shift in forward (+) or reverse (-) direction. Looking at the results, it is clear that differential pairs are very sensitive to the TID effect as expected. Furthermore, it is worth noting that switch transistors whose gates are connected to the clock signal are not very sensitive to the radiation effect. In addition, it can be said that the cross-coupled transistors in both circuits which are named the same (M_1 and M_4) have different sensitivities in each circuit as they are always active in CMOS Static Latched Comparator while they are not in Strong Arm Latch Comparator, which makes these transistors more important in terms of decision making in the former comparator.

Table 3.3: TID Sensitivity Table of the CMOS Static Latched Comparator [1].

Transistor	Relative Sensitivity (%)	Offset Sensitivity (%)
M3	100	143.2
M4	97.21	-139.2
M2	81.01	-116
M1	80.45	115.2
M5	69.83	100
M6	69.83	-100
M7	15.64	22.4
M8	13.97	-20
M9	0.56	0.8

Table 3.4: TID Sensitivity Table of the Strong Arm Latch Comparator [1].

Transistor	Relative Sensitivity (%)	Offset Sensitivity (%)
M5	100	100
M6	99.2	-99.2
M3	22.4	22.4
M4	21.6	-21.6
M1	5.6	5.6
M2	4.8	-4.8
M10	1.6	1.6
M7	0.8	0.8
M9	0.8	-0.8

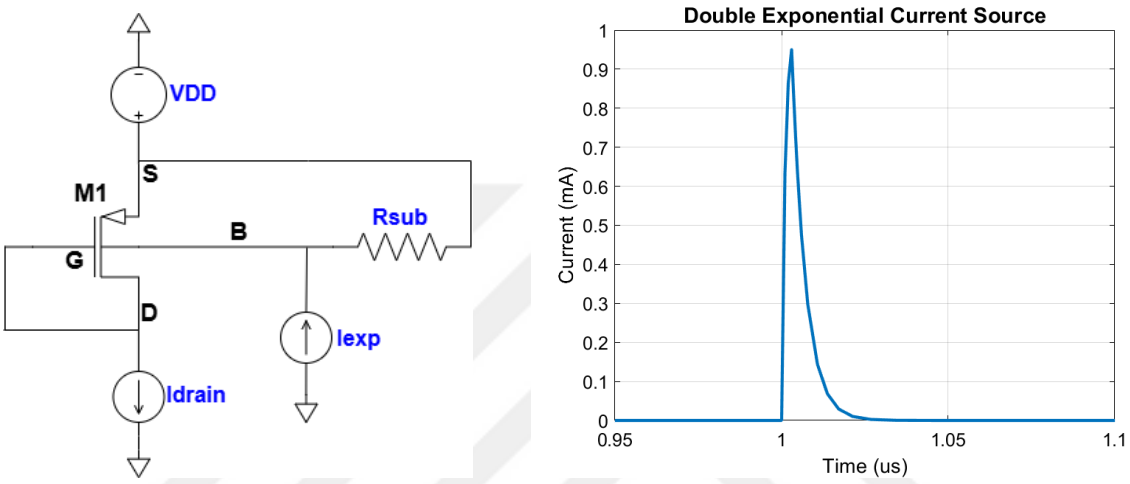
To conclude, it can be said that the TID and SET radiation effect tests are conducted on the two comparators and the offset histograms, transient graphs and sensitivity tables are obtained at the end. Looking at the results, it is clear that both comparators are prone to false logic pulses due to the SET effect. Moreover, it is worth keeping in mind that the offset histograms reveal that CMOS Static Latched Comparator ($\sigma = 26.9$ mV) is more sensitive to TID effect than Strong Arm Latch Comparator ($\sigma = 14.7$ mV) after comparing the two standard deviations of the histograms. Finally, it is clear that an electronic circuit designer can utilize these results in order to design circuits which are robust against radiation effects.

3.2. Layout Level Simulations

3.2.1. Substrate Resistance

In order to test the effect of an ideal substrate (bulk) resistance on a transistor to observe its importance when a charged particle hits the bulk node, a test bench was built in the Cadence environment, and it can be seen in Figure 3.19.

On the left side, there is a schematic including one transistor, a substrate resistance, a dc supply source, a current source to ensure current flow, and a double-exponential current pulse to represent the Single Event Transient effect, which can be seen on the right side.



(a) (b)

Figure 3.19: Test bench of the bulk resistance test: (a) the schematic of the test setup, (b) Double-exponential current pulse.

To study the impact of the Single-Event Transient (SET) effect on a transistor with bulk resistance, changes in both the threshold voltage (Vth) and gate-source voltage (VGS) were observed. These changes, induced by the SET effect, are crucial to monitor, as both Vth and VGS are key parameters in evaluating the reliability and performance of the transistor. Furthermore, while conducting the tests, in order to ensure stability and accuracy, needed parameters were taken from four articles: [44], [45], [46], and [47].

From the result tables, it is evident that using the parameters from [44] in the SET test results in a maximum change of %3.26 in Vth and %4.87 in VGS. In comparison, the changes are %6.93 and %10.86 for [45], %3.99 and %5.45 for [46], and %15.96 and %33.87 for [47].

Therefore, it is worth keeping in mind that a two-digit change in Vth and VGS can be crucial in circuits such as bandgap reference circuits and comparators, where transistor reliability has significant importance since a shift in transistor parameters can lead to a shifted reference voltage or errors in decision-making.

Table 3.5: Table of the bulk resistance effect on Vth and VGS for [44] where finger width is 4 µm.

Finger Number	**Vth (mV)**			**VGS (mV)**		
	Normal	**Minimum**	**Change**	**Normal**	**Minimum**	**Change**
6	-380	-392.4	-12.4 (**%3.26**)	-241.25	-253	-11.75 (**%4.87**)
18	-385	-391.9	-6.9 (**%1.79**)	-195.2	-202.2	-7 (**%3.59**)
36	-385.5	-393.9	-5.4 (**%1.39**)	-167.75	-173.75	-6 (**%3.58**)
72	-392.1	-397.4	-5.3 (**%1.35**)	-141.3	-148.1	-6.8 (**%4.81**)

Table 3.6: Table of the bulk resistance effect on Vth and VGS for [45].

Gate Length	**Vth (mV)**			**VGS (mV)**		
	Normal	**Minimum**	**Change**	**Normal**	**Minimum**	**Change**
60 nm	-389	-390.6	-1.6 (**%0.41**)	-173.6	-175.4	-1.75 (**%1**)
120 nm	-355	-366.4	-11.4 (**%3.21**)	-204	-216.4	-12.4 (**%6.08**)
240 nm	-324.5	-347	-22.5 (**%6.93**)	-221	-245	-24 (**%10.86**)

Table 3.7: Table of the bulk resistance effect on Vth and VGS for [46], where length is 55 nm, finger width is 2.5 µm and finger count is 8.

Active to Sub Spacing	**Vth (mV)**			**VGS (mV)**		
	Normal	**Minimum**	**Change**	**Normal**	**Minimum**	**Change**
1 um	-377.6	-389.2	-11.6 (**%3.07**)	-249.5	-260.4	-10.9 (**%4.37**)
1.5 um	-377.6	-389.6	-12 (**%3.18**)	-249.6	-260.6	-11 (**%4.41**)
3.5 um	-377.6	-391.3	-13.7 (**%3.63**)	-249.6	-262.5	-12.9 (**%5.17**)
5.5 um	-377.6	-392.7	-15.1 (**%3.99**)	-249.6	-263.2	-13.6 (**%5.45**)

Table 3.8: Table of the bulk resistance effect on Vth and VGS for [47].

Finger Number	**Vth (mV)**			**VGS (mV)**		
	Normal	**Minimum**	**Change**	**Normal**	**Minimum**	**Change**
	dH=1.5um					
8	-373.6	-409.6	-36 (**%-9.64**)	-272.8	-309.6	-36.8 (**%13.49**)
16	-376.5	-407.5	-31 (**%8.23**)	-243	-274	-31 (**%12.76**)
30	-379.5	-406.5	-27 (**%7.11**)	-217	-245	-28 (**%12.90**)
	dH=3.5um					
8	-373.3	-432.6	-59.3 (**%15.9**)	-273.2	-332.4	-59.2 (**%21.7**)
16	-376.5	-434.3	-57.8 (**%15.3**)	-243.1	-289.1	-46 (**%18.92**)
30	-379.6	-416.5	-36.9 (**%9.72**)	-217.1	-255.7	-38.6 (**%17.78**)
	dH=5.5um					
8	-376.4	-416.6	-40.2 (**%10.68**)	-243.5	-326	-82.5 (**%33.87**)
16	-376.5	-436.4	-60.1 (**%15.96**)	-243.3	-304.7	-61.4 (**%25.13**)
30	-379.6	-424.3	-44.7 (**%11.77**)	-217.1	-264.4	-47.3 (**%21.78**)

3.2.2. SET Tests with Substrate Resistance

In the previous section, it was shown that when a highly energetic particle hits the bulk node of a transistor, it can cause a significant change in the parameters of the transistor. Furthermore, it is worth noting that this effect can be crucial for logic circuits such as bandgaps and comparators. Therefore, this section is about the SET errors in bandgaps and comparators in the presence of a substrate resistance. In this context, the circuits that were originally designed in HSPICE were reimplemented in Cadence using a 65 nm process to enable testing and ensure compatibility with the Cadence environment. The first step was to rebuild and retest the circuits to confirm they performed as expected. Specifically, this included reconstructing and testing the bandgap [38] and comparator circuits [42,43] from earlier sections, but this time within the Cadence environment, as it will be used for additional testing.

Initially, the bandgap circuit is built and tested, which can be seen in Figure 3.20 and Figure 3.21. The results indicate an average reference voltage of about 1.17 V and a temperature coefficient of 3.11 ppm/°C, which are acceptable values for a bandgap circuit.

In the next step, the comparator circuits were built and tested. While applying the tests, input voltage was swept from 0 V to 1 V while the input reference voltage had a constant value of 0.5 V in order to see the full spectrum of the output voltage. Schematics can be seen in Figure 3.22 and Figure 3.24 while transient graphs can be seen in Figure 3.23 and Figure 3.25. The result graphs clearly show that both comparators work as expected since the output voltage toggles when the input voltage is bigger than the input reference voltage, which is 0.5 V.

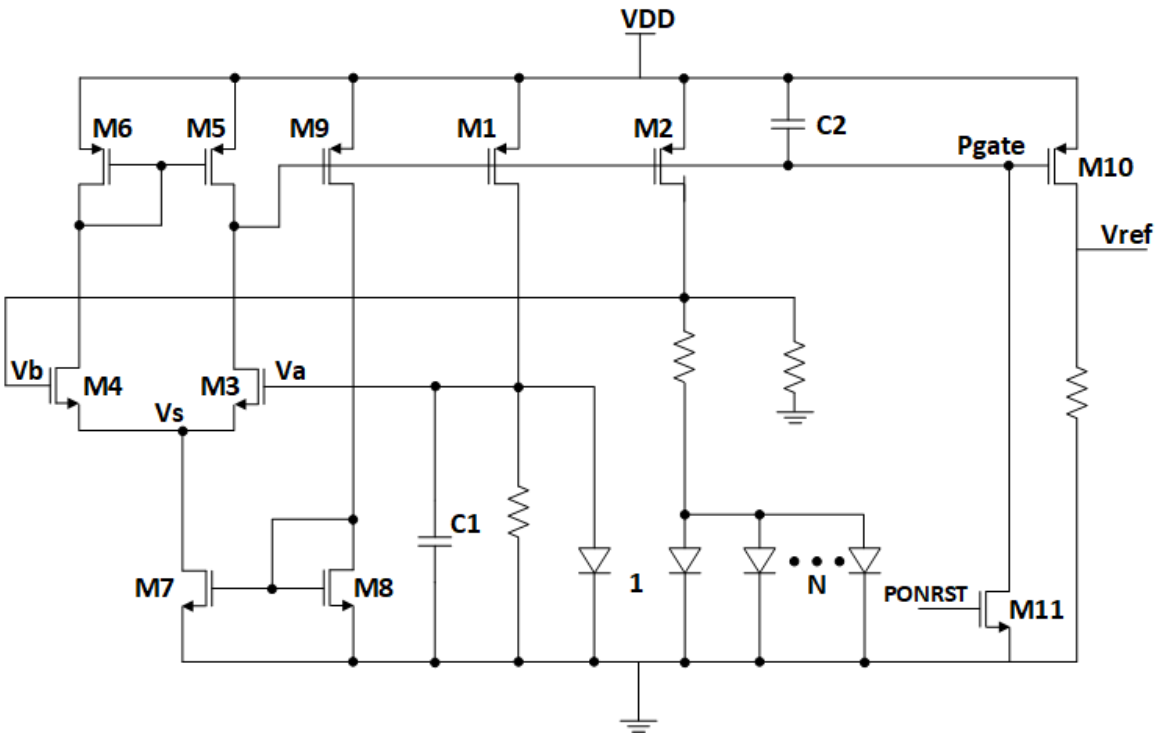


Figure 3.20: Schematic of the bandgap reference circuit [1].

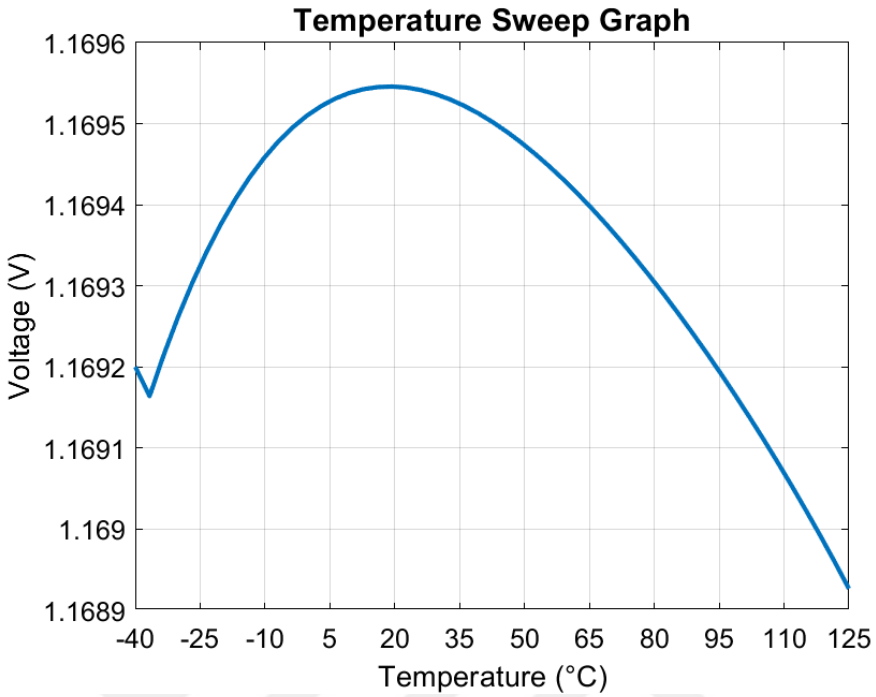


Figure 3.21: Temperature sweep graph of the bandgap reference circuit.

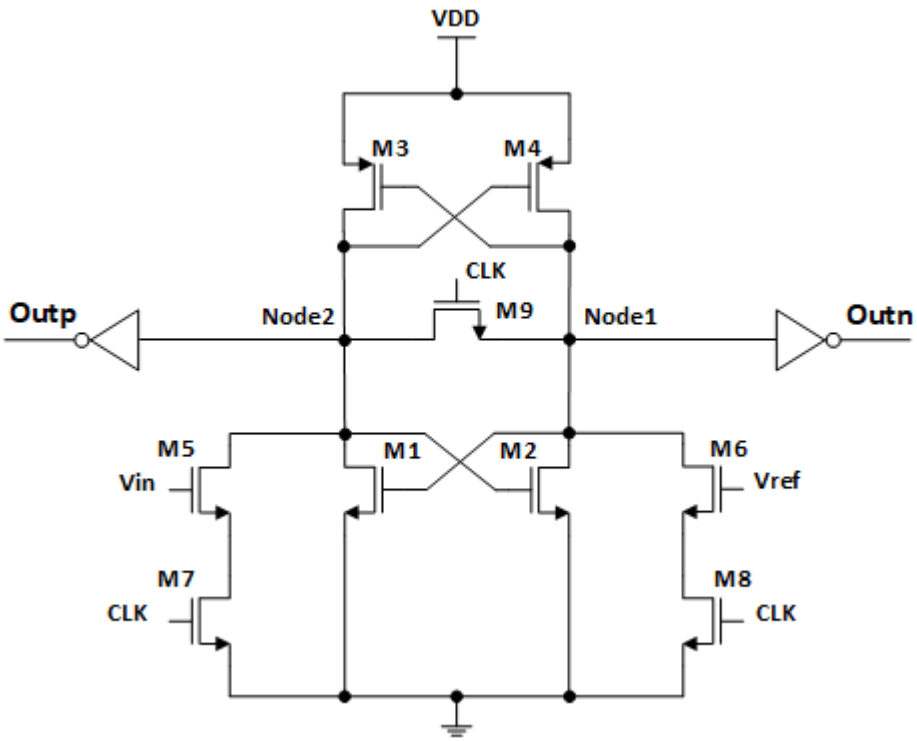


Figure 3.22: Schematic of the CMOS Static Latched Comparator [1].

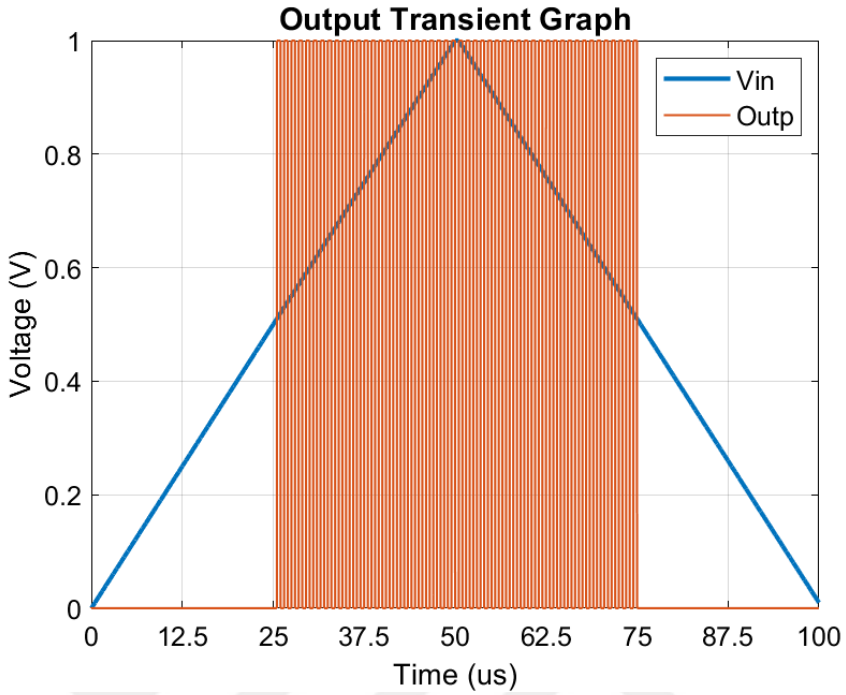


Figure 3.23: DC Sweep graph of the CMOS Static Latched Comparator.

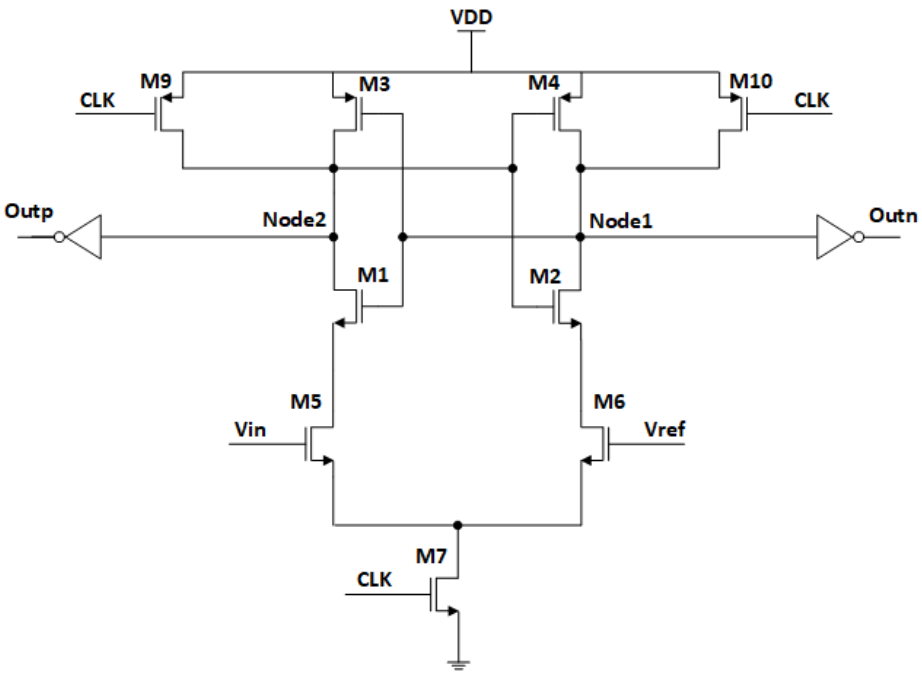


Figure 3.24: Schematic of the Strong Arm Latch Comparator [1].

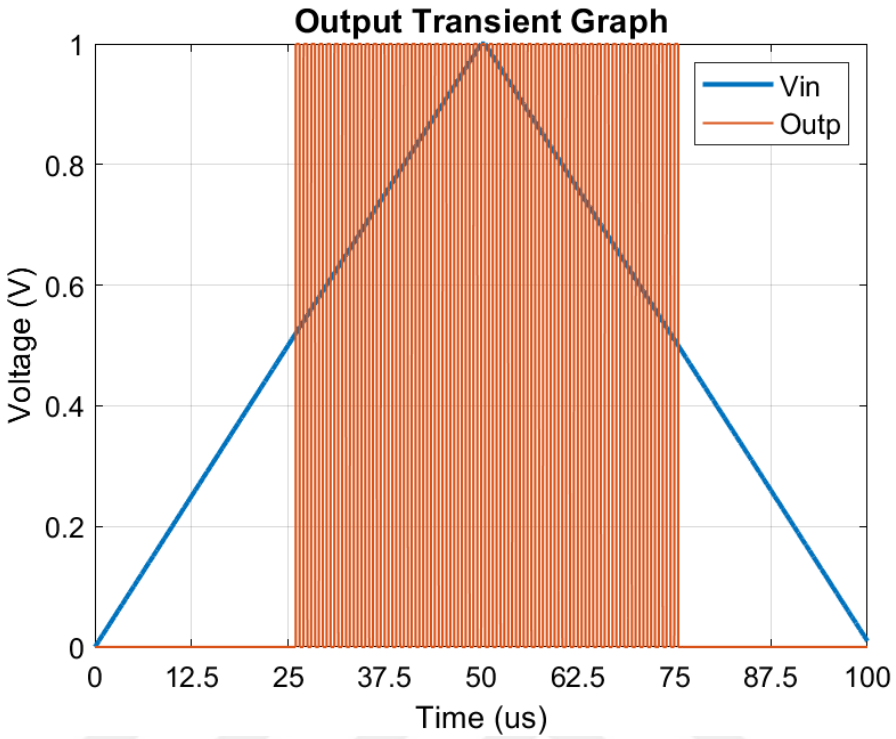


Figure 3.25: DC Sweep graph of the Strong Arm Latch Comparator.

After verifying all circuits work as expected, the next step was Single Event Transient tests including substrate resistances. For this purpose, schematics were modified to include substrate resistances and double-exponential current pulses which can be seen in Figure 3.26. In this method, each transistor has different current pulses which is useful for testing transistors individually.

For instance, Figure 3.27 shows that when the bulk node of the M10 transistor in the bandgap reference circuit gets hit by a heavily charged particle, the output reference voltage can shift up to 100 mV, which indicates a critical error.

In terms of SET tests in comparators, it is worth keeping in mind that the SET effect can cause a glitch at the output node as in Figure 3.28 or a false logic pulse as in Figure 3.29. The critical thing which determines this is the time when the SET event happens.

If it hits at the transition moment of the clock signal, then the output stays wrong till the next clock edge. Using this information, both comparators can experience false logic pulses at the output node as it is shown in Figure 3.30 and Figure 3.31.

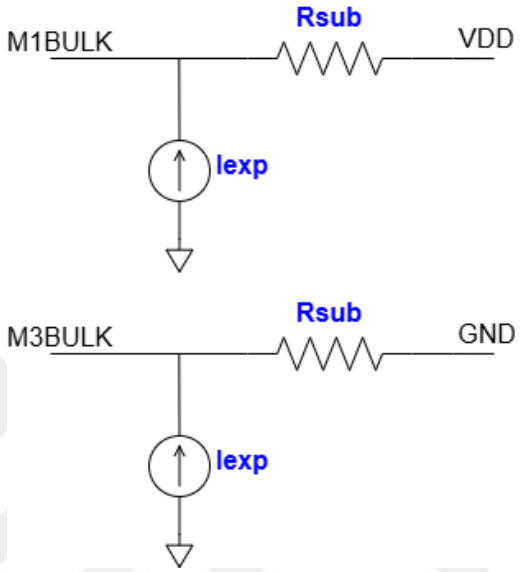


Figure 3.26: Resistors and double-exponential current pulses for the SET test.

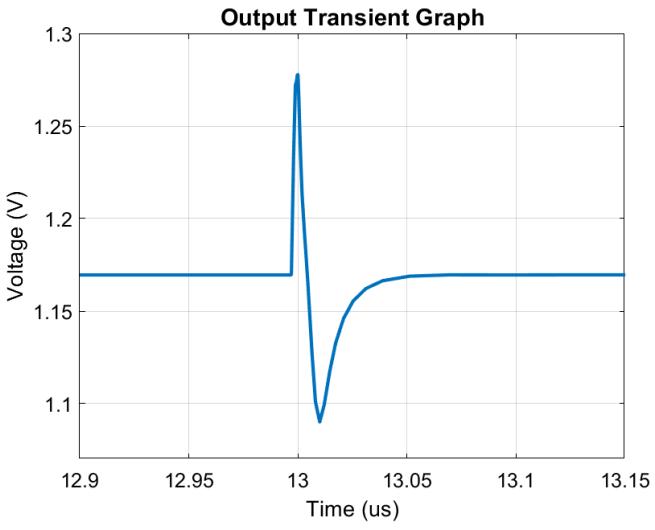


Figure 3.27: Transient graph showing SET effect on the bulk of a transistor causing a glitch at the output node of the bandgap reference circuit.

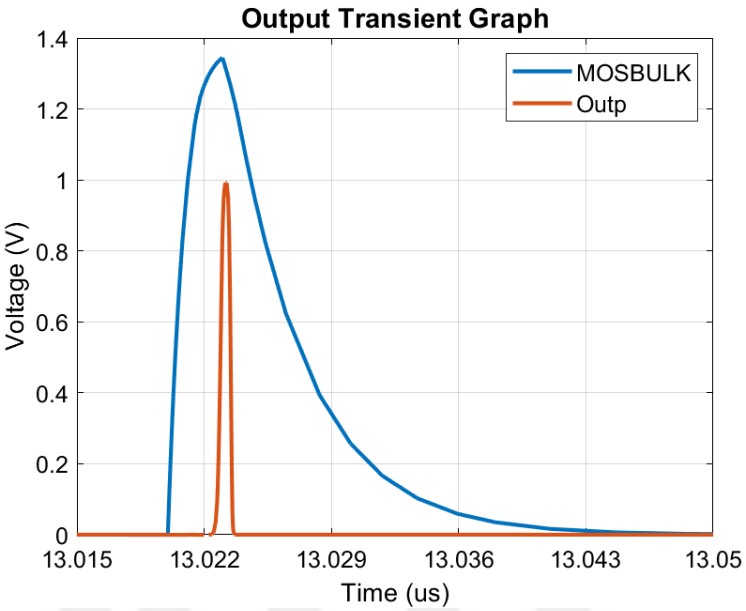


Figure 3.28: Transient graph showing the SET effect on the bulk of a transistor causing a glitch at the output of a comparator.

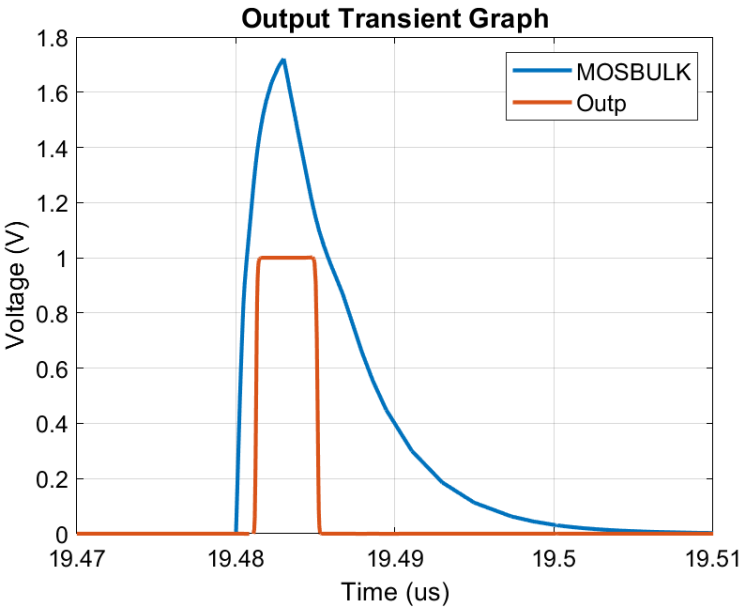


Figure 3.29: Transient graph showing the SET effect on the bulk of a transistor causing a false high pulse at the output of a comparator.

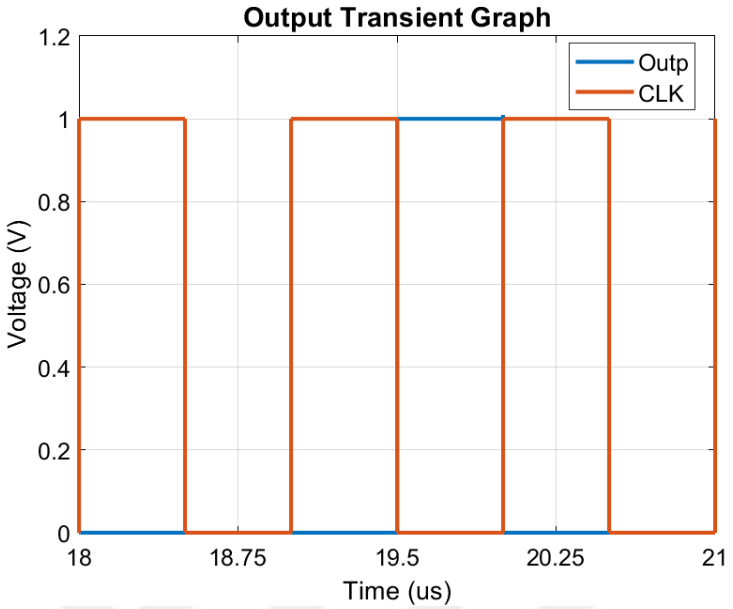


Figure 3.30: Transient graph showing false high pulse due to SET effect for the CMOS Static Latched Comparator.

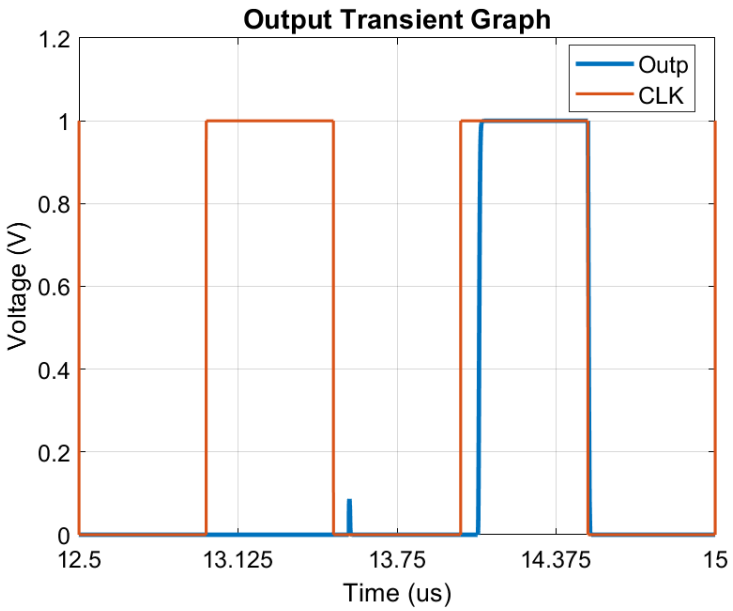


Figure 3.31: Transient graph showing false high pulse due to SET effect for the Strong Arm Latch Comparator.

3.2.3. Substrate Mesh Setup

After observing substrate resistance effect in the presence of a radioactive particle, the next step was building a resistance mesh representing the well using 1-R Resistor Network [33] with 80 rows and 80 columns. This mesh includes resistors in every node, a resistor layer at the outmost nodes representing a guard ring and a diode in every node connected to VDD for N-Well and ground for P-Well for physical accuracy. A script was developed in Cadence SKILL language in order to create the mesh network. After that, the symbol of the mesh was created in order to connect to the bulk node of the transistors for simulating the substrate. A single square of the mesh can be seen in Figure 3.32 and the overall 80x80 circuit block, represented as a simplified 15x15 version for clarity, can be seen in Figure 3.33.

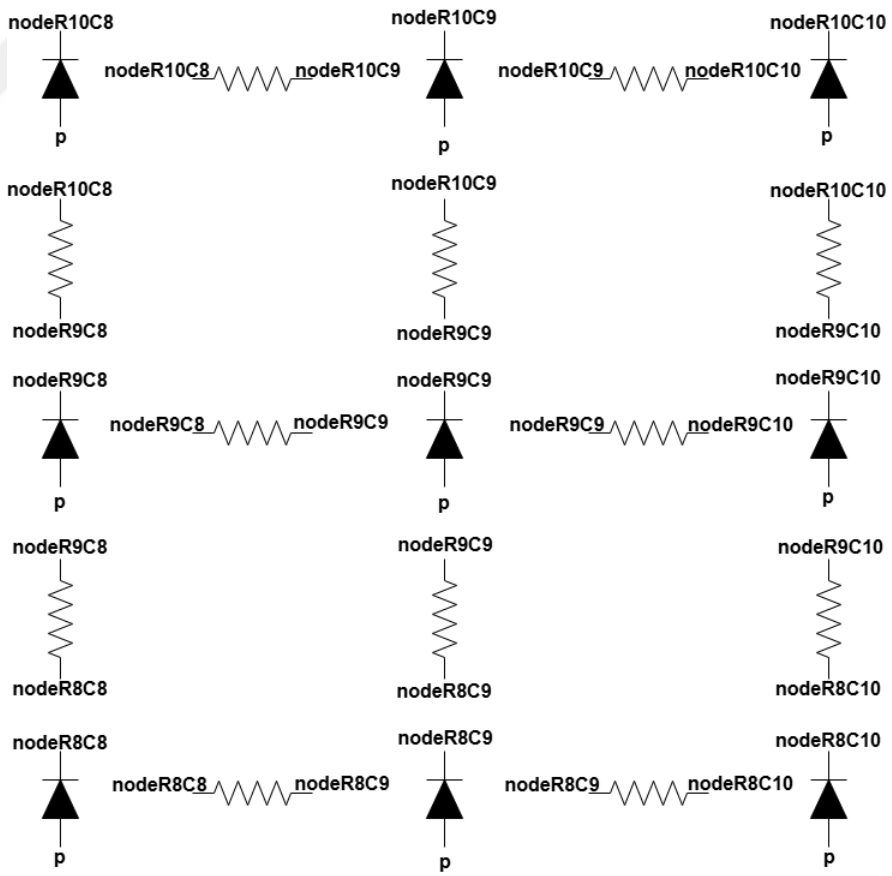


Figure 3.32: Narrowed image of the mesh.

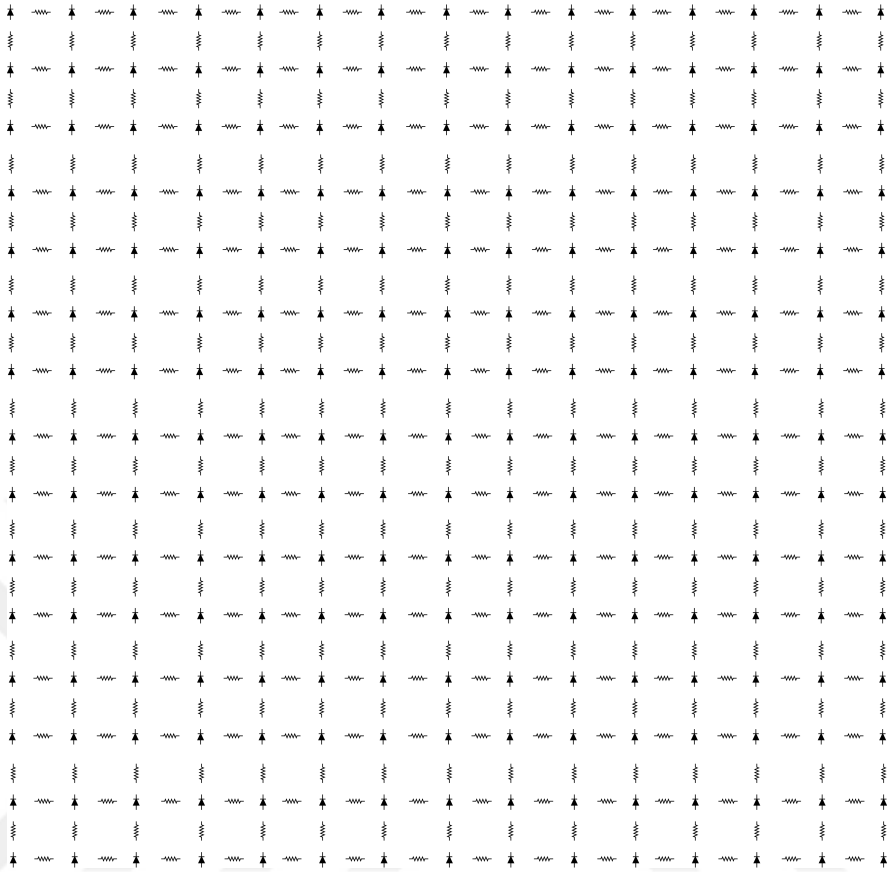


Figure 3.33: Complete schematic of the 80x80 Mesh (displayed as 15x15 for better visual clarity).

Once the mesh network building process was completed, the reliability and the accuracy of the mesh network were tested using the resistance values in the articles. For this purpose, three articles ([44, 46, 47]) were selected to compare with the resistance values that were obtained in Cadence environment using the mesh network.

While obtaining the substrate resistance values from the simulation, the MOSFET fingers and sizes were represented by connecting multiple nodes according to the width of the transistors, and the sub spacing distance parameter was represented by starting measurement after the appropriate distance from one end. Then, the resistance value was measured by simply adding a dc current source to the node and measuring the voltage change which would lead to the substrate resistance value after dividing it by the dc current value using the $V = I \cdot R$ formula.

Since the Rsquare values of the technologies used in the articles were not revealed, Rsquare values were calculated by using the Mean Squared Error method.

After interpreting the result graphs, it can be stated that the comparison graph for [44] (Figure 3.34) includes results for different finger cases and shows a maximum error of around %26.6, which decreases to a maximum of %10.8 for the cases compared to those in [46] (Figure 3.35), where 'Active to Sub Spacing' is the independent variable. Furthermore, after comparing the result graphs with those from [47], it is important to note that the error value increases as the body-contact to active-region distance (dH) increases, with maximum errors of %13.3 in Figure 3.36, %30.4 in Figure 3.37, and %51.1 in Figure 3.38.

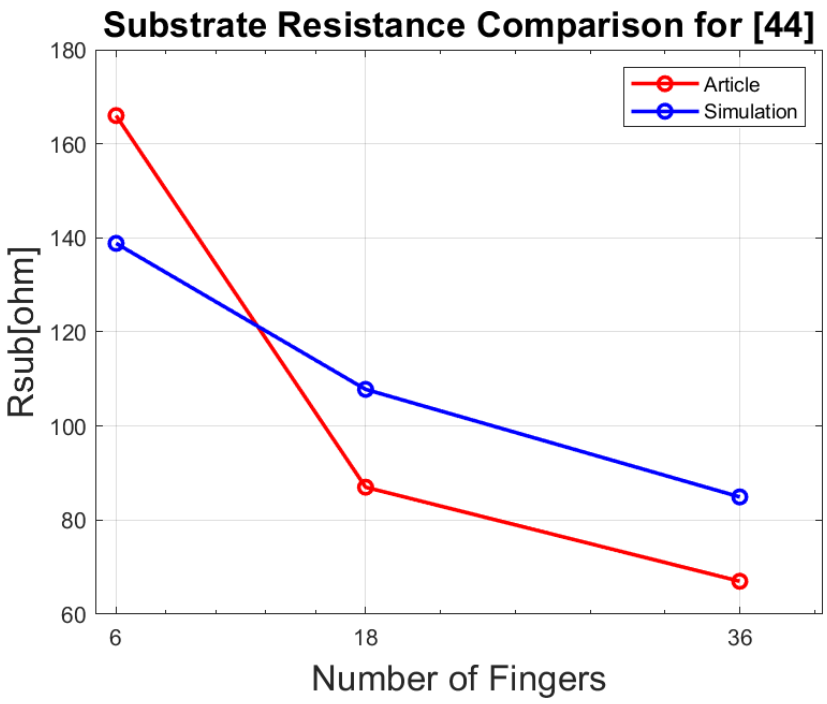


Figure 3.34: Graph of the substrate resistance comparison for [44].

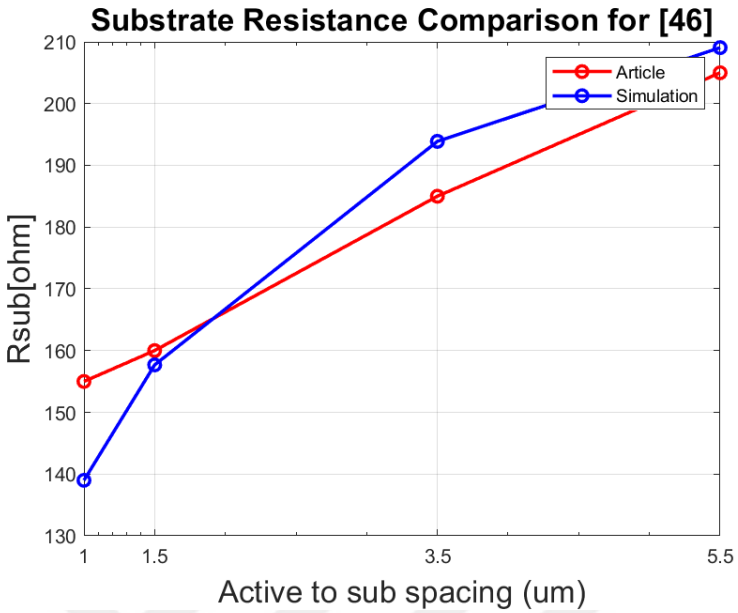


Figure 3.35: Graph of the substrate resistance comparison for [46].

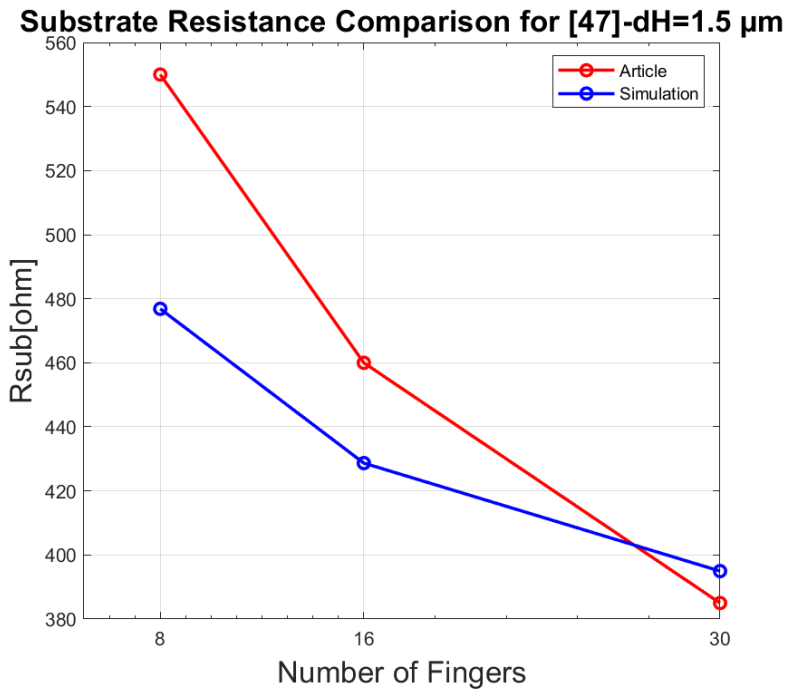


Figure 3.36: Graph of the substrate resistance comparison for [47] with dH=1.5 um.

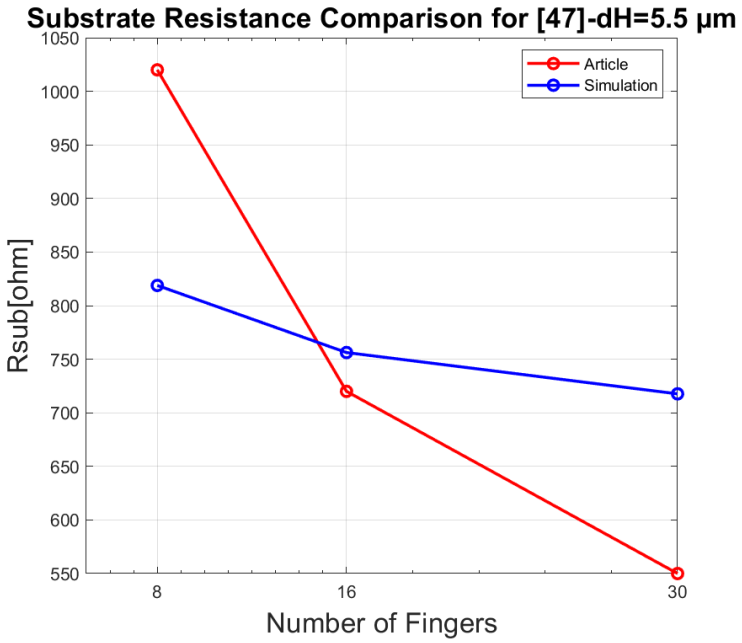


Figure 3.37: Graph of the substrate resistance comparison for [47] with dH=5.5 um.

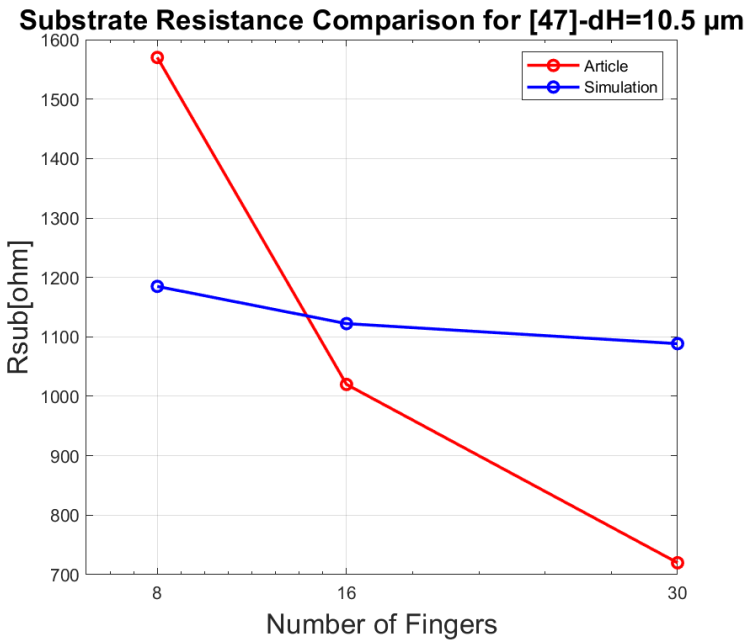


Figure 3.38: Graph of the substrate resistance comparison for [47] with dH=10.5 um.

3.2.4. Automated SET Tests

Once the mesh network was built and verified after testing, the next step was testing the new mesh network with the analog and digital circuits that were built previously. In this context, a SKILL based tool was developed in order to automate the process. The working principle of the tool can be seen in Figure 3.39. Initially, it obtains the circuit netlist and variables as inputs, then sets the current amplitudes for each node by using a Gaussian function, and then the simulation is performed. Lastly, the result parameters are measured and saved to a file which can be loaded to MATLAB for visualization of the results. Results can be in either histogram form for overall observation or heatmap, which shows the sensitive areas against the radiation effect.

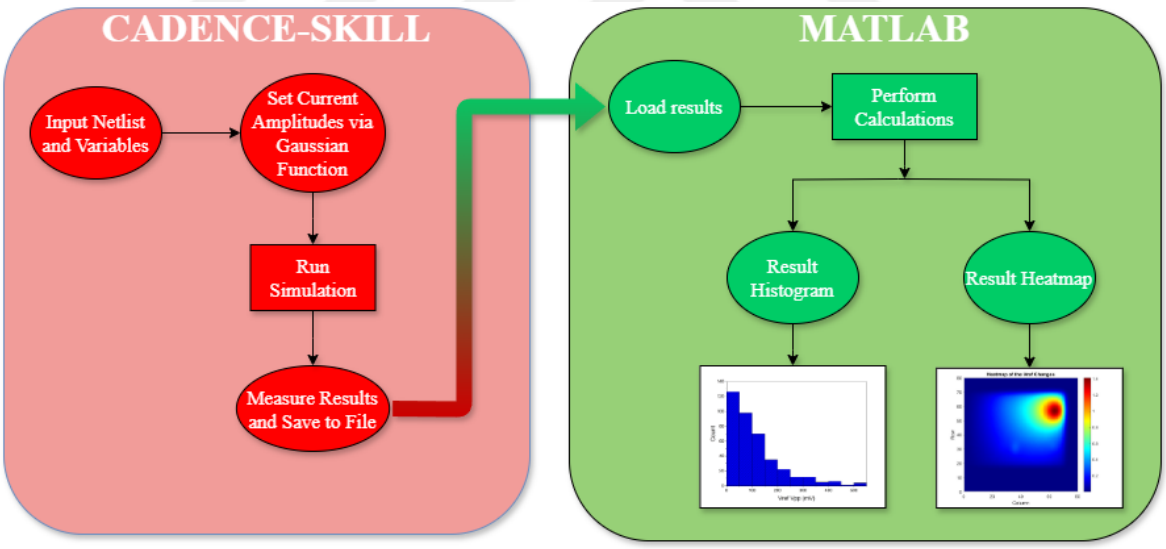


Figure 3.39: Diagram illustrating the simulation process.

As the first step, transistors were divided into multiple transistors in order to represent them as multiple nodes in the substrate mesh network, which would help the transistor placement process. Therefore, in the end, large transistors were represented as multiple small transistors.

After that, the bulk nodes of these transistors were connected to the substrate mesh network by using deep probes as it can be seen in Figure 3.40.

The next step was building another mesh network consisting of double-exponential current pulses in order to simulate the SET effect in each node of the substrate mesh network. A script using the Cadence SKILL language was developed for this purpose, and as it can be seen in Figure 3.41, current pulses were connected between ground and the individual nodes of the substrate mesh network. Plus, the parameters of the current pulses were arranged using variables so that they could be set individually before the simulation begins. The amplitude parameter was set within a Cadence SKILL function which includes a Gaussian distribution formula so that the SET only affects the area that is decided by the mean and sigma values of the Gaussian distribution. The overall schematic of the new current mesh network, shown as a simplified 15x15 version for clarity, can be seen in Figure 3.42.

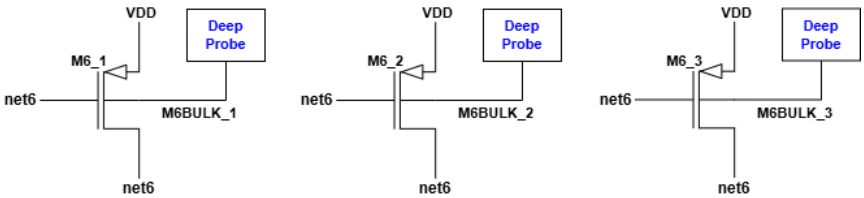


Figure 3.40: Multiple transistors representing a larger transistor.

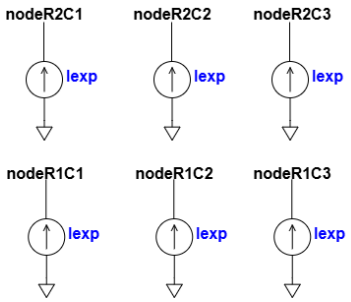


Figure 3.41: Narrowed image of the double-exponential current pulse mesh.

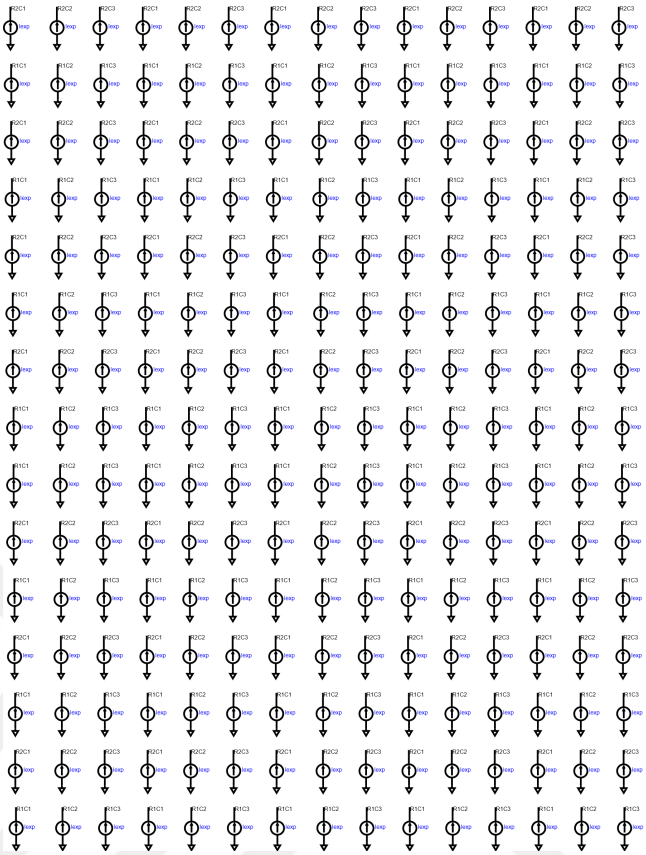


Figure 3.42: Overall schematic of the current mesh (displayed as 15x15 for better visual clarity).

First case was the previously built bandgap reference circuit and the transistors were placed accordingly in the substrate mesh grid using multiple fingers as it can be seen in Figure 3.44. Next, multiple Gaussian charge distributions were applied to cover the entire circuit, as seen in Figure 3.45. A single 3D visualization of one of these distributions is shown in Figure 3.43, illustrating how the charge density varies, with higher concentrations at the center and tapering off towards the edges. Then, the simulation was performed using a Cadence SKILL script and the changes in the output node were measured as it can be seen as a histogram in Figure 3.46. Looking at the results, it can be said that reference voltage changes between 0-20 mV in most cases, although there are some cases with more than 80 mV shift which is a concerning value.

Moreover, the heatmap created by using the change in reference voltage for every area can be seen in Figure 3.47 which reveals that the most vulnerable area includes M2 and M10 transistors, which is expected by looking at Table 3.2 where M2 and M10 have the largest output voltage change values.

Another test was performed on the bandgap reference circuit with a 50% larger sigma value in the Gaussian distribution with the same transistor placement in order to obtain a better heatmap. The new distribution can be seen in Figure 3.48 and the new histogram can be seen in Figure 3.49 which indicates much larger changes in the reference voltage as expected. Finally, the new heatmap in Figure 3.50 clearly shows a better view of the vulnerable areas in the circuit.

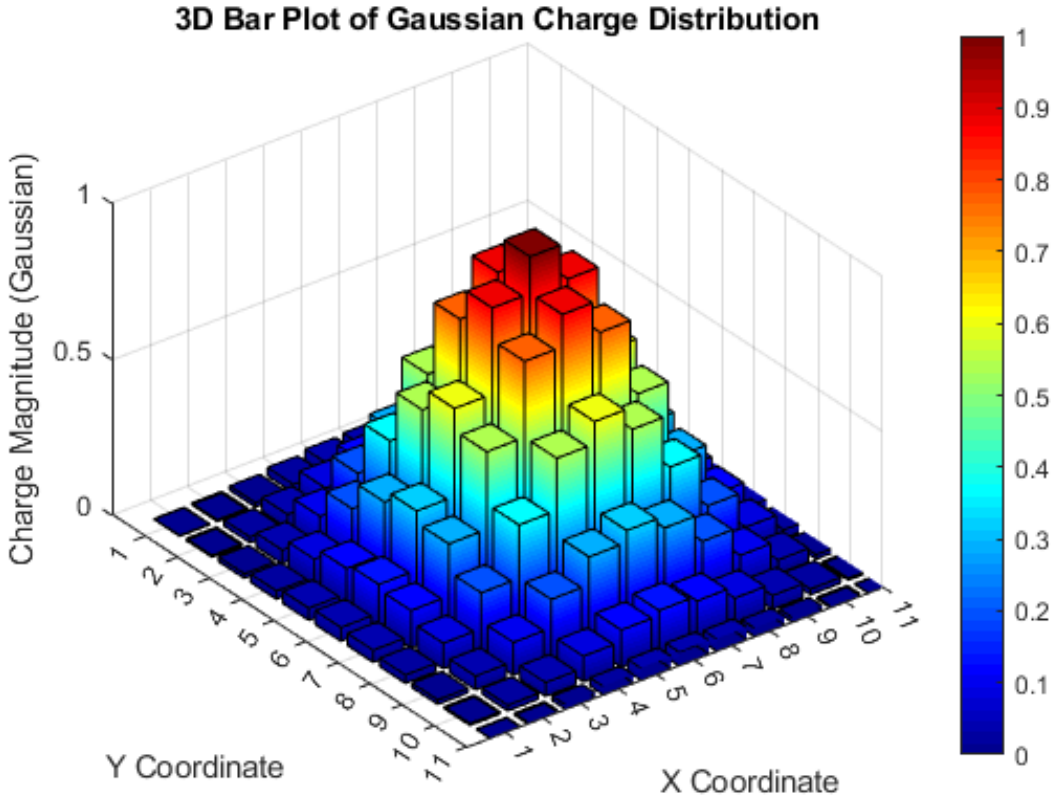


Figure 3.43: 3D Graph of Gaussian charge distribution.

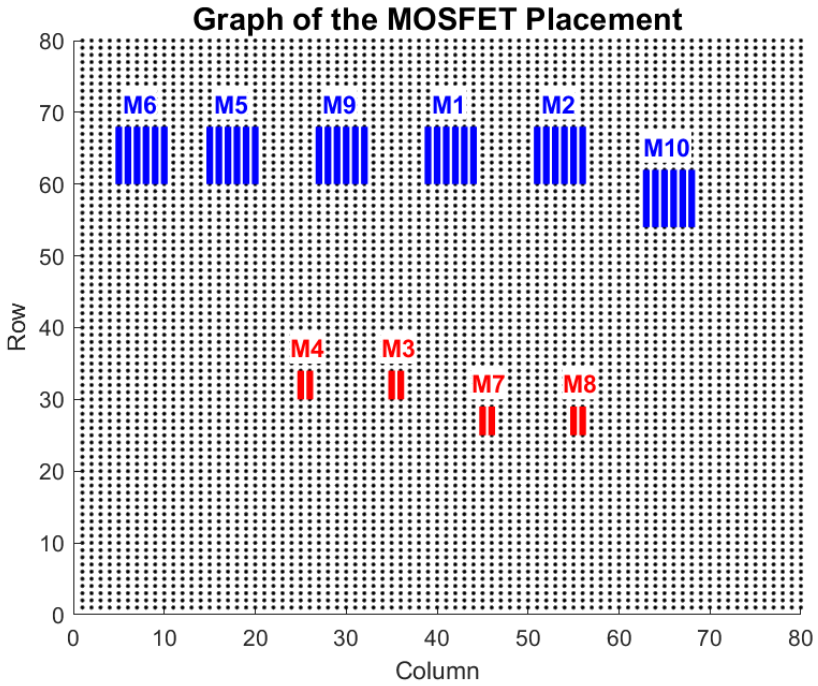


Figure 3.44: Transistor placement for the SET test of the bandgap circuit.

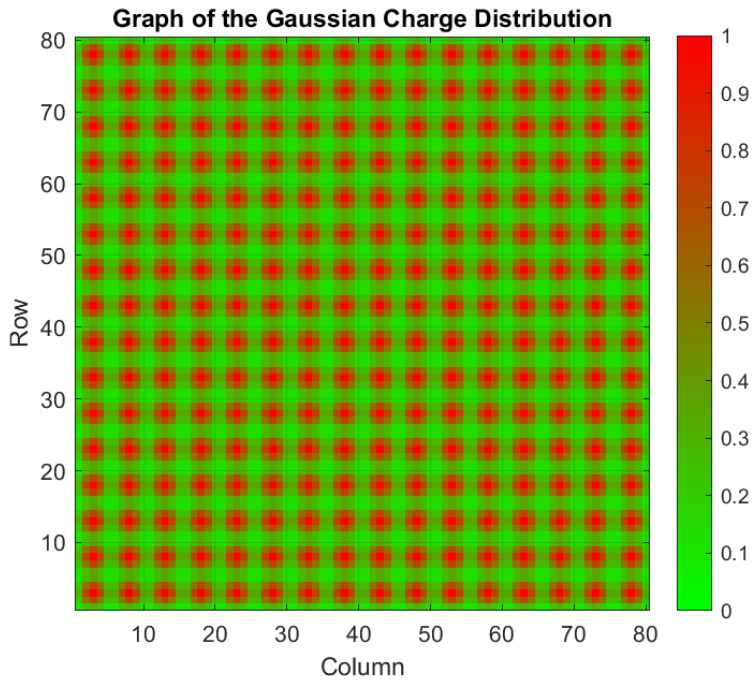


Figure 3.45: Charge distribution for the SET test of the bandgap circuit.

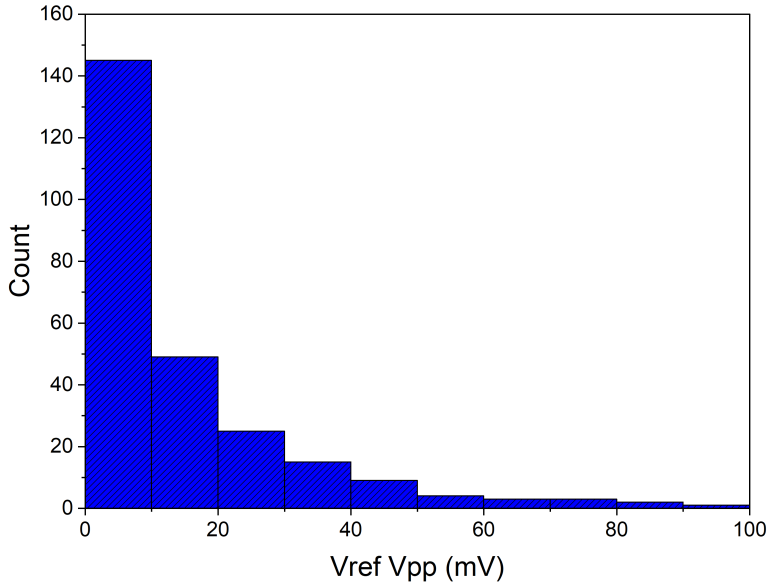


Figure 3.46: Histogram of the changes in the reference voltage.

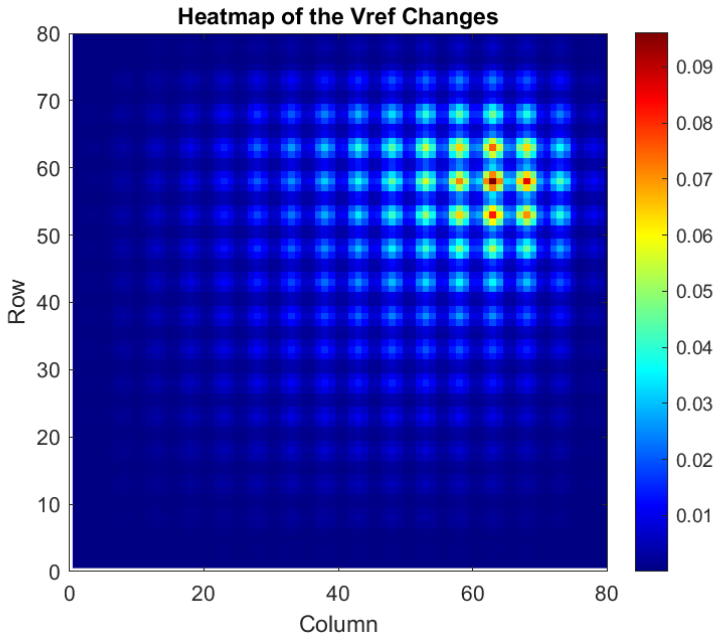


Figure 3.47: Heatmap graph for the SET sensitivity of the bandgap circuit based on reference voltage changes.

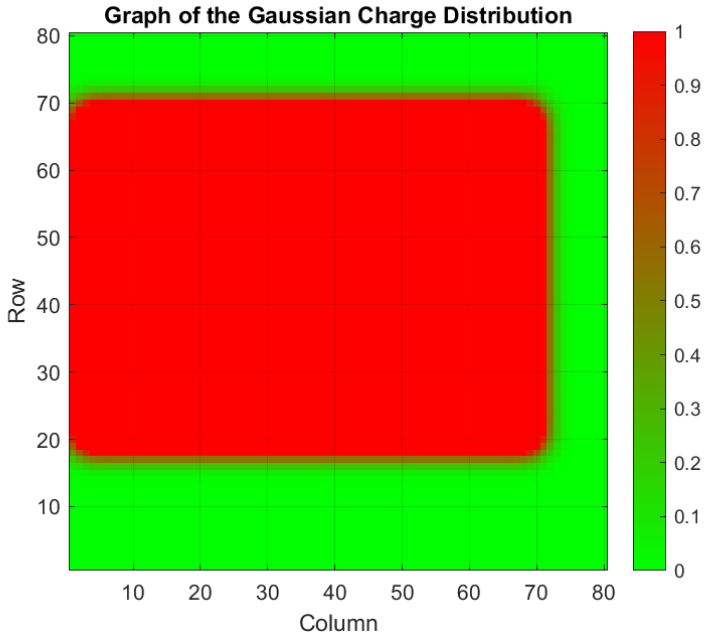


Figure 3.48: Charge distribution for the second SET test of the bandgap circuit.

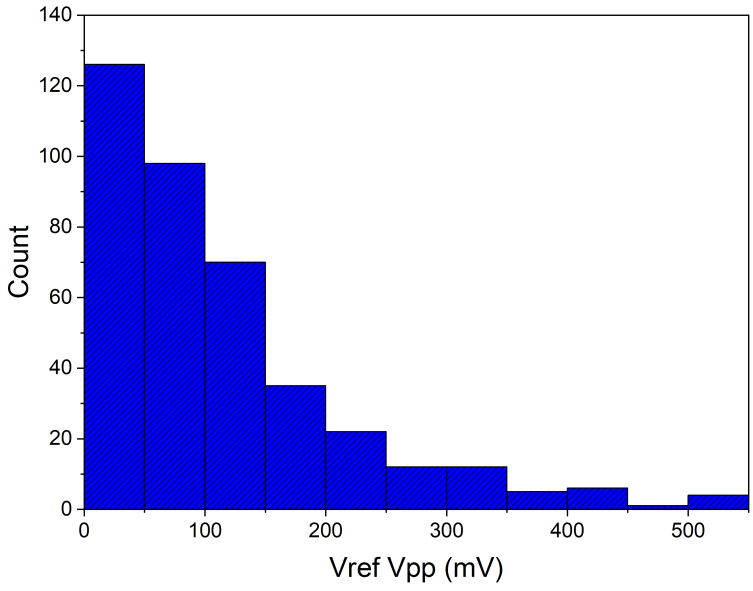


Figure 3.49: Histogram of the changes in the reference voltage for the second test.

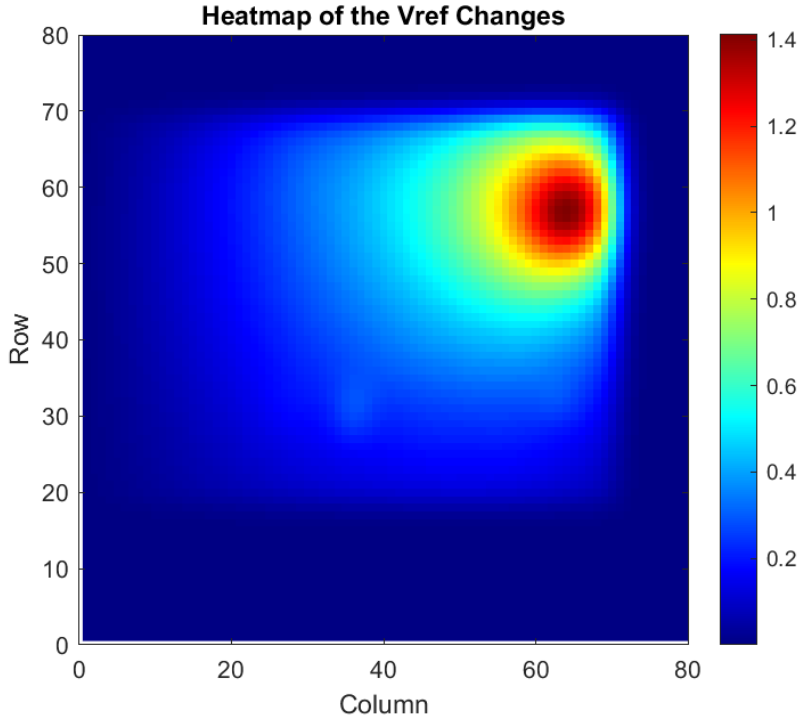


Figure 3.50: Second heatmap graph for the SET sensitivity of the bandgap circuit based on reference voltage changes.

The next test was for the Strong Arm Comparator with the same method in which the transistor placement can be seen in Figure 3.51 and charge distribution can be seen in Figure 3.52. In this test, input voltage was 1 mV less than the input reference voltage which means that this test was about observing false high pulses at the positive output node. The heatmap of the result can be seen in Figure 3.53 which reveals the vulnerable areas for false high pulses.

Another test was done for false low pulses in the same circuit with the same transistor placement, and the result heatmap can be seen in Figure 3.54.

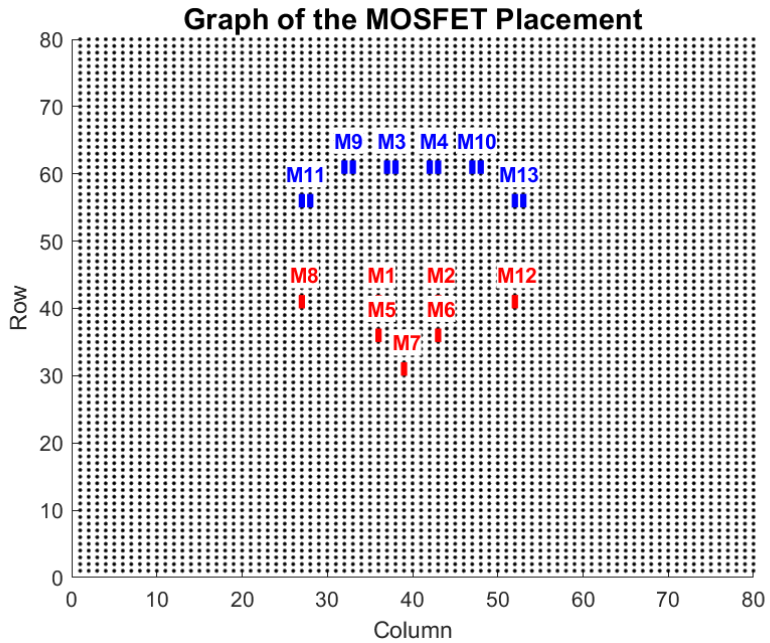


Figure 3.51: Transistor placement for the SET test of the Strong Arm Comparator.

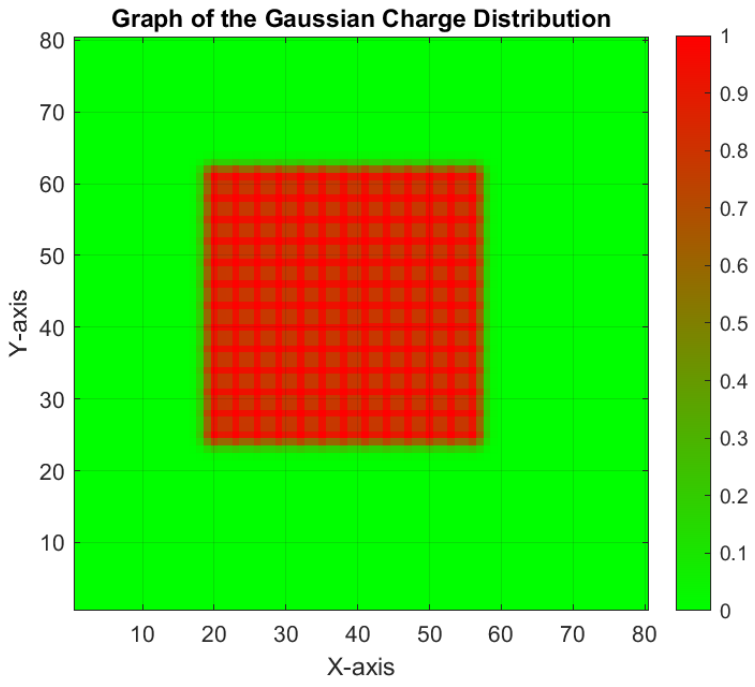


Figure 3.52: Charge distribution for the SET test of the Strong Arm Comparator.

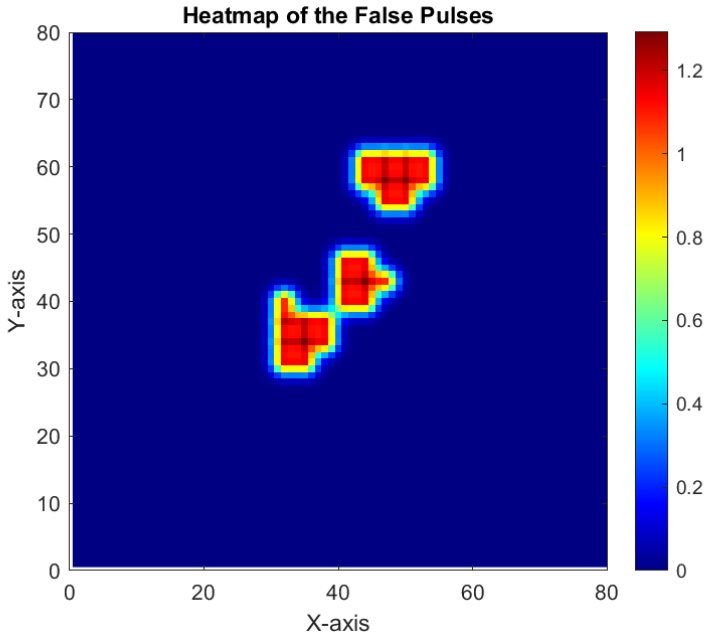


Figure 3.53: Heatmap graph for the SET sensitivity of the Strong Arm Comparator based on false high pulses.

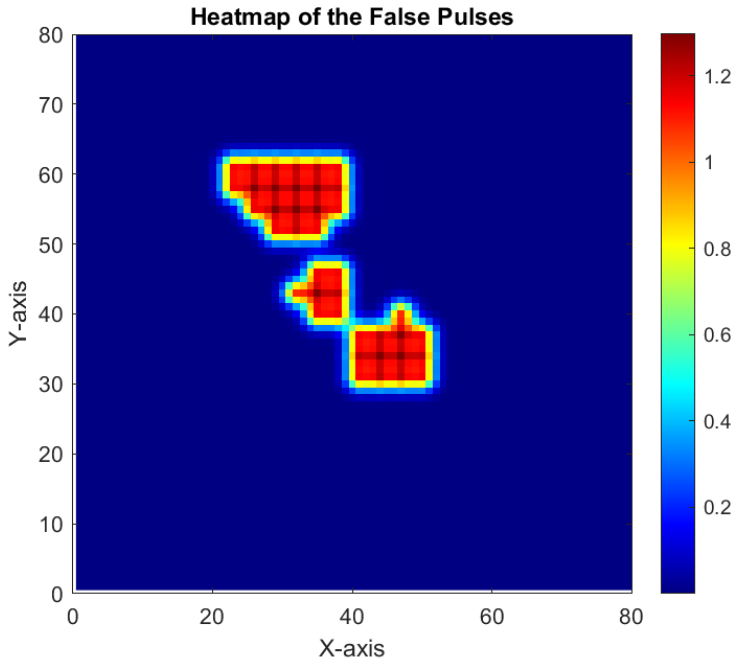


Figure 3.54: Second heatmap graph for the SET sensitivity of the Strong Arm Comparator based on false low pulses.

The tool has another useful feature which shows the node voltages of the substrate mesh network at different times, allowing the user to observe voltage rise and fall over time, similar to a timelapse. An example test was performed on the bandgap reference circuit and the node voltage graph for the P-Well can be seen in Figure 3.56 and the graph for the N-Well can be seen in Figure 3.57. Using the same feature, the effect of guard ring placement around the sensitive transistors, which is a simple and common solution [48–50] to radiation effect on a substrate can be observed. Firstly, a SKILL script was built to create a simple guard ring made out of small resistances of which one terminal is connected to the nodes in the chosen area and the other terminal is connected to the ground, which can be seen in Figure 3.55. After interpreting the graph in Figure 3.50, M10 transistor seems to be the most sensitive transistor thus the guard ring was created around the M10 transistor. Then, same SET simulation was performed again and the result graph in Figure 3.58 reveals that indeed the guard ring is an efficient solution for radiation effects. As a second test, the mean of the gaussian charge distribution was shifted to the center of the transistor M10 to observe the guard ring effect from a different perspective. The result graph before the guard ring is shown in Figure 3.59, while the graph after the guard ring is shown in Figure 3.60.

Another feature is that the tool is capable of performing Multi Event Transient (MET) simulations in which multiple SET events can happen in different areas of the circuit. An example can be seen in Figure 3.61 in which there are three different SET events in different areas with different sigma values.

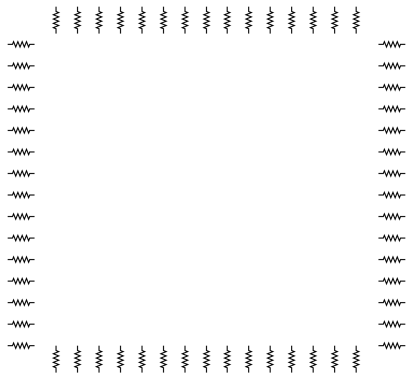


Figure 3.55: Guard Ring built with small resistances connected to ground.

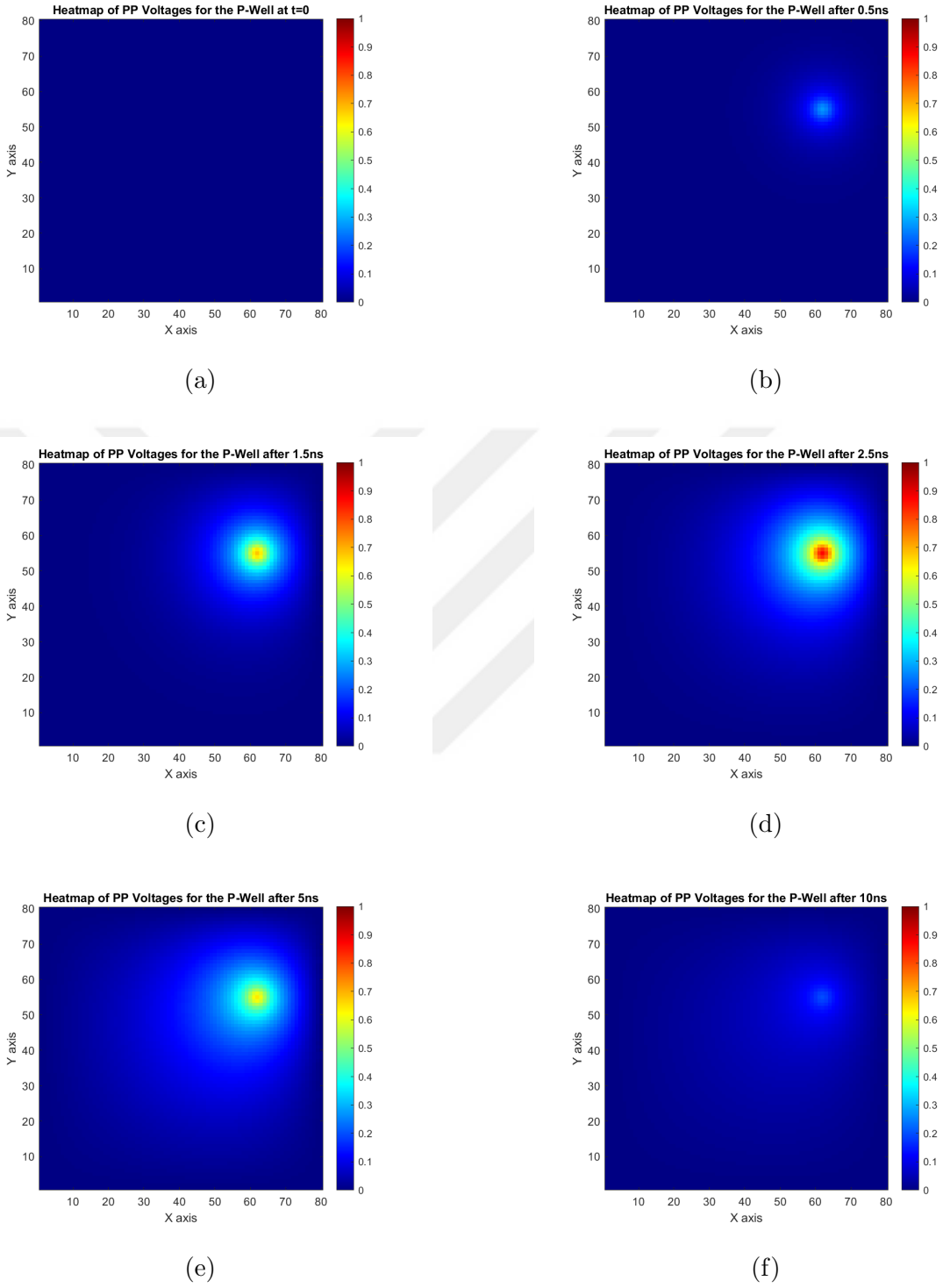
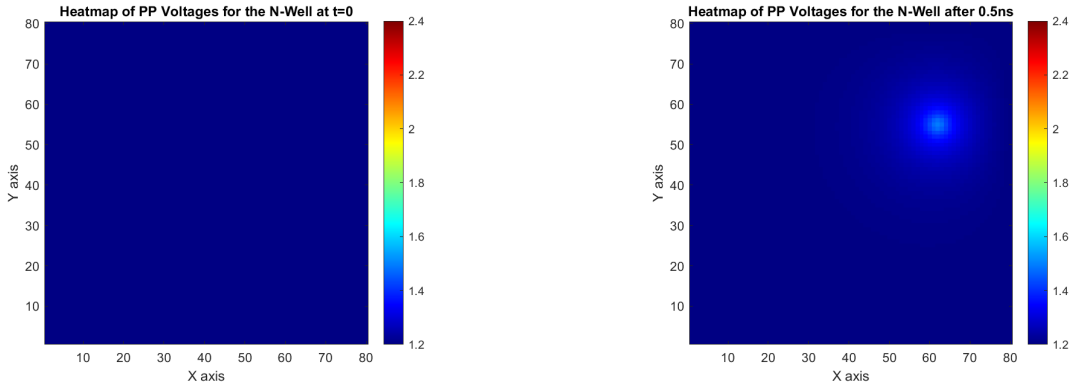
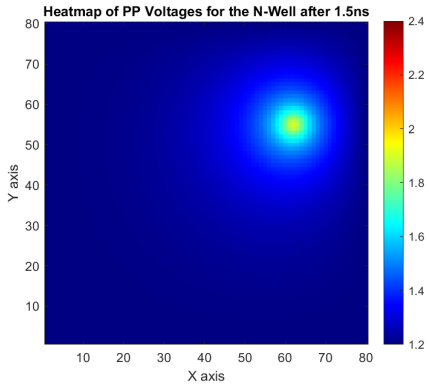


Figure 3.56: Heatmap graphs for the node voltages of the P-Well at different times during the SET test: (a) $t = 0$ ns, (b) $t = 0.5$ ns, (c) $t = 1.5$ ns, (d) $t = 2.5$ ns, (e) $t = 5$ ns, (f) $t = 10$ ns.

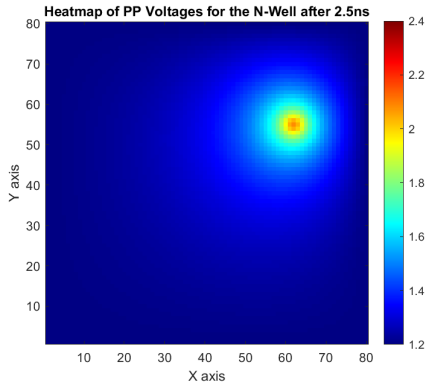


(a)

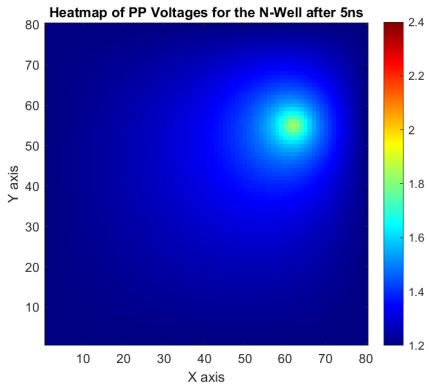
(b)



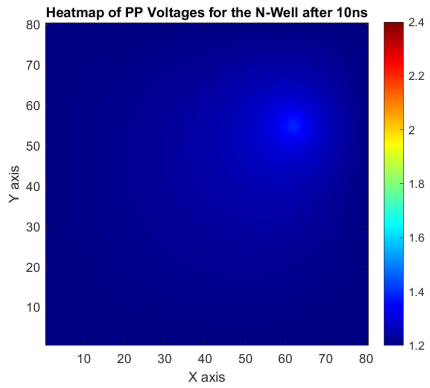
(c)



(d)



(e)



(f)

Figure 3.57: Heatmap graph at different times for the N-Well SET test: (a) $t = 0$ ns, (b) $t = 0.5$ ns, (c) $t = 1.5$ ns, (d) $t = 2.5$ ns, (e) $t = 5$ ns, (f) $t = 10$ ns.

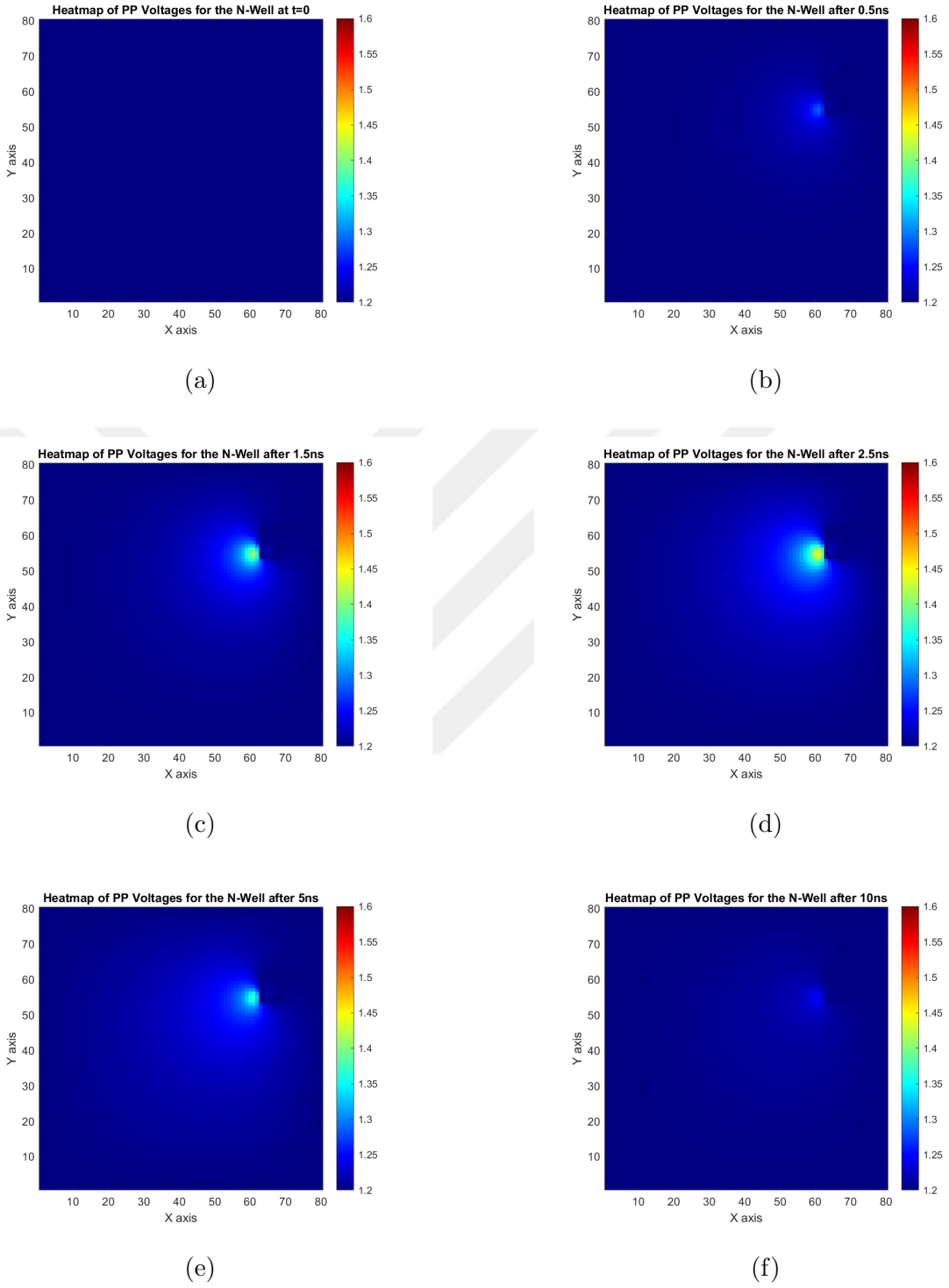


Figure 3.58: Heatmap graph at different times for the guard ring placement test: (a) $t = 0$ ns, (b) $t = 0.5$ ns, (c) $t = 1.5$ ns, (d) $t = 2.5$ ns, (e) $t = 5$ ns, (f) $t = 10$ ns.

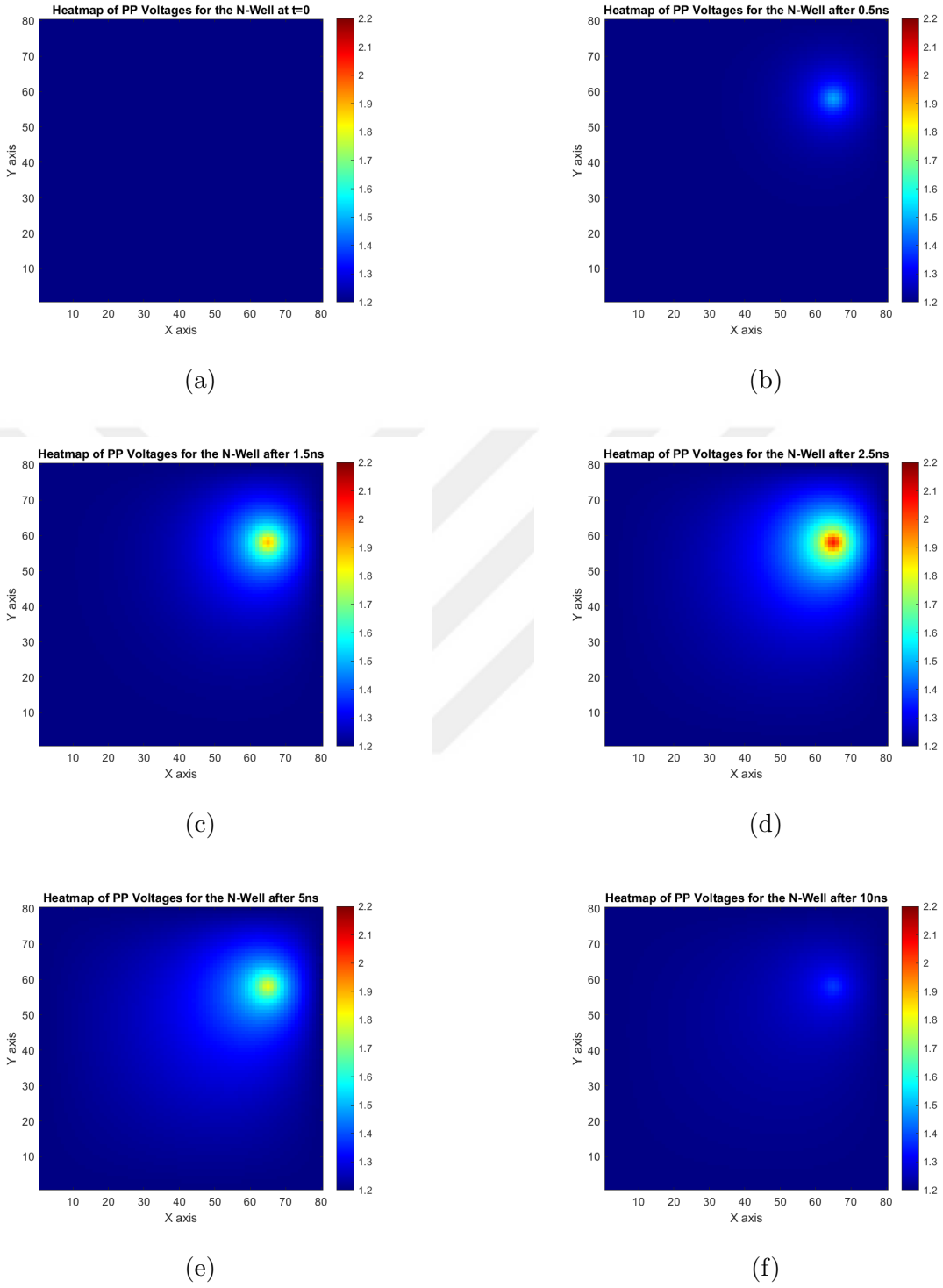


Figure 3.59: Heatmap graph at different times for the second N-Well SET test: (a) $t = 0$ ns, (b) $t = 0.5$ ns, (c) $t = 1.5$ ns, (d) $t = 2.5$ ns, (e) $t = 5$ ns, (f) $t = 10$ ns.

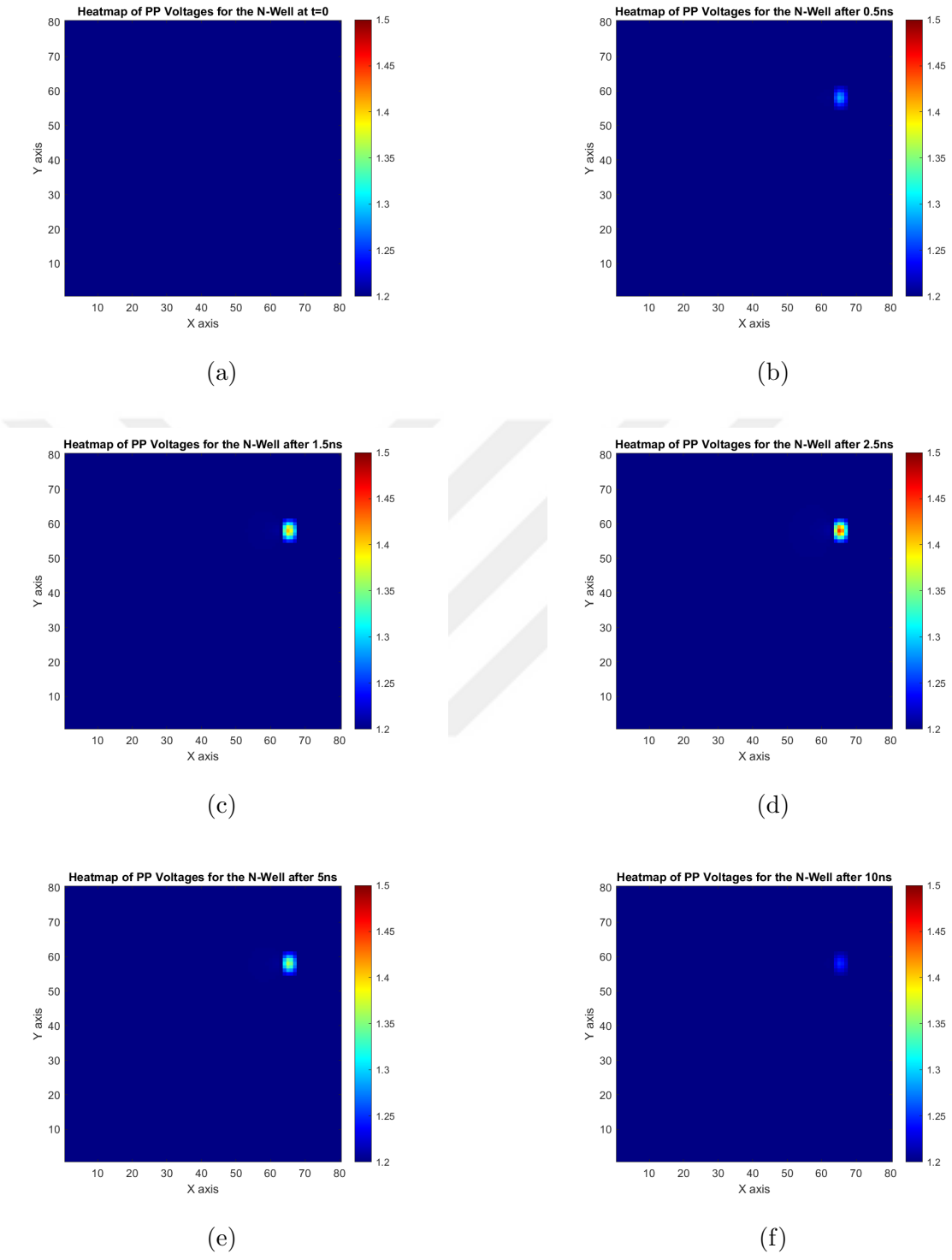
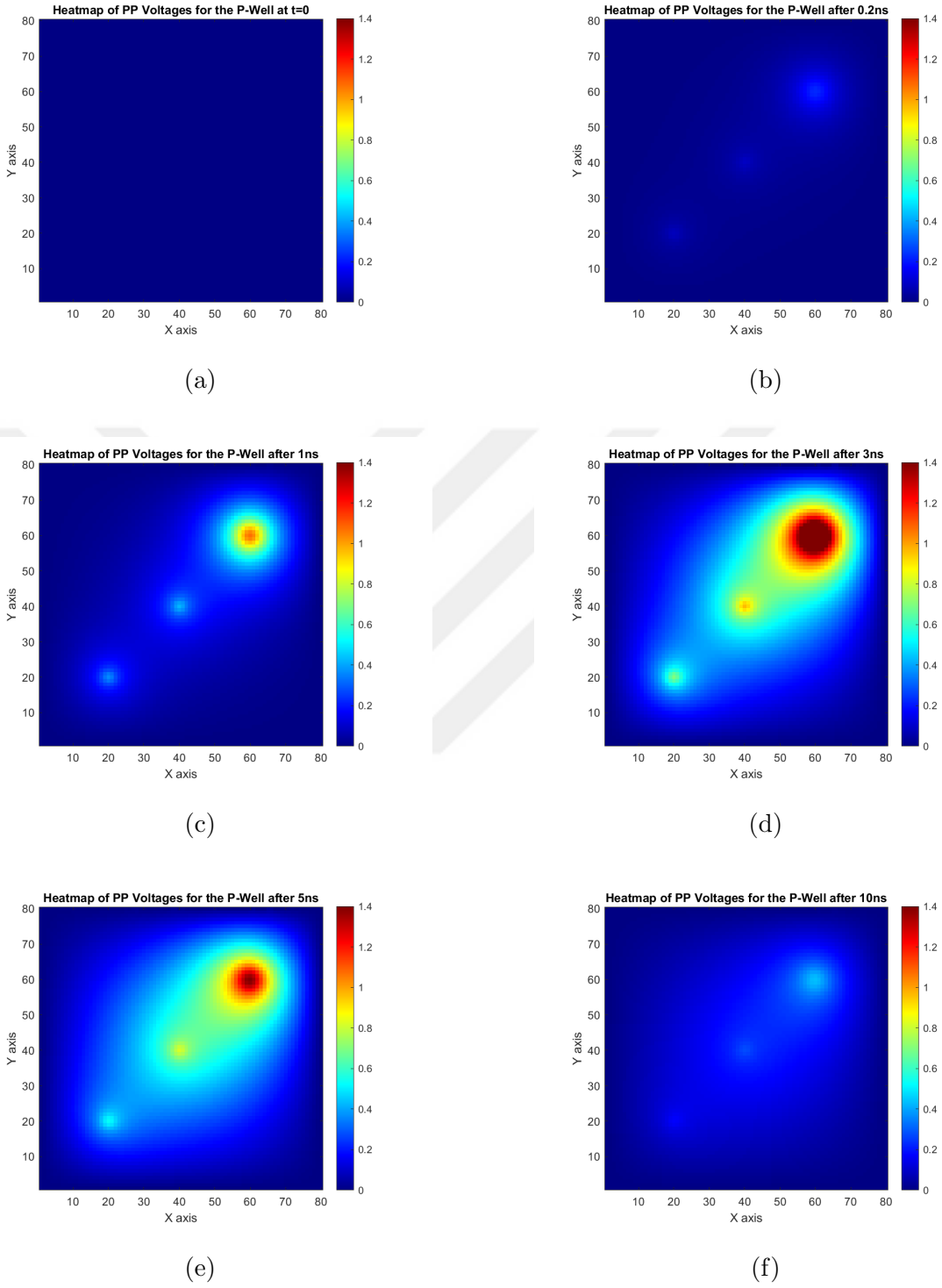


Figure 3.60: Heatmap graphs for the node voltages of the N-Well at different times during the second guard ring placement test: (a) $t = 0$ ns, (b) $t = 0.5$ ns, (c) $t = 1.5$ ns, (d) $t = 2.5$ ns, (e) $t = 5$ ns, (f) $t = 10$ ns.



(a) (b) (c) (d) (e) (f)

Figure 3.61: Heatmap graphs for the MET test of the P-Well at different times: (a) $t = 0$ ns, (b) $t = 0.2$ ns, (c) $t = 1$ ns, (d) $t = 3$ ns, (e) $t = 5$ ns, (f) $t = 10$ ns.

4. CONCLUSION AND FUTURE WORK

In conclusion, this thesis addressed the topic of simulating radiation effects on circuits through a straightforward and accessible approach. The developed tool, RadiSPICE, allows users to quickly and conveniently analyze radiation effects on their circuits.

Initially, the tool was developed and tested with various topologies including an amplifier, two bandgap reference circuits, and two comparators. Both permanent and temporary radiation effects were simulated successfully, and results were shown in histograms. After observing the overall simulations, another feature of the tool, which is revealing the sensitive parts of the circuit, was tested, in which the sensitivity tables were generated for each circuit, both for sensitive nodes and sensitive transistors. The results confirmed the tool's accuracy, as the identified sensitive elements aligned with established electronic theory.

After the circuit-level development, the tool was extended to the pre-layout stage, allowing users to identify the circuit's sensitive components before creating the layout. This early identification is valuable for reducing layout design time, given its complexity. The extension was validated using existing circuits, and the results aligned with previously generated sensitivity tables, confirming its accuracy. Additionally, a new feature was introduced, enabling users to visualize node voltages over time, providing insights into radiation effects on the substrate. This feature was used to test and verify the effectiveness of guard rings in mitigating radiation impacts.

In terms of future work, it is clear that this thesis provides a great contribution to radiation effect simulations, but there is always room for improvement such as advanced substrate modeling based on theoretical physics, which would increase the accuracy of the simulations, and automated radiation-hardened design, which would help circuit designers in a significant way.

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APPENDIX A: ABOUT THE FIGURES WITH REFERENCES

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