ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

DESIGN OF HIGH-PERFORMANCE CMOS CIRCUITS FOR INTERVAL TYPE-2 FUZZY LOGIC CONTROLLER

Ph.D. THESIS

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

ARALIK DEĞERLİ TİP-2 BULANIK MANTIK SİSTEMLERİ İÇİN YÜKSEK BAŞARIMLI CMOS DEVRE TASARIMI

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To my patient father and lovely mother

FOREWORD

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TABLE OF CONTENTS

Page

ABBREVIATIONS

ADC : Analog to Digital Converter
CCW : Counterclockwise
CM : Current Mirror
COG : Centre Of Gravity
CW : Clockwise
DT2MF : Diamond-shaped Type-2 Membership Function
FLC : Fuzzy Logic Controller
FLS : Fuzzy Logic System
FOU : Footprint Of Uncertainty
FVF : Flipped Voltage Followers
IT2FLC : Interval Type-2 Fuzzy Logic Controller
IT2FLS : Interval Type-2 Fuzzy Logic System
KM : Karnik-Mendel
LMF : Lower Membership Function
LTA : Loser Take All
LTOTA : Linearly Tunable Operational Transconductance Amplifier
LZMF : Lower Z-shape Membership Function
MAX : Maximizer
MF : Membership Function
MFLIPS : Mega Fuzzy Logic Inferences Per Second
MIN : Minimizer
NCM : NMOS Current Mirror
NPCM : NMOS Programmable Current Mirror
NT : Nie-Tan
OTA : Operational Transconductance Amplifier
PCM : PMOS Current Mirror
PID : Proportional Integral Derivative
PPCM : PMOS Programmable Current Mirror
T1FLC : Type-1 Fuzzy Logic Controller
T1FLS : Type-1 Fuzzy Logic System
T2FLC : Type-2 Fuzzy Logic Controller
T2FLS : Type-2 Fuzzy Logic System
T2MFC : Type-2 Membership Function Circuit
THD : Total Harmonic Distortion
TL : Translinear Loop
TR : Type Reduction
TSK : Takagi-Sugeno-Kang
UMF : Upper Membership Function
UZMF : Upper Z-shape Membership Function
WM : Wu-Mendel
WTA : Winner Take All
ZMF : Z-shape Membership Function

LIST OF TABLES

Page

LIST OF FIGURES

Page

DESIGN OF HIGH-PERFORMANCE CMOS CIRCUITS FOR INTERVAL TYPE-2 FUZZY LOGIC CONTROLLER

SUMMARY

Fuzzy logic has been applied to many fields, from control theory to artificial intelligence. The main application of fuzzy logic in engineering is in the area of control systems. In order to do this, fuzzy logic controllers have been proposed to control various systems implemented either in hardware or software. Due to the nature of fuzzy inference system computations, like possibility of parallel processing and its intensive calculations, the system is more appropriate to be implemented on a specialized hardware. Following that, many fuzzy logic controllers have been especially designed and implemented for different applications.

On the basis of fuzzy logic controllers type, two groups of fuzzy logic systems exist in the literature: type-1 fuzzy logic controller in which membership functions are totally certain. There are numerous number of works which have presented in this classification. The second group is called type-2 fuzzy logic controller in which membership functions are themselves fuzzy. There are limited implementation of type-2 controllers, while they have realized particular blocks of the whole system. Therefor the dissertation will focus on this type of fuzzy logic controller. The concept of type-2 fuzzy logic systems are the extension of the type-1 fuzzy logic systems which were first introduced by Zadeh. Experiments show that the type-2 fuzzy logic system may achieve better performance in comparison with type-1 fuzzy logic system because of the additional degree of freedom in their membership functions.

The dissertation consists of two main parts: first part will focus on the designing of high-performance circuits for type-2 fuzzy logic systems. In this regard, a diamond-shaped type-2 membership function is designed and implemented for a first time. Since the designed circuit is programmable in terms of slopes, upper and lower modal points, so the expert of the system can create other shapes of type-2 membership functions including rectangular, rhombus, triangular and trapezoidal.

A current-mode loser-take-all circuit is presented in the next section. The proposed circuit consists of a basic cell which allows implementation of a multi-input configuration by repeating the cell for each additional input. A high-speed feedback structure is employed to determine the minimum current among the applied inputs. Additionally, input dynamic range of the circuit can be efficiently controlled via the biasing current.

Another designed circuit is a new CMOS four-quadrant analog multiplier. High linearity, high precision and a wide dynamic range originating from the dual-translinear loop configuration are advantages of the circuit. Following that, the applicability of a new linearly tunable OTA as a basic building block for implementation of computational circuits either linear or nonlinear functions is investigated. The proposed transconductance amplifier provides a constant G_m over a wide range of input voltage which allows the implementation of high precision

computational circuits. In addition, the proposed linearly tunable OTA behaves as a bipolar OTA in which its transconductance is linearly tuned by the bias current, therefore all of the bipolar based OTA configurations can be easily replaced by the CMOS linearly tunable OTA, while their performance nearly remains the same.

Second part of the dissertation deals with realization of type-2 fuzzy logic controller using designed circuits in the first part. A current-mode two-input, single-output Takagi-Sugeno-Kang type-2 fuzzy logic controller is implemented in CMOS technology. Mixed analog/digital realization of the controller makes the design programmable and tunable (as the advantage of digital realization), while having relatively low power consumption (as the advantage of analog design), thus it can be programmed to employ in various applications. Simulation results of the controller are presented using HSPICE and level 49 parameters (BSIM3v3) in 0.35 µm technology. In order to compare the simulation results of the controller with the ideal functionality, the controller is programmed with a particular set of parameters. The simulation results are compared with the ideal results to prove the efficiency of the controller.

ARALIK DEĞERLİ TİP-2 BULANIK MANTIK SİSTEMLERİ İÇİN YÜKSEK BAŞARIMLI CMOS DEVRE TASARIMI

ÖZET

Bulanık küme teorisinin ilk olarak Lotfi A. Zadeh tarafından 1965 yılında ortaya atılması ile birlikte, keskin olmayan verilerin işlenmesi için sistematik bir yöntem olan bulanık mantıksal sistemler geliştirilmiştir. Klasik mantıksal sistemlerinin temeli "yanlış" ve "doğru" elemanlarından oluşan iki değerli kümeler iken, bulanık mantık sistemleri [0, 1] kapalı aralığında sürekli değerler alabilen çok değerli sistemlerdir. [0, 1] kümesinin sınır noktaları olan 0 ve 1 değerleri, sırasıyla klasik mantıksal sistemlerindeki "yanlış" ve "doğru" durumuna karşı gelmektedir. Bu çok değerli yaklaşım gerçek dünyada karşılaşılan bilginin genelde muğlak olması, keskin olmaması nedeniyle, fiziksel sistemlerin tanımlanmasında çok yararlı olmaktadır. Bulanık mantık tabanlı denetleyici sistemler, kısaca bulanık mantık denetleyicileri olarak adlandırılmaktadır. Bulanık mantık denetleyicileri işaret işleme, örüntü tanıma, sınıflandırma ve sistem modelleme gibi farklı mühendislik sistemlerinin analizinde kullanılmaktadır. Buna karşın bulanık mantığın en önemli mühendislik uygulaması, kontrol sistemlerinde olmuştur. Farklı sistemlerin denetlenmesi için hem yazılım tabanlı, hem de donanım tabanlı farklı bulanık denetleyiciler geliştirilmiştir. Bulanık küme işlemlerinin paralel işleme ve yoğun hesaplamalara imkan veren yapısından dolayı, bu tür sistemler özel donanım kullanılarak etkin bir şekilde gerçekleştirilebilmektedir. Bu doğrultuda, bulanık denetleyicilerin yüksek başarımlı gerçeklenmeleri için, CMOS, BJT ve BiCMOS entegre devre teknolojileri ile özel tümdevre tasarımları geliştirilmiştir.

Literatürde, iki ana bulanık mantıksal denetleyici sınıfı bulunmaktadır. Bunlardan tip-1 bulanık mantıksal denetleyicilerinde üyelik fonksiyonları tamamen belirlidir. Literatürde, bu konuda çok fazla çalışma yapılmıştır. İkinci grup denetleyiciler tip-2 tür denetleyici olarak adlandırılmaktadır ki, bu yapılarda üyelik fonksiyonları da bulanık fonksiyonlardır. Gerçekte, tip-1 bulanık mantık denetleyicileri, tip-2 türü denetleyicilerin özel hali olarak elde edilebilmektedir. Deneysel sonuçlar, tip-2 türü denetleyicilerin kullanılmasıyla, daha yüksek başarımın sağlandığını göstermektedir. Bunun temel nedeni, tip-2 türü denetleyicilerin yüksek serbestlik derecesine sahip üyelik fonksiyonları içermesi ve bu sayede sistemdeki belirsizliğin daha iyi yönetilebilmesidir.

Literatürde, tip-2 tür bulanık denetleyicilerin gerçekleştirilmesi için sınırlı sayıda çalışma bulunmaktadır. Bu çalışmalarda da, tüm sistemin özel alt blokları ele alınmıştır. Bu tezde, bu türden bir denetleyicinin içerdiği temel blokların yüksek başarımlı donanımsal gerçeklemesi üzerinde yoğunlaşılmıştır.

Tip-2 türü bulanık mantık denetleyicilerinin gerçeklenmesine üç farklı açıdan yaklaşılabilir: analog, sayısal veya karmaşık mod. Hangi yaklaşımın seçileceği, uygulamanın gerektirdiği şartlara bağlı olup, her yaklaşımın kendine göre üstünlük ve zayıflıkları bulunmaktadır. Analog denetleyiciler, sürekli-zamanlı olarak çalışmakta olup, sürekli zamanlı işaretler olan sensör ve aktuatörler çıkışları ile tam uyumlu

çalışabilmektedir. Bu sayede, doğal olarak bulanık olan analog işaretleri işlemede etkin olarak kullanılabilirler.

Buna karşın, analog devrelerin sayısal devrelere göre en önemli zayıflığı, esnek yapıda ve uyarlanabilir olmamasıdır. Programlanabilir ve esnek yapıda olmaları, sayısal bulanık mantık denetleyici gerçeklemelerin en temel üstünlüğü olarak ortaya çıkmaktadır. Bu gerçeklemeler genelde çok kullanıcılı, çok amaçlı sistem uygulamaları için kullanılır. Sayısal sistemlerde çok fazla sayıda üyelik fonksiyonları, bulanık işlemciler yer almaktadır. Öte yandan, bulanık vektörlerin ve paralel sistemlerin gösterilimi yüksek hızlı ve doğruluklu işlem gücü gerektirmektedir. Yaygın olarak bulanık mantık işlemleri ancak çok karmaşık VLSI sayısal devreler ile gerçeklenebilmektedir. Sayısal bulanık denetleyicilerin bu karmaşık yapısı yüzünden ortaya çıkan yüksek güç sarfiyatı, bu yaklaşımın en temel sorunu olarak ortaya çıkmaktadır.

Buna karşın, sayısal ve analog sistemlerin farklı açıdan birbirlerine göre üstün olan yanlarını birarada kullanmak için, bu iki yaklaşımı tek bir kırmık içinde bir araya getirmek yararlı bir yaklaşım olarak ortaya çıkmıştır. Üyelik fonksiyonlarına ilişkin parametrelerinin saklı olduğu özel alanlardan oluşan sayısal hafıza modülleri kullanılarak, bulanık bilgi programlanabilir hale getirilebilmektedir. Bu tezde, sayısal ve analog yaklaşımın bir arada kullanıldığı, karmaşık tür bulanık devre gerçeklemesine yönelik çalışmalar yer almaktadır.

Tasarımda kullanılan elektrik büyüklüğe göre, bulanık mantık denetleyicileri gerilim-modlu ve akım-modlu olarak iki ana grup altında sınıflandırılabilir: Akım-modlu devrelerin yüksek frekanslı çalışmaya uygun olma, düşük güç tüketimi ve basit iç yapı gibi özellikleri sayesinde, son on yılda bu tür devrelerin tasarımı konusunda çok fazla çalışma yer almıştır. Bu yaklaşımın diğer bir üstünlüğü, akım ile bilginin işlenmesi sayesinde, üretim belirsizliklerinin ve malzeme eşleşme hatalarının olumsuz etkilerinin azalmasıdır. Akım-modlu temel mantıksal hücreler, gerilim-modlu olarak gerçekleştirilemeyecek kadar iyi lineer davranışa sahiptir. Ayrıca, gerilim-modlu devrelerin aksine, akım-modlu devreler ile toplama ve çıkarma işlemleri kolaylıkla gerçeklenebilmektedir. Bu üstünlükleri dikkate alınarak, bu tezde bulanık mantık denetleyicisinde kullanılan devrelerin tasarımında akım-modlu yapılar üzerinde çalışılmıştır.

Tez iki ana kısımdan oluşmaktadır: ilk kısım tip-2 bulanık mantık sistemler için yüksek başarımlı devrelerin tasarımı ile ilgilidir. Bu doğrultuda, literatürde ilk defa analog bir elmas-türü tip-2 üyelik fonksiyonu tasarlanmıştır. Elde edilen devrenin tüm eğimleri programlanabilir olduğundan, sistem tasarımcısı üçgen, trapez türü gibi farklı tip-2 üyelik fonksiyonlarına ilişkin devre gerçeklemelerini de bu yapıyı düzenleyerek kolaylıkla elde edebilmektedir. Takip eden bölümde akım modlu kaybeden-hepsini-alır (loser-take-all) devresi önerilmiştir. Bu devre her giriş için yeni bir hücre ekleyerek geliştirilebilen bir mimaride olup, özellikle çok girişli devre gerçeklemelerine uygundur. Yüksek hızlı geribesleme yapısı sayesinde, girişlere uygulanabilecek işaretlerin alt sınırları belirlenmiştir. Ayrıca, devrenin giriş dinamik aralığı, kullanılan kutuplama akımlarının değerleri ile etkin bir şekilde ayarlanabilmektedir. Bunun dışında önerilen diğer bir devre, dört-bölgeli analog çarpma devresidir. Bu devrenin en temel üstünlüğü, başarımının transistorlerin gövde etkilerine, bir başka deyişle eşik gerilimindeki sapmalara daha az duyarlı olmasıdır. Devrede kullanılan translineer yapı sayesinde, devrenin diğer üstünlükleri yüksek lineerlik, yüksek doğruluk ve geniş dinamik aralık olarak ortaya çıkmıştır. Buna ilave olarak, devrenin translineer

çevrimlerde yer alan transistorların eşik gerilimlerindeki eşleşme hatalarına olan duyarlığı da incelenmiştir.

Devrenin yüksek başarımını göstermek amacıyla, devre dengeli modülatör ve frekans çiftleyici olarak çalıştırılmış ve yüksek başarımı doğrulanmıştır. Bunu takiben, bulanık mantık denetleyicisinde durulaştırıcı blok olarak kullanılabilecek yeni bir lineerliği iyileştirilmiş OTA yapısı önerilmiştir. Bu devrenin hem lineer, hem de lineer olmayan temel blokların gerçeklenmesinde nasıl kullanılabileceği araştırılmış, benzetim sonuçlarından devrenin geniş bir işaret aralığında sabit bir geçiş iletkenliğine sahip olduğu görülmüştür. Bu sayede, devre yüksek doğruluklu işlem devrelerinde kullanılabilecektir. Önerilen devrenin bir diğer avantajı geçiş iletkenliğinin kutuplama akımı ile doğrusal olarak ayarlanabilmesidir. Basit iç yapısı sayesinde, devre düşük güç harcamasına sahiptir.

Tezin ikinci kısmında, tip-2 mantıksal denetleyicinin, birinci kısımda elde edilen devreler ile gerçeklenmesi konusu ele alınmıştır. Akım-modlu iki giriş ve tek çıkışlı tip-2 Takagi-Sugeno-Kang türünden bulanık mantık denetleyicisi CMOS teknolojisinde gerçeklenmiştir. Karmaşık analog/sayısal modlu gerçekleme sistemin hem düşük güç sarfiyatına sahip olmasını, hem de programlanabilir ve ayarlanabilir olmasını sağlamıştır. 0.35 µm standard CMOS prosesi tabanlı HSPICE benzetim sonuçları denetleyicinin beklentilere uygun olarak etkin bir şekilde çalıştığını göstermiştir.

1. INTRODUCTION

Fuzzy logic is a form of multi-valued logic; it deals with reasoning that is approximate rather than fixed and exact. Compared to traditional binary sets (where variables may take on true or false values), fuzzy logic variables may have a truth value that ranges on the closed interval [0, 1], where 0 is equated with the classical false value and 1 is equated with the classical true value. Fuzzy logic has been extended to handle the concept of partial truth, where the truth value may range between completely true and completely false. Control systems acting based on this logic are called fuzzy logic controllers (FLCs).

Conventional control methods like proportional-integral-derivative (PID), robust control, adaptive control, nonlinear control methods and etc. have offered various techniques for designing controllers in dynamic systems. These methods are based on complex mathematical models in which the control system is described using one or more differential equations that define the system response to its input. However, in real-time industrial systems, it is often the case that there exist considerable difficulties in obtaining an accurate model. Even when the model is sufficiently accurate, there are many other uncertainties, for example due to the precision of the sensors, noise produced by the sensors, environmental conditions of the sensors, and nonlinear characteristics of the actuators. In such cases, model-free approaches are generally preferred for both modeling and control purposes.

Fuzzy logic is applied to problems that are either difficult to face mathematically or applications where the use of fuzzy logic provides improved performance and/or simpler implementations. Moreover its main advantages lies in the fact that it offers methods to control non-linear systems, known to be difficult to model.

Fuzzy logic was originally developed in the early 1960's by Professor Lotfi Zadeh, who claimed for a new kind of computational paradigm capable of modeling the own uncertainness of human reasoning. In 1965, Zadeh published the first ideas on fuzzy sets, the key concept in Fuzzy Logic [1]. Fuzzy logic has been developed over the past

decades into a widely applied technique in classification, control and electronics engineering.

Apart from the always-possible software implementation of FLC in a workstation, which offers the highest flexibility but the largest response time, the relative simplicity of the fuzzy algorithms makes attractive the use of hardware structures for implementing fuzzy controllers. Furthermore, fuzzy logic is well suited to low-cost implementations based on cheap sensors, low-resolution analogue-to-digital converters (ADC), and 4-bit or 8-bit microcontroller chips. Such systems can be easily upgraded by adding new rules to improve performance or add new features. In many cases, fuzzy control can be used to improve existing traditional controller systems by adding an extra layer of intelligence to the current control method.

In overall, some factors should be considered to decide whether a fuzzy-based control system is effective and beneficial to be used or not. The conditions in which fuzzy logic control is recommended can be listed as follows:

1. There is no simple mathematical model for the system, so the control process is very complex.
2. The processes are highly nonlinear.
3. Processing of linguistically formulated expert knowledge is to be performed.

On the contrary, the employment of fuzzy logic control is not recommended for case where:

1. Traditional control theory yields a satisfying result
2. High speed signal processing should be accomplished
3. An adequate and solvable mathematical model already exists
4. Very accurate and sensitive processes are required

In terms of inference process there are two main kinds of FLC: the Mamdani [2] and the Takagi-Sugeno-Kang (TSK) [3]. Since the TSK rules' consequents can have as flexible parameters per rule as input values, this translates into more degrees of freedom in the design than a Mamdani FLC, thus providing the system designer with more flexibility in the design of the system. Hence, realization of a TSK FLC is easier and more efficient than Mamdani type [4]. Hardware requirements of such controllers

are less, as well as computational complexity and power consumption. Thus, TSK type FLC is chosen to design in this dissertation.

From the design technique point of view, there are three approaches to design and implement FLC: analog, digital, and mixed-mode. Choosing of the approach mainly depends on the type of applications and required specifications, and obviously each method has some advantages and disadvantages as follows:

- **Analog Implementation**

As the advantages of the analog approach, they can perform continuous-time processing and have the particularity to be well compatible with sensors, actuators and all other analog signals. Therefore, they are obviously indicated to deal with fuzzy values, which are analog, by nature. In many cases, analog circuits can supplant digital controllers for some applications requiring low power consumption, compact and high-speed stand-alone chips.

On the contrary, analog circuits are much less flexible and adaptable than digital ones that are programmable, and they must be designed and implemented according to the structure of specific application.

Clearly, analog signals are represented either by voltages or by currents. Since voltage-mode approach makes it easier to distribute a signal in various parts of a circuit, it is more attractive.

As a drawback, voltage-mode fuzzy circuit implies a large stored energy into the node parasitic capacitances and speed is limited by charge delays of various capacitors. They are moreover penalized by a certain lack of precision because signals are sensitive to changes of supply voltages.

Voltage-mode approach needs resistors to achieve additions and to convert voltages into currents. Integrated resistors are unfortunately inaccurate, cumbersome and involve significant parasitic capacitances.

Unlike the voltage-mode approach, current-mode circuits do not need resistors and can achieve summation and subtraction in very simple way, just by wire connections. This leads to simple and intuitive configurations, which exhibits high speed and great

functional density. Current-mode circuits can also exhibit advantages as low power dissipation and low supply voltage, as good insensitivity to the fluctuation of the latter.

As a disadvantage, current-mode circuits are restricted to single fan-out; therefore current repeatability is of prime importance and the distribution of signals requires multiple current mirrors to share out signal among several operational blocks. Additionally, matching of transistors is worse than matching of capacitors or resistors.

- **Digital Implementation**

The digital implementation of fuzzy logic systems offers several advantages issued from the sound knowledge of digital circuit design and technology. Digital fuzzy processors are generally designed for multipurpose applications in order to interest a maximum of potential customers. They should thus implement a great and various number of fuzzy operators, membership functions and inference rules.

On the other hand, there are some disadvantage for digital realization. Complex representation of fuzzy vectors and parallel structures are however required to obtain accurate and fast processing. Digital implementations of common fuzzy operations leads unfortunately rapidly to complicated, enormous very large scale integration (VLSI) circuits [6, 8, 9].

- **Mixed-mode Implementation**

Fuzzy logic systems lend themselves well to analog integration, except for some control and reconfiguration structures. Several switches are thus often integrated on analog circuits and commanded by digital inputs.

It can actually be attractive to increase the complementarity between digital and analog features and to merge them into a single mixed chip, in order to improve the weak points of both. A fuzzy knowledge base can be programmed in a digital memory which consists of dedicated locations and stores a variable number of parameters characterizing membership function shapes and inference rules notably.

Another classification of fuzzy logic systems (FLS) is based on the type of FLC which is divided to two types: type-1 FLC (T1FLC) in which membership functions are totally certain. There are numerous works which have presented this classification [5–9]. The second group is called type-2 FLC (T2FLC) in which membership functions

are themselves fuzzy. Type-2 fuzzy sets and systems generalize Type-1 fuzzy sets and systems. In fact the concept of type-2 fuzzy logic systems (T2FLSs) is the extension of the type-1 fuzzy logic systems (T1FLSs) which were first introduced by Zadeh [10]. Experiments show that the T2FLS may achieve better performance in comparison with T1FLS because of the additional degree of freedom in their membership functions [11–13]. Although T2FLS cover T1FLS in many aspects, general type-2 fuzzy systems are computationally complicated and they cannot be easily implemented in software and hardware forms.

In order to reduce the complexity in computation of T2FLSs, interval type-2 fuzzy logic systems (IT2FLSs) were proposed in [14]. These fuzzy logic systems have attracted much research interest in recent years due to their ability to cope with uncertainty and robustness in comparison with ordinary T1FLSs [15, 16]. There are few implementations of type-2 controllers, therefore the dissertation will focus on this type of FLC.

In this dissertation, new high-performance circuits for IT2FLC are presented. Designing mixed analog/digital circuits provides a flexible configuration as well as a highly accurate performance, where analog circuits are employed to realize the required functions, while the programmable units are implemented using digital circuits. The current-mode approach is employed owing to the simple circuitry and intuitive configuration to design the circuits.

For a first time, design and implementation of a diamond-shaped type-2 membership function (DT2MF) is fully described. Also, a new CMOS four-quadrant analog multiplier circuit is proposed based on a pair of dual-translinear loops. Design of a current-mode loser-take-all circuit is presented to construct the fuzzy inference engine. In addition, the applicability of a new Linearly Tunable OTA (LTOTA) as a basic building block for implementation of fuzzy related circuits is introduced.

Finally, designed circuits are employed to realize IT2FLC. Simulation results of the controller are presented using HSPICE and level 49 parameters (BSIM3v3) in 0.35 µm technology. In order to compare the simulation results of the controller with ideal functionality, the controller is adjusted with a particular set of parameters. The simulation results are compared with the ideal results to prove the efficiency of the controller.

1.1 Purpose of Dissertation

Designing of high-performance circuits for IT2FLC are presented in this dissertation. Since most of the circuits consist of the basic operations (addition/subtraction, minimization/maximization, and bounded difference) the current-mode approach is preferable in the realization of fuzzy related blocks owing to the simple circuitry and intuitive configuration [8]. Moreover, potential advantages of high-speed operation due to low parasitic capacitor nodes and low power consumption highly encouraged us to employ this technique [17, 18]. Mixed analog/digital realization of the circuit provides a systematic way to program the circuit with a simple interface (as the advantages of digital realization), while having high accuracy and relatively low power consumption (as the advantages of analog design).

The following list describes the main objective of the dissertation:

- Proposing a circuit to realize DT2MF having the capability of programming in all aspects: slopes, upper and lower modal points.

- Designing a new multiplier circuit free from body-effect in order to implement the defuzzifier block of IT2FLC.

- Proposing a high-precision loser-take-all circuit with multi-input configuration which is employed to construct the inference engine of IT2FLC.

- The applicability of a new LTOTA as a basic building block for realization of analog computational circuits including squaring, square-rooting, multiplication and division of the signals.

- CMOS Implementation of IT2FLC using the designed circuits and comparing the results with the ideal outputs.

1.2 Dissertation Organization

In chapter 2, the basic concepts of fuzzy sets and systems are presented. In addition, type-1 and type-2 fuzzy logic systems are introduced to clarify the advantage of T2FLS rather than type-1 one. Moreover, three models of TSK structure are presented in section 2.5.3. Different methods of hardware realization of FLC as well as their advantages and disadvantaged are studied in the last subsection.

Chapter 3 will focus on the transistor-level design of diamond-shaped membership function which construct the fuzzifier block of the IT2FLC. The programmability of the circuit in terms of slopes, upper and lower modal points will enable the expert of the system to create other shapes of type-2 membership functions including rectangular, rhombus, triangular and trapezoidal.

In chapter 4, first we will review the former works regarding maximizer and minimizer circuits, and the advantages and drawbacks of each circuit are presented. Then a new high-precision loser take all (LTA) circuit is proposed based on a basic cell which allows realizing a multi-input configuration by repeating the cell for each additional input. A simple high-speed feedback structure determines the minimum current at the output. Additionally, input dynamic range of the circuit can be efficiently controlled via the biasing current. The designed circuit is employed to construct the inference engine of the IT2FLC.

In chapter 5, implementation of a four-quadrant analog multiplier circuit is presented. The designed circuit is based on a pair of dual-translinear loops. The significant features of the circuit are its high accuracy and high linearity, owing to the fact that the circuit relies on a new dual-translinear topology. Performance analysis of the proposed circuit is thoroughly discussed in which the harmonic distortion caused by mismatch in the input stage transistors are studied in details. The effects of mismatches in the transconductance parameters of the transistors in the dual-translinear loops as well as mismatch in the threshold voltages due to transistor body effects are fully analyzed. Finally, the input / output ranges and impedances of the proposed multiplier are derived. Following that, this chapter deals with the designing of linearly tunable OTA as a basic building block for realization of analog computational circuits including squaring, square-rooting, multiplication and division of the signals. In addition, the proposed circuit behaves as a bipolar OTA in which its transconductance

is linearly tuned by the bias current, therefore all of the bipolar-based OTA configurations can be easily replaced by the proposed CMOS OTA, while their performance nearly remains the same. The complete simulation results as well as the performance analysis are presented to verify the applicability of the circuit.

In chapter 6, complete schematic of the IT2FLC is presented. Implementation of the FLC based on the high-performance circuits explained in the previous chapters as well as some interface circuits (programmable rule base and type reducer circuits) are performed, then HSPICE simulation results are compared with the ideal results.

Finally, dissertation is concluded in chapter 7 and some scopes for future works are given.

2. BACKGROUND ON FUZZY LOGIC

This chapter provides a background overview of fuzzy sets, fuzzy logic, fuzzy logic controllers and fuzzy hardware. First, fuzzy set theory is introduced, then the basic structure of fuzzy logic system as well as its building blocks are presented. Next, different types and structures of FLCs are reviewed followed by possible methods for hardware implementation of fuzzy logic related circuits. Finally, advantages and disadvantages of each method are provided.

2.1 Fuzzy Set Theory

The classical set theory is built on the fundamental concept of "set" of which an individual is either a member or not a member.

The membership $\mu_A(x)$ of x a classical set A, as subset of the universe X, is defined by:

$$\mu_A(x) = \begin{cases} 1 & \text{iff } x \in A \\ 0 & \text{iff } x \notin A \end{cases} \qquad \textbf{(2.1)}$$

This means that an element x is either a member of set A ($\mu_A(x) = 1$) or not ($\mu_A(x) = 0$). A sharp, crisp, and unambiguous distinction exists between a member and a nonmember for any well-defined "set" of entities in this theory, and there is a very precise and clear boundary to indicate if an entity belongs to the set. In other words, when one asks the question "Is this entity a member of that set?" The answer is either "yes" or "no." This is true for both the deterministic and the stochastic cases. In probability and statistics, one may ask a question like "What is the probability of this entity being a member of that set?" In this case, although an answer could be like "The probability for this entity to be a member of that set is 90%," the final outcome (i.e., conclusion) is still either "it is" or "it is not" a member of the set. The chance for one to make a correct prediction as "it is a member of the set" is 90%, which does not mean that it has 90% membership in the set and in the meantime it possesses 10% non-membership. Namely, in the classical set theory, it is not allowed that an element is in a set and not in the set at the same time. Thus, many real-world application problems

cannot be described and handled by the classical set theory, including all those involving elements with only partial membership of a set.

On the contrary, fuzzy set theory accepts partial memberships, and, therefore, in a sense generalizes the classical set theory to some extent. In order to introduce the concept of fuzzy sets, we first review the elementary set theory of classical mathematics. It will be seen that the fuzzy set theory is a very natural extension of the classical set theory, and is also a rigorous mathematical notion.

A fuzzy set is a set with graded membership in the real interval: $\mu_A(x) \in [0, 1]$. A fuzzy set "*A*", a fuzzy subset of "*X*", is denoted by:

$$A = \sum_{i=1}^{m} \mu_A(x_i) / x_i = \mu_A(x_1) / x_1 + ... + \mu_A(x_m) / x_m \qquad \textbf{(2.2)}$$

where $\mu_A(x)$ is known as the membership function, and "*X*" known as the *universe of discourse*. When "*X*" is not finite, a fuzzy set "*A*" is defined by:

$$A = \int_X \mu_A(x) / x \qquad \textbf{(2.3)}$$

Let us consider an example for the age of the people with the labels of "OLD" and "YOUNG". In the classical logic, the characteristic functions for this example can be typically represented by:

$$\mu_{young}(x) = \begin{cases} 1 & \text{if} \quad x \le 40 \\ 0 & \text{if} \quad x > 40 \end{cases} \qquad \textbf{(2.4)}$$

and

$$\mu_{old}(x) = 1 - \mu_{young}(x) = \begin{cases} 1 & \text{if} \quad x \ge 40 \\ 0 & \text{if} \quad x < 40 \end{cases} \qquad \textbf{(2.5)}$$

It is obvious that the boundary of 40 year in this example is arbitrary. Independently of this boundary value, classical logic cannot interpret intermediate values. In this case, a graph of the membership function for the age category is shown in Figure 2.1.

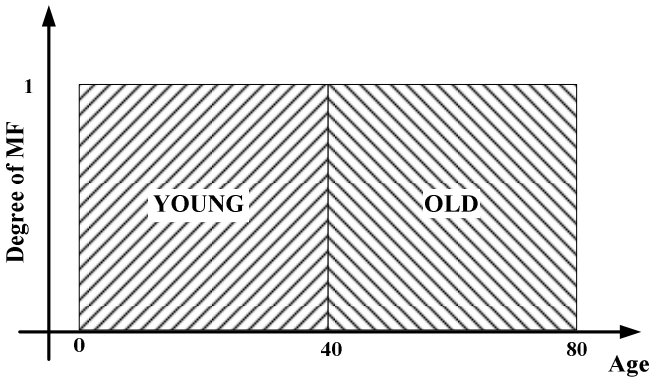


Figure 2.1 : The age category in the classical case.

According to the fuzzy logic, the problem of sharp and crisp membership functions can be solved by defining smooth membership functions. One possible definition of the membership functions can be written as follows for “YOUNG” people:

$$\mu_{young}(x) = \begin{cases} 1 & \text{if} \quad x \le 30 \\ \dfrac{50 - x}{20} & \text{if} \quad 30 < x < 50 \\ 0 & \text{if} \quad x \ge 50 \end{cases} \tag{2.6}$$

and for the “OLD” people we have:

$$\mu_{old}(x) = 1 - \mu_{young}(x) = \begin{cases} 0 & \text{if} \quad x \le 30 \\ \dfrac{x - 30}{20} & \text{if} \quad 30 < x < 50 \\ 1 & \text{if} \quad x \ge 50 \end{cases} \tag{2.7}$$

The graphic representation of these membership functions which are based on the fuzzy logic are shown in Figure 2.2.

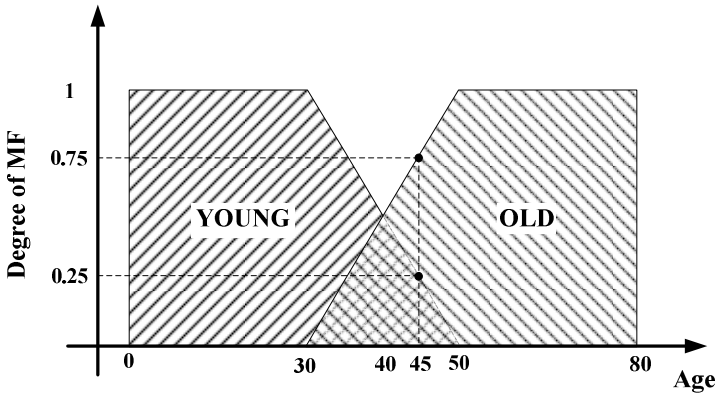


Figure 2.2 : The age category based on the fuzzy logic.

Let us consider a person whose age is 45; considering the classical membership function, the person is an “OLD” man! However, we know that it cannot really be right. According to the fuzzy membership functions presented in Figure 2.2, a 45 years old person belongs 25% to “YOUNG” and 75% to “OLD” which is an acceptable result.

Defining another label between the “YOUNG” and “OLD” can help us to have a better classification of the people. For the classical logic, the graph of Figure 2.3 can be considered in which it consists of three labels. The same classification is carried out for the membership functions based on the fuzzy logic shown in Figure 2.4. In this figure, the ages between 25 and 35 belong to two membership functions; “YOUNG” and “MIDDLE”. Similarly, the ages between 45 and 55 belong to “MIDDLE” and “OLD” membership functions and finally the ages between 35 and 45 belongs to three membership functions. Consider the previous example for a person with 45 years old; in the classical category, the person is classified in the middle-aged group while in the fuzzy logic he/she belongs to both “MIDDLE” and “OLD” membership functions. He/she is an “OLD” with the weight of 0.5; on the other hand, he/she is “MIDDLE” with the weight of 0.75, while his/her “YOUNG” weight is zero. We see that the fuzzy logic allows gradual membership to better adapt for our subjective criteria.

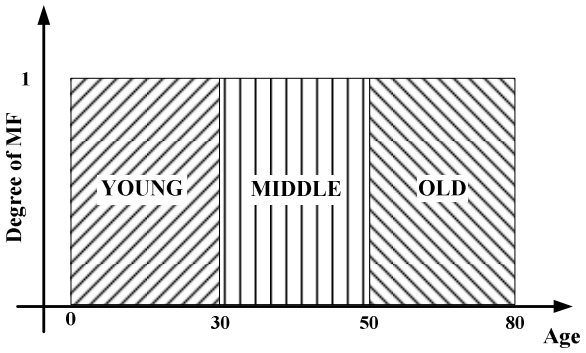


Figure 2.3 : The classical age category with more precision.

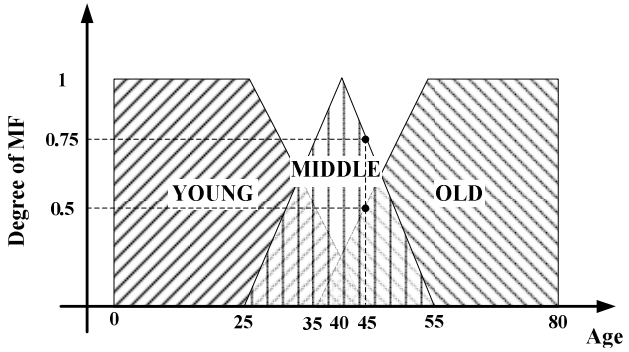


Figure 2.4 : The age category based on the fuzzy logic with three labels.

2.2 Fuzzy Membership Functions

A fuzzy set is completely characterized by its membership function (MF). A membership function for a fuzzy set "*A*" on the universe of discourse "*X*" is defined as $\mu_A: X \rightarrow [0, 1]$, where each element of "*X*" is mapped to a value between 0 and 1. This value, called membership value or degree of membership, quantifies the grade of membership of the element in "*X*" to the fuzzy set "*A*".

A more convenient and concise way to define a membership function is to express it as a mathematical formula. There are different shapes of membership functions which are mostly used in the fuzzy sets and systems:

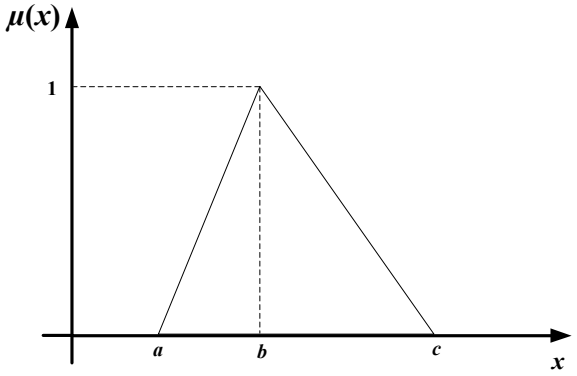


Figure 2.5 : Triangular membership function.

- **Triangular Membership Function:** Figure 2.5 demonstrates the shape of this membership function which is specified by three parameters {*a*, *b*, *c*} as follows:

$$\mu_A(x) = \begin{cases} 0 & x \le a \\ \dfrac{x-a}{b-a} & a \le x \le b \\ \dfrac{c-x}{c-b} & b \le x \le c \\ 0 & c \le x \end{cases} \qquad \textbf{(2.8)}$$

- **Trapezoidal Membership Function:** This shape of membership function which is depicted in Figure 2.6 specified by four parameters {*a*, *b*, *c*, *d*} as follows:

$$\mu_A(x)=\begin{cases}0 & x\le a\\ \dfrac{x-a}{b-a} & \mathrm{a}\le x\le b\\ 1 & \mathrm{b}\le x\le c\\ \dfrac{d-x}{d-c} & \mathrm{c}\le x\le d\\ 0 & d\le x\end{cases} \qquad \textbf{(2.9)}$$

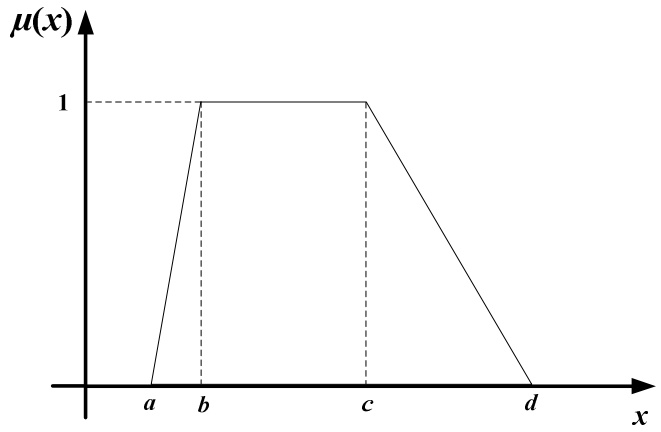


Figure 2.6 : Trapezoidal membership function.

- **Gaussian Membership Function:** A Gaussian membership function is completely determined by c and σ (see Figure 2.7); c represents the MFs center and σ determines the membership functions width:

$$\mu_A(x)=e^{-\frac{1}{2}\left(\frac{x-c}{\sigma}\right)^2} \qquad \textbf{(2.10)}$$

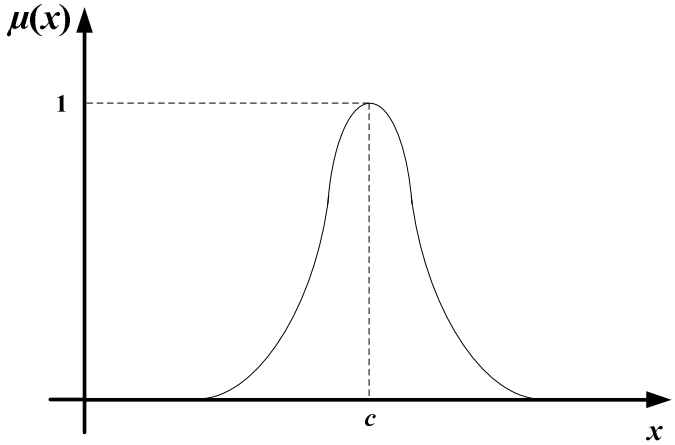


Figure 2.7 : Gaussian membership function.

- **Rational-Powered Membership Functions:** These functions are general form of triangular/trapezoidal forms membership functions. Figure 2.8 shows typical shapes of this function. Mathematically, the i[th] rational-powered membership function of the j[th] input (x_j) can be modeled as:

$$\mu_A(x_j)=\begin{cases}(1+\dfrac{x_j-c_i}{b_i^-})^{a_i^-} & \text{if } c_i-b_i^- \le x_j \le c_i \\ (1-\dfrac{x_j-c_i}{b_i^+})^{a_i^+} & \text{if } c_i \le x_j \le c_i+b_i^+ \\ 0 & \text{otherwise}\end{cases} \qquad \textbf{(2.11)}$$

where c_i is modal point, b_i^+ and b_i^- are upper and lower half-widths and a_i^+ and a_i^- are their powers, respectively. For an especial case of $a_i^+=a_j^-=1$; the function reduces to straight lines and the membership function is triangular.

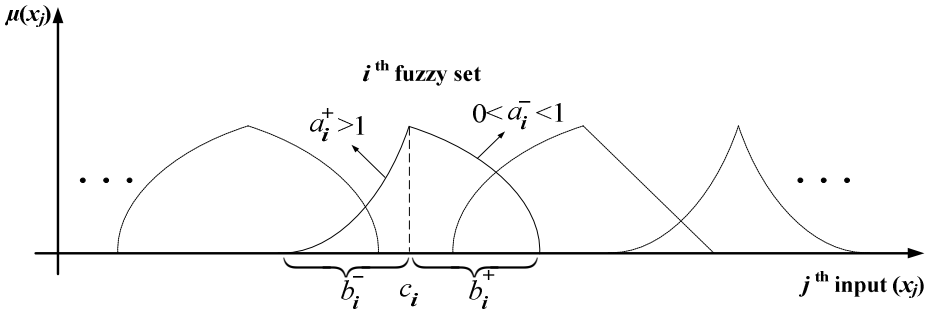


Figure 2.8 : Rational-powered membership functions.

2.3 Type-1 Fuzzy Logic Controller

The basic structure of a T1FLC is depicted in Figure 2.9. As seen, a T1FLC comprises four principal components, which are fuzzifier, rule base, fuzzy inference engine, and defuzzifier. The operation of T1FLC is as follows:

The crisp inputs (u_1, u_2, ..., u_n) are converted to fuzzy sets in the "fuzzifier" block. Fuzzy rules which are in the form of "IF-THEN" are considered in the rule base block. The "inference engine" uses the fuzzy rules to produce fuzzy conclusions, and finally the "defuzzifier" block can then convert the fuzzy outputs from the inference engine in order to produce crisp outputs (y_1, y_2, ... , y_n). In the following subsection, each of the four principal components will be described in detail to show how the fuzzy mathematical and logic principles are used in FLCs.

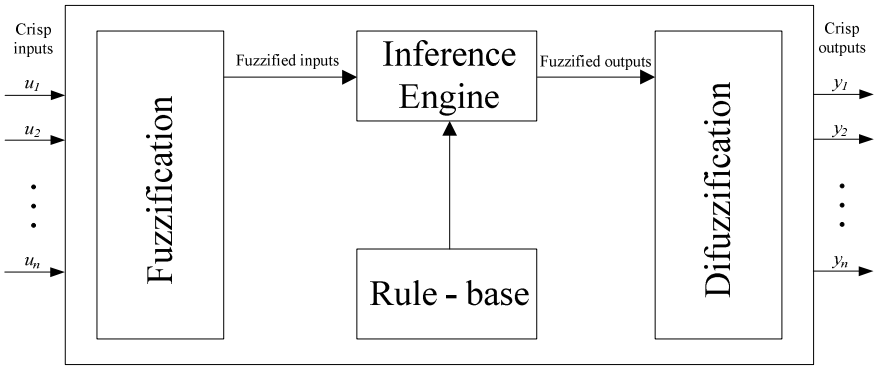


Figure 2.9 : Basic structure of a type-1 fuzzy logic system.

2.3.1 Fuzzifier

The fuzzifier block maps the input crisp numbers into the fuzzy sets to obtain degrees of membership. It is needed in order to activate rules, which are in terms of the linguistic variables. Each linguistic variable is considered as a suitable shape of membership function.

2.3.2 Rule base

Fuzzy logic based systems use “rules” to represent the relationship between observations and actions. These rules consist of a precondition (IF-part) and a consequence (THEN-part). The precondition can consist of multiple conditions linked together with AND or OR conjunctions. The rule structure of T1FLS with p inputs ($x_1 \in X_1, \ldots, x_p \in X_p$) and one output $y \in Y$ is as follows:

$$\textit{Rule } l^{th} : \textit{IF } x_1 \textit{ is } A_{1l} \textit{ and } \ldots \textit{ and } x_p \textit{ is } A_{pl} \textit{ Then } y \textit{ is } B \qquad \textbf{(2.12)}$$

where $l = 1,\ldots,M$; and M is the number of rules and $A_1,\ldots,A_p$ are the values for each input linguistic variables in the universes of discourse. This rule represents a relation between the input space $X_1 \times \ldots \times X_p$, and the output space, Y, of the fuzzy logic system.

2.3.3 Fuzzy inference engine

The fuzzy inference engine combines rules and gives a mapping from fuzzy sets in the input universe of discourse to fuzzy sets in the output universe of discourse based on the fuzzy logic principle. In the inference engine, multiple antecedents in the rules are connected using AND operation, and the degree of membership in the input sets are

combined using those in the output sets using sub-star composition, described in detail in [19] . Multiple rules are combined then by using a join operation.

2.3.4 Defuzzifier

The defuzzification process is used to transfer fuzzy sets into a crisp value. There are several defuzzifier methods in the literature. For engineering applications, the criterion for the choice of a defuzzifier is computational simplicity, such as maximum, centroid, center-of-sums, center average (also called the height defuzzifier [20], [21]), modified height, and center of sets. Centre of gravity (COG) is one of the most popular simple methods for defuzzification process. One of the important advantages of the COG method is that all activated membership functions of the consequents (all active rules) take part in the defuzzification process [22]. The COG method works based on the following equation for transferring fuzzy scheme into a crisp value [23]:

$$COG = \frac{\sum_{i=1}^{n} x_i \mu_A(x_i)}{\sum_{i=1}^{n} \mu_A(x_i)} \qquad \textbf{(2.13)}$$

where n is the number of the discrete elements in the universe of discourse, x and $\mu_A(x_i)$ are the output fuzzy variable and its membership function degree due to the consequent fuzzy rules, respectively. $\mu_A(x_i)$ value greatly depends on the shape, type and distribution of MFs.

2.4 Types of Fuzzy Systems

In fuzzy control, two types of fuzzy systems can be distinguished based on the form of the rules: Mamdani rules and Sugeno rules. The Sugeno rules are based on a different principle: the consequents of those rules are (linear) functions of the controller inputs. These two types of fuzzy rules are described in the following sections.

2.4.1 Mamdani type fuzzy systems

This type of fuzzy rule was used in the first reported applications of fuzzy control [2] and has the following general form:

$$\textit{Rule } l^{th}\textit{: IF } x_1 \textit{ is } A_1 \textit{ and}\ldots\textit{and } x_p \textit{ is } A_p \textit{ Then } y_1 \textit{ is } B_1 \textit{ and } \ldots \textit{ and } y_p \textit{ is } B_p \qquad \textbf{(2.14)}$$

2.4.2 Sugeno type fuzzy systems

Another type of fuzzy system is referred to as Sugeno rules, because of the introduction of this type of rule by Takagi, Sugeno and Kang [3] which was further exploited by Sugeno and co-workers. The general form of TSK rule is as follows:

$$\textit{Rule } l^{th}\textit{ : IF } x_1 \textit{ is } A_1 \textit{ and } \ldots \textit{ and } x_p \textit{ is } A_p \textit{ Then } y=f_1(x_1,\ldots,x_2) \qquad \textbf{(2.15)}$$

which shows that the consequents of these fuzzy rules are functions of the controller inputs. A simple expression is the linear functions as follows:

$$\textit{Rule } l^{th}\textit{ : IF } x_1 \textit{ is } A_1 \textit{ and } \ldots \textit{ and } x_p \textit{ is } A_p \textit{ Then } y=a_1x_1+\ldots+ a_px_p+ a_0 \qquad \textbf{(2.16)}$$

From (2.16), if $a_1,\ldots, a_p= 0$, then the system is called *zero-order* TSK and if $a_1,\ldots, a_p\neq 0$, then the system mapping is linear so it is called *first-order* TSK.

It should be pointed out that in the view of circuit implementation, realization of a TSK type FLC is easier and more efficient than Mamdani type [4]. Hardware requirements of such controllers are less, as well as computational complexity and power consumption. Moreover, the following are some advantages of Sugeno method in comparison with Mamdani type:

- **Advantages of the Sugeno Method**

It is computationally efficient.

It works well with linear techniques (e.g., PID control).

It works well with optimization and adaptive techniques.

It has guaranteed continuity of the output surface.

It is well suited to mathematical analysis.

- **Advantages of the Mamdani Method**

It is intuitive.

It has widespread acceptance.

It is well suited to human input.

2.5 Type-2 Fuzzy Logic System

The architecture of the T2FLS is demonstrated in Figure 2.10. It is seen that this structure is similar to the T1FLS presented in the previous section. The main structural difference is that the defuzzifier block of a T1FLS is replaced by the type reduction (TR) followed by defuzzification [30]. This difference will be discussed in subsection of 2.5.2.4.

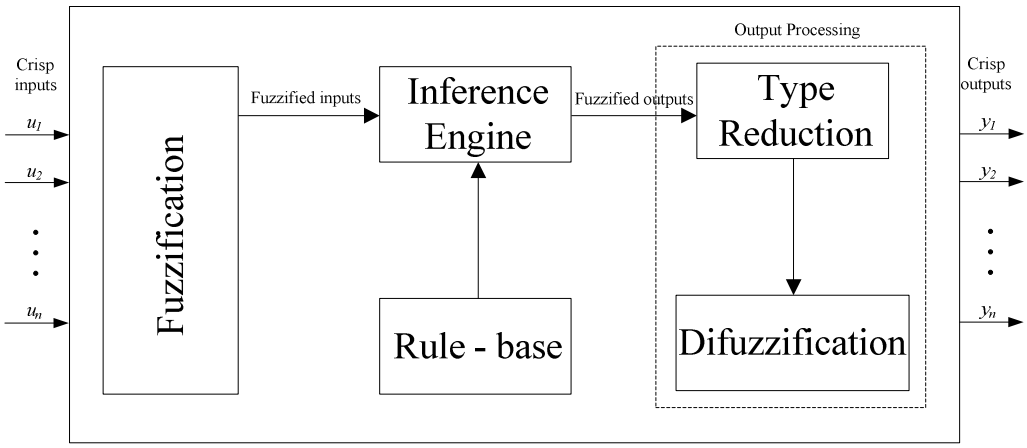


Figure 2.10 : Basic structure of a type-2 fuzzy logic system.

2.5.1 Type-2 fuzzy sets

A type-2 fuzzy set is characterized by a fuzzy membership function, i.e., the membership grade for each element of this set is a fuzzy set in [0,1], unlike a type-1 set where the membership grade is a crisp number in [0,1].

A type-2 fuzzy set $\tilde{A}$, may be represented as [28]:

$$\tilde{A} = \{((x,u), \mu_{\tilde{A}}(x,u)) \mid \quad \forall x \in X \quad \forall u \in J_x \subseteq [0,1]\} \tag{2.17}$$

where $\mu_{\tilde{A}}(x,u)$ is the type-2 fuzzy membership function in which $0 \leq \mu_{\tilde{A}}(x,u) \leq 1$. $\tilde{A}$ can also be defined as [28]:

$$\tilde{A}=\int_{x\in X}\int_{u\in J_x}\mu_{\tilde{A}}(x,u)/(x,u) \qquad J_x\subseteq[0,1]\} \tag{2.18}$$

where $\int\int$ denotes union over all admissible x and u. J_x is called primary membership of x [31]. Additionally, there is a *secondary membership* value corresponding to each primary membership value that defines the possibility for primary memberships [14]. Whereas the secondary membership functions can take values in the interval of [0,1] in generalized T2FLSs, they are uniform functions that only take values of 1 in interval T2FLSs.

An example of a type-2 principal MF is the Gaussian MF depicted in Figure 2.11, whose vertices have been assumed to vary over some interval of value. The footprint of uncertainty (FOU) associated with this type-2 MF is a bounded shaded region determined in the figure.

An upper membership function and a lower membership function are two type-1 membership functions that are the bounds for the FOU of a type-2 fuzzy set [30]. A special case of type-2 fuzzy set which is called interval type-2 fuzzy set, will be studied in the following subsection.

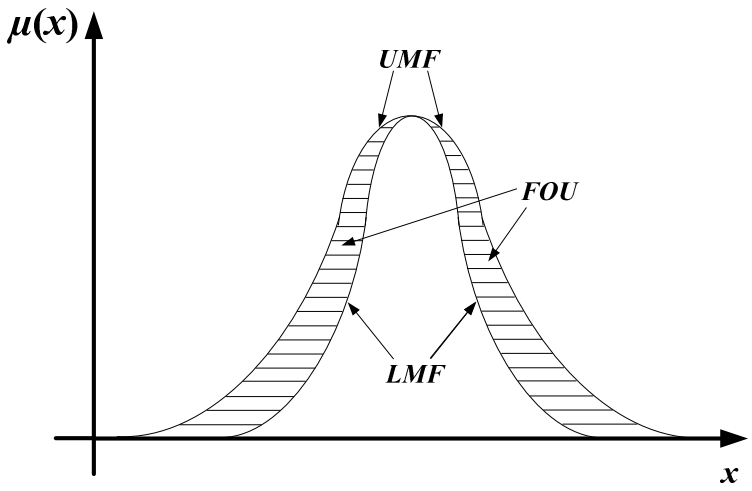


Figure 2.11 : Gaussian type-2 membership function.

2.5.2 Interval type-2 fuzzy sets

Interval type-2 fuzzy sets have received the most attention because the mathematics that is needed for such sets is much simpler than the mathematics which is needed for general type-2 fuzzy sets.

If all $\mu_{\tilde{A}}(x,u)$ are equal to 1, then $\tilde{A}$ is an interval T2FLS. The special case of (2.3) might be defined for the interval T2FLSs:

$$\tilde{A}=\int_{x\in X}\int_{u\in J_x} 1/(x,u) \qquad J_x \subseteq [0,1]\} \tag{2.19}$$

2.5.2.1 Type-2 fuzzy membership functions

2.5.2.2 Rule base

The structure of the rules in a T2FLS remains the same as in T1FLS, but in T2FLS some or all of the MFs are type-2. The rule structure of T2FLS with p inputs ($x_1 \in X_1,\ldots,$ $x_p \in X_p$) and one output $y \in Y$ is as follows:

$$\textit{Rule } l^{th} \textit{ : IF } x_1 \textit{ is } \tilde{A}_1^l \textit{ and } \ldots \textit{ and } x_p \textit{ is } \tilde{A}_p^l \textit{ Then } y \textit{ is } B \tag{2.20}$$

where $l = 1,\ldots,M$; and M is the number of rules. This rule represents a type-2 relation between the input space $X_1 \times \ldots \times X_p$, and the output space, Y, of the type-2 fuzzy logic system.

2.5.2.3 Fuzzy inference mechanism

The inference block in the type-2 fuzzy logic system is very similar to type-1. This block combines rules and then gives a mapping from input T2FSs to output T2FSs. In type-2 fuzzy sets, join (⊓) and meet operators (⊔) are used instead of union and intersection operators. These two new operators are used in secondary membership functions, and they are defined and explained in detail in [19].

2.5.2.4 Type reduction

The type-2 fuzzy outputs of the inference engine are transformed into type-1 fuzzy sets that are called *the type-reduced sets*.

Type-reduction methods include: centroid, center-of-sums, height, modified height, and center-of-sets. Let's assume that we perform centroid type-reduction. Then each element of the type-reduced set is the centroid of some embedded type-1 set for the output type-2 set of the fuzzy logic system. Each of these embedded sets can be thought as an output set of an associated T1FLS, and correspondingly, the T2FLS can be

viewed of as a collection of many different T1FLSs. Each T1FLS is embedded in the T2FLS; hence, the type-reduced set is a collection of the outputs of all of the embedded T1FLSs.

2.5.2.5 Defuzzification

The outputs of the type reduction block are applied to defuzzificaton block. The type-reduced sets are determined by their left end point and right end point, then the defuzzified value is calculated by the average of these points.

There are different methods for type reduction including Karnik-Mendel (KM) method [32], Wu-Mendel (WM) method [33], Nie-Tan (NT) method [34] etc. Since the NT method has the precise computation and also benefits from simple and intuitive configuration, then it is preferred to another methods. It is based on taking average of the lower and upper MFs of the interval set as follows [34]:

$$\mu_{TR} = \frac{1}{2}\left(\overline{\mu}(x_i) + \underline{\mu}(x_i)\right) \tag{2.21}$$

where $\overline{\mu}(x_i)$ and $\underline{\mu}(x_i)$ are the membership grades of the upper and the lower membership functions respectively. In this case the defuzzified output is obtained as [35]:

$$COG = \frac{\sum_{i=1}^{n} x_i \mu_A(x_i)}{\sum_{i=1}^{n} \mu_A(x_i)} \tag{2.22}$$

where COG is the defuzzified value, $\mu_A(x_i)$ is the activation degree of i^{th} rule, x_i is the weight of rule, and finally i and n represent the number of rules.

2.5.3 Type-2 TSK fuzzy logic system

As we mentioned in section 2.4, two kinds of FLSs exist in the literature, TSK and Mamdani. Both of them are characterized by IF-THEN rules and have the same antecedent structures. They differ in the structures of their consequents. The

consequent of a Mamdani rule is a fuzzy set, while the consequent of a TSK rule is a function.

For type-2 TSK models, there are three possible structures [36]:

1. Antecedents are type-2 fuzzy sets, and consequents are type-1 fuzzy sets. This is the most general case, and it is named A2-C1.
2. Antecedents are type-2 fuzzy sets, and consequents are crisp numbers. This is a special case of A2-C1, and it is named A2-C0.
3. Antecedents are type-1 fuzzy sets, and consequents are type-1 fuzzy sets. This is another special case of A2-C1, and it is named A1-C1.

Take notice that A and C represent the antecedent and consequent of fuzzy rules, 0, 1 and 2 represent the crisp number, type-1 and type-2 fuzzy sets, respectively. In this Ph.D. dissertation, because of the simple circuit implementation, A2-C0 TSK structure is used, therefore only A2-C0 TSK structure will be explained in detail.

2.5.3.1 A2-C0 structure of type-2 TSK

In a type-2 TSK A2-C0 structure with a rule base of M rules, with each rule having p antecedents, the l^{th} rule is denoted as:

$$Rule\ l^{th}: IF\ x_1\ is\ \tilde{A}_1^l\ and \ldots and\ x_p\ is\ \tilde{A}_p^l\ Then\ y^l = a_{1l}x_1 + \ldots + a_{pl}x_p + a_{0l} \quad \textbf{(2.23)}$$

where $l = 1,\ldots,M$, a_{il} ($i = 0,1,\ldots, p$) are the consequent parameters that are crisp numbers; y^l is an output and $\tilde{A}_i^l$ are type-2 fuzzy sets. The final output of the model can be written as follows [36]:

$$Y(F_1,\ldots,F_M) = \int_{f_1}\ldots\int_{f_M} \tau_{l=1}^{M} \mu_{\tilde{F}}(f_l) \Big/ \frac{\sum_{l=1}^{M} f_l y^l}{\sum_{l=1}^{M} f_l} \quad \textbf{(2.24)}$$

where M is the number of fired rules, $f_l \in F_l$, and τ indicates the t-norm.

For the interval type-2 TSK, the output of the A2-C0 structure rearranged as follows:

$$Y_{A2-C0} = \int_{f_1 \in [\underline{f}^1, \overline{f}^1]} \cdots \int_{f_M \in [\underline{f}^M, \overline{f}^M]} 1 \Big/ \frac{\sum_{l=1}^{M} f_l y^l}{\sum_{l=1}^{M} f_l} \tag{2.25}$$

where $\overline{f}^l$ and $\underline{f}^l$ are given by:

$$\overline{f}^l = \underline{\mu}_{\tilde{A}_1^l}(x_1) * \ldots * \underline{\mu}_{\tilde{A}_p^l}(x_p) \tag{2.26}$$

$$\underline{f}^l = \overline{\mu}_{\tilde{A}_1^l}(x_1) * \ldots * \overline{\mu}_{\tilde{A}_p^l}(x_p) \tag{2.27}$$

where * represents the *t-norm* which is the product operator in this study. The output of the IT2FLS is achieved in a closed-form via the NT inference engine given in [34] as follows:

$$Y_{TSK} = \frac{\sum_{l=1}^{M} \underline{f}_l u^l}{\sum_{l=1}^{M} \underline{f}_l + \sum_{l=1}^{M} \overline{f}^l} + \frac{\sum_{l=1}^{M} \overline{f}_l u^l}{\sum_{l=1}^{M} \underline{f}_l + \sum_{l=1}^{M} \overline{f}^l} \tag{2.28}$$

$$Y_{TSK} = \frac{\sum_{l=1}^{M} (\underline{f}_l + \overline{f}_l) u^l}{\sum_{l=1}^{M} \underline{f}_l + \sum_{l=1}^{M} \overline{f}^l} \tag{2.29}$$

2.6 Fuzzy Hardware

From the design technique point of view, there are three approaches to design and implement FLC: analog, digital, and mixed-mode. Choosing of the approach mainly depends on the type of applications and required specifications, and obviously each method has some advantages and disadvantages which is briefly discussed in the next section (This section is adopted from [37]).

2.6.1 Analog implementations of fuzzy logic circuits

Analog approach present several advantages in comparison with digital ones, especially regarding power consumption, speed of processing and functional density.

Moreover analog circuits can perform continuous-time processing and have the particularity to be well compatible with sensors, actuators and all other analog signals. Therefore, they are obviously indicated to deal with fuzzy values which are analog by nature. Some continuous representations of symbolic membership functions and some non-linear fuzzy operations can be easily synthesized using transistor characteristics. Analog circuits can supplant digital controllers for some applications requiring low power consumption, low cost, compact and high-speed stand-alone chips. Analog controllers can achieve fuzzy real-time reasoning with a large amount of fuzzy implications, especially when no high-level accuracy is needed. Precision of fuzzy systems is actually not always so important since there is no thorough mathematical background usable to define precise and exhaustive fuzzy methods. Consequently, imprecise but adjustable analog devices are suitable for a great number of cases (tunable membership functions are thus needed to optimize the performance).

On the contrary, the analog circuits suffer nevertheless of the lack of reliable memory cells. They are consequently not well appropriate to pipeline structures and have very restricted programmability possibilities. Stable and low-noise analog technologies must be used in order to design analog circuits having sufficient accuracy with wide frequency range. They are nevertheless much less flexible and adaptable than digital ones that are programmable, and they must be designed and implemented according to the structure of a specific application. Fortunately, the nature of fuzzy variable systems requires extensive parallelism which make analog circuits well appropriate to proceed high- speed numerous inferences and also limits the problem of error accumulation. A basic programmability is afforded when some analog external parameters can be adjusted or when some binary inputs allow the control of internal switches.

Clearly, analog signals are represented either by voltages or by currents. Each one can be preferred to other based on their advantages and drawbacks.

2.6.1.1 Voltage-mode implementation

Since voltage-mode approach makes easy to distribute a signal in various parts of a circuit, thus it is attractive.

As a drawback, voltage-mode fuzzy circuit implies a large stored energy into the node parasitic capacitances and speed is limited by charge delays of various capacitors.

They are moreover penalized by a certain lack of precision because signals are sensitive to changes of supply voltages. This is especially significant when the voltage range is restricted in order to limit transistor functioning to a small parts of their characteristic, or when the electrical consumption should be limited. The problems mainly lie in the sizing of some components.

Several functions are very difficult to build in voltage-mode, and it is also true for some basic ones as the algebraic sum. The voltage-mode approach needs resistors to achieve additions and to convert voltages into currents. Integrated resistors are unfortunately inaccurate, cumbersome and involve significant parasitic capacitances. This approach implies high-power dissipation and large chip area, and leads to high-costs implementations.

2.6.1.2 Current-mode implementation

Unlike the voltage-mode approach, the current-mode circuits do not need resistors and can achieve summation and subtraction in very simple way, just by wire connections. This leads to simple and intuitive configurations, which exhibits high speed and great functional density. They are used more and more, especially for systems requiring a high level of interconnectivity (neural networks for example). High speed is provided when capacitive nodes are not subject to great voltage fluctuations. Current-mode circuits can also exhibit advantages as low power dissipation and low supply voltage, as good insensitivity to the fluctuation of the latter. As another important advantage, since the signals are distributed as currents, the effect of process uncertainties and device mismatches are decreased. The basic logic cells exhibit good linearity which cannot be easily achieved in voltage-mode, and lead to fuzzy integrated systems which are globally smaller than in voltage-mode.

As a disadvantage, current-mode circuits are restricted to single fan-out; therefore current repeatability is of prime importance and the distribution of signals requires multiple current mirrors to share out signal among several operational blocks.

2.6.2 Digital implementations of fuzzy logic circuits

The digital implementation of fuzzy logic systems offers several advantages issued from the sound knowledge of digital circuit design and technology. Several mature CAD tools allow relatively easy design automation (synthesis & simulation) reducing

consequently time and cost of development. The automatic regeneration of logic levels involves high noise immunity and low sensitivity to the variances of transistor characteristics. This provides accurate and reliable data and signal processing.

Digital fuzzy processors are generally designed for multipurpose applications in order to interest a maximum of potential customers. They should thus implement a great and various number of fuzzy operators, membership functions and inference rules. This make them rather efficient for a large range of applications, provided that appropriate programming is possible (which supposes an appropriate internal or external memory).

On the other hand there are some disadvantage for digital realization. Complex representation of fuzzy vectors and parallel structures are however required to obtain accurate and fast processing. Digital implementations of common fuzzy operations leads unfortunately rapidly to complicated, enormous VLSI circuits.

Analog fuzzy values should be converted into strictly binary signals before being processed by standard digital circuits. On one hand, the analog input signals should be quantized through A/D converters, and on the other hand, the membership functions should be quantized to obtain their digital representations. Fuzzy sets are then storable but in the guise of stair-functions. The combination of these two round-off effect can deteriorate fuzzy processing if the fuzzy values are not represented with a sufficient number of bit. There is however a trade-off between precision and size (or speed) since the latter is proportional to the number of bit.

2.6.3 Mixed digital/analog implementations of fuzzy systems

Fuzzy logic systems lend themselves well to analog integration, except for some control and reconfiguration structures. Several switches are thus often integrated on analog circuits and commanded by digital inputs.

It can actually be attractive to increase the complementarity between digital and analog features and to merge them into a single mixed chip, in order to improve the weak points of both. A fuzzy knowledge base can be programmed in a digital memory which consists of dedicated locations and stores a variable number of parameters characterizing membership function shapes and inference rules notably.

3. DESIGN OF A NEW PROGRAMMABLE FUZZIFIER CIRCUIT

As stated in the previous section, the fuzzifier block maps the input crisp numbers into the fuzzy sets to obtain degrees of membership. Each fuzzifier block consists of membership function circuits which allow us to graphically represent a fuzzy set. The grade of membership of a membership function describes for the special element, to which grade it belongs to the fuzzy set. In this chapter, design and implementation of new programmable fuzzifier circuit is presented.

3.1 Introduction

Importance of membership functions in a fuzzy logic system has been studied in several literatures [38-40]. It has been shown that MFs have a dominant effect on the reasoning process of a FLC rather than number of rules or inference mechanism. Therefore, various shapes (triangular, trapezoidal, Gaussian, etc.) as well as types (type-1 and type-2) of MFs have been proposed and realized in order to improve the performance of these controllers. A type-1 triangular MF was designed by Kachare *et al.* in [41] which was followed by many other designs [42-44]. Khalilzadegan *et al.* have proposed a type-1 trapezoidal MF which utilized an analog programmable segment instead of digitally programming circuits to adjust the slopes of MF [45].

Focusing on non-linear MFs, a digital implementation of type-1 Gaussian MF suitable for neuro-fuzzy systems was studied by Basterretxea *et al.* [46], while the analog version of this function for classification applications was introduced by Fernandez *et al.* [47]. Another non-linear type-1 MF called rational powered, was implemented by Naderi *et al.* having high-resolution programmability [48] and then further examined by Kuo *et al.* [49] and Moshfe *et al.* [50] using truncated Taylor series approximation and translinear loop based method, respectively. All of these efforts were made to fulfill aforesaid demand.

In the past few years, type-2 MFs have been attracted a great deal of interest due to the additional degree of freedom provided by the footprint of uncertainty in the MFs of

type-2 FLCs in comparison with type-1 MFs [11, 51, 52]. The footprint of uncertainty represents the blurring of a type-1 MF, and is completely described by its two bounding functions, a lower membership function and an upper membership function, both of which are type-1 MFs [11]. Consequently, as a further advantage, type-2 MFs cover type-1 MFs in all of the features. In this regard, some limited implementation of type-2 MFs have been studied. Yazdanjouei *et al.* [53] proposed a tunable analog circuit to produce type-2 triangle and trapezoidal MFs. Another method has been employed by Mesri *et al.* to realize the same MFs [54].

Recently, a novel type-2 MF has been proposed by Khanesar *et al.* [55] which has certain values on both ends of the support and the kernel and some uncertain values for the other values of the support namely DT2MF. The authors have investigated the noise reduction property of this MF in the presence of noisy inputs and proved the advantages of this kind of MF. Additionally, it was demonstrated that for some specific parameters in DT2MF, the effect of distortion in the FLC can be minimized. Following this, a systematical methodology to construct a type-2 FLC using aforementioned MF was proposed by Aliasghary *et al.* [56, 57]. In these studies, the closed-form relation between input and output of the type-2 FLC was derived thanks to the DT2MF in which a superior performance was reported in comparison with other shapes of MFs. To the best of the authors' knowledge, there is no report in the literature for a circuit implementation of DT2MF.

In this chapter, design and implementation of a CMOS circuit which realizes DT2MF is fully described. Mixed analog/digital realization of the circuit provides a systematic way to program the circuit with a simple interface (as the advantages of digital realization), while having high accuracy and relatively low power consumption (as the advantages of analog design). Since the proposed method consists of the basic operations (addition/subtraction, minimization/maximization, and bounded difference) the current-mode circuits are preferable in the realization of fuzzy related blocks owing to the simple circuitry and intuitive configuration [8]. Moreover, potential advantages of high speed operation due to low parasitic capacitor nodes and low power consumption highly encouraged us to employ this technique [58, 59].

The chapter is organized in 5 sections: The block diagram of DT2MF circuit is presented in section 3.2, followed by the transistor level design of blocks in section

3.3. In section 3.4, HSPICE simulation results of proposed circuits are presented to prove the efficiency of the design. Finally, conclusions are outlined in section 3.5.

3.2 Proposed Block Diagram of DT2MF Circuit

As previously stated, type-2 MFs are generally divided into two MFs; upper membership function (UMF) and lower membership function (LMF). Consequently, type-2 MFs can be considered as two separate type-1 MFs [11]. A typical DT2MF composed of UMF (black line) and LMF (blue line) as well as its *mirrored* shape (marked with dashed line) are shown in Figure 3.1.

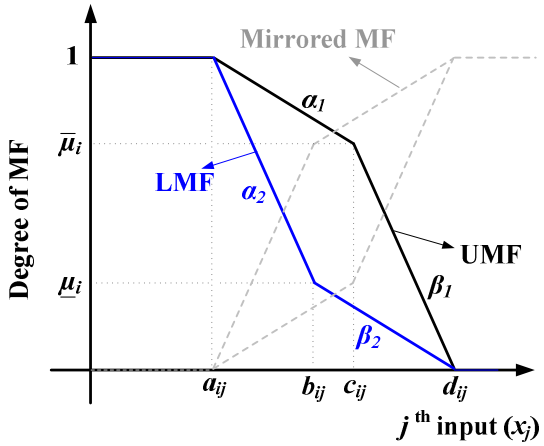


Figure 3.1 : Diamond-shaped type-2 membership function.

Mathematically, i^{th} upper diamond-shaped membership function (UMF) of the j^{th} input (x_j) can be modeled as:

$$\bar{\mu}_{ij}(x_j)=\begin{cases}1 & \text{if } x_j \le a_{ij}\\ 1+\left(\dfrac{\bar{\mu}_i-1}{c_{ij}-a_{ij}}\right)(x_j-a_{ij}) & \text{if } a_{ij}\le x_j \le c_{ij}\\ \bar{\mu}_i+\left(\dfrac{\bar{\mu}_i}{c_{ij}-d_{ij}}\right)(x_j-c_{ij}) & \text{if } c_{ij}\le x_j \le d_{ij}\\ 0 & \text{if } x_j \ge d_{ij}\end{cases} \quad \textbf{(3.1)}$$

while the lower one (LMF) is defined as:

$$\underline{\mu}_{ij}(x_j)=\begin{cases}1 & \text{if } x_j \le a_{ij}\\ 1+\left(\dfrac{\underline{\mu}_i-1}{b_{ij}-a_{ij}}\right)(x_j-a_{ij}) & \text{if } a_{ij}\le x_j \le b_{ij}\\ \underline{\mu}_i+\left(\dfrac{\underline{\mu}_i}{b_{ij}-d_{ij}}\right)(x_j-b_{ij}) & \text{if } b_{ij}\le x_j \le d_{ij}\\ 0 & \text{if } x_j \ge d_{ij}\end{cases} \quad \textbf{(3.2)}$$

where a_{ij}, b_{ij}, c_{ij} and d_{ij} are vertices, and $\bar{\mu}_i$ and $\underline{\mu}_i$ are the degrees of upper and lower MFs respectively. In addition, α_1, α_2, β_1 and β_2 are the slopes demonstrated on the figure.

Also the *mirrored* DT2MF satisfies the following relationships:

$$\bar{\mu}_{ij}(x_j)_{Mirrored} = 1 - \underline{\mu}_{ij}(x_j) \tag{3.3}$$

$$\underline{\mu}_{ij}(x_j)_{Mirrored} = 1 - \bar{\mu}_{ij}(x_j) \tag{3.4}$$

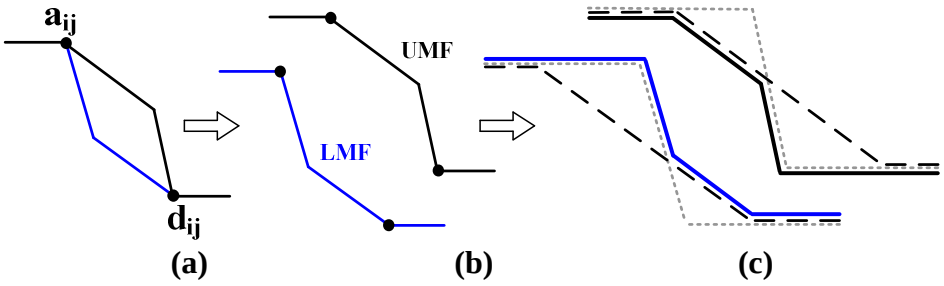


Figure 3.2 : (a) a typical DT2MF, (b) separated UMF and LMF and (c) isolation of UMF and LMF.

Figure 3.2(b) illustrates UMF and LMF separately. Considering circuit realization, each part can also be divided into two distinct segments as shown in Figure 3.2(c). Based on this figure, the design process of realizing DT2MF can be explained as follows:

1. Each separated part of Figure 3.2(c) consists of two Z-shape MFs (ZMFs) with different slopes (determined with dashed lines). Thus, a circuit which provide ZMF should be designed.

2. The designed ZMF circuit should have the ability of programming to produce various slopes, and also upper (a_{ij}) and lower (d_{ij}) modal points of MF; so that the programmability of the circuit will be investigated.

3. By taking the minimum and maximum of two Z-shape MFs, UMF and LMF are achieved respectively (As seen in Figure 3.2(c) with solid lines)). Therefore, minimizer and maximizer circuits of two MFs should be designed.

On the basis of these steps, the proposed architecture to realize DT2MF is illustrated in Figure 3.3. All of the circuits are designed in the current-mode; thus mathematical parameters are accordingly explained as the current signals. For instance, a_{ij} and d_{ij} are converted to $I_{a_{ij}}$ and $I_{d_{ij}}$ respectively. Considering the figure, crisp input (I_{in}) is

repeated by a simple current mirror and then injected to the inputs of each ZMF circuit to generate corresponding Z-shaped function. Besides, the switches $S_{U4}'S_{U3}'S_{U2}'S_{U1}'S_{U0}'$, $S_{U4}''S_{U3}''S_{U2}''S_{U1}''S_{U0}''$, $S_{L4}'S_{L3}'S_{L2}'S_{L1}'S_{L0}'$ and $S_{L4}''S_{L3}''S_{L2}''S_{L1}''S_{L0}''$ provide tunable MFs, as will be thoroughly discussed in the next section. Take notice that, the ZMF should be programmable in terms of three parameters: upper modal current or $I_{a_{ij}}$, lower modal current or $I_{d_{ij}}$ and finally slopes of MFs (α_1, α_2, β_1 and β_2) which determine vertices of b_{ij} and c_{ij}. In brief, two kinds of Z-shape MF circuit are required:

1. By sweeping the slope of ZMF, $I_{a_{ij}}$ is constant while the lower point changes. For the sake of briefness this kind of MF is called upper ZMF (UZMF).

2. By sweeping the slope of ZMF, $I_{d_{ij}}$ is constant while the upper point changes. This is also called lower ZMF (LZMF).

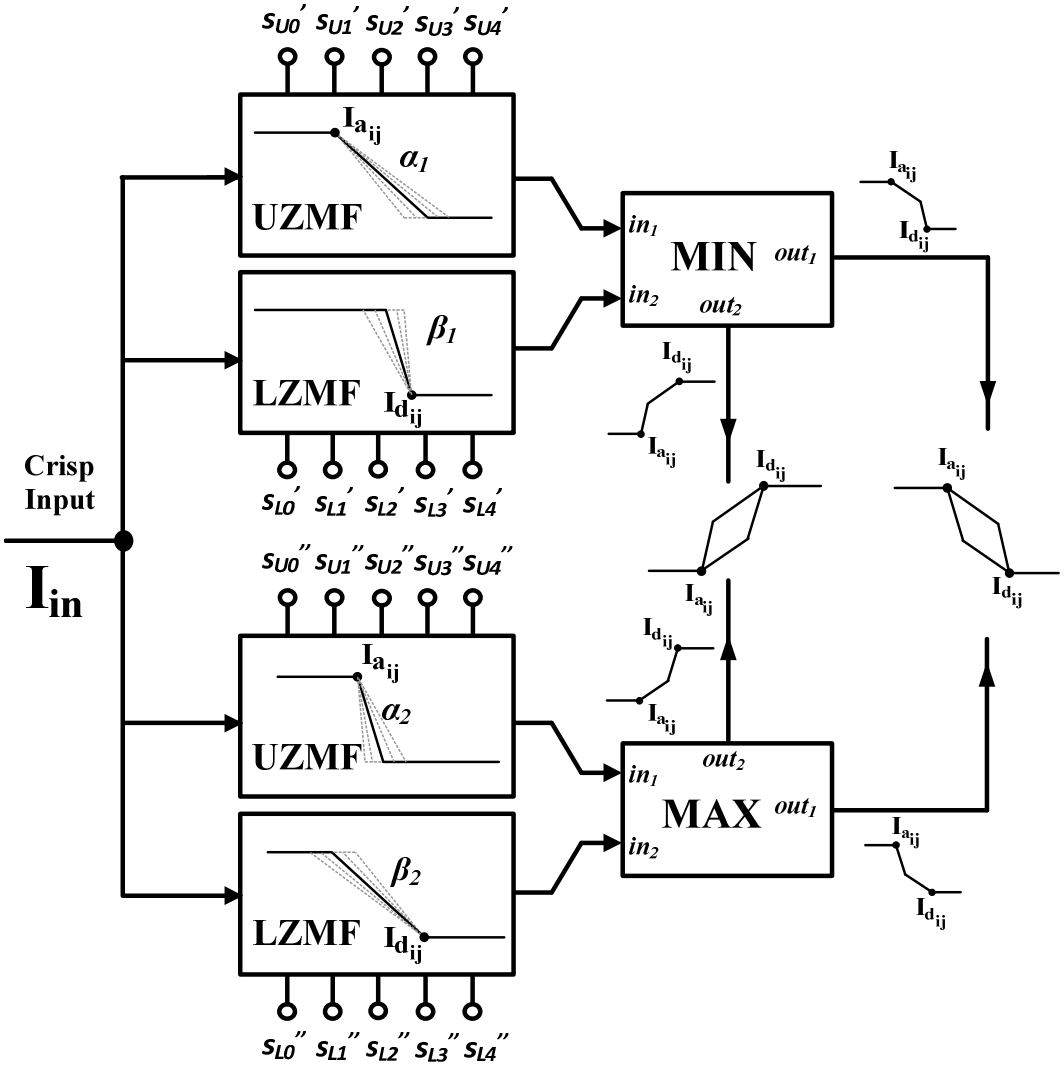


Figure 3.3 : Complete block diagram of the proposed DT2MF generator.

Then, the outputs of these blocks are applied to the minimizer (MIN) and maximizer (MAX) circuits in pair. Each circuit has two outputs; For MIN (MAX) circuit, one of the outputs (I_{out1}) is minimum (maximum) of two inputs, and since the *mirrored* shape of DT2MF is required, another one is constructed as: $I_{out2} = I_N - I_{out1}$ (see (3.3) and (3.4)), where I_N is normalized to 1. The resulting outputs are eventually DT2MF.

Usually, several MF circuits are needed in a FLC according to the fuzzy partitions of the input variables; therefore, MF circuit with compact structure is preferred in order to produce different MFs and save the chip area. Considering this feature, the programmability of the proposed circuit in terms of all parameters enables the expert of the system to create other shapes of type-2 MFs as is shown in Figure 3.4. For instance, if $\bar{\mu}_i = 1$ and $\underline{\mu}_i = 0$, by proper choosing of the slopes the resulting shape is type-2 triangular MF. Other realizable MFs are described as follow:

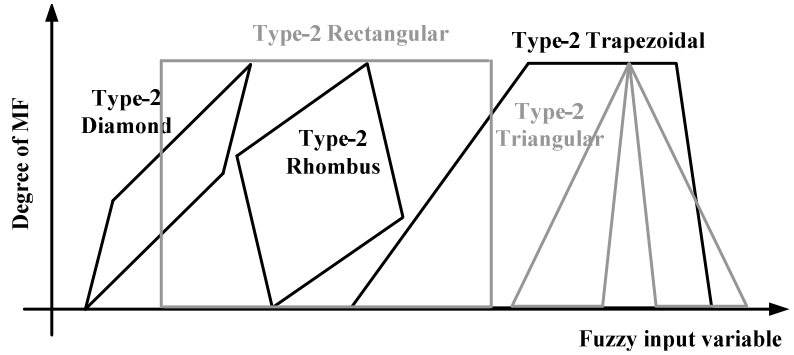


Figure 3.4 : Realizable type-2 membership functions using proposed circuit.

1. Type-2 rectangular MF reported in [60], that has been utilized to form footprint of uncertainty of a new general type-2 MF called granular MF. This kind of MF provides more degrees of freedom and design flexibility which allows us to model any desired discontinuity and various kinds of nonlinearities on the universe of discourse or in the input-output mapping. Consequently, it is quite effective in modeling and control of nonlinear systems having high nonlinearities. Note that, no design has been presented to generate this MF as yet. By choosing $a_{ij} = b_{ij}$, $c_{ij} = d_{ij}$, $\bar{\mu}_i = 1$ and $\underline{\mu}_i = 0$, rectangular MF is ultimately achieved.

2. Type-2 trapezoidal MF, which can be realized by appropriate programming of α_1, α_2, β_1 *and* β_2; however this form of MF has been implemented in [61].

3. Type-2 Rhombus MF, which is a special case of DT2MF when all four sides have the same length. This form of MF has been introduced in [62].

3.3 Circuit Design of DT2MF

In this section transistor-level design of functional blocks is discussed. Considering the block diagram of Figure 3.3, the following circuits are designed:

1. Programmable LZMF Circuit

2. Programmable UZMF Circuit

3. MIN and MAX circuits

It should be pointed out that the design procedure of the circuits starts by selection of currents of the devices. There is a trade-off for this. Although lower current ranges improve the power dissipation, it encounters the circuit with device mismatching and low speed operation. In order to satisfy the compromise between these parameters, the universe of discourse of the crisp inputs is set to the interval of [0, 10 μA], meaning the current value of 10 μA has been normalized to one.

3.3.1 Programmable LZMF circuit

3.3.1.1 Programmable current mirror

The NMOS programmable current mirror (NPCM) circuit is shown in Figure 3.5. The circuit is based on the wide swing cascade current mirror [63], with some modifications using a transmission gate to make it programmable. The input current is injected to the number of m_{in} parallel transistors. Since the drain terminals of output transistors are tied together, the value of mirrored current (I_{out}) can be adjusted via 5 bits $S_4S_3S_2S_1S_0$. In this case, it is obvious that the cell is repeated five times and m_0=1, m_1=2, m_2=4, m_3=8 and m_4=16 are chosen to produce output current with the resolution of 1/16=0.0625. If one of the switches including m_n parallel transistors is 1, the transmission gate shorts the gate of corresponding transistor to the bias line and the proportion ($\sum_{n=0}^{4} m_n/m_{in}$) of input current is transferred to the output. Therefor, 0.0625 to 2 times of the input current with the resolution of 0.0625 μA can be generated. This is believed to be enough to realize gentle slopes of α_1 and β_2. It is also possible to exchange the input and output ports which can be useful to create steep slopes of α_2 and β_1. In this case, 1 to 16 times of the input current is generated.

Note that the PMOS version of this structure called PPCM will be used as well in order to provide required slopes.

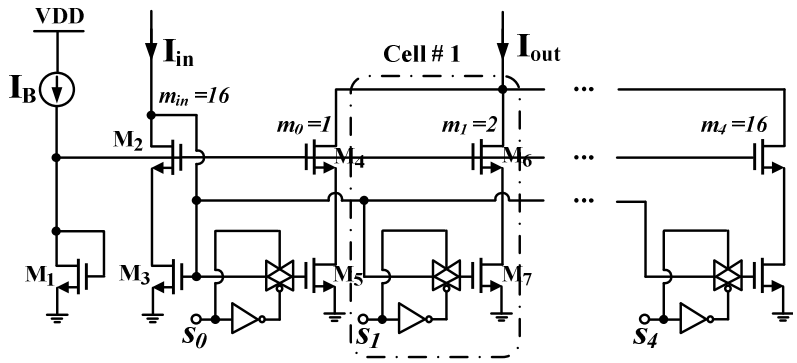


Figure 3.5 : NMOS programmable current mirror circuit.

3.3.1.2 Proposed LZMF circuit

The desired output and the conceptual scheme of proposed LZMF circuit are shown in Figure 3.6. The design idea has been taken from the concept reported in [64]. The difference between $I_{d_{ij}}$ and I_{in} flows in an NPCM with selectable gain of β controlled by switches $S_{L4}S_{L3}S_{L2}S_{L1}S_{L0}$. To restrict the output of the circuit, a normalize current of I_{N1} is defined and subtracted from the output of NPCM block. The resulted current (I_{S1}) is an S-shape MF. By converting the direction of I_{S1} using NMOS current mirror (NCM) and then subtracting from a normalize current of I_{N2}, the desired Z-shape output (I_{Z1}) is obtained. It should be pointed out that the output is a linear mapping between I_{Z1} and I_{in} which can be represented as:

$$I_{Z1} = I_{N2} - [I_{N1} - \beta(I_{d_{ij}} - I_{in})] \qquad \textbf{(3.5)}$$

Suppose that $I_{in}<I_{d_{ij}}$, in this case if β ($I_{d_{ij}}$-I_{in})>I_{N1}, NCM is entirely out of the circuit and hence I_{N2} is directly transferred to the output, until β ($I_{d_{ij}}$-I_{in})<I_{N1}; for this situation, subtracted current of I_{S1} proportionally increases by increasing I_{in}. At the same time, since I_{S1} is subtracted from I_{N2}, I_{Z1} decreases till I_{in} becomes equal to $I_{d_{ij}}$.

For the case that $I_{in}>I_{d_{ij}}$, since NPCM is open circuit and also $I_{N1}=I_{N2}=I_N$, the output current is equal to zero.

It should be noted that both slopes of β_1 and β_2 in Figure 3.3 are generated by tuning the gain of β via $S_{L4}'S_{L3}'S_{L2}'S_{L1}'S_{L0}'$ and $S_{L4}''S_{L3}''S_{L2}''S_{L1}''S_{L0}''$ respectively.

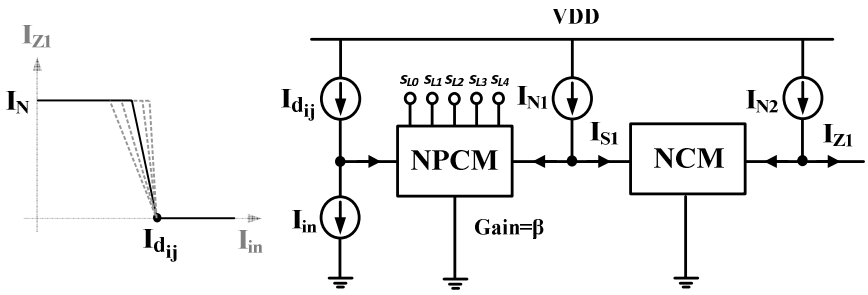


Figure 3.6 : Proposed LZMF circuit beside its desired output.

3.3.2 Proposed UZMF circuit

Figure 3.7 shows the proposed structure for the second type of Z-shape MF circuit and also desired output. Similar to the LZMF, the structure relies on the concept of [64] as well. The relationship between input and output currents can be driven as:

$$I_{Z2} = \alpha(I_{a_{ij}} - I_{in}) - I_N \tag{3.6}$$

where α is the gain of PPCM controlled via switches $S_{U4}S_{U3}S_{U2}S_{U1}S_{U0}$. As long as $I_{in}<I_{a_{ij}}$, PPCM is out of the circuit and I_N forms the output current. Once $I_{in}>I_{a_{ij}}$, the difference of currents by the factor of α is subtracted from I_N. The ultimate current is eventually what would be expected. It should be mentioned that the gain of α covers both slopes of α_1 and α_2 via switches $S_{U4}'S_{U3}'S_{U2}'S_{U1}'S_{U0}'$ and $S_{U4}''S_{U3}''S_{U2}''S_{U1}''S_{U0}''$ in Figure 3.3 respectively.

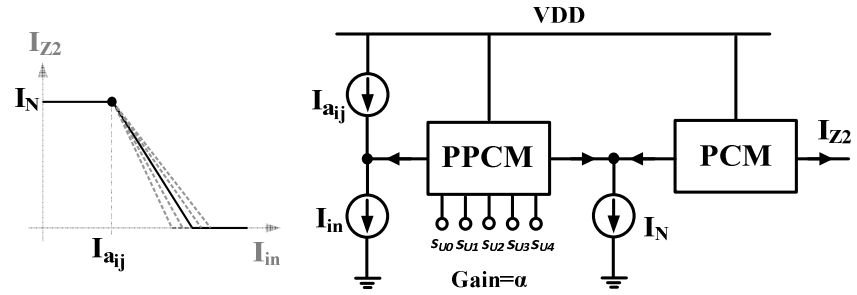


Figure 3.7 : Proposed UZMF circuit beside its desired output.

3.3.3 MIN and MAX circuits

According to the architecture in Figure 3.3, outputs of UZMF and LZMF are applied to MIN and MAX circuits. Several techniques are available in the literature to implement these circuits [65, 66]. The modified MIN circuit is shown in Figure 3.8. We have been presented the multi-input version of this structure in [67]. A high-speed feedback structure is employed to determine the minimum current among the applied

inputs. M_{b1} and M_{b2} as well as the constant current of I_b provide bias voltage for the circuit, and M_{b3} and M_{b4} make up the output stage.

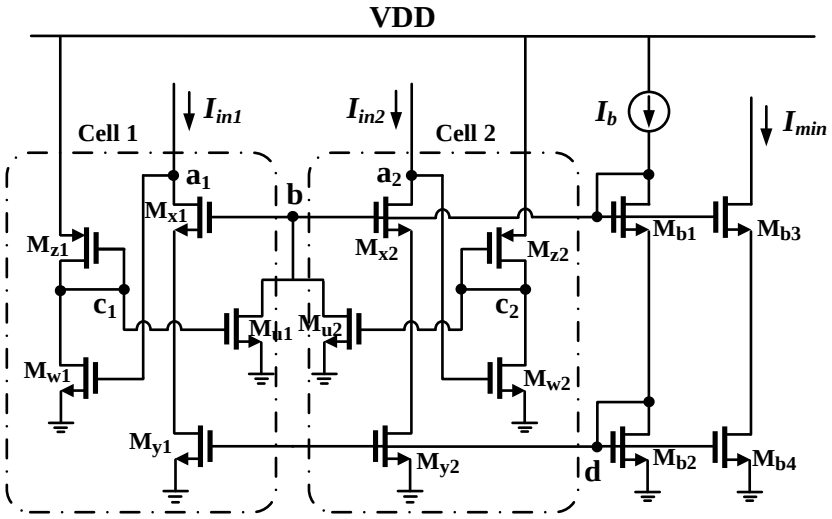


Figure 3.8 : Two-input one-output minimizer circuit.

M_{w1} and M_{w2} are biased in the triode region and perform as a resistor whose values are controlled by the overdrive voltage. The relationship can be represented by:

$$R_{w1,2} \approx V_{DS} / I_{DS} \approx (\mu C_{ox} (W / L)_{w1,2} (V_{GSw1,2} - V_{TN}))^{-1} \quad \textbf{(3.7)}$$

M_{u1} and M_{u2} are biased such that they operate in the threshold of turning on and off. To analyze the circuit, suppose that I_{in2} is more than I_{in1}, this leads to the voltage at node a_2 to be risen up to nearly V_{DD}. Hence, voltage at node c_2 falls down due to the reduction in the resistor of M_{w2}; therefore, M_{u2} leaves saturation region and will be cut-off and cell 2 makes no change in the output current. At the same time, considering cell 1, voltage of node a_1 decreases to nearly ground, which in turn increases the voltage of node c_1 thanks to the increasing of resistor of M_{w1}. Hence, M_{u1} turns on and sinks extra current of I_b up to the point that I_{min} becomes equal to I_{in1}. The same procedure occurs for $I_{in1}>I_{in2}$ for cell 1 instead of cell 2. When I_{in1} is equal to I_{in2}, the only difference is that both M_{u1} and M_{u2} go to saturation region simultaneously. They equally sink extra current of I_b. In this case I_{in1} or I_{in2} is transferred to the output.

MIN and MAX of two parameters like *x* and *y* can be converted to each other according to De Morgan's law as follows:

$$\max(x, y) = \overline{\min(\bar{x}, \bar{y})} \quad \textbf{(3.8)}$$

In order to realize this equation, since current of 10 µA has been normalized to 1, MAX of I_{in1} and I_{in2} can be given by:

$$\max (I_{in1}, I_{in2})=10\mu A-[\min (10\mu A-I_{in1}, 10\mu A-I_{in2})] \quad \textbf{(3.9)}$$

Thus, using designed MIN circuit and some current sub-tractor, MAX circuit is implemented as shown in Figure 3.9. Take notice that all of the normalized currents of 10 µA are provided via single source using a current mirror. Indeed, the current-mode designing provides simple and intuitive way for duplication and subtraction of the signals.

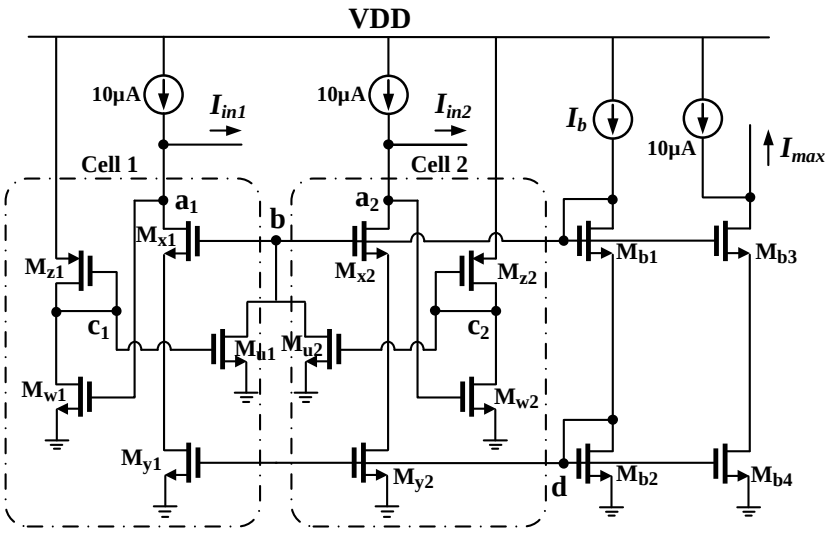


Figure 3.9 : The maximizer circuit based on De Morgan's law.

3.4 Simulation Results and Performance Analysis

In this section, post layout simulation results of the proposed circuits as well as the performance analysis are presented using HSPICE with TSMC level 49 (BSIM3v3) parameters for 0.35 µm CMOS technology so as to verify the performance of the circuits. The simulation results are carried out after extracting the layout which is drawn by Cadence software using single poly and two metals (Metal1 and Metal2). Figure 3.10 shows the full layout of the circuit in which the area is 97.95 µm*72.05 µm. For all of the simulations the normalize current of I_N is equal to 10 µA and the supply voltage is 3.3 V. Also the aspect ratio of transistors is given in Table 3.1. Take notice that the aspect ratio of transistors in NPCM, PPCM, PCM and NCM are the same.

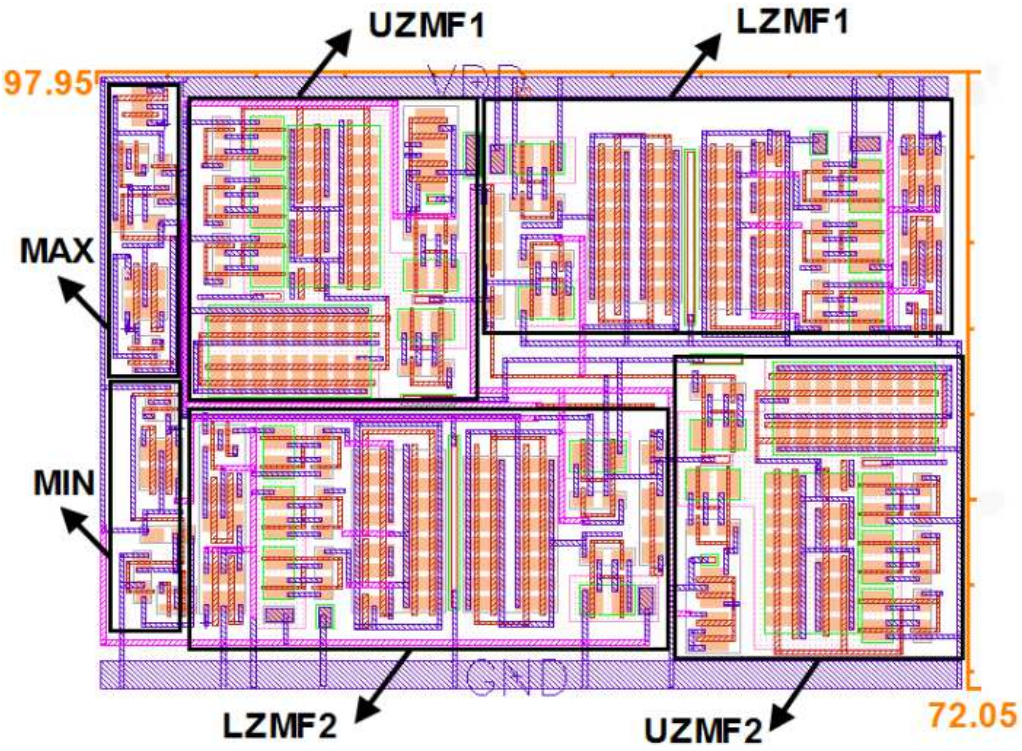


Figure 3.10 : Layout of the DT2MF circuit.

Table 3.1 : Transistors aspect ratio of proposed circuit.

Transistor name	W/L (µm/µm)
M_1	3/1.2
M_{w1}, M_{w2}	2/0.4
M_{z1}, M_{z2}	3/1
M_2, M_3, M_4, M_5, M_6, M_7	3/0.3
M_{b1}, M_{b2}, M_{b3}, M_{b4}, M_{x1}, M_{x2}, M_{y1}, M_{y2}	1/0.4

3.4.1 MIN and MAX

Figure 3.11 shows simulation results of the MIN and MAX circuits. Two triangular waves (dashed lines) in the scale of 100 kHz with different frequencies and amplitudes are applied and I_b is set to 10µA. Following that, minimum and maximum of the input signals (solid line) appear in the outputs. Measured error (solid line) as well as the average of relative error (dashed line) are demonstrated along the bottom of each figure. Maximum errors at the track points of MIN and MAX circuits are 138 nA and 150 nA respectively, while the relative errors are measured 14 nA and 18 nA which leads to the respective errors of 0.14 % and 18 %.

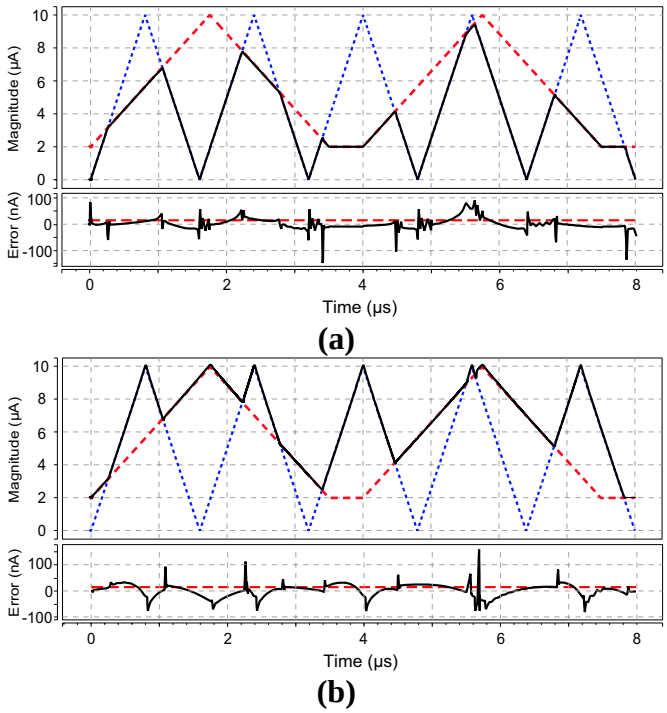


Figure 3.11 : Simulation results of (a) minimizer and (b) maximizer circuits as well as the measured errors.

3.4.2 Diamond-shaped type-2 MF

Simulations for DT2MF are carried out to verify the full programmability of the circuit in terms of all parameters (a_{ij}, b_{ij}, c_{ij} and d_{ij}) shown in Figure 3.1.

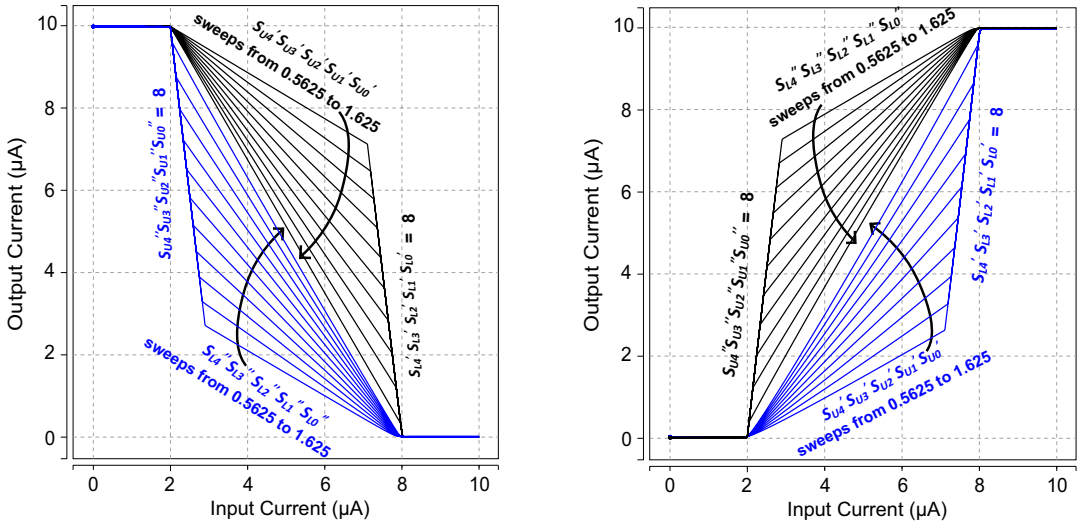
Figure 3.12(a) shows the DT2MF which is generated for assumed parameters as: $I_{a_{ij}}$=2 μA, $I_{d_{ij}}$ =8 μA. By keeping $I_{a_{ij}}$ and $I_{d_{ij}}$ as constant, the gains of α_1 and β_2 are simultaneously swept to prove the tunability of $I_{c_{ij}}$ and $I_{b_{ij}}$ through some states of programming switches $S_{U4}'S_{U3}'S_{U2}'S_{U1}'S_{U0}'$ and $S_{L4}''S_{L3}''S_{L2}''S_{L1}''S_{L0}''$ respectively which is shown on the figure. The *mirrored* DT2MF is also shown in Figure 3.12(b).

The same simulations are performed by sweeping the gains of α_2 and β_1 via the programming switches of $S_{U4}''S_{U3}''S_{U2}''S_{U1}''S_{U0}''$ and $S_{L4}'S_{L3}'S_{L2}'S_{L1}'S_{L0}'$ respectively. The result is shown in Figure 3.13. Note that the gain of α_2 as well as β_1 is generated by exchanging input and output ports of NPCM and PPCM (as explained in section 3.3.1.1) to provide the steep slopes.

Bearing in mind that unlike the vertices a_{ij} and d_{ij} which are apparently available via $I_{a_{ij}}$ and $I_{d_{ij}}$ respectively, b_{ij} and c_{ij} are defined in regard to $I_{a_{ij}}$, $I_{d_{ij}}$ and also the gains of α_1, α_2, β_1 *and* β_2 as follow:

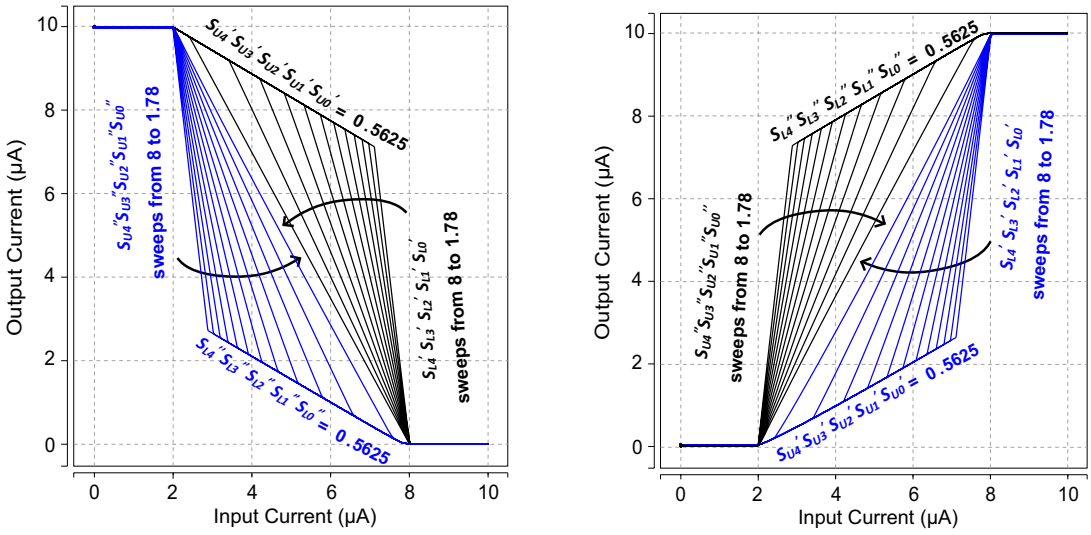
$$I_{b_{ij}} = \frac{\alpha_2 I_{a_{ij}} - \beta_2 I_{d_{ij}} - 1}{\alpha_2 - \beta_2} \tag{3.10}$$

$$I_{c_{ij}} = \frac{\alpha_1 I_{a_{ij}} - \beta_1 I_{d_{ij}} - 1}{\alpha_1 - \beta_1} \tag{3.11}$$



(a) **(b)**

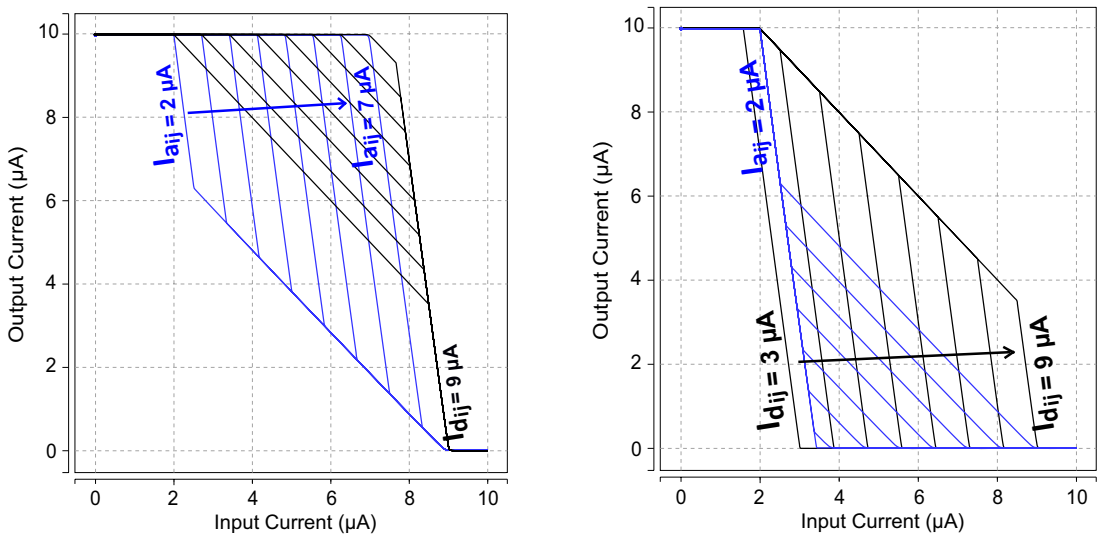
Figure 3.12 : (a) Programmability of DT2MF in terms of $I_{b_{ij}}$ and $I_{c_{ij}}$ by sweeping α_1 and β_2, (b) *Mirrored* DT2MF.



(a) **(b)**

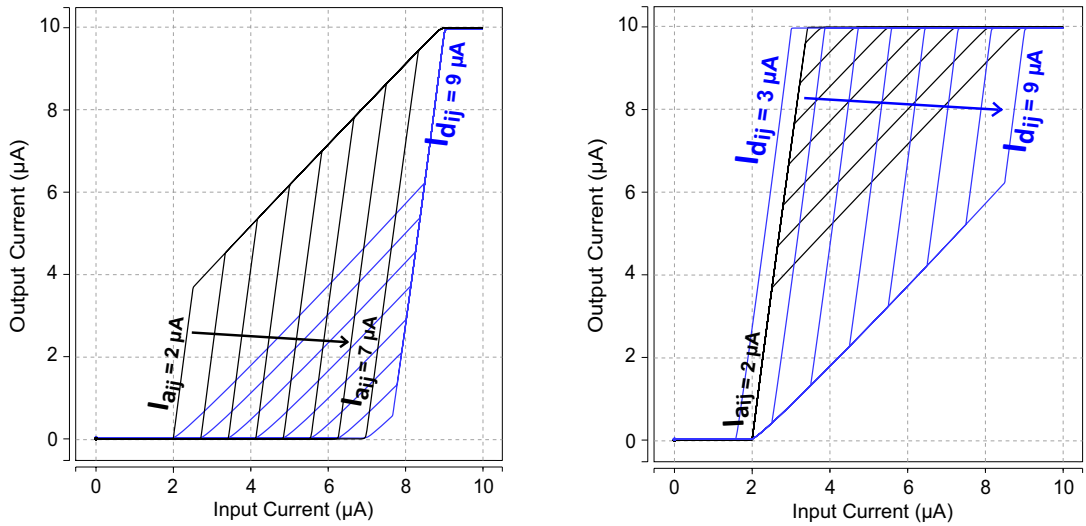
Figure 3.13 : (a) Programmability of DT2MF in terms of $I_{b_{ij}}$ and $I_{c_{ij}}$ by sweeping α_2 and β_1, (b) *Mirrored* DT2MF.

Figures 3.14(a) and (b) demonstrate the upper modal point ($I_{a_{ij}}$) and lower modal point ($I_{d_{ij}}$) programmability of the circuit respectively, in which the slopes are kept constant. The *mirrored* DT2MFs are also shown in Figure 3.15(a) and b). Take notice that in all of the simulations, UMF and LMF are specified by the black and blue colors respectively. In order to summarize the simulation details, the programming codes of parameters in each figure are listed in Table 3.2.



(a) **(b)**

Figure 3.14 : Tunability of DT2MF (a) for constant $I_{d_{ij}}$ and different $I_{a_{ij}}$ (b) for constant $I_{a_{ij}}$ and different $I_{d_{ij}}$.



(a) **(b)**

Figure 3.15 : Tunability of *Mirrored* DT2MF (a) for constant $I_{d_{ij}}$ and different $I_{a_{ij}}$ (b) for constant $I_{a_{ij}}$ and different $I_{d_{ij}}$.

Table 3.2 : The programming codes of parameters in the simulations.

Parameter	α_1		α_2		β_1		β_2		$I_{a_{ij}}$ (μA)		$I_{d_{ij}}$ (μA)	
Switches	$S_{U4}'S_{U3}'S_{U2}'S_{U1}'S_{U0}'$		$S_{U4}''S_{U3}''S_{U2}''S_{U1}''S_{U0}''$		$S_{L4}'S_{L3}'S_{L2}'S_{L1}'S_{L0}'$		$S_{L4}''S_{L3}''S_{L2}''S_{L1}''S_{L0}''$		–		–	
Sweep	From	To	From	To	From	To	From	To	From	To	From	To
Figure 3.12(a)	01001	11010	00010	–	00010	–	01001	11010	2	–	8	–
Figure 3.12(b)	01001	11010	00010	–	00010	–	01001	11010	2	–	8	–
Figure 3.13(a)	01001	–	00010	01001	00010	01001	01001	–	2	–	8	–
Figure 3.13(b)	01001	–	00010	01001	00010	01001	01001	–	2	–	8	–
Figure 3.14(a)	10000	–	00010	–	00010	–	10000	–	3	9	2	–
Figure 3.14(b)	10000	–	00010	–	00010	–	10000	–	9	–	2	7
Figure 3.15(a)	10000	–	00010	–	00010	–	10000	–	2	7	9	–
Figure 3.15(b)	10000	–	00010	–	00010	–	10000	–	2	–	3	9

As already mentioned, proposed DT2MF covers other shapes of type-2 functions. For instance, if $\bar{\mu}_i = 1$ and $\underline{\mu}_i=0$, then the resulting type-2 MF is achieved in the shape of triangular. To satisfy these conditions, by choosing the maximum value for β_1 (i.e., 16), the slope of α_1 determines right side of the triangular by establishing $\bar{\mu}_i = 1$. Also by choosing $\beta_2 \approx 0$, $\underline{\mu}_i=0$ is ultimately resulted. In order to simulate the circuit, $I_{a_{ij}}$=5 µA and $I_{b_{ij}}$=6 µA are assumed, then by keeping the slope of α_2 as constant (via $S_{U4}''S_{U3}''S_{U2}''S_{U1}''S_{U0}''$) and sweeping α_1 (via $S_{U4}'S_{U3}'S_{U2}'S_{U1}'S_{U0}'$), the right half of the triangle MF in Figure 3.16 is obtained. Similarly, the left half is realized using *mirrored* DT2MF by choosing the maximum value for $\alpha_2, \alpha_1 \approx 0$, $I_{a_{ij}}$=1 µA and $I_{d_{ij}}$=5 µA, keeping the slope of β_2 as constant (via $S_{L4}''S_{L3}''S_{L2}''S_{L1}''S_{L0}''$) and finally sweeping β_1 (via $S_{L4}'S_{L3}'S_{L2}'S_{L1}'S_{L0}'$). In order to compute the nonlinearity of the results, the same procedure in [68-70] is followed. Therefore the simulation results of Figures 3.12, 3.13, 3.14 and 3.15 are compared with the ideal results obtained from MATLAB, in which the nonlinearity error is found to be 0.55%.

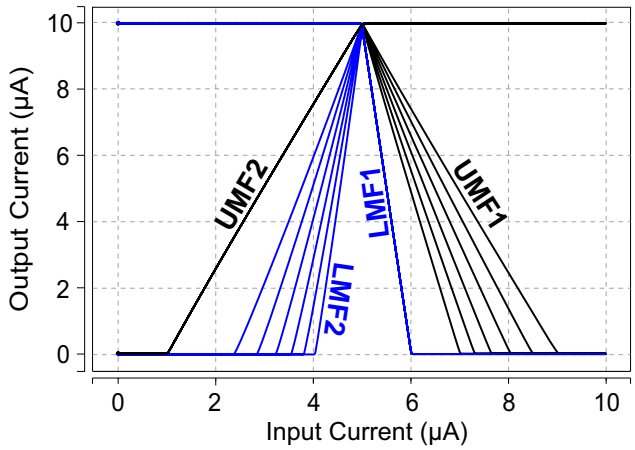


Figure 3.16 : Programmable type-2 triangular MF generated from DT2MF.

Other shapes of type-2 MFs including rhombus, trapezoid, rectangular and parallelogram can be readily generated by adjusting $I_{a_{ij}}$, $I_{d_{ij}}$, α_1, β_1, α_2 and β_2. For briefness, the simulation results of these MFs are not presented, because they are based on DT2MF and have almost the same performance.

3.4.3 Pulse response of DT2MF circuit

In order to examine speed of the circuit, a square pulse is applied to the input. Propagation times in low-to-high (t_{PLH}) and high-to-low (t_{PHL}) transitions are measured

for both of the outputs (UMF and LMF) at the 50% point; then the average propagation delays are computed. The input pulse as well as the output responses are depicted in Figure 3.17 in which the averages of propagation times for UMF and LMF are computed 8.7 ns and 4.8 ns respectively. This remarkable result is obtained owing to the design of current-mode circuits with low parasitic capacitor nodes which lead to a high speed operation.

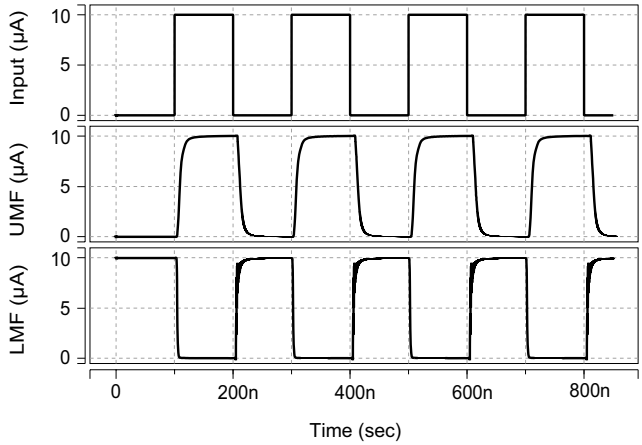


Figure 3.17 : Pulse input of the DT2MF circuit and responses of the outputs (UMF and LMF).

3.4.4 Monte-Carlo analysis

To ensure the robustness of the circuit against the process variation, the Monte Carlo analysis with 100 iterations is performed by applying mismatch in the transistors aspect ratio and threshold voltage. The variation for these parameters can be given by [145]:

$$\Delta V_T(mV) = \frac{A_{VTH}}{\sqrt{MWL}} \tag{3.12}$$

$$\Delta(\mu C_{ox}\frac{W}{L})(\%) = \frac{A_K}{\sqrt{MWL}} \tag{3.13}$$

where A_{VTH} and A_K are proportionality factors in which for 0.35 µm technology are 0.2 for PMOS or NMOS transistors and are 7.5 for NMOS and 11.25 for PMOS transistors, respectively. In addition, M is the number of parallel transistors. The simulation result is depicted in Figure 3.18, in which 95% of samples are occurred with the error of less than ±1%.

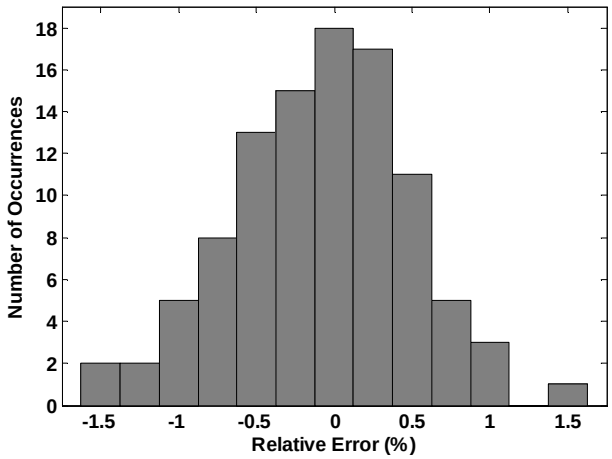


Figure 3.18 : The result of Monte Carlo analysis of DT2MF circuit for mismatch in threshold voltage and transistors aspect ratio.

3.4.5 Temperature analysis

The threshold voltage is the most important parameter in the analysis of temperature dependence of CMOS circuits, owing to the fact that current–voltage characteristic of MOS transistor is proportional to the square of the difference of gate-source and threshold voltages. Thus, a small variation in threshold voltage causes a large change in the output current. The threshold voltage of MOSFET is given as:

$$V_T = \phi_{ms} - \frac{Q_{ss}}{C_{ox}} + 2\phi_F + \gamma\sqrt{2\phi_F} \qquad \textbf{(3.14)}$$

where $\phi_{ms} = \phi_T \ln(N_A N_G / n_i^{\,2})$ is the gate-substrate contact potential, N_A and N_G are the substrate and gate doping concentrations, respectively and n_i is the intrinsic carrier concentration of Si, Q_{ss} the surface charge density, and C_{ox} the oxide capacitance; $\gamma$is a body effect constant and $\phi_F = \phi_T \ln(N_A/n_i)$ is the Fermi energy with the thermal voltage $\phi_T = kT/q$.

Since ϕ_{ms} and ϕ_F both contain ϕ_T, they are only parameters causing a temperature dependence of threshold voltage ($\partial V_T/\partial T$) which can be derived as [71]:

$$\frac{\partial V_T}{\partial T} = \frac{\partial \phi_{ms}}{\partial T} + 2\frac{\partial \phi_F}{\partial T} + \frac{\gamma}{\sqrt{2\phi_F}}\frac{\partial \phi_F}{\partial T} \qquad \textbf{(3.15)}$$

To analyze the performance of the proposed DT2MF circuit regarding temperature variations, three main circuits of LZMF, UZMF and MIN/MAX are discussed separately: NMOS and PMOS current mirrors are basic building blocks of LZMF and UZMF circuits either cascode or wide swing cascode. The current mirrors work on the principle that identical transistors with equal gate-to-source and drain-to-source voltages carry equal drain currents. Since these voltages of corresponding transistors are equal in all conditions, any variations in threshold voltage are automatically compensated. Therefore, probable temperature variations do not affect the performance of the current mirrors and subsequently LZMF and UZMF circuits. On the other hand, output characteristic of the MIN/MAX circuit reveals dependency of the circuit to the threshold voltage as follows [67]:

$$I_{\min} + I_b + 4\sqrt{I_{\min}(I_b - I_{\min})} \le \frac{K}{2}\left[V_{DD} - (|V_{TP}| + 2V_{TN})\right]^2 \qquad \textbf{(3.16)}$$

where K is transconductance parameter and V_{TN} and $|V_{TP}|$ are threshold voltages of NMOS and PMOS transistors, respectively. Based on this equation, as V_{DD}-($|V_{TP}|+2V_{TN}$) <1, squaring of this difference makes it smaller, especially when it is multiplied by the small factor of K/2. Consequently, variation of threshold voltage caused by temperature fluctuation would not significantly affect the performance of DT2MF circuit. Figure 3.19 shows the relative error of the circuit in different temperatures, where the maximum error occurred at -40 ^{o}C with 0.82%.

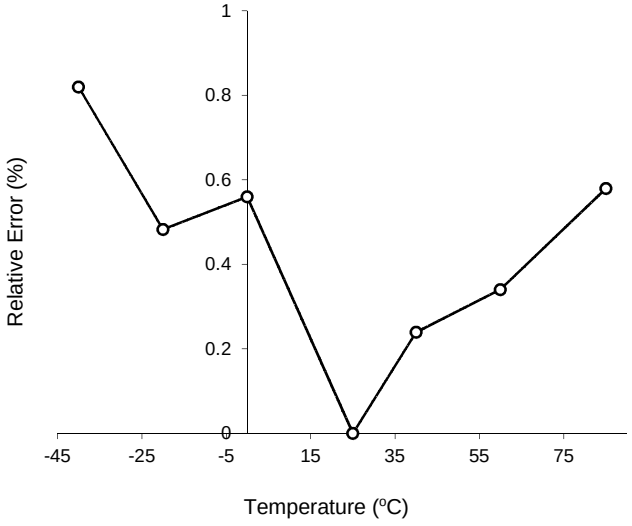


Figure 3.19 : Relative error of DT2MF circuit versus different temperatures.

3.5 Conclusion

Mixed analog/digital circuit implementation of T2DMF in CMOS technology was presented in this chapter. The current-mode approach was employed owing to the simple circuitry and intuitive configuration to design the circuits. Since the proposed circuit was fully programmable in terms of all parameters, other various shapes of type-2 membership functions including rectangular, rhombus, triangular and trapezoidal could be readily generated. In order to simulate the circuit, HSPICE simulator was utilized to verify the validity of the theoretical formulations. The simulated characteristics proved the efficiency of the circuit regarding programmability, speed and eventually power consumption. Furthermore, Monte Carlo analysis was carried out to ensure the robustness of the circuit performance against the process variation. To estimate the power consumption, it was measured for a typical DT2MF in which the average power consumption was 688 μW. The characteristics of the proposed circuit are tabulated in Table 3.3.

Table 3.3 : Characteristics of the proposed circuit.

Feature	Value/Quality
Power supply (V)	3.3
Power consumption (μW)	688
Slop programmability	Yes
Vertices programmability	Yes
Propagation delay (ns)	4.8, 8.7
Relative error	< ±1%
Nonlinearity	0.55%
Active area (mm^2)	0.007
Input signal	Current
Output signal	Current
Technology (μm)	0.35

4. FUZZY INFERENCE ENGINE

The fuzzy inference engine combines rules and gives a mapping from fuzzy sets in the input universe of discourse to fuzzy sets in the output universe of discourse based on the fuzzy logic principle. In the inference engine, multiple antecedents in the rules are connected using AND operation, and the degree of membership in the input sets are combined using those in the output sets using sub-star composition, described in detail in [19] . Multiple rules are combined then by using a join operation.

The inference block combines rules and then gives a mapping from input T2FSs to output T2FSs. In type-2 fuzzy sets, join (⊓) and meet operators (⊔) are the main operators which can be realized using MIN or MAX circuits, respectively.

In the most general case, there is one MIN or MAX per rule connecting “N” fuzzy membership functions outputs, where “N” stands for the number of inputs of the controller. For this reason, circuits allowing multiple inputs are well adapted for multiple-input fuzzy controllers. One important issue to consider while designing multiple-input operators concerns its complexity as a function of the number of inputs “N”. A conventional approach to design an N-input MIN or MAX consists in building a binary tree by cascading 2-input operators [72, 73]. However, this method accumulates errors and degrades the operation speed.

From the above discussion it turns out that the main criterions that should be taken into account while designing these operators are:

1. Multi-input MIN or MAX structures are preferred to dual input circuits.
2. Cascading of unit cells should be avoided.
3. Simplicity is a main factor to reduce the power consumption of the circuit.
4. High-speed circuit should be design to avoid any delay at the output.
5. The accuracy of the operators should be taken into account.

4.1 Introduction

Minimum and maximum functions are widely used in computational systems such as fuzzy controllers and neural networks. There are also various applications for which the smallest/highest input value is required [7, 66]. On the basis of circuit implementation, multiple input MIN and MAX circuits are called loser-take-all (LTA) and winner-take-all (WTA), respectively, which can be converted each other according to DE Morgan's law.

Several LTA and WTA circuits have been proposed in the literature [5], [74]-[77] either in current-mode or voltage-mode. The inherent advantages of current-mode approach such as high speed due to low parasitic capacitor nodes, low power consumption and simple circuitry have recently encouraged authors to design these circuits in current-mode. Owing to the compact and simple design, the seminal paper in [74] has been selected as a starting point for many designers. There is a tradeoff between key parameters of LTA or WTA circuits consisting of speed, precision and power consumption. High-speed circuits was proposed in [75], however its accuracy was low. A higher precision was achieved using flipped voltage followers (FVF) [7], structures with O(N) complexity [76], cascode [5] and Wilson current mirror based topologies [76], and circuits using local positive feedbacks [77], while they suffer from low operation speed.

Moreover, designing a basic cell in MIN or MAX circuits which can be repeated for each additional input signal is a serious challenge and yet a distinct advantage. The circuits reported in [5, 75] have been designed for only two-input signals and were not be extended as a LTA or WTA. In many applications [78], it is required to utilize multi-input MIN (LTA) or MAX (WTA) circuit. As a conventional method "*binary tree*" structure based on the two-input MAX or MIN is employed. However, this method accumulates errors and degrades the operation speed.

In this chapter, a new high-precision LTA circuit is proposed. The structure is based on a basic cell which allows realizing a multi-input configuration by repeating the cell for each additional input. A simple high-speed feedback structure determines the minimum current at the output. Additionally, input dynamic range of the circuit can be efficiently controlled via the biasing current.

The chapter is organized in two main sections: A brief review of the former works as well as their advantages and disadvantages are discussed in section 4.2. The proposed circuit is presented in section 4.3. Also, the HSPICE simulation results, performance analysis and the conclusions are discussed in this section.

4.2 Literature Review

A simple and intuitive configuration based on the subtraction of input currents was proposed in [5] (see Figure 4.1). Considering I_1 and I_2 as the input currents; if $I_1 > I_2$, then the difference current of $I_1 - I_2$ in the input subtraction node flows in PMOS current mirror and then subtracted from I_1 in output subtraction node, resulting in:

$$I_{out} = I_1 - (I_1 - I_2) = I_2 \qquad \textbf{(4.1)}$$

On the other hand, if $I_2 > I_1$, then there is no difference current flowing in PMOS current mirror; hence, in output subtraction node we have:

$$I_{out} = I_1 - 0 = I_1 \qquad \textbf{(4.2)}$$

Then the minimum current flows into the output node. The number of possible applied input currents is limited by two, then it cannot be used as a multi-input MIN or MAX circuit. It should be pointed out that since the circuit is based on the current subtraction method in the input and output nodes, there will be a tradeoff between the speed and accuracy. However, in the low frequencies, the circuit benefits from high accuracy performance.

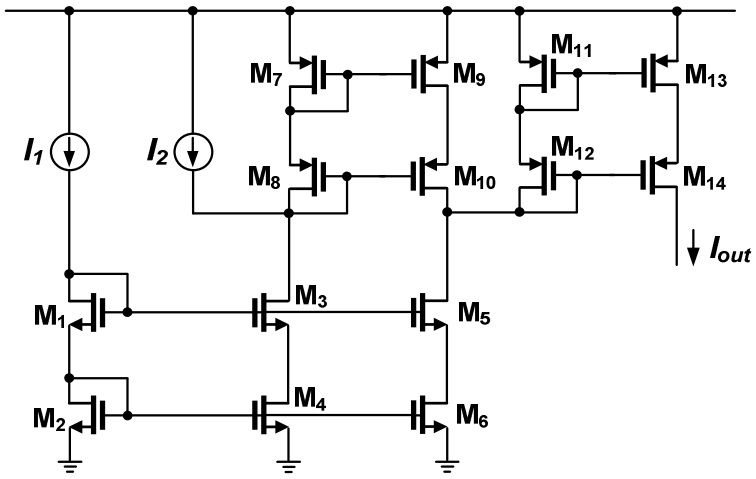


Figure 4.1 : Circuit diagram of the minimum current selector [5].

Aminifar et al. have been proposed another method to implement MAX circuit [9] shown in Figure 4.2. The key idea of the design is that there exists an individual way for I_1 to pass through transistor M_1. Moreover, there is an individual way for I_2 to pass through transistor M_2. If $I_1 > I_2$, transistors M_1 and M_2 act as a current mirror and I_1 passes through each of them. In addition, corresponding to that the I_2 necessarily has a single pass to go through. The extra current of $(I_1 - I_2)$ is provided through M_f. Therefore, the reflected current in M_3 will be equal to I_1, which is the maximum current of the applied inputs.

If $I_2 > I_1$, corresponding to that I_2 goes through M_2 and I_1 goes through M_1 and the least current which goes through M_f is zero. Then M_f will be disconnected and the currents of M_1 and M_2 will be different. Consequently, M_1 goes to linear state and M_2 remains in saturation region. Therefore, the reflected current of M_3 is equal to I_2, which is the maximum current of I_1 and I_2.

Take notice that transistors M_{11}, M_{22} and M_{33} are added to provide cascode structure for having more precision.

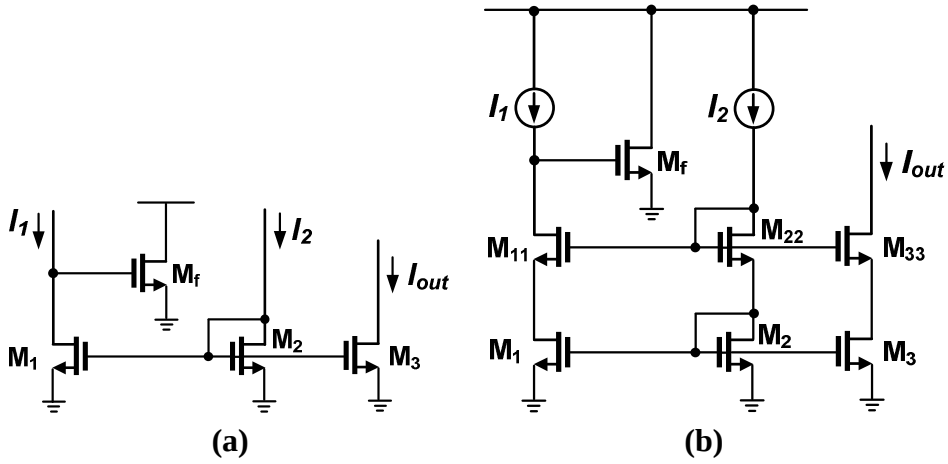


Figure 4.2 : (a) Main idea of Max circuit in [9] and (b) complete schematic of more accurate Max circuit.

Mesgarzadeh [79] has presented a new implementation of MIN-MAX circuits based on the mathematical representation of MIN and MAX operators. The principle of his proposed MIN-MAX circuits comes from following expressions:

$$Min(a,b) = \frac{a+b}{2} - \frac{|a-b|}{2} \qquad \textbf{(4.3)}$$

$$Max(a,b) = \frac{a+b}{2} + \frac{|a-b|}{2} \qquad \textbf{(4.4)}$$

In order to implement these equations in circuit level, circuits of Figure 4.3(a) and (b) has been proposed. In Figure 4.3(a) the Current Mirror (CM) consisting of M_1-M_2 is responsible for producing the term of $(I_1+I_2)/2$. The size of $M_1$is twice as much as the size of M_2. Two similar CM structure consisting of M_3-M_4 and M_5-M_6 are producing the second term at the right side of expressions (4) and (5). When $I_1 > I_2$ in the upper CM all of four transistors go to cut-off region. In this case CM consisting of M_5 and M_6 sinks a current equal to absolute value of $(I_1-I_2)/2$ from M_7. Otherwise the other CM will have the responsibility to conduct. In Figure 4.3(b) the same principle has been used but M_8 is eliminated to have sum operation between currents at output node. In this case the output can be equal to the maximum value of I_1 and I_2.

Because of the expression of (4.3) and (4.4), only two input can be applied to the circuit, then it cannot be used as a multi-input MIN or MAX circuit. Similar to Ref. [5] since the circuit is based on the current subtraction method, there will be a tradeoff between the speed and accuracy.

However, in the low frequencies, the precision of the circuit in selecting MIN or MAX input is acceptable.

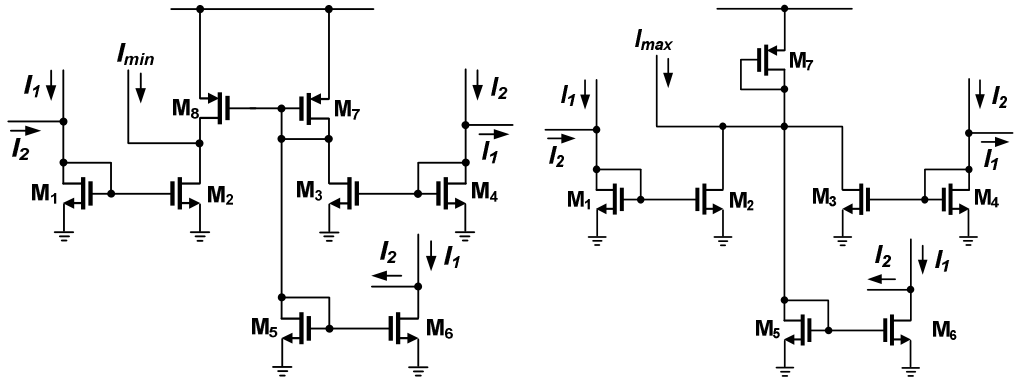


Figure 4.3 : Presented circuits in [79], (a) MIN circuit and (b) MAX circuit.

The circuit of Figure 4.4 have been proposed by Alikhani et al. which can detect minimum and maximum of the input currents at the same time [75]. Operation of the circuit is based on the modified-Wilson current mirror in bottom of the figure, which creates equal current in the branches under nodes A and B. Let us assume one of the input currents, for instance I_2 increases and ($I_1 < I_2$). This rise leads to a voltage

increase at the node B in comparison with the node A. Due to this difference M_{13} is on and M_{14} turns off, hence an extra current equal to I_2 - I_1 is transferred to the other current mirror through M_{13} and will be added to the minimum current of inputs (I_1) to produce the maximum output of the inputs which in this case is I_2. In other words, to obtain maximum of the inputs, the absolute difference between two inputs ($|I_1 - I_2|$) is added to the minimum current value of them. Similarly, if ($I_1 > I_2$), then the voltage of node A increases in comparison with the voltage of node B. Therefore, M_{13} is off and M_{14} is on and the extra current ($I_1 - I_2$) is transferred to the current mirror through M_{14} and will be added to the minimum current of the inputs to produces the maximum value of the two input currents. If the input currents are equal, two node voltages of A and B will be equal and both transistors M_{13} and M_{14} will turn off. In this case, both output currents of the circuit, minimum and maximum, are equal.

The main advantage of this structure is that both minimum and maximum of the inputs are simultaneously detected. Since the circuit performance relies on the current subtraction in the input nodes, so the error due to this operation is transfer to the output using Wilson current mirrors. As an another drawback, the number of possible applied input currents is limited by two, then it cannot be used as a multi-input MIN or MAX circuit.

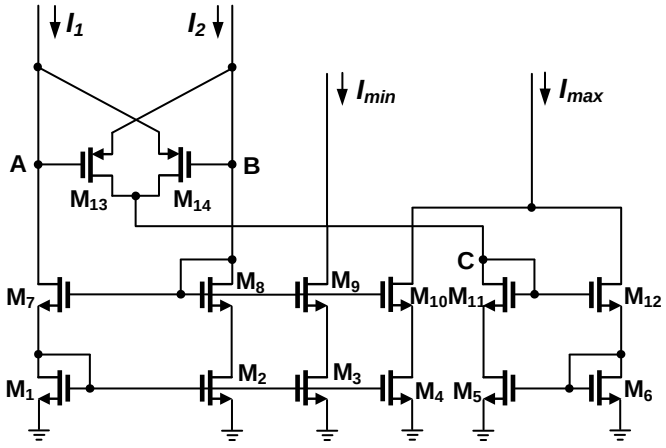


Figure 4.4 : Presented MIN-MAX circuit in [75].

A multi-input structure of MIN circuit have proposed by Asloni et al [76]. There are N cells which correspond to N inputs of the structure shown in Figure 4.5. The first input block is different from the others because this block produces the bias voltage of the circuit. For simplicity, suppose that the circuit has two inputs. In order to analyze the circuit, the operation region of the circuit is divided into three regions: In the first

region, $I_2 > I_1$. In this case, since the bias voltage is identified by I_1, and $I_2 > I_1$, M_4 cannot sink all of the current I_2. Therefore, M_4 only sinks I_1 and $I_2 - I_1$ is drawn by M_6. In the second region, $I_1 > I_2$; as I_1 is more than I_2 and the bias voltages of the circuit are identified by I_1, then M_2 and M_4 tend to work in triode region. For this reason, M_5 will be on and $I_1 - I_2$ is drawn by M_5. Therefore, M_2 stays in saturation region but M_4 leaves saturation region and operates in triode region. In the third region, $I_1 = I_2$, this region is located between latter two regions. In this region, as I_1 is the same as I_2 and the overdrive voltages of M_1 and M_2 are the same, hence M_5 and M_6 are in cut-off region. I_1 or I_2 is transferred to the output.

Although the circuit benefits from Multi-input configuration as well as the low power consumption feature, but it suffers from limited applied range of input current which is 0-20μA. In addition, the precision of the circuit in high frequencies is reduced, especially in the case of $I_1 \geq I_2$. The reason is that M_1, M_2 and M_5 are in saturation region, and drain to source voltages of M_1 and M_2 are not the same.

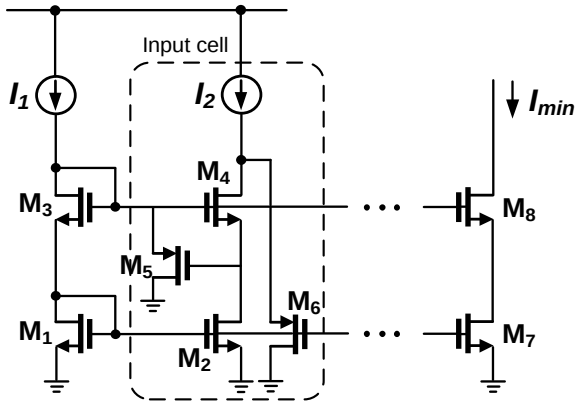


Figure 4.5 : Loser take all circuit presented in [76].

Peymanfer et al. have proposed a MAX circuit having the capability of being multi-input structure [7]. The circuit is based on the FVF configuration shown in Figure 4.6. The gate of all M_s transistors are connected to V_b and bias current is flowing through each of them, so gate-to-source voltage of all M_s transistors are the same, then V_{in} remains constant for each input current. When "m−1" input currents are less than winner input, M_t transistors of loser inputs are in saturation region, M_s transistors are in linear region, and M_f transistors are cut off.

When one of the input currents begins to increase, the gate voltage of M_t transistors increases lightly and drain voltage of M_s of winner input cell increases, then M_s goes

to saturation region. In this case, M_f of winner input cell begins to operate in saturation region, so the maximum input current appears at the output.

The input range of the circuit is relatively narrow (0-10μA) and the operation speed is low due to the fact that large channel length transistors should be chosen to accurate mirror of the input currents. On the contrary, the precision of the circuit is acceptable in low frequencies especially at the tracking points of the signals, as the author claimed this point.

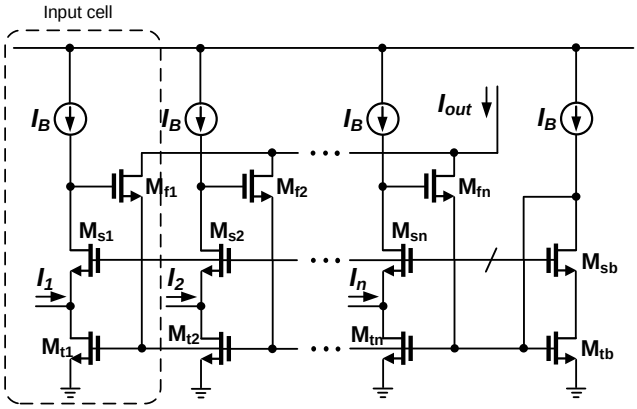


Figure 4.6 : Winner take all circuit presented in [7].

4.3 Proposed LTA and WTA Circuits

The proposed *n*-input LTA circuit is shown in Figure 4.7. Corresponding to each input, there is a cell determined within the dashed box in the figure. This structure uses a simple feedback to identify the minimum value of the input currents. The gates of all M_{xn} and M_{yn} transistors are connected in nodes b and d respectively. Each input signal is applied using a PMOS cascode current mirror depicted in the figure. M_{b1} and M_{b2} as well as the constant current of I_b provide bias voltage for LTA cells, and M_{b3} and M_{b4} make up the output stage.

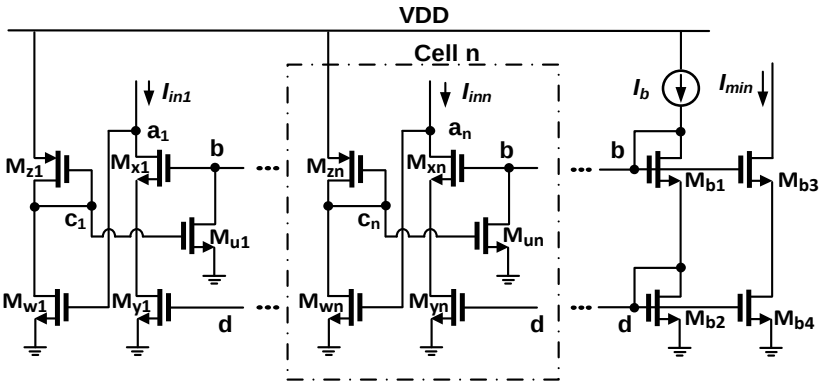


Figure 4.7 : Proposed n-input loser-take-all circuit.

M_{wn} is biased in the triode region, and performs as a resistor whose value is controlled by the overdrive voltage. The relationship can be represented by:

$$R_{wn} \approx V_{DS} / I_{DS} \approx (\mu C_{ox} (W / L)_{wn} (V_{GSwn} - V_{TN}))^{-1} \quad \textbf{(4.5)}$$

M_{un} is biased such that it operates in the threshold of turning on and off. To analyze the circuit, assume that LTA consists of two inputs (n=2) for simplicity. Suppose that I_2 is more than I_1, this leads to the voltage at node a_2 to be risen up to nearly V_{DD}; therefore, M_{g2} and M_{h2} go to triode region. However, voltage at node c_2 falls down due to the reduction in the resistor of M_{w2}; therefore, M_{u2} leaves saturation region and will be cut-off and cell 2 makes no change in the output current. At the same time, considering cell 1, voltage of node a_1 decreases to nearly ground, which in turn increases the voltage of node c_1 thanks to the increasing of resistor of M_{w1}. Hence, M_{u1} turns on and sinks extra current of I_b up to the point that I_{out} becomes equal to I_1. Take notice that, this process happens to all cells of the circuit, as a result, output current is always equal to the minimum value of the input currents. The same procedure occurs for $I_1 > I_2$ for cell 1 instead of cell 2. When I_1 is equal to I_2, the only difference is that both M_{u1} and M_{u2} go to saturation region simultaneously. They equally sink extra current of I_b. In this case I_1 or I_2 is transferred to the output.

MIN and MAX of n parameters like x_1 , x_2,..., x_n can be converted to each other according to De Morgan's law as follows:

$$\max\ (x_1, x_2, ..., x_n) = \overline{\min\ (\overline{x_1}, \overline{x_2}, ..., \overline{x_n})} \quad \textbf{(4.6)}$$

In order to realize this equation, since current of 10 µA has been normalized to 1, MAX of I_{in1}, I_{in2} ,..., I_{inn} can be given by: follows:

$$\max\ (I_{in1}, I_{in2}, ..., I_{inn}) = 10\mu A - [\min\ (10\mu A - I_{in1}, 10\mu A - I_{in2}, ..., 10\mu A - I_{inn})] \quad \textbf{(4.7)}$$

Thus, using designed MIN circuit and some current sub-tractor, MAX circuit is implemented as shown in Figure 4.8. Take notice that all of the normalized currents of 10 µA are provided via single source using a current mirror.

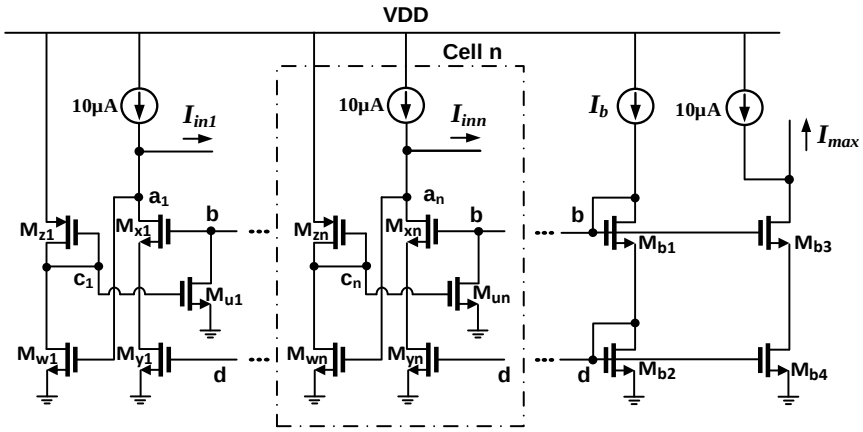


Figure 4.8 : Winner-take-all circuit based on De Morgan's law.

4.3.1 Performance analysis

In this section, the conditions in which the circuit operates are thoroughly analyzed. For the case of $I_2>I_1$, M_{u1} goes to saturation region, while M_{w1} still is in triode region and since $V_{GSu1}=V_{DSw1}$, the relationship can be written as:

$$V_{TN} \le V_{GSu1} \le V_{GSw1} - V_{TN} \tag{4.8}$$

$$V_{TN} \le V_{GSu1} \le V_{DD} - |V_{GSg1}| - |V_{DSh1}| - V_{TN} \tag{4.9}$$

Because M_{un} sinks extra current of I_b, the minimum current in terms of I_b, I_{DSu1} and I_{DSu2} yields to:

$$I_{\min} = I_b - (I_{DSu1} + I_{DSu2}) \tag{4.10}$$

Replacing (4.9) into (4.10) and simplifying the inequality we have:

$$0 \le \sqrt{\frac{2(I_b - I_{\min})}{k_{u1}}} \le V_{DD} - |V_{TP}| - 2V_{TN} - 2\sqrt{\frac{2I_{\min}}{k_{g1}}} \tag{4.11}$$

where $k_{n(p)}= \mu_{n(p)}C_{ox}$ (W/L) is transconductance parameter and V_{TN} and $|V_{TP}|$ are threshold voltages of NMOS and PMOS transistors, respectively. Since the mobility of an NMOS transistor is approximately three times larger than that of a PMOS transistors ($\mu_n \approx 3\mu_p$), the aspect ratios of M_{un} and M_{gn} are chosen to have $k_{u1} \approx k_{g1}=K$. Solving (4.11) gives $I_b \ge I_{min}$ as a first condition. It means that bias current must be chosen larger than input current of each cell. In other words, input dynamic range of the LTA circuit can be broadened by setting I_b. It is worthwhile to mention that second

answer determines the minimum (output) current in terms of I_b, V_{DD} and transistor parameters as follow:

$$\sqrt{2(I_b - I_{\min})} + 2\sqrt{2I_{\min}} \le \sqrt{K}(V_{DD} - |V_{TP}| - 2V_{TN}) \quad \textbf{(4.12)}$$

When I_1 and I_2 are equal, the same procedure can be followed to obtain output current, except for (4.11). Both M_{u1} and M_{u2} are on so that: $I_{DSu1}=I_{DSu2}=(I_b-I_{min})/2$. Rewriting (4.11) we have:

$$\sqrt{\frac{I_b - I_{\min}}{k_{u1}}} + 2\sqrt{\frac{2I_{\min}}{k_{g1}}} \le V_{DD} - |V_{TP}| - 2V_{TN} \quad \textbf{(4.13)}$$

$$\sqrt{2(I_b - I_{\min})} + 4\sqrt{I_{\min}} \le \sqrt{2K}(V_{DD} - |V_{TP}| - 2V_{TN}) \quad \textbf{(4.14)}$$

4.3.2 Simulation results

To verify the performance of the proposed circuit, simulation results are presented using HSPICE with TSMC level 49 (BSIM3v3) parameters for 0.35 μm CMOS technology. Figure 4.9(a) shows simulation results of the proposed LTA as well as error values, in which two sinusoidal and one pulse signals in the range of 100 kHz with different amplitudes are applied. I_b is set to 10μA and the supply voltage is 3.3 V. Maximum error at the track point is 94 ns, while the average of absolute error is measured 12 ns which leads to the error of 0.12 %. The same simulation is carried out with the frequency of 10 MHz and input range of 0-100 μA as is shown in Figure 4.9(b). Other simulations are performed to prove the speed, input range and accuracy of the circuit for three input signals. The results are presented in Table 4.1. To examine the robustness of the circuit against the process variation, the Monte Carlo analysis is performed by applying mismatch in the transistors aspect ratio and threshold voltage according to (3.12) and (3.13). The result is depicted in Figure 4.10 and proves that 99% of samples are occurred with the error of less than ±1%.

Table 4.1 : Simulation results of LTA for three inputs.

Frequency (MHz)	Input range (μA)	Error (%)	Bias current (μA)
0.1	0-10	0.12	10
1	0-10	0.19	10
10	0-100	0.39	100

Table 4.2 : Comparison of the proposed LTA with previous works.

	[5]	[9]	[79]	[75]	[76]	[7]	This work
Multi-input	×	×	×	×	✓	✓	✓
Accuracy	✓	×	✓	×	×	✓	✓
Speed	×	✓	×	✓	×	×	✓
Power Consumption	×	×	×	×	✓	✓	×
Input Range	✓	✓	✓	✓	×	×	✓

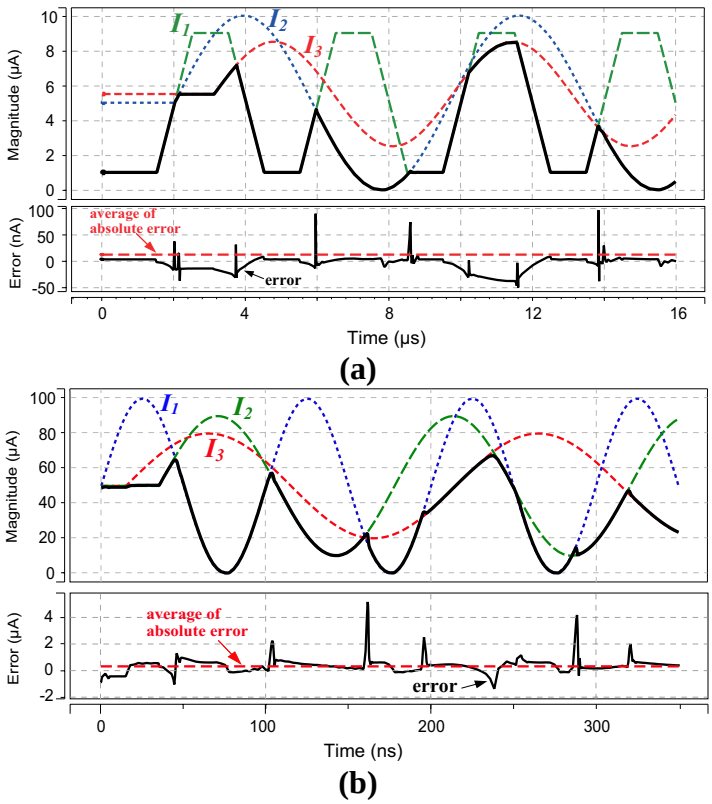


Figure 4.9 : Simulation results of the proposed LTA circuit for three inputs and corresponding error (a) f=100 kHz, (b) f=10 MHz

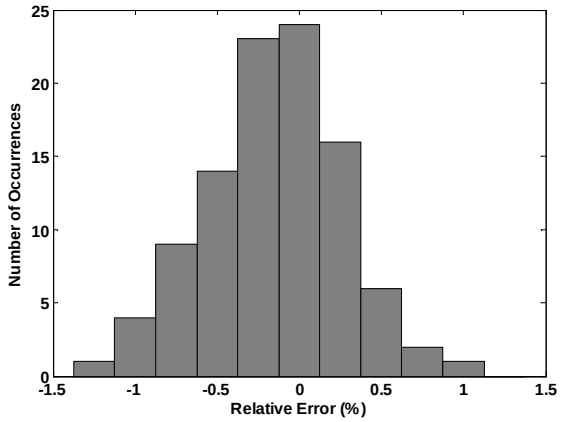


Figure 4.10 : The Monte Carlo analysis of LTA circuit for mismatch in threshold voltage and transistors aspect ratio (No. of iterations = 100).

4.4 Conclusion

A new CMOS current-mode loser-take-all circuit was presented. The proposed circuit consisted of three blocks; bias circuit, output stage and the basic cell. The bias circuit provided wide input dynamic range by setting the bias current. Simple expansion of the circuit to multi-input LTA was the advantage of designing basic cell. High accuracy as well as high speed operation were achieved owing to the usage of feedback structure. To increase the input range of LTA, it was required to increase the bias current, while the circuit dissipated more power. In view of this, as a further work low-voltage low-power methods such as level shifting techniques can be proposed. Comparison of the proposed circuit with former works are summarized in Table 4.2.

5. IMPLEMENTATION OF DEFUZZIFIER BLOCK

As mentioned in section 2.3.4, due to the fact that all activated membership functions of the consequents (all active rules) take part in the defuzzification process, COG is one of the most popular methods for defuzzification process. Mathematically, the COG method can be expressed as follows [23]:

$$COG = \frac{\sum_{i=1}^{n} x_i \mu_A(x_i)}{\sum_{i=1}^{n} \mu_A(x_i)} \quad \textbf{(5.1)}$$

where n is the number of the discrete elements in the universe of discourse, x and $\mu_A(x_i)$ are the output fuzzy variable and its membership function degree due to the consequent fuzzy rules, respectively.

In the view of circuit realization, the current-mode expression of (5.1) can be written as:

$$I_{COG} = \frac{\sum_{i=1}^{n} I_{x_i} I_{\mu_A(x_i)}}{\sum_{i=1}^{n} I_{\mu_A(x_i)}} \quad \textbf{(5.2)}$$

Therefore we need circuits to multiply x_i and $\mu_A(x_i)$, and divide the results over the sum of firing values. Then summing all output currents by simple wiring results in the desired defuzzification.

In the following subsections, firstly, a new multiplier circuit is proposed based on the dual-translinear loop. The circuit relies on a specific topology to omit the body effect of the multiplier circuit.

Secondly, a novel method to implement computational circuits including divider, multiplier, squarer and square-rooter using a linearly tunable OTA are proposed.

5.1 Design of Analog Multiplier

5.1.1 Introduction

The four-quadrant multiplier is a very important building block of analog signal processing system. It has many applications in automatic gain controlling, modulation, frequency translation, square rooting of signals, phase locked loop, neural networks and fuzzy integrated systems. Many CMOS circuits pertaining to these basic blocks are already available in the literature [80-83]. Ideally, an analog multiplier produces linear product of two input signals such as x and y, yielding $z=K\times x\times y$, where K is a constant with suitable dimension. Similar to other analog circuits, multiplier circuits can be categorized into two main groups: voltage-mode and current-mode. The current-mode multipliers attracted significant interest and have been extensively investigated in recent years [83-100], thanks to the potential advantages of high speed operation due to low parasitic capacitor nodes, low power consumption and simple circuitry [70].

Translinear principle is one of the most utilized methods in the design of current-mode circuits, employing loop transistors operating either in subthreshold region [85]-[87] or saturation region [84], [88]-[92]. Although the technique leads to circuits offering low power consumption in subthreshold region, the dynamic range and the operation speed of the designed circuits turn out to be limited. In the saturation region, the conventional translinear circuits are of so called *"stacked"* and *"up-down"* topologies which are realized using only NMOS or PMOS transistors [84, 90, 91]. On the other hand, design experiences in the past years indicate that circuits based on the *"dual translinear loops"* which consist of both NMOS and PMOS transistors may offer significant advantages in comparison with the conventional *"stacked"* or *"up-down"* topologies in terms of bandwidth, dynamic range and speed [70, 88, 89, 92] which compose of only NMOS or PMOS transistors.

Nonetheless, the body effect is an important problem in circuits based on dual translinear loops in a way that this effect causes mismatches in the threshold voltages which in turn, influences the linearity and accuracy of the circuit. In some existing analog multipliers, the effect of the transistor mismatches was properly studied and a few techniques were proposed in order to reduce the body effect [93, 94]. However,

none of these are of dual-translinear configurations and they suffer from low accuracy and/or low bandwidth.

In addition, multipliers reported in [82, 88, 95, 99] require dual supply voltage, which is not suitable for integrated circuit design. Another salient feature of multiplier circuits is the four-quadrant operation capability, an important asset very useful in various applications [96, 97]. Some of the well known multiplier circuits operate only in one [91, 98] or two [95, 99, 100] quadrants.

In this section, a new four-quadrant analog multiplier circuit based on the dual-translinear loop is proposed. High linearity, high precision and a wide dynamic range originating from the dual-translinear loop configuration are advantages of the circuit. The performance of the proposed multiplier is characterized using Cadence and HSPICE with TSMC level 49 (BSIM3v3) parameters for 0.35 μm CMOS technology.

This section is organized in 5 subsections: The circuit description of proposed multiplier is presented in subsection 5.1.2, followed by the performance analysis in subsection 5.1.3. In subsection 5.1.4, HSPICE simulation results of proposed circuit are presented to prove the efficiency of the design. Finally, conclusions are outlined in subsection 5.1.5.

5.1.2 Circuit description

The principle of the proposed multiplier is based on the square-difference algebraic identity, which is $(x+y)^2 - (x-y)^2=4\times x\times y$. Thus, the multiplier needs summing, subtraction and squaring operations. In the current-mode approach, the summation and subtraction of two signals are simply realized by interconnecting the corresponding current output terminals, as a result of Kirchhoff's current law. The design of the squarer and subsequently multiplier circuit are described below.

Figures 5.1 and 5.2 show the proposed squarer and the four-quadrant multiplier circuits, respectively. The squarer circuit is designed based on the translinear principle, and the multiplier circuit consists of two dual-translinear loops, where the first loop consists of M5, M8, M10 and M12 realizes $(x+y)^2$ function, while the second loop (M25, M26, M29, M33) provides $(x- y)^2$ function.

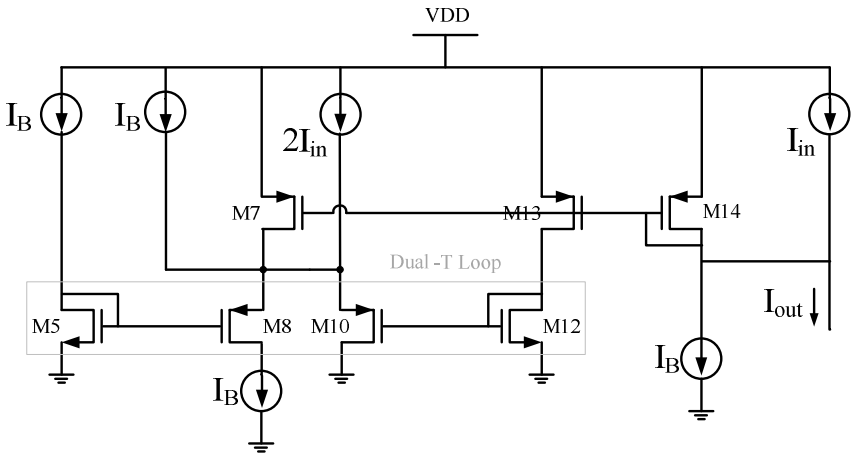


Figure 5.1 : Basic schematic of the proposed squarer circuit.

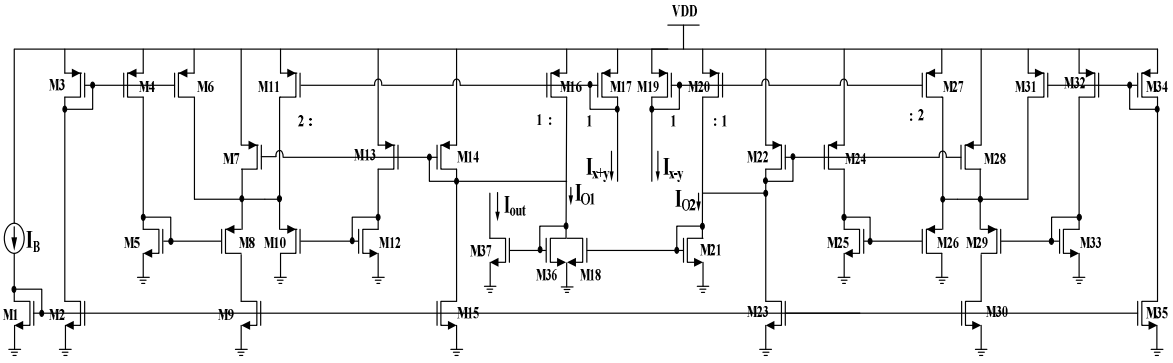


Figure 5.2 : Proposed analog multiplier circuit based on two dual-translinear loops.

Let us consider the dual-translinear loop composed of transistors M5, M8, M10 and M12 in Figure 5.2, yields to:

$$V_{GS5} + V_{GS8} = V_{GS10} + V_{GS12} \qquad \textbf{(5.3)}$$

Assuming that these transistors are biased in the saturation region and perfectly matched, from translinear loop principle, one can obtain:

$$\sqrt{I_{DS5}} + \sqrt{I_{DS8}} = \sqrt{I_{DS10}} + \sqrt{I_{DS12}} \qquad \textbf{(5.4)}$$

Since the drain currents I_{DS5} and I_{DS8} are equal to a constant current source, i.e., I_B, one can easily express the drain currents of M10 and M12 as follows: as:

$$I_{DS10} = I_{O1} + I_{x+y} + I_B \qquad \textbf{(5.5)}$$

$$I_{DS12} = I_{O1} - I_{x+y} + I_B \tag{5.6}$$

Substituting (5.5) and (5.6) into (5.4) and taking the square of both sides, we have:

$$2\sqrt{I_B} = \sqrt{I_B + I_{O1} - I_{x+y}} + \sqrt{I_B + I_{O1} + I_{x+y}} \tag{5.7}$$

$$4I_B = 2I_B + 2I_{O1} + 2\sqrt{I_B{}^2 + I_{O1}{}^2 + 2I_B I_{O1} - I_{x+y}{}^2} \tag{5.8}$$

By squaring both sides again, output current can be written as:

$$I_{O1} = \frac{I_{x+y}{}^2}{4I_B} \tag{5.9}$$

It can be seen from (5.9) that the current I_{O1} is the square of the input current; hence, this subcircuit is the basic building block of the CMOS analog multiplier. The same procedure can be followed for the second translinear loop to obtain I_{O2}.

To design the four-quadrant multiplier, output of the squarer circuit resulted from positive input current, should remain the same as the input becomes negative. Considering Figure 5.2 and first translinear loop, by changing the polarity of the input current (positive into negative or vice versa), rewriting the currents of M10 and M12 yields:

$$I_{DS10} = I_{O1} - I_{x+y} + I_B \tag{5.10}$$

$$I_{DS12} = I_{O1} + I_{x+y} + I_B \tag{5.11}$$

The only difference is that the corresponding terms in (5.5) and (5.6) are interchanged, while the output current is still the same.

M18, M21, M31 and M37 form current subtraction of two squarer circuits as:

$$I_{out} = I_{O1} - I_{O2} = \frac{(I_x + I_y)^2}{4I_B} - \frac{(I_x - I_y)^2}{4I_B} = \frac{I_x I_y}{I_B} \tag{5.12}$$

Thus, (5.12) yields the multiplication between I_x and I_y divided by constant current of I_B which is normalized to one. Bearing in mind that the signals I_{x+y} and I_{x-y} are realized using an additional input stage composed of simple current mirrors (see Figure 5.3).

Next section provides performance analysis of the circuit and deviations from ideal assumptions followed by supporting simulation results.

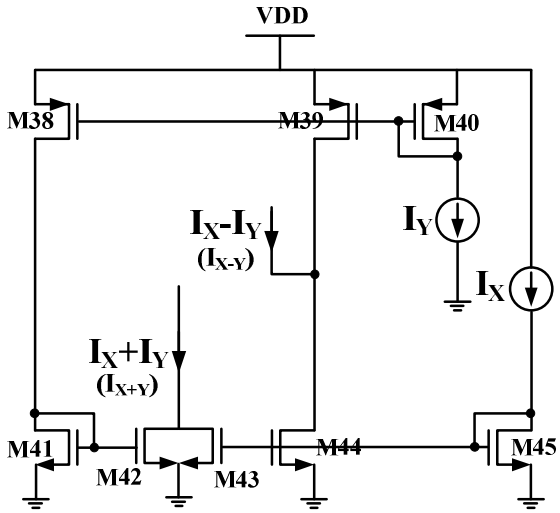


Figure 5.3 : Additional circuit to provide required currents for multiplier circuit.

5.1.3 Performance analysis

In this section, the harmonic distortion caused by mismatch in the input stage transistors are studied in details which leads to errors in the currents I_{x+y} and I_{x-y}. Following that, the effects of mismatches in the transconductance parameters of the transistors in the dual-translinear loops as well as mismatch in the threshold voltages due to transistor body effects are thoroughly analyzed. Finally, the input / output ranges and impedances of the proposed multiplier are derived.

5.1.3.1 Input current mismatch

The proposed multiplier requires two well-matched input signals (I_x and I_y). It is worthwhile to mention that the mismatch in the input signals leads to second harmonic distortion terms at the output of the multiplier circuit.

$$I_{xi} = \hat{I}_x + \Delta x_i \hat{I}_x \quad \textbf{(5.13)}$$

$$I_{yi} = \hat{I}_y + \Delta y_i \hat{I}_y \quad \textbf{(5.14)}$$

The where $\hat{I}_x$ and $\hat{I}_y$ are mean values, and Δx_i and Δy_i are mismatch percentages of $\hat{I}_{xi}$ and $\hat{I}_{yi}$, respectively. By applying $\hat{I}_x + \hat{I}_y$ and $\hat{I}_x - \hat{I}_y$ to the multiplier circuit, and considering Δx_i^2, Δy_i^2 and $\Delta x_i \Delta y_i << 1$ the output current is given by:

$$I'_{out} \approx \frac{\hat{I}_x \hat{I}_y}{I_B} + \frac{\delta_x \hat{I}_x{}^2 + \hat{I}_x \hat{I}_y (\delta_x + \delta_y) + \delta_y \hat{I}_y{}^2}{2I_B} \quad \textbf{(5.15)}$$

where:

$$\delta_x = \Delta x_1 - \Delta x_2 \quad \textbf{(5.16)}$$

$$\delta_y = \Delta y_1 - \Delta y_2 \quad \textbf{(5.17)}$$

If one of the inputs ($\hat{I}_x$) is kept constant and the other one is sinusoidal in the form of $\hat{I}_y = \hat{i}_m \sin \omega t$, second harmonic distortion with respect to the input signal mismatches can be derived as follows:

$$HD_2 = \frac{\delta_x}{\hat{I}_x (\delta_x + \delta_y) + 2\hat{I}_x} \hat{i}_m \quad \textbf{(5.18)}$$

It should be point out that when the mismatch percentage of $\hat{I}_x$ increases (see (5.18)), second harmonic distortion also increases (decrease in dB). Nonetheless, it nearly remains steady and does not significantly affect the third harmonic distortion as did not appear in the hand calculations.

5.1.3.2 Transconductance parameter mismatch

In this section, detailed analysis of mismatching between the transconductance parameters of NMOS and PMOS transistors is provided and the errors affecting the ideal performance of the proposed circuit are studied.

The mismatch of the transconductance parameter can be modeled as follows:

$$K_P = K + \Delta k K \quad \textbf{(5.19)}$$

$$K_N = K - \Delta k K \quad \textbf{(5.20)}$$

where K is a mean value and Δk is a mismatch percentage of the transconductance parameter. Assuming this, (5.4) becomes:

$$\sqrt{\frac{I_B}{K+\Delta kK}}+\sqrt{\frac{I_B}{K-\Delta kK}}=\sqrt{\frac{I''_{O1}+I_{x+y}+I_B}{K+\Delta kK}}+\sqrt{\frac{I''_{O1}-I_{x+y}+I_B}{K-\Delta kK}} \quad \textbf{(5.21)}$$

Simplifying (5.21) and ignoring terms containing Δk^2 (because $\Delta k << 1$), output current of the squarer circuit can be written as:

$$I''_{O1} \approx \frac{I_{x+y}{}^2+2\Delta kI_BI_{x+y}}{4I_B+2\Delta kI_{x+y}} \quad \textbf{(5.22)}$$

Equation (5.22) implies that, transconductance mismatch leads to the slope and offset at the output of the squarer circuit. By applying summation and subtraction of the signals to the proposed multiplier circuit, one can reach the output current as:

$$I''_{out}=I''_{O1}-I''_{O2} \approx \frac{4I_B{}^2I_y\Delta k+4I_xI_yI_B+I_x{}^2I_y\Delta k-I_y{}^3\Delta k}{4I_B{}^2+4I_BI_x\Delta k} \quad \textbf{(5.23)}$$

Applying $\hat{I}_x$ as a constant current and $\hat{I}_y = \hat{i}_m \sin\omega t$, third harmonic distortion caused by the transconductance parameter mismatch is given by:

$$HD_3=\frac{\Delta k}{16I_B{}^2\Delta k+4I_x{}^2\Delta k+16I_BI_x+3\Delta k}\hat{i}_m{}^2 \quad \textbf{(5.24)}$$

In short, when the transconductance mismatch of loop transistors increases, third harmonic distortion increases at the same time (decrease in dB), while the second harmonic distortion is not much affected by this.

5.1.3.3 Error due to body effect and threshold voltage mismatch

In section 5.1.2, body effect which influences threshold voltages of the loop transistors was ignored to simplify the basic circuit calculations. This section investigates the effect of this non ideality on the circuit performance.

In an MOS transistor, body effect refers to change in the transistor threshold voltage (V_{TH}) resulting from a voltage difference between the transistor source and substrate, which can be characterized by:

$$V_{TH} = V_{t0} + \gamma[\sqrt{(V_{SB} + |2\varphi_F|)} - \sqrt{|2\varphi_F|}] \quad \textbf{(5.25)}$$

where V_{t0} is the zero-bias threshold voltage, γ is the body-effect coefficient and ϕ_F is the Fermi potential.

Considering non-ideal case for equality of threshold voltages for NMOS and PMOS transistors in one of the dual-translinear loops and subsequently, rewriting (5.4) we have:

$$V_{TH5} + \sqrt{\frac{I_{DS5}}{K_5}} + V_{TH8} + \sqrt{\frac{I_{DS8}}{K_8}} = V_{TH10} + \sqrt{\frac{I_{DS10}}{K_{10}}} + V_{TH12} + \sqrt{\frac{I_{DS12}}{K_{12}}} \quad \textbf{(5.26)}$$

Since sources of M8 and M10 are tied to the same node, V_{SB8} and V_{SB10} are quite equal; as a result V_{TH8} and V_{TH10} are modified equally by body effect. So, although it is possible, there is no requirement for separate wells to obtain $V_{TH8} = V_{TH10}$ equality. Similarly, since V_{SB5} and V_{SB12} are zero, V_{TH5} and V_{TH12} are not affected by body effect so that this results in their equality (equal to V_{t0}). This causes V_{TH5} and V_{TH8}, cancel out V_{TH10} and V_{TH12}, respectively, and (5.4) can be written precisely.

5.1.3.4 Input /output ranges and impedances

Input dynamic range of the multiplier is restricted by the dual-translinear loop transistors which should operate in the saturation region.

To determine this range in terms of bias current assume that $I_{in} = \beta I_B$, rewriting (5.4):

$$2\sqrt{I_B} \geq \sqrt{(1-\beta)I_B + \frac{\beta^2 I_B}{4}} + \sqrt{(1+\beta)I_B + \frac{\beta^2 I_B}{4}} \quad \textbf{(5.27)}$$

Solving this inequality gives $-2I_B \leq I_{in(SQ)} \leq 2I_B$ as an input range of the squarer circuit, and $-I_B \leq I_{in(MUL)} \leq I_B$ for the multiplier circuit. In addition, one can find the output ranges as $0 \leq I_{out(SQ)} \leq I_B$ and $-I_B \leq I_{out(MUL)} \leq I_B$ for the squarer and multiplier circuits, respectively.

It should be noted that high output impedance is an important characteristic of the current mode circuits. The proposed circuit enjoys this feature providing an output impedance equal of the intrinsic drain-source resistance of M37. Although typical value of this impedance value is sufficiently high for many applications, higher output

impedance can be further achieved by using cascade-connected transistors instead of M18, M21, M36, M37, where the bias current is chosen 10 μA. On the other hand, small input impedance is equally important asset of current-mode circuits. Considering Figure 5.3 as the input stage of the circuit, and I_X and I_Y are the input currents, it is easy to verify that the input impedances are equal to $1/g_{m45}$ and $1/g_{m40}$, respectively.

5.1.4 Simulation results

In this section, post layout simulations are presented using Cadence and HSPICE with TSMC level 49 (BSIM3v3) parameters for 0.35 μm CMOS technology so as to verify the performance of the proposed circuit.

Figure 5.4 shows layout of the multiplier circuit drawn by single poly and two metals (Metal1 and Metal2), in which the area is 39.95 μm × 40.15 μm.

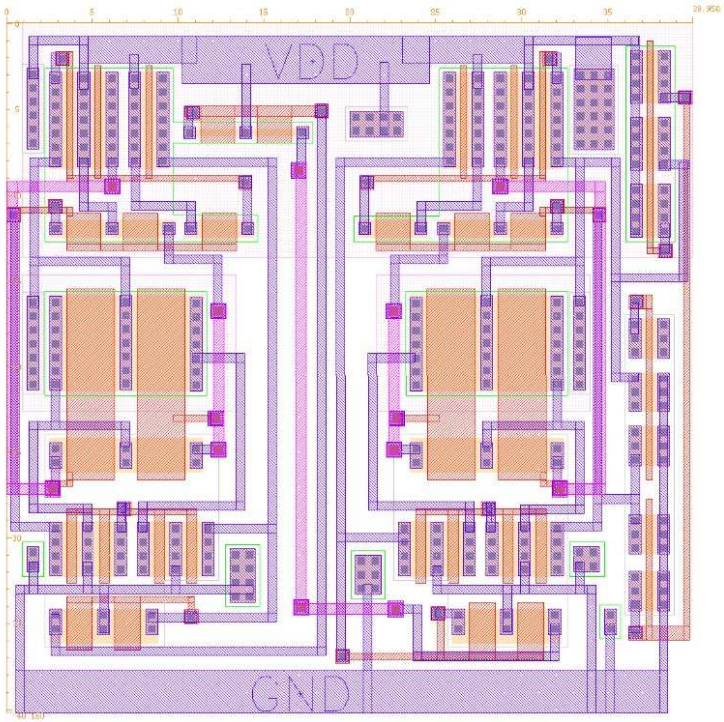


Figure 5.4 : Layout of proposed analog multiplier.

The aspect ratio of transistors is given in Table 5.1, the supply voltage is 3.3 V, and I_B is set to 10 μA. Simulation result for the squaring circuit is depicted in Figure 5.5, while a triangle waveform is applied to the circuit; then output current as well as the error value are illustrated. It shows a maximum of 60 nA error at the output which verify the accuracy of the circuit.

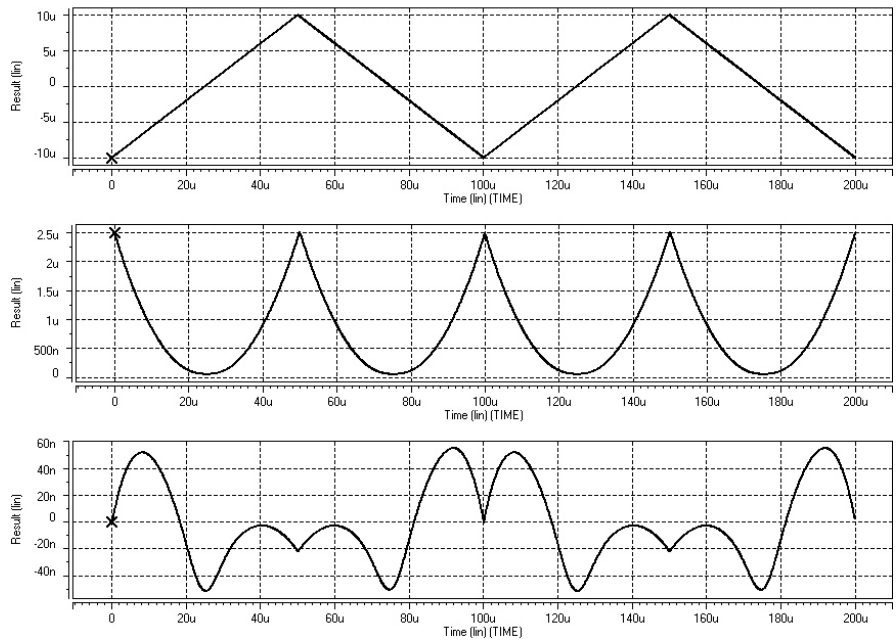


Figure 5.5 : Simulation result of the current squaring circuit and error measurement.

Figure 5.6 shows DC transfer characteristic of the proposed analog multiplier which illustrates high linearity in the mentioned range of the inputs, where the output current swings between -10 μA to +10 μA. Within this range, the measured nonlinearity error is 1.12%.

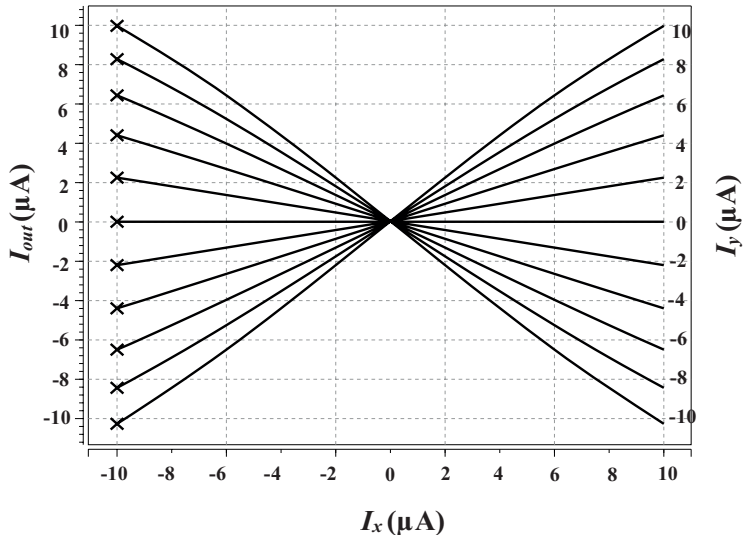


Figure 5.6 : Post layout simulation result for DC transfer characteristic.

Table 5.1 : Transistor aspect ratios.

Transistor name	W/L (µm/µm)
M1, M2, M9, M15, M23, M30, M35	3.2/0.6
M7, M13, M14, M22, M24, M28	5.6/0.35
M3, M4, M6, M31, M32, M34	1/2
M16, M17, M19, M20	4/0.35
M5, M12, M25, M33	2/2.8
M8, M10, M26, M29	5.6/2.8
M11, M27	8/0.35
M18, M21, M36, M37	2/ 0.6
M38, M39, M40	3/0.5
M41, M42, M43, M44, M45	2/0.5

Figure 5.7 shows the multiplier being used for balance modulator. I_x and I_y are 1 MHz and 100 kHz, 20 $\mu A_{P\text{-}P}$ sinusoidal carrier and modulation signals, respectively fed to inputs of the proposed multiplier, while I_B is constant. Figure 5.8 shows how the multiplier circuit can be employed as a frequency doubler. If both frequencies of the input currents are 1 MHz, the figure shows the corresponding output waveform with double frequency as well as the error quantity.

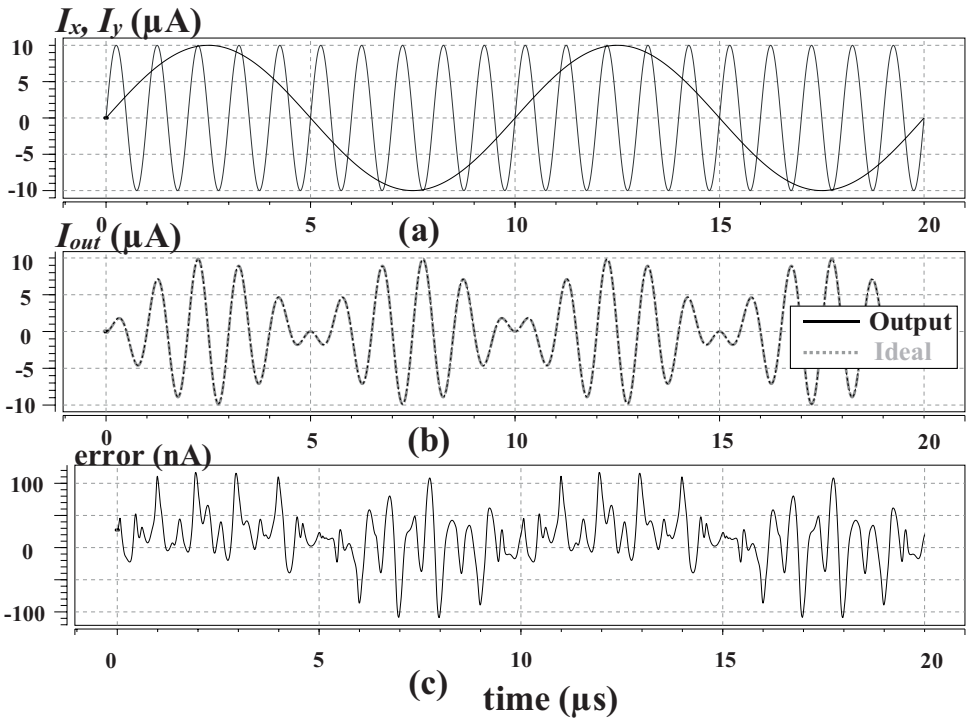


Figure 5.7 : The proposed multiplier as an amplitude modulator, (a) 100 kHz modulating signal and 1 MHz carrier signal; (b) modulated output (c) error measurement.

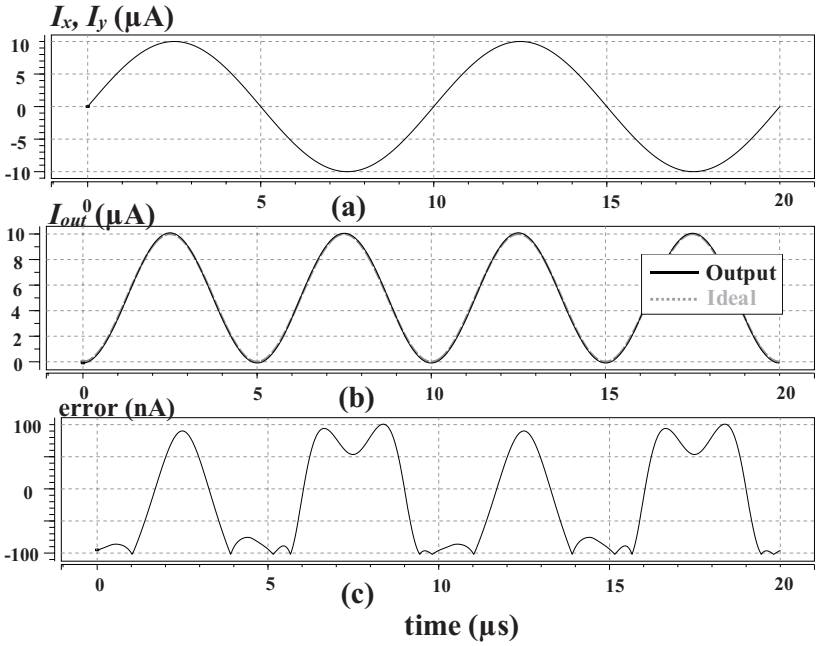


Figure 5.8 : The proposed multiplier is used as a frequency doubler (a) the input waveform (b) the output waveform (c) error measurement

The total harmonic distortion versus input signal at 100 kHz and 1 MHz is shown in Figure 5.9. In the worst case, an input signal of 20 μA_{p-p} at a frequency of 1 MHz resulted in a total harmonic distortion (THD) of less than 1.45%. Simulation results of Figures 5.10 and 5.11 verify the hand calculations of harmonic distortions in the previous section, where second and third harmonic distortions versus mismatch percentage of input signals and transconductance are achieved.

Figure 5.12 shows threshold voltage difference of NMOS and PMOS transistors in the dual-translinear loop versus different inputs, where I_x swings from - 10 µA to + 10 µA while I_y is constant (10 µA).

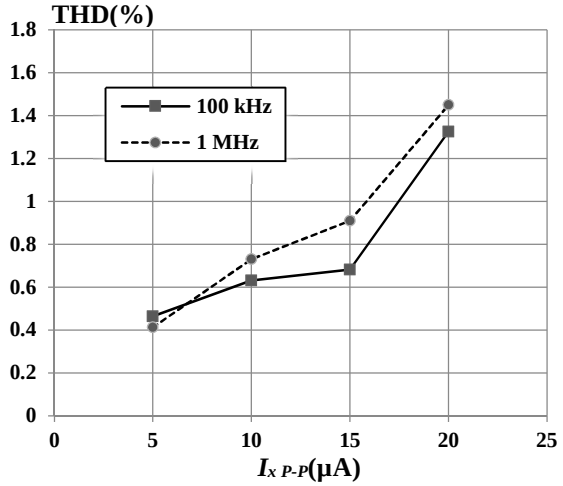


Figure 5.9 : Relation between THD and I_x.

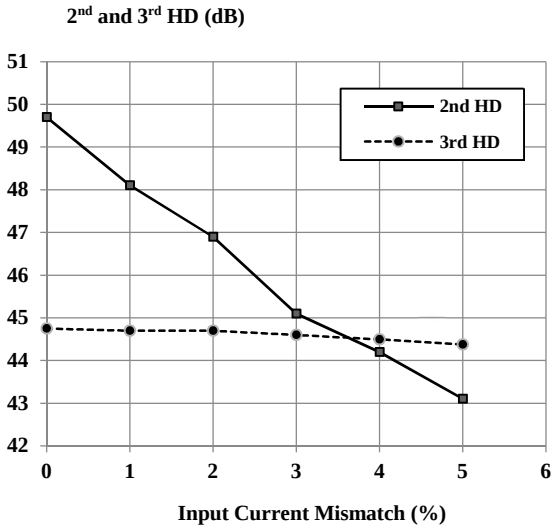


Figure 5.10 : Input current mismatch as a factor of second harmonic distortion.

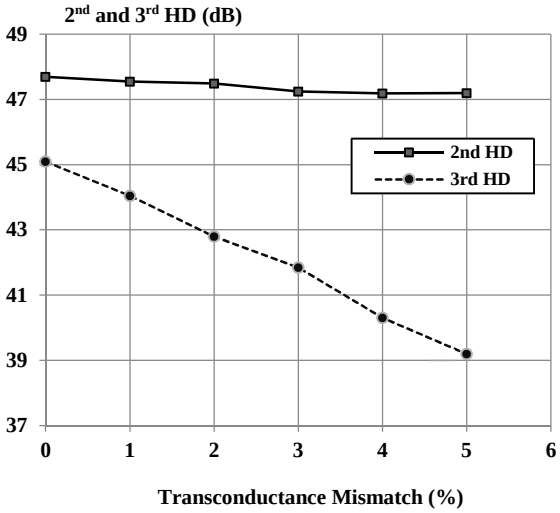


Figure 5.11 : Transconductance mismatch as the factor of third harmonic distortion.

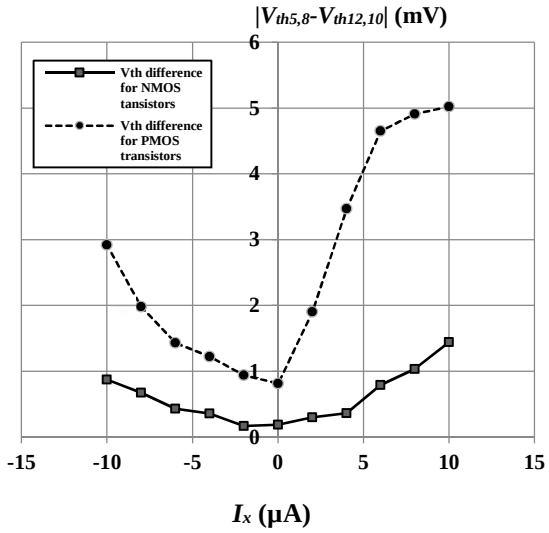


Figure 5.12 : Threshold voltage difference of NMOS and PMOS transistors in the dual-translinear loop versus different inputs.

The Monte Carlo analysis of the proposed circuit with 100 iterations is carried out by applying mismatch in transistors aspect ratio and threshold voltage with Gaussian distribution. This was done to ensure the robustness of the circuit performance against the fabrication process (see Figure 5.13). According to the figure, 91% of samples are occurred with the error of less than ±1%.

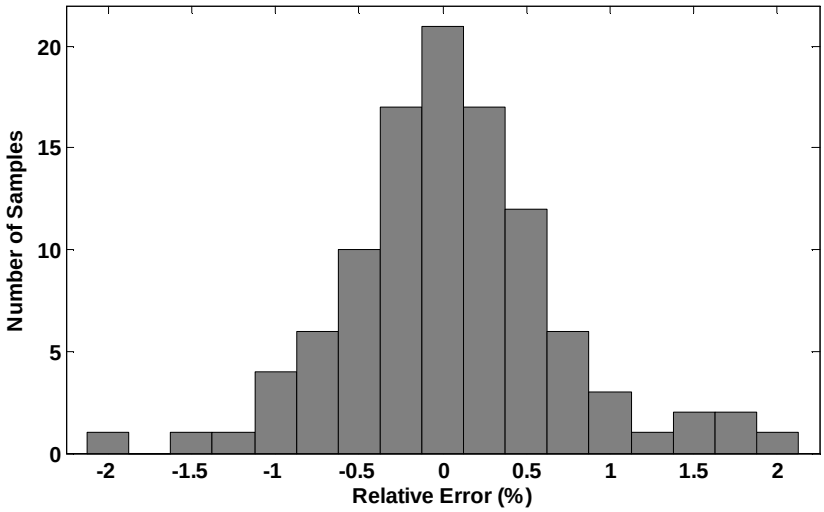


Figure 5.13 : Monte Carlo analysis of the multiplier circuit for mismatch in transistors aspect ratio and threshold voltage.

Frequency response of the circuit shows that -3 dB bandwidth is 137 MHz when the input signal is applied to I_x, and I_y = 10 μA and maximum power consumption is obtained 0.521 mW.

Table 5.2 summarizes some relevant results of the proposed multiplier and allows a deeper comparison. Take notice that in comparison with Ref. [89] (in 0.25 μm) speed was sacrificed in the design at the expense of more accuracy as shown in Figures 5.7 and 5.8; In addition, to improve the linearity of the multiplier circuit, fairly large gate length transistors was used, which affected the bandwidth of the circuit. Owing to the designing specific topology of dual-translinear loop, power consumption is slightly higher than prior works. It is worthwhile to mention that the power consumption can be decreased by reducing the bias current of the circuit. As an example, for the bias current of 1 μA, the dissipated power is obtained 0.12 mW.

Table 5.2 : Comparative parameters of the proposed multiplier with recent works.

	[100]	[90]	[89]	[88]	[70]	[82]	This work
Translinear Type/Method	Triode	Up-down	Dual	Dual	Dual	Subthreshold	Dual
Sensitivity to body effect	Dependent	Free	Dependent	Dependent	Dependent	Dependent	Free
Power cons. (mW)	2	0.6	0.17	0.46	0.34	0.067	0.521
Power supply (V)	3.3	3.3	2.5	± 1.5	3.3	1.5	3.3
THD(%) (1MHz-20μA)	0.2 (100 kHz)	1.5 (10 kHz)	0.91	3.7	0.97	4.2 (10 kHz)	1.45
Nonlinearity (%)	2.5	1.9	2.5	1.20	1.1	3.2	1.12
-3dB bandwidth (MHz)	3	3	278	19	41.8	0.268	137
Tech. (μm)	0.5	2.4	0.25	0.5	0.35	0.35	0.35
Area ($mm^{2)}$	0.083	0.24	0.033	-	0.009	-	0.016
Sim. or Meas.	Meas.	Meas.	Post Layout	Sim.	Sim.	Sim.	Post Layout

5.1.5 Conclusion

A new all-MOS analog multiplier was presented having the capability of operation in four-quadrant. The circuit relies on a specific topology of dual-translinear loop to omit the body effect of the multiplier circuit. High linearity and high accuracy were significant characteristics of the circuit. To study the performance of the proposed circuit, input and output range and harmonic distortion analysis were thoroughly discussed. In addition, the effects of mismatch in the transconductance parameters of the transistors in the dual-translinear loops as well as mismatch in the threshold voltages were analyzed. In order to simulate the proposed circuit, Cadence design tool and HSPICE simulator were utilized to verify the validity of the theoretical analysis. To illustrate the efficiency of the presented multiplier, it was employed as a balance modulator and frequency doubler, and the simulation results were compared with ideal performance of these applications. The presented topology of dual-translinear loop, consumed slightly more power than that of prior works, in view of this, as a further work low-voltage low-power methods such as level shifting techniques can be proposed.

5.2 Design of Computational Circuits Based on a New OTA

5.2.1 Introduction

Analog computational circuits are very useful building blocks finding various applications in the signal processing domain. These circuits realize multiplication, division, squaring and square rooting functions which are widely used in disk drives [101, 102], hearing aids [103, 104], medical equipment [105], modulators [82, 106, 107], artificial neural networks [108, 109] and fuzzy control systems [48, 107, 110].

There are many techniques to implement analog functional circuits [111-126] which can be roughly categorized in three main groups. The first group is based on the trans-linear (TL) principle introduced in [111]. This group is also classified in two subgroups including BJT and MOS trans-linear circuits.

In bipolar transistors, it employs the exponential characteristic of current and voltage [111], [112]. In this method the cause of error originates from the nonzero values of the base currents and of the temperature dependence of the bipolar transistor

parameters (the thermal voltage is linearly increasing with temperature and the saturation current has an exponential dependence on temperature).

In CMOS technology, TL principle relies on the exploiting of loop transistors operating either in weak inversion [113-115] or strong inversion [89, 90, 91, 116]. For weak inversion, although it leads to circuits offering low power consumption, the dynamic range and the operation speed turn out to be limited. For the TL principle in strong inversion, the body effect is a serious problem in a way that this effect causes mismatch in the threshold voltages which in turn, influences the linearity and accuracy of the circuits, however in some studies this effect was properly discussed and a few techniques were proposed [117, 118].

The most important aspects of computational circuits include power consumption, operation speed, design cost, simplicity and area efficiency. Although in practice, most of these parameters trade with each other and several design techniques have been proposed [119-121] to satisfy the compromise between these characteristics, but the main challenge in designing computational circuits is how to implement with minimal effort a large number of these functions [122]. One possible technique to do this is to design a multifunctional computational structure which is based on the possibility of a multiple use of the same structure as a core of the design. On the basis of this technique, if the design effort being mainly focused on the improving of the core performances, all of the functions which will be implemented through the use of the core structure will automatically be improved.

From this point of view, the second and third groups can be also classified; the second group emphasizes on the use of piecewise linear approximation method [123]-[127], expansion of the functions using Taylor series [128]-[130] and presenting a new approximation [131-134] in which each term of the approximated series is realized using a current-mode [123]-[128], [131]-[134] or voltage-mode [129, 130] basic building block. In order to simple realization of the functions, some of these approximations have been used second-order [128]-[130] or third-order [124, 133, 134] of terms which leads to low-precise implementation of computational circuits. Following this, the higher order approximations [127, 131, 132] have been proposed to achieve higher accuracy at the expense of complex structure and consequently higher consumption of power. The complex structures reported in [135, 136], but not based on the piecewise linear approximation method or expansion of Taylor series or

not CMOS-based circuits can be located in this group, owing to the fact that they also consume more power.

The third group deals with the structure based on the OTA. Although these structures can implement slightly less functions rather than the second group, but the advantages of reconfigurability, lower power consumption and higher accuracy encourage the designers to utilize this method. There are limited number of literatures on the use of OTAs for designing these circuits [137]-[141], while some of them do not allow multifunctional operation [137, 138] and some others suffer from having constant transconductance and not having entire linearity over the input range [139]-[141]. This problem in turn influences the performance of the implemented computational circuits in terms of accuracy and efficiency.

The objective of this work is to examine the applicability of a new LTOTA as a basic building block which is employed in a modified structure to implement computational circuits either linear or nonlinear functions. The proposed transconductance amplifier provides a constant G_m over a wide range of input voltage which allows the implementation of high precision computational circuits. In addition, the proposed LTOTA behaves as a bipolar OTA in which its transconductance is linearly tuned by the bias current, therefore all of the bipolar-based OTA configurations can be easily replaced by the CMOS LTOTA, while their performance nearly remains the same. Due to the simple and compact structure, the power consumption of the implemented circuits are comparatively low.

This section is organized as follows: Section 5.2.2 describes the proposed structure as well as the transistor level design for implementation of computational circuits. Section 5.2.3 analyzes the performance of the circuits with respect to input range, fundamental noise and transistor mismatch, followed by HSPICE simulation results of computational circuits in Section 5.2.4. Finally, conclusions are outlined in section 5.2.5.

5.2.2 Circuit description

In order to realize computational circuits, a CMOS based transconductance circuit is employed as a basic building block of the design. The proposed structure is shown in Figure 5.14, where I_{in} is the input current. The trans-conductance gains of OTA_1 and OTA_2 can be varied by adjusting an external dc bias current of I_1 and I_2 respectively.

According to the figure, the input current of I_{in} is injected into the OTA_1, which is employed as a current controlled grounded resistor. The voltage across the OTA_1 is then utilized as the input voltage for the OTA_2. Considering G_{m1} and G_{m2} as the trans-conductance gains of the OTA_1 and OTA_2 respectively, one can find the input-output relationship as follows:

$$\left.\begin{aligned} G_{m1}V_X &= I_{in} \\ G_{m2}V_X &= I_{out} \end{aligned}\right\} \Rightarrow I_{out} = \frac{G_{m2}}{G_{m1}} I_{in} \qquad \textbf{(5.28)}$$

If the trans-conductance of OTA_2 (G_{m2}) has the square-root proportion to its current, by keeping I_{in} and G_{m1} constant, the square-rooter circuit can be achieved. In the case of direct proportion of G_{m1} and G_{m2} to the current, the multiplier and divider circuits will be obtained. Also if $I_{in}=I_{Gm2}$ the squaring circuit is implemented. The implementation of these functions as well as their performance analysis will be thoroughly discussed in sections 5.2.4.

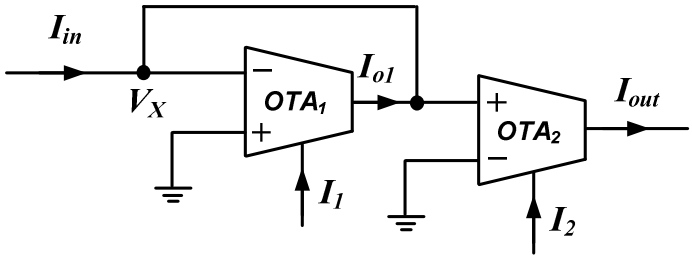


Figure 5.14 : Proposed structure for implementation of computational circuits.

5.2.2.1 Proposed CMOS OTA circuit

Figure 5.15 shows the trans-conductance circuit which is the basic building block to implement computational circuits. The differential input voltage of V_{in} is applied in the form of $V_{in} = V_1 - V_2$, and I_a and I_{ss} represent the bias and tail currents respectively. The operation of circuit is as follows:

Since the drain current of M_1 is constant ($I_{DS1}=I_a$), neglecting the body effect, V_{GS1} also has to remain constant; as a result any variation in the voltage of V_1, will be reflected to the source terminal (V_A) level-shifted by V_{GS1}. Supposing M_1 operates in saturation region, the voltage of this node is given by:

$$I_a = K(V_1 - V_A - V_{TH})^2 \qquad \textbf{(5.29)}$$

$$V_A = V_1 - V_{TH} - \sqrt{\frac{I_a}{K}} \tag{5.30}$$

where $K=0.5\mu_0 C_{OX}(W/L)$ is related to trans-conductance parameter and V_{TH} is the threshold voltage of MOS transistor.

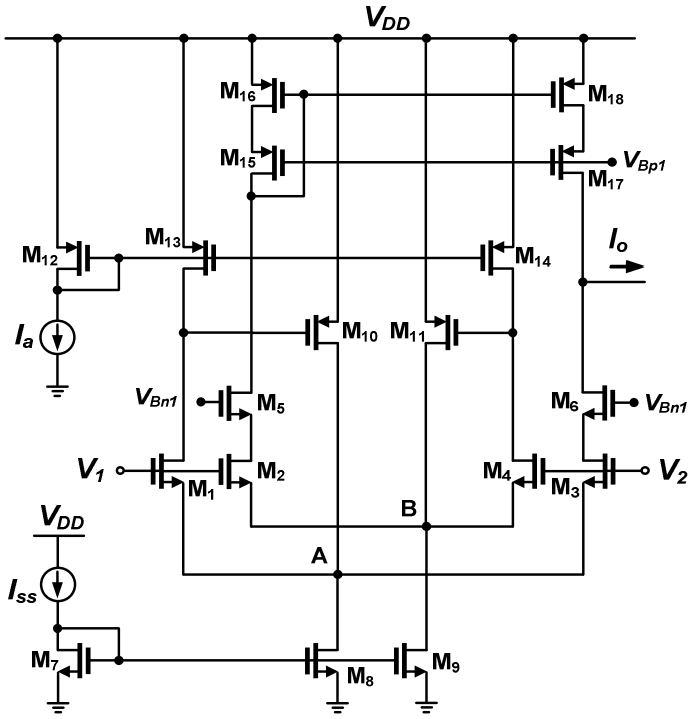


Figure 5.15 : Proposed OTA circuit.

The transistor M_3 works in saturation region as well, thus its current can be written as:

$$I_{DS3} = K(V_2 - V_A - V_{TH})^2 \tag{5.31}$$

Replacing (5.30) in (5.31) yields:

$$I_{DS3} = K\,(V_2 - V_1 + \sqrt{\frac{I_a}{K}})^2 \tag{5.32}$$

Similarly, one can find the current of transistor M_2 as:

$$I_{DS2} = K(V_1 - V_2 + \sqrt{\frac{I_a}{K}})^2 \tag{5.33}$$

Transistors M_{10} and M_{11} sink extra currents of nodes A and B respectively. This is due to the fact that I_{DS2} and I_{DS3} change with input voltage and since M_1 and M_4 have the

constant current of I_a, in order to prevent M_2 and M_3 being in linear region, M_{10} and M_{11} are considered.

Also transistors M_5 and M_6 are employed as a cascode stage to provide high output impedance at the output node. V_{Bn1} is chosen in which these transistors operate in the saturation region.

The transistors M_{15}-M_{18} act as a current sub-tractor which form the output current as follow:

$$I_o = I_{DS2} - I_{DS3} = 4\sqrt{KI_a}\left(V_1 - V_2\right) \tag{5.34}$$

or:

$$I_o = 4\sqrt{KI_a}V_{in} \tag{5.35}$$

From (5.35), it is obvious that G_m of the circuit is $4\sqrt{0.5\mu_0 C_{ox}(W/L)_{2,3}I_a}$ which can be adjusted via the bias current of I_a and also aspect ratio of transistors M_2 and M_3. Also it implies that I_a has the square root proportion with the trans-conductance gain. In order to have linearly tunable OTA, a current squaring circuit is employed in which its output will be applied as the bias current of the proposed OTA. Therefore, the next section will deal with current squaring circuit.

5.2.2.2 Current squaring circuit

The modified current squaring circuit which is based on the TL principle is shown in Figure 5.16 [70]. The MOS TL principle was stated as follows: In a loop with an even number of gate-source connections and with the same number of transistor arranged clockwise (CW) and counterclockwise (CCW), if it is assumed that all the transistors operate in saturation region then:

$$\sum_{CW}\sqrt{\frac{I_{DS}}{W/L}} = \sum_{CCW}\sqrt{\frac{I_{DS}}{W/L}} \tag{5.36}$$

Supposing transconductance parameter of all transistors are well matched, by applying (5.36) in the translinear loop composed of M_1 to M_4, we have:

$$\sqrt{I_{DS1}} + \sqrt{I_{DS2}} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} \quad \textbf{(5.37)}$$

Writing KCL at nodes C and D:

$$I_{DS3} = \frac{I_{SQ}}{4} + I_x + I_b \quad \textbf{(5.38)}$$

$$I_{DS4} = \frac{I_{SQ}}{4} - I_x + I_b \quad \textbf{(5.39)}$$

where I_b is bias current and I_x and I_{SQ} represent input and output currents respectively. Considering $I_{DS1}=I_{DS2}=I_b$, substituting (5.38) and (5.39) into (5.37) and squaring both sides twice, the output current is given by:

$$I_{SQ} = \frac{I_x^{\,2}}{I_b} \quad \textbf{(5.40)}$$

It is clearly seen that the squaring of I_x is appeared at the output. It should be pointed out that the bias current of I_b is normalized to one.

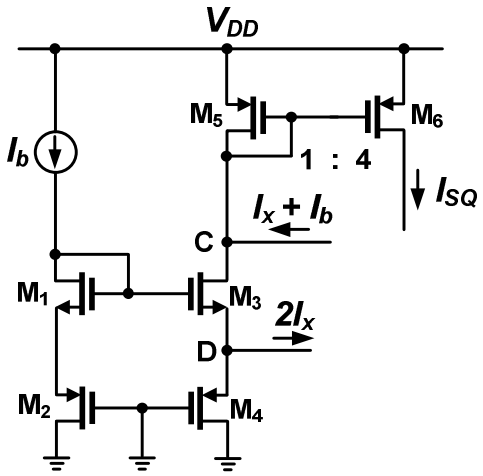


Figure 5.16 : Modified current squaring circuit.

5.2.2.3 Proposed linearly tunable OTA

The complete circuit of LTOTA is shown in Figure 5.17, where the right side (M_1-M_{18}) specifies trans-conductance circuit which its G_m can be adjusted via I_{SQ} fed to transistors M_{13} and M_{14}. Transistors M_{s1}-M_{s4} form the core of squaring circuit and M_{19}-M_{36} provide required signals in a way that M_{19}-M_{24} produce the current of $2I_x$ and M_{25}-M_{36} yield I_x+I_b. Finally, the squaring current is mirrored through M_{12}-M_{14} to the trans-conductance circuit. Considering (5.40) and (5.35) as the output of squaring and trans-conductance circuits respectively, the final output can be written as:

$$I_{out} = 4I_x\sqrt{\frac{K}{I_b}}V_{in} \qquad \textbf{(5.41)}$$

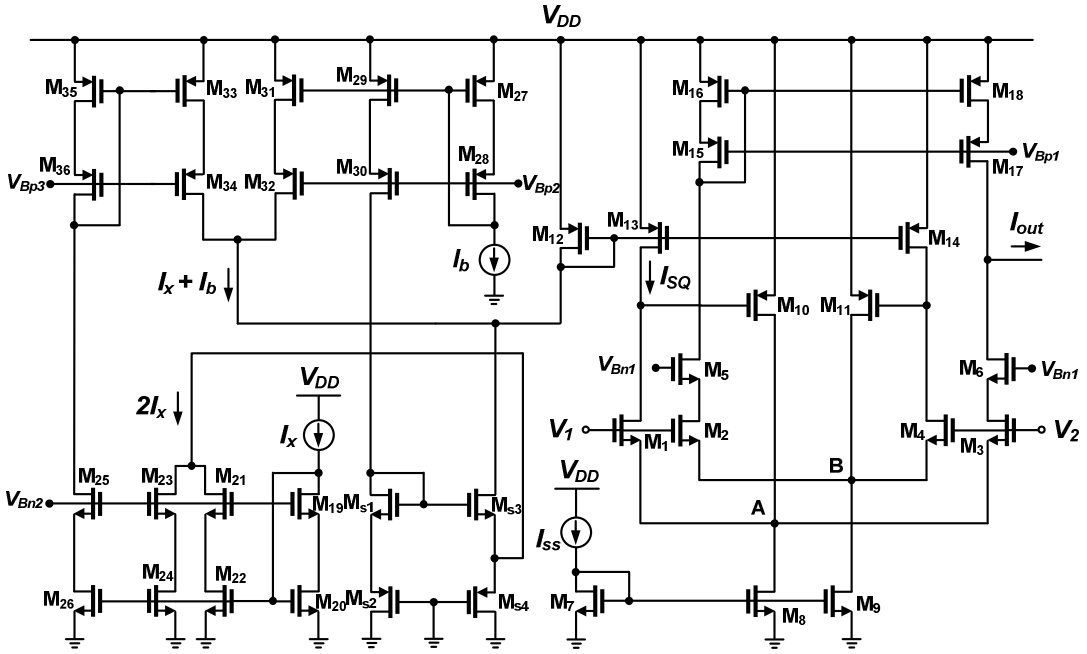


Figure 5.17 : Complete schematic of LTOTA circuit.

Equation (5.41) indicates that the trans-conductance gain can be linearly tuned by the current of I_x, while K and I_b are constant values. Take notice that this linear relationship is the same as the trans-conductance gain in the bipolar-based OTA which is very useful in many applications [142]. Since the proposed LTOTA is realized by MOS transistors all in saturation region, therefore it is very suitable and efficient for fabricating in CMOS process.

5.2.3 Performance analysis

In this section, the performance of the proposed transconductance circuit in term of the threshold voltage mismatch in the input transistors are studied. Following that, the input range of the proposed circuit is derived. Finally, the noise analysis of the circuit is carried out and the flicker and thermal noises are considered as the major noise contributors of the design.

5.2.3.1 Threshold voltage mismatch

Mismatch between transistors is one of the main sources of non-idealities in linear transconductors. This is typically due to the mismatch in threshold voltage of transistors which is mainly caused by body effect.

In an MOS transistor, body effect refers to change in the transistor threshold voltage (V_{TH}) resulting from a voltage difference between the transistor source and substrate, which can be characterized by [143]:

$$V_{TH} = V_{t0} + \gamma[\sqrt{(V_{SB} + |2\varphi_F|)} - \sqrt{|2\varphi_F|}] \quad \textbf{(5.42)}$$

where V_{t0} is the threshold voltage with zero-bias, γ is the body-effect coefficient, ϕ_F is the Fermi potential and V_{SB} is the voltage between source and bulk.

Considering the mismatch for equality of threshold voltages in pair transistors of M_1 and M_3 and also M_2 and M_4 and subsequently rewriting (5.32) and (5.33) we have:

$$I'_{DS3} = K(V_2 - V_1 + \sqrt{\frac{I_a}{K}} + V_{TH1} - V_{TH3})^2 \quad \textbf{(5.43)}$$

$$I'_{DS2} = K(V_1 - V_2 + \sqrt{\frac{I_a}{K}} + V_{TH4} - V_{TH2})^2 \quad \textbf{(5.44)}$$

Supposing V_{TH1}-V_{TH3} $=\Delta V_{T1}$ and V_{TH4}-V_{TH2} $=\Delta V_{T2}$, ignoring the terms of ΔV_{T1}^2 and ΔV_{T2}^2 (since ΔV_{T1}, $\Delta V_{T2} << 1$), the output current can be derived as:

$$I'_o = K\left[(4\sqrt{\frac{I_a}{K}} + 2\Delta V_{T1} + 2\Delta V_{T2})(V_1 - V_2) + 2\sqrt{\frac{I_a}{K}}(\Delta V_{T2} - \Delta V_{T1})\right] \quad \textbf{(5.45)}$$

From (5.45), the mismatch values are subtracted in the second term (ΔV_{T1}- ΔV_{T2}) of equation, and consequently they cancel each other or minimize the error quantity. On the other hand, considering first term of the equation, the mismatch leads to a small DC offset in the output current. This DC component can be regarded as an error in the bias input current of I_a or a DC compensated current at the output node.

5.2.3.2 Input range

The input range of transconductance circuit is restricted by the input transistors operating in saturation region. The maximum input voltage is given by the level that places M_2 at the edge of triode region, therefor it is determined by the supply voltage V_{DD}, the source to gate voltage of M_{16} in the current mirror, the $V_{DS(sat)}$ and the threshold voltage of M_2. On the other hand, a minimum allowable input range is restricted by the gate to source voltage of M_2 in the input cell and the $V_{DS(sat)}$ in the NMOS transistor of the tail-current source. Therefore the input range of the transconductance circuit can be expressed as:

$$V_{GS} + V_{DS(sat)} \le V_1, V_2 \le V_{DD} - |V_{SG}| - V_{DS(sat)} + V_{TH} \qquad \textbf{(5.46)}$$

However it is obvious that (5.46) is not satisfied on condition that the tail-current of I_{ss} is small. In such a case, the input voltage range depends on not only (5.46) but also the value of tail-current.

5.2.3.3 Noise analysis

The major noise contributors of an MOS transistor are the flicker and thermal noises, which are independent of the input terminal where the noise is referred. The flicker noise has been extensively studied because it dominates low-frequency noise and there is an increasing need to accurately design low-noise analog circuits in CMOS technology [144].

The flicker noise is modeled as a voltage source in series with the gate and roughly given by:

$$\overline{V_{n,1/f}^2} = \frac{K}{C_{ox} f W L} \qquad \textbf{(5.47)}$$

where K is a process-dependent constant on the order of 10^{-25} V^2F, Cox is the oxide capacitance and f is the frequency. Take notice that the drain noise current per unit bandwidth is obtained by multiplying the noise voltage at the gate by the transistor trans-conductance:

$$\overline{I_{n,1/f}^2} = \frac{K}{C_{ox} fWL} g_m^2 \qquad \textbf{(5.48)}$$

The derivation of thermal noise is straightforward and is due to the resistive channel of MOS transistor in the saturation region which can be modeled by a current source connected between the drain and source terminals:

$$\overline{I_{n,th}^2} = 4kT\gamma g_m \qquad \textbf{(5.49)}$$

where k is Boltzmann's constant, T is the temperature in Kelvin, and, the coefficient γ is derived to be equal to 2/3 for long channel transistors and may be needed to be replaced by a larger value for submicron MOSFETs.

Let us consider the OTA circuit shown in Figure 5.15. At relatively low frequencies, the cascade devices contribute negligible noise [145], leaving M_2, M_3, M_{16} and M_{18} as potentially significant noise sources.

In order to calculate the total output noise including thermal and flicker noises, considering (5.47)-(5.49) and the Lemma proved in [145], we have:

$$\overline{I_{n,out}^2} = \overline{I_{n,th_{M\,2,3}}^2} + \overline{I_{n,1/f_{M\,2,3}}^2} + \overline{I_{n,th_{M\,16,18}}^2} + \overline{I_{n,1/f_{M\,16,18}}^2} \qquad \textbf{(5.50)}$$

yielding:

$$\overline{I_{n,out}^2} = 4kT\left[\frac{2}{3}(g_{m2,3} + g_{m16,18})\right] + \frac{1}{C_{ox} f}\left[\frac{K_N}{(WL)_{2,3}} g_{m2,3}^2 + \frac{K_P}{(WL)_{16,18}} g_{m16,18}^2\right] \qquad \textbf{(5.51)}$$

where K_N and K_P denote the $1/f$ noise coefficients of NMOS and PMOS transistors, respectively.

Also, the total input-referred noise can be readily obtained using the following relationship:

$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{A_v^2} \tag{5.52}$$

Consider A_v=-G_mR_{out}, one can obtained G_m=$g_{m2,3}$ and also the output impedance as follows:

$$R_{out} = \left[r_{o6} + r_{o3}(1+r_{o6}g_{m6})\right] \| \left[r_{o17} + r_{o18}(1+r_{o17}g_{m17})\right] \tag{5.53}$$

Also $\overline{V_{n,out}^2}$ is given by:

$$\overline{V_{n,out}^2} = \overline{I_{n,out}^2}.R_{out}^2 \tag{5.54}$$

Replacing (5.53) and (5.54) in (5.52), after few mathematical manipulations we have:

$$\overline{V_{n,in}^2} = \frac{8kT}{3}\left[\frac{1}{g_{m2,3}} + \frac{g_{m16,18}}{g_{m2,3}^2}\right] + \frac{1}{C_{ox}f}\left[\frac{K_N}{(WL)_{2,3}} + \frac{K_P}{(WL)_{16,18}}\frac{g_{m16,18}^2}{g_{m2,3}^2}\right] \tag{5.55}$$

It is concluded that the input-referred noise decreases if the trans-conductance of input transistors M2-M3 increases. This can be done by increasing the width or drain current of corresponding transistors, however this leads to larger input capacitance and greater power dissipation respectively, and consequently reduce the speed of the circuit. Therefore, these observations point to the trade-offs between noise, power consumption and speed of the circuit.

$$I'_{DS3} = K(V_2 - V_1 + \sqrt{\frac{I_a}{K}} + V_{TH1} - V_{TH3})^2 \tag{5.56}$$

$$I'_{DS2} = K(V_1 - V_2 + \sqrt{\frac{I_a}{K}} + V_{TH4} - V_{TH2})^2 \tag{5.57}$$

Supposing yielding:

$$\overline{I_{n,out}^2} = 4kT\left[\frac{2}{3}(g_{m2,3} + g_{m16,18})\right] + \frac{1}{C_{ox}f}\left[\frac{K_N}{(WL)_{2,3}}g_{m2,3}^2 + \frac{K_P}{(WL)_{16,18}}g_{m16,18}^2\right] \tag{5.58}$$

5.2.4 Simulation results

In this section, simulation results of the proposed circuits and their applications are presented through the use of HSPICE with TSMC level 49 (BSIM3v3) parameters for 0.35 µm CMOS technology so as to verify the performance of the circuits.

Figure 5.18 illustrates the linear output current resulted from subtraction of two nonlinear input currents (I_{DS2} and I_{DS3}) which were formulated in (5.32), (5.33) and (5.35). The constant G_m in the corresponding range of the input voltage is shown in the figure as well. For this simulation, the bias current of I_a which determines the transconductance is 100 µA and the tail current of I_{ss} is set to 300 µA.

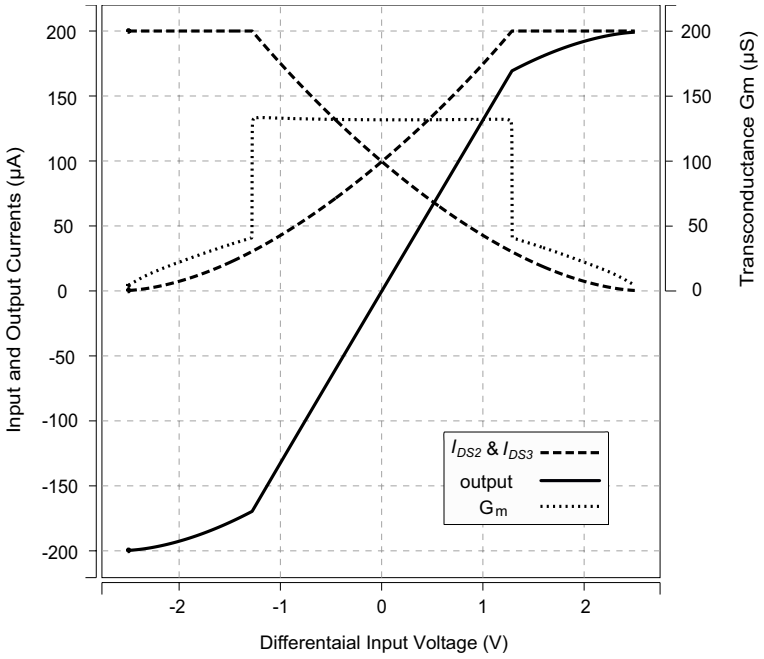
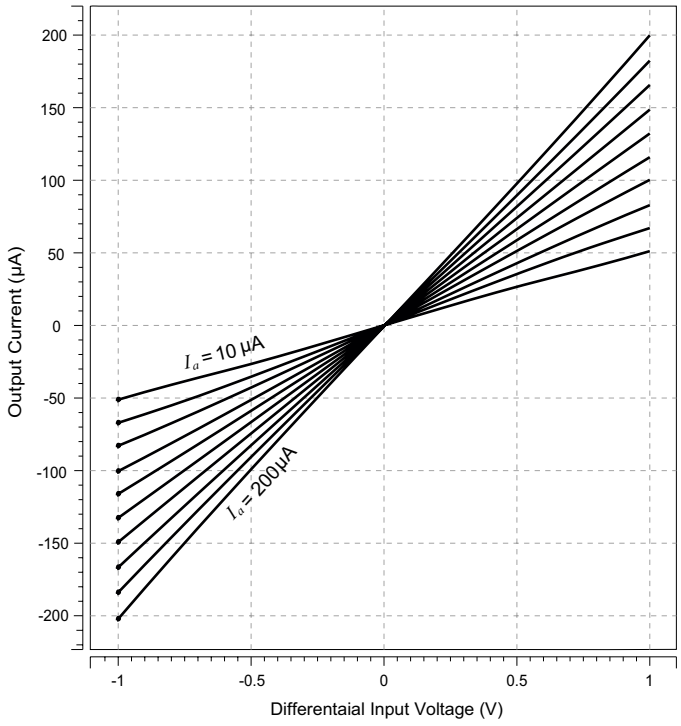
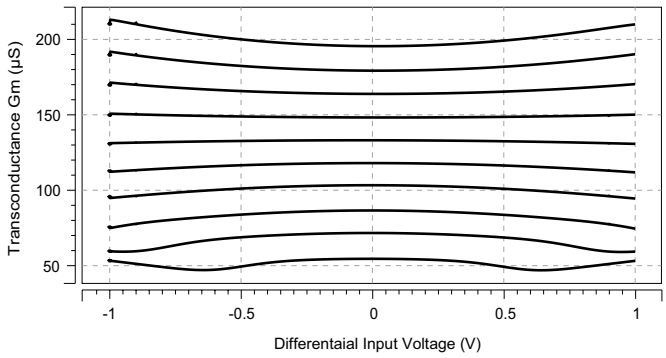


Figure 5.18 : Input and output currents along the transconductance characteristic of OTA for a typical value of parameters.

Figure 5.19(a) shows the simulated transfer characteristic of the OTA of Figure 5.15 in which I_a sweeps from 10 µA to 200 µA and I_{ss} is kept constant as 300 µA. The plots of the output current versus the differential input voltage (V_1-V_2) show that by changing the DC bias current of I_a, the OTA can linearly convert the input voltage in the range of −1 to 1V into output current with nonlinearity less than 1%. Figure 5.19(b) proves the high linearity of the OTA circuit where the constant value of transconductances are clearly shown.



(a)



(b)

Figure 5.19 : (a) The output currents of OTA when I_a sweeps from 10 μA to 200 μA (b) transconductance characteristic.

The plot of the relation between the transconductance gain and the bias current of I_a in the circuits of Figure 5.15 and 5.17 are simultaneously measured by fixing V_{in} = 100 mV and changing I_a from 0 to 100 μA where the simulated conversion error found to be 1.3%. The simulation results are shown in Figure 5.20 in which for the circuit of Figure 5.15 since $G_m = 4\sqrt{0.5\mu_0 C_{ox}(W/L)_{2,3} I_a}$, hence the trans-conductance changes with the square-root proportion of I_a, while for the LTOTA circuit because $G_m = 4I_a\sqrt{K/I_b}$, therefore G_m linearly varies by changing the bias current of I_a.

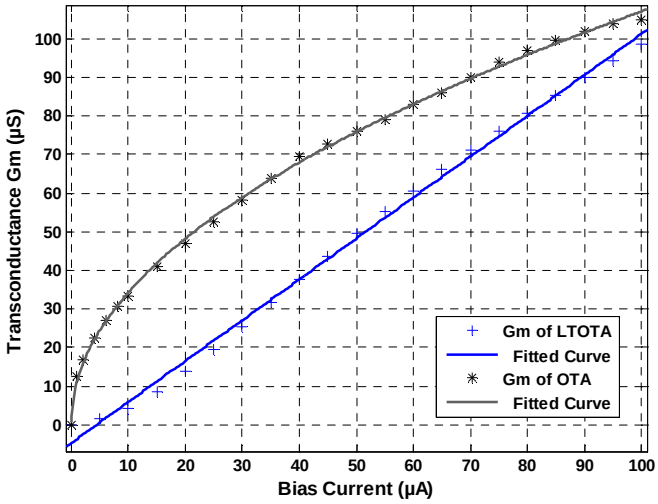


Figure 5.20 : Relation between the transconductance gain and the bias current in OTA and LTOTA circuits.

In order to demonstrate the feasibility of the designed OTA and LTOTA, they are employed in the structure of Figure 5.14 for realization of some functional circuits.

Replacing LTOTA in the structure leads to implement a multiplier/divider circuit. Since the bias current has a linear relation with G_m we have:

$$I_{out} = \frac{G_{m2}}{G_{m1}} I_{in} = \frac{I_2}{I_1} I_{in} \qquad \textbf{(5.59)}$$

Considering I_{in} and I_2 as the input currents and I_1 as the normalized current (I_{norm}), so the multiplier function is achieved. Also supposing I_2 and I_1 as the input currents namely I_{num} (numerator) and I_{den} (denominator) respectively and I_{in} as the normalized current, the output current will be proportional to I_{num}/I_{den}. Thus the structure performs as a divider circuit.

Figure 5.21 shows how the structure works as a multiplier circuit and can be employed as a balance modulator. In this simulation, two sinusoidal inputs in the form of I_1= 10 $\sin(2\pi 10^6 t)$ µA, I_2= 5 µA + 5$\sin(2\pi 10^5 t)$ µA are applied to the structure and I_{norm} is kept constant as a normalized value (10µA). The output signal as well as the error measurement are shown in the figure. This result confirms that the circuit can precisely modulate two different input currents.

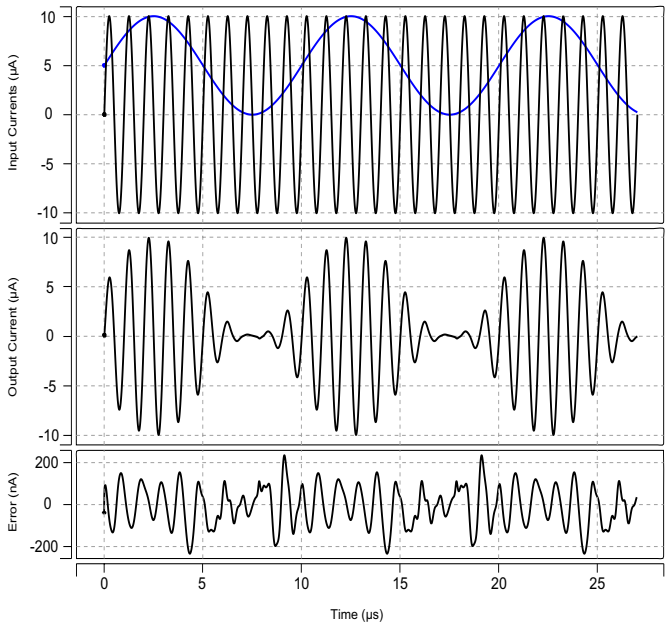


Figure 5.21 : The structure is used as an amplitude modulator. 1 MHz carrier sinusoid and 100 kHz modulating signal (upper waveform); AC modulated output (middle waveform); Error measurement (lower waveform).

The DC transfer characteristics of the multiplier circuit are shown in Figure 5.22 which obtained by variation of I_1 from 0 to 10µA and I_2 from -10µA to 10µA with 2µA per step and setting I_{norm}=10µA. The comparison of simulated and expected results implies that the circuit works well over the mentioned range.

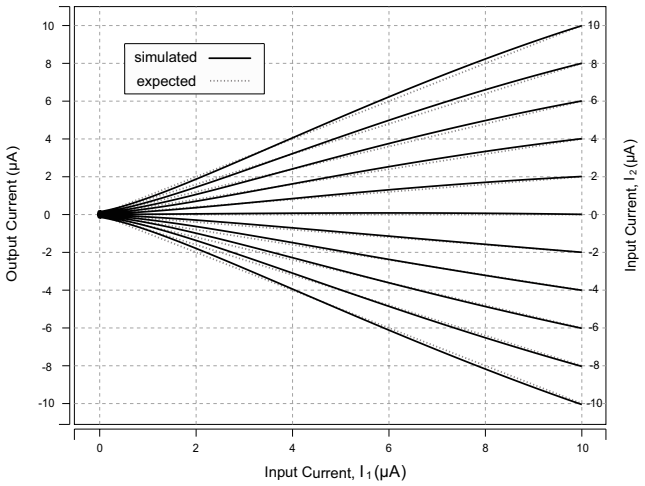


Figure 5.22 : DC transfer characteristic of multiplier circuit.

The simulation result of the structure when it employs as a divider circuit is depicted in Figure 5.23. The characteristic between I_{out} and denominator current (I_{den}) for swept currents of numerator (I_{num}) between -4.5µA and -4.5µA with 0.5µA per step isplotted while I_{norm} is set to 10µA. In this case, the circuit satisfies the following relationship:

$$I_{out} = \frac{I_{num}}{I_{den}} I_{norm} \tag{5.60}$$

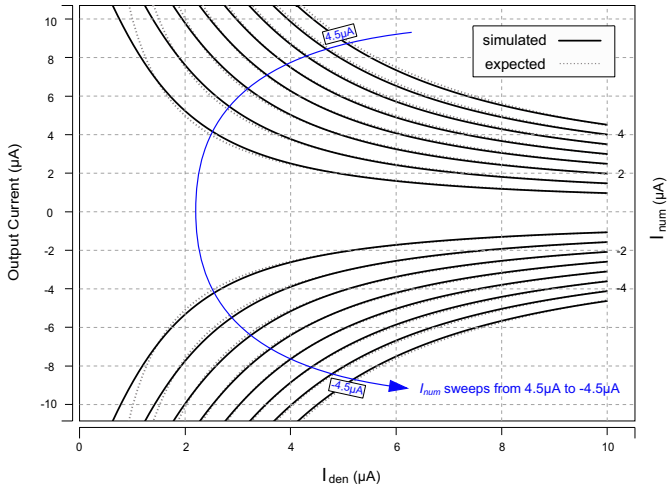


Figure 5.23 : Simulated DC transfer characteristic of the divider circuit.

In the case that I_{in} and I_2 are equal and I_1 being considered as a normalized current, a squaring function will be readily realized. The output current is given by:

$$I_{out} = \frac{I_{in}^{\ 2}}{I_{norm}} \tag{5.61}$$

By applying a triangle waveform with the frequency of 100kHz to the input, the squaring function as well as the error value are appeared at the output (see Figure 5.24). It can be clearly seen that the simulated result is in a close agreement with the expected output, and the maximum error is 173nA.

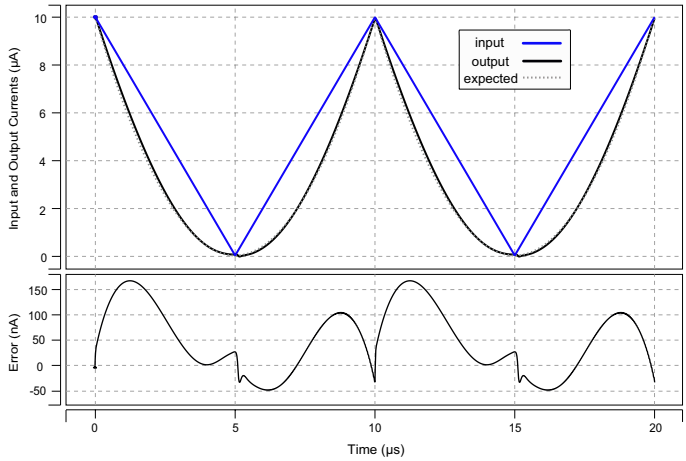


Figure 5.24 : Simulated transient response of the squaring circuit and its error.

Let us consider the structure of Figure 5.14. Replacing the OTA of Figure 5.15 in this structure, one can find the output current as:

$$I_{out} = \sqrt{\frac{I_2}{I_1}} I_{in} \tag{5.62}$$

In the case that $I_1 = I_{in}$, we have:

$$I_{out} = \sqrt{I_1 I_2} \tag{5.63}$$

Considering I_1 as the input current, by applying I_2=10µA as a normalize current the square-rooter function is implemented. To prove the efficiency of the circuit, a triangle waveform similar to the squaring circuit is applied; then the output current is achieved as shown in Figure 5.25.

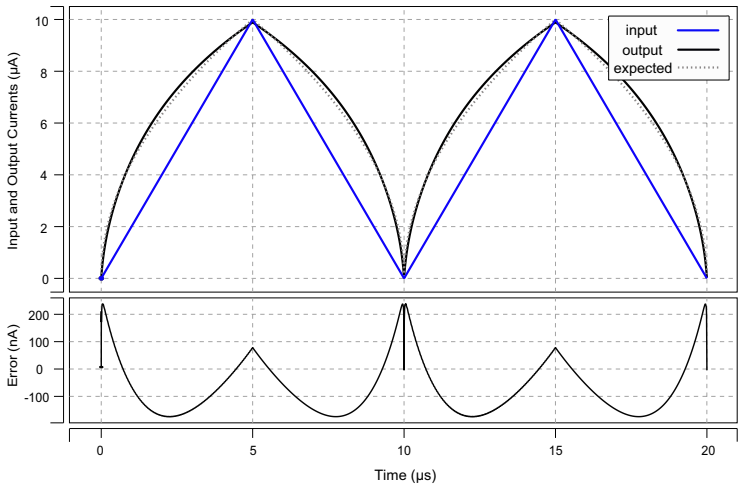


Figure 5.25 : Simulated transient response of the square-rooting circuit and its error.

In order to evaluate the robustness of the OTA circuit against the process variation, the Monte Carlo analysis with 100 iterations is carried out by applying ±5 % Gaussian distribution at $\pm 3\sigma$ level in the variation of all transistors threshold voltage and aspect ratio simultaneously.

In this analysis, similar conditions of simulation in Figure 5.18 is applied and then the transconductance G_m is considered as a parameter which can be affected by the conceivable mismatch under the mentioned conditions. The transconductance gain without any mismatch was obtained 130 µS in Figure 5.18, while the Monte Carlo

analysis in Figure 5.26 demonstrates that 87% of total samples occurs with the error of less than ±1% for threshold voltage and transistors aspect ratio variations.

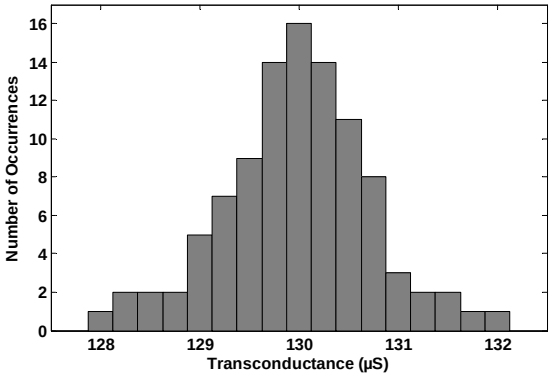
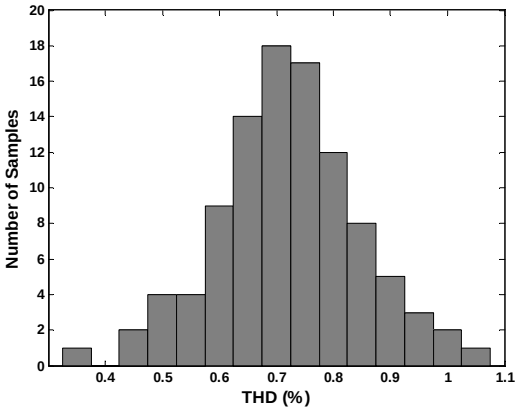
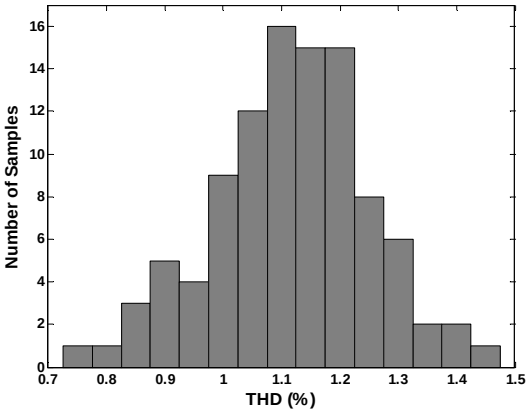


Figure 5.26 : Transconductance variations from Monte Carlo simulations for mismatch in threshold voltage and transistors aspect ratio.



(a)



(b)

Figure 5.27 : Monte Carlo results by applying threshold voltage mismatch for (a) OTA circuit and (b) LTOTA circuit for 2.0 Vp-p 1 MHz sine wave.

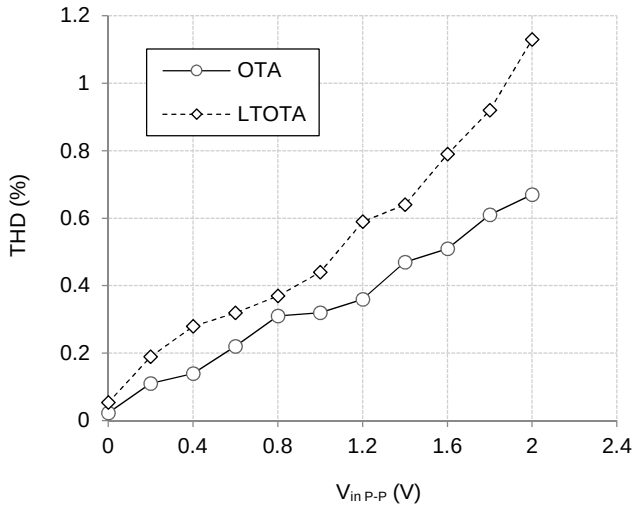


Figure 5.28 : Relation between THD and input voltage.

The Monte Carlo analysis for THD is shown in Figure 5.27. The same conditions and distribution of simulations in Figure 5.26 are applied for both of OTA and LTOTA circuits. The results show that most of the samples occur in the ranges of 0.6-0.8 % and 1.0-1.2 % for OTA and LTOTA circuits respectively. Also, the THD versus different values of input voltages at 1 MHz for both of the circuits are simultaneously shown in Figure 5.28. In this simulation, the bias current is set to 50µA and the tail current is equal to 200µA. In the worst case, an input signal of 2 V_{p-p} resulted in a THD of 0.67% and 1.13% for the proposed circuits.

A 2V_{p-p} step waveform is applied to unity-gain closed loop OTA whose response is shown in Figure 5.29. The currents of I_{ss} and I_a are set to typical values of 400µA and 150 µA respectively, and the output load is considered a capacitance with 10 pF capacity. Measuring the slope of output response gives its both positive and negative slew rate as 5.7 v/µs.

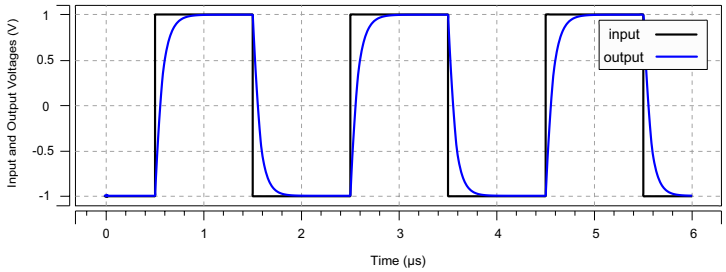


Figure 5.29 : Step response of the OTA for slew rate simulation.

5.2.5 Conclusion

The applicability of a new LTOTA as a basic building block for realization of computational circuits was investigated in this section. The proposed transconductance amplifier provided a constant G_m over a wide range of input voltage which allowed the implementation of high precision computational circuits. The implemented circuits were included squarer, square-rooter, multiplication and division operations. Due to the simple and compact structure, the power consumption of the implemented circuits were comparatively low. As we discussed in the introduction section, the analog realization of fuzzy circuits occupies lower area and consumes less power than digital ones. Table 5.3 compares the parameters of digital and analog realizations.

Table 5.3 : Comparative parameters of the proposed analog multiplier/divider with digital ones.

	[146]	[147]	[148]	[148]	[149]	This work
Power cons. (mW)	5.8	1.48	9.619	2.445	2.99	0.521
Power supply (V)	5	0.5	1.8	1.8	1.8	3.3
Array	4×4	8×8	16×16	8×8	8×8	Continuous
Tech. (μm)	1.2	0.13	0.18	0.18	0.18	0.35
Area (mm^2)	1.35	0.07	0.372	0.094	0.14	0.016
Sim. or Meas.	Meas.	Meas.	Post Layout	Post Layout.	Sim.	Post Layout

6. IMPLEMENTATION OF IT2FLC

This chapter deals with the hardware realization of IT2FLC in current-mode. The complete schematic of the proposed controller is shown in Figure 6.1 in which two inputs of I_{in1} and I_{in1} are applied to the controller and one output (I_{out}) is resulted at the output. The fuzzifier block consists of six type-2 membership function circuit (T2-MFC) and each one is constructed from UMF and LMF. Figure 6.2 shows the typical membership functions applied to the controller. For each input two diamond-shaped membership functions and one triangular membership function are considered with different slops, upper and lower modal points.

6.1 Implementation of Rule Base

As discussed before, the consequent of a rule in TSK type-2 FLC is a function of its inputs. For a first order TSK type-2 FLC, the consequent is a linear function of inputs as follows:

$$\textit{Rule } l^{th} : \textbf{IF } x_1 \textit{ is } \tilde{A}_1^l \textit{ and } \ldots \textit{ and } x_p \textit{ is } \tilde{A}_p^l \textbf{ Then } y^l = a_{1l}\, x_1 + \ldots + a_{pl} x_p + a_{0l} \qquad \textbf{(6.1)}$$

Considering two-input one-output FLC, the current-domain representation of this expression can be written as:

$$\textit{Rule } l^{th} : \textbf{IF } I_{x1} \textit{ is } \tilde{A}_1^l \textit{ and } I_{x2} \textit{ is } \tilde{A}_2^l \textbf{ Then } I_{yl} = a_{1l}\, I_{x1} + a_{2l} I_{x2} + a_{0l}\, I_{Norm} \qquad \textbf{(6.2)}$$

where I_{x1} and I_{x2} are the inputs, $\tilde{A}_1^l$ and $\tilde{A}_2^l$ are input fuzzy sets, I_{yl} is the output, and "a_{1l}", "a_{2l}" and "a_{0l}" are constants. It should be pointed out that in order to make the rule consequents programmable, an architecture must be designed in such a way that they can be defined and changed in different applications. This can be easily done using current mirrors with selectable gains. These constants can be programmed with a resolution of 4-bits as shown in Figure 6.3. Take notice that coefficient "c" determines a constant bias current in the rule consequent (singleton) and is constructed from I_{Norm}.

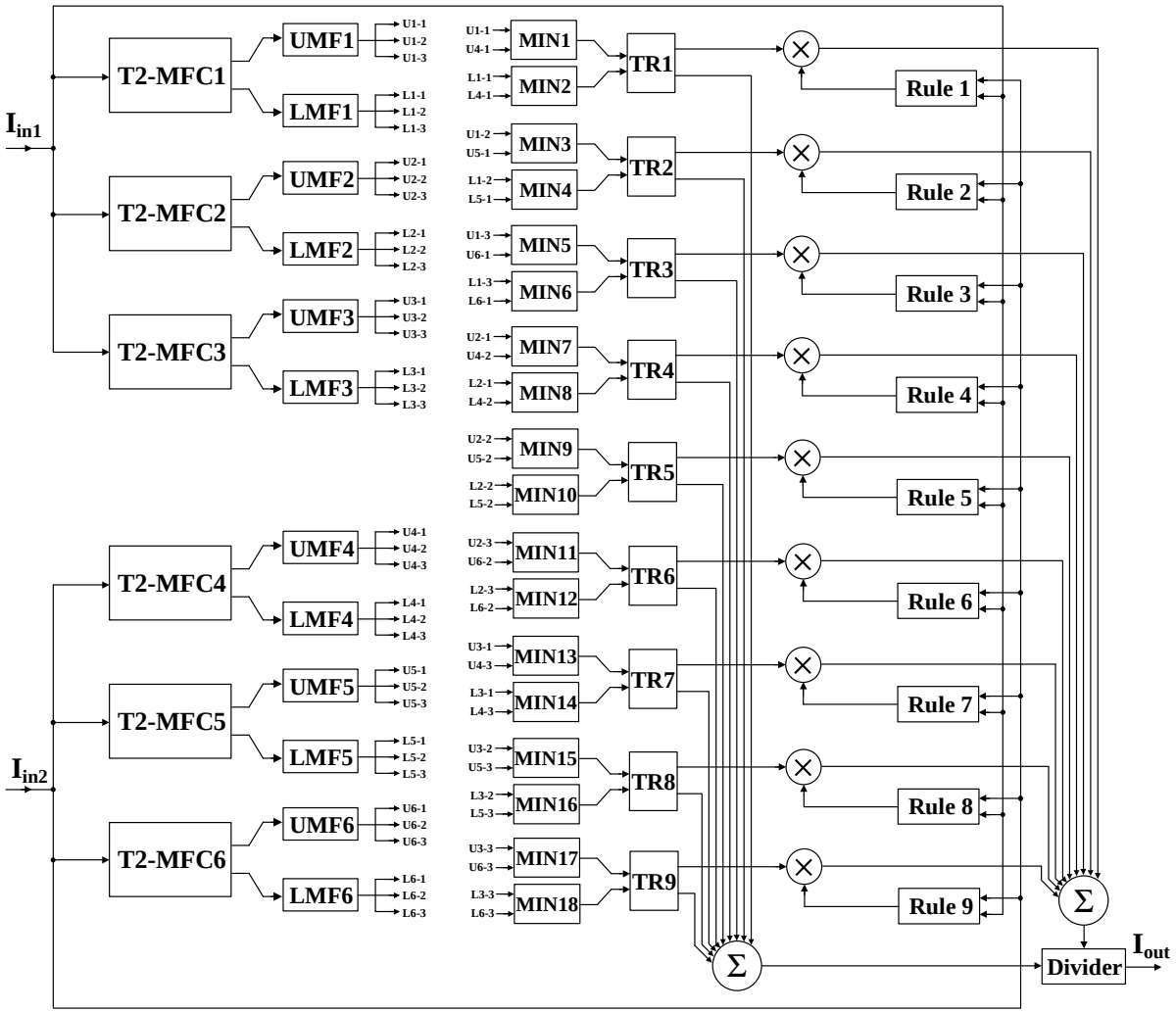


Figure 6.1 : Complete block diagram of proposed IT2FLC.

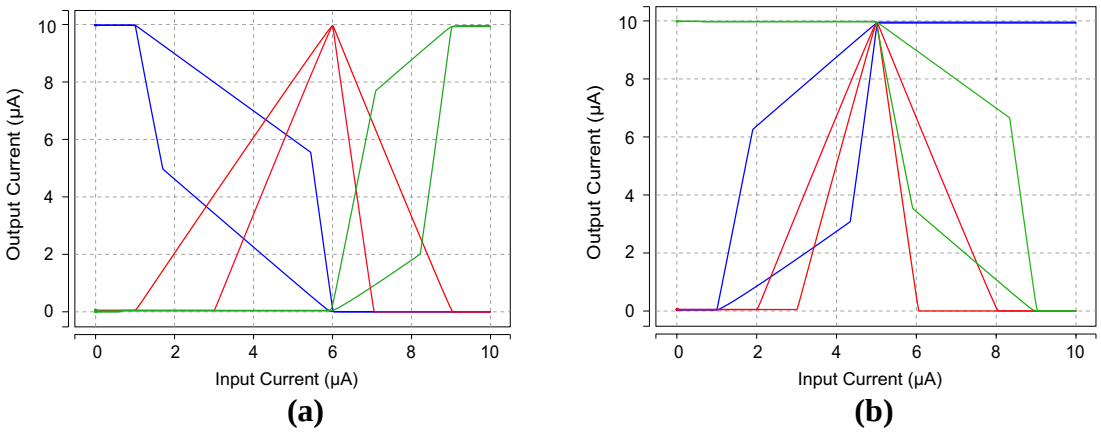


Figure 6.2 : Input membership functions (a) first input (b) second input.

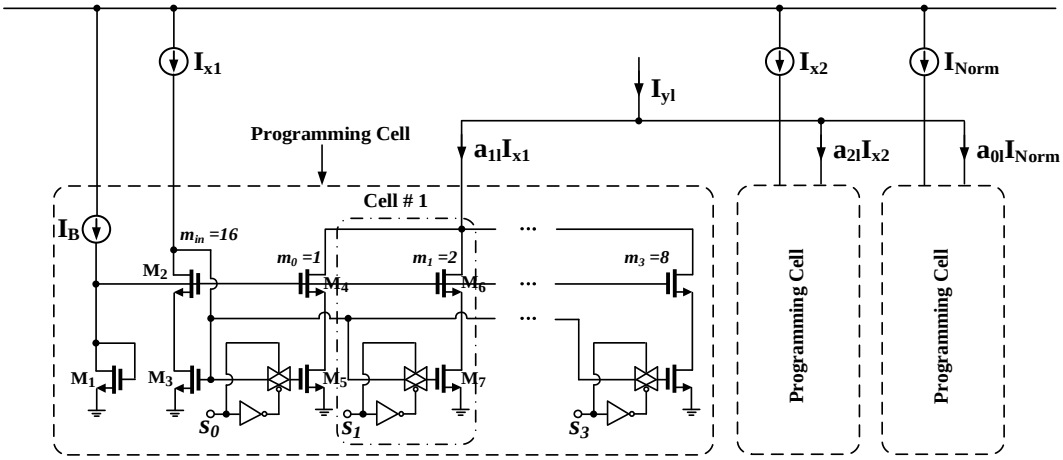


Figure 6.3 : Programmable implementation of rule base.

6.2 Inference Engine

As stated in chapter 4, the minimum operator is used for deriving activation levels (firing values) of rules which construct the main part of inference engine. This operator is implemented using loser-take-all circuit presented in section 4.3. The minimized values are duplicated using simple current mirrors and then transferred to the output processor which consists of type reduction and defuzzification blocks.

6.3 Type Reduction Circuit

The type-reducer generates a type-1 fuzzy set output, which is then converted in a crisp output through the defuzzifier. As discussed in section 2.5.2.5, there are different methods for type reduction and since the NT method has the precise computation and also benefits from simple and intuitive configuration, then it is preferred to another

methods. It is based on taking average of the lower and upper MFs of the interval set. The NT type reduction relation in current-domain can be written as:

$$I_{\mu_{TR}} = \frac{1}{2}\left(I_{\bar{\mu}(x_i)} + I_{\underline{\mu}(x_i)}\right) \tag{6.3}$$

where $I_{\bar{\mu}(x_i)}$ and $I_{\underline{\mu}(x_i)}$ are the membership grades of the upper and the lower membership functions respectively. As shown in Figure 6.4, the implementation of NT method is simple and easy to understand. It is realized using current mirrors with suitable dimensions.

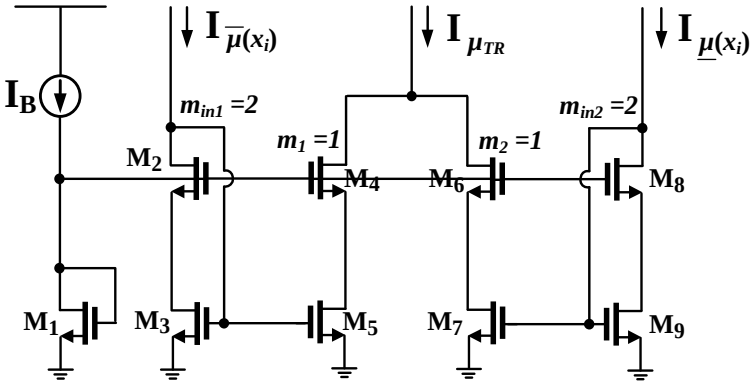


Figure 6.4 : Circuit realization of Nie-Tan type reduction.

6.4 Defuzzification

Since COG is one of the most popular methods for defuzzification process due to the simple realization and institutive configuration, then we implement this method using the designed multiplier and divider circuits presented in section 5.1 and 5.2, respectively. As mentioned before the current-mode expression of COG method can be written as:

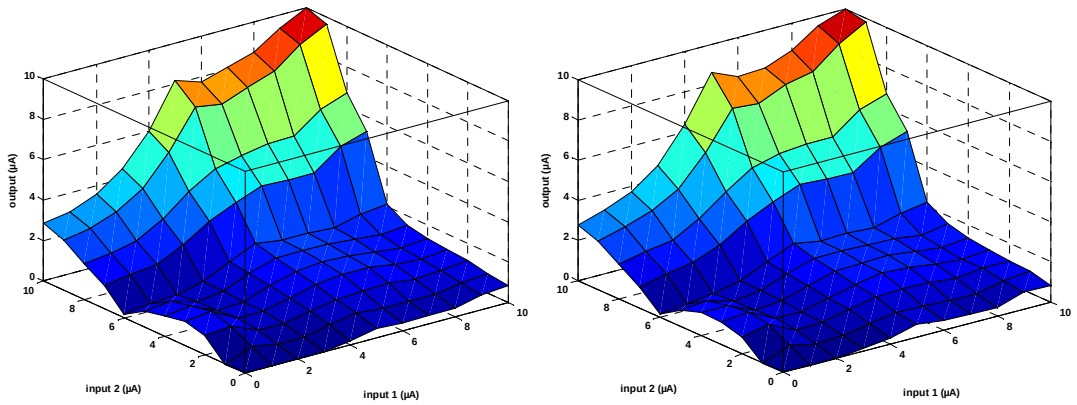
$$I_{COG} = \frac{\sum_{i=1}^{n} I_{x_i} I_{\mu_A(x_i)}}{\sum_{i=1}^{n} I_{\mu_A(x_i)}} \tag{6.4}$$

According to the schematic of Figure 6.1, the multiplier circuits accept the inputs from rule base and type reduction blocks. The summation of all multiplications construct the numerator of (6.4).

The denominator is obtained by simple wiring of all type reduction values to a single node (summation). Numerator and denominator are applied to the divider circuit and ultimately the crisp value is appeared at the output.

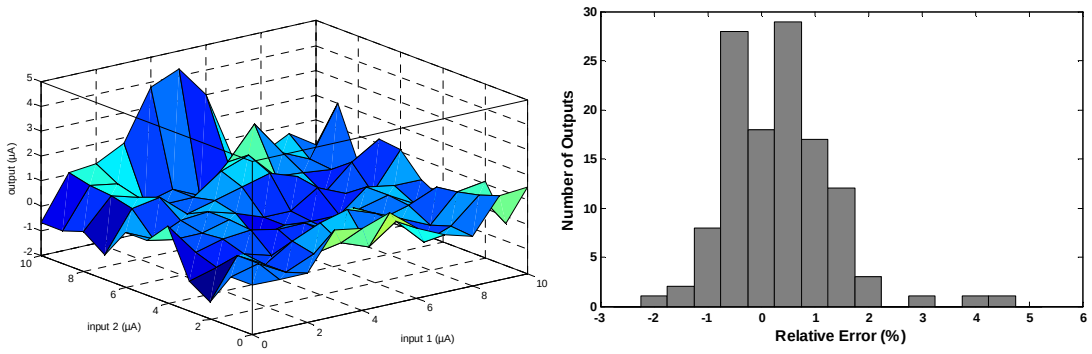
6.5 Simulation Result

In order to verify the performance of the controller, layout of the controller is drawn by Cadence virtuso, and then post layout simulation results are presented using HSPICE and level 49 parameters (BSIM3v3) in 0.35 µm technology. The resulted output surface for 100 sample inputs is shown in Figure 6.5(a) while the expected output surface demonstrated in Figure 6.5(b). Figure 6.6(a) shows the percentage of error versus the applied inputs where the RMS error between two surfaces is 1.6%. In addition, Figure 6.6(b) indicates the number of total 100 outputs versus the relative errors. The average power consumption is found to be 25.7 mW with a power supply of 3.3V. It should be pointed out that the maximum power consumption depends on the programming parameters and can vary by a fraction for different settings.



(a) **(b)**

Figure 6.5 : Output surface of the Type-2 controller (a) Simulated results (b) expected outputs.



(a) **(b)**

Figure 6.6 : Relative error of Type-2 FLC versus (a) applied inputs (b) number of the output.

To ensure the robustness of the controller against the process variation, the Monte Carlo analysis with 100 iterations is performed by applying mismatch in transistors aspect ratio and threshold voltage. According to Figure 6.7 90% of the total samples occurred with the relative error of less than ±1%.

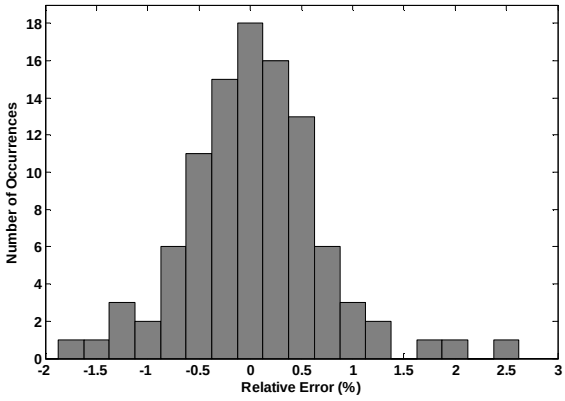


Figure 6.7 : The result of Monte Carlo analysis of controller for mismatch in threshold voltage and transistors aspect ratio.

In order to examine speed of the circuit, a square pulse is applied to the input. Figure 6.8 shows the applied pulse as well as the response of the controller, while the first input (I_{in1}) is a square pulse with 10 μA peak gain and the second input (I_{in2}) remains constant.

The total average delay (t_{rise}+ t_{fall}/2) is around 170 ns (@C_L=5pF) which corresponds to 5.88 MFLIPS (mega fuzzy logic inferences per second).

As we discussed in the introduction section, the analog realization of fuzzy circuits occupies lower area and consumes less power than digital ones. Table 6.1 compares the parameters of digital and analog realizations.

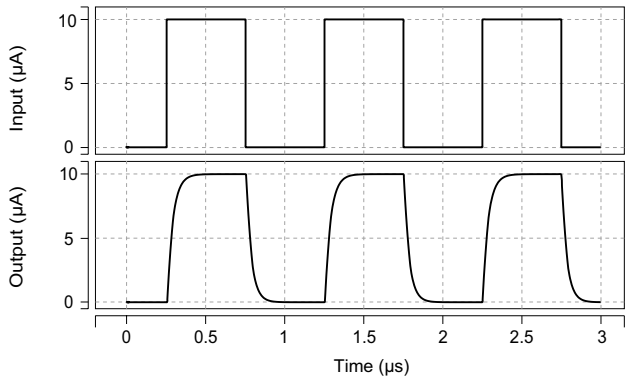
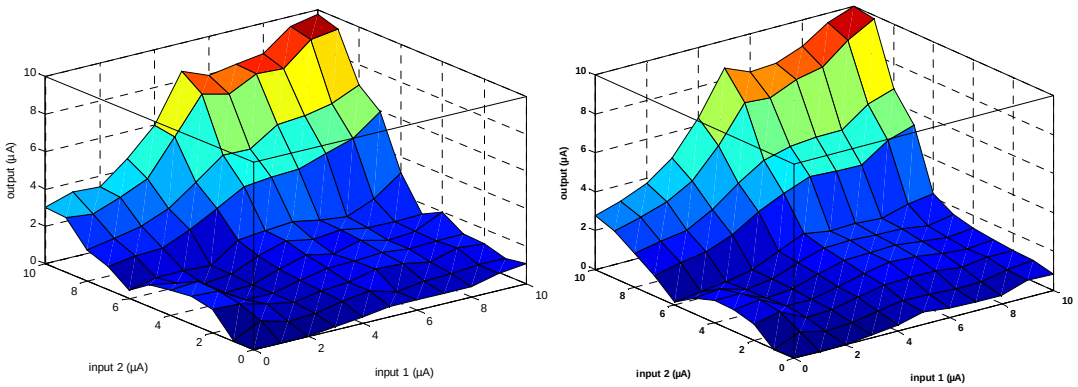


Figure 6.8 : Input pulse of the IT2FLC and response of the controller.

Table 6.1 : Comparison of analog and digital realizations of FLC.

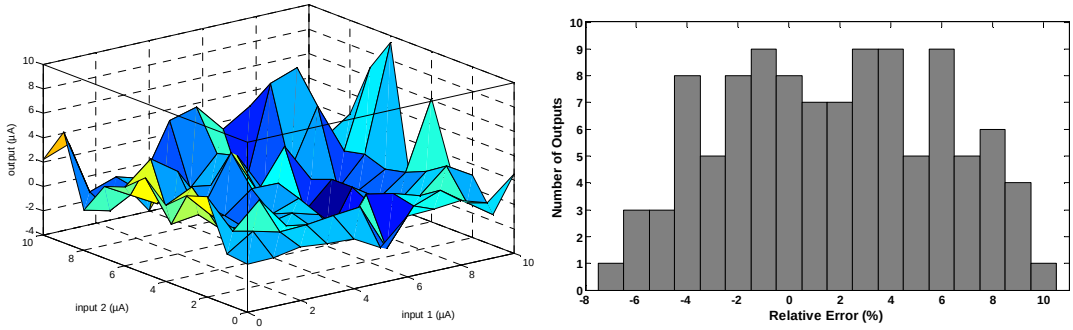
	[150]	[151]	[152]	[153]	This Work
Analog (A) / Digital (D)	D	D	D	D	A
Speed (MFLIPS)	0.25	2.85	8.85	3.61	5.88
FLC type	Type-1	Type-1	Type-1	Type-1	Type-2
Power supply (V)	3.3	N/A	3.3	3.3	3.3
Power consumption (mW)	142	120	49	104	25.7
Area (mm^2)	70	12.3	0.11	0.54	0.09
Technology (μm)	1	1	0.35	0.35	0.35

Also, as mentioned in section 2, because of the flexibility of membership functions in Type-2 FLC in comparison with Type-1 one, higher accuracy is achieved in Type-2 FLC. In order to compare the precision of two FLCs, the outputs of Type-1 and Type-2 FLCs are compared. Figure 6.9 shows the corresponding surface of Type-1 FLC which is realized using the same circuits of Type-2 FLC. The resulted error for Type-1 FLC is demonstrated in Figure 6.10 where the RMS value is obtained 3.47%. Considering 1.6% of error in Type-2 FLC, precise performance of that controller is proved. This is due to the fact that the membership functions in Type-1 FLC have unique value for each point, however, in Type-2 ones the footprint of uncertainty associates with the membership function which consists of LMF and UMF for each point. Consequently, the input membership functions track the target surface having more flexibility in comparison with Type-1 membership functions.



(a) **(b)**

Figure 6.9 : Output surface of the Type-1 controller (a) Simulated results (b) expected outputs.

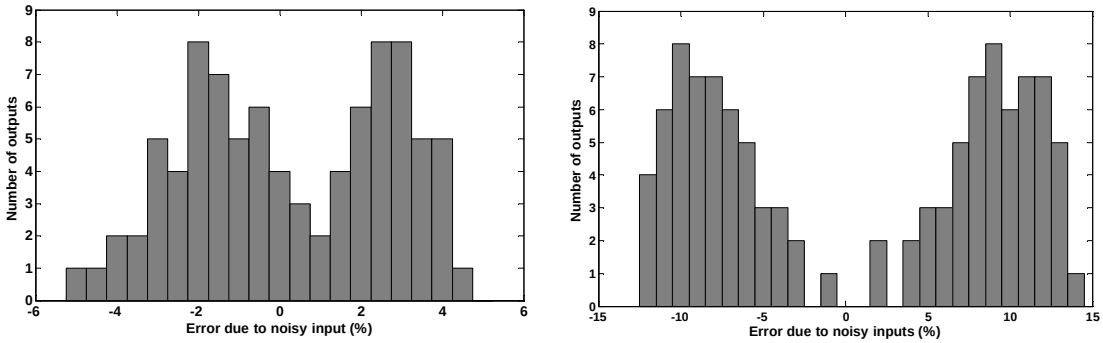


(a) **(b)**

Figure 6.10 : Relative error of Type-1 FLC versus (a) applied inputs (b) number of the output.

Additionally, as mentioned in section 3, the noise reduction property of DT2MF in the presence of noisy inputs was discussed and the advantages of this kind of MF was shown. Applying noisy inputs to the fuzzifier block affect the membership functions of the FLC, which in turn change the rule-base of the controller. In these conditions, the output of the FLC will change as well. However, in Type-2 FLC because of employing DT2MF the effect of noise is comparatively low rather than that in Type-1 FLC. Figure 6.11 shows the output error of both FLCs in the presence of noisy inputs in which are 3.47% and 8.65% for Type-2 and Type-1 FLCs, respectively. Table 6.2 compares the performance of Type-1 and Type-2 FLCs in which the Type-1 uses four different shapes of membership functions while Type-2 FLC employs only one membership function (DT2MF). In addition, power supply and technology of both controllers are the same. It should be pointed out that because of the simple structure

of Type-1 FLC in comparison with Type-2 one (as discussed in section 2), the power consumption as well as the speed of type-1 FLC are better than Type-2 one.



(a) **(b)**

Figure 6.11 : Error of the controller (a) Type-2 FLC (b) Type-1 FLC.

Table 6.2 : Comparison of Type-1 and Type-2 FLCs.

	Type-1 FLC	Type-2 FLC
Speed	6.4 MFLIPS @ 5 pF	5.88 MFLIPS @ 5 pF
Error	3.47 %	1.6 %
Error (noisy input)	8.65 %	2.14 %
Design complexity	2-inputs, 1-output, 9-rules	2-inputs, 1-output, 9-rules
Used MFs	S, Z, Trapezoidal, Triangular	Diamond
Power supply	3.3 V	3.3 V
Power consumption	15.3 mW	25.7 mW
Technology	0.35 µm	0.35 µm

7. CONCLUSION

7.1 Summary of the Work

Fuzzy hardware developments have been a major force driving the applications of fuzzy set theory and fuzzy logic in both science and engineering. The fuzzy boom in Japan, as well as in other parts of the world, has generated a host of products and techniques demonstrating superior performance to conventional products.

In order to utilize fuzzy logic in engineering applications, fuzzy logic controllers have been presented and implemented. Although many research have been made in implementing T1FLC, unfortunately there are limited number of works in the field of T2FLC, while they suffer from lack of sufficient circuits to realize this purpose. Therefore, we focused on this subject as the essential part of developing fuzzy hardware in the engineering applications.

New high-performance circuits for IT2FLC were presented in this dissertation. The current-mode approach was employed owing to the simple circuitry and intuitive configuration to design the circuits. Designing of mixed analog/digital circuits provided a flexible configuration as well as the highly accurate performance, where analog circuits were employed to realize required functions, while the programmable units implemented using digital circuits.

In this regard, design and implementation of a DT2MF was fully described for a first time. We investigated the programmability of the circuit in terms of slopes, upper and lower modal points. This feature enabled the expert of the system to create other shapes of type-2 membership functions including rectangular, rhombus, triangular and trapezoidal. Furthermore, Monte Carlo analysis was carried out to ensure the robustness of the circuit performance against the process variation. To estimate the power consumption, it was measured for a typical DT2MF in which the average power consumption was 688 μW.

Moreover, design of a current-mode loser-take-all circuit was presented to construct the fuzzy inference engine. The proposed circuit consisted of a basic cell which

allowed implementation of a multi-input configuration by repeating the cell for each additional input. A high-speed feedback structure was employed to determine the minimum current among the applied inputs. High accuracy as well as high speed operation were achieved owing to the usage of feedback structure. To increase the input range of LTA, it was required to increase the bias current, while the circuit dissipated more power. In view of this, as a further work low-voltage low-power methods such as level shifting techniques can be proposed.

A new CMOS four-quadrant analog multiplier circuit was proposed based on a pair of dual-translinear loops. The significant features of the circuit were its high accuracy and high linearity, owing to the fact that the circuit relied on a new dual-translinear topology. Additionally, the applicability of a new LTOTA as a basic building block for implementation of fuzzy related circuits was introduced. The proposed transconductance amplifier provided a constant G_m over a wide range of input voltage which allowed the implementation of high precision computational circuits. The proposed LTOTA behaved as a bipolar OTA in which its transconductance was linearly tuned by the bias current, therefore all of the bipolar based OTA configurations could be easily replaced by the CMOS LTOTA.

Finally, designed circuit were employed to realize IT2FLC. Mixed analog/digital realization of the controller made the design programmable and extendable. Simulation results of the controller were presented using HSPICE and level 49 parameters (BSIM3v3) in 0.35 µm technology. In order to compare the simulation results of the controller with ideal functionality, the controller was adjusted with a particular set of parameters. The simulation results were compared with the ideal results to prove the efficiency of the designed IT2FLC. Moreover, the result of proposed controller were compared with a realized Type-1 FLC using the same circuits in which it demonstrated better performance of Type-2 FLC in terms of accuracy and immunity in the presence of noisy inputs.

7.2 Scope of Future Works

Some points are suggested as future works which can be probably improve the performance of the designed circuits and implemented IT2FLC. A Mamdani type of the controller can be proposed, but in this case more complicated circuits will be required, consequently the power consumption increase as well. Therefor more simple

circuits as well as the low voltage / low power circuits can be designed to reduce the power dissipation of the IT2FLC.

Although the mixed-signal realization is preferable as discussed in detail in section 2.6.3, but digital realization of IT2FLC can be proposed to improve the precision of the circuit. Moreover, digital circuits have better performance against the noise contributors. The drawback of digital realization originates from using high number of transistors to accomplish the same tasks of analog circuits. This leads to the circuits which consume more power, thus low power digital circuits can be designed to deal with power dissipation.

In recent years, importance of membership functions encourage the fuzzy researchers to propose new shapes, because they have a dominant effect on the reasoning process of a FLC rather than number of rules or inference mechanism. Therefore, any possible new functions is always an opportunity for circuit designers to realize them in order to improve the performance of the controllers. This is exactly what we carried out regarding DT2MF, Which requires to be up-to-date with fuzzy published articles.

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