# SUB-TERAHERTZ AND RFIC IMPLEMENTATIONS: DC-300 GHZ SOI SWITCH AND HIGHLY EFFICIENT SIGE BICMOS PAS

by
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**SUB-TERAHERTZ AND RFIC IMPLEMENTATIONS: DC-300 GHZ SOI SWITCH AND HIGHLY EFFICIENT SIGE BICMOS PAS**

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# ABSTRACT

SUB-TERAHERTZ AND RFIC IMPLEMENTATIONS: DC-300 GHZ SOI SWITCH AND HIGHLY EFFICIENT SIGE BICMOS PAS

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Keywords: wideband, efficiency, PA, switch, millimeter-wave

Driven by the accelerating demands of high-throughput wireless communication, autonomous systems, and compact radar platforms, radio frequency (RF) and millimeter-wave circuit design is undergoing a decisive shift toward higher frequencies. As systems transition beyond the conventional microwave spectrum into the D-band (110–170 GHz) and beyond, the development of wideband, power-efficient, and compact circuit blocks becomes essential. Applications such as 100 Gb/s backhaul links for 5G/6G networks, short-range radar for robotics and automotive sensing, and gesture-controlled wearable electronics require highly integrated, broadband transceiver front-ends capable of operating deep into the millimeter-wave regime. This thesis addresses these emerging challenges through the design and implementation of core RF/millimeter-wave front-end components. First, a high-efficiency, small-area power amplifier with a modeling approach using IHP 0.13 $\mu$m SiGe BiCMOS technology is presented, which is suitable for compact transceiver, radar, or sensor applications. Secondly, power combined PAs consisting of 2-way and 4-way power combination at 160 GHz are presented to offer a less efficient, larger area; however, a larger output version is given for reaching further distances for the systems. Finally, a DC-300 GHz switch was provided, enabling multi-band operation, therefore allowing for access to the advantages of both lower frequency bands and higher frequency bands. Each block's design and implementation methodology is showcased and compared with the current state-of-the-art, achieving a performance comparable to or better than the current state-of-the-art.

# ÖZET

TERAHERTZ ALTI VE RADYO FREKANS ENTEGRE DEVRE İMPLEMENTASYONLARI: DC-300 GHZ SOI ANAHTAR VE YÜKSEK VERİMLİ SIGE BICMOS GÜÇ AMPLİFİKATÖRLERİ

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Anahtar Kelimeler: genişbant, verimlilik, güç amplifikatörü, anahtar, milimetredalga

Yüksek veri aktarım kapasiteli kablosuz iletişim, otonom sistemler ve kompakt radar platformlarına artan talep, RF ve milimetre dalga devre tasarımını daha yüksek frekanslara taşımaktadır. Sistemler, mikrodalga spektrumunun ötesine geçerek D-bandı (110–170 GHz) ve ötesine yönelirken, geniş bantlı, verimli ve kompakt devre bloklarının geliştirilmesi kritik hâle gelmiştir. 5G/6G için 100 Gb/s üzeri backhaul bağlantılar, kısa menzilli radarlar ve giyilebilir elektronikler gibi uygulamalar, milimetre dalga frekanslarında çalışan, yüksek derecede entegre ve geniş bantlı alıcı-verici ön uçları gerektirmektedir. Bu tez, bu zorluklara RF/milimetre dalga ön uç bileşenlerinin tasarımı ve gerçekleştirilmesiyle yanıt vermektedir. İlk olarak, IHP 0.13 µm SiGe BiCMOS teknolojisi kullanılarak kompakt alıcı-verici/radar/sensör uygulamalarına uygun, yüksek verimli ve küçük alan kaplayan bir güç amplifikatörü sunulmaktadır. İkinci olarak, 160 GHz'de çalışan 2-yollu ve 4-yollu güç birleştirmeli PAlar tanıtılmakta; daha düşük verimliliklerine rağmen daha yüksek çıkış gücü ile daha uzak mesafelere erişim sağlamaktadır. Son olarak, DC–300 GHz aralığında çalışan bir anahtar devresi ile çok bantlı çalışma imkânı sunulmakta, böylece hem düşük hem de yüksek frekans bantlarının avantajlarına erişim mümkün olmaktadır. Her bloğun tasarım ve uygulama yöntemleri detaylı olarak sunulmuş ve literatürdeki en güncel çalışmalarla kıyaslandığında benzer veya üstün performans gösterdiği ortaya konmuştur.

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*To my family...*
*Aileme...*

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# 1. INTRODUCTION

## 1.1 Milimeter-Wave Integrated Circuits

Over the past century, there has been a continuous shift toward higher operating frequencies in electronic circuits, driven by the increasing demand for higher data rates, resolution, faster operation, and reduced area. From the early days of radio broadcasting in the kilohertz range to the development of microwave radar systems during World War II (Singh, 2021), this trend has steadily continued. Today, advancements in silicon-based semiconductor technologies have sparked an interest in the millimeter-wave spectrum, extending up to 300 GHz (Heydari, 2021). The advantages offered by millimeter-wave make applications such as multi-gigabit wireless communication (Emami et al., 2011), automotive radar systems (Forstner et al., 2008), and various types of sensors (Wang et al., 2018) desirable. As illustrated in Fig. 1.1, wireless and fiber-optic backhaul links are projected to require millimeter-wave integrated circuits (ICs) capable of supporting data rates exceeding 100 Gb/s (Voinigescu et al., 2017). Furthermore, as noted in (Voinigescu et al., 2017), a broad array of emerging autonomous platforms—including drones, robots, lawn mowers, and snow blowers—as well as compact wearable and IoT-connected devices that rely on touchless gesture control, stand to benefit from miniature D-band and J-band distance and velocity sensors with in-package antennas, such as those depicted in Fig. 1.2 (Bredendiek et al., 2013; Nasr et al., 2015; Sarkas et al., 2012,1; Statnikov et al., 2014).

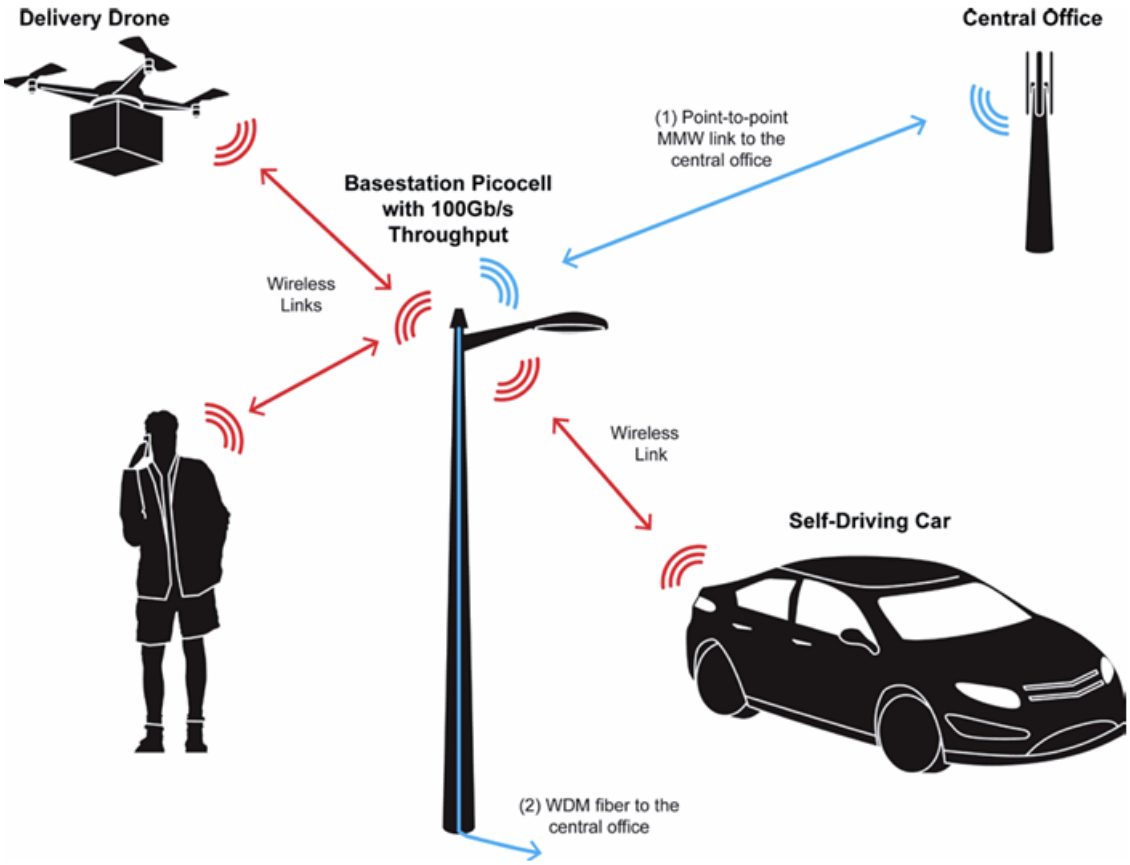



Figure 1.1 Cartoon of a possible millimeter-wave backhaul scenario in 5G networks where a millimeter link at >100 Gb/s will be required between picocells and the central office (Voinigescu et al., 2017).

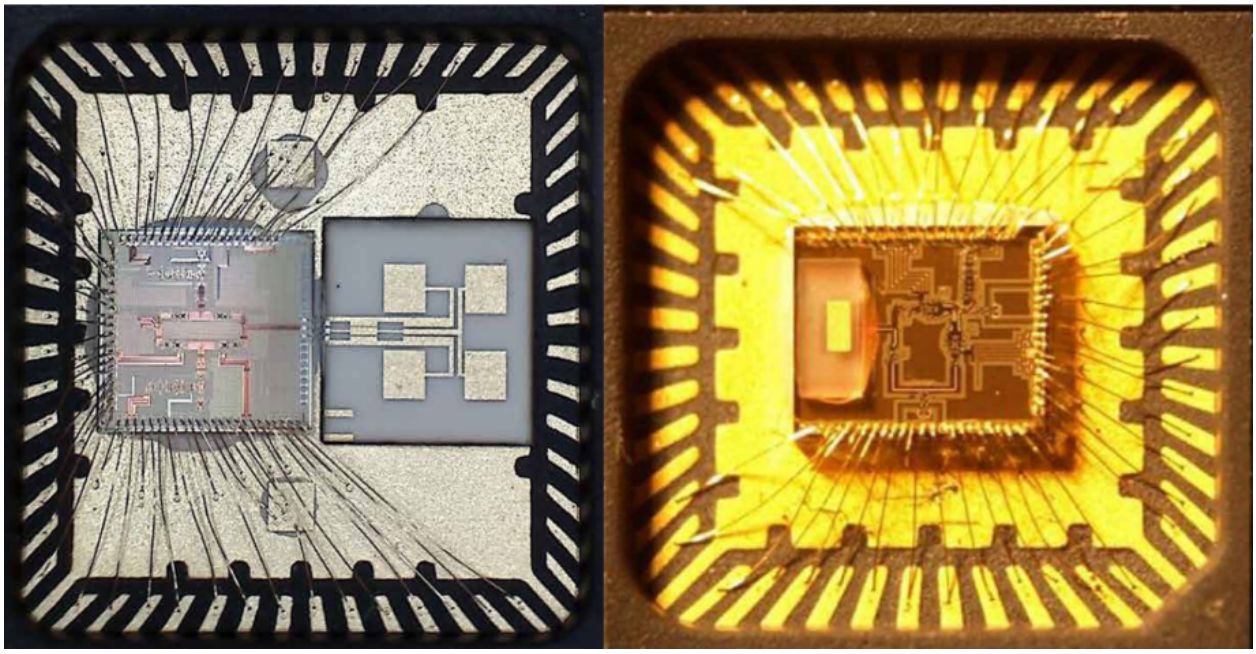


Figure 1.2 Single-chip millimeter-wave systems: (right) 120 GHz distance sensor and (left) 143–152 GHz radar transceiver with built-in calibration. (Sarkas et al., 2012)

While high-frequency operation offers numerous advantages, it also introduces some challenges. One significant issue in millimeter-wave systems is atmospheric attenuation, which increases as frequency rises. As shown in Fig.1.3, higher frequencies suffer greater signal loss. Although atmospheric loss generally increases with frequency, it exhibits distinct peaks at certain absorption bands. Between these peaks, there are relatively flat regions—known as frequency windows—where signal attenuation is more manageable. Notable examples include the W-band (70–110 GHz), D-band (110–170 GHz), and J-band (220–325 GHz).

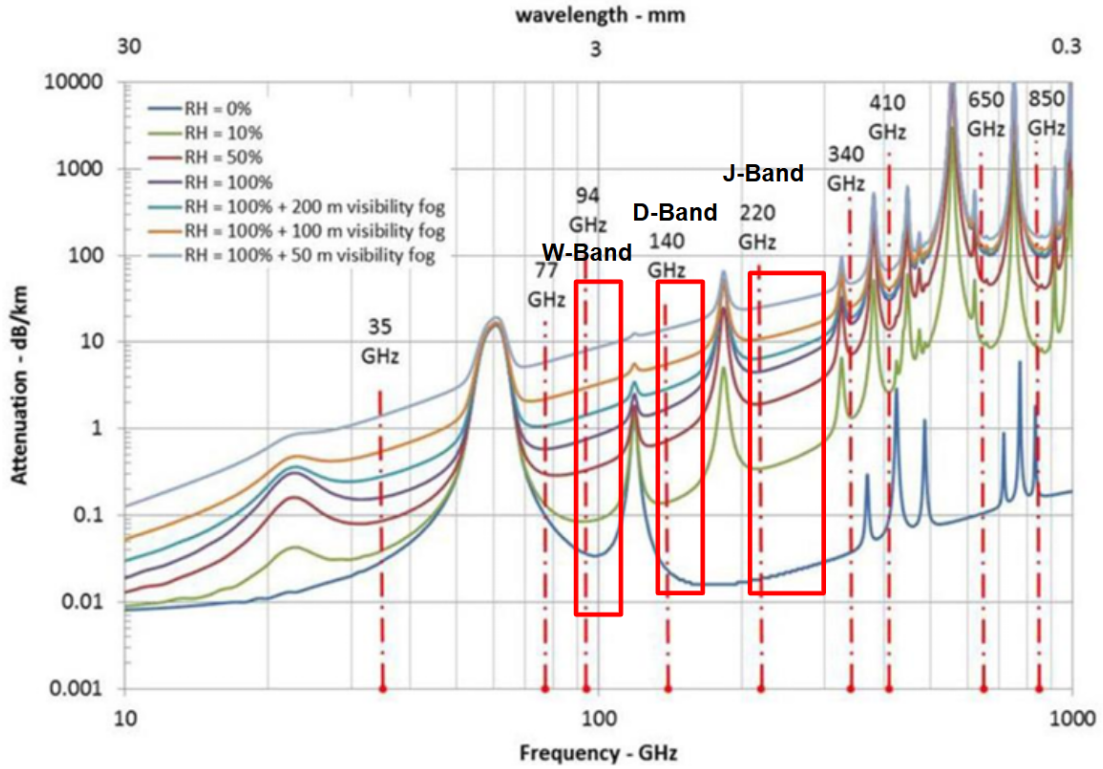



Figure 1.3 Atmospheric attenuation(in dB/km) versus frequency (in GHz) (Turkmen, 2018)

One significant factor to consider is the skin effect, a physical phenomenon where current tends to flow near the surface of a conductor rather than through its core. The skin depth, which is the distance over which the current density decreases, reduces with the square root of the frequency (Pozar, 2012). As the operating frequency rises, this reduced skin depth results in higher losses, impacting both transmission lines and inductors.

## 1.2 Technology Overview

In this section, the technology segments employed in this thesis will be discussed, beginning with the Bipolar Complementary Metal-Oxide-Semiconductor(BiCMOS) technology. The foundational concepts of Bipolar Junction Transistors (BJTs) will first be introduced, followed by an exploration of the role of Germanium (Ge) in enhancing device performance and its resulting technology variants. The discussion will then proceed to Silicon-on-Insulator (SOI) technology.

### 1.2.1 SiGe BiCMOS Technology

Silicon-Germanium Heterojunction Bipolar Transistors (SiGe HBTs) are a type of BJT in which different semiconductor materials are used to form the junctions, giving rise to the term heterojunction. To understand how changes in band structure affect the Direct Current (DC) behavior of a SiGe HBT, it is helpful first to examine the operation of a conventional silicon BJT. A standard BJT consists of two p–n junctions connected back-to-back, forming either NPN or PNP configurations. As illustrated in Fig. 1.4, the cross-sectional and simplified views of an NPN device highlight its three terminals: emitter, base, and collector. In typical operation, current flows from the collector to the emitter. Two physical mechanisms contribute to current conduction in a BJT: diffusion and drift. When the base-emitter (BE) junction is forward-biased with a positive $V_{BE}$, electrons from the heavily doped n-type emitter are injected into the lightly doped p-type base. These electrons diffuse across the base and are swept into the collector by the electric field present across the reverse-biased collector-base (CB) junction, forming the collector current. During their transit, a small fraction of electrons may recombine in the base. To minimize such recombination losses and improve carrier collection efficiency, the base is designed to be both thin and lightly doped (Sedra & Smith, 2014). Concurrently, holes from the base are injected back into the emitter, but this back-injection is minimal due to the emitter's significantly higher doping level. The resulting asymmetry between electron and hole injection leads to a high current gain, denoted as $\beta$ (Cressler, 2008). In SiGe HBT technologies, the base region is engineered with a graded Ge profile rather than being purely silicon. The Ge concentration typically increases linearly from approximately 0% at the emitter-base junction to a peak of around 8 % to 15% near the CB junction. Then it decreases back to nearly 0% to-

ward the collector side (Cressler, 2008). This grading profile, as shown in Fig. 1.5, introduces an internal electric field across the base that accelerates electrons and significantly enhances transport efficiency. The bandgap narrowing effect caused by the increasing Ge content reduces the potential barrier for electron injection at the emitter-base junction, thereby exponentially increasing the collector current density and improving the overall current gain $\beta$. Since emitter charge storage delay is inversely proportional to $\beta$, this enhancement directly contributes to faster switching speeds and higher frequency operation. Another advantage of SiGe grading is the decoupling of base doping concentration from the current gain. This allows for higher base doping levels, which reduce base resistance without compromising gain. The resulting decrease in base resistance enhances the transit frequency ($f_T$). Furthermore, the inclusion of Ge near the CB junction improves the transistor's output characteristics by increasing the Early voltage. Although this effect is not immediately intuitive, it arises from the bandgap narrowing on the collector side of the base, which alters the intrinsic carrier profile and mitigates the base widening effect associated with increasing $V_{CB}$. In essence, the graded Ge profile shortens the electron transit time through the base, which is a critical limiting factor in high-frequency performance. It thus enables SiGe HBTs to operate effectively at much higher frequencies compared to conventional Si BJTs. This limitation mentioned can be observed in the equations for $f_T$, maximum frequency ($f_{max}$) and minimum noise figure ($NF_{min}$) in equations 1.1, 1.2 and 1.3 respectively.

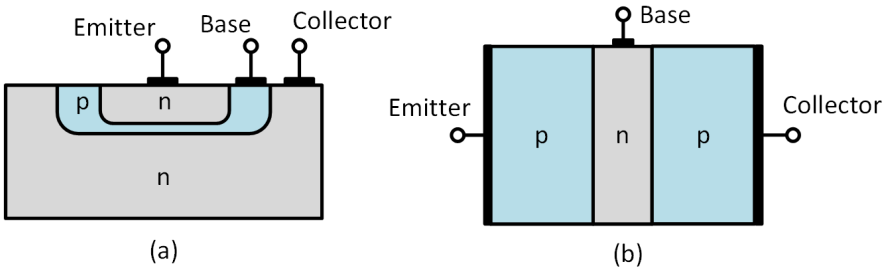



Figure 1.4 Cross-sectional (a) and simplified view (b) of BJT

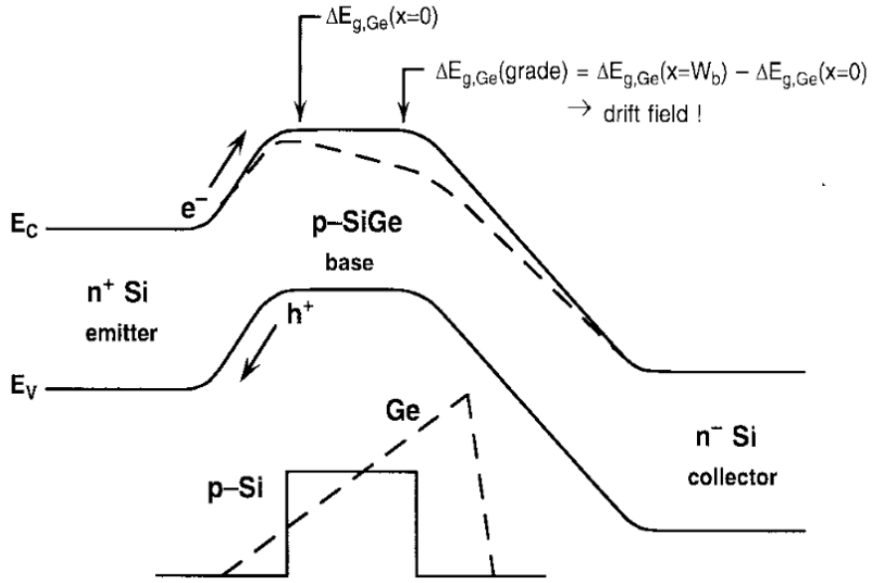



Figure 1.5 The representation of the energy band diagram of SiGe HBT (top) and Si BJT (bottom)(Cressler, 1998)

$$f_T = \frac{1}{2\pi}\left(\tau_b + \tau_c + \frac{1}{g_m}(C_\pi + C_\mu) + (r_e + r_c)C_\mu\right)^{-1} \tag{1.1}$$

$$f_{\max} = \sqrt{\frac{f_T}{8\pi C_\mu r_b}} \tag{1.2}$$

$$NF_{\min} = 1 + \frac{n}{\beta_{DC}} + \sqrt{\frac{2J_c}{V_t}(r_e + r_b)\left(\frac{f^2}{f_T^2} + \frac{1}{\beta_{DC}}\right)} + \frac{n^2}{\beta_{DC}} \tag{1.3}$$

### 1.2.2 G2 and G3 Technologies

In February 2008, the European Union launched the DOTFIVE project under the Seventh Framework Programme (FP7)DOTFIVE Project (2008), to push the performance limits of SiGe HBTs toward a $f_{max}$ of 500 GHz Chevalier et al. (2011). The targeted enhancements are illustrated in Fig. 1.6, which highlights the improvements achieved in this technology node. The outcomes of the DOTFIVE project later contributed to the development of IHP's SG13G2 technology. In October 2012, the EU initiated the DOTSEVEN project as a continuation of this effort to further increase performance by developing SiGe HBTs capable of operating at frequen-

cies approaching 700 GHz. Several process-level innovations were introduced during this phase. Adjustments in the collector region, including optimized doping profiles and geometries, led to improved breakdown voltages and lower collector resistance. The Ge concentration in the base was precisely graded to establish an internal electric field, which accelerates electron transport and reduces base transit time. Additionally, the incorporation of carbon into the SiGe base effectively suppressed boron diffusion, helping maintain a sharp doping profile and improving long-term device reliability(Ruecker & Heinemann, 2018). These process improvements also contributed to a reduction in base resistance, which is critical for high-frequency operation. As a result, a significant improvement in the $f_T$ was achieved, as shown in Fig. 1.7.

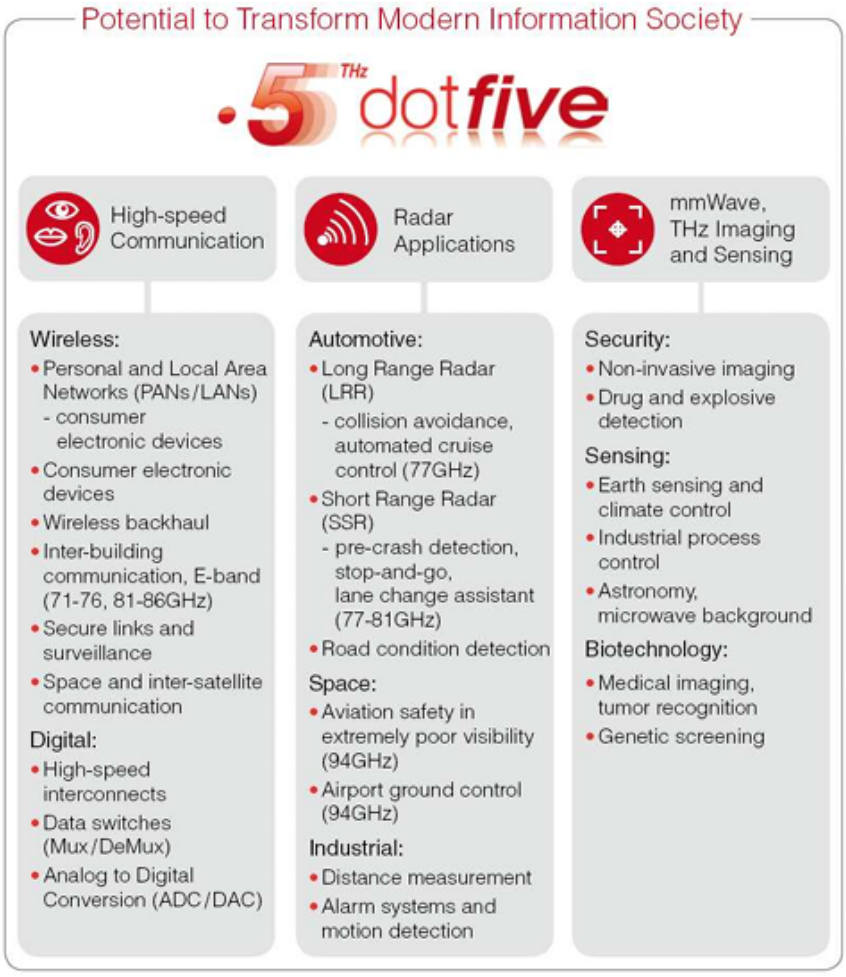



Figure 1.6 Overview of the applications targeted by the DOTFIVE european project (Chevalier et al., 2011)

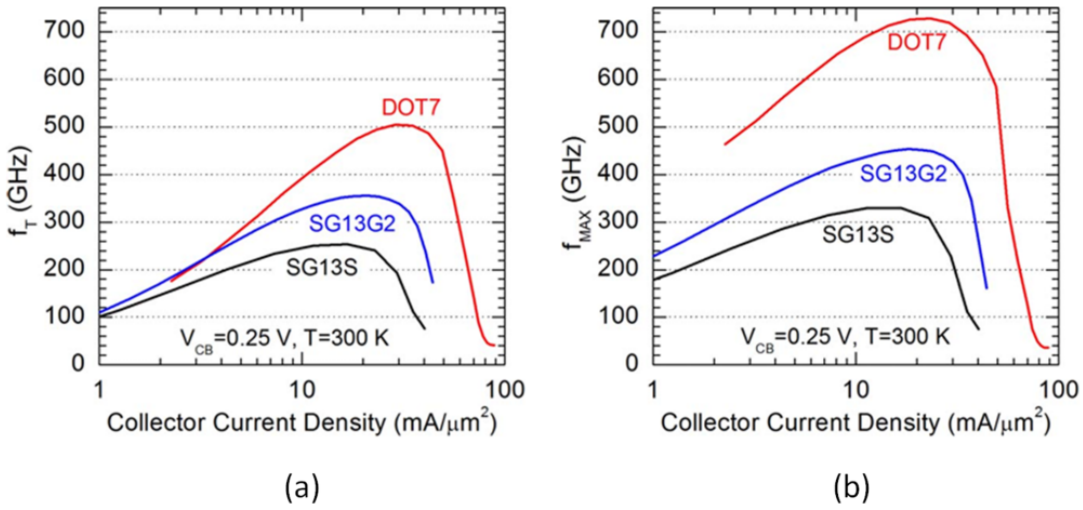



Figure 1.7 fT and fmax comparison of G3,G2 and S technologies(Rücker & Heinemann, 2018)

### 1.2.3 SOI Technologies

SOI MOSFETs are a class of transistors fabricated on a layered substrate that includes a buried oxide (BOX) layer beneath a thin silicon film. This structure fundamentally differs from conventional bulk CMOS devices by electrically isolating the transistor from the substrate, reducing parasitic capacitance and leakage currents. Building up from the traditional SOI, several variants further reduce the capacitance, such as air gap transistors, where, by forming an air gap in the interconnect dielectric directly above the transistor gate, the effective dielectric constant above the gate is significantly reduced; therefore, $C_{OFF}$ (off capacitance) is diminished. The air gap SOI transistors look like in Fig. 1.8. The SOI technology is highly desired in switch design because of its reduced $R_{ON}$(on resistance) and $C_{OFF}$ compared to bulk CMOS technology because this technology do not use a BOX layer to isolate substrate resulting in more capacitances, likewise SiGe BiCmos technology previously described is not a good fit for a switch design because not only does it have no isolation to substrate but also HBT processes introduces extra leakage through the base when used in saturation mode leading to excessive losses primarily when used as a series device. SOI technology is designed for lowest $R_{ON}$ and $C_{OFF}$ for comparison in Table 1.1 is shown some technologies and their corresponding $R_{ON}C_{OFF}$ values for the designs manufactured by the works (Gianesello et al., 2016; Meng et al., 2015a; Moen et al., 2015).

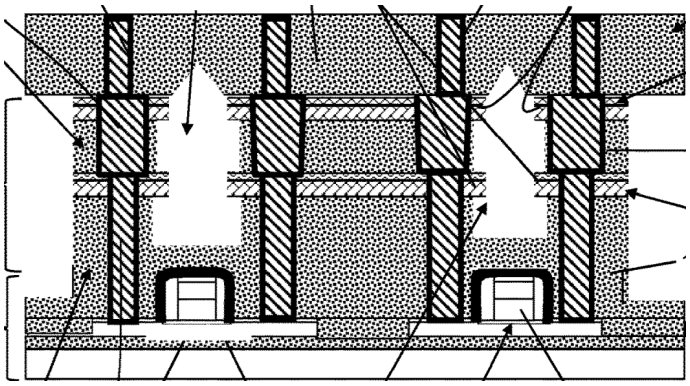


Figure 1.8 Air gap SOI transistor side-view (He et al., 2017)

Table 1.1 Comparison of $R_{ON}C_{OFF}$ across technologies

| | 180 nm SiGe BiCMOS | 65 nm Bulk CMOS | 130 nm SOI CMOS |
|---|---|---|---|
| $R_{ON}C_{OFF}$ | 300 fS | 147 fS | 80 fS |

# 2. D-BAND POWER AMPLIFIER DESIGN

A Power Amplifier (PA) is an integral part of a system where power transmission is required, whether it is a communication system, radar, or any other applications mentioned in Chapter 1. To transmit a signal further, a PA needs to be implemented in the chain. The most essential requirements for a PA include output power ($P_{out}$), gain, and power added efficiency (PAE). In this chapter, the fundamentals of PAs will be discussed. Then, PAs will be addressed in the context of millimeter-wave circuits, along with the current works in the literature. Next, three SiGe BiCMOS-based PAs will be introduced and explained. Finally, these works will be compared with the current state-of-the-art designs.

## 2.1 Power Amplifier Fundamentals

The design of PAs differs from that of small-signal amplifiers. In classical small-signal amplifier design, the input and output are conjugately matched to the source and load impedance, respectively. This approach cancels out parasitic reactances and equates the real parts of the impedance. However, in PA design, the output is typically not conjugately matched to the load impedance. Instead, it is matched to an optimum load resistance ($R_{opt}$), which enables higher $P_{out}$.

In Fig. 2.1, two different matching strategies are illustrated. In Fig. 2.1(a), power matching is performed by presenting the amplifier with $R_{opt}$, enabling power matching. In Fig. 2.1(b), conjugate matching is shown, where the reactive components are canceled, and the impedance seen at the drain has the same resistive value as the source. The question arises: Why does power matching enable better performance than conjugate matching for PAs?

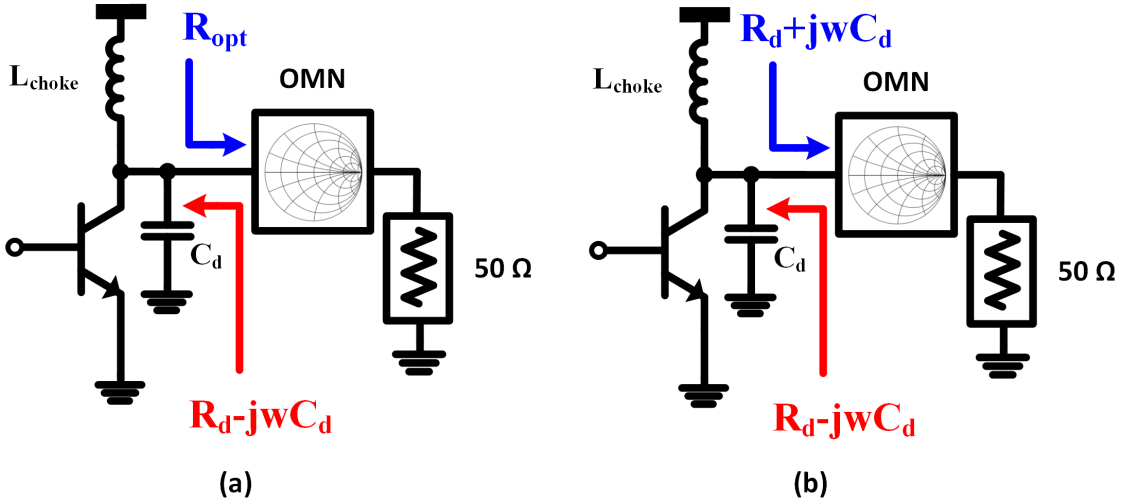



Figure 2.1 Power match (a) and conjugate match (b)

Imagine there is an ideal current source supplying $I_G$ current with an output resistance of $R_G$ that is connected to an $R_{Load}$ whose value we can tune as seen on Fig. 2.2. Let $I_G$ be 1 Amp and $R_G$ be 100 ohms. According to conjugate matching, an $R_{Load}$ of 100 ohms needs to be selected, which means a 50 V swing will occur at the output. However, the device probably will not be able to withstand 50 V. Also, there are limitations on the DC voltage supply side (Cripps, 2006), raising constraints on conjugate matching. Therefore, instead of a 50 V voltage swing, the maximum voltage, denoted as $V_{MAX}$, whose value is smaller than 50 V, will be determined by the device voltage rating. Under this condition, the voltage swing is the maximum possible that the device can handle; however, the current swing is not maximum, denoted by maximum current swing $I_{MAX}$, which creates a suboptimal PA design when conjugately matched. This can be seen on Fig. 2.3(a) where voltage is at maximum however current is far from optimal value whose $P_{out}$ is lower as can be exemplified by Fig. 2.3(b) where dashed line is the circuit that is power matched as opposed to straight line that is conjugately matched. The value of $R_{load}$ is smaller than its conjugate-matched value because increasing $I_{Max}$ requires a reduction in load resistance. Therefore, $R_{load}$ can be considered small compared to $R_G$, leading to an optimal $R_{load}$ which is $R_{opt}$ that is equal to the ratio of $V_{MAX}$ to $I_{MAX}$, as expressed in (2.1).

Linearity is characterized by the output 1 dB compression point (OP1dB), which is the $P_{out}$ level at which the gain drops by 1 dB from its small-signal, linear behavior. This point indicates the deviation from the ideal linear gain that would be expected if the amplifier continued to respond linearly to increasing input power ($P_{in}$). Also especially in high frequency circuits and radar applications saturated output power

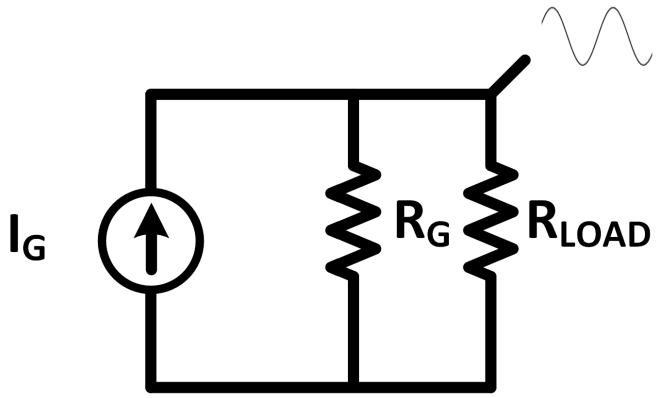



Figure 2.2 Representative resistive matching circuit

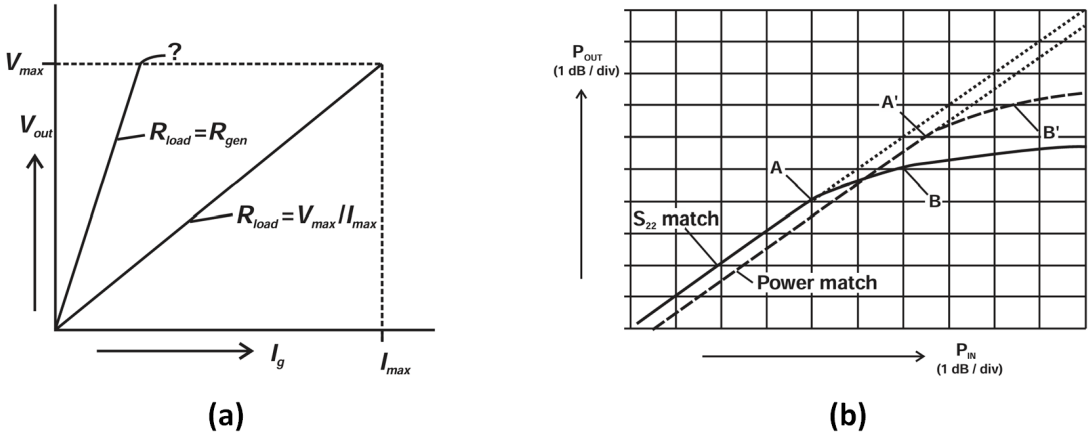



Figure 2.3 (a) Loadline vs conjugate matching curves and (b) $P_{out}$ increase upon power matching the circuit(Cripps, 2006)

($P_{sat}$) is preferred which shows full compression fo the power meaning the input power is increased to a point where $P_{out}$ is not changing anymore with respect to $P_{in}$ these measures can be seen on Fig. 2.4.

$$R_{opt} = \frac{V_{MAX}}{I_{MAX}} \tag{2.1}$$

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.2}$$

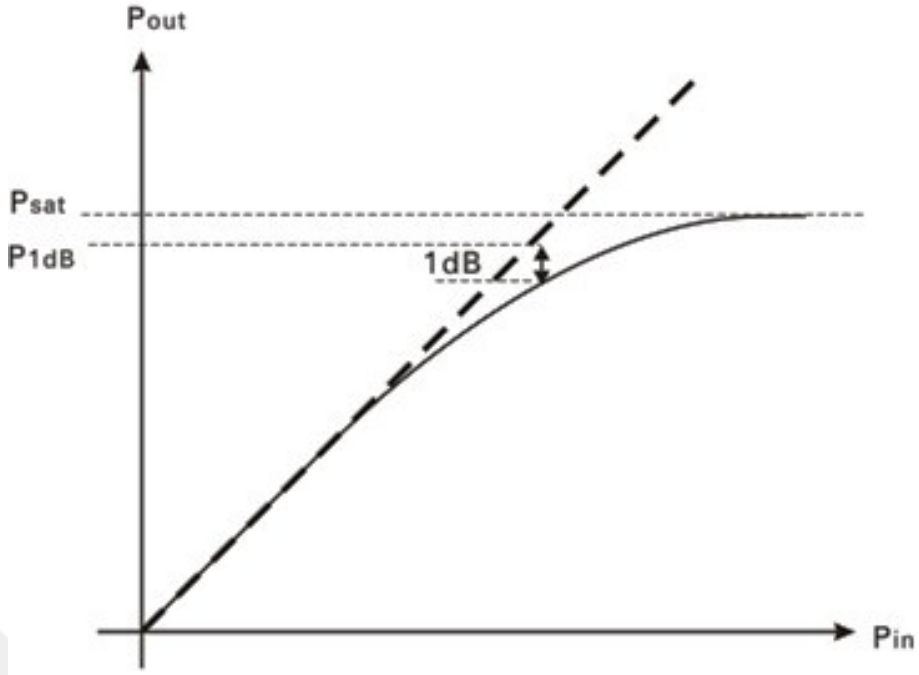



Figure 2.4 OP1dB and $P_{sat}$ values vs $P_{in}$ (Keysight Technologies, nd).

$$PAE = \frac{P_{out} - P_{out}}{P_{DC}} \tag{2.3}$$

Another Concern in an PA design is the efficiency, the designer is concerned with two types of efficiencies that is drain efficiency symbolized as $\eta$ which is basically the $P_{out}$ divided by the dc power as seen in (2.2) this efficiency measure does not take into account input power, the other type is PAE which as the name suggests takes $P_{in}$ into account as seen in (2.3).

## 2.2 Power Amplifier Classes

Over time, various amplifier classes have been developed to meet different design requirements. Broadly, PAs fall into two categories: transconductance amplifiers and switching-mode amplifiers. The transconductance category includes Class A, AB, B, and C, while switching-mode amplifiers encompass Class D, E, and F. Each class targets specific performance criteria. The primary distinction between transconductance and switching-mode amplifiers lies in the balance between linearity and efficiency. Class A amplifiers provide good linearity but are limited to a maximum

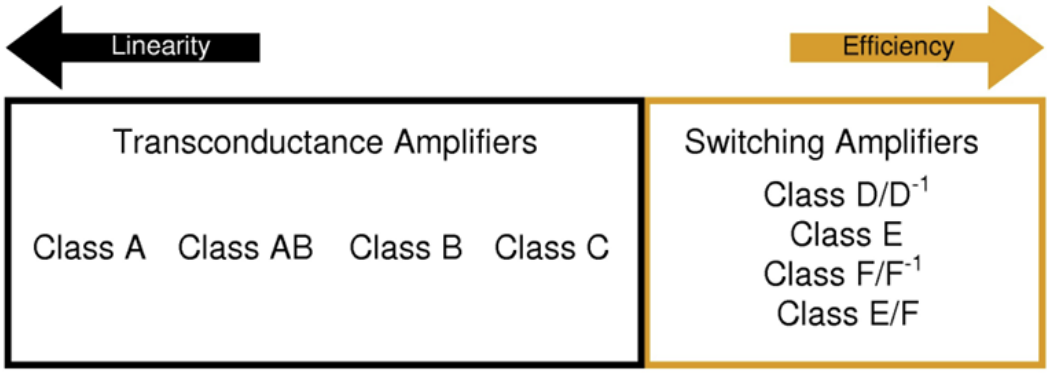



Figure 2.5 The linearity-efficiency trade-off between different classes of amplifiers (Zihir, 2011)

efficiency of around 50%. In contrast, switching-mode amplifiers can theoretically reach 100% efficiency, though they exhibit significant nonlinearities. Intermediate classes like AB, B, and C offer varying compromises between these two extremes, as illustrated in Fig. 2.5.

### 2.2.1 Class A

Class-A PAs operate with a conduction angle $\theta_C$ =2$\pi$, meaning the transistor conducts over the entire cycle, resulting in large swings, larger than any other class PAs. In Fig. 2.6, the loadline behavior of a Class-A amplifier is illustrated. In this figure, a quiescent point is selected, enabling maximum swing for both current and voltage. The voltage swing $V_{swing}$ can be found in Equation 2.4, and the DC voltage can be found in Equation 2.6. Also, the current swing and DC current are $I_{MAX}$ as seen in Equation 2.6. To calculate drain efficiency, we need to calculate the RF power ($P_{RF}$) and dc power ($P_{DC}$), as shown in equations 2.8 and 2.7. Finally, using 2.2, the final drain efficiency value can be obtained in 2.9. For $V_{MIN} = 0$, an ideal efficiency value of 50% can be obtained.

$$V_{swing} = \frac{V_{MAX} - V_{MIN}}{2} \tag{2.4}$$

$$V_{DC} = \frac{V_{MAX} + V_{MIN}}{2} \tag{2.5}$$

$$I_{swing} = I_{MAX} = I_{DC} \tag{2.6}$$

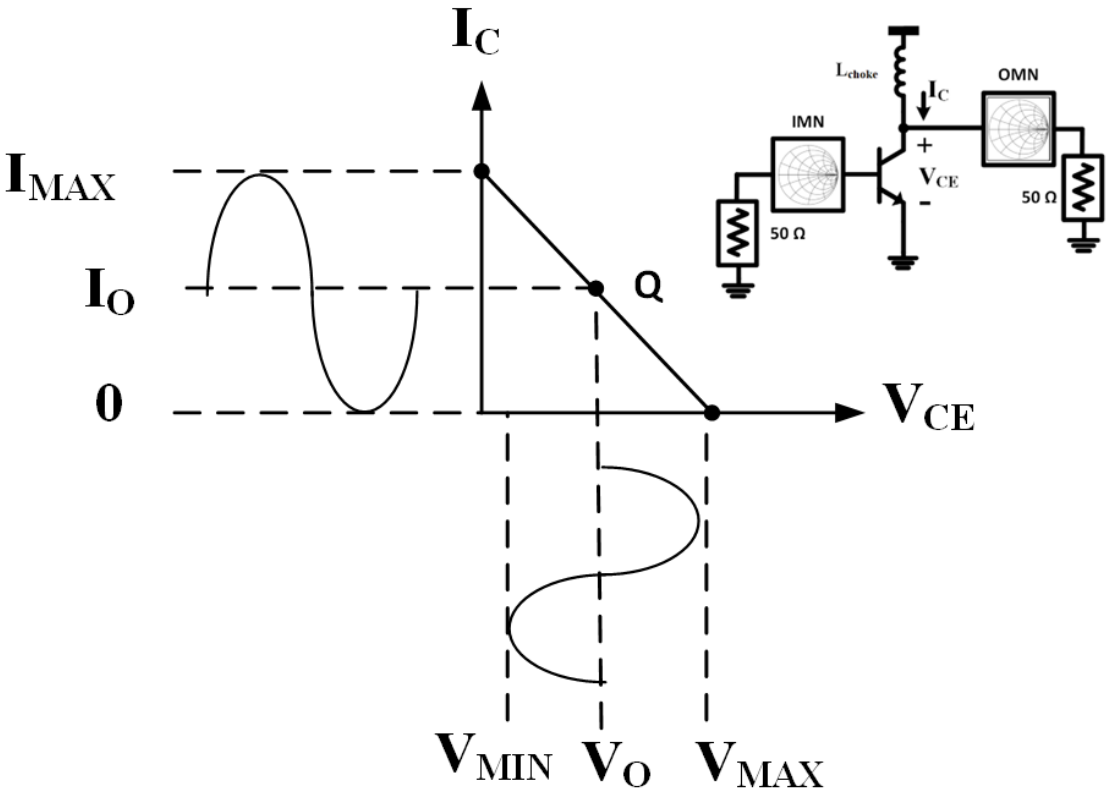



Figure 2.6 Load-line behavior of class A amplifier with inductive load.

$$P_{RF} = \frac{1}{2} V_{swing} I_{swing} \tag{2.7}$$

$$P_{DC} = \frac{1}{2} V_{swing} I_{swing} \tag{2.8}$$

$$\eta_{ClassA} = \frac{P_{RF}}{P_{DC}} = \frac{1}{2} \frac{V_{MAX} - V_{MIN}}{V_{MAX} + V_{MIN}} \tag{2.9}$$

### 2.2.2 Class B

In Class B amplifiers, $\theta_C = \pi$, meaning the current wave clips half of the cycle while still having a full swing voltage. The voltage and current waves of the Class B amplifier can be seen in Fig. 2.7. The immediate consequence of this waveform is reduced linearity because $I_{MAX}$ is lowered to half of its value. How about efficiency?

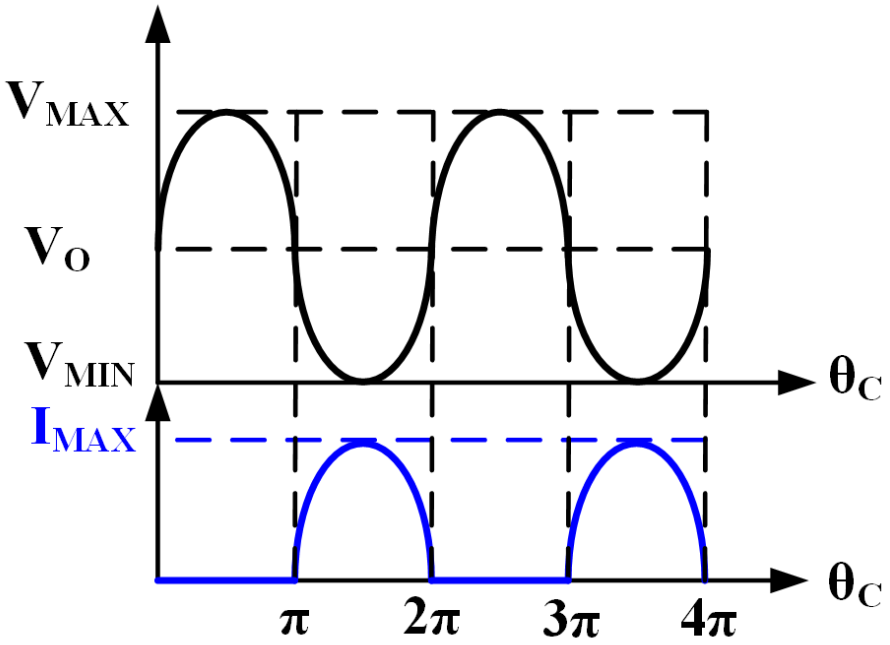



Figure 2.7 Class B amplifier voltage and current waveforms vs conduction angle

RF and DC powers need to be calculated; however, it is not so evident from the current waveform. Indeed, the current waveform consists of many sinusoidal waves having different amplitudes and frequencies according to (Bracewell, 1978). Half clipped sine DC term can be found as seen in Equation (2.10) also since we are interested in efficiency of fundamental frequency, half clipped sine wave current wave at fundamental frequency ($I_{fund}$) can be as in Equation (2.11), using the same flow used in Class A we can find the $P_{RF}$ in Equation (2.12) and $P_{DC}$ in Equation (2.13) to end up with the $\eta$ in Equation (2.14). We end up with a larger efficiency value of 78.5% because the DC current is not conducting half of the time. As a consequence of many frequency components in Class B operation, these values need to be removed by a harmonic filter that will only allow for the fundamental frequency to travel to the output.

The gain of the circuit will also drop due to half of the waveform being clipped. Half the amplitude means, in power terms, a quarter of the power that corresponds to 6 dB.

$$I_{\text{dc}} = \frac{1}{2\pi}\int_0^{\pi} I_{\text{MAX}} \sin\theta \, d\theta = \frac{1}{2\pi} \cdot I_{\text{MAX}} \cdot [-\cos\theta]_0^{\pi} = \frac{I_{\text{MAX}}}{\pi} \tag{2.10}$$

$$I_{\text{fund}} = \frac{1}{\pi}\int_0^{\pi} I_{\text{MAX}} \sin^2\theta \, d\theta = \frac{1}{\pi} \cdot I_{\text{MAX}} \cdot \pi \cdot \frac{1}{2} = \frac{I_{\text{MAX}}}{2} \tag{2.11}$$

$$P_{\mathrm{RF}} = \frac{1}{2} V_{\mathrm{fund}} I_{\mathrm{fund}} = \frac{1}{2} R_L \left( \frac{I_{\mathrm{MAX}}}{2} \right)^2 = \frac{1}{2} \cdot \frac{V_{\mathrm{MAX}}^2}{R_L} \tag{2.12}$$

$$P_{\mathrm{DC}} = V_o \cdot I_{\mathrm{dc}} = V_o \cdot \frac{I_{\mathrm{rf}}}{\pi} \tag{2.13}$$

$$\eta_{ClassB} = \frac{P_{\mathrm{rf\ out}}}{P_{\mathrm{dc}}} = \frac{\frac{1}{8} R_L I_{\mathrm{MAX}}^2}{\frac{1}{\pi} V_o I_{\mathrm{MAX}}} = \frac{\pi}{8} \cdot \frac{R_L I_{\mathrm{MAX}}}{V_o} = \frac{\pi}{4} \cdot \frac{V_{\mathrm{rf}}}{V_o} = \frac{\pi}{4} = 78.5\% \tag{2.14}$$

### 2.2.3 Class AB

Class AB is an amplifier whose conduction angle is between Class A and Class B, which will land on $\pi < \theta_C < 2\pi$; consequently, an ideal efficiency value can be expected between 50% and 78.5%. Also, since the current amplitude is between Class A and Class B, an intermediate linearity value can be expected.

### 2.2.4 Class C

In a Class C amplifier, the gate voltage is set so that the device conducts for only a small portion of the input current cycle. This limited conduction results in much lower power dissipation compared to other amplifier classes, allowing Class C amplifiers to achieve efficiencies as high as 90%. Despite this advantage, Class C amplifiers have notable limitations, particularly in high-frequency applications. One major issue is the trade-off between efficiency and power gain: as efficiency nears 100%, the $P_{out}$ and consequently the power gain drop toward zero. This trade-off is problematic for high-frequency systems where power gain is essential. Another drawback is the significant nonlinearity of Class-C amplifiers. They require high-Q resonators at the output to function effectively, which is impractical for on-chip high-frequency designs.

### 2.2.5 Class D and E

Unlike traditional amplifier classes that use active devices in a linear mode, Class D and Class E amplifiers operate in switching mode, where transistors act as ideal switches either entirely on or fully off. This approach minimizes power dissipation, enabling theoretical efficiencies up to 100%, as no voltage and current overlap occurs during switching. Class D amplifiers generate square-shaped voltage waveforms using two or more switching transistors, while the current waveform remains sinusoidal. They are effective but can be challenging to implement due to real-world non-idealities in switching behavior. Class E amplifiers address some of these limitations through a technique called soft-switching. By shaping the voltage and current waveforms using a reactive network, they ensure zero voltage or zero current switching conditions, reducing power loss even when transitions are not instantaneous. Class E designs are often simpler than Class D but may experience high voltage peaks, which can stress or damage transistors.

## 2.3 High Frequency Power Amplifiers Differences

As the frequency of operation increases, the way that the RF/millimeter-wave circuits look changes from inductor-based design to transmission line-based design, as seen in Fig. 2.8. In inductors, the physical asymmetry in their geometry further exacerbates these losses. For example, in a loop inductor, the current tends to concentrate toward the inner radius of the conductor (Niknejad & Hashemi, 2008). This crowding effect is one reason transmission lines are preferred over inductors at higher frequencies. Another reason is the resonant behavior of inductors at high frequencies. The coiling of the inductor creates parasitic capacitances, which can cause the inductor to resonate. An inductor functions effectively only when magnetically stored energy dominates over electrically stored energy(Niknejad & Hashemi, 2008). When inductors resonate at high frequencies, they are less effective, making them unsuitable for high-frequency designs.

Higher frequencies also bring some challenges to PA design, in particular. The trade-offs mentioned earlier, using Class operations on linearity and efficiency, do not apply anymore. In these Classes, such as Class D, E, and F, the voltage and current waveforms are manipulated at the output based on the device's intrinsic

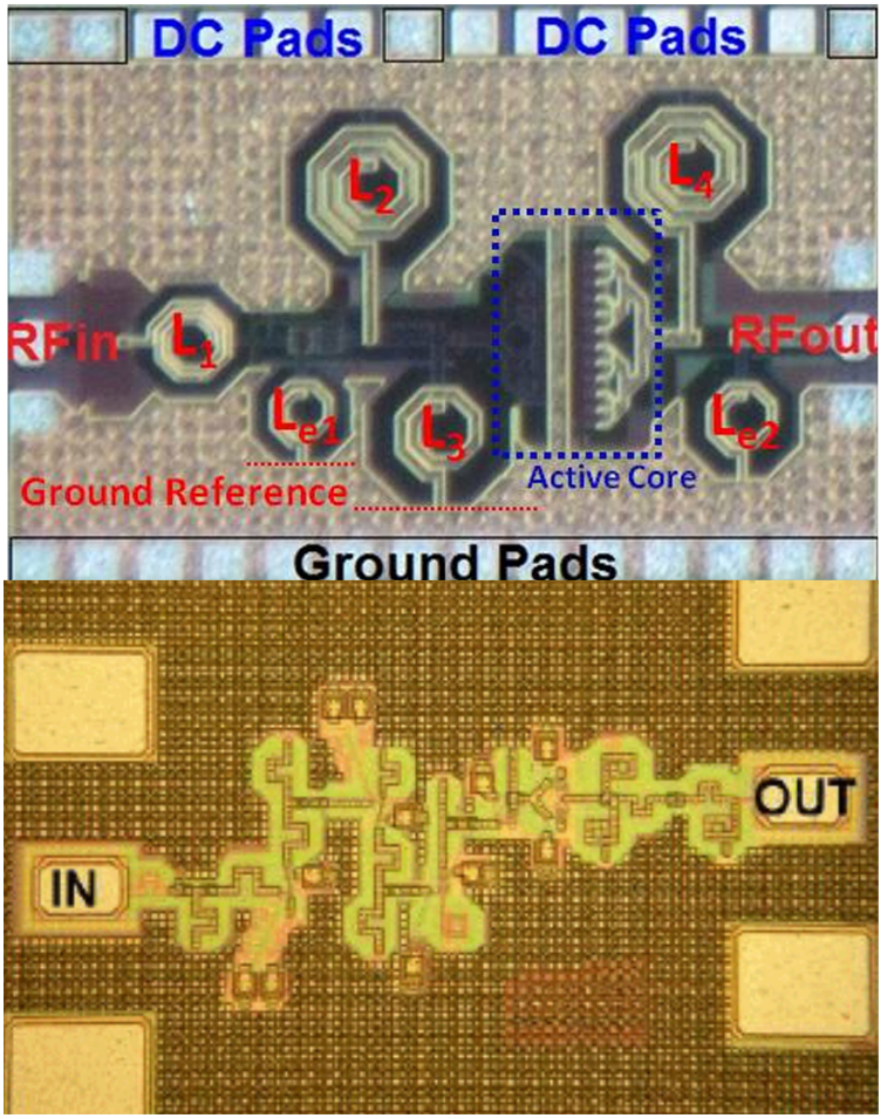



Figure 2.8 Inductor based X-Band PA circuit(top) (Zihir, 2011) and transmission line based D-Band PA circuit(bottom) (Laskin et al., 2007)

behavior. However, as operation shifts into the Millimeter range and beyond, the increasing complexity of parasitic elements within the transistor prevents accurate extraction of its intrinsic characteristics. The dominance of capacitive parasitic lowers the output impedance, complicating harmonic management. As a result, techniques that rely on harmonic tuning and switching mechanisms become difficult to implement for silicon-based PAs operating at millimeter-wave frequencies.

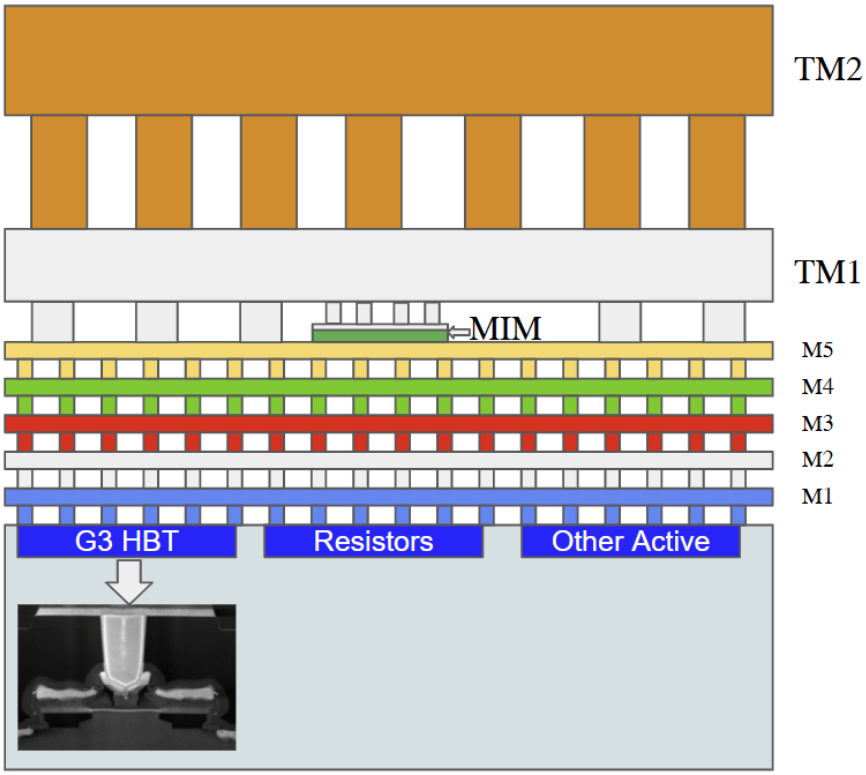



Figure 2.9 IHP 130 nm BEOL

## 2.4 Two Stage Differential Power Amplifier Design

The PA is fabricated using the 130 nm SiGe BiCMOS process (IHP SG13G3), which offers $f_T$ and $f_{max}$ of 450 GHz and 700 GHz, respectively. The back-end-of-line (BEOL) stack comprises five thin metal layers and two thick top metal layers, with a metal-insulator-metal (MIM) capacitor layer implemented between metal 5 and top metal 1. The complete stack-up is depicted in Fig. 2.9. For RF Metalizations, the top thick metals are preferred, which have a thickness of 3 $\mu$m and 2 $\mu$m. Metal 4 and metal 2 are used for ground, whereas metal 1 and metal 3 are used for DC routing. Using metal 4 as ground gives the advantage of efficiently routing under metal 4 without having to worry about top metals coupling to the DC routing metals.

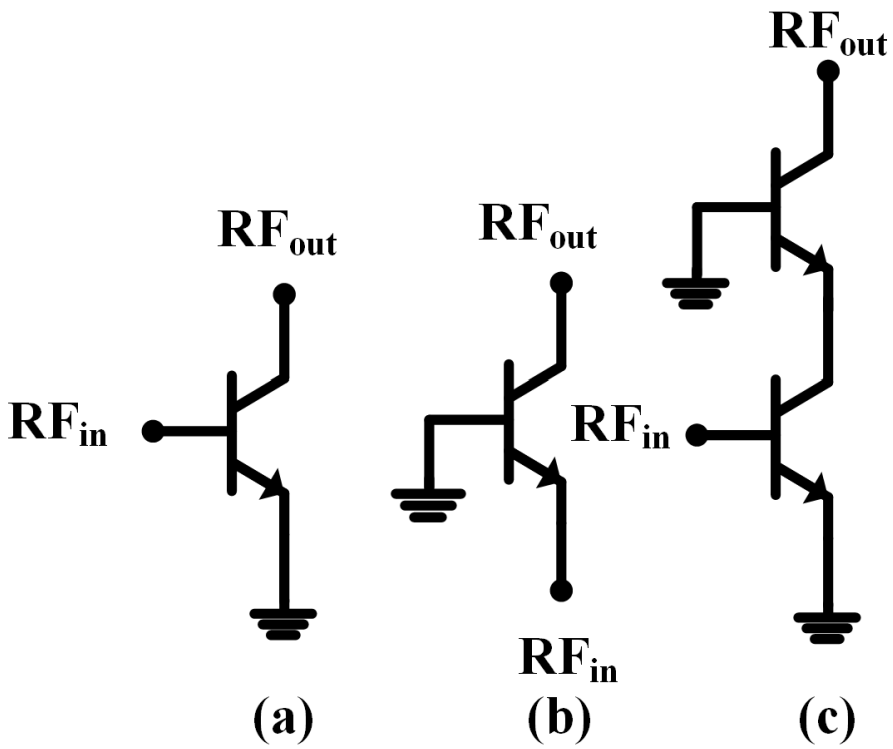



Figure 2.10 (a) CE, (b) CB, and (c) cascode amplifiers

### 2.4.1 Core Optimization

For RF amplifier topology selection, Common Emitter (CE), CB, and cascode configurations are among the most widely considered options, as illustrated in Fig. 2.10. In the case of SiGe HBTs, the collector-emitter breakdown voltage ($BV_{CEO}$), which defines the maximum signal swing permissible between the collector and emitter terminals, is approximately half of the collector-base breakdown voltage ($BV_{CBO}$) (Grens et al., 2005). This inherent advantage renders the CB configuration more favorable in terms of linearity. By combining the CE and CB stages in a cascode configuration, the breakdown voltage can be further enhanced not only by distributing the voltage swing across two transistors but also by utilizing the CE stage as a transconductance element to regulate the emitter current of the CB stage, thereby optimizing its breakdown characteristics. Based on these considerations, the cascode topology has been adopted. Conventionally, the core layout is designed to minimize parasitic effects; in this PA, these parasitics are deliberately incorporated as functional elements of the output matching network. For millimeter-wave and sub-terahertz, the interconnections and the metal layer around the transistors, namely the core layout of the PA, play a critical role.

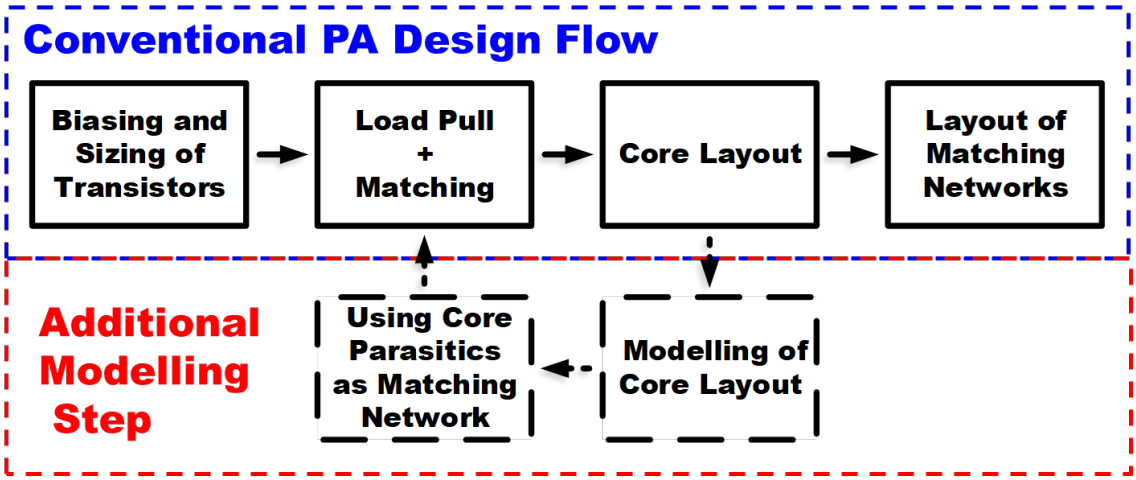



Figure 2.11 Core layout design flow

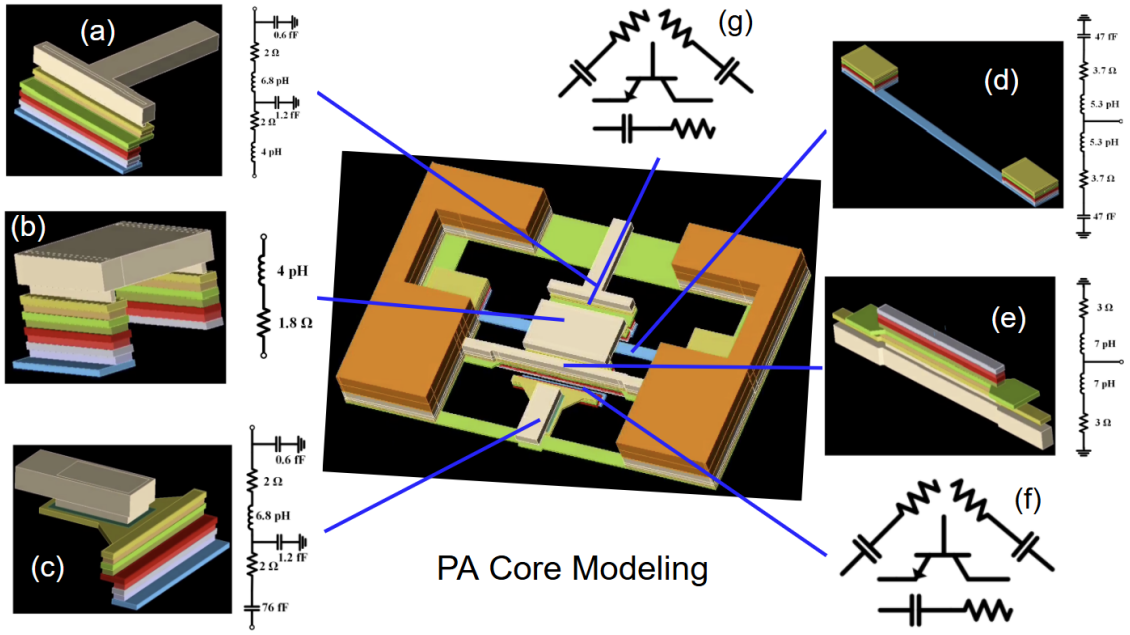


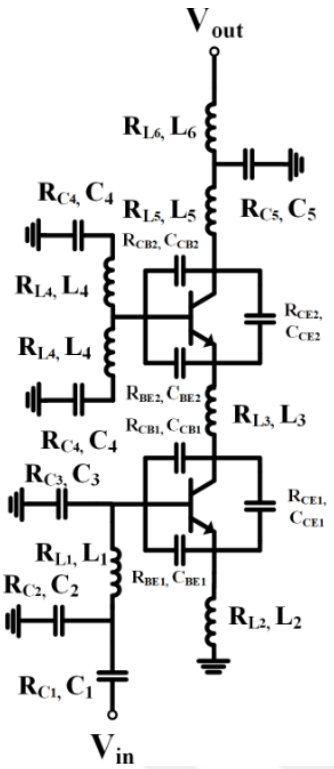

Figure 2.12 PA core modelling of the sections

Small traces can significantly impair the behavior of the circuit. A line of a few microns of metal can shift the output impedance of the PA away from the desired optimal value. Therefore, understanding the effect of the parasitics on the layout of the core using a lumped-element model enables their exploitation as part of the overall matching network. This approach can optimize the size and the loss of the output matching network, thereby improving the PAE. A practical design approach is illustrated in Fig. 2.11, where, rather than directly optimizing the physical layout, a model of the key interconnect metallization is first constructed. By developing a schematic that mirrors the actual circuit through section-wise modeling, design trade-offs can be evaluated more effectively. A single-ended version of the PA stage has been modeled to improve accuracy while reducing complexity. The initial step

involved identifying key nodes and extracting the relevant metallization. In Fig. 2.12, the core layout and its associated metallization models are shown. The model is composed of five sections, along with terminal capacitances introduced by the metallization. In (a), the output of the core is depicted. The transistor collector is placed on metal 1, the lowest metal level, as discussed earlier. Via inductance and resistance are modeled, and for each step of the stairs, shunt capacitance is included. The metal routing extends up to the top metal. Then it continues to the output, enabling the matching network to be implemented at higher metal levels, such as top metal 1 and top metal 2. In (b), the interconnect between CE and CB is modeled. Rather than stepping gradually through intermediate levels, the connection directly transitions to top metal 1. This reduces shunt capacitance and increases inductance, which will be advantageous, as discussed later in this section. Section (c) models the input side, where a stair-like structure forms a $\pi$-network that aids matching. In (d), the base of the CB stage is modeled. Here, metal 1 extends outward as a thin line, contributing inductance and terminating in a metal-on-metal (MOM) capacitor. This capacitor provides 47 fF by overlapping metals 1, 3, and 5 to create a fringing field. Section (e) models the emitter connection to the ground in the CE stage via an inductor. Finally, in (f) and (g), equivalent capacitances arising from the metallization are included. While some of these are negligible, others have a measurable effect and are selectively retained in the final model. Using the sections that are modeled along with the terminal capacitances, the following model has been extracted in Fig. 2.13. To align the model values with the EM simulation, both the real and imaginary components of the two-port S-parameters from the EM and modeled data are mapped. To ensure that each value contributes uniformly to the overall mapping, normalization is applied to both the real and imaginary parts, as shown in Equation 2.15. Since two-port S-parameters characterize the system, the indices i and j take values from 1 to 2.

$$\mathrm{err}_{S_{ij}} = \frac{\mathrm{real}|\mathrm{imag}(S_{ij}^{\mathrm{model}}) - \mathrm{real}|\mathrm{imag}(S_{ij}^{\mathrm{em}})}{\mathrm{real}|\mathrm{imag}(S_{ij}^{\mathrm{model}}) + \mathrm{real}|\mathrm{imag}(S_{ij}^{\mathrm{em}})} \tag{2.15}$$

Eight equations for each S parameter, real and imaginary parts, are extracted and mapped. In this procedure, $S_{12}$ is given a negligibly small weight because it is usually shallow, and removing that reduces the optimization complexity and gives a better chance for other S-parameters to be accurately mapped. Both EM and model are terminated with the same input and output impedance for accurate comparison. The error values can be seen for the four different S-parameters real and imaginary parts in Fig. 2.14. In Fig. 2.15, a comparison of the return loss values can be seen,




| $L_1$ (pH) | $L_2$ (pH) | $L_3$ (pH) | $L_4$ (pH) | $L_5$ (pH) | $L_6$ (pH) |
|---|---|---|---|---|---|
| 7 | 7 | 4 | 5.3 | 4 | 6.8 |
| $R_{L1}$ (Ω) | $R_{L2}$ (Ω) | $R_{L3}$ (Ω) | $R_{L4}$ (Ω) | $R_{L5}$ (Ω) | $R_{L6}$ (Ω) |
| 2 | 3 | 1.8 | 3.7 | 2 | 2 |
| $C_1$ (fF) | $C_2$ (fF) | $C_3$ (fF) | $C_4$ (fF) | $C_5$ (fF) | |
| 76 | 1.2 | 0.6 | 47 | 1.2 | |
| $R_{C1}$ (Ω) | $R_{C2}$ (Ω) | $R_{C3}$ (Ω) | $R_{C4}$ (Ω) | $R_{C5}$ (Ω) | |
| 2 | 0 | 0 | 0 | 0 | |
| $C_{BE1}$ (fF) | $C_{CB1}$ (fF) | $C_{CE1}$ (fF) | $C_{BE2}$ (fF) | $C_{CB2}$ (fF) | $C_{CE2}$ (fF) |
| 3.2 | 0.6 | 4.8 | 0.1 | 4.4 | 1 |
| $R_{BE1}$ (Ω) | $R_{CB1}$ (Ω) | $R_{CE1}$ (Ω) | $R_{BE2}$ (Ω) | $R_{CB2}$ (Ω) | $R_{CE2}$ (Ω) |
| 0.1 | 0.5 | 0.1 | 0.1 | 0.1 | 0.1 |

Figure 2.13 Modeled PA schematic and corresponding extracted parameter table

which are S(1,1) and S(2,2), having a maximum 2 dB difference at 200 GHz. In Fig. 2.16, S(2,1) values can be seen for the model and EM. Finally, in 2.17, a comparison of PAE and $\eta$ can be seen, where around 2% optimistic difference in the model can be observed.

One of the key advantages of the model is that, once the values are appropriately assigned with physical correspondence, it enables a more efficient understanding of design trade-offs. In a conventional core layout design, multiple interconnect configurations are typically explored, such as deciding which metal layer to route signals through, how many vias to use, or how long the interconnect paths should be. These decisions usually require extensive EM simulations, which are computationally demanding given the high operating frequency. Furthermore, for accurate harmonic balance simulations that capture the true large-signal behavior of the circuit, the analysis must be extended to at least the second and third harmonics, if not higher. For a circuit operating at a center frequency of 160 GHz, this implies EM simulations must also be performed at 320 GHz and 480 GHz, further increasing computational requirements. By utilizing a lumped component model, harmonic effects up to the nth order can be evaluated without additional simulation overhead. Beyond accelerating the design process, this approach also offers greater insight into the internal node behavior and clarifies the underlying design trade-offs. In Fig. 2.18, the intermediate inductor $L_3$ is swept to evaluate its impact on efficiency and gain.

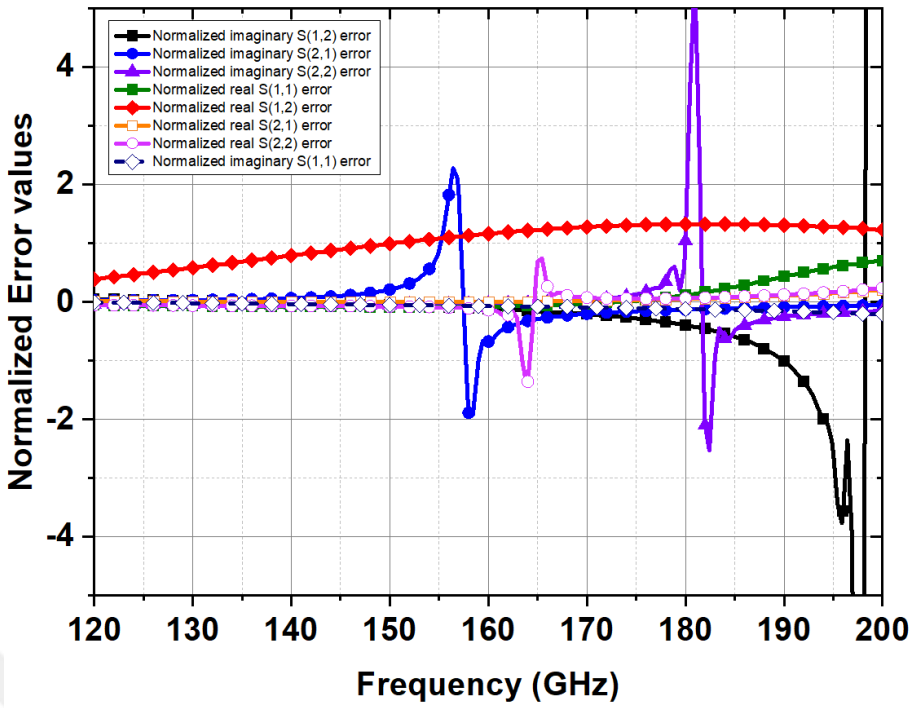



Figure 2.14 Normalized error values vs frequency

The efficiency peaks around 3 pH and decreases as the inductance increases, while the gain exhibits a slight improvement with higher inductance values. In Fig. 2.19, a sweep of the series resistance $R_3$ associated with $L_3$ is performed over a range from 1 Ω to 5 Ω. Increasing $R_3$ leads to a reduction in PAE, accompanied by a marginal increase in gain. In Fig. 2.20, the gain peaks around 60 fF, whereas the efficiency peaks around 20 fF, so that an intermediate value can be chosen. These sweeps illustrate how the selected components contribute to steering the output matching toward the optimal point without introducing significant loss. While the combined effect of these elements may shift the matching closer to or further from the ideal point, the individual sweeps offer valuable insight into which components are suitable for local resonance. Naturally, these components also influence the S-parameters, which are analyzed in detail in (Singh et al., 2023).

### 2.4.2 Circuit Design

A differential architecture along with cascode has been selected because of the reasons discussed in the preceding subsection. In Fig. 2.21, a simplified single stage of the core of the design is illustrated. To bias the base of the transistor, a 5k Ω resistor value was used, which is going to behave like an open because, as also seen

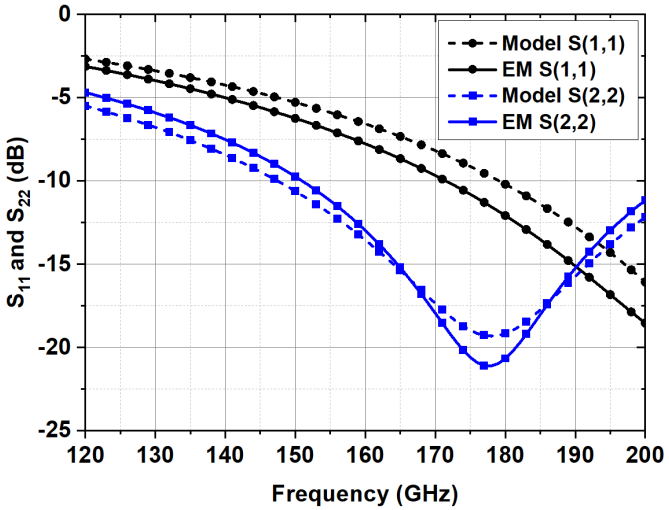



Figure 2.15 Model and EM return loss values in dB vs frequency

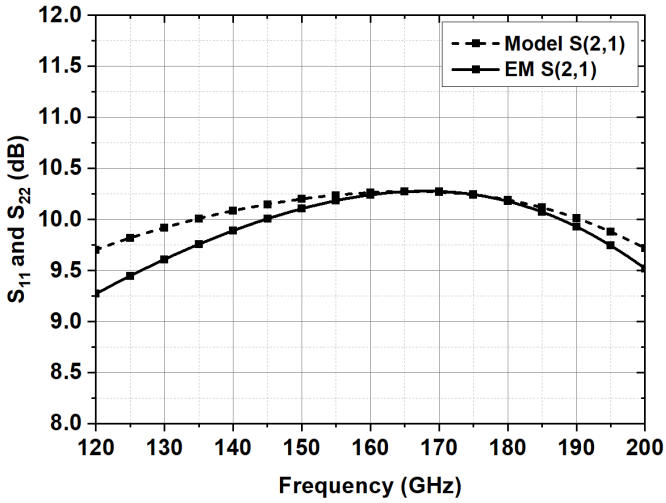



Figure 2.16 Model and EM gain values in dB vs frequency

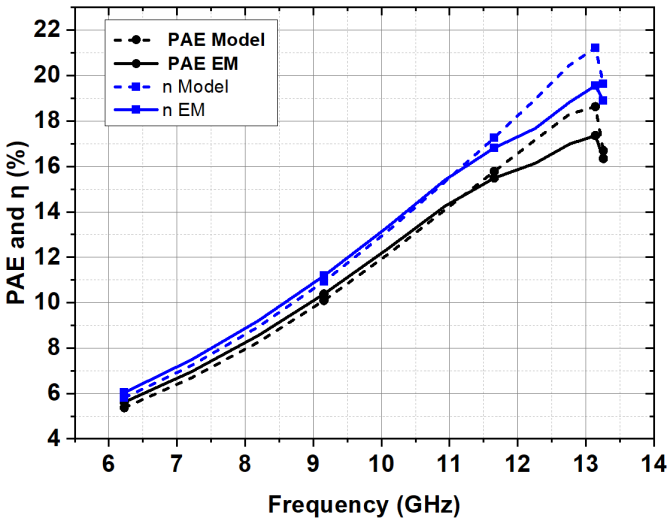
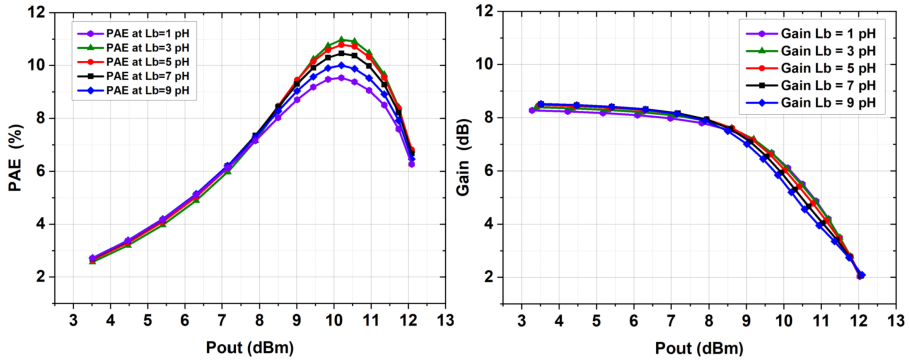
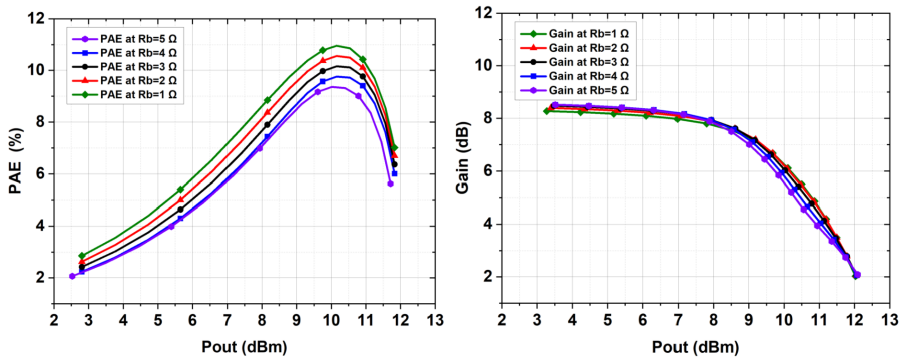



Figure 2.17 Model and EM PAE and n values vs $P_{out}$




(a) (b)

Figure 2.18 $L_3$ values sweep for (a)PAE (b)Gain vs frequency




(a) (b)

Figure 2.19 $R_3$ values sweep for (a)PAE (b)Gain vs frequency

on Fig. 2.22, base resistance in the range of 2 to 30 ohms compared to the bias resistor placed has 3-4 orders of magnitude larger. Also, some MOM capacitors are used to ground the RF, which, as discussed previously, influences gain and PAE.

In Fig. 2.24, the two-stage PA design with matching networks is illustrated, consisting of a Driving Amplifier (DA) and a PA. The transistor sizing in both stages is optimized to maximize $P_{out}$ and PAE. The DA stage draws 7.5 mA per differential arm, while the PA stage draws 22 mA per differential arm, which are sized with an emitter finger number of 3 and 10, respectively, to allow desired current levels. The stages are designed such that the OP1dB of the first stage occurs 2–3 dB before the input 1 dB compression point (IP1dB) of the second stage, allowing a larger voltage swing compared to equal OP1dB allocation across stages. This approach reduces the current required in the first stage, resulting in improved overall compression performance. To better show the benefit of non-uniform current allocation and staged linearity distribution, an example from (Voinigescu, 2013) can be considered. In this example, a three-stage amplifier is analyzed, where each stage initially provides 10 dB of gain with an OP1dB of 10 dBm. Applying the cascaded linearity equation

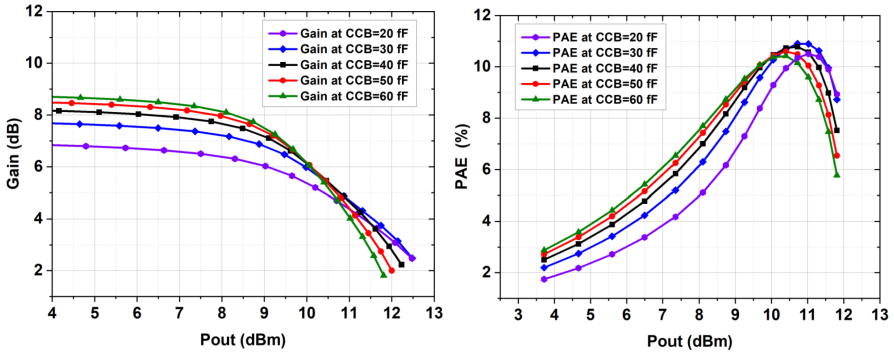



Figure 2.20 $C_4$ values sweep for (a)PAE (b)Gain vs frequency

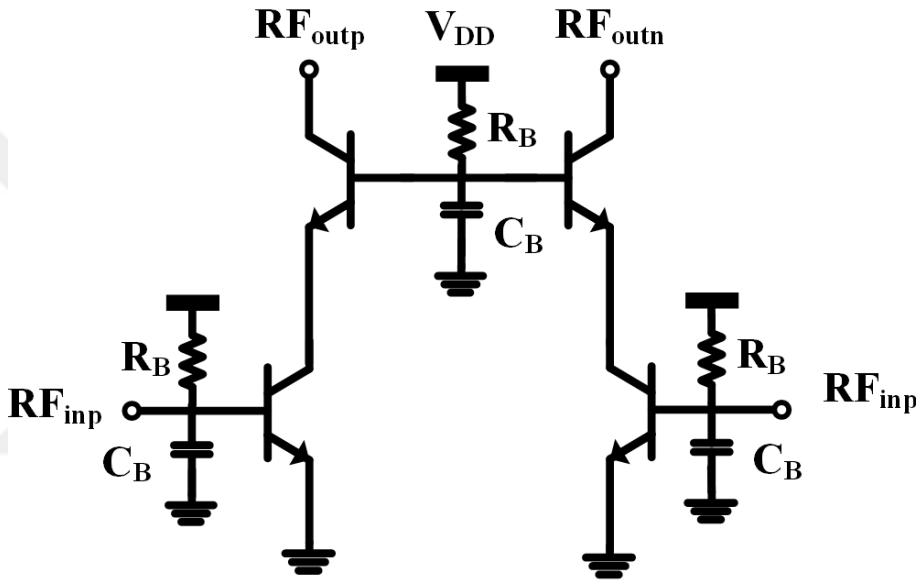



Figure 2.21 Schematic view of the single-stage G3 core

given in (2.16), the overall OP1dB is calculated as 9.33 dBm. Subsequently, while maintaining the same total gain of 30 dB and constant overall DC current, the current is redistributed by increasing it by a factor of 10 from stage 1 to stage 3. This results in OP1dB values of -5.7 dBm, 4.3 dBm, and 14.3 dBm for the first, second, and third stages, respectively. With this redistribution, the overall OP1dB remains at 9.33 dBm, while the third stage handles approximately three times the voltage swing compared to the uniform current allocation scenario.

$$\frac{1}{OP_{1\mathrm{dB}_{cascade}}} = \frac{1}{OP_{1\mathrm{dB}_3}} + \frac{1}{OP_{1\mathrm{dB}_2} \cdot G_3} + \frac{1}{OP_{1\mathrm{dB}_1} \cdot G_2 \cdot G_3}. \tag{2.16}$$

At this stage, the concept of Load-Pull is introduced. It involves sweeping the load impedance seen by the amplifier, typically visualized on the Smith chart, to

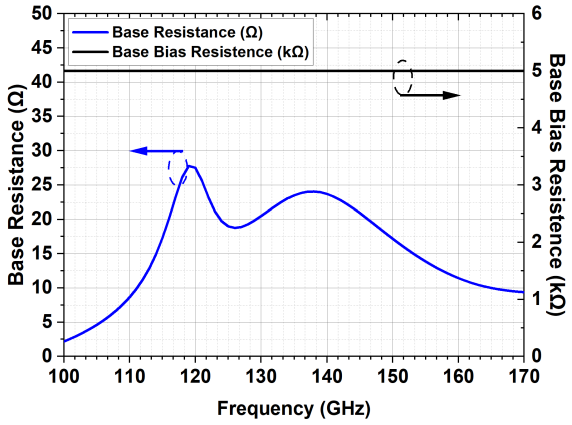



Figure 2.22 Base resistance vs base bias resistor value vs frequency (GHz)

evaluate performance metrics such as $P_{out}$, PAE, or linearity. Both DA and PA have optimal load values that maximize efficiency. Fig. 2.23 shows the Load-Pull efficiency contours of the standalone DA and PA under different compression levels. For the DA, the transistor is compressed by 3 dB, corresponding to an OP1dB of 7 dBm. As discussed earlier, PAE depends on the level of compression and is optimized at the load $Z_{Load}$ = 19 + j25 ohms, which is targeted at the DA output. Similarly, the PA reaches its peak efficiency at $Z_{Load}$ = 14 + j41 ohms, as observed in its Load-Pull results. In Fig. 2.24, the complete schematic of the overall structure is shown. The output matching network is designed to present the most efficient load to the PA. Similarly, the interstage matching network provides the optimal load for the DA output. The input matching network transforms the DA input impedance to 100 ohms, which is then converted to 50 ohms (single-ended to differential) for measurement compatibility, as measurement equipment typically operates at 50 ohms.

The whole layout and micrograph of the PAs are shown in Fig.2.25, where the transmission lines are implemented using Top metal 2, with metal 4 serving as the ground plane. The vertical spacing between these layers is approximately 7 $\mu$m, and the upper metal layer has a thickness of 3 $\mu$m. Consequently, transmission lines with a width of 10 $\mu$m are employed. A similar T-network matching strategy is used for input, interstage, and output matching. To conserve area and maintain symmetry, the shorted stubs are curled inward in a W-shape. This configuration serves two purposes: first, it ensures that differential signals encounter a common ground by bringing the differential lines to a single meeting point; second, the W-shaped interstage and input matching network and 8-shaped output matching network reduce the required footprint. Also, increased parasitic capacitance of the signal lines,

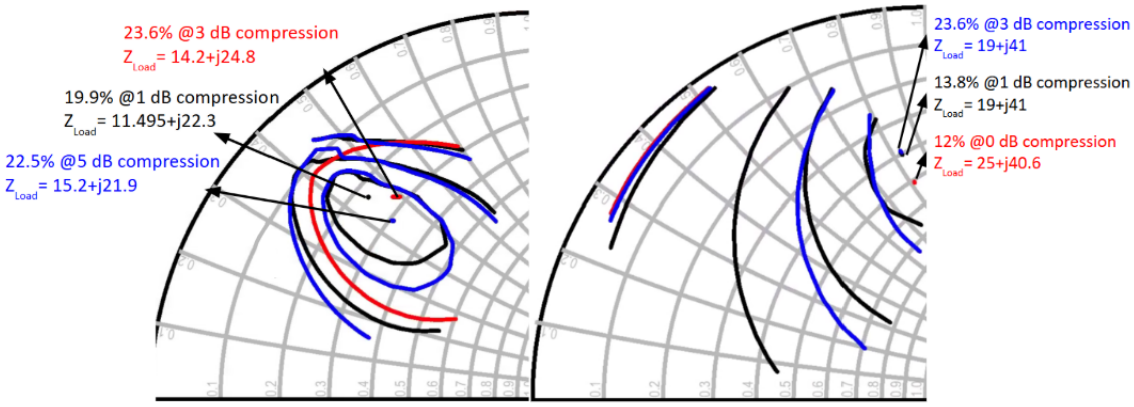



Figure 2.23 Simulated load pull values of DA and PA under different compression conditions

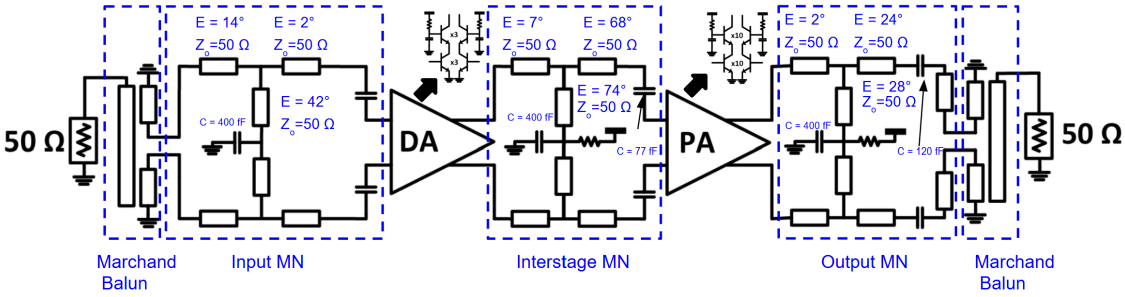



Figure 2.24 Schematic view of the two-stage PA

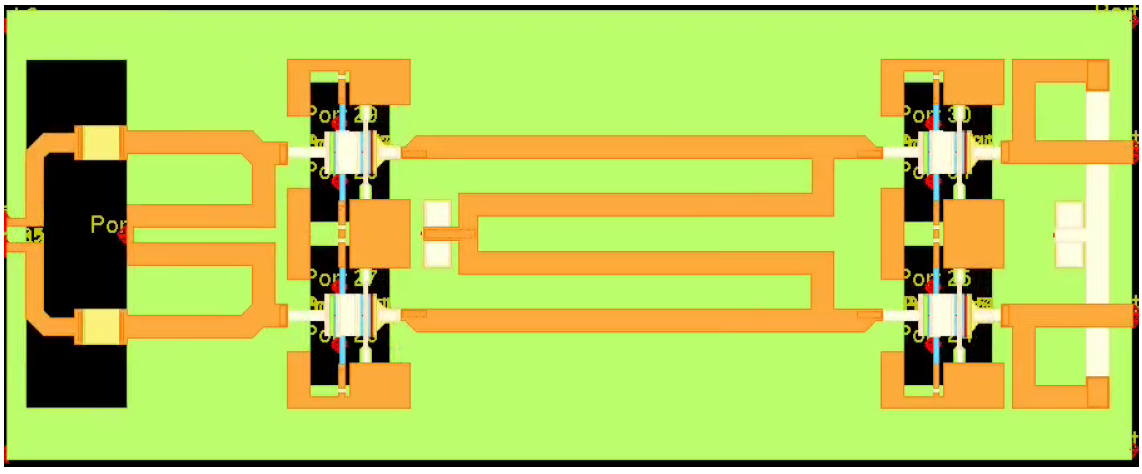


Figure 2.25 3D EM view of the PA

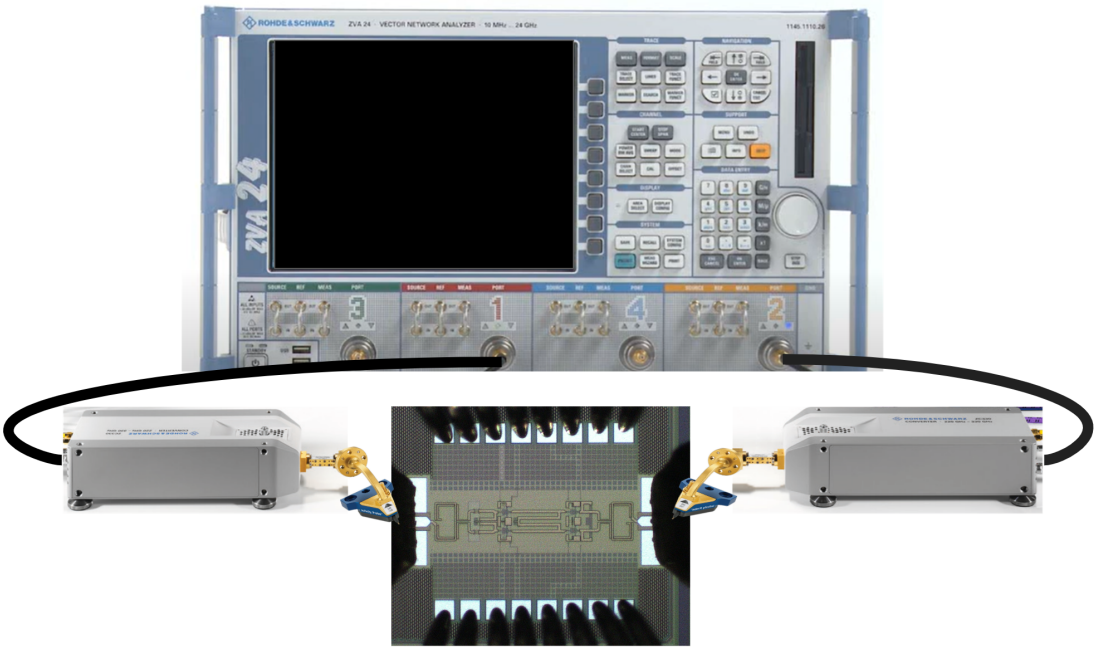



Figure 2.26 Small signal measurement setup probing on chip micrograph of PA

which effectively elongates the electrical length of the transmission lines without increasing their physical length, analogous to the behavior of slow-wave transmission lines, but in the horizontal direction.

### 2.4.3 Measurement Results

The measurement setup consists of a small signal and a large signal measurement setup. Small signal measurement setup can be seen in Fig. 2.26 where Rohde&Schwarz ZVA 24 vector network analyzer (VNA) was used, this device can take measurements up to 24 GHz at the input and outputs of the VNA, Rohde&Schwarz ZC170 frequency extenders were use that takes the frequency up to D-Band frequencies which is connected to FormFactor Infinity Probes that can cover D-Band for probing on the chip. Finally, GGB multi-needle DC probes were used in the north and south directions of the chip to supply the DC voltages. Large-signal setup uses NRP170TWG thermal waveguide power sensor to capture output and input power, which enables the measurement of $P_{sat}$.

To measure a differential amplifier, either a differential measurement setup using differential probes must be used, or single-ended measurements can be performed with the help of a balanced-to-unbalanced (Balun) transformer. In our setup, we

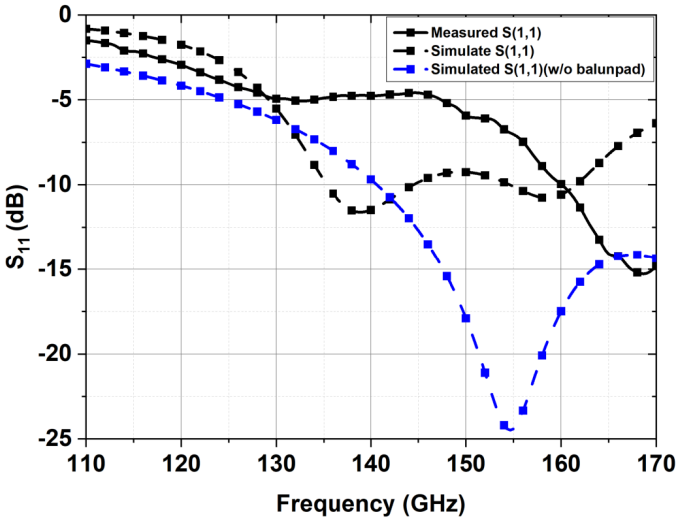



Figure 2.27 Input return loss vs frequency

used a Marchand Balun centered at 160 GHz to convert the single-ended signal to a differential one, along with a matched pad. Both the pad and the Balun introduce additional loss, which is de-embedded. In Fig.2.27, the input return loss performance of the PA is shown. The simulated S(1,1) stays below –10 dB from 142 GHz to 170 GHz. Since the measurements include the pad and Balun, it is more relevant to observe the S(1,1) with these components included. At 160 GHz, the measured and simulated S(1,1) with pad and Balun show good agreement, although there is a frequency shift across the band. In Fig. 2.28, the output return loss performance can be seen, where pad and Balun measurements agree with each other. Also, S(2,2) performance is a bad match, which is done on purpose to achieve better efficiency in the amplifier. In Fig. Z, the small signal gain performance of the amplifier, along with the back-to-back Balun-pad measurements, can be seen. There is a pretty good agreement with simulation results for both Balun and pad included or deembedded. The peak gain is 20.8 dB at 158 GHz with a 3 dB bandwidth of 26 GHZ, including the frequencies 143-169 GHz.

In Fig. 2.30, the measured and simulated gain and PAE are plotted. The simulated large-signal gain is 22 dB, while the measured gain is 21.4 dB at zero dBm input power, indicating good agreement between simulation and measurement. The simulated PAE peaks at 20.3% at a $P_{out}$ of 16.5 dBm, whereas the measured PAE reaches 19.73% at 17 dBm $P_{out}$, showing a slight shift in the PAE peak value.

In Fig. 2.31, the frequency-dependent performance of the measured PA is presented. Several local maxima in PAE are observed, specifically 19.66% at 150 GHz, 19.73% at 158 GHz, and 18.68% at 166 GHz—each representing state-of-the-art efficiency values. The corresponding PAE at the 1 dB compression point (PAE1dB) for these

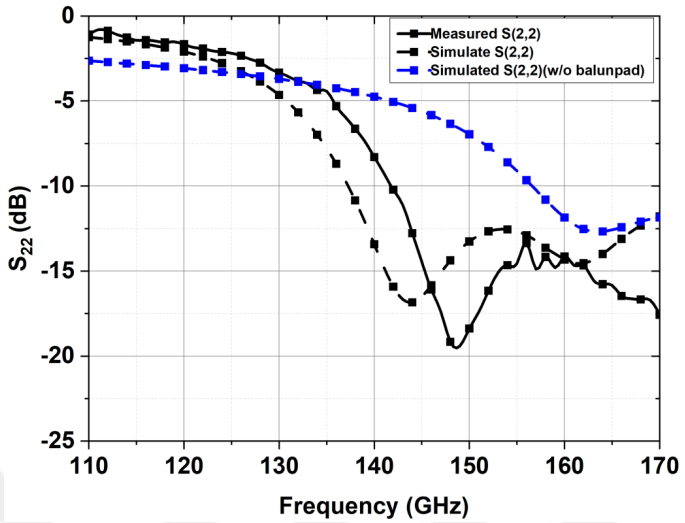



Figure 2.28 Output return loss vs frequency

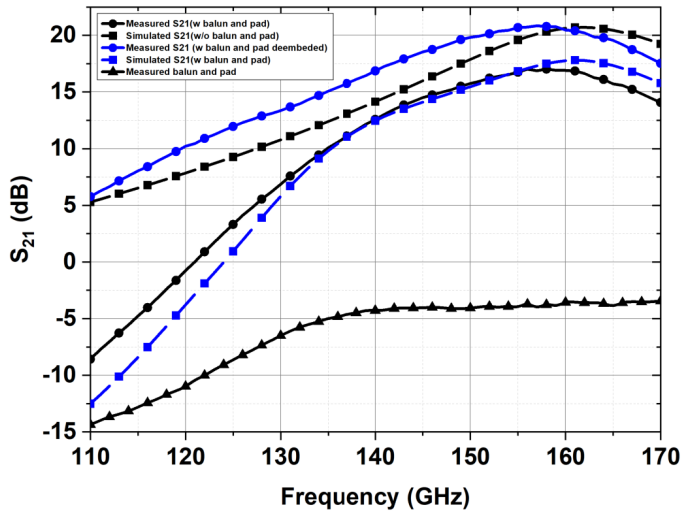



Figure 2.29 Gain vs frequency

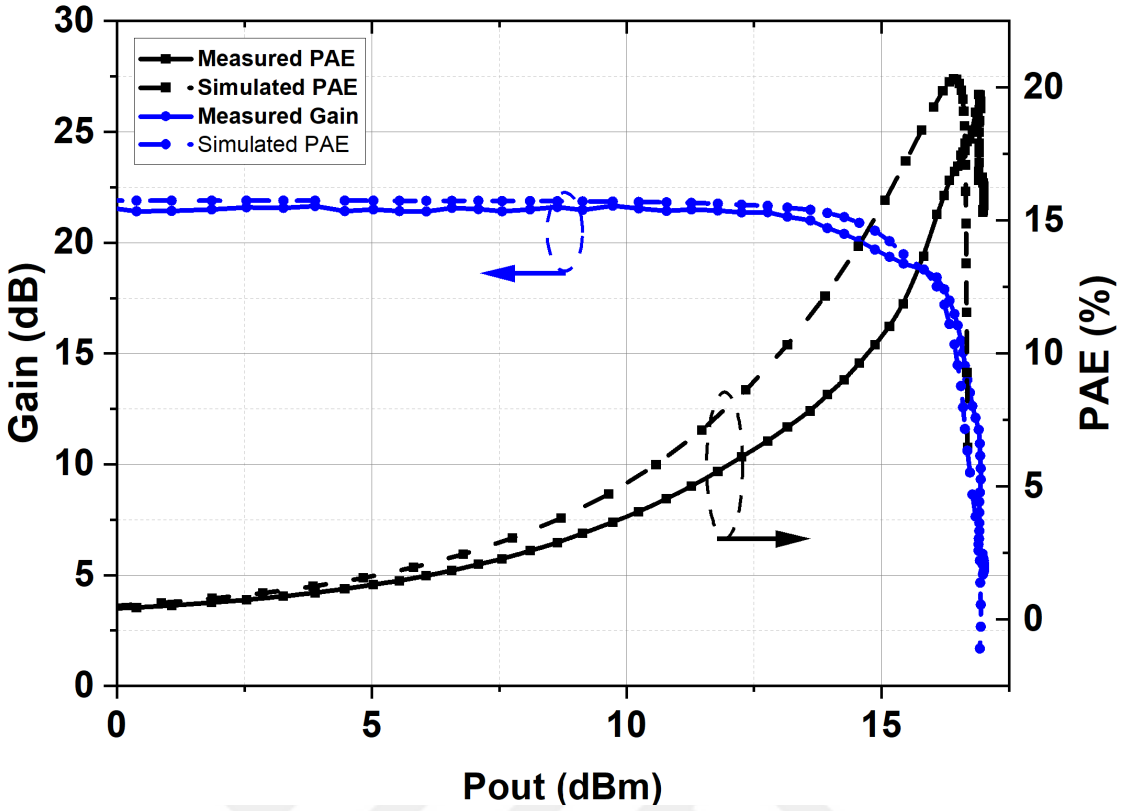



Figure 2.30 Measured and simulated PAE (right) and gain (left) values vs $P_{out}$

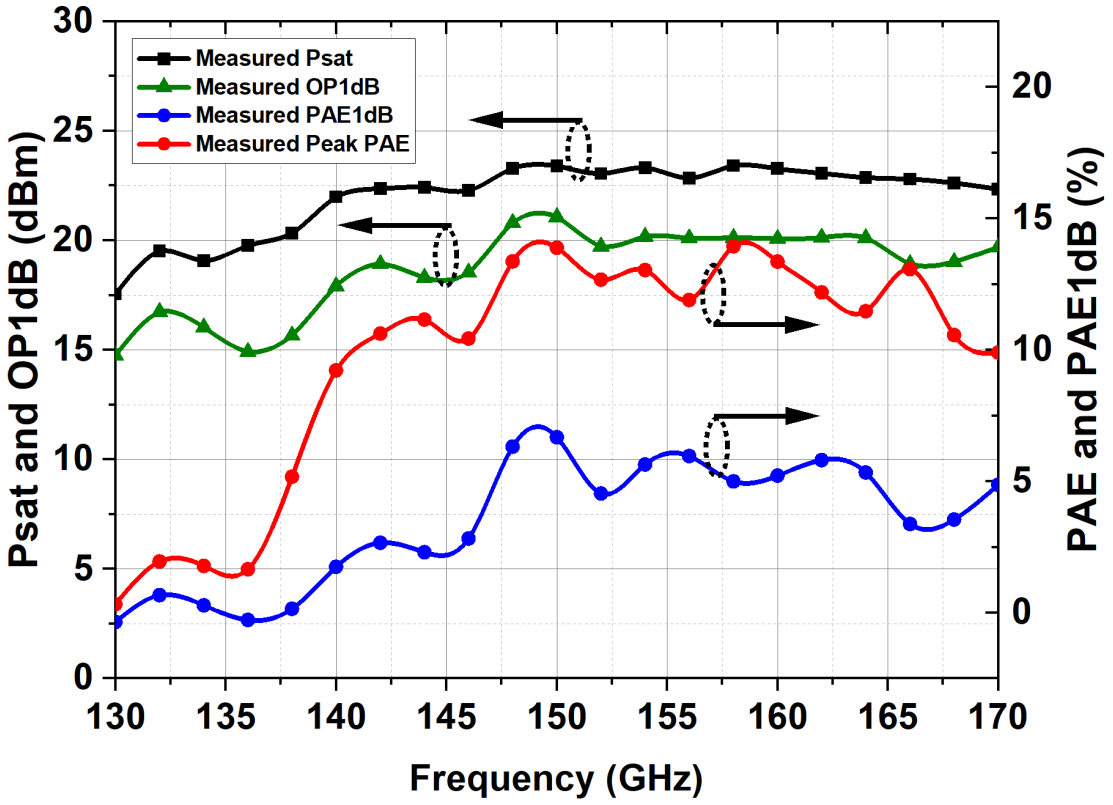



Figure 2.31 Measured PAE, PAE1dB, $P_{out}$, and OP1dB values vs $P_{out}$

frequencies is 11%, 9%, and 7%, respectively. The Psat remains relatively flat across the 142–170 GHz range, varying between 16–17 dBm, with a peak value of 17 dBm at 158 GHz. Similarly, OP1dB exhibits a flat response from 148–170 GHz, ranging between 14–15 dBm, with a maximum of 15 dBm at 150 GHz and a value of 14.2 dBm at 158 GHz.

## 2.5 Power Combined Power Amplifiers

Power combining is employed to increase the $P_{out}$ by aggregating the output of multiple PA blocks. At higher frequencies, the maximum achievable power from a single device becomes limited due to scaling constraints. Increasing $P_{out}$ typically requires enlarging the device size, which in turn increases parasitic elements, particularly capacitance. At high frequencies, even small parasitic capacitances significantly degrade performance, thus limiting the extent to which device scaling can be utilized. To overcome this limitation, power combining techniques are used. In an ideal scenario, where the combiner introduces no additional loss, combining two identical PAs yields a 3 dB increase in $P_{out}$ while maintaining the same PAE, as both the $P_{out}$ and the DC power consumption double relative to a single PA.

In this section, power combining of multiple amplifiers is presented. The PA stages are implemented using the same methodology described in the previous section; however, a different process is explicitly employed, the IHP SG13G2 technology, which offers an $f_T/f_{MAX}$ of 300/500 GHz. While the overall design approach remains consistent, there are subtle differences compared to the previous implementation, such as the use of a single-ended architecture. The discussion begins with the design of the first PA stage, followed by an overview of the power combining technique. Finally, simulation and measurement results are presented and discussed.

### 2.5.1 Two Stage Single Ended PA Design

A single-ended design was preferred over a differential implementation to reduce the complexity of the power combining network, as shown in Fig. 2.32. A two-stage cascode topology is employed. The sizing and biasing of the transistors follow the

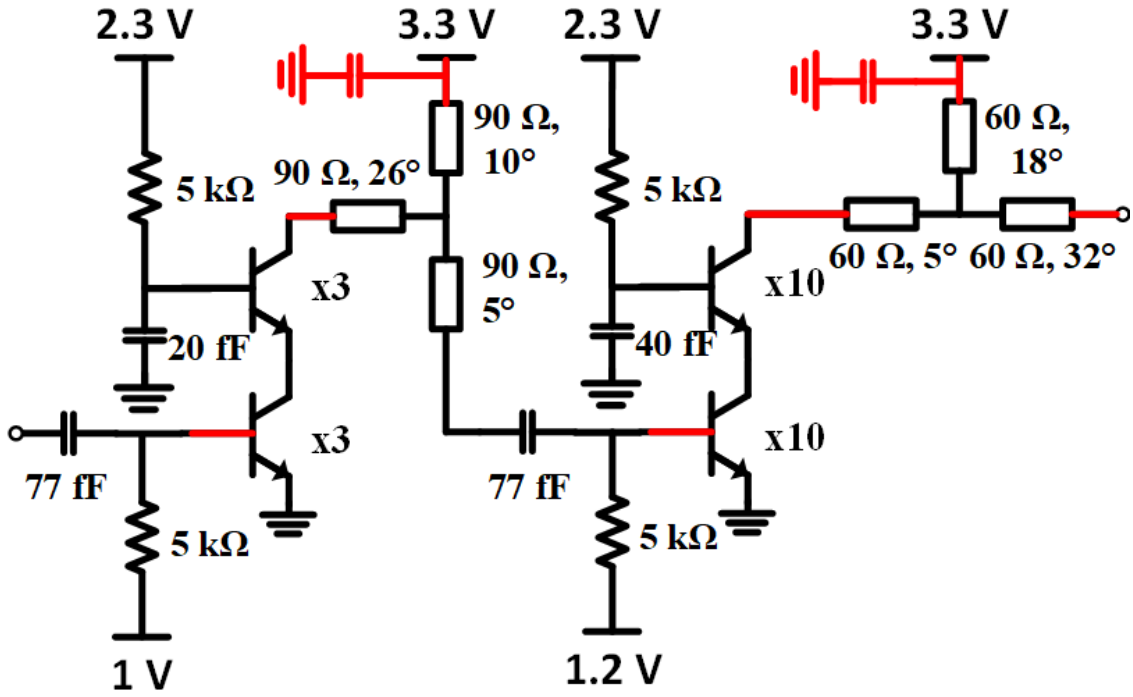



Figure 2.32 Schematic view of the two-stage PA

same approach used in the previous design, aiming to optimize the compression point for both the DA and PA, thereby maximizing efficiency. Core optimization methodologies discussed earlier were applied at this stage. Both the interstage and output matching networks utilize T-networks, consisting of a series–shunt–series transmission line configuration placed adjacently.

### 2.5.2 Power Combining Network

The power combining network should exhibit low insertion loss and wide bandwidth, as excessive loss directly reduces both the $P_{out}$ and overall efficiency. For instance, in an ideal scenario, combining two identical PAs would result in a 3 dB increase in $P_{out}$. However, if the combining network itself introduces a 3 dB loss, this gain is nullified, effectively negating the benefit of power combining while significantly degrading efficiency due to increased power dissipation. Therefore, minimizing insertion loss in the combining network is critical. Additionally, if the PA exhibits wideband performance but the combiner is narrowband, the overall system bandwidth becomes limited by the narrower component, undermining the wideband advantage of the amplifier design. To achieve low-loss performance, a broadband coupler was

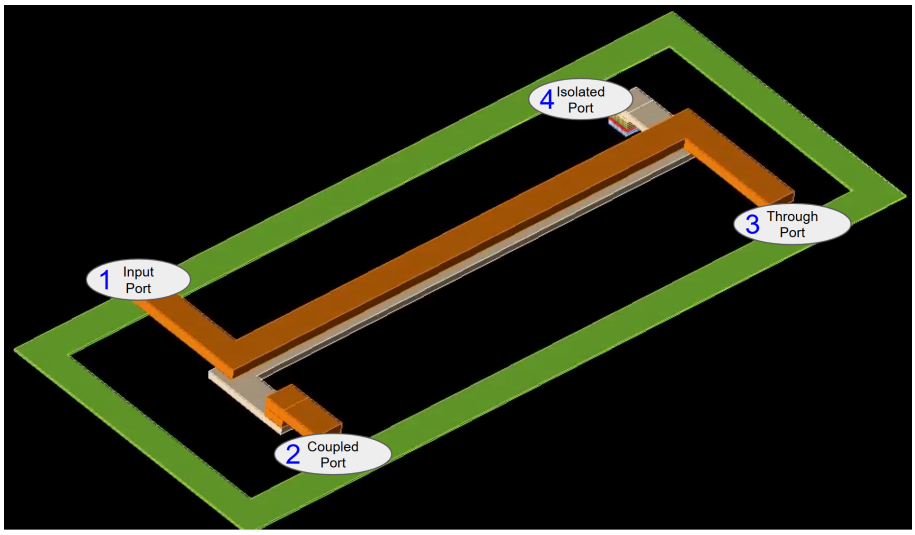



Figure 2.33 Broadside coupler 3D layout view

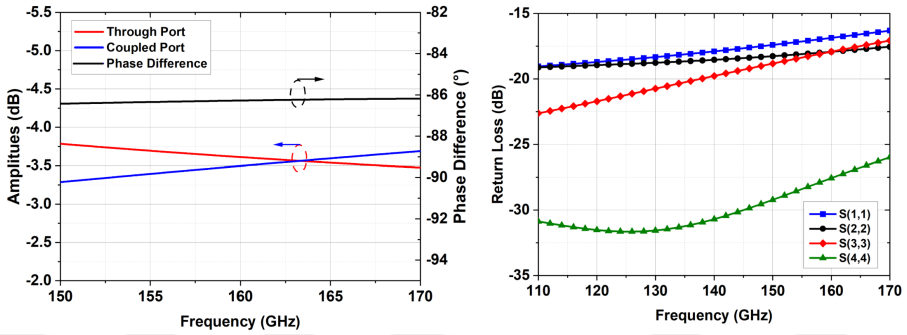



Figure 2.34 Coupler amplitudes for through and coupled and their phase differences(left), return loss values for each port (right)

employed, as illustrated in Fig. 2.33. The coupler is implemented using two stacked metal layers, TM2 and TM1. The transmission lines are arranged directly above each other and extended to provide an electrical length of 90 degrees at 160 GHz, thereby utilizing broadside coupling. The vertical spacing between TM2 and TM1 is approximately 2 $\mu$m, which facilitates efficient electromagnetic coupling. This configuration results in a 90-degree phase shift and enables equal power splitting between the coupled paths. The performance of the coupler is shown in Fig. 2.34. The 3 dB amplitude observed is inherent to the equal power division between the two output ports. The additional loss—attributed to insertion loss—is centered around 162 GHz and remains approximately 0.5 dB. Within the frequency range of 150–170 GHz, the amplitude variation remains within 1 dB. The phase difference between the coupled and through ports is approximately 86°, with less than 1° variation across the same bandwidth. Additionally, all ports exhibit return loss values better than 15 dB.

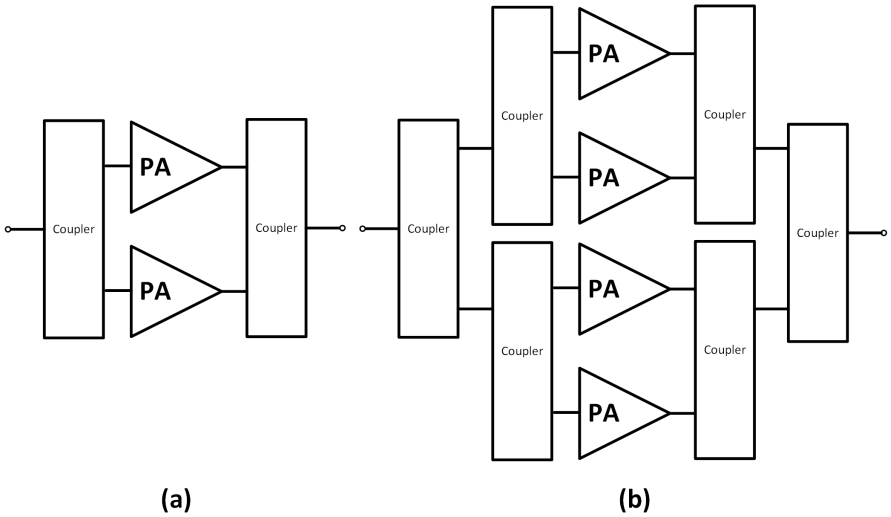



Figure 2.35 Block diagrams of (a) 2-way combined PA and (b) 4-way combined PA

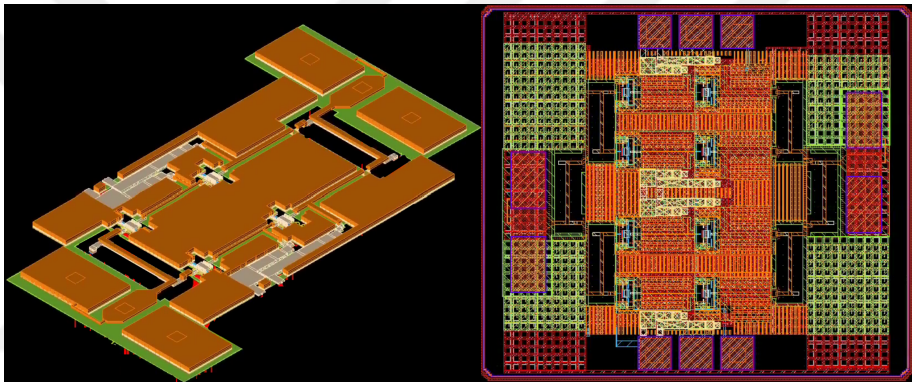


Figure 2.36 Block diagrams of (a) 2-way combined PA and (b) 4-way combined PA

### 2.5.3 2-way and 4-way Power Combined PAs

In this work, two standalone PAs are combined to implement a 2-way power-combined PA, and subsequently, two of these 2-way combined PAs are further combined to realize a 4-way power-combined PA. The block diagrams of the combined architectures are shown in Fig. 2.36. Power combining at each stage is achieved using couplers presented in the prior subsection, selected for their low insertion loss and favorable phase characteristics.

3D views of the 2-way combined PA and final layout, ready for tapeout, are shown in Fig. 2.36. For both of the layouts, many mim capacitors are used for short subs that bias the circuit through interstage and output matching. To properly short a variety of frequencies, a range of capacitors with different values ranging from 55 fF to 2.4 pF are utilized. The PAs are spaced away from each other according to the spacing that couplers need for the power combined PAs.

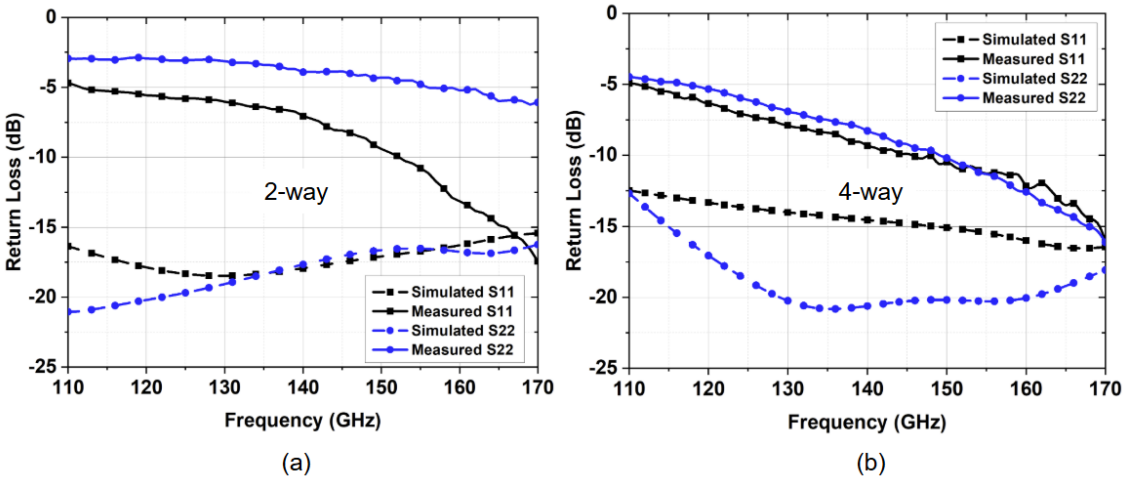



Figure 2.37 Return loss vs frequency of (a) 2-way combined PA and (b) 4-way combined PA

### 2.5.4 Simulation and Measurement Results

The measurements were conducted using the same setup as in the previous block. For small-signal characterization, a 24 GHz VNA and D-band extenders were again used, along with DC probes. The DC currents drawn from the circuits in simulation and measurement were 54 mA and 48 mA, respectively, for the 2-way PA, and 55 mA and 108 mA, respectively, for the 4-way PA, indicating a variation between simulation and measurement. In Fig. 2.37 2 2-way and 4-way return loss values are shown for both of the amplifiers. Despite remaining under 15 dB for the desired operation frequency for both PAs, the measurement results do not support the simulations. In Fig. 2.38, gains of the PAs are shown, which also do not map to having excessive loss. In Fig. 2.38, the gain results of the PAs are shown, which indicate that the performance does not align. In Fig. 2.39, the simulated efficiency results are presented, while in Fig.2.40, $P_{out}$ simulation results are shown without corresponding measurements. Since only small-signal measurements were conducted, which disagreed with the measurements, large-signal measurements were not pursued. Simulations reveal that, despite using low-loss couplers, the additional loss in the 4-way configuration causes a slight drop in efficiency, decreasing from 14.3% to 11.32% compared to the 2-way case. However, thanks to the added power combining, the $P_{out}$ increases by nearly 3 dB.

There are several reasons why the em-simulated PAs did not map to the measurement results. The reasons consist of several reasons, which are that the structure being simulated is limited to a single two-stage PA. At the same time, the remaining sections were assembled in the schematic using corresponding EM sub-blocks. This

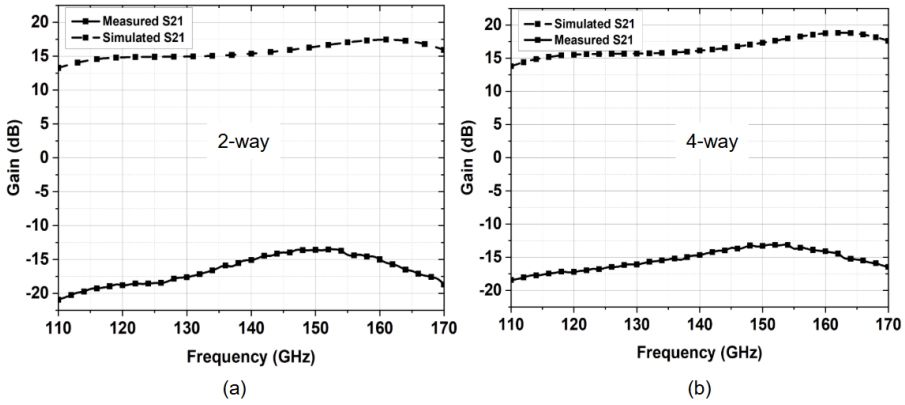



Figure 2.38 Gain vs frequency of (a) 2-way combined PA and (b) 4-way combined PA

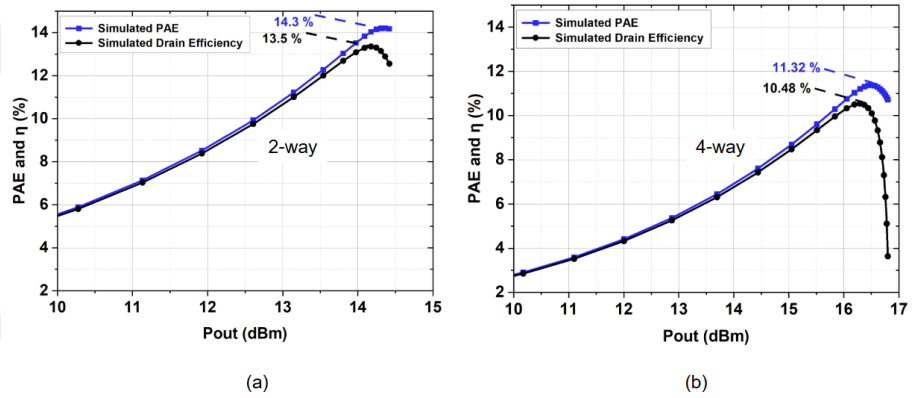



Figure 2.39 PAE and $\eta$ vs $P_{out}$ of (a) 2-way combined PA and (b) 4-way combined PA

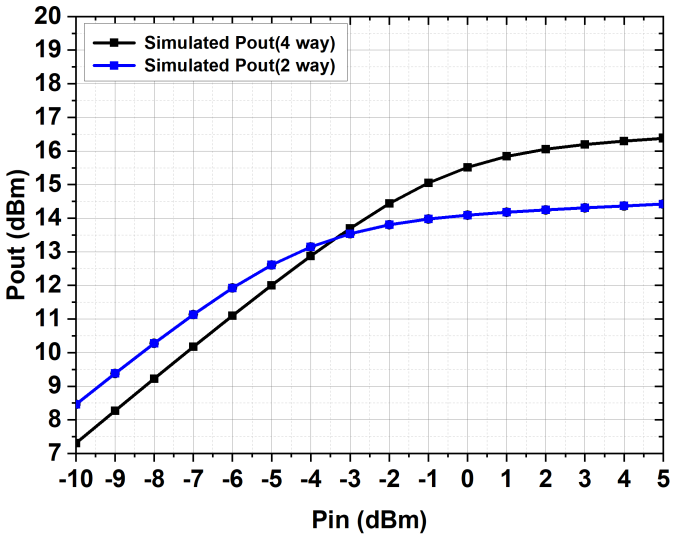



Figure 2.40 $P_{out}$ vs $P_{in}$ of (a) 2-way combined PA and (b) 4-way combined PA

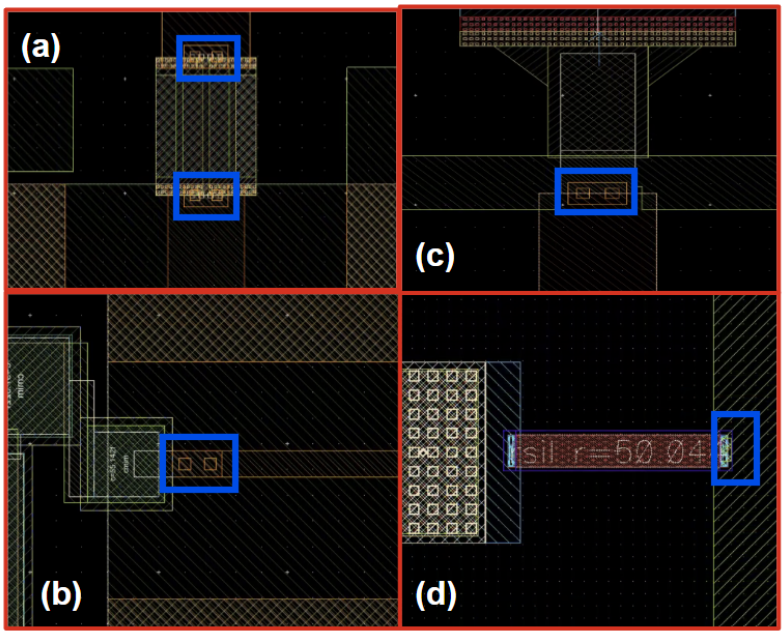



Figure 2.41 Small via connection examples in the circuit

approach did not account for integration losses, particularly those introduced by the connection vias. These vias were designed to be very small, which introduced excessive resistance and inductance. Ideally, vias should be made large enough to parallel their resistance and inductance, thereby minimizing their parasitic effects—an aspect that was neglected in the design. In Fig.2.32, the red lines indicate the regions where narrow vias were used, which contributed to performance degradation. Moreover, the output via was not included in the EM simulation, which significantly affected the overall performance. Fig.2.41 shows zoomed in view in parts of the layouts to capture some via connections that are located at: (a) the output-dc block capacitance-output coupler path (b) dc block capacitors connection at output stage (c) input coupler connection to the DA (d) coupler's resistance connection to the ground which via connections are ensquared in blue. Another reason is that, as also seen in Fig. 2.41, coupler resistance is connected by a single 50 ohm, which will lead to variations. One primary source of discrepancy arises from the MIM capacitor connections at the ends of the short stubs, as shown in Fig. 2.42. In the circuit, the MIM capacitor is implemented between TM1 and M4. The top and bottom views in the figure show that the top and bottom metal of the capacitor are interconnected. TM1 is appropriately connected, but M4 is connected through thin metal traces. This results in a poor connection to the ground. Consequently, at the ends of the shunt stubs, there is effectively no proper grounding, which disrupts the circuit's matching and severely degrades performance.

PAs are compared in 2.1

Table 2.1 Comparison with the state-of-the-art PAs

| **References** | **Frequency (GHz)** | $P_{sat}$ **(dBm)** | **PAE**$_{max}$ **(%)** | **Gain (dB)** | **3dB-BW (GHz)** | **Area (mm$^2$)** | **Technology** |
|---|---|---|---|---|---|---|---|
| Al-Eryani et al. (2016) | 161 | 18.1 | 12.4 | 30.7 | 40 | 0.42 | 130 nm SiGe |
| Li et al. (2022) | 160 | 18.0 | 9.4 | 24.0 | 20 | 0.84 | 130 nm SiGe |
| Sarmah et al. (2013) | 135–170 | 14–17 | 1.6 | 5–8 | 35 | 0.57 | 130 nm SiGe |
| Furqan et al. (2017) | 131–180 | 14.0 | 5.7 | 27.0 | 50 | 0.48 | 130 nm SiGe |
| Al-Eryani et al. (2016) | 155–165 | 14.0 | 4.8 | 35.4 | 10 | 0.068 | 130 nm SiGe |
| Kucharski et al. (2019) | 155–180 | 18.0 | 4.0 | 30.2 | 25 | 0.85 | 130 nm SiGe |
| Daneshgar & Buckwalter (2018) | 120 | 22 | 3.6 | 7.7 | 35 | 0.79 | 130 nm SiGe |
| Zhang et al. (2023) | 140 | 16.2 | 8.6 | 22.6 | 28 | 0.99 | 28 nm SOI CMOS |
| Li & Rebeiz (2021) | 140 | 16.0 | 12.5 | 22.2 | 21 | 0.43 | 45 nm SOI CMOS |
| This Work (2-way PA) | 160 | 14.5 | 13.5 | 18.0 | 49 | 0.54 | 130 nm SiGe |
| This Work (4-way PA) | 160 | 16.4 | 10.5 | 17.0 | 48 | 1.056 | 130 nm SiGe |
| This Work (PA) | 158 | 17.0 | 19.73 | 21.56 | 26 | 0.10 | 130 nm SiGe |

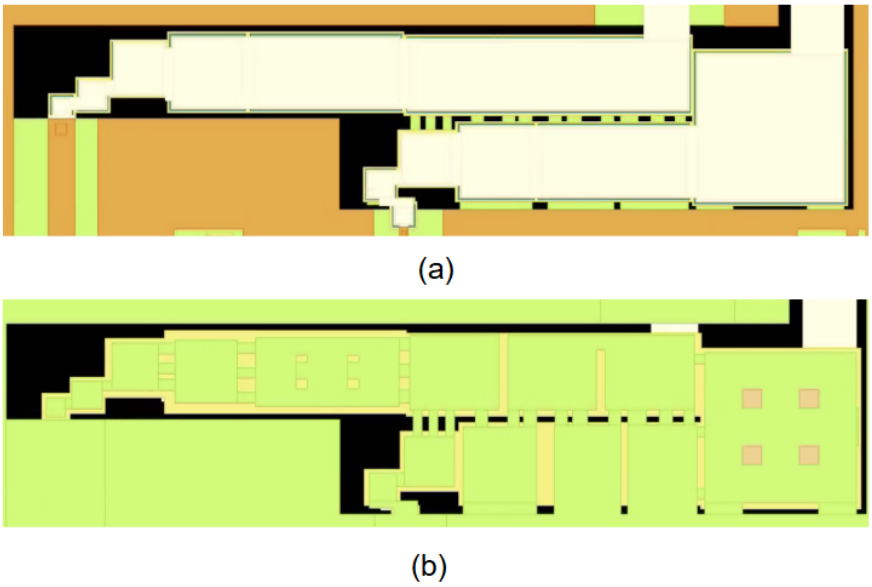



Figure 2.42 Bypass capacitor from (a) top (b) bottom

# 3. WIDEBAND SPDT SWITCH USING SOI PROCESS

Depending on the frequency of operation, several topologies are discussed in the literature. For lower frequency bands (DC to 120 GHz), the series-shunt topology with varying numbers of stacks is commonly used, depending on the required specifications. This topology typically provides improved isolation due to the series transistor, which introduces extra resistance in the off state. Several designs using the series-shunt topology have been reported in the literature. For instance, (Jin & Nguyen, 2007) utilized this topology with a single-stack series-shunt configuration and incorporated series inductors at all three ports to cancel parasitic capacitances. In another example, (Ohnakado et al., 2003) employed transistor stacking in combination with the series-shunt topology to achieve high linearity. However, these designs were limited in bandwidth due to high substrate coupling in their respective technologies. (Rack et al., 2022) leveraged state-of-the-art 22 nm FDSOI technology with substrate isolation rings to achieve performance up to 120 GHz, with more than 20 dBm input power at IP1dB, benefiting from transistor stacking. Meanwhile,(Cetinoneri et al., 2009) and (Min & Rebeiz, 2009) demonstrated single-pole four-throw (SP4T) switches operating up to 70 GHz. However, these designs suffered from high insertion loss (up to 3.5 dB) and persistent capacitive feedthrough issues. (Eltaliawy et al., 2020) presented a differential single-pole single-throw (SPST) switch with a neutralization technique to cancel feedthrough capacitances, achieving a very high isolation of at least 50 dB. However, this design only covers a frequency range from DC to 43 GHz. In summary, for frequencies beyond 120 GHz, employing the series-shunt topology remains challenging due to its inherent limitations. To achieve frequencies beyond 110 GHz, particularly in the D-Band and higher, removing series components is necessary. However, this removal would halve the impedance seen at the input port, requiring additional impedance matching. More importantly, the arm whose gate is excited would short the entire signal to ground. To address this, adding a quarter-wave transformer to each arm converts the RF short to an RF open on the off-arm, making it appear as if nothing is connected there, while converting the RF open to an RF short on the on-arm, allowing the signal to pass through. Several papers in the literature discuss vari-

ations of this topology. In the works by (Chen, Wang, Yao & Heydari, 2012) and (Uzunkol & Rebeiz, 2012), a quarter-wave shunt single-pole double-throw (SPDT) switch is implemented using a single shunt CMOS transistor and a shunt short stub to cancel out parasitics. This design minimizes insertion loss by using a single transistor. A similar structure can be found in (Ulusoy et al., 2014), where BiCMOS technology is utilized to achieve higher bandwidth. This paper also explores the use of reverse-saturated BiCMOS to reduce on-state resistance, thereby improving gain and isolation. (Cetindogan, Ustundag, Turkmen, Wietstruck, Kaynak & Gurbuz, 2018a) further explores the reverse-saturation concept with an additional output matching network to cover the entire D-Band. For better isolation, double-shunt devices are also used, although at the cost of reduced bandwidth due to the doubling of shunt devices, as demonstrated by (Schmid et al., 2014) and (Çağrı Ulusoy, Schmid, Kaynak, Tillack & Cressler, 2015) using CMOS. The traveling wave topology, which is an extension of the quarter-wave topology with three or more shunt devices, offers improved isolation. (Wu et al., 2021) presents this topology in an SPST switch reaching up to 220 GHz, leveraging a high-order circuit composed of an LC network. Additionally, (Lai, Chou, Huang, Huang & Chuang, 2017) discusses an SPDT switch version aimed at the W-Band, employing the traveling wave topology with transmission lines between sections to create an LC network effect. A magnetically switchable SPDT switch was realized within 220-285 GHz, which operates on the very high frequency side of the spectrum. Above all these mentioned switch topologies, each targeting different bands from DC to 285 GHz, there is not a switch that can cover all of these at once. One reason for not doing such a circuit is that it would cover the band but have limited performance for example a highest bandwidth according to literature done in this text is series shunt topology due to quarter-wave shunt having limitations due to quarter-wave transmission line, transformer based having limitations due to changing inductance and coupling with respect to frequency also magnetically switchable topology frequency having frequency limitations for the same reason. However, using a series shunt topology with a series transistor introduces a high loss, which is a key parameter in the switch design. In this section, we will introduce a series shunt switch with higher order matching to realize a DC-300 GHz working switch that can overcome topology loss limitations, and it is the highest frequency switch in the literature.

As discussed in the literature review, designs target different bands with as large a bandwidth as they can achieve because a switch is supposed to have a large bandwidth due to the applications that it might be used for. Let's say a dual band transceiver or a sub-block that will work in 30 GHz, 150 GHz and 300 GHz needs to be realize, it is challenging and requires various tradeoffs to be able to real-

ize such a wideband architecture therefore blocks that work in 30 GHz, 150 GHz and 300 GHz can be used alongside the DC-300 GHz switch that will enable all these bands. For example, in (Van Dijk, Patra, Subramanian, Xue, Samkharadze, Corna, Jeon, Sheikh, Juarez-Hernandez, Esparza, Rampurawala, Carlton, Ravikumar, Nieva, Kim, Lee, Sammak, Scappucci, Veldhorst, Vandersypen, Charbon, Pellerano, Babaie & Sebastiano, 2020), multiple bands are used, enabled by the switch incorporated in their system

## 3.1 Circuit Design

Switch transistors are operated in triode region for which drain to source voltage ($V_{DS}$) is lower compared to gate voltage ($V_G$) this way increasing $V_{DS}$ voltage will linearly increase the Drain current ($I_D$) passing through the circuit therefore act like a resistor, this is true for when there is a voltage applied that forms $R_{ON}$. When applied with a gate voltage value below threshold voltage ($V_{th}$), only parasitic capacitance values collectively form an overall capacitance $C_{OFF}$. The most crucial parameter in a switch design is the Ron*Coff parameter of the transistor, which is provided by the foundry. Alternatively, a two-port analysis of the transistor on a schematic can be made. Our design will be based on GF 130 nm technology, for which simulated $R_{ON}$*$C_{OFF}$ values can be simulated to end up with around 80 fS, which is suitable for a very large bandwidth design. To check this in simulations for both ON and OFF states of the circuit, a very large resistance needs to be biased to prevent RF leakage. The Y(2,1) parameters can be used to extract only the series resistance or capacitance value. Y(2,1) gives this value by finding the ratio of output current and input voltage while shorting the output, which effectively eliminates the effect of the shunt component and provides a pure series component. This is useful because we already know its shunt components are negligibly small.

In Fig. 3.1, the schematic view of the SPDT switch is shown at the top. Transistors $M_1$ to $M_7$ serve as series and shunt elements with varying stack numbers, while transmission lines are depicted with different lengths and characteristic impedances. The control voltages $V_G$ and $\bar{V}_G$ indicate complementary biasing—when one is high, the other is low—effectively turning devices on and off. Qualitatively, the operating principle is as follows: when $M_1$ is turned on, the shunt transistors on the same path are turned off, allowing signal transmission through that arm. Simultaneously, $M_2$ on the opposite path is turned off, and its corresponding shunt transistors are

turned on. Ideally, the off arm appears as an open circuit, ensuring isolation. This is true for the case where one arm has zero resistance and the other arm has zero capacitance; however, due to the existence of $R_{ON}$ and $C_{OFF}$, some of the signal is leaked to the off arm, creating isolation problems. While a fundamental feasibility analysis can be performed using $R_{ON}$ and $C_{OFF}$ at low frequencies, this design targets 300 GHz, where such schematic-level approximations become insufficient without incorporating layout parasitics. In Fig. 3.1, the layout view of the design is shown at the bottom, with the input port located on the left side and the output ports on the right. The metalization used for the layout includes one thick top metal layer named MA that has a thickness of 4 $\mu$m, and it is 3 $\mu$m away from the lowest metal, which is used as a ground layer, making the lines thinner compared to the metalization used in the previous chapter.

The main objective of the circuit is to achieve the broadest possible bandwidth. To this end, several techniques are employed, including transistor sizing, optimizing the order of the network, effective capacitance reduction, utilizing high-impedance and multi-section transmission lines, and optimizing the number of stacked transistors. Each of these approaches is detailed in the following subsections.

### 3.1.1 Transistor Sizing

Transistor sizing is significant in a switch, where $R_{ON}$ and $C_{OFF}$ of the device are determined. Let's first examine the series transistors $M_1$ and $M_2$ . Let $M_1$ be turned on hence be modeled as a $R_{ON}$ and $M_2$ be turned of hence be modeled as a capacitance. Increasing $R_{ON}$ will increase insertion loss because we are effectively increasing the resistance in that path also since device is symmetrical and $R_{ON}C_{OFF}$ is fixed for all devices, $C_{OFF}$ will decrease which means there is less of the signal will couple to the other side that will improve isolation. How about bandwidth? To better grasp this, we need to go to the Smith chart. In Fig. 3.3, the behavior of series resistance on a frequency variable impedance can be seen, where increasing the resistance from 25 to 100 ohms gradually decreases the change of imaginary part of the impedance on the Smith chart, which is the key for a wideband design. Therefore, the series $R_{ON}$ of 15 ohm resistors is utilized in our design, corresponding to a device size of 12 $\mu$m x 15 $\mu$m, which creates a larger capacitance at the off arm, that leaks some signal. For the shunt arms at $M_1$, reducing the device size means reducing $C_{OFF}$.

The sizing of the transistor not only matters due to its $R_{ON}$ $C_{OFF}$ values but also

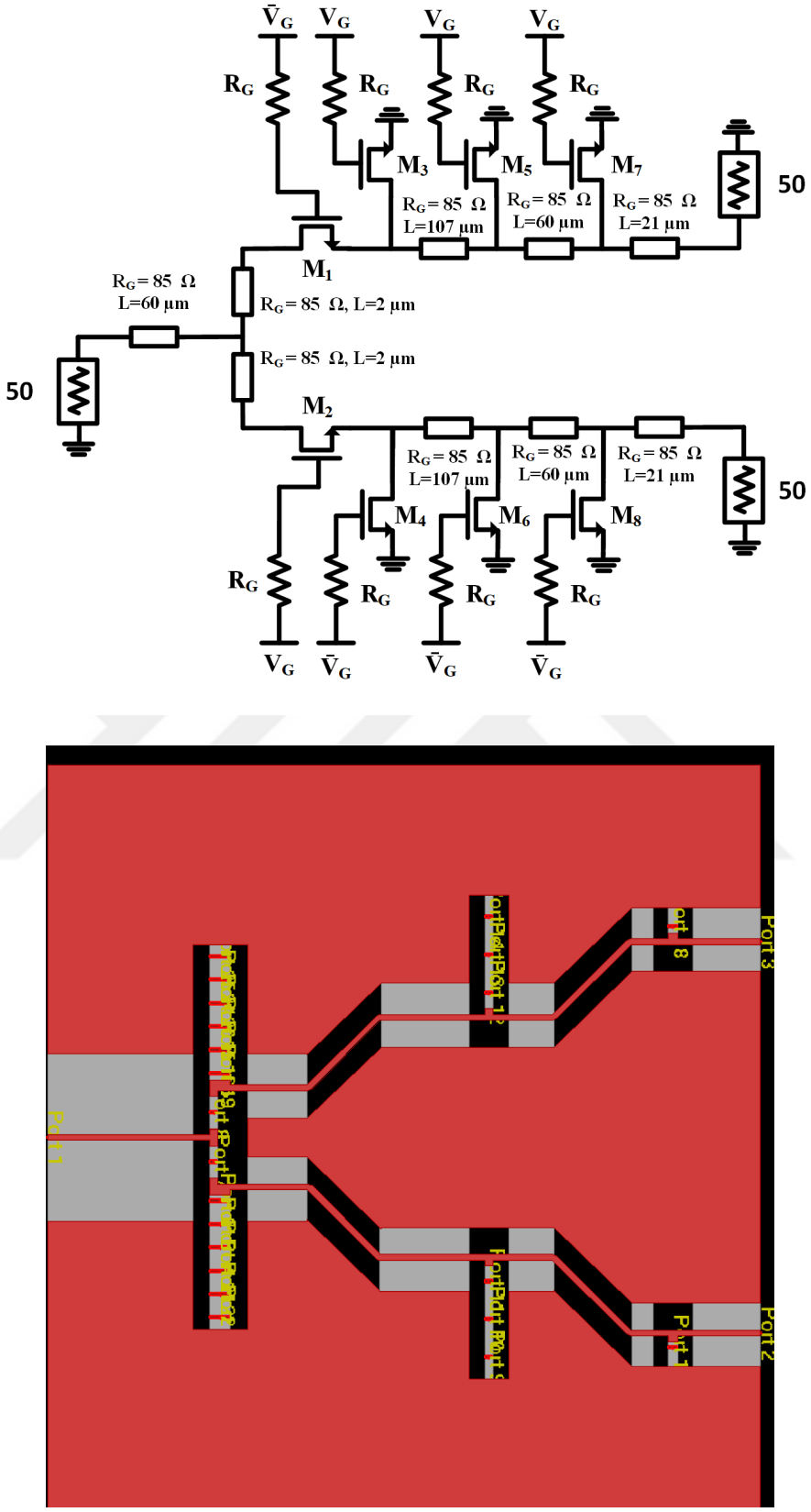



Figure 3.1 Schematic (top) and layout (bottom) view of the SPDT switch.

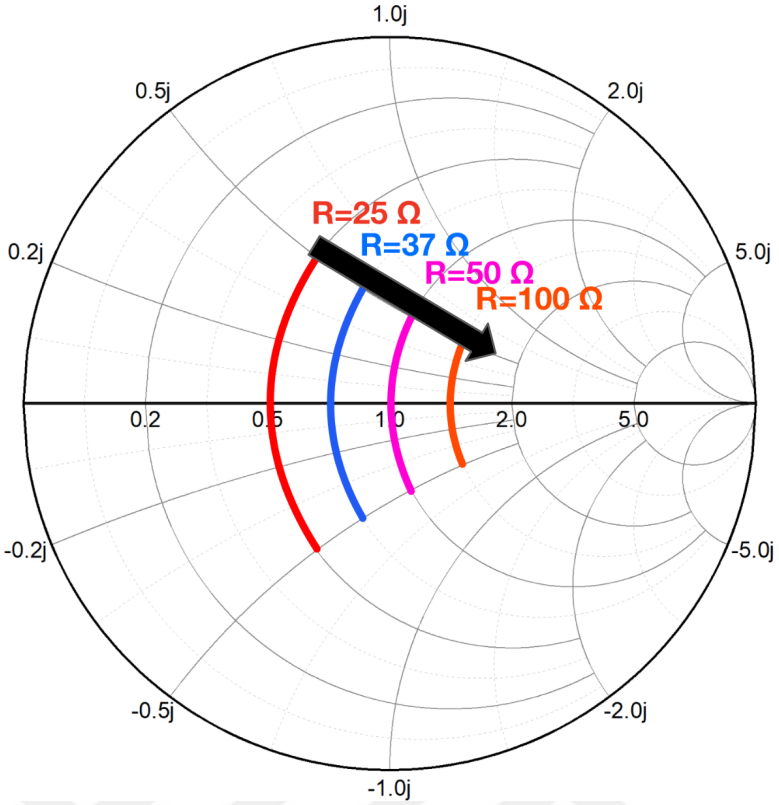



Figure 3.2 Impedance change of an arbitrary impedance with respect to frequency for different series resistance values

due to other parasitics that the dimensions of the transistors will bring. If the shape of the device is long and thin, it will start producing some inductance due to the transistor itself, and the metallization used to connect the device will also be long and bring inductance that will limit the bandwidth. Therefore, in this design, shorter transistors are used.

### 3.1.2 Order of the Circuit

As we increase the order of the matching network, the bandwidth of the network increases by decreasing the Q of the matching network. In Fig 3.3 three matching networks are shown that symbolizes possible matching arrangements at the ON arm of the network. From real 25 ohm to 50 matching is realize with first, second and third order series transmission line shunt capacitance circuits where first order shown with red line and circuit can remain under Q= 0.8, second order shown with blue can remain under Q = 0.5 and third order circuit can remain under Q = 0.4 showing that higher the order of matching wider the bandwidth can get. However, as seen, the decrease in Q is slowing with each order, meaning that at some point, the

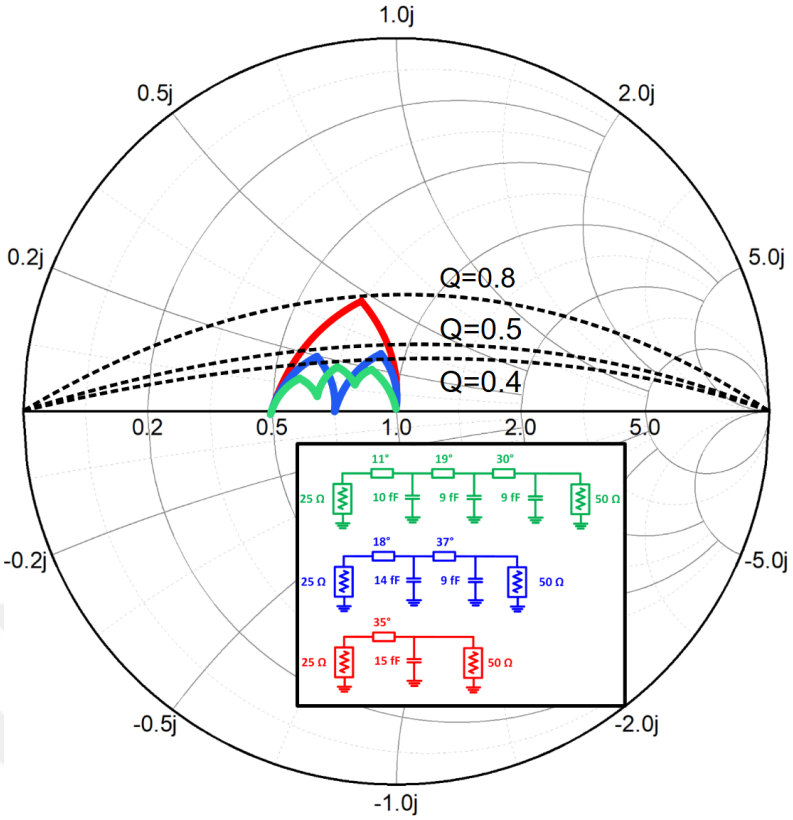



Figure 3.3 Series transmission line shunt capacitor matching network using 50 ohm lines at 150 GHz

improvement in bandwidth will be negligible. On the other hand, each order brings a linear amount of loss; therefore, no further than the third order shunt is selected for our design. One other factor with having more shunts is reducing the shunt resistances at the off arm, since more parallel resistance will have less resistance to the ground, which will minimize improvement as the number of shunts increases.

### 3.1.3 Effective Coff Reduction

In the layout of our circuit shown in Fig. 3.1, effective reduction of Coff is applied in eight locations: at the point where the first transmission line splits into two branches and at each shunt connection. These points share a common design principle: minimizing the interconnection length when lines split. This is critical because placing a series inductor before a capacitor effectively increases the perceived capacitance.To illustrate this, consider a series inductor $L_{\text{ser}}$ and a series capacitor $C_{\text{ser}}$ , with an equivalent capacitance $C_{\text{eff}}$ . Assuming $C_{\text{eff}}$ remains positive (i.e., $L_{\text{ser}}$ is small enough to avoid resonance at the frequency of interest), the relation-

ship is given in Equation 3.1. Rewriting $C_{\text{eff}}$ in terms of $L_{\text{ser}}$ and $C_{\text{ser}}$ as shown in Equation 3.2, and taking the ratio with $C_{\text{ser}}$ (Equation 3.3), it can be observed that for frequencies below resonance, the effective capacitance increases compared to the standalone capacitor. An increased effective capacitance results in reduced bandwidth, which is undesirable in this design. Therefore, the interconnection lines are kept as short as possible, just enough to connect to the transistor.

$$j\omega L_{\text{ser}} + \frac{1}{j\omega C_{\text{ser}}} = \frac{1}{j\omega C_{eff}} \tag{3.1}$$

$$C_{eff} = \frac{\omega \cdot C_{\text{ser}}}{1 - \omega^2 \cdot L_{\text{ser}} \cdot C_{\text{off}}} \tag{3.2}$$

$$\frac{C_{eff}}{C_{\text{ser}}} = \frac{\omega}{1 - \omega^2 L_{\text{ser}} C_{\text{ser}}} \Rightarrow C_{eff} > C_{\text{ser}} \tag{3.3}$$

### 3.1.4 Use of Transmission Lines

Using high impedance transmission lines will make the physical dimension of a line thinner. A width of around 6-8 $\mu$m will result in a 50 ohm transmission line. We went to the highest impedance we can go, which is 2 $\mu$m, the design rule check (DRC) limit that determines the minimum manufacturable width for each metal. Using a 2$\mu$m transmission line, an impedance of 85 ohms can be achieved. The short answer is that using a high impedance transmission line makes easier matching possible. For the long answer, we need to consider the transmission line at the input and the transmission lines in between the shunt arms. For the input one if we look at the impedance seen at the input prior to the transmission line is around 160 $\Omega$ in Fig. 3.4 comparison of using $Z_0$= 85 $\Omega$ and $Z_0$ 50 $\Omega$ is shown, clearly, it is desirable to use high impedance transmission line to match a high impedance to 50 $\Omega$. Similar reasoning can be carried out for the inter stage matching transistors where taking higher impedance value is easier with high impedance lines. One bandwidth optimization technique involves the use of multisection transmission lines, implemented by removing the ground plane beneath the intermediate sections, as illustrated in Fig. 3.5. Instead of varying line thickness to achieve different impedances, the proximity to the ground is modified. In these sections, the bottom ground plane is effectively absent (infinitely far), and only the sidewalls serve as the return path. This increases the effective ground distance, resulting in higher impedance. An ad-

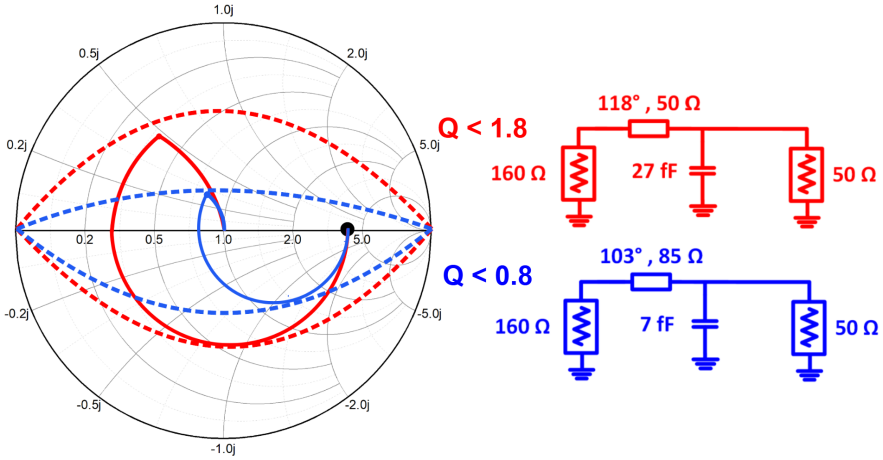



Figure 3.4 IMN

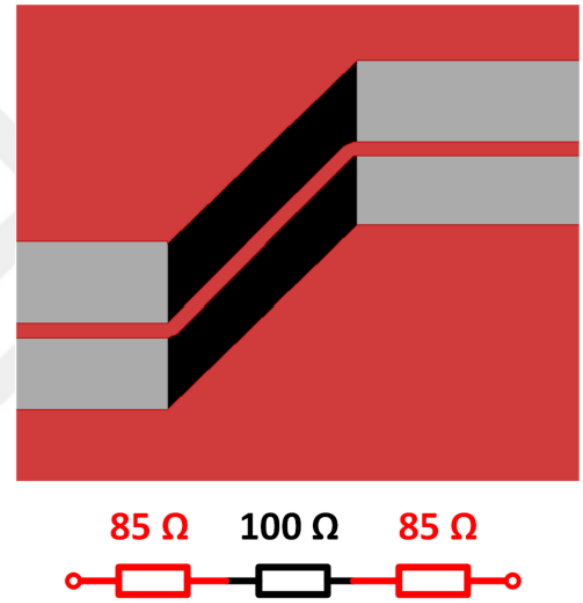



Figure 3.5 Multisection transmission line realized by selective grounding

ditional advantage of this approach is that the line thickness remains constant at 2 $\mu$m throughout, thereby avoiding losses associated with interconnects between lines of varying thickness.

### 3.1.5 Number of Stacks

As the number of stacks increases, the inductance of metal interconnects and parasitic capacitances also increases. This results in a higher effective capacitance when observing the impedance of an off-arm. Therefore, the smallest effective capacitance

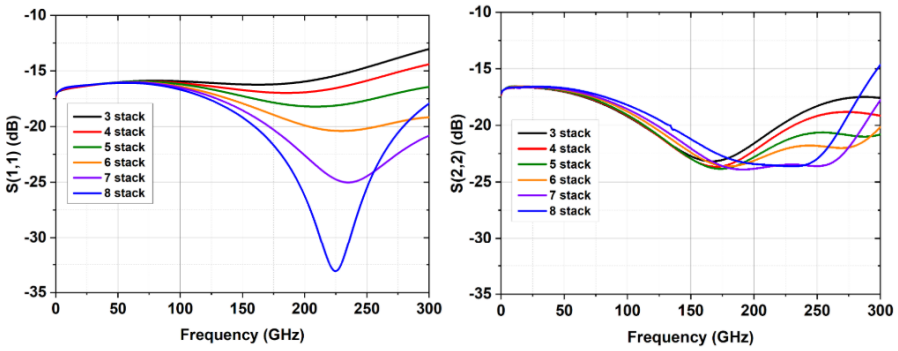



Figure 3.6 S(1,1) and S(2,2) vs frequency for different stack numbers

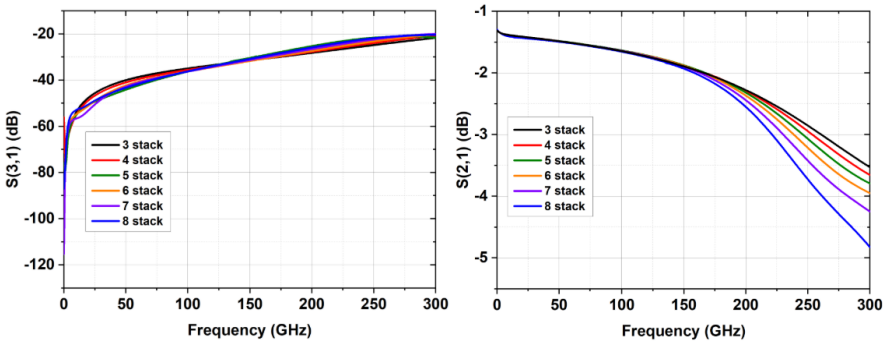



Figure 3.7 S(2,1) and S(3,1) vs frequency for different stack numbers

is seen with the fewest number of stacks. However, the bandwidth-limiting effects of the arm with shunt devices that are on should also be considered, especially at higher frequencies. To better understand this, we will analyze the number of stacks versus S-parameter performance for EM-simulated samples. In this analysis, the effective Coff value seen from the input of the stack is kept constant apart from metal interconnects and parasitics. For example, in a 3-stack device, each transistor is sized to have 8 fF, resulting in an effective capacitance of 2.66 fF per stack. Similarly, in a 5-stack configuration, each device is 13.3 fF, again yielding an effective 2.66 fF. To isolate the effect of the number of shunt devices and eliminate the influence of device sizing, the metalization size above the transistors is kept constant across all configurations. Fig. 3.6 shows the S(1,1) and S(2,2) parameters, Fig. 3.7 shows S(2,1) and S(3,1) parameters of the switch with varying device sizes. As the number of stacks increases after around 100 GHz, the effect of the off arm starts to kick in, and it starts changing the impedance. However, if there are more stacks due to their high value, the effect increases more slowly, therefore keeping the change of impedance slower. On the other hand, having more parasitics degrades the loss performance of the switch with every stack.

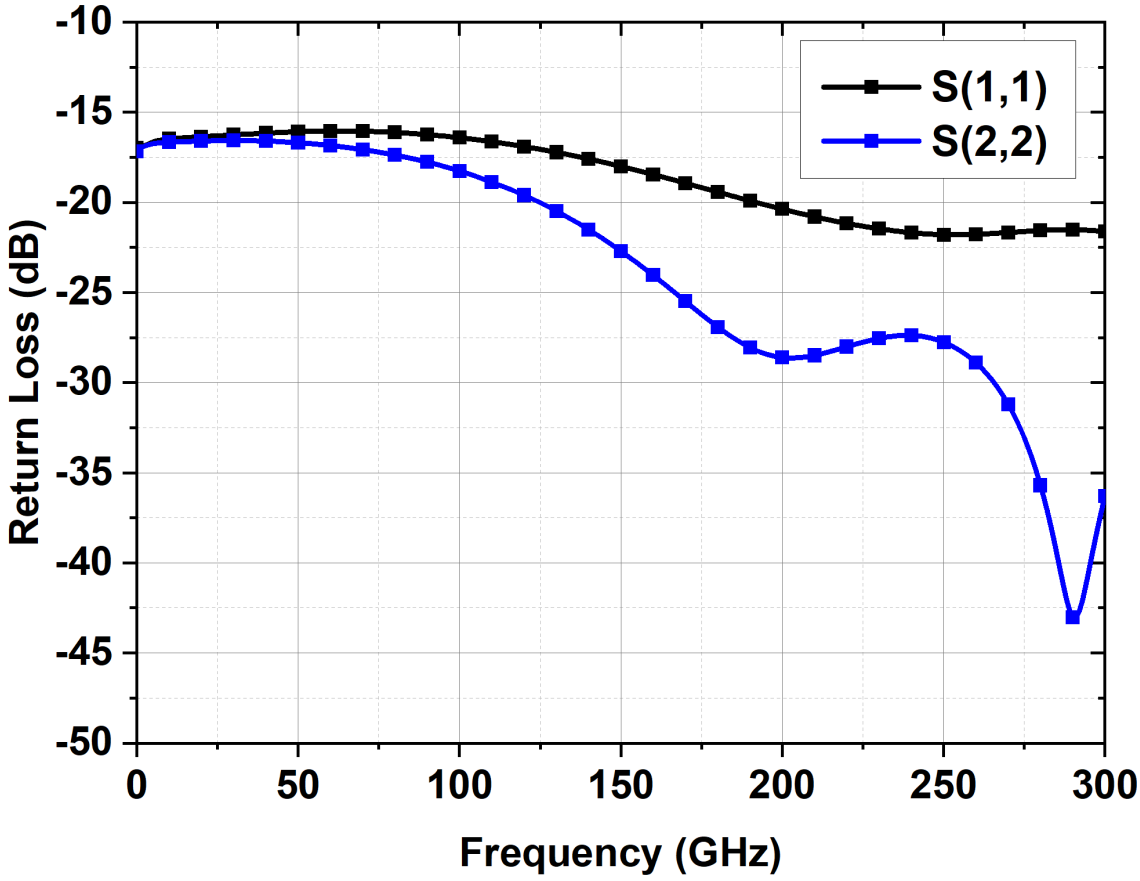



Figure 3.8 Return losses vs frequency

### 3.2 Simulation Result

The simulation was done using the Finite Element Method (FEM), which is more accurate and more suitable for 3D designs than Momentum RF or Momentum Microwave; however, it requires more RAM and simulation time. The six stacks are finally chosen, and their corresponding device size is scaled for the final simulation. The simulation results can be seen for S(1,1) and S(2,2) in Fig. 3.8 where form DC to 300 GHz the return losses remain under -16 dB. The loss and isolation performance can be seen in Fig. 3.9, where loss and isolation performance can be noted for every 100 GHz for DC to 300 GHz, which are 1.3 dB, 1.6 dB, 2.3 dB, and 3.7 dB for loss and 90 dB, 37 dB, 30 dB, and 24 dB.

Table 3.1 Comparison with the state-of-the-art switches

| References | Frequency (GHz) | Isolation (dBm) | Insertion Loss (%) | Area ($mm^2$) | Topology | Technology |
|---|---|---|---|---|---|---|
| (Khan et al., 2015) | 110-170 | <-22 | <-4 | 0.18 | Quarterwave single shunt | 32 nm SOI CMOS |
| (Cetindogan et al., 2018b) | 110-170 | <-22 | <-2.6 | 0.16 | Quarterwave single shunt | 130 nm SiGe BiCMOS - |
| (Chien & Buckwalter, 2023) | 110-132 | <-33.8 | <3.8 | 0.094 | Reflective Type | 250 nm InP |
| (Meng et al., 2015) | 130-180 | <-5 | <-21 | 0.0035 | Magnetically Switchable | 65 nm CMOS |
| (Meng et al., 2015b) | 220-285 | <-4 | <-17 | 0.002 | Magnetically Switchable | 65 nm CMOS |
| This Work | 0-300 | <-25 | <-3.7 | -0.0625 | Series Shunt | GF 130 nm |

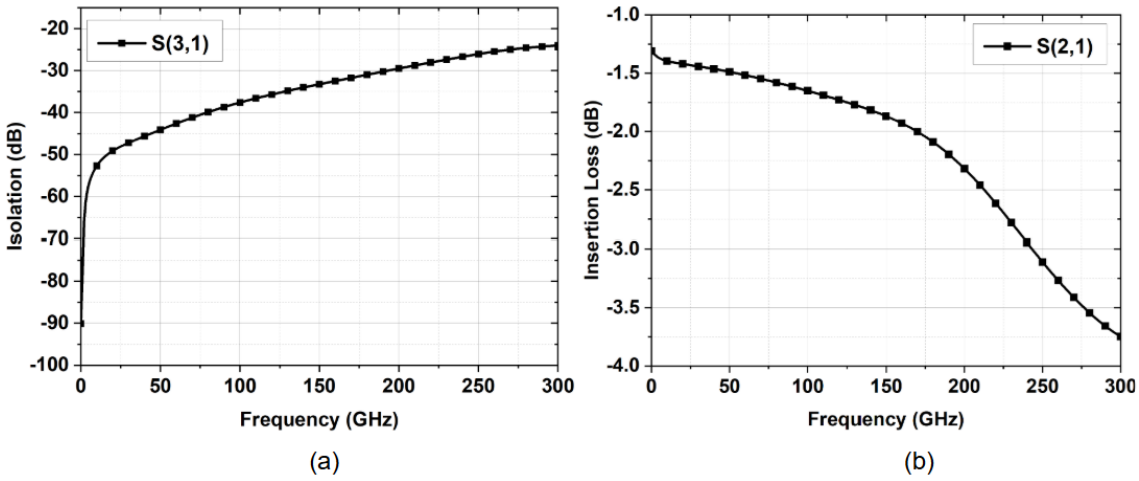



Figure 3.9 Loss (a) and isolation (b) versus frequency.

# 4. CONCLUSION

Driven by the accelerating demands of high-throughput wireless communication, autonomous systems, and compact radar platforms, RF and millimeter-wave circuit design is undergoing a decisive shift toward higher frequencies. As systems transition beyond the conventional microwave spectrum into the D-band and beyond, the development of wide-band, power-efficient, and compact circuit blocks becomes essential. Applications such as >100 Gb/s backhaul links for 5G/6G networks, short-range radar for robotics and automotive sensing, and gesture-controlled wearable electronics call for highly integrated, broadband transceiver front-ends capable of operating deep into the millimeter-wave regime. This thesis addresses these emerging challenges through the design and implementation of core RF/millimeter-wave front-end components. First, a high efficiency, small area power amplifier using IHP 0.13 $\mu$m SiGe BiCMOS technology presented having a PAE of 19.3 %,$P_{sat}$ of 17 dBm, Gain of 21.56 dB, 3 dB bandwidth of 26 GHz and an area of 0.1 mm$^2$ that is suitable for compact transceiver, radar or sensor applications that exhibits the highest PAE in the literature beating the last PAE value by 8% with quarter of the area and a similar output power also the proposed design shows maximum 1 dB variation in $P_{sat}$ can be seen from 150 GHz to 170 GHz and 3 dB drop from center frequency 130 GHz to 170 GHz that makes this PA usable not only in single frequency but a span of frequencies. To realize these specifications several approaches are use that include a methodology firstly conventional PA core design is carried out until layout level then a model of the current layout is fitted onto a schematic by a normalized S parameter fitting that captures the behaviours of all interconnects such as stairway connection then using fitted schematic best efficiency design is achieved by analyzing the tradeoffs of each section. Secondly, the two-stage amplifier optimal compression points are found through load pull analysis since efficiency is a function of compression. Thirdly, to achieve such a wide $P_{sat}$ and PAE bandwidth, meandered transmission lines are used that form parasitic capacitances between the lines, which increases the order of the matching network, also making the PA very small. Secondly, power combined PAs consisting of 2-way and 4-way power combinations at 160 GHz are presented. Simulated values achieve a PAE of 13.5/10.5 %, $P_{sat}$

of 14.5/16.4 dBm, Gain of 18/17 dB, 3 dB bandwidth of 49/48 GHz, and an area of 0.54/1.056 $mm^2$ for 2-way and 4-way, respectively. The same core optimization processes were utilized to model each section and optimize for the best efficiency. On top of two-stage PA power combining, a low-loss coupler has been used that minimizes the efficiency drop from single-stage PA to power-combined PA. Finally, an ultra-wideband SOI switch is proposed on a simulation level with input and output return loss being matched under -15 dB within the DC-300 GHz band, with a maximum loss of -3.7 dB at 300 GHz and an isolation of -25 dB at 300 GHz.To achieve this performance, a high bandwidth and high loss topology utilizing a series of transistor-shunt transistor-line-shunt transistor-line-shunt transistor is used, which is usually not preferred in high frequencies. Thanks to SOI technology, this topology could be realized at high frequencies. Also several techniques were used to increase further bandwidth which are sizing of the series transistor to move to a more compact circle in smith chart, having a high order circuit consisting of two more line shunt sections that enables moving in a lower Q circle in smith chart, effective Coff reduction by minimizing the series inductor at the connection off Coff, using high impedance transmission lines along with multi section transmission lines by ground proximity adjustment instead of changing width of the line and stack optimization. Each block's design and implementation methodology is showcased and compared with the current state-of-the-art, achieving a performance comparable to or better than the current state-of-the-art.

# 5. FUTURE WORK

The future works include firstly to further measure the differential PA with modulated signals such as chirp signal to measure the metrics such as Error Vector Magnitude (EVM), bit error rate (BER) that will show the performance of the circuit on a system level which will be decisive in what kind of modulation a system this PA can be used. Planned future work includes the realization of a compact transmitter system named as LO-scalable MIMO architecture, similar to that mentioned in (Sutbas, Hasan, Gadallah, Eissa & Carta, 2025). Furthermore, since the PA is compact, it has high efficiency for a given band and a considerable output power for the concerned frequencies, making it possible to realize a Doherty PA in a small area. Potential improvements may include a transformer-based inter-stage matching that will further shrink the size, since inductors at these frequencies are tiny. Furthermore, modeling of meandered transmission line networks can be co-analyzed with the core modeling to have a more efficient overall design. On the other hand, a DC-300 GHz switch was realized whose isolation value is mediocre, which can be made into a state-of-the-art design by either trading off loss and bandwidth since shunt resistors are the most limiting factor, or another way would be to implement an isolation cancellation network to cancel the signal remaining at the off arm. Another improvement may be to use meandered lines to reduce the area since the current implementation uses long transmission lines.

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