CHARACTERIZATION AND COMMERCIALIZATION OF SILICON AND INGAAS-BASED SINGLE PHOTON DETECTORS

A Thesis

by

Alper Özülker

Submitted to the
Graduate School of Sciences and Engineering
in Partial Fulfillment of the Requirements for
the Degree of

Master of Science

in the
Department of Electrical and Electronics Engineering

Özyeğin University
February 2024

CHARACTERIZATION AND COMMERCIALIZATION OF SILICON AND INGAAS-BASED SINGLE PHOTON DETECTORS

Approved by:

Asst. Prof. Kadir Durak, Advisor
Dept. of Electrical & Electronics Eng.
Özyeğin University

Asst. Prof. Ahmed Akgiray
Dept. of Electrical & Electronics Eng.
Özyeğin University

Prof. Dr. Oğuzhan Gürlü
Dept. of Science and Letters
Istanbul Technical University

Date Approved: January 4, 2024

To my family and friends

ABSTRACT

This thesis delves into the intricacies of quenching circuitry, specifically tailored for free-running single photon detectors working within the visible and near-infrared spectra. It embarks on a comprehensive exploration, commencing with an in-depth analysis of designing quenching circuitry customized for Silicon and InGaAs avalanche photodiodes (APDs). This investigation thoroughly examines the merits and drawbacks of various quenching circuit topologies, elucidating their diverse applications.

The challenges inherent in Silicon and InGaAs APDs are examined, highlighting optimization strategies for quenching and resetting circuitry while navigating electronic intricacies. Moreover, an emphasis is placed on developing a CubeSat compatible, miniaturized design, detailing its schematic blueprint.

The thesis explicitly covers the processes of designing, testing, debugging, and characterizing these detectors from both electronic and optical standpoints, providing detailed insights into the experimental outcomes. Parameters such as dead time, timing jitter, afterpulsing, and photon detection efficiency are scrutinized, elucidating their electronic ramifications on the designs. Comprehensive explanations are provided regarding the testing and characterization methodologies employed.

Furthermore, the thesis showcases three distinct single photon detector schematics and their corresponding PCB designs. It outlines the development of two disparate high-voltage amplifier designs, crafted to meet the requisite parameters for these detectors, all of which have evolved into viable commercial products.

This comprehensive exploration combines theoretical insights with practical implementations, culminating in a refined understanding of quenching circuitry intricacies tailored explicitly for free-running single-photon detectors. The resulting designs and

methodologies represent a gathering of interdisciplinary knowledge, offering profound implications for the advancement of single photon detection technologies.

ÖZETÇE

Bu tez, görünür ve yakın kızılötesi spektrum içinde çalışan tetiklemesiz (free-running) tek foton detektörleri için özel olarak tasarlanmış sönümleme devrelerinin inceliklerine inmektedir. Silikon ve InGaAs çığ fotodiyotları (APD'ler) için özelleştirilmiş sönümleme devrelerinin tasarımını derinlemesine analiz ederek kapsamlı bir keşifle başlamaktadır. Bu araştırma, çeşitli sönümleme devre topolojilerinin artılarını ve eksilerini ayrıntılı olarak inceleyerek çeşitli uygulamalarını açıklamaktadır. Silikon ve InGaAs APD'lerde bulunan zorluklar, elektronik karmaşıklıklara değinerek, sönümleme ve resetleme devrelerinin optimizasyon stratejilerini vurgulayarak incelemektedir. Ayrıca, küp uydu uyumlu, inyatürize edilmiş bir tasarımın geliştirilmesine odaklanarak, şematik tasarımı detaylandırılmaktadır.

Tez, bu detektörlerin elektronik ve optik açılardan tasarlanması, test edilmesi, hata ayıklanması ve karakterize edilmesi süreçlerini ayrıntılı bir şekilde ele almakta olup, deneysel sonuçlara dair detaylı iç görüler sunmaktadır. Ölü zaman, zamansal belirsizlik, artçı sinyal ve foton algılama verimliliği gibi parametreler ve tasarımlar üzerindeki elektronik etkileri açıklayarak incelenmektedir. Kullanılan test ve karakterizasyon metodolojileri hakkında kapsamlı açıklamalar sunulmaktadır.

Ayrıca, tez üç farklı tek foton detektörü şemasını ve bunların karşılık gelen PCB tasarımlarını sergilemektedir. Bu detektörlerin gereksinim duyduğu parametreleri karşılamak üzere hazırlanan iki farklı yüksek voltajlı amplifikatör tasarımının geliştirilmesini ayrıntılı olarak ele alır, ve hepsi başarılı ticari ürünlere dönüşmüştür. Bu kapsamlı araştırma, teorik bilgileri pratik uygulamalarla birleştirerek, tetiklemesiz tek foton detektörleri için özel olarak tasarlanmış sönme devrelerinin inceliklerinin rafine bir anlayışla birleşmesini anlatmaktadır. Ortaya çıkan tasarımlar ve metodolojiler,

disiplinler arası bir bilgi birikimini temsil eder ve tek foton algılama teknolojilerinin gelişimi için derin etkiler sunmaktadır.

ACKNOWLEDGEMENTS

I extend my sincere appreciation to my mentor, Kadir Durak, whose guidance and opportunity allowed me to delve into product development and research in this field.

Special gratitude to Can Eraydın for engaging discussions, collaborative experiments, and for inspiring the idea that evolved into a potential patent through my designs.

I am deeply thankful to Muhammed İzçınar for their invaluable assistance in implementing the circuitry and conducting experiments, contributing significantly to this work.

I am grateful to my friends and colleagues for their support and assistance whenever needed, which has been instrumental throughout this endeavor.

Lastly, I would like to thank my family for their nonstop help, care, support and encouragement.

The work in this thesis is supported by the Scientific and Technological Research Council of Turkey (TUBITAK) with project no: 3220445, 1501 project call, and no: 9200113 is a part of the Uzay Tabanlı Kuantum İnternet (SQUINT) project under the EUREKA program.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER I

INTRODUCTION

1.1 Background

Single photon detection stands as a pivotal technology across both academia and industry due to its applications and fundamental role in various domains. Single photon detectors play a critical role in quantum information science, facilitating experiments and investigations on quantum mechanics, quantum computing, and quantum communication. These detectors are essential for experiments in fundamental physics research, aiding studies on particle interactions, quantum entanglement, and probing the behavior of light at its most fundamental level. It is one of the modules that enables researchers to explore the principles of quantum mechanics, quantum entanglement, and quantum superposition, leading to advancements in quantum technologies. Moreover, in applied sciences and engineering, single photon detection finds extensive use in fields like astronomy and astrophysics for the observation of faint celestial objects, helping in the exploration of distant stars and galaxies. Additionally, it's crucial in biomedical imaging techniques, such as single photon microscopy and tomography, allowing for high-resolution imaging at the cellular or molecular level. In the industrial landscape, single photon detection is pivotal in various sectors like telecommunications, enabling secure quantum communication and cryptography protocols. Its importance lies in its ability to detect and process individual photons accurately, providing enhanced sensitivity, low-light imaging capabilities, and quantum-based secure communication protocols, thereby driving advancements across scientific research, technological innovations, and industrial applications.

Historically, photomultiplier tubes (PMTs) have been used for the detection of

single photons. PMTs were first introduced in 1935 [3]. Photomultipliers are commonly built within a sealed glass enclosure, similar to other vacuum tubes, ensuring a stringent and robust glass-to-metal seal. This housing encompasses essential components: a photocathode, multiple dynodes, and an anode. Incoming photons interact with the photocathode, typically a slender conductive layer deposited as a coating on the interior surface of the device's entry window. As a result of the photoelectric effect, electrons are emitted from this surface. Subsequently, a focusing electrode guides these electrons towards the electron multiplier, where a process of secondary emission amplifies their numbers.

Chronologically Geiger counters have been presented for the applications for single-photon detection. A Geiger counter comprises two main components: The Geiger-Müller tube, responsible for radiation detection, and the associated processing electronics, tasked with presenting the detected results. Within the Geiger-Müller tube, an inert gas like helium, neon, or argon is maintained at low pressure and subjected to high voltage. When high-energy particles or gamma radiation ionize the gas, momentarily creating conductivity, the tube briefly carries an electric charge. The Townsend discharge effect significantly amplifies this ionization within the tube, generating a readily measurable detection pulse. Subsequently, this pulse is conveyed to the processing and display electronics for interpretation and presentation.

Single-photon avalanche diodes (SPADs) are highly sensitive semiconductor devices designed to detect single photons. These diodes operate in a process called Geiger mode, where a single photon absorbed by the semiconductor material triggers an avalanche of charge carriers, generating a detectable electrical signal. Their unique capability to register individual photons makes SPADs crucial components in various applications such as quantum communication, LiDAR systems, and low-light imaging, enabling precise photon counting and high-speed detection in diverse fields of research and technology.

In the realm of academia, SPADs have emerged as pivotal components, prompting the publication of electronic circuit designs. The advent of the active quenching circuit technique in 1982 marked a significant milestone [4]. Subsequently, the commercialization of SPADs in the early 1990s [5] led to extensive research focused on their performance and operational longevity. Notably, EG&G Canada (later Perkin-Elmer, presently Excelitas Technologies) commercially produced single-photon detector modules during the 1990s [6]. Since then, a proliferation of companies, including IDQuantique, Laser Components, Micro Photon Devices (MPD), and Qubitrium, have entered the market, manufacturing SPDs. This burgeoning industrial presence reflects the ongoing evolution and wider accessibility of SPD technology across various sectors and applications.

Advancements in space technology demand highly efficient and reliable photonic instrumentation, particularly in the detection of individual photons. Single photon detectors based on Silicon (Si) and Indium Gallium Arsenide (InGaAs) avalanche photodiodes hold immense promise for applications such as time-correlated single photon counting (TCSPC), quantum communications and their space applications, due to their superior performance in capturing low-intensity light signals. Here, we delve into the comprehensive characterization and potential commercialization prospects of Si and InGaAs-based SPDs specifically engineered for both laboratory use and space-oriented functions. Drawing inspiration from seminal works in the field, such as the groundbreaking research bolstered photon detection efficiency and timing accuracy [7]. Additionally, optimization of active quenching circuits, improving timing precision within the picosecond range for single photon avalanche diodes, demonstrates promising advancements [8].

The transformative contributions, including the monolithic active quenching circuit for large-area SPADs signify pivotal milestones in pushing the boundaries of SPD capabilities [9, 10]. Enhancements in free-running InGaAs APDs enabled efficient

single photon counting at telecom wavelengths, representing a crucial leap in space communication technologies [11]. Furthermore, the proposal of an active quenching circuit tailored for single-photon detection using Geiger-mode avalanche photodiodes (GM-APDs) enabled a novel optimization avenue for these detectors in light on crucial control mechanisms [12]. Understanding and elucidating control mechanisms for actively-quenched single photon detectors under exposure to intense light sources represented a pivotal step in ensuring operational efficiency in space-based scenarios.

Silicon avalanche photodiodes, known for their sensitivity in detecting visible to near-infrared light, pose a challenge when used for single photon detection in Geiger mode. This mode causes controlled breakdowns emitting fluorescence light upon detecting photoelectrons, potentially impacting critical applications like quantum cryptography or single-particle spectroscopy [13]. Many applications using telecom wavelengths offers rapid deployment benefits, leveraging established optical fiber infrastructure and advanced telecom technologies. InGaAs avalanche photodiodes are the favored detectors at these wavelengths for photon detection. Like Silicon counterparts operating at shorter wavelengths, they also demonstrate fluorescence resulting from electron-hole pair recombination during the avalanche breakdown process [14].

In amalgamating these seminal studies and leveraging their findings, this work aims to present a comprehensive overview of the customization in Silicon and InGaAs-based single photon detectors, their operational nuances, performance characteristics, and potential avenues for commercial utilization in laboratory and space applications.

1.2 Objectives & Scope

The application of quenching circuits finds relevance in various fields such as time-correlated single-photon counting, quantum key distribution (QKD), and light detection and ranging (LIDAR). When subjected to a bias voltage, the utilized APDs exhibit an avalanche of electrons upon photon detection, a phenomenon known as

avalanche current. However, to facilitate subsequent photon detection, this avalanche must be promptly terminated, constituting a period termed as "dead time".

The primary objective of this work is to minimize the interval between the detection of individual photons and the readiness to detect subsequent ones, often referred to as dead time. In this work a distinctive method employed, targeting a dead time of approximately 40 nanoseconds for the SPAD. To this end, a non-conventional technique called mixed quenching has garnered attention due to its integration of advantages from both passive and active quenching methods, mitigating their respective drawbacks [15]. Furthermore, the circuit design incorporates an active reset, a feature instrumental in reducing the dead time.

The primary challenge lies in managing the timing aspects of the circuit. Achieving a reduced dead time necessitates a more intricate circuit design, leading to increased components and subsequently introducing more delay into the circuit [16]. Key components of this circuit, such as comparators and transistors, need to possess ultra-fast speeds, making them not only more expensive but also challenging in terms of procurement. Another critical goal of this project revolves around cost minimization. To ensure adaptability across diverse projects, the circuit's affordability is paramount. Optimization strategies directed towards cost reduction, coupled with comprehensive market analysis, stand as pivotal factors driving this endeavor.

1.3 Techniques & Technology

Primarily, two predominant quenching methodologies prevail:

- Passive quenching
- Active quenching

Passive quenching involves the use of passive components, like resistors placed between the voltage source and the diode, to cease the avalanche current. Although

this method requires a longer time to halt the avalanche compared to active quenching, its advantage lies in the ease of component adjustment, necessitating fewer and simpler elements. Typically, the quenching duration for this technique falls within the microsecond range [17].

Conversely, active quenching promptly responds to the bias voltage. Upon measuring the avalanche current, the quenching circuit acts swiftly to reduce the bias voltage below the detector's reverse bias level. This technique entails a diverse array of components, particularly for bias voltage control, including transistors (CMOS, DMOS), logic gates, and microcontrollers. In contrast to passive quenching, the typical quenching time for this method ranges about 20 nanoseconds [4].

Mixed quenching, on the other hand, amalgamates the strengths of both techniques. This approach involves connecting the photodiode to both a high impedance setup and to the active quenching and reset circuits.

A specialized quenching technique, the fast active quenching technique, stands out for its applicability to InGaAs photodiodes. This technique dramatically reduces circuit dead time to a range between 2 to 3 nanoseconds [18]. However, its implementation poses significant challenges and substantially escalates circuit costs.

Various studies have introduced diverse solutions that address quantum efficiency, afterpulsing rate, dark count rate, excessive voltage, among other factors [19, 20]. These investigations reveal nuanced differences in circuit purposes and emphasize the significance of minimizing dead time while preserving detection efficiency. Despite advancements in InGaAs APDs following the 2000s, very few InGaAs APDs are available on market. Their commercial accessibility and availability remain relatively stagnant compared to Silicon counterparts, warranting further advancements in market readiness.

CHAPTER II

METHODOLOGY

Active quenching and mixed quenching techniques are employed for Single-Photon Detectors (SPDs) to leverage and optimize the benefits of both active and passive quenching methodologies. This comprehensive approach aims to experimentally explore and refine the advantages inherent in these techniques while mitigating their respective limitations. The foundational principle involves operating the GM-APD below its breakdown voltage (Vbd), typically at Vbd = 125V with a bias voltage (Vbias) set at 130V, thereby activating the Geiger-mode. In this mode, the APD attains heightened sensitivity, capable of generating an avalanche current even upon the impact of a single photon, induced by impact ionization.

Upon the occurrence of an avalanche, necessary circuitry processes the resulting pulse into a digital output, the fundamental objective of the detector. However, without biasing the APD above its breakdown, the avalanche persists, preventing the detection of subsequent photons. Quenching, a technique used to stop the avalanche current, prevents to sense the next photon, as it elevates the APD's bias voltage beyond its breakdown, Vbias (after quenching) = 120V, necessitating a resetting mechanism.

Resetting mechanism restores the increased bias voltage to its initial value, Vbias1 = 120V (after quenching), Vbias2 = 130V (after resetting), preparing the APD for subsequent photon detection. The minimum time interval between two single photon detection, in other words avalanche occurrence, is referred to as the detector's dead time (Tdead = Tquench + Treset). These processes operate independently, with quenching increasing the bias voltage, and resetting subsequently reducing it, ensuring

they don't interfere.

Additionally, several pertinent parameters, including excess bias voltage (Vexcess), dark count rate (DCR), saturation value, timing jitter, photon detection efficiency, and afterpulsing, significantly influence the detector's performance. These parameters encompass key aspects such as voltage disparities, photon detection rates, timing uncertainties, and potential avalanche occurrences without photon inputs:

- Excess bias voltage represents the difference between the APD's breakdown voltage and its bias voltage (Vexcess = Vbias - Vbd).
- Dark count rate (DCR) signifies the count rate in counts per second (cts/s) when there are no photons coming on to the APD's active area. This parameter exhibits proportional dependence on the APD's temperature.
- Saturation value denotes the maximum count rate achieved by the detector under steady-state conditions.
- Timing jitter can be expressed as the uncertainty in photon arrival, and electronic stability, in other words variations in the dead time. This metric is proportionally linked to the count rate and is measured in seconds.
- Photon detection efficiency quantifies the likelihood of detection, based on the wavelength of incident photons and the efficiency of the electronics to sense and convert it to a meaningful value. It is mostly expressed as percentage value.
- Afterpulsing refers to the occurrence of avalanche pulses without an incident photon on the APD. This phenomenon arises when rapid quenching fails to entirely stop the avalanche current, leaving residual charge carriers that initiate a subsequent avalanche after resetting. Afterpulsing probability is typically represented as percentage value.

Further elucidation on these parameters will be presented in subsequent sections.

2.1 Functional Blocks

The SPD design consists of consecutive operations. In Figure **??**, the block diagram of the detector is shown.

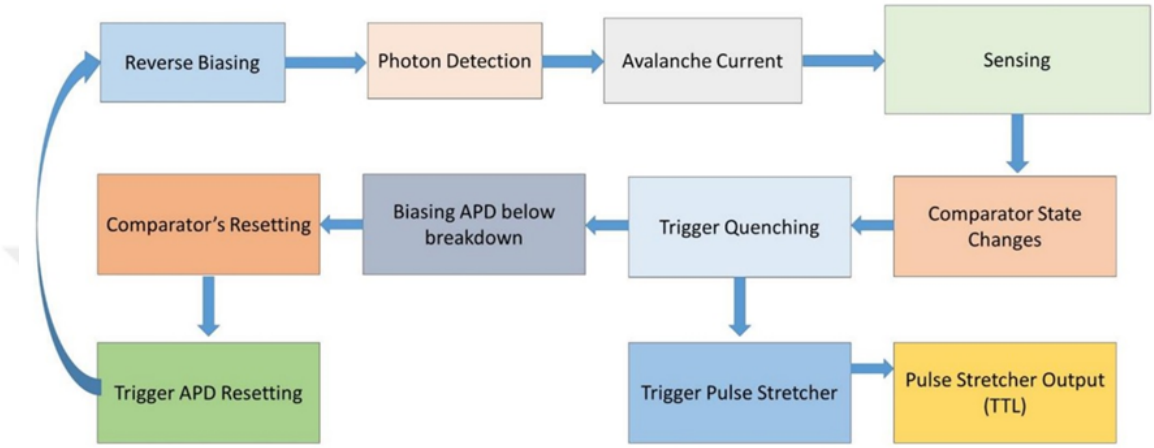

Figure 1: The block diagram showing SPD's working principle

The circuit initialization commences with the power-up sequence. Upon activation, the circuit would make the APD ready for detection of single photons, commencing with the "reverse biasing" step indicated in Figure 1. When the APD would be biased below its breakdown voltage in a reverse-biased state, it would become available for photon detection. Upon impact of a single photon on the APD's active area, an avalanche current would be generated, denoted as "Photon detection" and "Avalanche current."

The resulting avalanche current would be directed to the non-inverting input "Sensing" of a comparator. This comparator is pre-configured to shift its output from logic 0 to logic 1, indicative of photon detection, triggered by the increase in voltage at its non-inverting input, termed as "Comparator state changes." This change in logic state at the comparator's output would activate an analog switch Integrated Circuit (IC), known as "Trigger quenching." This switch would alter its output from

0V (GND) to a positive supply voltage of 12V, effectively quenching the avalanche pulse at the APD's anode. Simultaneously, it triggers a pulse stretcher to indicate photon detection, labeled as "Trigger pulse stretcher."

Concurrently, the pulse stretcher would produce a TTL output ("Pulse stretcher output"), while the 12V output from the switch would quench the avalanche current by reducing the biasing voltage by 12V, signifying "Biasing APD below breakdown." The comparator reverts to its initial state, where the inverting input exceeds the non-inverting input, termed as "Comparator's resetting." As the comparator's output shifts to logic 0, the switch would adjust its 12V output back to 0V (GND), activating the "Trigger APD resetting." Consequently, the quenching pulse is purged, and the APD's bias voltage reverts to its initial value, encapsulated as "Reverse biasing." This iterative cycle persists upon circuit power-up. A comprehensive discussion on these functions will be further expounded in the schematic design.

2.2 Approach & Simulation

The initial phase of circuit design involved validating the block diagram's concept through simulation software like LTspice and Pspice. Due to the unavailability of a simulation profile specific to Geiger-Mode Avalanche Photodiodes (GM-APDs), a basic current source was employed as a substitute. While publications exist on emulating APDs in simulation programs [21, 22], a new, more basic approach is utilized for LTspice simulations, necessitating the use of the basic current source. The precise avalanche current value remains indeterminate; however, estimations based on datasheets from commercially available GM-APDs (such as the Laser Components SAP500 series and Excelitas C30902SH series) suggest a probable value of around 200uA. Nonetheless, the design operates within an estimated avalanche current range exceeding 10uA, as ascertained from the simulations.

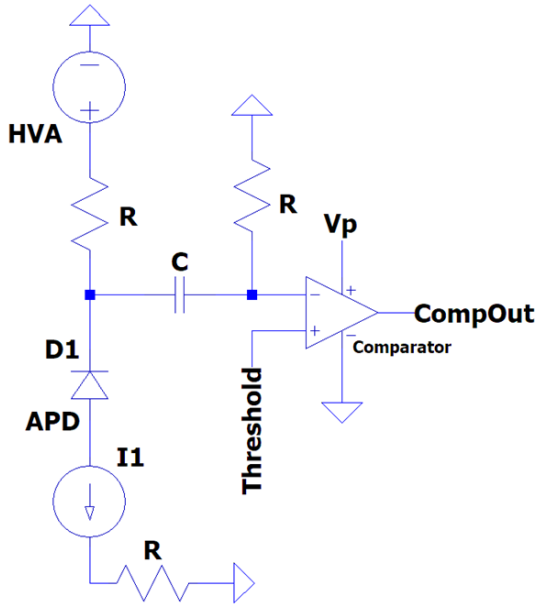

Figure 2: The simplified LTspice schematic of the mixed quenching circuit design (sensing stage) [1]

It became evident that an ultra-fast comparator is imperative to achieve enhanced bandwidth, as the frequency of the detector circuit's output hinges on the level of illumination on the APD. This frequency can range from tens of Hz, in the absence of illumination (dark count) to tens of MHz in the saturation regime. The initial objective is to set the bandwidth range from DC as a starting point to at least 1MHz as the endpoint. A fast, wide-voltage ranged comparator is chosen due to the status as the fastest available comparator with a compatible simulation profile in LTspice. In simulations, the avalanche pulse is transmitted to the comparator's non-inverting input through a capacitor to provide sufficient AC input for pulse detection. A sensing resistor, connected to the ground, is introduced to convert the avalanche current into a voltage signal, facilitating the adjustment of the threshold voltage at the inverting input. The threshold voltage, set by a 10mV voltage source, closely approximates the DC bias of the non-inverting input (GND), mitigating susceptibility to noise.

Operating at 5V and 0V at the comparator yields logic 0 as GND and logic 1 as 5V. Initially, the comparator's output was utilized for the APD's quenching and resetting in simulations. However, it is subsequently determined that the quenching and resetting pulses requires dominance to regulate the anode of the APD. Consequently, a CMOS topology is adopted to verify the proof of principle. The PMOS and NMOS are chosen according to rapid response times. The PMOS, serving as the quenching pulse source, is fed with a 5V supply, while the NMOS, operating as the resetting pulse source, is supplied with 0V. Their respective drains were interconnected and linked to both the APD's anode and each other. Furthermore, their gates were interconnected and connected to the comparator's output, TTL.

No disparity has been observed between the attained parameters and the targeted parameters, indicating the circuit's stable operation from DC to 1MHz, maintaining consistency with an avalanche pulse range of 10uA to 10mA. This successful outcome validates the achievement of the proof of principle. The subsequent phase involves enhancing the quenching process's reliability by generating a larger quenching pulse. To accomplish this, options include elevating the supply voltage of both the comparator and PMOS or opting for a high-output voltage switch compatible with CMOS or TTL logic inputs. The selection leans toward utilizing an analog switch due to its perceived advantages in terms of reliability and speed. Although the comparator can support a 12V range, maintaining the same slew rate results in increased delay, potentially slowing down the circuit. Conversely, an analog switch is more adept at handling higher frequencies with increased output current, presenting less problems in terms of complexity and offering simpler logic compatibility. Despite the absence of a suitable default profile for an analog switch IC in LTspice simulations, given the user-friendly nature of analog switches in schematic and PCB design, the decision to proceed with the analog switch concept is made.

Similarly, it's determined that simulation isn't imperative for the pulse stretcher

IC. A D-type flip-flop topology is preferred for the pulse stretcher due to its necessity for rapid pulse response, aimed at reducing jitter in the detector's output. Additionally, the straightforward adjustment of the output pulse width using a simple time constant topology (RC) favors the D-type flip-flop.

The sensing stage of the circuit design in Figure 2 has been patented in Türkiye [21].

2.3 First Design

The simulated circuitry design has commenced, initiating the determination of DC voltage stages. To ensure simplicity and diverse options for integrated circuits (ICs), the primary DC voltage is established as 5V. Additionally, for a dependable and consistent quenching voltage, 12VDC is designated.

Opting for the main DC voltage (5V) involves numerous voltage regulator alternatives. The choice gravitates toward the 5V linear voltage regulator due to its compatibility with a commonly available and cost-effective 6V plug converter, serving as its input supply. Key features of the linear voltage regulator encompass high regulation efficiency, relatively low noise, a 500mA current output, and minimal component requirements for operation. With an estimated overall circuitry current demand not surpassing 150mA, selecting a minimum output current of 500mA for the voltage regulator allows adequate headroom.

The suitability of the plug supply voltage, whether 12V or 6V, is deliberated upon. Due to the typically high noise associated with plug converters, using an unregulated 12V feed for the analog switch is deemed unsuitable. This decision arises from the difficulty in finding a wide supply voltage range analog switch with logic compatibility, compounded by a very low power supply rejection ratio (PSSR), thereby limiting viable IC choices in the market. Consequently, the utilization of a 6V plug converter, providing a minimum 1A current output, is decided upon. The

strategy is to establish consecutive blocks as DC voltage supplies. Therefore, the challenge shifts toward converting 5V to 12V. Numerous ICs are available for this purpose, and a step-up voltage regulator topology is chosen.

In order to cool down the APD, the integrated TEC element is decided to be employed. Referencing the SAP500-T8 datasheet [23], the built-in TEC possesses strict operational limits, accommodating a maximum voltage of 2V across its pins and a peak current of 1.4 amperes. Due to these stringent constraints, a step-down voltage regulator becomes imperative. Seeking a high current output with feedback, a step-down voltage regulator IC was chosen for its versatile current output range (up to 2A) and stable low output voltage parameters. Its topology mirrors that of a step-up voltage regulator, with the step-down variation requiring solely the inclusion of an inductor to channel current to its output.

Moreover, a high voltage amplifier (HVA) is essential to provide the reverse bias voltage to the APD. Numerous modules available on the market suit this purpose. Ensuring compatibility with both the Matsusada TS-0.3 module and Qubitrium HVA module, it was decided that the detector can be adapted for either topology. Both systems support a 12V supply and offer an adjustable output voltage range of 0V to 300V. Their divergence lies in the control mechanisms; the TS-0.3 necessitates an external control voltage, whereas the Qubitrium HVA requires a resistive divider to the ground due to its internal feedback topology. Adjustment of the output voltage is easily facilitated via a trimpot in both instances.

By materializing the preliminary stage, determining the initial components to be integrated into the circuitry, the realization has started. For powering up the detector module, a 2.5mm shielded female jack connector (providing 6VDC in this instance) is employed. The incorporation of a large polarized capacitor alongside two smaller capacitors are prioritized to filter any potential AC voltage fluctuations and maintain stability. A 10V zener diode serves the purpose of capping the input voltage at 10V,

preventing potential damage to the linear voltage regulator. Additionally, an EMI filter was introduced to stabilize the 6V input. Decoupling capacitors were integrated into the design to filter out any AC components that might disrupt these DC paths.

An arrangement of utilizing either 6V or 12V, accounts for the scenario involving the use of the Qubitrium HVA, which features a broad supply voltage range (from 5V to 18V), allowing the 12V supply to manage a lighter load, ensuring greater headroom.

In the high-speed segment of the detector, the chosen components (comparator, analog switch, flip-flop) will not be specified, considering that the intellectual property (IP) belongs to Qubitrium Ltd. Şti. An additional comparator option is being considered to mitigate unforeseen parasitic properties. Given the intricate nature of an IC such as a comparator, unforeseen issues might arise during the design phase. Two compatible comparator ICs have been found. To ensure a fair comparison of the performance between the two comparators with identical topologies, adjustments should be made to align their input/output stages and supply voltages as closely as possible.

The high-speed segment's design commenced with the selection of the SAP500-T8 APD from Laser Components, chosen for its integrated TEC and thermistor facilitating temperature control. For the reverse biasing setup, the APD's cathode needs connection to the HVA output, while the anode links to the comparator, serving as the sensing component. The thermistor pins remain unconnected initially, allowing initial use of the APD without cooling. Later, these can be linked to a control unit (TEC driver) via cables. Regarding the TEC pins, TEC+ connects to the TEC driver's output, while TEC- links to ground. To control the current passing through the TEC, a resistor is series-connected between TEC- and GND, providing an option for cooling or non-cooling use by soldering or desoldering it.

At the APD's anode, a resistor serves to convert the avalanche current to a voltage value and maintain anode voltage close to GND.

Two comparators will be integrated into the design and chosen accordingly. These comparators share identical input and output stages. The initial stage involves a non-inverting input stage. Utilizing a resistive divider with trimpot, the DC offset voltage can be adjusted. Although numerous resistors may be used, trimpot would seem enough to serve the purpose. A zener diode can be used to limit the DC offset voltage from deviating in between zener voltage and -0.7V.

It's essential to note the use of ferrite beads and capacitors along the DC lines. Ferrite beads are inserted between the ICs' supply nodes and their respective regulator outputs to prevent unwanted frequency coupling. These nodes solely necessitate DC voltages. The capacitors, meanwhile, serve for minor filtering of AC signal components at these nodes.

The output pin of the comparators is linked to both the analog switch and the control inputs of the flip-flop. In ensuring stability, a parasitic capacitor plays a crucial role. The chosen analog switch boasts a broad supply and switching voltage range. As detailed in its datasheet, higher supply voltage enables faster response times. Consequently, both the switching and supply voltage have been set to 12V. The switch determines the connection of its output pin based on the logic value at its input pin. For quenching and resetting, voltage values were predetermined at 12V and 0V (GND), respectively.

In the preliminary phase, numerous ICs suitable for pulse stretching were considered. Opting for simplicity, rapid response, and analog control, the choice fell on a flip-flop as the preferred topology. A cost-efficient and widely available flip-flop has been decided. The primary goal for the pulse stretcher is to modulate the output pulse's characteristics, including its amplitude, pulse width, and waveform. A square wave shape is targeted, and the amplitude is set to 5V for compatibility with TTL and CMOS standards. It's worth noting that the termination impedance of the output might cause slight variations in the pulse amplitude. Similar filtration methods have

been applied to the supply (DC) voltage pathways to ensure stable performance.

The pivotal aspect of the topology involves the external negative feedback. To regulate the output pulse width easily, external manipulation would be essential. To establish a consistent delay, the fundamental approach involves a basic time constant topology. Employing a series resistor and a grounded capacitor, this setup generates a defined time delay. Typically, this configuration entails the signal encountering the resistor first, followed by a parallel capacitor before reaching its destination. However, this method might necessitate precise capacitor and resistor values during the debugging phase to achieve the desired accuracy.

Instead of the conventional approach, we've configured the topology to enable the signal to simultaneously encounter the capacitor and resistor. This adjustment aims to reduce sensitivity regarding pulse width changes. This modification allows for adjusting values in larger increments, resulting in a slower change in outcomes, suitable for the intended nanosecond-range output pulse width. Ensuring a precise output stage is crucial. This entails maintaining a clear path devoid of additional components. The low current output of the flip-flop and the potential adverse impact of additional loads on signal integrity drive this necessity. Introducing a termination to the ground could distort the signal. To maintain transmission line integrity and match pin impedance, a 50-ohm impedance is chosen. For connection purposes to another module, typically time tagging units, a 50-ohm SMA connector has been selected.

Utilization of the TEC in the APD is considered optional. The primary function of the built-in TEC component operates based on the cooling proportional to the current across its positive and negative pins. Due to the constraints outlined in the preliminary phase, a step-down converter IC is chosen. This converter boasts reliable feedback, precise regulation, and minimal output ripple as highlighted in its datasheet.

Two capacitors serve as input stage decoupling components, aimed at filtering out unwanted frequencies. Output filtering capacitors, tasked with minimizing output voltage ripple. Lastly, feedback resistances can be tailored using basic resistive voltage divider formulas. In this scenario, we aimed for a practical characterization to observe the proportional impact on the TEC of the APD. To achieve this, we required flexibility in adjusting resistance values. As a result, a trimpot and two additional resistances have been incorporated into the design.

The first idea for high-voltage supply is to accommodate an HVA module, referencing the Matsusada TS-0.3P and Qubitrium HVA modules discussed in the preliminary section. Both modules feature five pins for input and output, positioned identically. For the Matsusada TS-0.3P, a 12V supply voltage is required, hence the 12V link is selected. On the other hand, the Qubitrium HVA module operates within a wide voltage range. Opting for the 6V input provides a lighter load compared to other supplies, offering an alternative to the 12V supply. Output capacitors, designed to handle high voltage, aims to minimize unwanted noise and reduce output ripple from the HVA.

Finally, a basic voltage divider has been incorporated to fine-tune the input control voltage for the Matsusada TS-0.3P module. This setup is necessary as it's specifically compatible with an external voltage control configuration. Conversely, for the Qubitrium HVA module, as it internally relies on feedback from its output, it solely accepts output resistance toward the ground. Adjusting a simple trimpot would then be sufficient for controlling the output voltage.

2.4 CubeSat Compatible SPD

The first detector design has undergone rigorous characterization and debugging, leading to the finalization of all components. Subsequently, trimpots, redundant passive footprints, and certain filters have been omitted as they were solely intended

for characterization and debugging purposes.

The primary objective of this design is to downsize the detector for integration into a nanosatellite, specifically a CubeSat structure. The physical considerations related to this, including the PCB design, will be elaborated upon in the dedicated PCB design section. In addition to addressing the PCB concerns, preparing the design to function reliably in challenging conditions like Low Earth Orbit (LEO) involved seeking components with space compatibility or heritage. However, due to cost constraints and limited availability, the focus shifted towards selecting the most durable components meeting industrial standards as close equivalents.

In the intended CubeSat structure, a 5V supply voltage is available. The previous linear voltage regulator utilized in the first design is no longer necessary due to the redundancy constraints of the CubeSat. The circuit's input voltage is the CubeSat's 5V supply, with a zener diode integrated to safeguard against potential voltage spikes that could pose a risk to the circuitry. The former step-up voltage regulator continues to be employed for the quenching voltage, maintaining its original topology.

In the HVA segment, there's been a reduction in passive components to achieve a smaller footprint. Through experimentation, it was observed that the filtering capacitors aren't crucial for the functionality of the employed HVA. Additionally, the trimpot has been omitted to further minimize the circuit's size. Since the Matsusada TS-0.3P module's datasheet provides a control voltage versus output voltage graph and specifies a control pin input resistance of 10k ohms, determining the R5 resistance value for the desired module output voltage becomes straightforward.

This topology is tailored for compatibility with the Matsusada TS-0.3P module due to its space heritage. The design allows using Qubitrium HVA if needed.

The TEC driver's topology underwent minor modifications, particularly in its feedback stage. In the previous design, it was observed that the thermistor values used as feedback for the step-down voltage regulator ensured a stable temperature

state for the employed APD models (SAP500-T6 and SAP500-T8).

In the high-speed section major simplification adjustments has been done by trimming down unnecessary components, including passives and ICs. The second comparator was identified as redundant. After assessing, it was concluded that the first comparator has a smaller footprint and better bandwidth compared to the counterpart. Additionally, the unused pins of the second comparator, such as latch and Q not, further supported the decision to replace it with the first comparator based on experimentation. Examining the APD segment of the circuit, the thermistor legs were integrated to stabilize the APD's temperature via the TEC driver. As the APD temperature decreases, the thermistor resistance decreases correspondingly. Consequently, the TEC driver modulates its current output proportionally to maintain the APD's temperature stability. The aim was to keep the resistance between TEC- and GND minimal to avoid constraining the TEC driver's output current below the desired levels. An essential consideration when selecting the resistance from the market is its maximum power rating. Given the high current it would experience, the power rating must surpass the power being driven through it. For instance, if it were set at 1 ohm, and the maximum current through it is 1A, the power across it would reach 1W. This power rating must align with the maximum current flowing through the TEC element of the APD. The resistance serves to limit the current flow; selecting 0 ohms can also be an option. In the event it malfunctions, causing its value to rise above 1k ohms, it significantly reduces TEC current (by at least 1/1000), preventing the cooling mechanism from functioning.

The sensing segment of the circuit has been streamlined in terms of component count. For sensing purposes, a capacitor was deemed sufficient to detect an avalanche pulse. Alternatively, a jumper (0 ohm resistor) could be placed there for sensing purposes. It's been decided that no DC bias is needed at the non-inverting input pin of the comparator since the avalanche pulse itself would raise the voltage. A diode

footprint, like a zener or general-purpose diode, has been included optionally to limit the maximum voltage at that node, acting as a safeguard to prevent exceeding the absolute maximum voltage rating of the comparator's input stage.

A low-value resistor, is situated to convert the avalanche current into voltage. The resistive voltage divider for adjusting the threshold voltage at the inverting input of the comparator has been simplified. At the comparator's output stage, a small capacitor plays a crucial role in preventing unstable oscillation.

A significant alteration from the first design involved redirecting the comparator output, which was initially going to the input of the analog switch, to now feed the switch input with the output from the pulse stretcher. This adjustment was made experimentally and showed that it allows the adjustment of the dead time duration according to the pulse width of the signal output from the pulse stretcher. The main idea behind this modification and the optimization process is precision control of the both output and the quenching pulse durations in order to tailor and maximize the performance parameters of the SPD. Regarding the pulse stretcher segment, changes were implemented to reduce optional components such as capacitive filtering and ferrite beads connecting two nodes, altering the output connector, and linking the output of the pulse stretcher to the input of analog switch. Due to size constraints, these components were minimized, causing a slight reduction in circuit reliability. However, the fundamental operational principle remains unchanged. Furthermore, the output RF connector has been downscaled from SMA to MMCX for a more compact footprint.

The analog switch topology fundamentally stayed similar to the previous version. It still takes its input as a TTL pulse and gives 12V quenching pulse and 0V resetting pulse to the anode of the APD. A basic 0 ohm jumper can be used for connecting the output of the analog switch and the anode of the APD instead of capacitances.

To sum up, the aim was to reduce the size of the circuitry by getting rid of the

footprints that have been put for debugging purposes. With that, the control of the dead time has been implemented as an option for any customer to customize that parameter. The only downside for this design is that there are only two pin headers for the supply voltage to connect with jumper cables. There is no power connector like the previous design's jack connectors. On the other hand, this can be implemented to the design rather easily without resulting major size adjustments to the design.

2.5 Cathode Sensing Based SPD

The concept behind this topology stems from a fundamental approach aimed at segregating functionalities from the conventional anode of the APD. Ordinarily, the APD's cathode solely supplies the high voltage to trigger the Geiger mode. Recognizing that the cathode provides a strictly DC function, I envisioned utilizing the potential AC component—generated by the avalanche current—to understand whether a photon has been detected or not. This technique offers an opportunity to gain a deeper insight into the circuit's operational principles and any potential parasitic properties. By relocating sensing from the anode to the cathode, separating it from the quenching and resetting process, the operations become more autonomous. This separation is anticipated to enhance the detector's saturation rate (in other words, bandwidth) and enhance the circuit's efficiency in converting avalanche pulses into digital electrical pulses which can be identified as electrical detection efficiency.

Another advantageous aspect or simplification arises from previous designs where the sensing node's work of maintaining the avalanche, quenching, and resetting pulses. That configuration made circuit stabilization challenging. In this new topology, by separating these pulses, it becomes significantly easier to stabilize the sensing part. Moreover, this separation provides flexibility to optimize the threshold voltage for sensing at the comparator, specifically focusing on the avalanche pulse. This approach allows us to closely focus on the threshold voltage (noise level), thereby enhancing

detection efficiency and the circuit's bandwidth. On the other hand, sensing from the cathode, poses challenges particularly in detecting the avalanche pulse without affecting the efficiency of the high voltage supply to the cathode. Typically, the HVA supplies' output directly connects to the APD's cathode. To isolate the avalanche pulse (AC) from a DC node, a small resistance is initially required, inducing a voltage drop from the HVA output to the cathode of the APD. This step separates the cathode and HVA output nodes. Sensing the AC component at the anode (avalanche pulse) involves placing a capacitor between the cathode and the designated node for coupling the sensed pulse (comparator input). This topology can be categorized as the mixed quenching.

A possible key factor to consider is a slight reduction in detection efficiency. The resistor placed between the cathode and the HVA output leads to passive quenching and reset actions independently from the circuit's active quenching operation. This situation concerns us because this resistor could impact quenching and resetting while not directly affecting sensing. To mitigate this, the resistor's value must be minimal to minimize its influence on quenching and resetting without interfering with sensing. Consequently, during the debugging phase, fine-tuning this value will be a challenge.

At the start of this design, we opted to include debugging (optional) footprints carried over from previous designs to address any potential issues. Additionally, we incorporated various supply voltage values to assess their potential impact on the circuit's operational principles. The supply segment closely resembles previous designs. It incorporates a power jack connector for plug converters, a zener diode serving as a fuse, a 5V linear voltage regulator, a step-up voltage regulator providing a 12V quenching voltage, along with passive components used for biasing and filtering purposes. Moreover, a 3.3V linear voltage regulator has been introduced to investigate potential dependencies of the circuit on its supply voltages. A jumper has been added to enable connection to the 3.3V regulator if necessary. Except for the addition of the

3.3V linear regulator, the existing circuitry has been retained due to its consistent performance.

The high voltage amplifier (HVA) and TEC driver sections haven't undergone significant changes. In comparison to the first design, the HVA segment had changes such as the removal of certain optional components, like the 6V connection and extra ferrite beads. It was observed that the 6V supply voltage had no noticeable impact on the HVA's operation, rendering the connection redundant. Additionally, the removal of the extra ferrite beads, replaced with 0 ohm jumpers, didn't affect the paths due to minimal existing noise, leading to their exclusion from the design.

Similarly, the TEC driver segment had minimal alterations. Since it was thoroughly tested for functionality and conditions, substantial changes weren't necessary. This design aimed for an adjustable current output to the TEC, hence the inclusion of a trimpot. The only adjustment based on experimental data was the reduction of the feedback resistor value in order to achieve a broader range of current output, in other words, increasing the sensitivity from temperature alterations of the APD (the thermistor value changes).

The high-speed segment of the design, maintains identical ICs to ensure simplicity and reliability. The primary goal of this design iteration is to evaluate the effectiveness of the cathode sensing technique and assess its potential benefits. As such, alterations beyond sensing have been minimized. Another modification from the first design is the connection scheme; the output from the comparator now directly goes to the flip-flop, which in turn controls the analog switch, aligning with the CubeSat compatible version.

The components surrounding the APD are highlighted. As previously explained, the addition of ballast resistor facilitates the separation between the HVA output node and the APD cathode. This segregation enables the cathode node to retain an AC pulse upon an avalanche occurrence. A capacitor couples this AC pulse to the

comparator's input stage for avalanche pulse detection. Previous experiments have optimized the capacitor to be picofarad range. The thermistor pins serve as feedback for the TEC driver to maintain the temperature stability of the APD. Finally, the inclusion of a resistor aims to restrict the maximum current flowing through the TEC pins of the APD. It is crucial to consider the power rating of the resistor; selecting a resistor with a low power rating may lead to burning and subsequent disruption of the cooling mechanism in the circuit.

The sensing (comparator) section, retains the previously used comparator due to its simplicity and high-speed operation. Although not significantly altered, several changes have been included to fine-tune the circuit's performance. Resistive divider with trimpot collectively manage the DC offset voltage, optimizing the sensing process. Meanwhile, a feedback mechanism has been integrated, either from the comparator itself or from the D-type flip-flop output, to reset the comparator's state. Two jumpers are inserted to choose the supply voltage for the comparator, exploring whether the voltage range affects the circuitry's speed. Despite minimal changes, these components offer opportunities for fine adjustments in the circuit's functionality.

The output stage of the comparator has remained unchanged; hence, only additional resistances have been included. These connectors offer options for exploring new configurations or isolating connections between nodes during the debugging process. An output capacitor plays a crucial role in maintaining the comparator's stability. In case of high-current drive and unstability a series resistance can be utilized to sustain a stable voltage for the node as a reference.

In contrast to the first design, a significant alteration has been implemented: the connection from the flip flop's output to the analog switch. Previously, the comparator output managed both the flip flop and analog switch inputs. With this modification, the comparator output solely controls the flip flop input. The flip flop then directs its output to both the RF connector (SMA) and the analog switch. This change aims

to regulate the duration of the circuit's dead time, adjustable by modifying the pulse width of the flip flop output.

In the pulse stretcher section, two jumpers are utilized to select input supply voltage values, aiming to determine whether a lower supply voltage can expedite the operation of the flip flop. The pivotal section involves the feedback between the inverting output and the negative clear input. Similar to previous designs, an RC filter topology (time constant) is integrated, the rationale for which was discussed in the first design. The specific values of the capacitances and resistances configure the output pulse duration of the pulse stretcher.

As previously mentioned, the output of the flip flop triggers the analog switch to generate either a quenching or a resetting pulse. When the rising edge or high logic value is detected by the analog switch, it initiates the quenching process, duration of which is contingent on the pulse width. Subsequently, the resetting process is activated by the falling edge of the pulse. If the pulse stretcher's output pulse duration is too short, it might inadequately execute quenching, resulting in afterpulsing. Hence, the aim is to optimize the pulse width to enhance the quenching process. The analog switch section remains unchanged in its output functionality.

2.6 InGaAs SPD Configuration

For InGaAs APD, the cathode sensing-based SPD design has been utilized. Because that design enables a lot of different debugging opportunities. Every parameter for a single photon detector can be controlled, such as dead time, comparator threshold, HVA output voltage, quenching, and resetting time. The InGaAs APD would be a new semiconductor used in this circuit, the expectations were to be faced with lots of debugging and optimization situations. The selected APD for InGaAs was RMY's PGA-314-100 [24]. The experimental results will be discussed in the Testing, Debugging & Electronic Characterization section.

2.6.1 HVA Topology

The Qubitrium HVA employs a distinctive combination of two fundamental methodologies to generate its output. Initially, it utilizes a step-up (switching) voltage regulator capable of generating high-voltage switching pulses, reaching peak-to-peak amplitudes of up to 120 volts. An exceptional aspect of this setup is its adaptability; employing a feedback mechanism from the output to the step-up voltage regulator's feedback pin allows for fine-tuning the voltage swing. This adjustment is achieved through a resistive divider topology, providing precise control over the amplitude of the output pulses.

Additionally, the design integrates diode multiplication stages to further amplify the signal. These stages increase the amplitude of the signal by a factor of 3, resulting in an amplified output reaching approximately 360 volts in peak-to-peak amplitude. However, the output signal is oscillating. For practical applications requiring stable DC voltage, such as most electronic devices, rectification is essential. Rectification diodes are incorporated into the circuit to convert the oscillating signal into a steady, direct current (DC) voltage. This conversion enhances the applicability and usability of the signal in various electronic configurations and experimental setups.

2.7 PCB Designs

During the design process of the PCB, the Altium PCB Designer software was utilized. The board layout design consists of four layers: Top layer, two GND layers, and bottom layer. The PCB material employed is FR4 because of its accessibility and reliability. High-speed circuits such as SPD implement a 50-ohm impedance. According to the impedance calculations the trace width corresponding to a 50-ohm impedance equates to 0.378mm for FR4. The 3D images of the PCB design are shown in Figures 3 and 4.

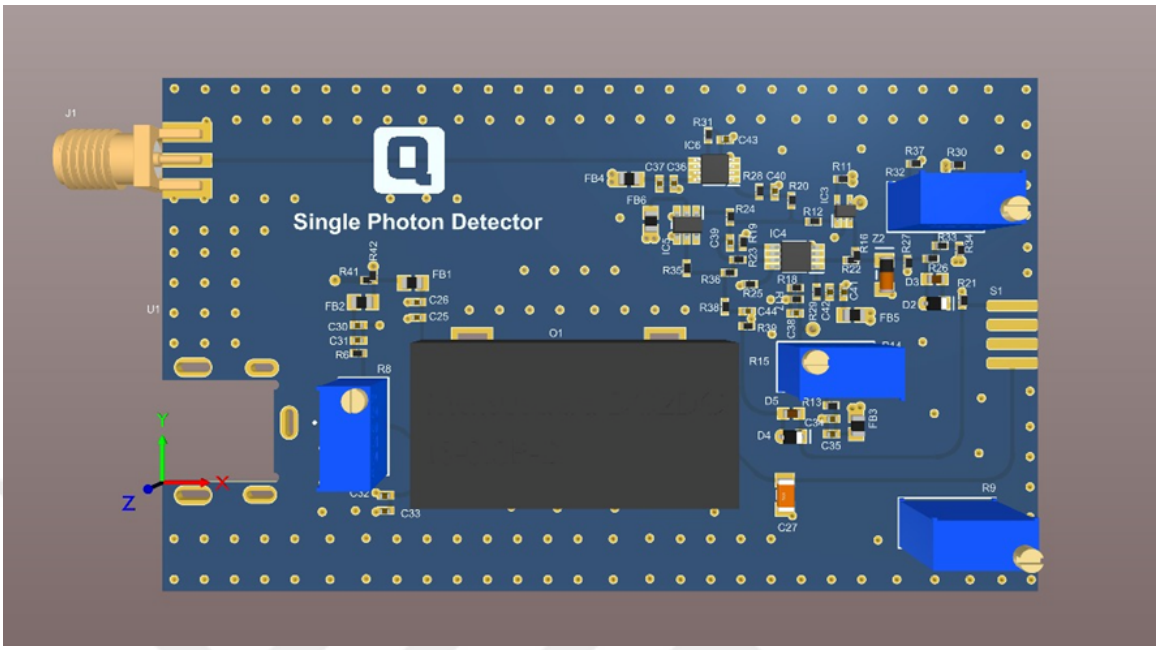

Figure 3: The 3D view of the first design's PCB (Top view)

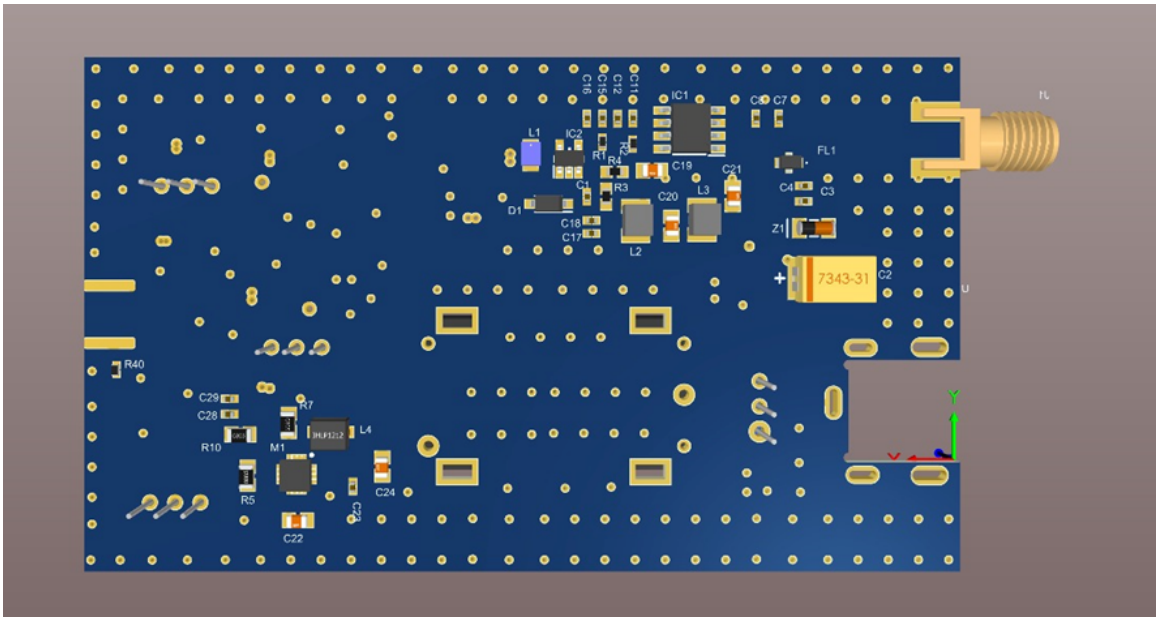

Figure 4: The 3D view of the first design's PCB (Bottom view)

The top layer comprises the resetting, sensing, quenching, and output topologies,

along with the HVA segment of the design. Trimpots are used in four sections of the circuit to facilitate easier determination of ideal resistance values during testing.

The HVA segment features an HVA module measuring 28mm x 16mm, powered by +12V, capable of outputting up to 300V. The green and yellow-colored traces on the above image depict the pathways for resetting, sensing, quenching, and the high-speed output sections, designed to maintain a 50-ohm impedance (0.378mm trace width) where applicable.

Attention was given to maintaining proper track widths and keeping pathways short in the high-speed circuitry section of the PCB design. Integrated circuits and passive components in this section are placed closely but not densely, ensuring ease of soldering. GND vias across the PCB aim to minimize potential noise. These vias have a minimum hole size of 0.3mm, although the exact size may vary between manufacturing companies.

The bottom layer of the PCB encompasses the DC segment (+5V, +6V, +12V) and the optional segment, dedicated to cooling the APD. The TEC segment, due to its high current requirements and the absence of high-speed circuits, is placed on the bottom layer. In contrast, high-speed circuits generally reside on the top layer due to the need for shorter traces. In this regard, the majority of the top layer is comprised of high-speed circuitry, while wider traces are preferred for circuits carrying high current, hence the TEC segment being placed on the bottom layer.

The CubeSat compatible and the cathode sensing PCB designs have been made with exactly the same rules as the first design. The 3D and layout images are shown in Figures 5, 6 and 7.

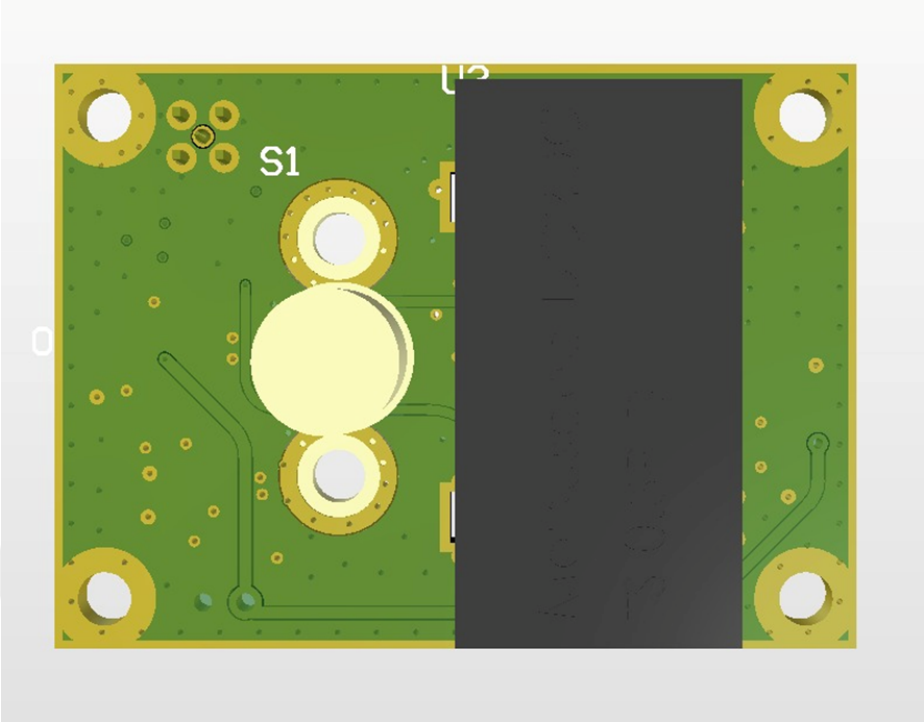

Figure 5: The 3D view of the CubeSat compatible design's PCB (Top view)

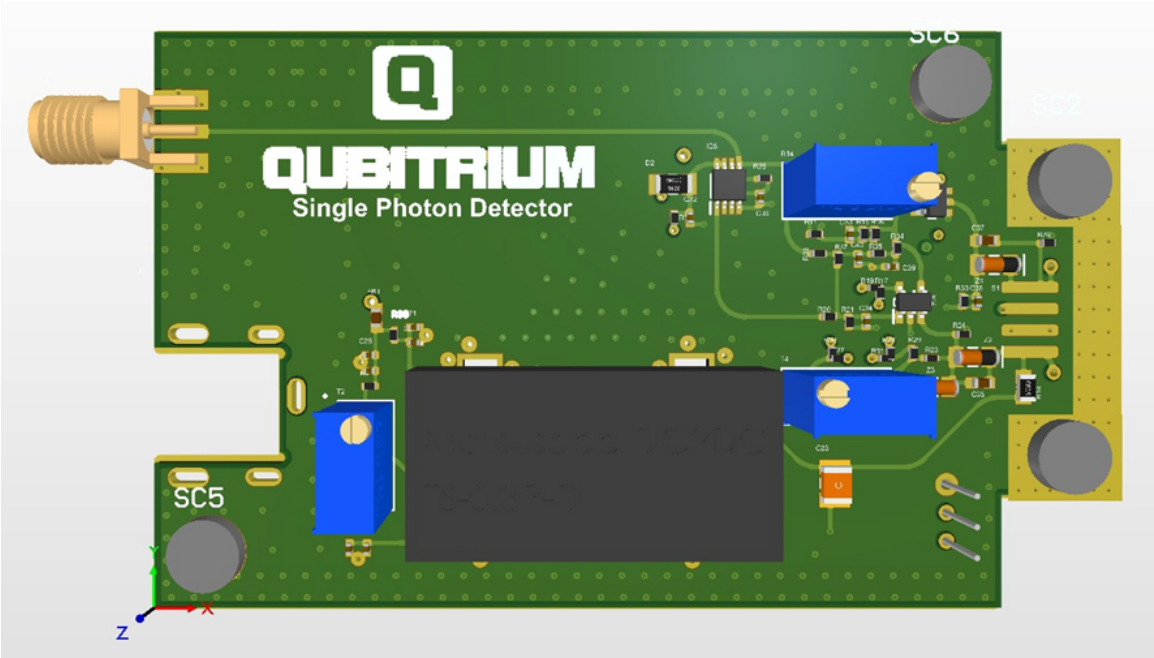

Figure 6: The 3D view of the cathode sensing design's PCB (Top view)

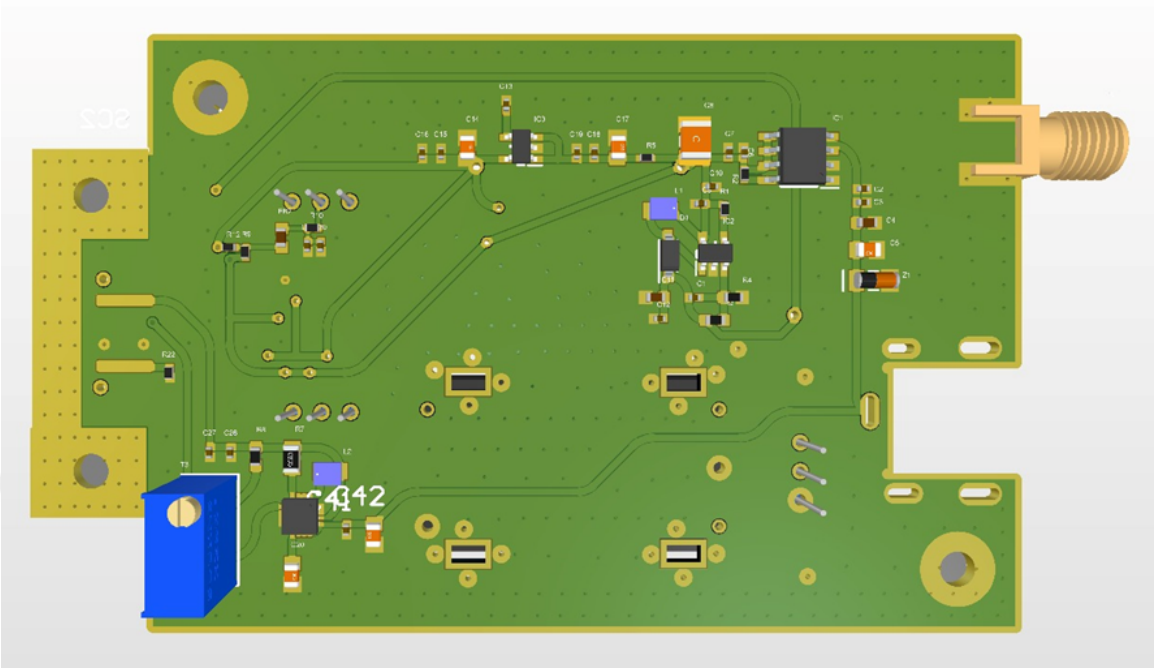

Figure 7: The 3D view of the cathode sensing design's PCB (Bottom view)

2.8 Testing, Debugging & Electronic Characterization

Each testing and debugging phase commences with the assembly of the design. Simultaneously initiating soldering and testing has proven beneficial in promptly identifying potential issues. Consequently, these processes are divided into at least three main sections (which can vary based on the design): the DC segment, the high-speed segment, and the functional segment. For single photon detectors, the segments are the DC part, high voltage amplifier segment, high-speed segment, functional segment, and an optional segment, respectively and in sequence. These segments will be detailed for each design in subsequent sections denoted by their specific names.

During the testing and debugging, measurement tools like a 30V - 3A power supply, a multimeter, and Rohde Schwarz oscilloscopes (with bandwidths of 100MHz and 1GHz) were utilized. Throughout most sections, the oscilloscopes were set to a 50MHz filter, while in the high-speed analysis, the maximum bandwidth filter was

engaged (with the 1GHz oscilloscope using a 500MHz filter window by default). While there was no option to operate without the filter, the 500MHz filter window was chosen as the most suitable setting for this process.

2.8.1 First Design

2.8.1.1 DC Segment

The testing and debugging procedure commence with populating regulators, primarily the voltage regulators, along with the adjacent components. The main goal is to assess if any issues arise without any load connected to the output of these regulators. Components were pre-soldered before initiating this process. A power supply is employed to provide a 6V supply voltage to the circuit. This voltage is either delivered through a jack connector or via two basic jumper cables connected, linked to the power supply providing the 6V output.

Two primary aspects need identification: the AC noise level within the circuit and whether the ICs are outputting the expected voltage values. Ground noise was measured at $<$ 2mVpp with a 20MHz filter and $<$ 7mVpp with a 500MHz filter, shown in Figure 8 and 9 respectively. The AC noises at various nodes were negligible enough to proceed. Specifically, the noise measured $<$ 7mVpp at 6V input (Figure 10), $<$ 7mVpp at 5V input, $<$ 7mVpp at 5V output (Figure 11), and $<$10mVpp at the 12V output (Figure 12). The 12V node's noise shows contributions from the circuit's components and a ripple component sourced from the output of step-up regulator's switching topology. In this configuration, the voltage values aligned perfectly with expectations. A 6V input supply, along with 5V and 12V, were observed accurately. Both regulators demonstrated proper voltage output regulation due to the surrounding components (filters, rectifiers, etc.). It's important to note that these regulators were evaluated without any connected loads.

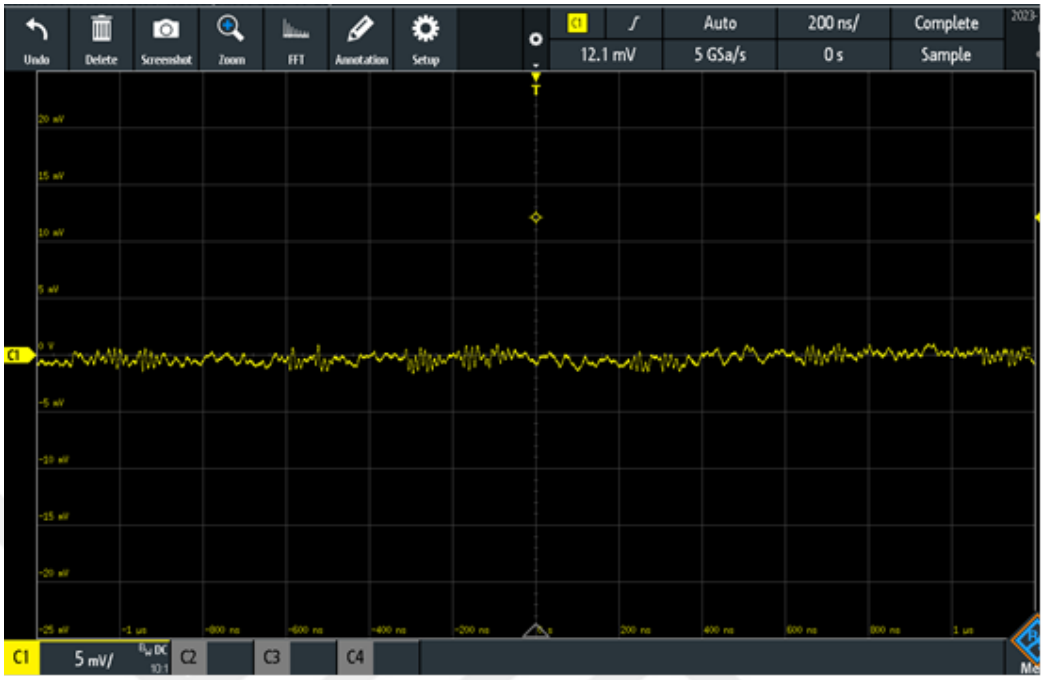

Figure 8: The ground noise of the design with 20 MHz oscilloscope filter

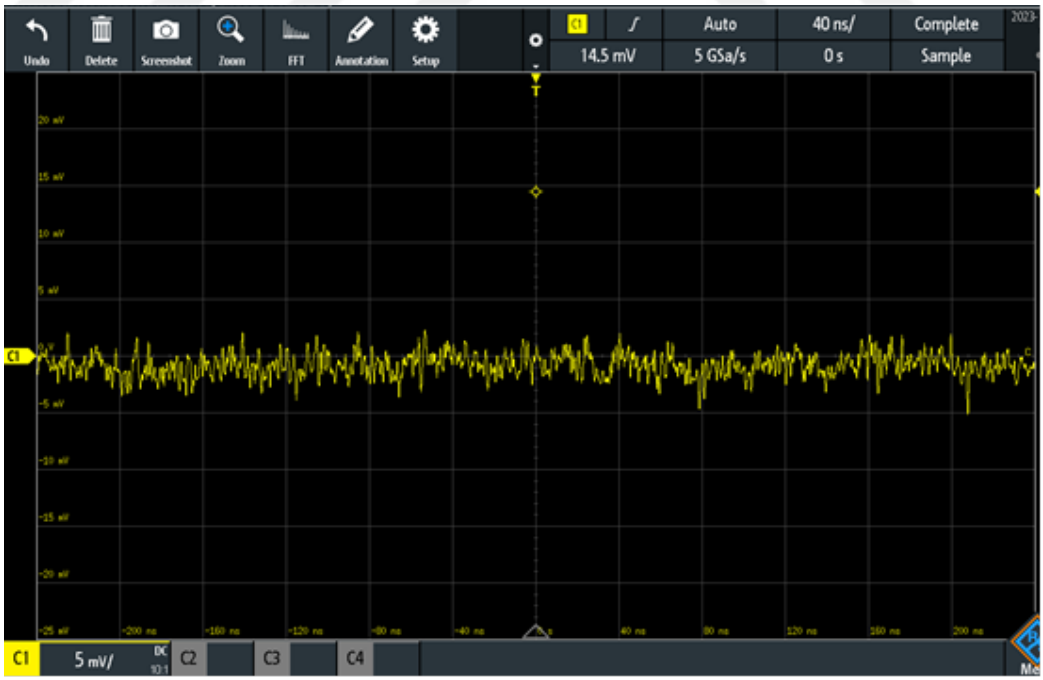

Figure 9: The ground noise of the design with 500 MHz oscilloscope filter

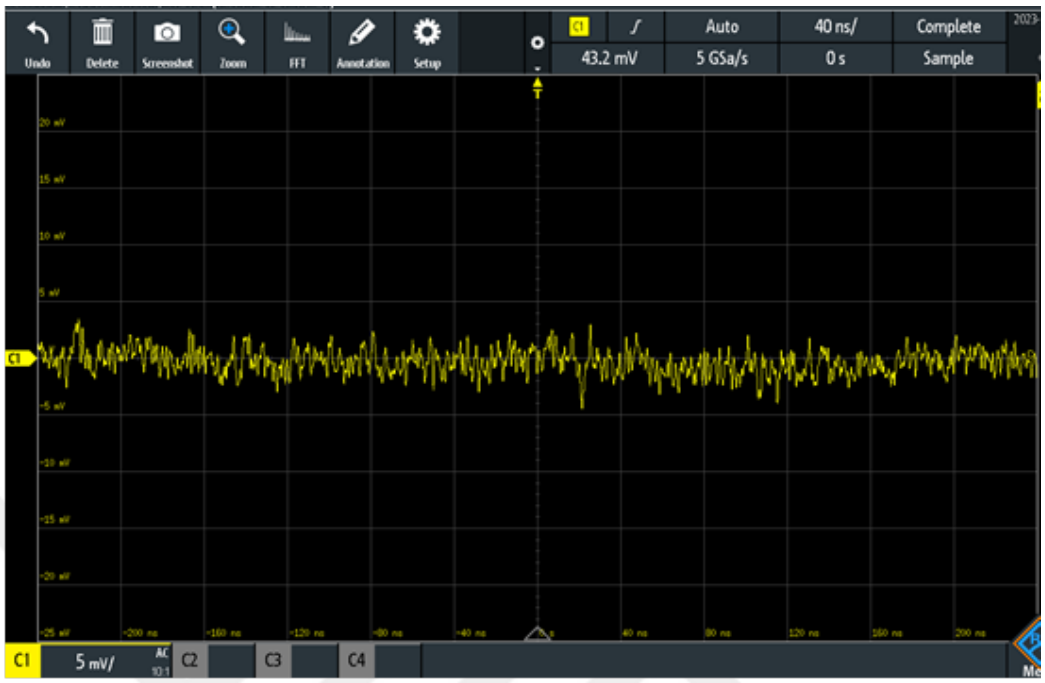

Figure 10: The 6V input noise of the design with 500 MHz oscilloscope filter

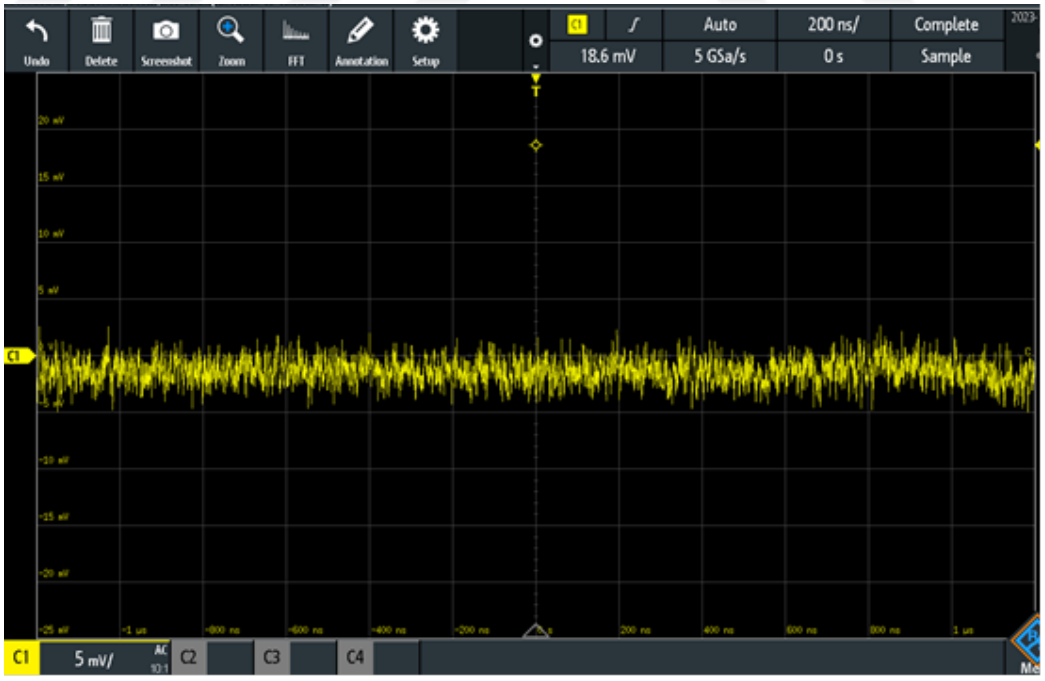

Figure 11: The 5V output noise of the design with 500 MHz oscilloscope filter

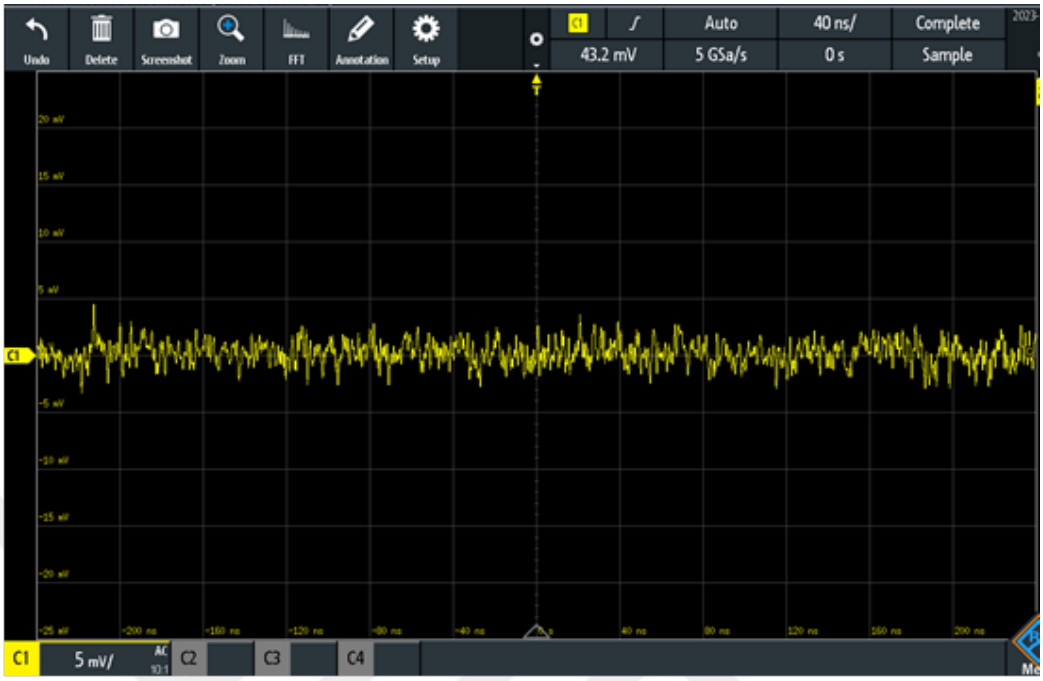

Figure 12: The 12V output noise of the design with 500 MHz oscilloscope filter

A minor issue surfaced upon soldering the high-speed section, specifically affecting the DC part. Consequently, this concern isn't detailed within the high-speed section. Upon applying loads to regulators, including components like comparator, flip flop, HVA, and analog switch, the 5V voltage regulator experienced notable noise levels, approximately 500mVpp at its output, at a frequency around 20MHz. This noise manifested across GND, the supply input, and the regulators' outputs, exhibiting a dominant presence. Given the noise's prevalence, especially at the input, it became evident that one of the regulators entered an oscillation state. A thorough review of the regulators' datasheets led to a decision. Typically, such components integrate relatively large capacitors to the GND at their inputs and outputs, although this was not explicitly stated in their datasheets. Initially attributing the issue to the linear regulator, we experimented with progressively larger capacitors (22uF or more) at both the input and output stages of IC1. This adjustment yielded stable operation across various loads for the IC1.

Design principles discourage overly large total capacitance in circuits. Additionally, in single-photon detectors, the APD is highly sensitive to electrostatic discharge (ESD). Hence, minimizing total capacitance is preferred. While 22uF capacitors suffice, for enhanced reliability and error margin, a recommendation stands to employ 100uF capacitors for both the input and output stages of the linear voltage regulator. In the event of instability with step-up regulator, incorporating an output capacitor around 22uF between the output and the GND is also advised.

2.8.1.2 HVA Segment

In the HVA segment, testing and debugging were relatively straightforward due to the absence of integrated circuits in the design. As outlined in the circuit design description, the HVA's role offers two options: The Matsusada TS-0.3P and the Qubitrium HVA module. It's essential to note that the Matsusada TS-0.3P requires a 12V supply voltage within a 1V error margin and necessitates a voltage control input. Conversely, the Qubitrium HVA module operates across a wider supply voltage range and accepts a control resistance input. The design has been configured to accommodate either HVA module.

For the Matsusada TS-0.3P, decoupling capacitors can be soldered to filter out noise if present at their nodes. A resistive divider should limit the maximum voltage for control pin to align with the Matsusada TS0.3P's input control voltage range of 0V to 10V and an input resistance of 10k ohms at the control pin to GND, detailed in its datasheet. If opting for the Qubitrium HVA module, either the 6V or 12V input can be used. In both scenarios, the trimpot plays a pivotal role. For the Matsusada TS-0.3P, it fine-tunes the input DC voltage, while for the Qubitrium HVA module, it adjusts the resistance input to control the output voltage. In both modules' output stages, the high-voltage capacitors should be as large as feasible to deliver sufficient current with minimal voltage ripple. Aim for a value exceeding 150nF; if possible,

moving into the uF range would be even more advantageous.

The objective of this test was to determine the AC noise level of the HVA modules under no load. Using an oscilloscope for measurement, when powered up and set to provide a 150V output, less than 15 mVpp of noise was observed (Figure 13). This noise measurement held consistent across different filtering windows of the oscilloscope. This noise figure encompasses both the HVA's output ripple voltage and the general circuitry noise. The Matsusada TS-0.3P exhibited slightly lower noise (<10mV) than its Qubitrium counterpart without a load (Figure 14).

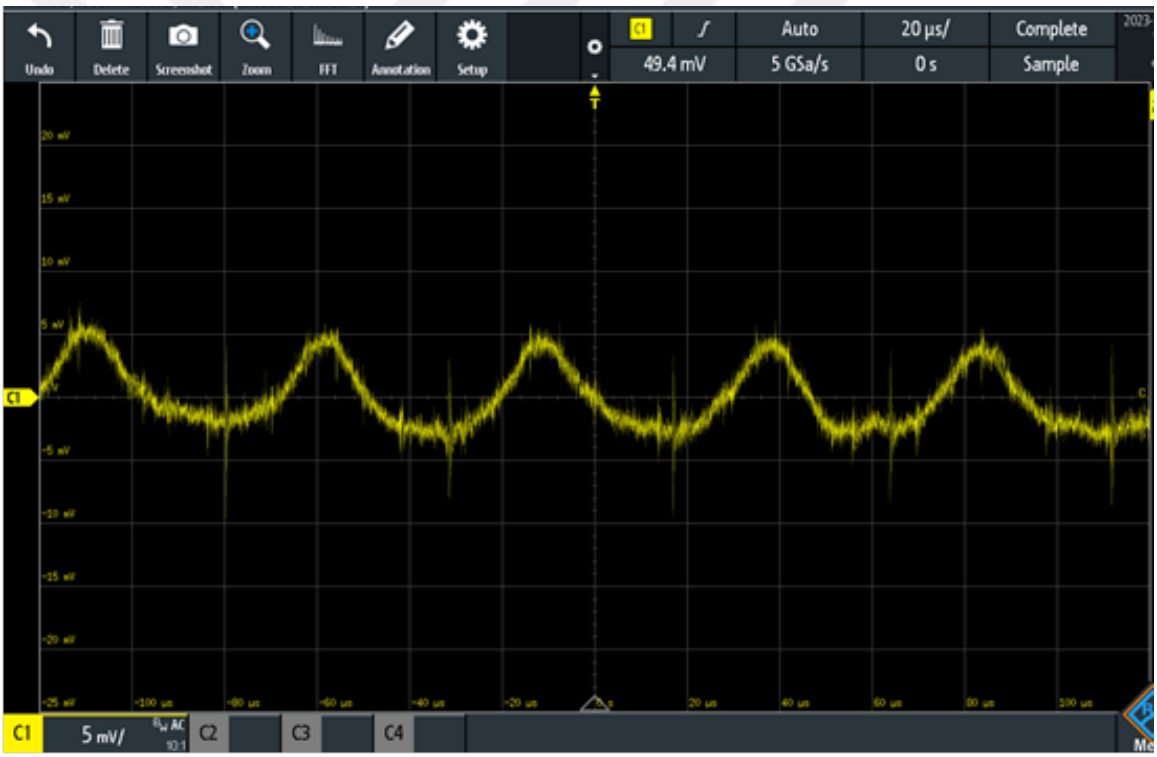

Figure 13: The HVA output noise of the design with 20 MHz oscilloscope filter

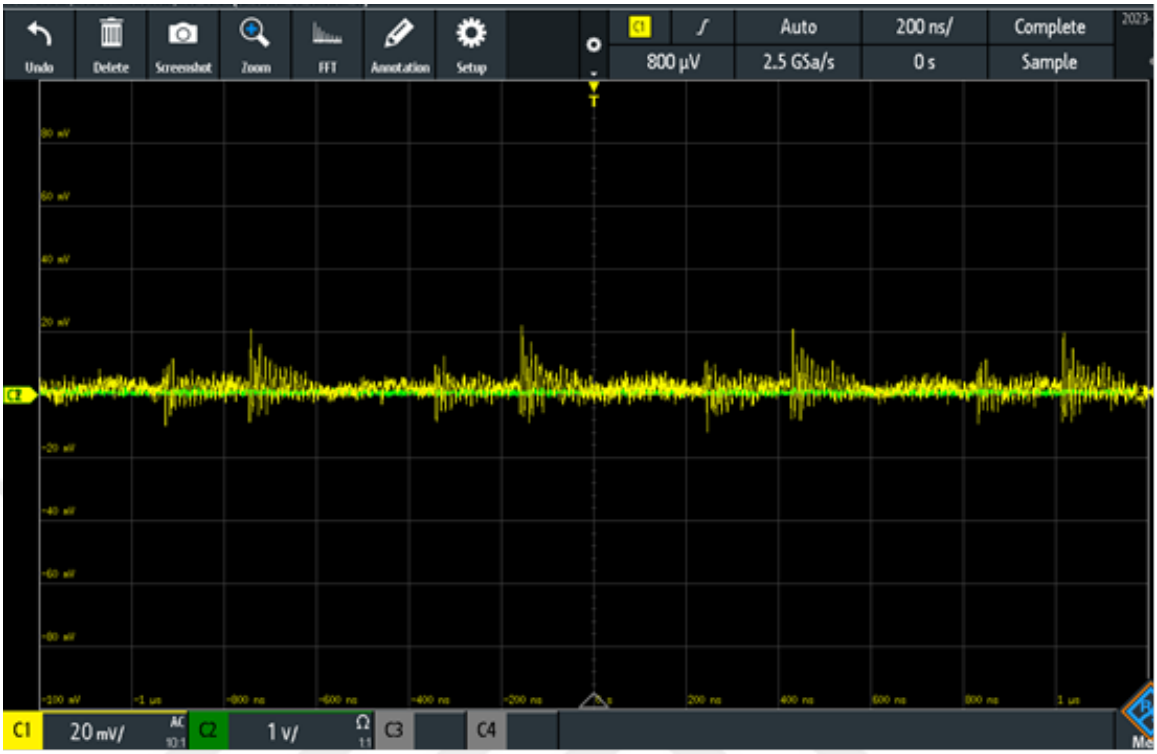

Figure 14: The Matsusada TS-0.3P output noise of the design with 500 MHz oscilloscope filter

Another test was conducted to ascertain the current output values of the high voltage amplifiers. The output voltage was set to 150V, and the output load value was varied (starting from a resistor value of 200k ohms). The resistance value at which the output voltage drops from the set 150V was noted. Results showed that the Qubitrium HVA module can supply up to 3mA of current, translating to a maximum power delivery of 450mW to the load. Conversely, the Matsusada TS-0.3P can supply less than 1mA of current, capping the power delivered to the load at 150mW. The output current measurements hinted that higher current output from the HVA can potentially enhance the detector's bandwidth. The ultra-high-speed avalanche pulse requires more rms (root mean square) current, and a higher current output from the HVA can support this need.

2.8.1.3 High-speed Segment

The testing process for the high-speed section begins after the assembly of the sensing, quenching, resetting, and output components. Notably, the APD hasn't been soldered onto the PCB at this stage. The primary aim is to verify the circuit's operational principle while minimizing any parasitic properties. To mimic the avalanche pulse from the APD, a signal generator will be employed. Similar to simulation, the signal generator can produce a pulse closely resembling the real avalanche pulse. In the simulation, a current source emulated the avalanche pulse. Instead of the APD, a cable was connected to the circuit's anode and soldered to be linked with the signal generator. This signal generator can create pulse signals with 6ns rise and fall times at a maximum repetition rate of 5MHz. As this test aims to verify the circuit's functionality, the signal generator serves to validate the principle. A range of frequencies (1kHz to 5MHz sweep) will be applied to observe the circuit's response. For this test, all ICs were soldered.

This initial test aims to observe the circuit's response when presented with an input similar to the avalanche pulse. The anticipated outcome is a TTL output, a 12V quenching pulse, and a 0V resetting pulse. Notably, the output of the high voltage amplifier was left floating (no load) during this test to prevent any potential harm to the signal generator due to voltage connection. Commencing with a 1kHz signal, 6ns rise/fall time, and a minimum pulse width square wave from the signal generator to the anode, the signal traversed through the sensing capacitor to reach the non-inverting input of comparator. However, the comparator failed to recognize the signal initially. The DC bias voltages at the comparator inputs weren't suitable for signal interpretation. Consequently, adjustments were made: the threshold voltage was set to approximately 15mV using the trimpot. While the non-inverting input node's offset voltage was zero, the trimpot value needed fine-tuning to optimize sensing. It was previously calculated that the sensing resistor should have a small value, around

300Ω. Therefore, the trimpot was adjusted to roughly 350Ω, and the test was repeated accordingly. This time, the pulse was successfully sensed, causing a transition in the comparator's output from 0V (logic 0) to 5V (logic 1). The logic 1 pulse was confirmed and distinctly observable at the relevant nodes. Flip flop's output appeared as a TTL pulse, exhibiting a pulse width of about 16ns. Upon examining the feedback, the delay from the logic 1 to the threshold value of the clear not pin also measured at 16ns. This feedback mechanism appears to modulate the pulse width of the output pin. In the case of the analog switch, the response to the comparator output was observed, transitioning its output from 0V (resetting) to 12V (quenching). However, the 12V pulse wasn't observable at the anode due to the signal generator's connection. The signal generator dominance at the anode limited the 12V pulse to a maximum of 5V. Consequently, the connection was unlinked to isolate the output of the analog switch from the anode. Upon repeating the test, the analog switch was observed to function correctly.

2.8.1.4 Functional Segment

In this phase, the cable connected to the anode was removed, and the SAP500 APD was soldered in its place. To ensure the APD didn't enter Geiger mode upon power-up, the HVA output was reduced to 80V. The initial goal was to determine the APD's breakdown voltage while the circuit remained on standby. Notably, key parameters obtained earlier were the comparator's threshold voltage at around 15mV and the sensing resistor value (to GND) approximately at 350 ohms. Upon powering up the circuit after soldering the APD, no output was observed, indicating it was in standby mode. To prevent any unwanted exposure to light, the APD's active area was either covered and the environment was kept as dark as possible. Even minimal light can saturate the APD, potentially causing harm. Typically, a cap is placed on the APD's head to maintain it in a dark count phase. Gradually, the HVA output increased until

an avalanche pulse appeared at the anode. Once the avalanche pulse was detected, the HVA's output stopped sweeping, and the final value was measured. For this specific APD, the value recorded was 119.8V, signifying the APD's breakdown voltage at room temperature of approximately 23°C.

The breakdown voltage varies across different APDs (at the same temperature). Every time a new APD is employed, regardless of the circuitry used, determining its breakdown voltage is necessary. Interestingly, the recorded breakdown voltage values provided on the APDs' measurement result sheets don't always align with the laboratory-measured results. While they exhibit proportionality, there can be a discrepancy of around 5V between them.

As per the design, the quenching voltage was set at 12V, intending to bias the APD with a 10V excess bias voltage $V_{\text{excess}} = V_{\text{bias}} - V_{\text{bd}}$, resulting in approximately 130V at the HVA output. Increasing the V_{excess} enhances the clarity and sensitivity of the avalanche pulse. Upon adjusting the HVA output to 130V, the detection of the avalanche pulse was observed through the sensing capacitor. This triggered a change in the comparator state from logic 0 to logic 1, consequently activating the remaining circuitry. Subsequent experimentation validated the functionality of the quenching and resetting processes. However, an issue arose with the quenching pulse's width, approximately 26ns (FWHM, Full Width at Half Maximum), indicating an unreliable quenching process. The rise and fall times for the analog switch are both around 10ns, suggesting insufficient time for the signal to remain at the 12V maximum state. Manipulating the control pulse of the analog switch became challenging using the comparator output, as it heavily relied on its input states. Considering the complexity and non-linear nature of the latch option using another comparator, an alternative solution emerged. We proposed utilizing the output pulse from the pulse stretcher to control the analog switch input since the pulse width of the flip-flop was already adjustable.

The initial strategy involved cutting the connection between the comparator output and analog switch input pins, instead linking the flip flop output to the analog switch input. Consequently, a basic jumper cable was employed to connect the pulse stretcher output pin to the input pin of analog switch. Testing the circuit under this configuration revealed an issue: due to the 16ns pulse width of the flip flop output, the analog switch output during quenching failed to reach the intended 12V. Instead, the quenching signal only managed to reach a maximum of around 8V. There was an expectation that the cable used in this rapid reconfiguration might seriously compromise signal integrity, but surprisingly, the signal remained unaffected by this makeshift setup. Following this adjustment, the width of the analog switch output pulse became adjustable by manipulating the pulse width of the pulse stretcher output through its feedback topology. To determine the optimal values, various iterations of the time constant component values were conducted to assess their practical impact on the output. The values acquired, which closely approached the optimized values, are detailed in the Table 1 below.

Table 1: The passive component values for different output pulse widths.

R31 Value (ohm)	C43 Value (Farad)	Pulse Width (ns)
17.8k	1n	80
12k	1n	60
12k	220p	50
12k	1.8n	70
12k	1.47n	62
7.68k	1.47n	54
5.6k	1.47n	48
4.7k	1.47n	42
3.3k	1.47n	38
2.4k	1.47n	34
2k	1.47n	33
1.8k	1.47n	32
1.5k	1.47n	31
1k	1.47n	29

As outlined in the schematic design section, the adjustments in R31 and C43 were aimed at reducing sensitivity (enhancing resolution) in relation to passive component values. Table 1 illustrates the sensitivity of the output pulse width. Through iterations, it was found that the optimal value for the C43 capacitor is approximately 1.47nF. Regarding the R31 resistance, values between 2k and 3k are recommended. Experimental observations have shown that pulse widths around 32ns to 35ns are sufficiently short for effective quenching pulses and are fast enough to minimize the dead time.

The configuration set at a pulse width of 33ns (R31 at 2k ohms, C43 at 1.47nF) retains the quenching pulse at 12V for roughly 20ns, with a FWHM value of about 42ns. To mitigate afterpulsing from the APD, a quenching pulse duration exceeding

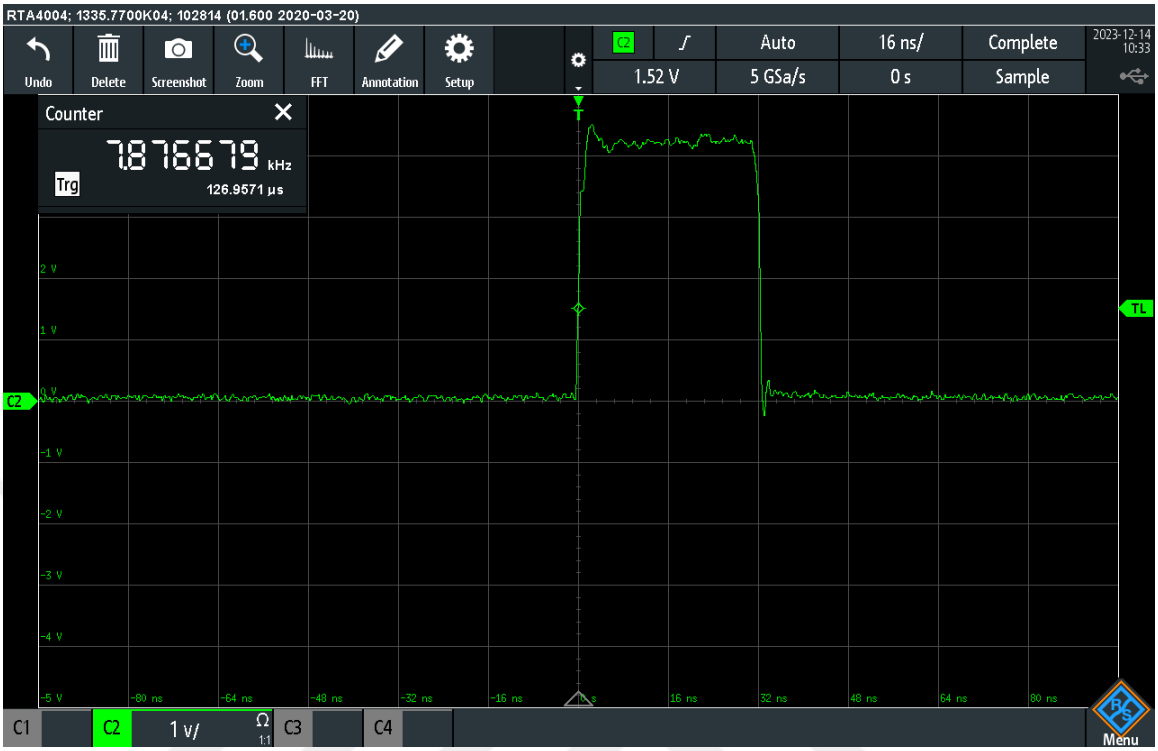

Figure 15: The flip flop output pulse from the design with 50 Ω termination and 500 MHz oscilloscope filter

10ns seemed sufficient. From the values tabulated in Table 1, a 33ns pulse width for the pulse stretcher output was selected, shown in Figure 15. To assess the circuit's bandwidth, the light intensity on the APD was varied from its minimum to maximum levels, covering a range from 10kHz to 5MHz. Notably, the excess bias voltage stood around 10V, and the APD temperature remained unchanged (room temperature of 23 degrees Celsius).

The circuit's input-output efficiency was calculated by simultaneously probing the avalanche pulse (at the sensing node and/or anode) and the output pulse at the SMA connector (specifically the pulse stretcher output at the SMA connector). The oscilloscope displayed the recorded measurements, showcasing the correlation between input and output. Across multiple instances (more than 10 times, each lasting for one second), the match between input and output remained consistent, resulting in a

100% electrical detection efficiency, regardless of varying light intensities (count rates ranged from 10kHz to 5MHz).

Determining the dead time involved measuring the duration between the rising edge of the avalanche pulse and the falling edge of the quenching pulse (resetting). Based on the measurements, the calculated dead time stood at approximately 60ns. Additionally, the timing delay, defined as the time between the occurrence of the avalanche pulse and the output pulse (the interval between their rising edges), was calculated at 18ns.

The circuit's total power consumption was measured at 450mW during dark count and 1W at saturation (without APD cooling). Assessing afterpulsing involved using an autocorrelation function via a time tagging unit, revealing a maximum afterpulsing probability within the bandwidth of less than 2.5% at high count rates.

For detection efficiency, a TCSPC technique was employed with Excelitas' SPCM-AQRH detector as a reference [25]. The results indicated a peak detection efficiency of over 50% at 780nm. Jitter analysis was conducted similarly to TCSPC, evaluating the coincidence cumulative histogram's FWHM value at a count rate of 300kHz. The observed jitter value for this design was below 1ns.

While unpopulated footprints were filled with the intended component range, their inclusion did not significantly alter the discussed parameters. Consequently, the discussed components were retained due to the design's inherent simplicity.

2.8.1.5 Optional Segment

The optional segment of the design focused solely on the temperature control system (TEC driver). Initially, the goal was to verify the TEC driver's ability to cool down the APD, a concept first explored theoretically and through simulation. The initial step involved populating the TEC driver circuit without linking it to the APD, preventing current flow through the APD's TEC element. Upon circuit power-up, probing the

driver output revealed a ripple voltage of approximately 75mV, shown in Figure 16. To mitigate this noise, filtering capacitors, with values exceeding 10nF, were soldered. This action significantly reduced the noise to below 15mV.

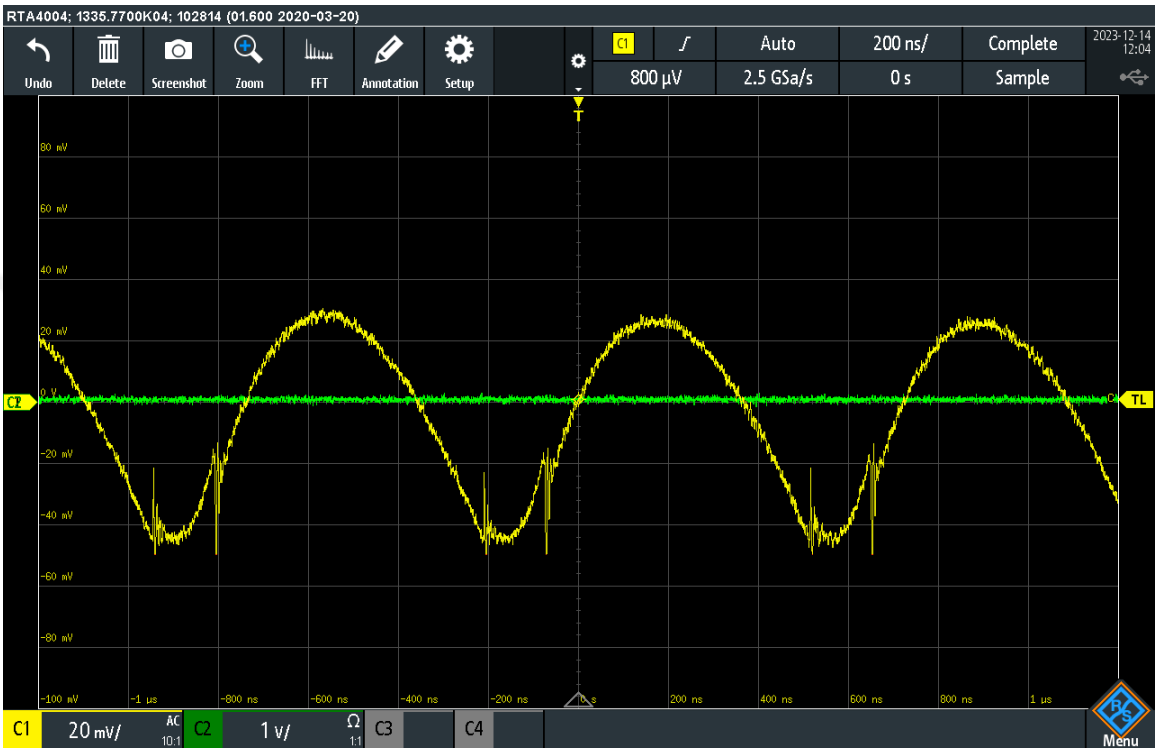

Figure 16: The TEC regulator output noise of the design with 500 MHz oscilloscope filter (75 mVpp, yellow).

A 4.6-ohm resistor was then soldered to prevent overloading the TEC element with excessive current. The output voltage of the HVA was reduced to approximately 80V, preventing the APD from entering Geiger mode before powering up the APD. The primary objective was solely to cool the APD without introducing other potential issues. Subsequent power-up led to a noticeable heating of the heatsink surrounding the APD, indicating successful operation of both the TEC in the APD and the TEC driver circuit. The value of the trimpot was adjusted to explore its correlation with the output current from TEC driver while maintaining the excess bias voltage as

close to 0V as possible. The aim was to enhance cooling, recognizing that a lower breakdown voltage in the APD results in greater cooling. It was observed that as the resistance value of decreased, the current output increased proportionally.

Upon adjusting the circuit to achieve a 10V excess bias voltage during the ongoing cooling process, the aforementioned procedures were reiterated. Two significant changes were noted in the parameters. First, the bandwidth range, previously 10kHz to 5MHz without the TEC driver part active, shifted to 1kHz - 4.9MHz. The dark count rate reduced as anticipated, albeit with a slight decrease in the saturation rate, which remained relatively insignificant. The second change pertained to the total power consumption, increasing in alignment with the current output from the TEC driver.

The subsequent plan involved stabilizing the APD's temperature. During the circuit's design, the paths for the thermistor pins were left unconnected. It was decided to utilize these pins for temperature stabilization, as the TEC driver operates on resistive feedback. Two cables were soldered to the thermistor pins and connected to relevant pads, effectively linking the thermistor pins to feedback resistor, as a parallel resistor. Although this stabilized the APD's temperature, the breakdown voltage remained largely unchanged, suggesting that the other feedback resistors had exceedingly high values.

The process of adjusting the trimpot value commenced, yet even at the minimum setting, there was only a slight change in the breakdown voltage and the APD's temperature. This indicated that feedback series resistor required a significant decrease. Consequently, different values were tested, ranging from 100 Ω to 5k Ω. The optimal value determined through experimentation was 470 ohms for the resistor. The breakdown voltage, set to a relatively low value of 105V, remained stable while adjusting the trimpot. The approximate 15V change in the breakdown voltage correlated with a temperature shift of about 35 degrees Celsius, as per the SAP500-T8 datasheet. Due

to voltage interference from the driver feedback, measuring the thermistor values was not feasible. However, upon powering down the circuit, the maximum resistance at the thermistor pins was observed, indicating an approximate stabilization of the APD's temperature to -15 degrees Celsius. At the stabilized condition, the trimpot value settled at 1.4k ohms, resulting in a reduction of the circuit's dark count to 500Hz. The power consumption increased to approximately 1.3W during the dark count and reached 1.9W near saturation when the APD's temperature was stabilized.

The alternative comparator in the design, was tested once stability was achieved. It functioned similarly to its counterpart without any significant changes observed in the parameters. Consequently, the said comparator can also be effectively utilized in this configuration.

2.8.2 CubeSat Compatible Design

The test and debugging process for the CubeSat compatible version posed fewer challenges compared to the first design. This smoother process stemmed from maintaining identical component values and parameters—paths, impedance values, etc.—as determined in the experimental testing and debugging of the first design. Hence, each component's value was precisely set in the design. Distinguishing features between this version and the first design include the removal of trimpots and the control of the analog switch solely by the output of the pulse stretcher. To accommodate CubeSat compatibility through miniaturization, additional resistor footprints replaced the trimpots. In cases where precise resistance values were required, two footprints were employed at specific nodes, like the HVA control input. Other trimpots, such as those at the comparator inputs, had specific experimentally measured values. Redundant optional (debugging) components from the first design were eliminated in this version, aligning it more closely with an end product. Values derived from previous experimental processes remained intact in this version, maintaining consistency with

the earlier test and debugging process, comprising five distinct parts.

2.8.2.1 DC Segment

As outlined in the design phase, this iteration excludes the 5V linear voltage regulator as the circuitry can leverage the 5V supply from the CubeSat. Hence, this phase solely involves the step-up voltage regulator. Via jumper cables connected to two headers, a 5V supply voltage was introduced into the circuit. GND noise was approximately 7mVpp (with 500MHz oscilloscope filter). The noise level at the input voltage mirrored that of the GND noise. At the output node of the step-up regulator, a stable 12V was observed with an AC component of under 10mVpp. The DC section exhibited stability (without a load), prompting the progression to the subsequent phase.

2.8.2.2 HVA Segment

The Matsusada TS-0.3P module stood as the primary HVA choice for this CubeSat-oriented design, given its space heritage. The components were rearranged to accommodate it within the setup. The key variation from the prior design resides in the control mechanism. As this module features a 10k ohms input resistance at its control pin, series resistances suffice to regulate its output voltage. To determine the output voltage, a basic resistive divider formula was applied based on the control voltage versus output voltage graph provided in its datasheet. The equivalent resistance aimed for roughly 10k ohms to achieve an output voltage around 130V. Depending on the desired voltage, these resistance values could be adjusted accordingly. Upon powering up, the noise figures at both the input and output nodes of the TS-0.3P were under 10mVpp.

Once the APD was soldered for characterization, we put a trimpot. This adjustment aimed to easily modify the HVA output to evaluate the APD's breakdown voltage and determine the total resistance for stabilized excess bias voltage control.

At an ambient temperature of 23 degrees Celsius (without cooling the APD), the APD's breakdown voltage measured about 124V. The combined resistance value required to achieve a 10V excess bias voltage (134V) totaled around 10.7k ohms. To verify the match between the resistances and determine the resulting HVA output voltage, we soldered the resistances and conducted measurements. Due to potential measurement errors, there might have been a relatively larger margin of error. As we iterated through different values of resistances, we eventually attained a 134V output at a total resistance of approximately 12k ohms. This iterative process was necessary for each unique APD. Despite close theoretical estimations, the iterations substantially minimized the error margin for the resistance values.

2.8.2.3 High-speed Segment

In the high-speed section, we've soldered all the associated components. The primary goal was to assess if there were any troublesome noise levels at the high-speed points without any input signals. Fortunately, in a steady state, no issues surfaced. This confirms that the working principle established in the first design experimentation holds true in this PCB. Within this high-speed section, only three optional footprints exist.

In contrast to prior testing methods, we didn't use a signal generator to replicate the avalanche pulse. This decision stemmed from the confirmation of the circuit's previous successful performance in experimentation.

2.8.2.4 Functional Segment

The APD was integrated with a low output voltage from the HVA. Before assessing its functionality, determining the breakdown voltage was crucial, as outlined in the HVA segment. Following the breakdown voltage determination, a 10V excess bias was applied to the APD. Results obtained under various light intensities perfectly matched those from the first design's testing phase. This alignment led to the decision that

there was no necessity for iterative performance enhancements. The primary goal for this design was to achieve the same results and parameters as observed in the previous design.

As an additional point, a diode footprint was intentionally left empty. This decision stemmed from the realization that the node neither reaches negative voltage values nor attains dangerously high, positive voltages for the utilized comparator. Hence, the notion of employing a reverse-polarized diode (anode to node, cathode to GND) appeared unnecessary.

2.8.2.5 Optional Segment

This segment is focused on cooling down the APD. All components were assembled on the PCB, utilizing previously acquired component values. Acting as on/off switch, a jumper, for controlling the cooling operation was soldered, and the circuit was activated. A heatsink was employed to absorb and disperse heat generated by the TEC element within the APD. The power consumption of the circuitry in a thermally stable state (during dark count or outside the Geiger mode operation) was experimentally observed to be consistent with this configuration, at 1.3W. Cooling the APD alters its breakdown voltage, requiring a trimpot to replacing the resistive divider to determine this voltage and set a 10V excess bias. The breakdown voltage for the SAP500-T6 APD settled around 113V, with the total combined resistance measuring approximately 12.8k ohms at an HVA output of 123V. Once this information was achieved, equivalent resistance value was set to the appropriate values to achieve the desired HVA output voltage.

During measurement, the thermistor pins indicated the APD's temperature was near zero degrees Celsius. Power consumption ranged between 1.3W at dark count rate and 1.9W at saturation. All parameters observed in the first design were similarly reflected in this testing process for the CubeSat-compatible design.

2.8.3 Cathode Sensing Design

In the schematic phase, there was a desire to experiment with various supply voltages and, notably, explore the cathode sensing topology. Consequently, the inclusion of the 3.3V linear voltage regulator and the debugging components (similar to those in the first design) was implemented. As per the routine, the initial phases of testing and debugging commenced with the DC section of the design.

2.8.3.1 DC Segment

Relevant components were soldered onto the PCB. This testing phase had two primary objectives. The first was to assess the noise levels at the nodes within this section and, if high, consider implementing filters. The second objective was to verify if the output nodes of the voltage regulators produced the intended voltage values 5V, 12V, and 3.3V, respectively. The noise levels at all nodes in this section were below 10mVpp, matching the GND noise, which was also below 10mVpp. Hence, no additional filtering was deemed necessary. The output nodes +5V, +12V, and +3V3 demonstrated the desired voltage values. It's important to note that the voltage regulators were not under any load yet, resulting in very low circuit power consumption of less than 60mW (as per the minimum resolution of the DC power supply).

2.8.3.2 HVA Segment

This section has been directly adopted from the first design with few modifications. The 6V connection was deemed unnecessary, and due to the absence of noise at the input part of the HVA, the ferrite beads were removed. Since the noise figure of the input stage was less than 10mVpp, no additional decoupling capacitors were soldered. The output of the HVA module exhibited a noise figure (ripple and white noise) of approximately 15mVpp at a 150V output, which is considered an acceptable value. The output voltage was intentionally set below 80V to avoid supplying sufficient voltage for the APD to enter Geiger mode when soldered.

2.8.3.3 High-speed Segment

In this segment, due to the cathode sensing topology, adjustments were needed to reverse the polarity and offset bias at the comparator. Steady-state measurements indicated noise figures below ¡10mVpp at all nodes.

When a signal generator was linked to the cathode, the generator supplied a 1Vpp, 1kHz signal with a -0.5V offset and maximum duty cycle, simulating the effect of an avalanche pulse on the cathode. Despite adjusting the comparator's threshold voltage to 15mV and ensuring no DC offset at the sensing node, the comparator failed to detect the signal from the generator. Upon inspecting the circuit's logic, we realized the polarity at the sensing node was incorrect. The avalanche pulse, being a fast-decreasing signal sensed from the anode, was connected to the comparator's non-inverting input (Vp). In the absence of an avalanche, the comparator should output logic 0. However, the voltage at Vp was lower without the pulse, and when the avalanche occurred, it decreased the Vp voltage further. Consequently, the comparator's threshold (Vn) was consistently higher than Vp, causing it to misinterpret the avalanche pulse.

Given the nature of cathode sensing, we opted to reverse the polarity of the comparator. This involved rerouting the sensing node to the Vn pin and the threshold voltage to the Vp pin. To achieve this, we cut the paths nearest to the Vn and Vp pins of the comparator. Using as short jumper cables as possible, we connected Vn to the sensing part and Vp to the threshold part. Despite these adjustments, when simulating the avalanche pulse with the signal generator again, the comparator still failed to recognize it. This time, it became apparent that the threshold voltage was higher than the DC bias of the sensing node. To address this, a 0 ohm jumper was soldered, adjusting the DC bias to 0V. Additionally, we modified the trimpot values to achieve a sensing part DC bias of approximately 15mV. Following these iterations, the ICs were observed to be functioning correctly.

2.8.3.4 Functional Segment

The HVA output was initially set below 80V, and the APD was integrated onto the PCB, with a ballast resistor soldered to establish the connection between the APD and the high voltage. Gradually increasing the HVA output allowed determination of the APD's breakdown voltage, measured at 123V. Subsequently, the HVA output was adjusted to 133V to provide the APD with a 10V excess bias voltage. There were concerns about the reliability of sensing due to cut paths in the high-speed section. However, experimental testing revealed no adverse effects on signal integrity or performance. The comparator successfully sensed the avalanche pulse, the pulse stretcher produced output triggering the analog switch, and the analog switch effectively provided the quenching and resetting pulses.

Performance tests indicated that, apart from the saturation value of the detector circuit, all other parameters aligned with those of the first design's performance tests. Implementing a cathode sensing topology aimed to enhance the detector's bandwidth, and it indeed increased from 5MHz to approximately 15MHz. During performance testing, iterations were made on the ballast resistor value to comprehend its impact on the measured parameters. After an optimization process, a small value (below kilo ohms) for the ballast resistor emerged as the most suitable.

2.8.3.5 Optional Segment

The optional segment is focused on cooling operations for the APD. Based on the reliability observed in previous circuits and their tests (first and CubeSat Compatible Designs), the employed topology was deemed reliable. The trimpot was fine-tuned to around 1.4k ohms, as per previous results. The APD, placed in a heatsink, had the HVA output reduced to 80V to assess the breakdown voltage at the newly stabilized temperature. The updated breakdown voltage was measured at 111V, and the HVA output was adjusted to 121V to provide a 10V excess bias voltage.

Repeated performance tests confirmed that the parameters achieved previously in the functional section were applicable and valid in this cooling-oriented segment.

2.8.4 InGaAs SPD

Following the completion of the circuit soldering, a 5V supply was applied. No issues were observed in the DC voltages of the circuit (12V, 5V). A reading of 83.4V was noted at the HVA output, and attempts to reduce it using the trimpot proved unsuccessful. Consequently, it was decided to replace the inadequate 20k trimpot with a 50k trimpot. With the new trimpot, a voltage drop was achieved, settling at 56 volts. After concluding the DC tests, noise tests commenced. Switching noise originating from the HVA was detected in the unloaded GND, along with noise from the step-up regulator's oscillator in the 12V output. It was determined that there were no significant issues. A 20mVpp ripple was observed at the HVA output. The breakdown voltage of the diode was calculated to be 75V based on the diode's current breakdown voltage multiplied by the temperature change factor of 0.1. Attempts to enter Geiger mode were made by gradually increasing the voltage with the trimpot from 56V, but Geiger mode could not be achieved. We observe the voltage value at the cathode in the anode as well, and the voltage was maintained at 56 volts. Due to being in the linear mode, we cannot increase the HVA value further as it draws excessive current. Removing the cathode leg of the diode, the HVA output observed was 101 volts. Upon reconnecting the cathode leg to the circuit, it drew nearly 1 amp of current, indicating the APD may be damaged. Repeating the process, the circuit was tested with 107 volts, drawing high current.

The testing process without the APD began on the DC segment on the cathode sensing design circuit where the HVA is installed. The cathode resistance was increased 1000 times in order to prevent any possible voltage peaks and reliability of passive quenching mechanism. It was noticed that the diode drew excessive current,

prompting an inspection. While unused diodes showed a resistance of approximately 1M ohms, on multimeter, between the anode and cathode pins, the diode under examination displayed a measured resistance of about 7-8 ohms between its anode and cathode. This led to the conclusion that the diode was faulty.

Concerned about damaging the new diodes, we reviewed our approach to identify potential issues. We listed several potential problem areas that need attention to minimize the risk of damaging the new diodes. These include the initial testing with a low resistance in the anode, along with the big resistance between the cathode and HVA output, conducting noise and stabilization tests on the HVA before operational use, gating to ascertain the diode's functionality, and prioritizing certain steps from the listed measures for initial testing.

The HVA was fixed at 50V and will be gradually increased to a maximum of 85V. The reason for this increment limitation is the diode's breakdown in the linear mode, which is at 80V. Avoiding damage to the diode, passive circuitry instead of active components will be used, disconnecting all IC component connections in the circuit. Passive quenching will be carried out using resistors. When voltage is applied to the circuit without the diode installed, a high noise level of approximately 25 mV is observed. The noise level is also detected at 25 mV when examining the GND noise, speculated to potentially originate from the power supply. To address this, different power supplies have been tested, and despite using a different power supply, the same 25 mV noise is observed, hinting that the problem might be circuit-related. The noise issue was deemed non-disruptive, and precautions such as using a wrist-attached GND cable was taken to prevent ESD. The diode was installed in the circuit with an anode, cathode, and GND connection. The resistance between the diode's anode and cathode is approximately 1Mohm indicating that it was not damaged. The HVA set to 50V, no avalanche was observed, and a total current of 0.058 A was drawn from the circuit. This process was repeated at HVA values of 63V, 74V, where no avalanche

was observed, drawing currents of 0.061 A and 0.064 A respectively. However, at 80V, an avalanche was observed with a peak-to-peak of 45 mV, with a maximum frequency of 30kHz and an average of 25 kHz, indicating an approximate dark count of 25 kHz. The circuit drew a total current of 0.064 A. At room temperature, the breakdown voltage of the diode measured 79.5V with a multimeter. The HVA was stabilized at 80.4V, producing an avalanche peak-to-peak of approximately 100 mV and drawing a total current of 0.065 A (Figure 17).

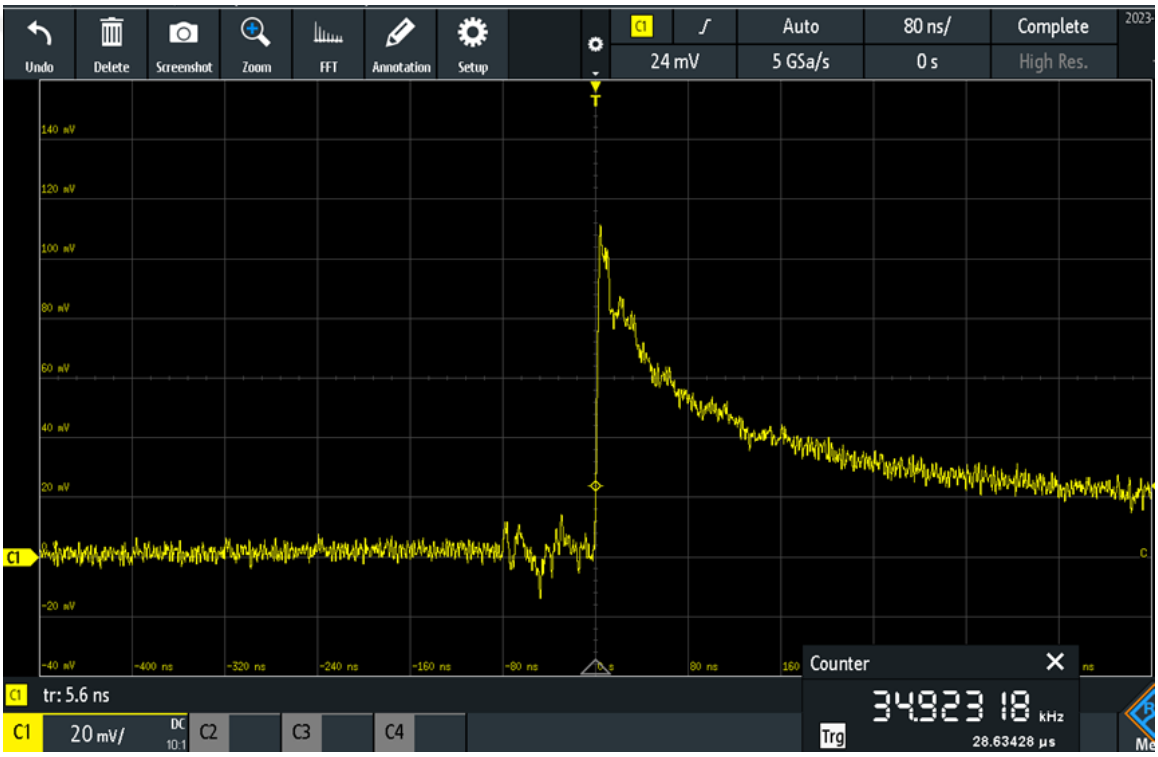

Figure 17: The oscilloscope screenshot of the avalanche pulse when the detectors dark count rate was about 35 kHz, with a Vpp of approximately 100 mV

The HVA was fixed at 81V, resulting in an avalanche peak-to-peak of approximately 130 mV and a total current of 0.067 A, with a dark count of approximately 39 kHz. At 81.6V, no significant changes were observed, maintaining a dark count of approximately 35 kHz. Progressing to 82V from HVA output, the dark count decreased

to 16 kHz, with a total current of 0.068 A, and an average avalanche peak-to-peak of 110 mV. At 82.6V, the dark count further reduced to 2.5 kHz, drawing the same total current of 0.068 A, with an average avalanche peak-to-peak of 95 mV. Reaching 83.2V, the dark count decreased to below 1 kHz, maintaining a total current draw of 0.068A and an average avalanche peak-to-peak of 80 mV. Considering the observation of avalanche in passive quenching and achieving the desired results, a decision has been made to transition to the primary process of active quenching. The APD was removed from the circuit to proceed with active quenching tests. Initially, the circuit only had a DC section. Components like the comparator, analog switch, and flip-flop on the active side of the circuit were soldered, and necessary resistors and capacitors were installed. Later, an APD was added for testing. Before attaching the APD, the ballast resistor at the anode was replaced with a slightly bigger resistor. Subsequently, the APD was installed to commence testing.

The HVA output was set at 57V. The HVA output was gradually increased up to 79V without observing any avalanche occurrences. At 79V, minor avalanches began to appear, coinciding with a comparator threshold of 20 mV. Approximately 50 kHz frequency was observed at 79V. Around 80.2V, the frequency at the anode node reached approximately 900 kHz, consistently observed across all points. As the HVA output increased, the frequency decreased from 900 kHz to 800 kHz. It was apparent that there was considerable noise around 900 kHz. To filter this noise, the threshold value was raised to around 40 mV, resulting in an observed frequency of approximately 225 kHz. It was noted that when the threshold was at 20 mV, the frequency fluctuated between 700-950 kHz. Raising the threshold to 40 mV led to an observed frequency between 215-225 kHz. The hypothesis suggesting potential noise at lower thresholds was supported by these observations. The circuit was slowed down by extending the pulse width to approximately to 2.6 microseconds to understand whether the suspected noise was circuit-based by increasing the dead time, thereby

reducing the diode's photon count potential. As the dead time decreased, an increase in afterpulse counts was observed. At an approximate dead time of 60 nanoseconds, counts between 800-900 kHz were observed at 2.5V excess bias, indicating an error margin of over 10%. Increasing the dead time aimed to reduce this error margin, and at a dead time of approximately 2.6 microseconds, the error was observed to be below 10 %, approximately 7 %.

The adjustments conducted in the experimental steps aimed to refine the system's performance. Small adjustments were made in a output pulse width to increase it and the dead time to 80 nanoseconds and 100 nanoseconds respectively, contributing to an approximate count rate of 450 kHz. In the subsequent step, the output pulse width was increased to be 135 nanoseconds and the dead time became 155 nanoseconds. The modifications continued. The changes aimed to augment the amplitude of the avalanche pulse, enhancing its distinction from noise interferences. Alongside these alterations, grounding procedures were applied to the HVA. The ballast resistor underwent shifts from 100 kohms down to 20 kohms, optimizing passive and active quenching while aiming for a more efficient excess bias voltage. Other adjustments included lowering the sensing threshold from 40 mV to 20 mV. These series of modifications were conducted to enhance the system's performance and sensitivity, facilitating better operational control and noise reduction.

In the InGaAs SPD, it was observed that as the excess bias voltage increased at room temperature, the number of dark counts proportionally increased. To distinguish whether genuine photons were being counted, a plan was devised to reduce the number of dark counts. Accordingly, a thermal mass design was conceptualized to aid in cooling the APD by direct contact. Due to the considerable time required for the construction and procurement of this design, an improvised thermal mass, thermoelectric cooler, and heat sink were implemented in parallel with this plan. Our

objective was to minimize the APD's temperature, hence we employed a cascaded configuration using multiple 15x15 mm TEC modules successively. Attempting thermal mass cooling without the APD was performed in a cascaded manner. Temperature values were measured using a thermistor. Two TECs were connected in a cascaded manner, achieving temperature stabilization at 6 degrees Celsius as observed in the experiment. To reach lower temperature values, an additional TEC was added to the cascaded module, and the experiment was repeated. Subsequently obtaining a similar stabilization at approximately 6 degrees Celsius, the cascaded configuration was abandoned in favor of conducting the experiment with a single TEC. When the single TEC experiment resulted in a stabilization at around 7 degrees Celsius, it indicated a potential issue with the earlier cascaded process, prompting its suspension for further consideration.

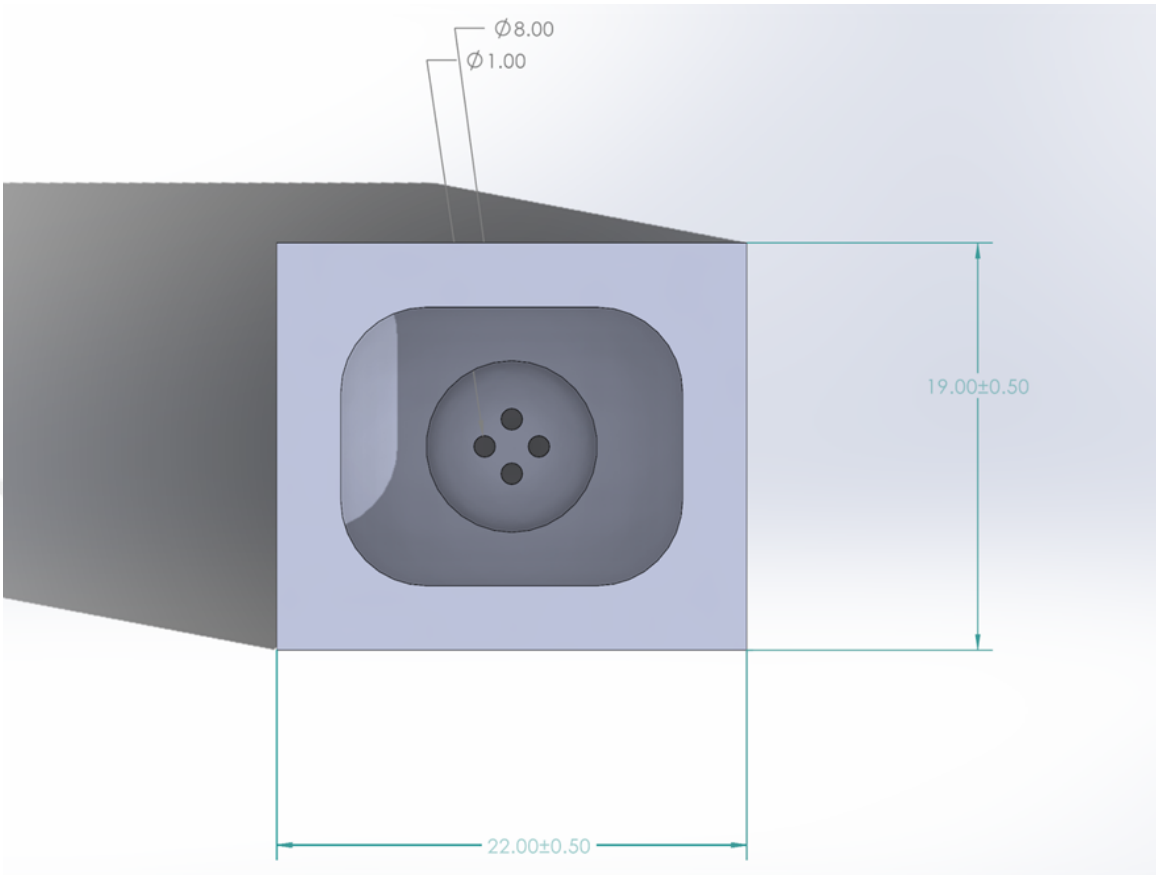

Figure 18: The thermal mass design for InGaAs APDs

During the experiments, the thermal mass we designed was procured (Figure 18). Initially, thermal tests were conducted without connecting the APD. The obtained stabilization value from these tests was recorded at approximately 2.8 degrees Celsius. Due to the better result obtained compared to previous tests, the experiment was repeated by connecting the APD. The test conducted with the APD yielded a temperature stabilization of approximately 3.5 degrees Celsius. While the desired temperature was not achieved, the APD was connected to the active quenching circuit to measure how the obtained temperature affected the dark count value. A decrease in the dark count value was observed based on the excess bias voltage value. This decrease was comparatively lower than the measurements taken before cooling.

As the voltage value supplied to the APD could not be accurately measured using the current HVA module, a plan has been made to transition to a specialized HVA designed for the previously used InGaAs APDs instead. Compatibility assessments have commenced on the existing InGaAs HVA circuit for this purpose.

2.8.4.1 InGaAs HVA

The lower excess bias sensitivity of the InGaAs APD compared to the silicon APDs resulted the previous HVA designs unusable. Additionally, the lower breakdown voltage of InGaAs diodes compared to silicon diodes necessitated a new design approach. Furthermore, the voltage given to the APD could not be measured clearly, because of the sensitivity of the APD. When the HVA output was measured with a multimeter or an oscilloscope probe the APD becomes inactive. This phenomenon indicated that even the sampling signal taken from the probe, decreased the voltage value at the anode of the APD below its breakdown voltage. When determining the regulator to be used, the primary concern, owing to the InGaAs APD's excess bias sensitivity, was anticipated to be the noise level of the high-voltage output. A voltage level of approximately 100V was deemed more than sufficient for the InGaAs APD. It was also desired for the design to match the size of other HVAs used, enabling debugging without the need for a new PCB layout. Following the circuit design, a compact HVA was achieved.

The InGaAs HVA design have been populated and tested without load in order to first understand the voltage range and the noise level. The voltage range was measured to be 0 to 85V and the noise at its output was recorded to be exactly same with the GND noise, ¡10 mVpp. These parameters made the design suitable for InGaAs APD application. After it was assembled with the InGaAs APD, it was seen that, the output voltage regulation was faster than its previous counterparts. Therefore, the output voltage value could be measured without effecting the APD's

performance.

However, the adjustment of the output voltage of this HVA was too sensitive to be precisely set. It was recorded that the APD's breakdown voltage was around 79V. Therefore, in order to increase the resolution of the output voltage adjustment, the planned voltage range for the HVA became 75V to 83V. The output voltage can be adjusted with a basic resistive divider. According to our calculation results, these resistances were set, and the multi turn trimpot value was decreased. Those adjustments enabled the output voltage to be set precisely. When the breakdown voltage of the APD was set, the HVA voltage value was swept according to the dark count rate value of the InGaAs APD.

2.8.5 TCSPC Test

A setup was constructed using TCSPC to assess the optoelectronic properties of single-photon detectors. The primary objectives were to determine the photon detection efficiency and timing jitter, with a secondary focus on evaluating dark count and saturation rates. For this purpose, a correlated single photon pair source was employed to establish timing correlations between the detectors.

Figure 19 illustrates the schematic representation of this setup. A 405 nm pump laser was utilized, collimated by an aspheric lens, and the polarization angle was adjusted using a half-wave plate. The correlated photons, having wavelengths of 780 nm (signal) and 842 nm (idler), were generated through the spontaneous parametric down-conversion (SPDC) phenomenon in a Beta barium borate (BBO) crystal. To filter out the pump photons post-crystal, a longpass filter with a cutoff wavelength of 700 nm was applied. Subsequently, a plano-convex lens was used to collimate the pair photons. A dichroic mirror was employed to separate the 780 nm and 842 nm photons. Following this, mirrors and additional plano-convex lenses were used to focus these respective photons onto the APD of the SPDs. The TTL outputs from the

SPDs were linked to the TSU using SMA cables. The TSU recorded the data and was interfaced with the PC through a USB connection. Through the PC, various metrics such as the count rate for each detector, coincidence data, and the cross-correlation histogram were all accessible and monitorable.

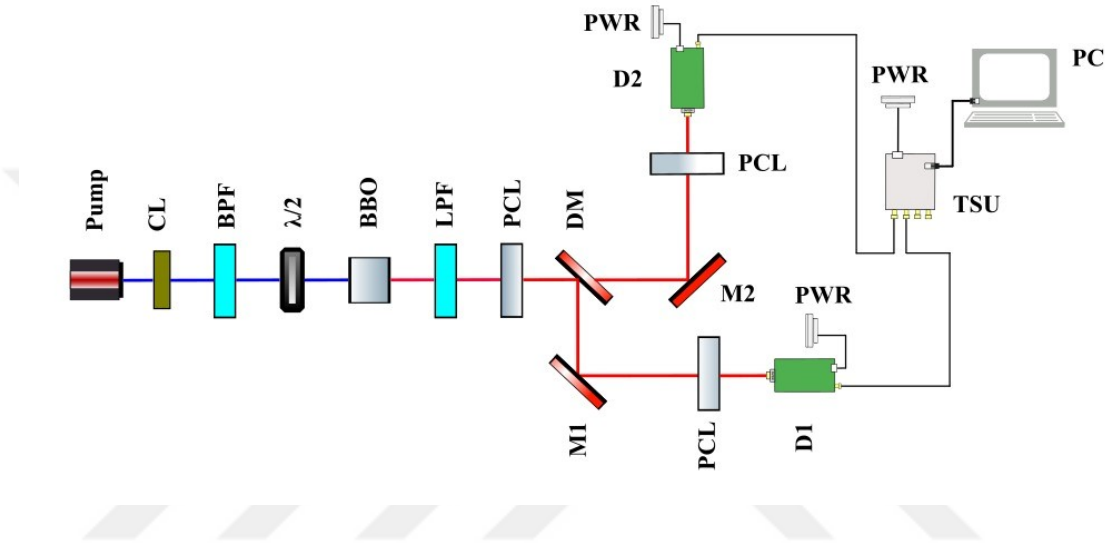

Figure 19: The schematic of the TCSPC setup. Pump: 405 nm laser, CL: Collimation (aspheric) lens, BPF: Bandpass filter, $\lambda/2$: Half-wave plate, BBO: Beta barium borate crystal, LPF: Longpass filter, PCL: Plano-convex lens, DM: Dichroic mirror, M1 & M2: Mirror, D1 & D2: SPDs, PWR: Power supply, TSU: Time stamping unit, PC: Computer

The photon detection efficiency has been determined by a reference detector of Excelitas SPCM-AQRH-14 [25] as D2. All the silicon APD based designs have been used as D1. The detection efficiency was calculated according to the count rate of the detectors, SPCM-AQRH-14's detection efficiency and the coincidence rate. According to the calculations, our detection efficiency at 780 nm for all silicon APD based detectors was 55%. It has been seen that the calculated detection efficiency aligned with the datasheet of the utilized APD, SAP500 [23]. This also proves the

measurement results for the electronic detection efficiency is 100% for those designs.

Timing jitter value was determined by the cross correlation histogram for D1 and D2. We employed a variable neutral density filter in between bandpass filter and half-wave plate in order to adjust the total SPDC photon number. The histogram FWHM value corresponds to the total timing jitter of the detectors. According to the datasheet of the SPCM-AQRH module the timing jitter value is 350 ps. The FWHM value of the histogram was 1.2 ns, therefore the timing jitter value of our designs was 850 ps. This measurement has been recorded when the count rate of each detector was around 350 kcts/s. It's important to note that varying count rates for detectors result in different timing jitter values. Specifically, a detector's timing jitter shows a proportional relationship with its count rate. As the count rate of a SPD increases, the timing jitter value also increases. This correlation was evident in our observations, where an incremental rise in the total count rate for both detectors resulted in a widening of the histogram width.

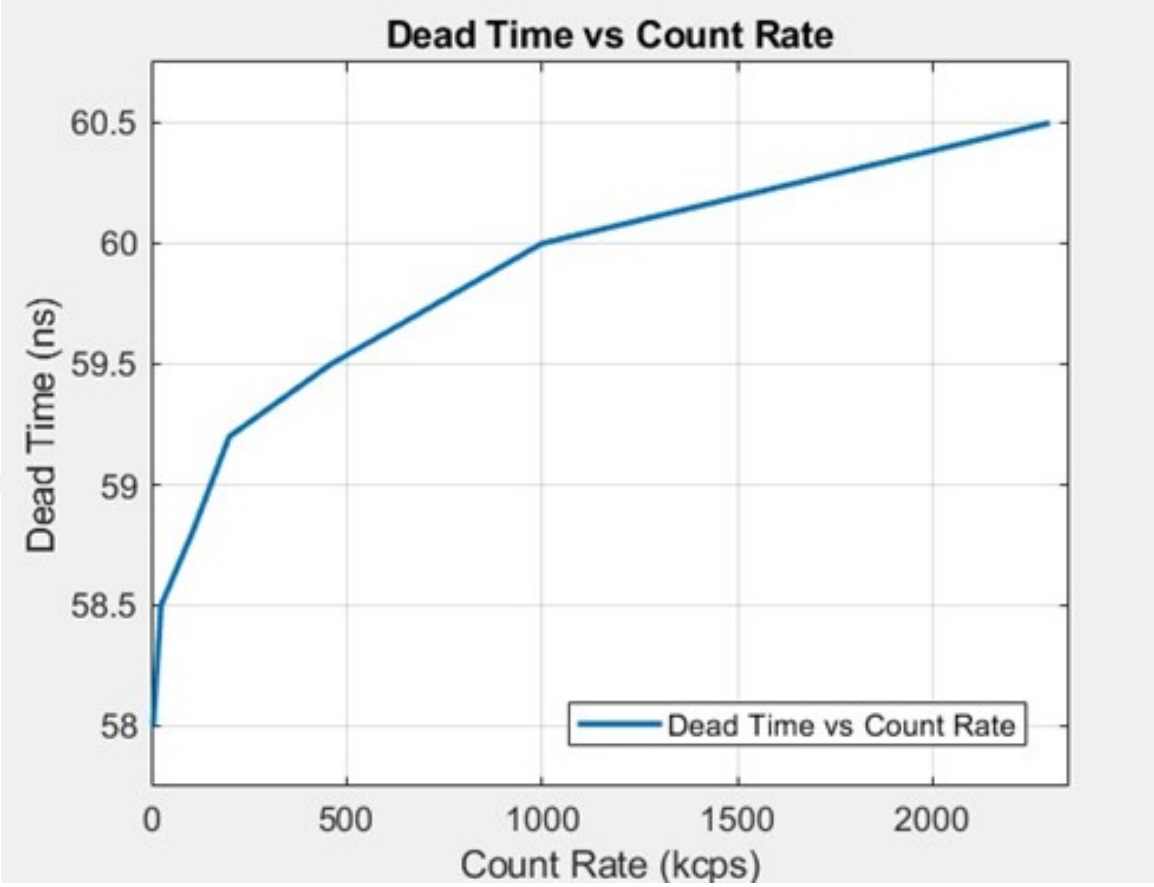

Figure 20: The relation between the count rate and the dead time of the detector

After establishing a correlation between the detectors' count rates and their respective timing jitter values, we gathered various count rate data for analysis. In Figure 20, the relation between them is illustrated. The timing jitter can be defined as the changes in the dead time of a detector. Therefore, if the minimum and maximum dead time measurements were subtracted, it would yield the timing jitter of the detector in between specified count rate interval. In this specific case, the count rate ranges between 5 kcts/s to 2.3 Mcts/s. The timing jitter value can be expressed as 2.5 ns for all silicon APD based designs.

2.8.6 Afterpulsing Test

Afterpulsing is a phenomenon observed in SPDs that manifests as delayed pulses occurring after the primary detection event. This delayed response is attributed to the trapping and subsequent release of charge carriers within the semiconductor. When a photon is initially detected, it may create electron-hole pairs that get captured by defects or traps within the detector. These trapped carriers can later be released, leading to additional spurious signals or afterpulses that can be misinterpreted as separate photon events. Afterpulsing introduces a temporal correlation between successive detection events and poses a significant challenge in achieving precise and accurate temporal resolution in photon detection applications. Mitigating afterpulsing typically involves advanced detector design and optimization strategies, as minimizing the trapping and detrapping processes is crucial for enhancing the overall performance and reliability of single photon detectors.

The distinct feature of the afterpulses comes from the time duration of the quenching. When the quenching signal could not entirely stop the avalanche current, intrinsically, leftover charge carriers produces an avalanche current when the APD is biased above its breakdown voltage. This phenomenon happens as soon as the APD becomes active, meaning when the resetting ends. Therefore, if there would be afterpulsing effects on a detector, they would occur after the dead time. It should be noted that, longer dead time corresponds less probability of afterpulsing. For identification of the afterpulsing character of a detector, an autocorrelation function was used. Figure 21 shows the experimental setup for identifying the afterpulsing characteristics of an SPD.

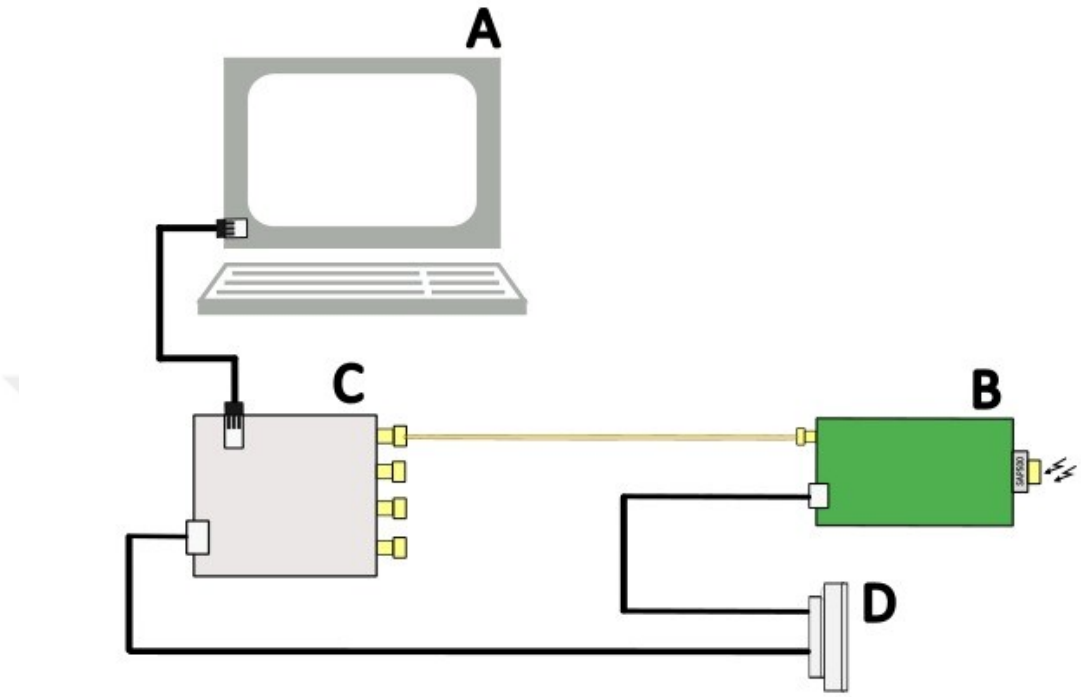

Figure 21: The schematic of the afterpulsing test setup. A: Computer, B: Single photon detector, C: Time stamping unit, D: Power supply

We aimed to explore the relationship between count rate, illumination, and afterpulsing probability using the InGaAs APD with the cathode sensing design. Initially, we anticipated a close-to-linear correlation between count rate and illumination. However, due to a dark count rate of approximately 200 kcts/s at room temperature with the InGaAs APD, we expected some non-linearity within these parameters. To enhance the clarity of the afterpulsing probability relative to the count rate, we utilized normalized illumination. As depicted in Figure 22, the afterpulsing probability indeed rises with an increase in the count rate. Given the data's acquisition through a time stamping unit with an 81 picosecond resolution, the error bars represent the

resolution's impact on the associated parameter.

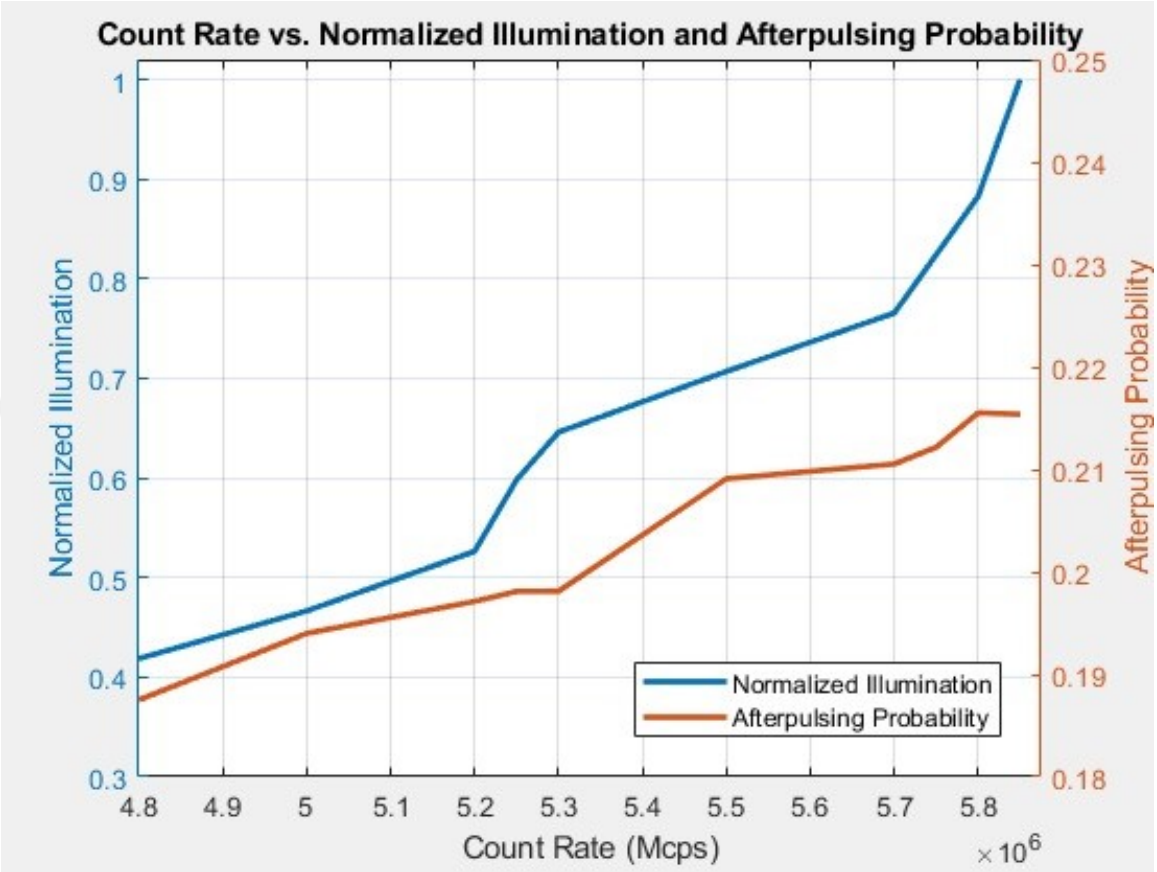

Figure 22: The afterpulsing probability (orange) and normalized illumination (blue) versus the total count rate of the InGaAs SPD

2.8.7 Electronic Jitter Test

Main purpose with this test was to understand if there was additional uncertainty between the count rate of a detector and the APD utilized. As stated in the SAP500 datasheet [23], the timing jitter of the APD would be in the order of its rise time. The output signal from the detector was divided into two cables which are connected to a time stamping unit, with a resolution of 81 picoseconds, to its first and fourth channel. The total cable length from the first and the fourth channel to the detector were approximately 30 cm and 130 cm respectively. In order to understand the timing

jitter coming from the APD to the data, a cross correlation function was applied to the first and fourth channels in the TSU. In a perfect scenario, a graph similar to the Dirac delta function was expected. However, if there was additional timing jitter, the FWHM value of the cross correlation histogram would increase as the count rate of the detector would increase. The experimental setup is shown in Figure 23.

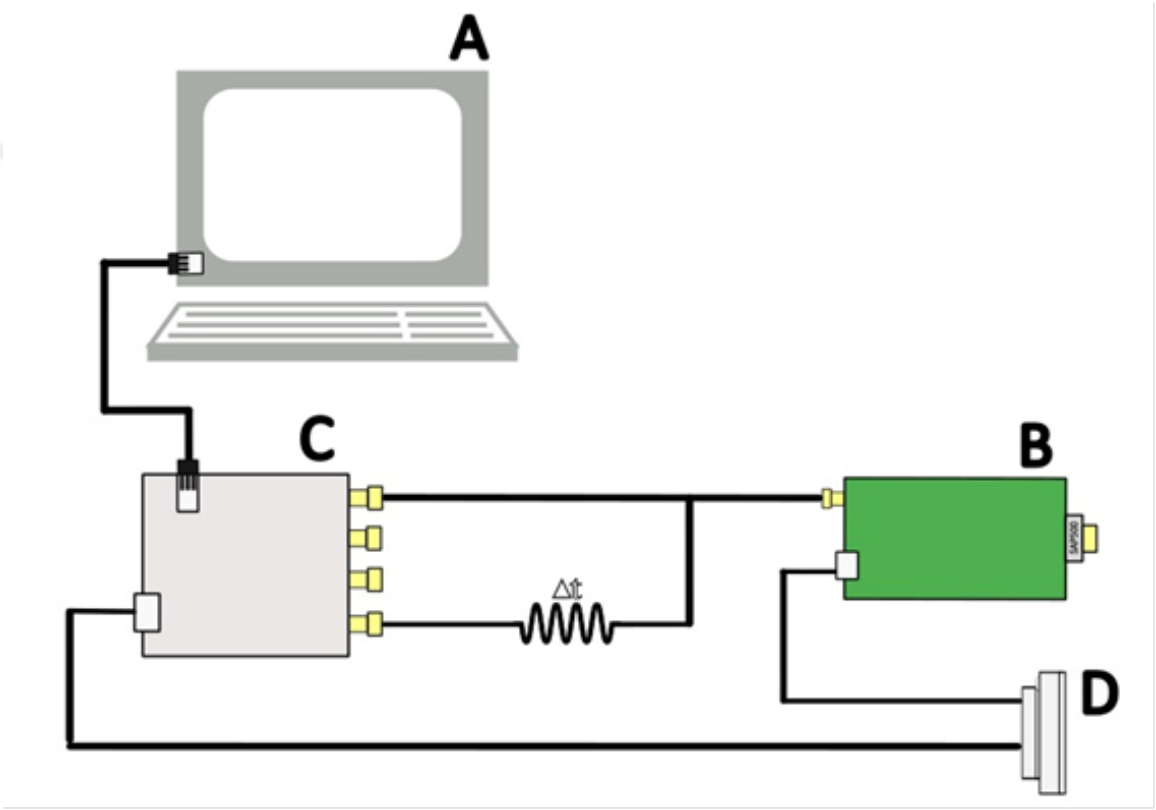

Figure 23: The experimental setup for electronic jitter test. A: Computer, B: SPD, C: Time stamping unit, D: Power supply, Δt: The additional delay given to the output of the SPD, which is 1-meter c, which is 1-meter responds to 4.5 ns of delay.

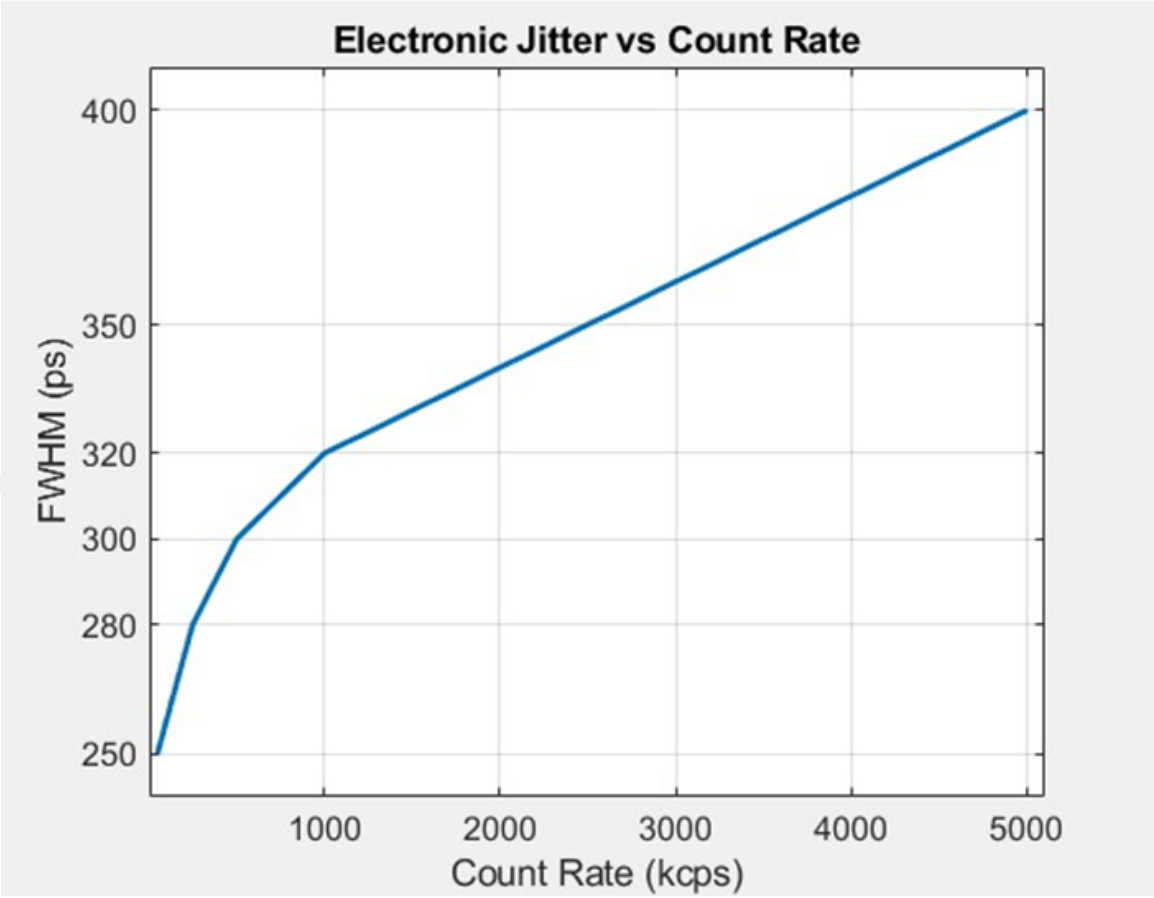

Figure 24: The relation between the APD's jitter with the total count rate

The count rate of the detector has been swept between, 50 kcts/s and 5 Mcts/s via controlling the illumination. As the count rate increases, the FWHM value from the histogram increases, as expected. The resulting graph is shown in Figure 24. The minimum and maximum FWHM difference would yield the APD's intrinsic timing jitter value which is approximately 150 picoseconds, between the applied count rates. The error bars on the graph, in Figure 24, show the uncertainty of the data, coming from the utilized time stamping unit's resolution of 81 picoseconds.

CHAPTER III

CONCLUSION

In the pursuit of advancing single-photon detection technology, here we delved into the design, test, and characterization of active-quenching circuitry within the visible and near-infrared spectrum. The multifaceted discussions and explorations showcased the intricate nature of these detectors and the nuances encountered in their performance evaluation. Through a comprehensive series of experiments and analyses, a deeper understanding emerged, shedding light on critical aspects impacting their functionality.

The initial focus centered on the complex dynamics of active quenching circuitry in single-photon detectors. Three different schematic and hardware designs have been detailed. Additionally, two different HVA designs have been discussed. Four different single photon detectors have been realized and characterized experimentally. The experimental results revealed the intrinsic differences between Silicon and InGaAs APDs, notably their excess bias sensitivities and breakdown voltages. All the realized SPDs have become products of Qubitrium.

A profound examination revealed that the afterpulses could be examined by an autocorrelation function. Moreover, the intrinsic correlation between quenching time duration and the generation of leftover charge carriers elucidated the necessity of post-dead time observation to discern these phenomena accurately. The discussions underscored the pivotal role of dead time in mitigating afterpulsing, highlighting its substantial correlation with the detection efficiency.

The exploration extended to the evaluation of the timing jitter values, which

exhibited a proportional relationship with the count rate of detectors. This relationship, explained through experimentation, facilitated the identification of timing jitter trends concerning the count rate intervals. It was evident that various count rate data gathered in these investigations enabled the depiction of the correlation between count rate and timing jitter, signifying its pivotal impact on detector performance.

Furthermore, the intricacies of temperature modulation in both Silicon and InGaAs APDs were examined, aiming to understand the interplay between count rate, illumination, dead time, timing jitter, and afterpulsing probability. The experimental results concerning the relationship between count rate and illumination due to the saturation rate of the detectors at room temperature presented challenges. Enhancing the signal-to-noise ratio via cooling down the InGaAs APD, showed that the APD can be utilized with higher excess bias voltage values for better detection efficiency. The optimization of dead time, dark count and saturation rates have been explained. Throughout these deliberations, the significance of experimentation, precise measurements, and critical data analysis emerged as key elements in comprehending the intricacies of single-photon detectors. The iterative process of exploring and analyzing various parameters, including afterpulsing, timing jitter, and count rate, contributed substantially to unraveling the complexities inherent in these detectors.

In conclusion, this work explains the nuanced nature of active-quenching circuitry for free-running single-photon detectors in the visible and near-infrared regimes. The combination of theoretical insights and empirical investigations underlines the continuous effort towards refining these detectors' functionalities, thus paving the way for further advancements in the field of quantum photonics and high-precision photon detection.

APPENDIX A

ELECTRONIC SETUP DRAWING

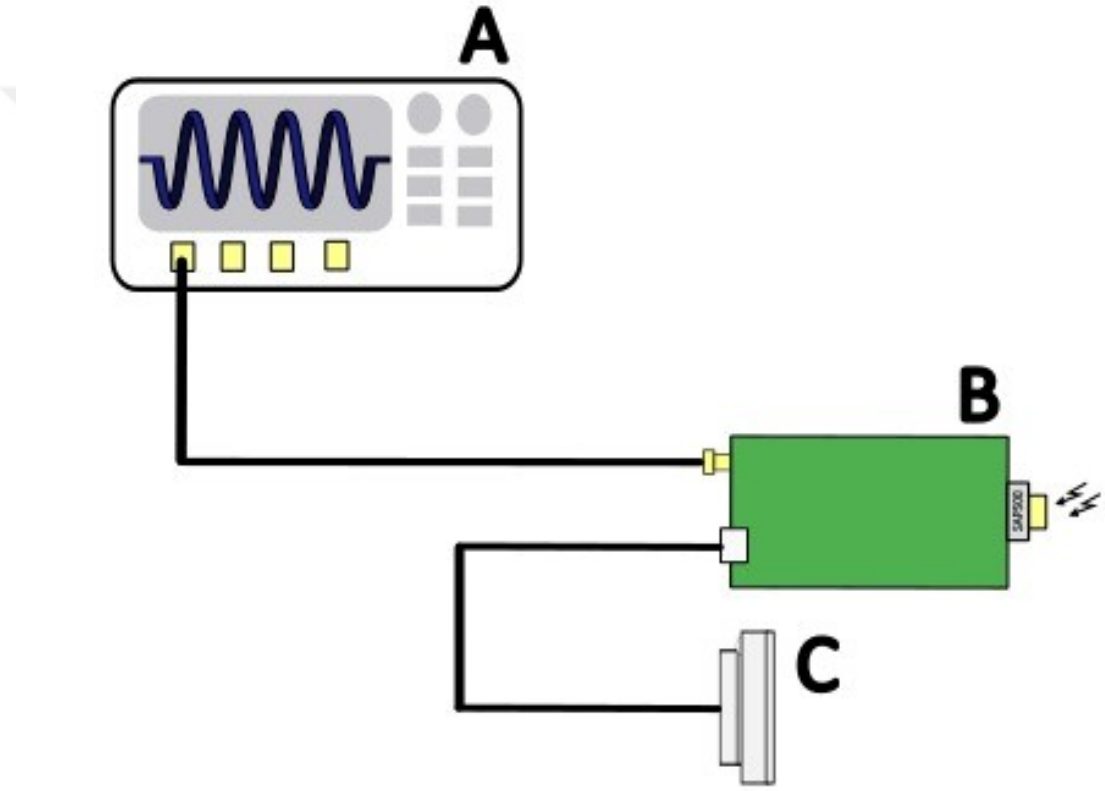

Figure 25: The electronics experimentation setup illustration. A: Oscilloscope, B: Single photon detector, C: Power supply

APPENDIX B

EXPERIMENTAL PHOTOS

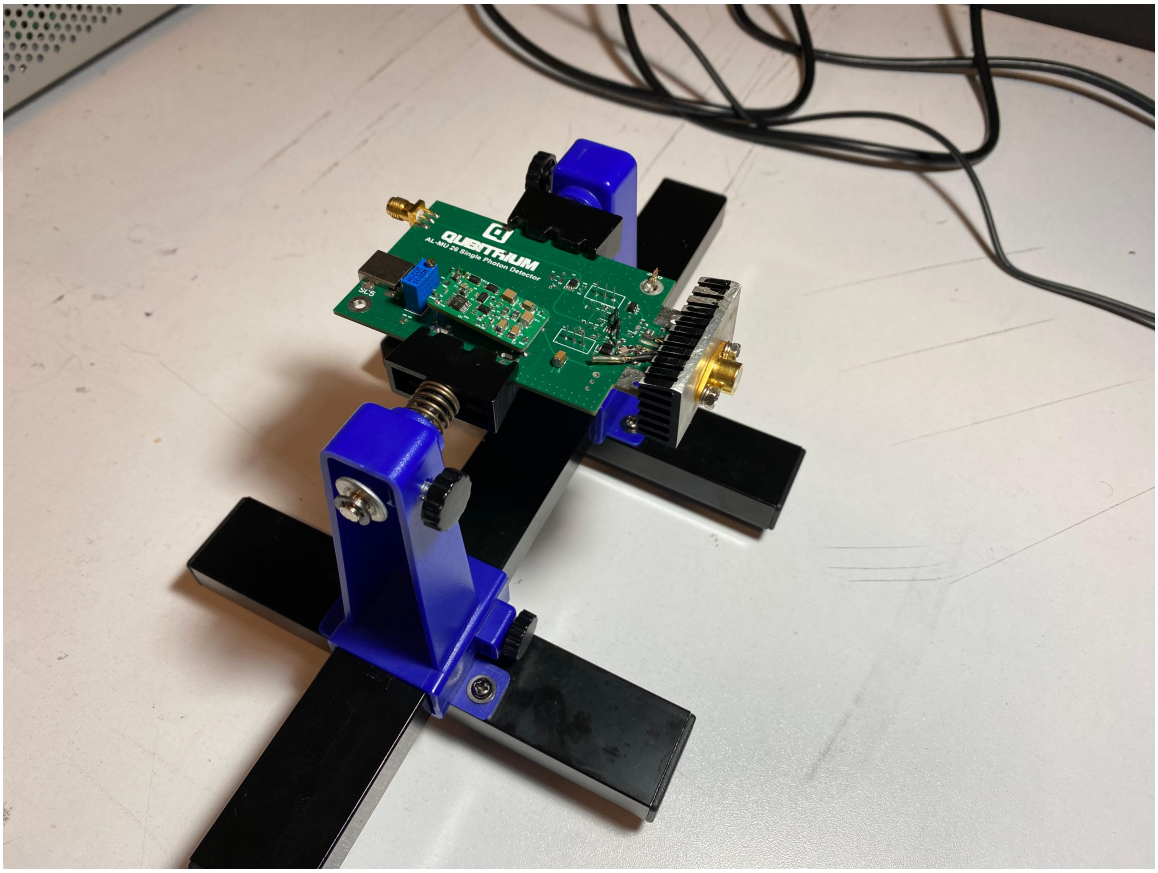

Figure 26: The fully populated version of the first SPD design

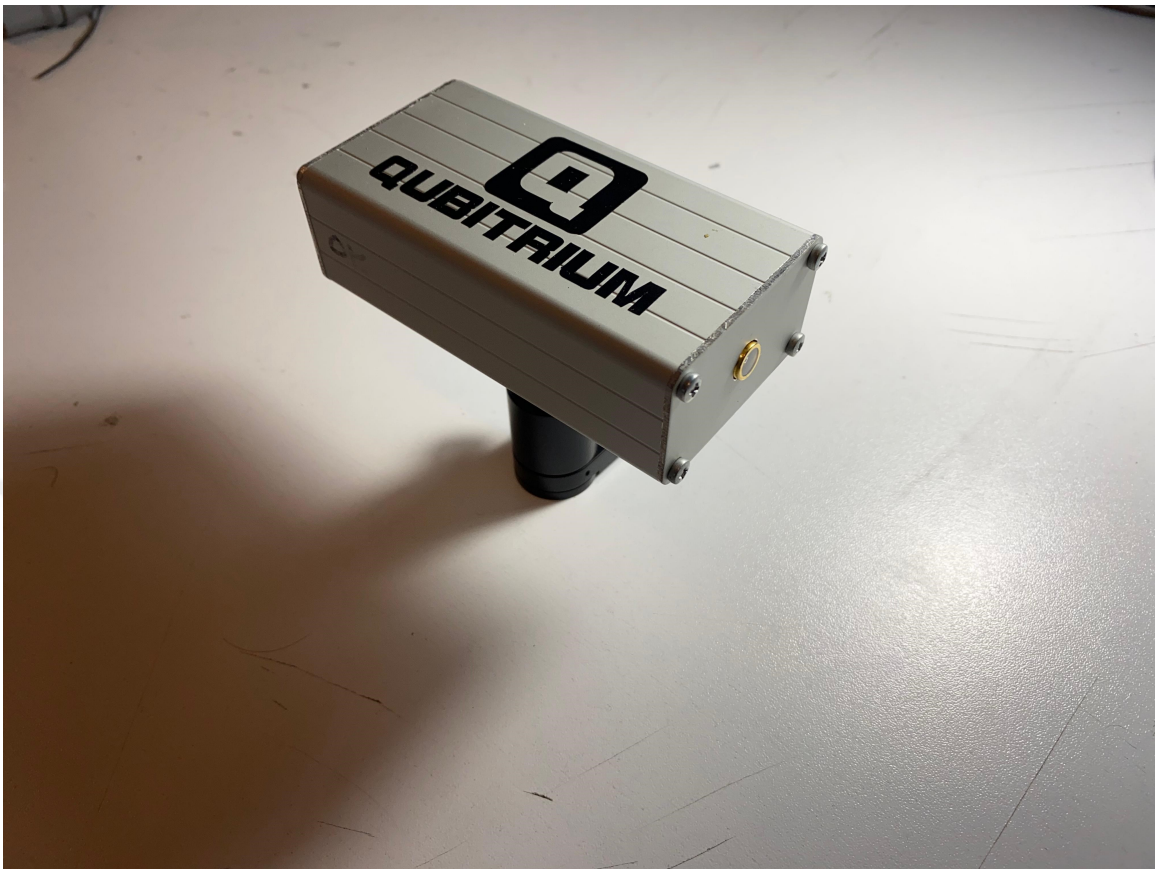

Figure 27: Cathode sensing design as products (Geon-20, Qubitrium) [2]

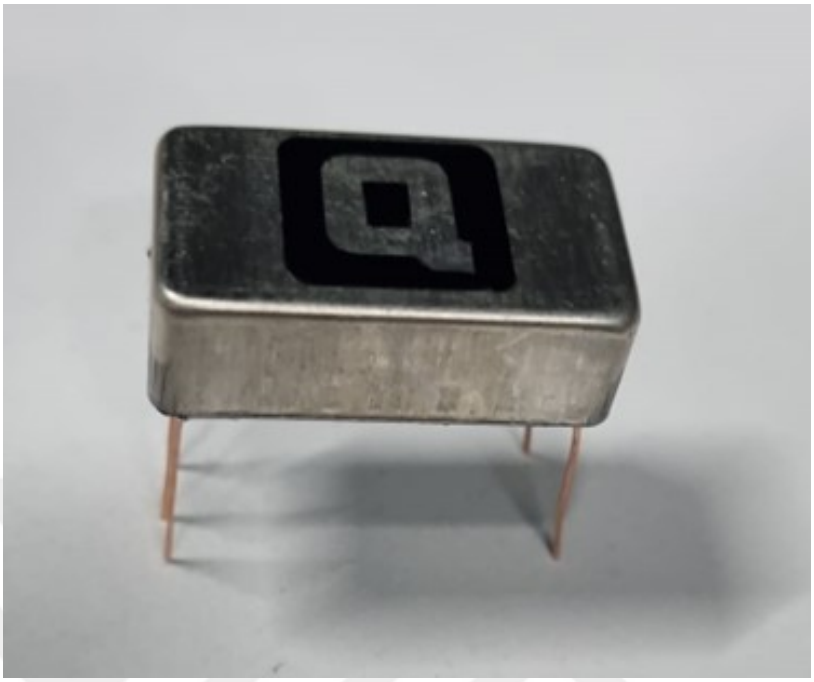

Figure 28: The Qubitrium HVA module as a product

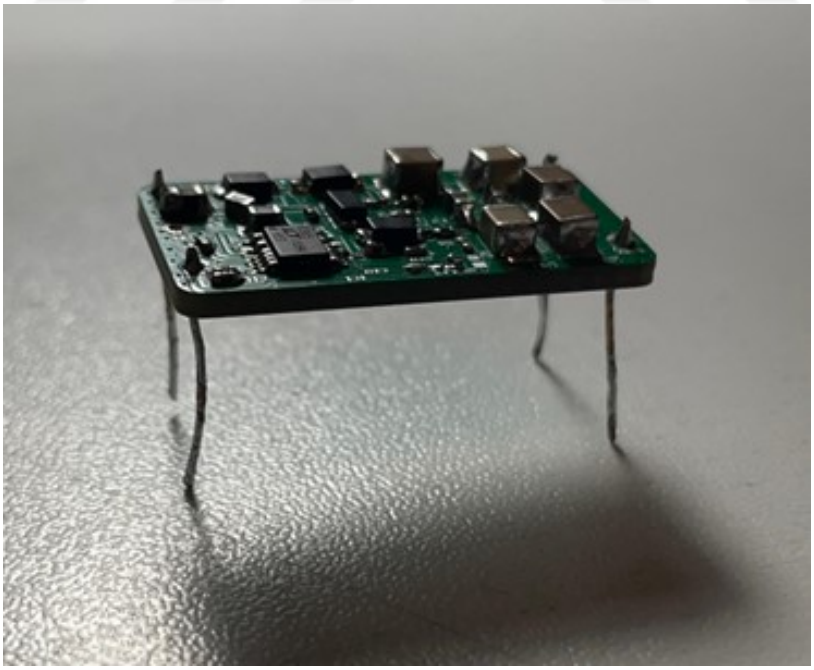

Figure 29: The Qubitrium HVA module (inside)

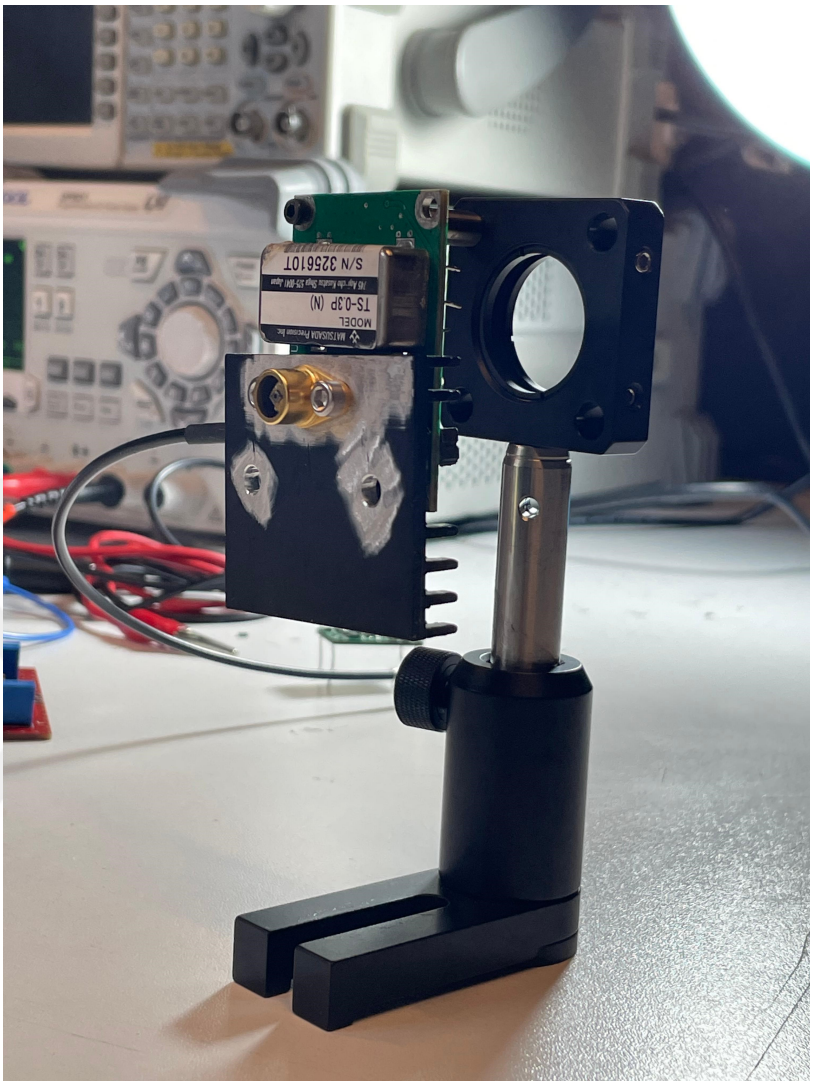

Figure 30: The CubeSat compatible SPD, fully populated, test mount

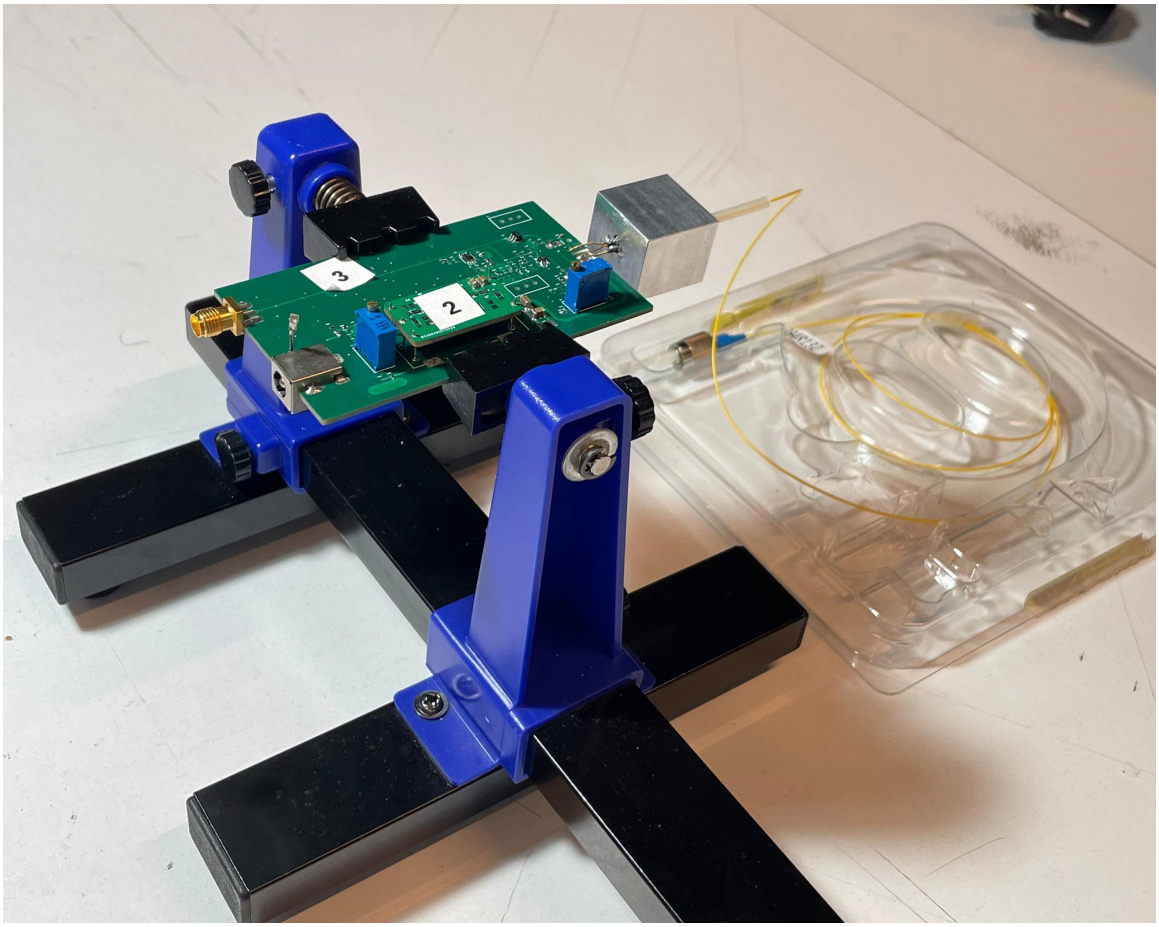

Figure 31: The fully functional InGaAs SPD

APPENDIX C

EXPERIMENTAL RESULTS

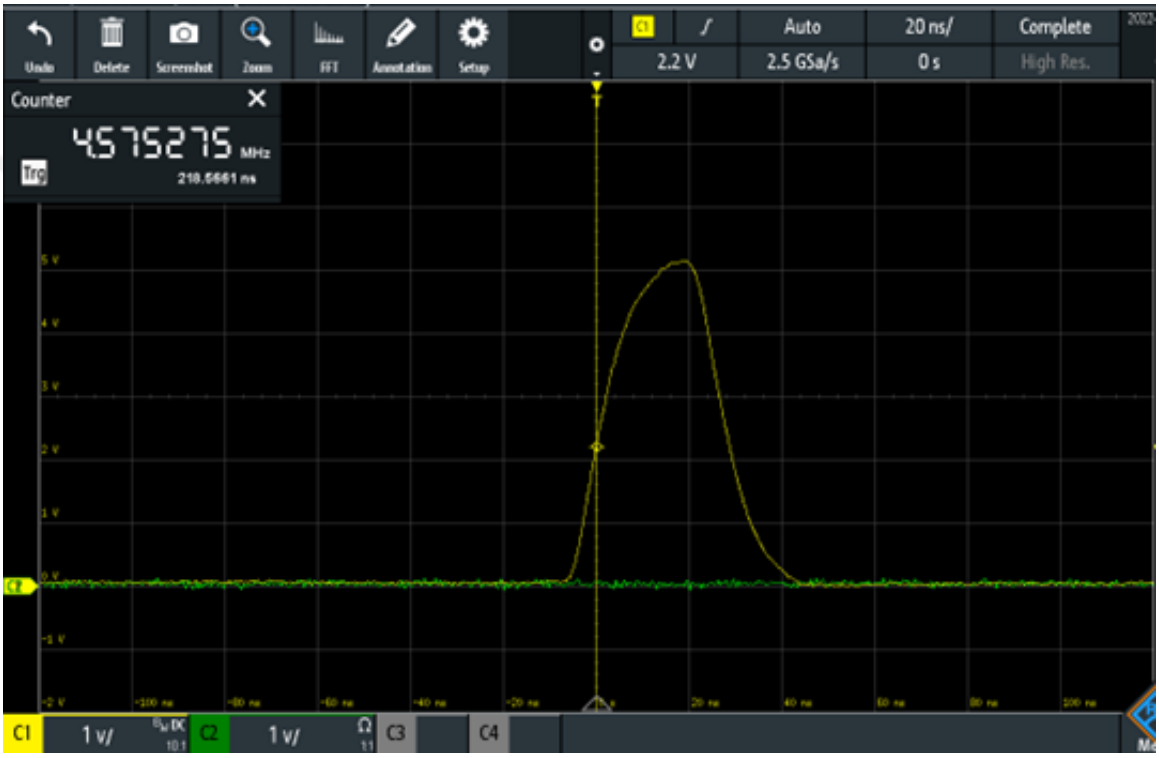

Figure 32: The output signal from the cathode sensing SPD with 20 MHz oscilloscope filter, with 1 Mohm termination

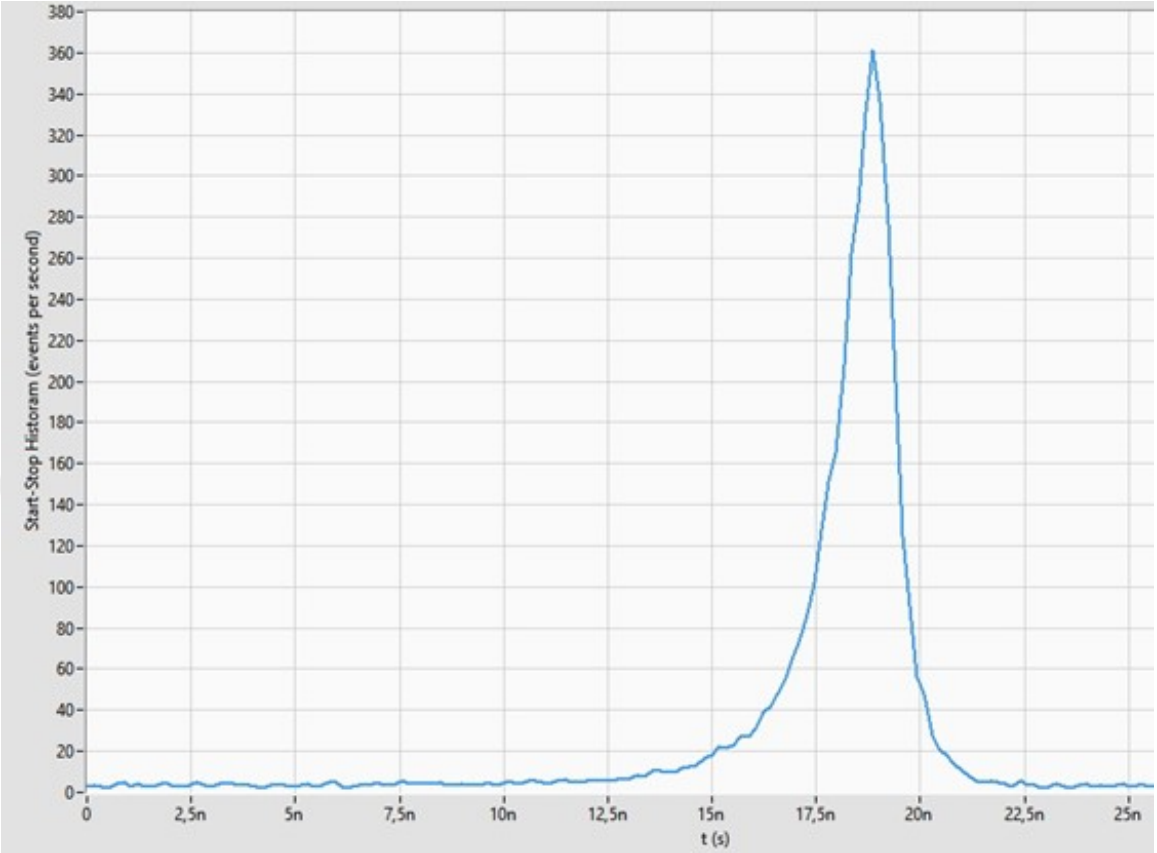

Figure 33: The cross correlation histrogram between SPCM-AQRH and first design detectors with both count rates about 300 kcts/s. FWHM = 1.5 ns (combined timing jitter values of both detectors)

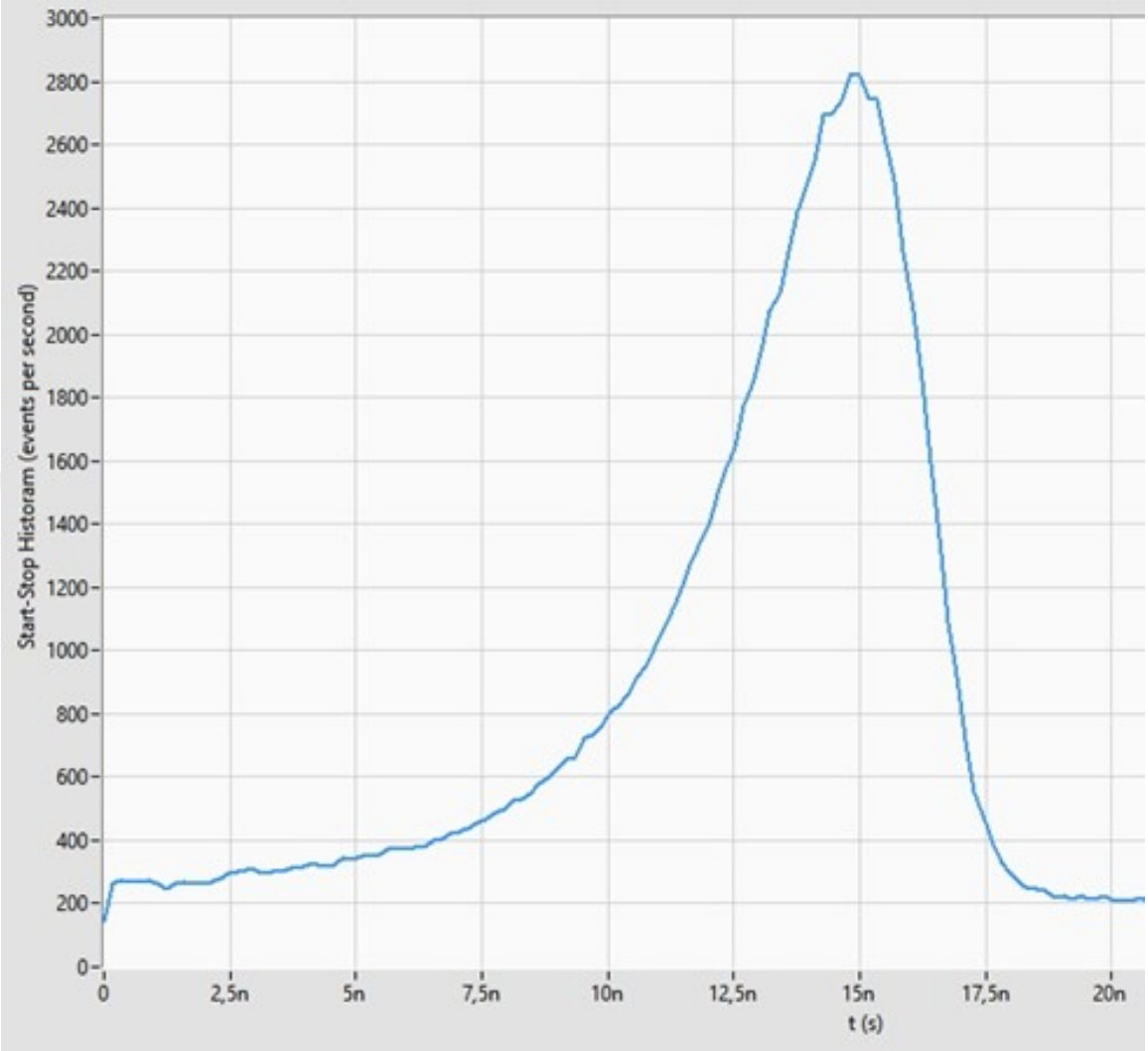

Figure 34: The cross correlation histrogram between SPCM-AQRH and first design detectors with both count rates about 5 Mcts/s. FWHM = 3.9 ns (combined timing jitter values of both detectors)

APPENDIX D

DATASHEETS

Description	Condition	Min.	Typ.	Max.	Units
Supply Voltage		5.6	6	6.5	V
Supply Current			500	2400	mA
Active Area			500		um
Photon Detection Efficiency	840nm		43		%
Dark Count Rate (at 22°C ambient)	For all wavelength range		1k	2k	counts/sec
Output Pulse Width (TTL)	Configurable by manufacture	30	32	33	ns
Dead time	Configurable by manufacture	40	50	65	ns
Timing Jitter	300kcounts/sec at 780nm		1	1.4	ns
Count Rate before Saturation		3.5	4	10	Mcounts/sec
Excess Bias Voltage	Vbias - Vbreakdown	10	11	12	V
Output Connector Impedence	SMA		50		Ω
Spectral Range		300		1000	nm

Figure 35: The performance parameters of the first and CubeSat compatible designs

Parameter	Condition	Min	Typical	Max	Units
Supply Voltage	Power Jack connector	5.75	6	6.25	V
Supply Current		15	50	150	mA
Active Area (diameter)			16		µm
Wavelength Range		950		1650	nm
Dark Count Rate (DCR)	Changes with excess bias voltage		200k		Counts/s
Output Pulse Width			40		ns
Output Pulse Amplitude	TTL	4	4.2		V
Timing Resolution (jitter)	at 200k counts/s		0.2		ns
Count Rate before Saturation	at 200k counts/s DCR		5	8	Mcounts/s
Photon Detection Efficiency	at 1550 nm & 200k counts/s DCR	10			%
Dead Time			105		ns
Excess Bias Voltage *	Adjustable				V
Input Type	Single Mode Fibre (SMF)				
Operating Temperature	Ambient	18	22	26	°C
Dimensions			100 x 50 x 30		mm
Weight				350	g
Output Connector (impedance)	SMA		50		Ohm Ω

Figure 36: The performance parameters of InGaAs SPD

Description	Condition	Min.	Typcial	Max.	Unit
Supply Voltage		5.4	6	6.5	V
Supply Current	It may vary according to the stabilized temperature of the APD.		300	1100	mA
Active Area (Diameter)	For SAP500 T6		500		um
Photon Detection Efficiency	Tested at 840 nm illumination.		45		%
Dark Counts				1k	count/s
Output Pulse Width (TTL)	Adjustable		32		ns
Output Pulse Amplitude	Adjustable	4	4.2	5	V
Dead Time	Adjustable	35	60		ns
Timing Jitter	at 300 kcount/s		1		ns
Saturation Value	Adjustable		15		Mcount/s
Output Connector	Adjustable		50		Ω (SMA)
Wavelength Range		300		1000	nm
Size			100x50x30		mm

Figure 37: The performance parameters of cathode sensing design

REFERENCES

[1] A. Özülker, M. İzçınar, and K. Durak, "Tek foton dedektörü," 2023. Türkiye: Patent 2021 021657.

[2] Qubitrium, "Geon-20." Datasheet, Dec. 2023. Available at `http://qubitrium.com.tr/products/geon-20.html`.

[3] H. Iams and B. Salzberg, "The secondary emission phototube," *Proceedings of the Institute of Radio Engineers*, vol. 23, no. 1, pp. 55–64, 1935.

[4] S. Cova, A. Longoni, and G. Ripamonti, "Active-quenching and gating circuits for single-photon avalanche diodes (spads)," *IEEE Transactions on Nuclear Science*, vol. 29, no. 1, pp. 599–601, 1982.

[5] H. Dautet, P. Deschamps, B. Dion, A. D. MacGregor, D. MacSween, R. J. McIntyre, C. Trottier, and P. P. Webb, "Photon counting techniques with silicon avalanche photodiodes," *Appl. Opt.*, vol. 32, pp. 3894–3900, Jul 1993.

[6] E. Optoelectronics, "Egg spcm-200-pq." Datasheet, 1991.

[7] J. Liu, Y. Li, L. Ding, Y. Wang, T. Zhang, Q. Wang, and J. Fang, "Fast active-quenching circuit for free-running ingaas(p)/inp single-photon avalanche diodes," *IEEE Journal of Quantum Electronics*, vol. 52, pp. 1–6, 2016.

[8] A. Lacaita, S. Cova, C. Samori, and M. Ghioni, "Performance optimization of active quenching circuits for picosecond timing with single photon avalanche diodes," *Review of Scientific Instruments*, vol. 66, pp. 4289–4295, 08 1995.

[9] A. Gallivanoni, I. Rech, D. Resnati, M. Ghioni, and S. Cova, "Monolithic active quenching and picosecond timing circuit suitable for large-area single-photon avalanche diodes," *Opt. Express*, vol. 14, pp. 5021–5030, Jun 2006.

[10] M. Stipčević, "Active quenching circuit for single-photon detection with geiger mode avalanche photodiodes," *Applied Optics*, vol. 48, p. 1705, Mar. 2009.

[11] R. T. Thew, D. Stucki, J.-D. Gautier, H. Zbinden, and A. Rochas, "Free-running InGaAsInP avalanche photodiode with active quenching for single photon counting at telecom wavelengths," *Applied Physics Letters*, vol. 91, p. 201114, 11 2007.

[12] S. Sauge, L. Lydersen, A. Anisimov, J. Skaar, and V. Makarov, "Controlling an actively-quenched single photon detector with bright light," *Optics Express*, vol. 19, p. 23590, Nov. 2011.

[13] C. Kurtsiefer, P. Zarda, S. Mayer, and H. Weinfurter, "The breakdown flash of silicon avalanche photodiodes-back door for eavesdropper attacks?," *Journal of Modern Optics*, vol. 48, p. 2039–2047, Nov. 2001.

[14] Y. Shi, J. Lim, H. S. Poh, P. K. Tan, P. Tan, A. Ling, and C. Kurtsiefer, "Breakdown flash at telecom wavelengths in ingaas avalanche photodiodes," *Optics Express*, vol. 25, pp. 30388–30394, 08 2017.

[15] Y. Yu, C. Wang, H. Shi, B. Yang, and X. Liu, "A review of quenching circuit design based on geiger-mode apd," in *2018 IEEE International Conference on Mechatronics and Automation (ICMA)*, pp. 28–33, IEEE, 08 2018.

[16] S. Cova, M. Ghioni, A. Lacaita, C. Samori, and F. Zappa, "Avalanche photodiodes and quenching circuits for single-photon detection," *Appl. Opt.*, vol. 35, pp. 1956–1976, Apr 1996.

[17] F. Zappa, A. Lotito, A. Giudice, S. Cova, and M. Ghioni, "Monolithic active-quenching and active-reset circuit for single-photon avalanche detectors," *Solid-State Circuits, IEEE Journal of*, vol. 38, pp. 1298 – 1301, 08 2003.

[18] R. Mita, G. Palumbot, and G. Fallica, "A fast active quenching and recharging circuit for single-photon avalanche diodes," in *Proceedings of the 2005 European Conference on Circuit Theory and Design, 2005.*, vol. 3, pp. III/385–III/388 vol. 3, 2005.

[19] D. Bronzi, S. Tisa, F. Villa, S. Bellisai, A. Tosi, and F. Zappa, "Fast sensing and quenching of cmos spads for minimal afterpulsing effects," *IEEE Photonics Technology Letters*, vol. 25, no. 8, pp. 776–779, 2013.

[20] M. Hofbauer, B. Steindl, and H. Zimmermann, "Temperature dependence of dark count rate and after pulsing of a single-photon avalanche diode with an integrated active quenching circuit in 0.35 m cmos," *Journal of Sensors*, vol. 2018, pp. 1–7, 07 2018.

[21] F. Zappa, A. Tosi, A. Dalla Mora, and S. Tisa, "Spice modeling of single photon avalanche diodes," *Sensors and Actuators A: Physical*, vol. 153, pp. 197–204, 08 2009.

[22] D. Huang, R.-x. Zhu, S.-y. Liu, W.-f. Sun, J. Wu, and D.-j. Ma, "Spice modeling for single photon avalanche diode," *Proc SPIE*, vol. 8908, 08 2013.

[23] L. Components, "Sap500 datasheet." Datasheet, 2023. Available at `https://www.lasercomponents.com/us/news/sap500-silicon-apds-for-photon-counting-applications-1/`.

[24] B. R. E. Ltd, "Pigtailed coaxial single photon avalanche diode (spad) pga-314-100." Datasheet, 2020. Available at `http://www.rmyelectronics.com/uploads/EN/TO46/PGA-314-100V3.1.pdf`.

[25] E. Technologies, "Spcm-aqrh single photon counting module." Datasheet, 2020. Available at `https://www.excelitas.com/product-category/low-light-level-detection-modules`.

VITA

Alper Özülker got his bachelor's degree from the Electrical & Electronics Engineering Department at Ozyegin University in 2020. His journey into the realm of quantum optics commenced in 2019 when he joined Dr. Durak's Quantum Optics Laboratory. He began his Master's degree program under the mentorship of Kadir Durak, starting in 2020. Simultaneously, he became a part of Qubitrium, an innovative quantum technology start-up, in 2021. His primary area of focus lies within the domain of single-photon detectors, with his thesis centered around their comprehensive characterization and the subsequent avenues for their commercialization.