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Software Defined Radio with Multiple Antennas for GPS Receiver

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ABSTRACT

In civil and commercial market, global positioning is ubiquitous. A wide range of mobile phones have Global Navigation Satellites Systems (GNSSs) chips and demands are growing for precise location information due to increasing number of applications. Global Position systems is used for road transport, scientific, aviation, railway, and maritime applications with availability of low-cost receiver. Since the number of uses of GPS increases, the threat of spoofing, sending false replica of GPS signal to receiver will also increase. The multiple antennas are used by the military to overcome spoofing and jamming by using beamforming very early. However, these systems are expensive and there is an increased demand for developing low cost solutions. The main motivation of this project is to design and implement radio frequency (RF) front-end that is suitable for the detection of GNSS signal upper L frequency band.

The requirements for a GPS front-end are antenna, LNA, which is low noise with high gain, narrowband filter, down-conversion mixer, intermediate frequency amplifier and high-speed comparators. To achieve these goals, with the aim of yielding low noise figure, the radio frequency stage has been optimised by suitable matching and biasing. RF stage signal has been down-converted by double balanced. Since targeted system needs double local oscillator, this system oscillator is provided by PLL, that two differential output. The IF stages are implemented using a differential structure, to enhance high noise immunity with low cost. Since targeted receiver structure needs digital input to process, high speed comparators have been used in the inter-stages connection at the output convert from analogue to digital.

All of the yielding conclusion that front-end implemented four layers PCB structure. RF stage provides 18 dB gain, and mixer down-converted signal 26.00 MHz with low insertion loss (3.2 dB). Besides, reasonable performance provides with low-cost high-speed comparators and video amplifiers instead of expensive AGC.

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1. INTRODUCTION

1.1. Introduction

Since the design and development of the most well-known and widespread localization terminal is Global Navigation Satellite System (GNSS), which is known as Global Positioning System (GPS), GNSSs have proven ubiquitous for a multitude of civil applications. Thus, new independent GNSSs, such as GALILEO in Europe, GLONASS in Russia, and BEIDOU in China were or have being designed and improved over planet [1, 2]. Thus, the availability of precise, upgradeable and reconfigurable receivers is becoming the most important part of host satellite navigation applications for including civil, commercial, research and military [1]. An effective software-defined radio approach meets both reprogrammable to adapt to different conditions and easily adjustable for future desires[1]. The availability and precision of GPS provides civil and commercial market opportunity with moving forward navigation to growing range of new applications. These include road transport, marine applications, aviation, agriculture, law enforcement, fisheries, energy production and management, services for vulnerable people, energy production and management, health services, highways management, surveying, information services, financial services, safety monitoring, search and rescue, scientific studies, tracking vehicles and valuable, telecommunications [2, 3]. Owing to large distances between satellite and receivers, on condition that transmitting signal that can appear to be genuine GNSS signal to receiver, GNSS is going to be disrupted.

When it comes to usage of GNSS, the treat of jamming and spoofing inclines and this can be result in catastrophic effect on economy. As in reported [4], GNSS is widely used, with 5.8 billion GNSS devices in use in 2017. By 2020, this number is estimated to rise sharply to almost 40 percent (8 billion), which an assumption of approximately one and half device per person all over the world. According to this study [4], the annual revenues of added-value services will reach a peak € 195 billion in 2025, nearly three higher than the expected GNSS device and

service revenues with the advent of 5G, Automated Driving, Smart Cities and the Internet of Things [4]. Another research shows that the direct economic costs of GNSS disruption for 5 days has been forecasted to be £5.2 bn through commercial GPS users and GPS manufacturers are in the United Kingdom [5].

Even though the reports of jamming and spoofing have hardly ever been witnessed, increasing usage of GNSS could cause widespread and frequent problems because of vulnerabilities [6]. The academic and researcher proved that disruption of navigation devices and receiver timers were achievable under arranged condition. For example, academics at the University of Texas at Austin proved that spoofing attack on a yacht and drone were with simple research device, which is design by commercially available components [7]. Academics spoofed the GPS signal until they eventually acquire control of superyacht and it was transferred from desired track to a parallel track several hundred meter far away from expected one, although autopilot shows the original moving direction [8].

Having said that, interfering with communications or surveillance (jamming) and broadcast of signals which can be replica of GNSS signals (spoofing) is never thought as treat by each user except the military [2, 9]. Military aware of these treat very early and introduced multielement adaptive antenna arrays with the intention of antijamming by using beamforming [3]. These made by using the antennas, where accommodated closely mounted array and distance from each other is half of wavelength [3, 10, 11]. Therefore, they are able to neglect the interference signal with processing with digital matrix technique to supress signal interference from desired one [3, 12, 13]. However, these types of receivers are very expensive and civil and commercial market needs to design and develop new cheaper solutions. The objective of the project is to design, develop and implement a radio frequency (RF) front-end receiver that is usable to detect civil and commercial frequency band, which is known upper L frequency band [14] and can be utilized as a main construction block in a beam forming applications. Thus, the angle of

receiving signal can be calculated from multiple antenna array. This gives receivers opportunity with additional information not only being used for tracking aid but also overcome spoofing attack.

1.2. GNSS Overview

GNSS is the general architecture is to include a wide ranges of different networks of technologies and devices that are able to provide three crucial services: position, navigation, and timing (PVT) [1, 2]. The overall architecture of the navigation systems consists of three essential elements, known as segments. The first one, which is known as the control segment, is used for tracking satellite and computing navigation data, synchronizing time across the constellation and sending data to the satellites [1, 2]. The second component is the space segment consisting of a constellation satellites that transmit positioning signals which contains integrity, the satellite position, and clock synchronism. These data are critical for typical receiver operation such as making a prediction of satellite visibility and estimating of atmospheric delays [1]. Finally, is the user segment is the last component of the system and consists of the receivers that are enabled to performs acquisition, tracking, and processing the signal to provide position, navigation and timing information [1, 2].

1.3. GNSS Signal

The fundamental characteristic of GNSS signals for systems that are currently under operation and are summarized in Table 1.3-1, which represents main difference as regards GPS, GLONASS, and GALLILEO [1, 2, 14-17]. Each of GPS satellites broadcasting at the same frequency bands with using code division multiple access (CDMA) techniques [1, 14, 18]. The higher-data rate pseudorandom noise (PRN) binary ranging code is used for coding data at the chip rate [3, 18]. Each satellite has unique PRN code so that all satellite can detectable by matching the received signal with a satisfactorily shifted received clone of satellite received signals [14, 18].

Table 1.3-1 Summary of main parameters GPS, GLONASS, GALILEO

Signal Parameter		***GPS***	***GLONASS***	***GALILEO***
Multiple Access Technique		*CDMA*	*FDMA*	*CDMA*
Data Modulation		*BPSK*	*BPSK*	*CBOC*
Carrier Frequency (MHz)		*1575.42 L1*	*1598.06-1609.31 L1*	*1575.42 E1*
Code Length (Chip)	*C/A*	*1023*	*511*	*4092*
	P	*2.35.1014*	*5.11.106*	*-*
Code Rate (Mcps)	*C/A*	*1.023*	*0.511*	*1.023*
	P	*10.23*	*5.11*	*-*
Code Frequency (MHz)		*1.023*	*0.511*	*1.023*
Data Rate (bit/s)		*50*	*50*	*250*
Minimum Received Power (dBW)		*-158*	*-161*	*-157*

Three crucial code are transmitted from all satellites. These are P code, long code high precision, is principal navigation ranging data, the Y code is used instead of P code when anti-spoofing mode activated, C/A coarse and acquisition code, short code low precision, used for accusation of P code and has also only usage in commercial and civil applications [3, 18-20]. Also L1 an E1 known as carrier frequencies 1575.42 MHz, whereas BPSK and CBOC is stands for binary shift keying modulation and composite BOC is particular case of composite binary coded symbols (CBCS) Modulation [1, 14]. The P code and C/A code are two codes on the L1 carrier. For the C/A code chip rate is 1.023 $Mchip/s$ from Table 1.3-1 and the bandwidth of main lobe of spectrum is 2.046 MHz and repetition lasts for exactly 1 millisecond [14, 18]. Thus, with small a carrier Doppler shift, the receiver and sufficiently signal-to-noise ratio (SNR), the receiver can detect start of the C/A code with trying several times by eliminating

errors in an observation time 1 millisecond [3, 14, 18]. The L1 frequency carried the C/A and P signal for nth satellite, as follows:

$$s_n(t) = \sqrt{2P_n}c_n(t)d_n(t)\cos(2\pi f_{RF}t) \quad (1\text{-}1)$$

where the transmitted signal, $s(t)$, the transmit power, P, the carrier frequency, f_{RF}, and the navigation message, $d(t)$, and a pseudo-randomly changing chipping sequence, $c(t)$, , and time is denoted by t [3, 6, 14, 18]. The navigation message $d(t) = \pm 1$ has symbol rate of $25 - 100$ symbols/s [6]. The chipping sequence $c(t) = \pm 1$ higher rate of $0.5 - 10$ MHz [6]. Moreover, the P and the C/A code, and they have coherent carrier frequencies, which means that they have a fixed phase and frequency association between each other [3, 18].

1.4. General Receiver Architecture

The general receiver architecture for GNSS is described at this section [19-22]. Considering the GPS $L1$ signal as reference channel the single frequency approach is used for comprehensive definition of a GNSS receiver. The receiver is essential component of a wireless systems to recover the desired signal from a wide band spectrum of transmitting sources, interferences, and noise [23]. The weak electromagnetic field incident on the on the antenna of a receiver tuned to the RF Carrier frequency must be amplified sufficiently for demodulator circuits to recover information [24]. Other undesired electromagnetic field must be filtered or attenuated at the receiver front end to overcome interference [24]. The basic architecture of a GNSS receiver is demonstrated Figure 1.4-1 and six different essential system components. These are antenna, radio frequency (RF) stage, analogue-to-digital converter (ADC) stage, signal processing stage (DSP), navigation processing stage, local oscillator (LO) or frequency synthesizer [18].

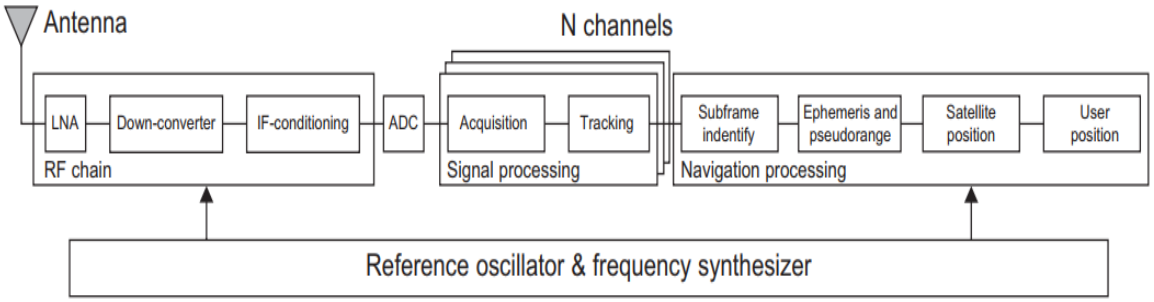


Figure 1.4-1 General GNSS receiver block diagram [18]

1.5. Introduction of a GNSS Software Defined Radio

It is essential to understand basic definitions before going to the comprehensive design of a GNSS software-defined radio receiver from throughout the literature [1, 25-28].Software Defined Radio (SDR) has a radio frequency (RF) and an intermediate frequency (IF) stage done prior to analogue-to-digital converter (ADC), after front-end stage the incoming signal converted to digital signal to be processed by digital signal processor, which means software performs at residing programmable platform [1]. Therefore, the analogue signal part at front end states without change, whereas all processing system works as fully reconfigurable [1]. An essential block diagram of general SDR architecture is illustrated in Figure 1.5-1. It demonstrates it is consist of front-end stage followed by ADC stage and eventually digital signal processing stage (DSP).

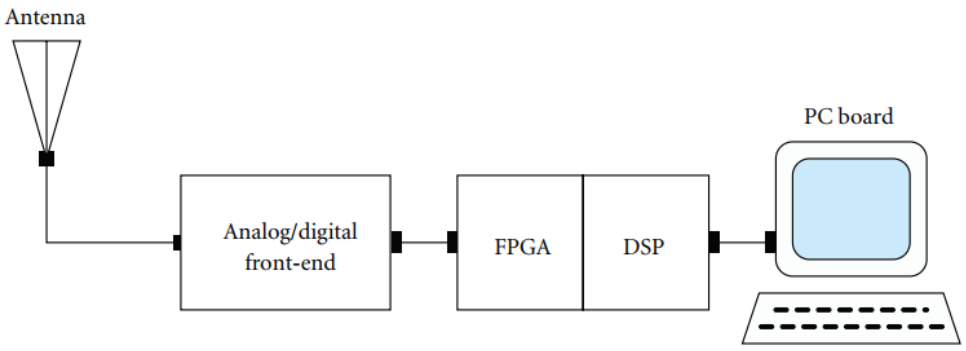


Figure 1.5-1 Hardware of software-defined radio receiver [1]

1.6. Architectural Design of a Software-Defined Radio

There are several ranges of possibilities for implementing SDR and they are constructed five main sections can determined from Figure 1.5-1. These are receiving antenna, the analogue or digital front-end, the field programmable gate array (FPGA) for the digital section and digital signal processing platform (DSP), and personal computer. There are three types of SDR architecture depending the processing task adjusted for each section. Firstly, software-controlled hardware architecture is type that front-end obtain from RF signal, and perform a down conversion to intermediate frequency (IF), and then digitise signal, where FPGA is programmed to simple high-rate computation, whereas the DSP runs all baseband operation algorithms and PC only provide user interface [1]. Second one is hybrid architecture, which means the FPGA perform most of the baseband operation and provide high-rate data for PC and DSP only perform initialization and configuration task, whereas PC runs navigation algorithms [1]. Finally, full software is a type that the FPGA only perform service functions and send to PC, whereas PC runs all baseband and navigation functionality and DSP runs configuration tasks only [1].

1.7. The Front-End

The general RF front-end includes filters, an RF low-noise amplifier (LNA), a mixer, a local oscillator (LO), quadrature intermediate frequency (IF), and direct modulation or I/Q sampling followed by digital modulation in digital signal processing (DSP) as illustrated Figure 1.7-1. A narrow band filter at the RF stage of the receiver to receive the desired signal while supressing adjacent channels, image, and interference. However, these filters are generally in efficient to detect at RF frequencies because their bandwidth and cut off requirements [23].

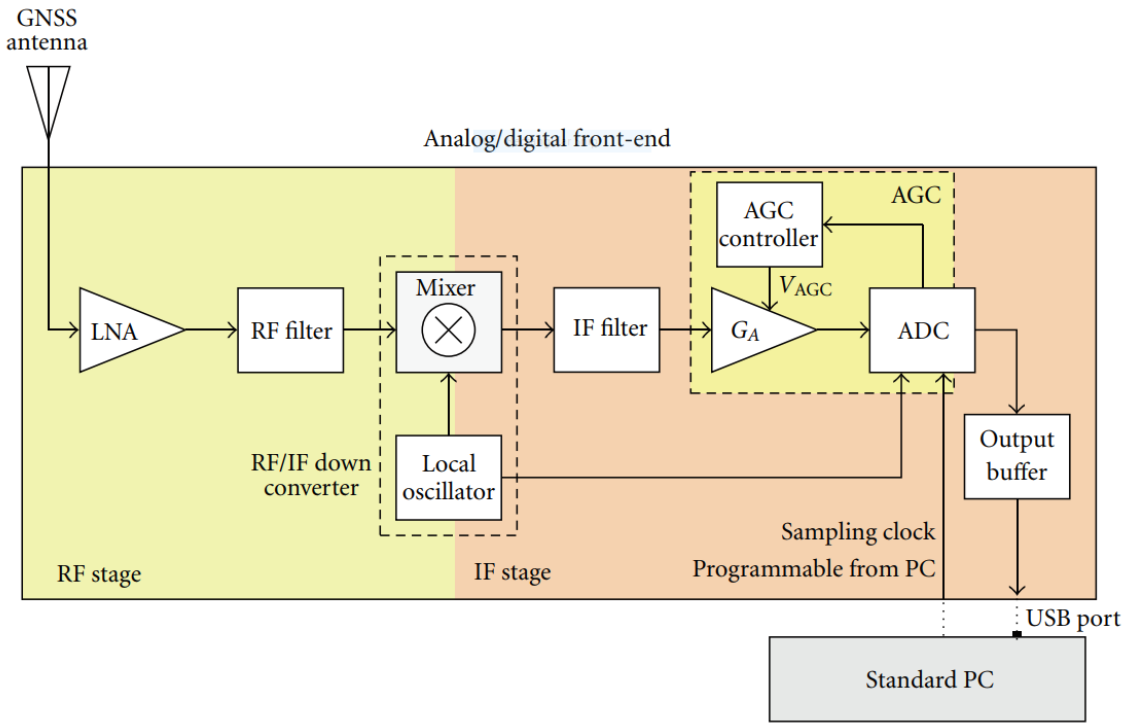


Figure 1.7-1 A simplified architecture of a GNSS front-end [1]

Figure 1.7-1 show RF signal is mixed with the local oscillator to generate modulated sum- and difference- frequency signals. The difference-signal, which is known as intermediate frequency that includes modulated information, accommodates between RF a low frequency information. Therefore, a down-converted IF signal, amplified and demodulated, is produced by difference-frequency is filtered out of mixer circuit. Down conversion is used for efficiency and adjusting for additional interference. Having sampled the baseband IF in the above architecture, a digital baseband I and Q components are created. The ADC is used for converting the signal to digital domain before running signal processing algorithms in order to create high-data-rate digital stream[18]. With the aim of accomplishing signal acquisition, tracking, and navigation, an independent channel is needed for each satellite that is being processed.

The signal from Nth satellite arrive user receiver, a received signal $r(t)$ can be written as

$$r(t) = \sum_{n=1}^{N} \sqrt{2C}\, c_n\big(t - \tau_n(t)\big) d_n\big(t - \tau_n(t)\big) \times \cos\Big(2\pi f_{RF}\big(t - \tau_n(t)\big)\Big) + n(t) + I(t) \tag{1-2}$$

where noise, $n(t)$, potentially interference, $I(t)$, and propagation delay, (τ_n), the noise $n(t)$ is white noise across hall bandwidth B considered for processing and with a power spectral density of N_0 and received signal strength C describes the signal to noise C/N_0 [3, 6, 14, 18]. The noise power spectral density is at the $-174\ dBm/Hz$ [6]. The timely varying delay also results in a Doppler shift [6].The Doppler shift can be defined as

$$f_{D,n} = -\frac{f_{RF}}{c}\frac{d\tau_n(t)}{dt} \tag{1-3}$$

with the speed of light c. The received signal $r(t)$ is filtered by front end and processed by DSP. In the digital signal stages, the receiver generates a clone of genuine signal with adding τ and Doppler f_D and through auto-correlation filter approach it acquires the estimates values $\hat{\tau}_n, \hat{f}_{D,m}$:

$$\hat{\tau}_n, \hat{f}_{D,m} = \arg\max_{\tau, f_D} |P(\tau, f_D)| \tag{1-4}$$

with the correlator value $P(\tau, f_D)$ over the coherent integration time T_{coh} written as

$$P(\tau, f_D) = \int_{t_0}^{t_0 + T_{coh}} \tilde{r}(t) c_n(t - \tau) \exp\big(2\pi j\big(f_{RF} + f_{D,m}\big)t\big) \tag{1-5}$$

where filtered signal $\tilde{r}(t)$, the desired filtered GNSS signal $\tilde{s}(t)$, filtered noise $\tilde{n}(t)$, and filtered interference $\tilde{I}(t)$. Matched filter provides that only the desired signal from satellite n correlates with clone signal or more accurately that the cross-correlation of the interference or of the noise with the clone is much smaller than the matched filter [6].

At the signal processing stage, acquisition is the phase that adjusting a channel to certain satellite when ranging code delay of the satellite and a carried out assigning PRN code each incoming signal [1, 18]. This is synchronization that runs a two dimensional search in the frequency and time domain [1]. The received signal is matched with a stored clone of the associating ranging code of the certain satellite [1, 18].

Then, the tracking loops use the output of this matching filter as an input with the aim of computing the code delay and accurate estimation of the carrier phase. The navigation message can be decoded while the tracking loop synchronisation parameters are locked so that the time delay of the ranging code is detected [1, 14, 18]. After that, the input of the navigation processing functions is described the parameters generated by the signal processing block. The measurements of time delay are converted into variable coefficient of the distances from the user terminal to the pseudo ranges during navigation [1, 18]. Hence, the navigation message is decoded to detect ephemeris that is a sort of refined orbital parameters, and from those, to calculate position of the satellite in the sky [18]. The user position can be finally computed with the pseudo ranges data and the satellite positions [1, 18].

1.8. The Spoofing Threat

Spoofing will occur when interference signal $I(t)$ has same characteristic as $s(t)$ causing also unique shapes for $G_S(f)$ is the spectrum of $s(t)$, and $G_I(f)$ is the spectrum of $I(t)$ for which a maximum overlap may be provided [6]. The spoofing signal for certain satellite at the receiving antenna can be described as

$$I(t) = \sqrt{2C_I}c\big(t - \tau_I(t)\big)d_I\big(t - \tau_I(t)\big)\cos(2\pi f_{RF}(t - \tau_I(t)) \tag{1-6}$$

with the delay $\tau_I(t)$ associated with true delay $\tau_m(t)$ for the considered satellite n through intentional offset $\Delta\tau(t)$

$$\tau_I(t) = \tau_m(t) + \Delta\tau(t) \tag{1-7}$$

Several different types pf spoofing attacks can exist, which is related to spoofer power $C_I(t)$ and the certain form of applied spoofing delay $\tau_I(t)$ [6].

The correlation values $P_I(\tau, f_D)$ of GNSS receiver in presence of genuine and a spoofing signal defines the impact of a spoofing attack, as follows:

$$P_I(\tau, f_D) \sim \sqrt{2C} d_n(t) R(\tau - \tau_n(t)) \times sinc((f_D - f_{D,n}) T_{coh}) e^{j\phi_n} + \tilde{n}(t) \qquad (1\text{-}8)$$

$$+ \sqrt{2C_I} d_I(t) R(\tau - \tau_n(t) - \Delta\tau_I(t))$$

$$\times sinc((f_D - f_{D,I}) T_{coh}) e^{j\phi_I}.$$

The Doppler frequency $f_{D,I}$ of the spoofer is described with equation (3) and it may be applied additional nongeometric Doppler offsets. The symbols ϕ_n and ϕ_I are phase offset authentic and replica of signal, $R(\tau)$ is the normalised matching value of the GNSS signal $c(t)$ at a delay τ and genuine data d and interfered data symbols d_I [6].

There are wide variety of different spoofing attacks exists in literature [3, 6].First one is the navigation message attacks that spoofer can demodulate navigation data $d(t)$, which includes the clock and ephemeris data, predict , change it and retransmitted it with adding false position, ranging, and timing information estimates at the user terminal. If $\Delta\tau \sim 0$ and $C_I > 0$, this attack is possible.

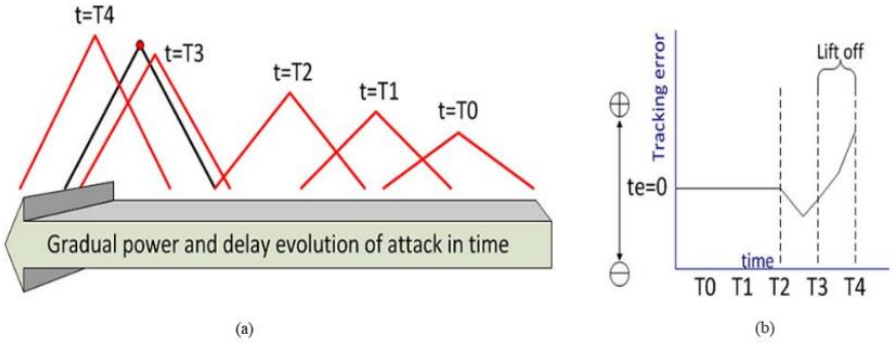


Figure 1.8-1 Lift-off-delay spoofing attack (a) and corresponding tracking error te (b) with spoofing commenced at T2 [6]

Lift-of-delay is an attack type that spoofer approaches the genuine signal with a relative delay $\Delta\tau_I(t)$ with arranging power of signal Figure 1.8-1. It shows at $\Delta\tau_I(t = T2)$, the spoofer approaches genuine signal with a delay with less power, and then, when $\Delta\tau_I(t = T3)\sim 0$, the C_I power become having higher power than genuine signal C and the delay $\Delta\tau_I(t)$ cause moving farther away from the original route [6]. From Figure 1.8-2, Meaconing attack is a fixed delay clone spoofing signal, which power level is adjustable, however, interference time delay constant. In this attack, signal repeats at multipath with power level $C_I < C$ so that ranging precision of receiver degrades.

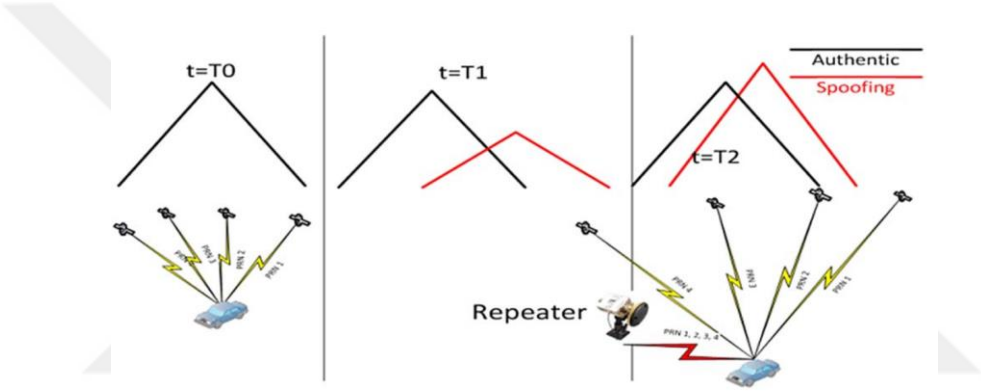


Figure 1.8-2 Meaconing attack: introducing a delayed replica with varying amplitude [6]

1.9. Detection and Mitigation of Spoofing

Anti-spoofing can be incorporated at GNSS system level by signal design and this level techniques are grouped as their capabilities [29]. Clock state monitoring method is proposed [29], this technique is built on single antenna spoofing source, while PRNs are received from different satellites with different directions. This method is appropriate for unsophisticated receivers with calibration. Multipath detection techniques use signal quality monitoring (SQM) to identify underway spoofing attacks and SQM-based methods have simple structures, which a test-statics with a combination of autocorrelation function and correlation values at difference spacing , however, suffered from degradation of performance unlocked spoofing cases in the presence of multipath [6, 30-32]. Absolute power monitoring includes measuring the received

signal strength versus the expected signal levels [29]. Since signal varying due to atmospheric interference and be changed by the automatic gain controller. Thus, the risks of false alarms could be serious problem so that AGC in receivers makes them more vulnerable to spoofing in order to adjust gain to compensate for fluctuating signal strength [3, 33].

1.9.1. Receiver Techniques

Method of cross checks between carrier phase measurement and code as well as C/N0 monitoring of the individual satellites, range measurements from different frequency bands, and step-detections on the unprocessed measurements of all tracked signals can be used as illustrator for spoofing attacks [9]. When received antenna moved and this movement is known from receiver, there is an efficient technique to detect correlations in raw data output from single transmitter antenna spoofing attack [34]. The satellite signals are not spatially correlated, whereas, spoofing signals are correlated. Similarly, high frequency antenna motion can be used spoofing detection and correlation motion [35].

1.9.2. Antenna Techniques

Since wide range of the spoofing attacks are used by a single transmitter, matrix or array processing technique is the best approach to detect and spoofing attacks by using spatial dimension [9]. Using an array of multiple antennas receiver describes the angle of arrival between spoofed and non-spoofed situation [12, 35-40]. With dual antenna architecture, the genuine signal properties used to detect spoofing are the associations with the signal arrival directions to the vector that points from one antenna the other [36].

Figure 1.9.2-1 demonstrates the geometry of single satellite s is the unit of sights vector to a GPS satellite b is the baseline vector between two antenna in units of L1 cycles and lines of constant phase transmitted from the certain satellite illustrated by graphical form of parallel lines that are orthogonal to s and separated by wavelength of the L1 carrier frequency [41]. For the nth satellite, carrier phase difference between two antennas defined as:

$$d\phi_n = b^T A\hat{s}_n + N_n + B + \gamma_n \qquad (1\text{-}9)$$

where A is a direction of cosine matrix to rotate vectors in the east-north-up body frame, N_n is an integer of satellite, $\hat{s}_n$ is the unit line of sight vector to satellite in east-north-up frame B is time varying delta-clock term and γ_n is the all carrier phase error [41].This equation (9) terms can be eliminated because of atmosphere has common mode millimetre level, whereas meter level baseline is assumed between antennas and for twin antenna receiver with a local oscillator, B must be constant and it depends on the difference of electrical length of the pathways from antennas two receivers. If the measurement of $d\phi_n$ is not as same as desired values with in boundary region expected altitude precision and noise, then spoofing signal is detected with a simple way [41].

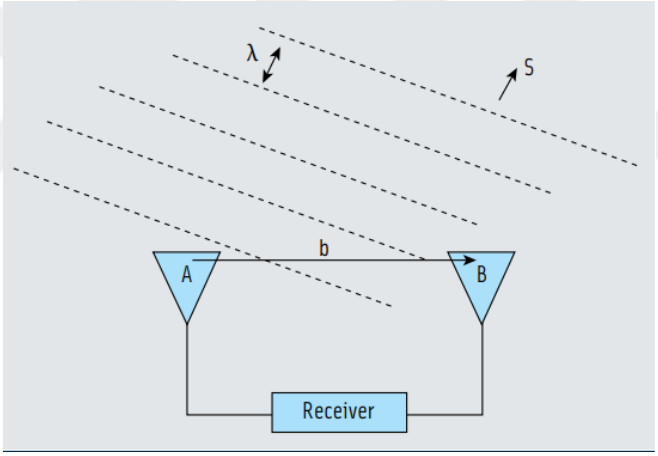


Figure 1.9.2-1 Antenna diversity geometry for a single satellite[42]

In summary, multiantenna architectures estimates direction of arrival of received signal and matched them with the expected ones by using adapting antenna gain pattern and ephemeris of satellites towards desired satellite positions. Then, it nulls the spoofed signal.

2. ESSENTIAL BACKGROUND OF RECEIVER

2.1. Receiver Sensitivity

RF sensitivity is S the minimum usable received RF signal is that can provide a specified signal-to-noise ratio at a user's receiver [24].The main contributors to receiver are transmitter noise relative to the unmodulated RF carrier, Johnson thermal noise density ($kT = 174dBm/Hz$), receiver quiescent (dc) shot noise $(2qI_{Q,rx})$, noise at the image frequency, and mixer noise "noise balance" [24]. All of them can be dealing with by referring noise components back to receiver input, taking the power sum relative to kTB to get the total noise figure (NF_T) for computing noise floor. Then receiver sensitivity is

$$S = k.T.B.SNR.NR_T \tag{2-1}$$

or

$$S = k.T.B.(SNR - 1).NR_T \tag{2-2}$$

if the requirement is given with signal-plus-noise-to-noise ratio. Since the available noise power to a receiver of input resistance R_i can be described by

$$V_n^2 = V_{Th}^2(NR_T) \tag{2-3}$$

where

$$V_{Th}^2 = 4kT\int_{f_1}^{f_2} Re(Z)df \tag{2-4}$$

them the actual input received signal voltage sensitivity is

$$V_s = \sqrt{kTB(SNR-1)R_i} \tag{2-5}$$

An LNA is always need in an RF applications and microwave communication receiver. However, more than one LNA stage may be required if far away distance links or expected that very strongly experienced power fades will happen in the RF transmission environment. The receiver dynamic range is degraded by adding additional stage, which means that the minimum received signal strength is divided by maximum allowable input signal. When an additional LNA is placed between the antenna and first receiver stage, one can calculate the dynamic range of receiver and degradation is experienced because of this connection.

2.2. Receiver Thermal and Shot Noise

Most of the noise on the input of a typical receiver consists of both *thermal* and *shot noise*. Since the random motion of charge carriers produces current, and a current in any passive circuit element that consists of loss, such as lossy transmission line, resistors produce a voltage so that these behave as random noise generators [23, 24]. This random current or voltage know as *thermal noise* is directly related to the temperature. This random thermal noise is expressed as non-periodic waveform and it has purely random behaviour, however, it is predicted by the kinetic energy of heat and the power spectrum flat with frequency [23, 24]. Since all frequencies are presented in this thermal noise, it known as *white noise*, which defines that white light made up of all other visible light frequency [23, 24]. The average noise power that can be delivered to a system at a temperature T is defined by

$$N_{th} = kTB \tag{2-6}$$

where the average power in watts N_{th}, absolute temperature in Kelvins, ($K = X°C + 273°$), T,Boltzmann's constant $k = 1.38 \times 10^{-23} \frac{watt}{K}.Hz$, and the bandwidth in which the measurement is made, in hertz. If thermal noise is measured with a true rms voltmeter, and if the noise meter impedance is matched to the impedance of noise source, then the meter will read $E_n = \sqrt{kTBR}$ in volt rms., whereas impedance are not matched and a resistor is considered on its own [24]. Therefore, the available noise voltage will be defined as

$$E_n = \sqrt{4kTBR} \tag{2-7}$$

From Figure 2.2-1, the 2-to-1 voltage drop when a $50\ \Omega$ noise generator is connected to a system for which the input impedance is $50\ \Omega$.

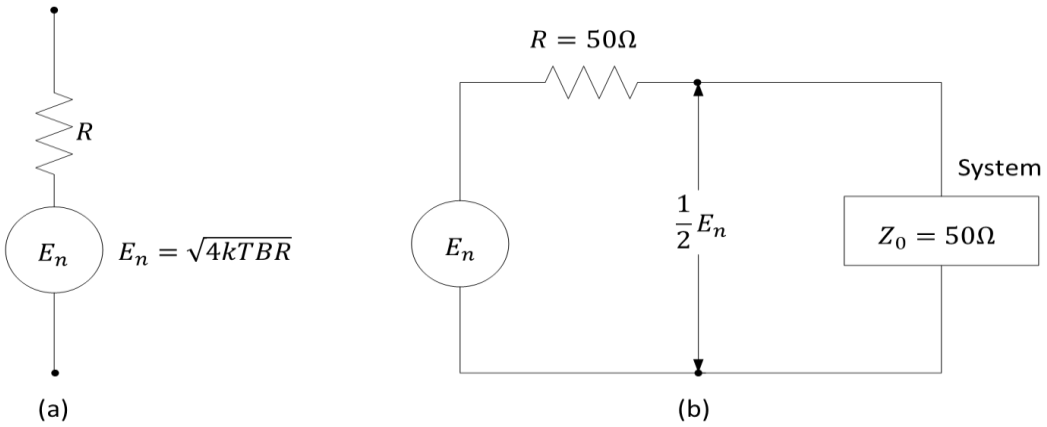


Figure 2.2-1 (a) No power delivered; open circuit equivalent noise generator (b)Power delivered to the system is $N = kTB$, where B is the equivalent noise bandwidth an system the system is impedance noise-matched to noise source [24].

When the electrons with charge q, comprising an average current I_{dc}, cross potential barrier, *shot noise* is produced in semiconductor junctions[24]. A semiconductor diode anode heats up considerably from bombardment of electrons. Besides, transistor generate a noise from random electrons, while some of them go into base current, whereas other go into collector plate current.

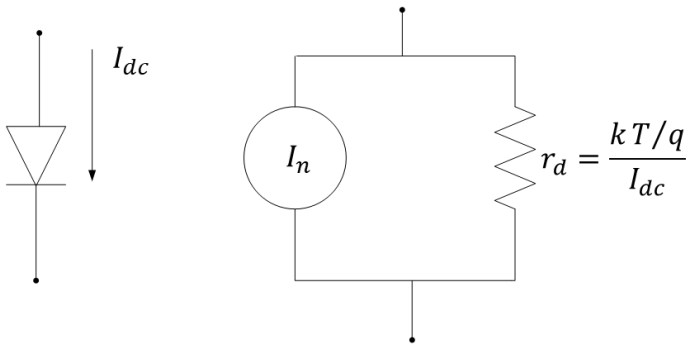


Figure 2.2-2 Shot noise model [24]

The power generated by shot noise is directly proportional to the dc bias current. Shot noise is random like as thermal noise and its power spectrum is flat with frequency. Shot noise is described by below equations

$$I_n = \sqrt{2qI_{dc}B} \tag{2-8}$$

where rms average noise current in amperes rms (I_n), the charge $(q = 1.6 \times 10^{-19}\, Coulombs\, (C))$, dc bias current in the device (I_{dc}), and bandwidth that the measurement is made hertz (B) [23, 24]. These equations are applicable up to frequencies comparable to the inverse of transient time of the electron across the device junction [23, 24]. From Figure 2.2-2, equivalent noise generator concept can be utilized for a diode junction.

2.3. Noise Temperature

In principle, the amount of noise added by noisy front end of receiver can be explained in terms of equivalent temperature [24]. The conversion of noise ratio NR an equivalent noise temperature T_{eq} is

$$T_{eq} = T_0(NR - 1) \tag{2-9}$$

where T_0 is equal to $290K$ as a reference.

Figure 2.3-1 demonstrates equivalent noise temperature of amplifier and the output noise consist of noise power produced by amplifier and power from the source lossy resistor.

$$N = GkTB + GkT_{eq}B \tag{2-10}$$

where GB is product of gain and bandwidth of the amplifier. Low noise antennas and low noise, high gain amplifier used for reduced noise figure and SNR of received can be developed by reducing receiver bandwidth.

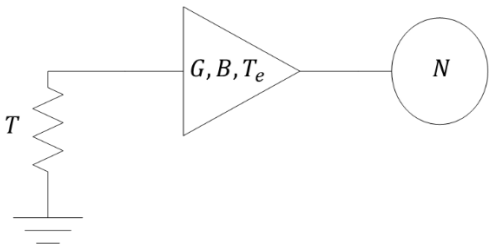


Figure 2.3-1 Equivalent noise temperature of an amplifier

2.4. System Noise Figure

Semiconductor pn junctions and resistor in a receiver generate noise that results in a decline in data owing to rise noise that decrease the proportionality of expected signal relative to noise [24]. Due to transducers, internal noise, and other circuits incline noise power by more than the circuit signal [24].

Receiver noise ratio (NR) is the proportion by which the input signal-to-noise ratio (SNR) and deteriorates because of noisy receiver circuits [24]. The noise figure (NF) is the decibel form of noise ratio $(NF = 10logNR)$. The additional noise is reduced the input SNR so that, for a linear system, the noise ratio (NR) is expressed as

$$NR = \frac{SNR_{In}}{SNR_{Out}} \tag{2-11}$$

or can be written as $SNR_{Out}(dB) = SNR_{In}(dB) - NF.$

These equations expected that the bandwidth used to calculate the input SNR is the net bandwidth of the system [24].

2.5. Receiver Noise

The shot noise and thermal present in electronic components was explained previous sections. Shot noise is related to the bias current in diodes, transistor, whereas thermal noise power depends bandwidth and temperature [24]. The average noise power that can be delivered to a system at temperature T and it is convenient to write an expression in dBm. This is written as follows:

$$10\log(kTB) = 10logkT + 10logB \tag{2-12}$$

or $$10\log(kTB) = 10logkT + 10logB$$

where $k = 1.38 \times 10^{-23}\ W.s/K$ and T is equal to $290\ K$.

Total receiver noise power is described as follows sum of the thermal noise and total noise figure and that is

$$N = (kTB)(NR) \tag{2-13}$$

or, in dBm, $N(dBm) = (-174dBm + 10logN) + NF(dB)$

where NF is the total system noise ratio.

2.6. Derivation of Noise Figure Equations

The noise figure for a system with cascaded amplifiers is derived from simple approach. Firstly, an expression for the amount of noise power internal to a single amplifier is derived, then it is added to the thermal noise present at the input amplifier [24]. Finally, noise figure for cascaded system is derived.

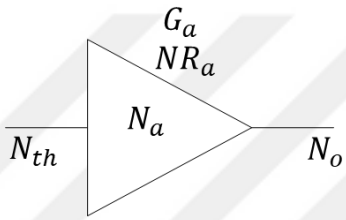


Figure 2.6-1 Amplifier with noise[24]

Referring to Figure 2.6-1, the total noise power at the amplifier output is

$$N_o = N_{th}G_a + N_a \tag{2-14}$$

where the input thermal noise power is amplified by the power gain G_a, N_a is the amplifier noise power and noise power ratio (NR_a). The thermal noise always presents at the input amplifier with $N_{th} = kTB$ where temperature T, bandwidth B and N_{th} watts of power. From definition of noise ratio is the total noise output power divided by amplifier gain and thermal noise power and as follows:

$$NR_a = \frac{N_o/G_a}{N_{th}} \tag{2-15}$$

At output is also written as

$$NR_a = \frac{N_{th}G_a + N_a}{N_{th}G_a} = 1 + \frac{N_a/G_a}{N_{th}} \tag{2-16}$$

Then, the noise power added to any input noise can be rewritten by

$$N_a = N_{th}G_a(NR_a - 1) = N_{th}G_aNR_a - N_{th}G_a \tag{2-17}$$

The input noise times gain is subtracted from total output noise equals noise added by the amplifier.

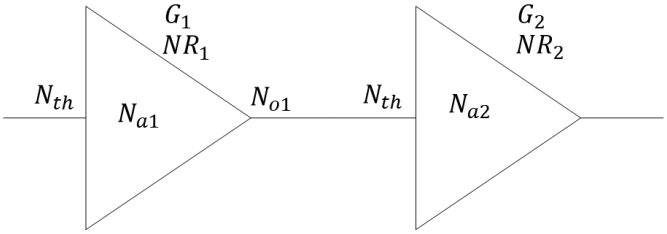


Figure 2.6-2 Two noisy amplifier cascaded [24]

Figure 2.6-2 illustrates the NF of the two-transducers cascade and it is derived from the total noise power at the output transducer

$$N_{o1} = N_{th}G_1 + [N_{th}G_1(NR_1 - 1)] \tag{2-18}$$

Noise power is N_{o1} is amplified by G_2 added amount of noise, $N_{a1} = N_{th}G_2(NR_2 - 1)$, added amplifier 2, that is

$$N_{o2} = N_{th}G_2(NR_2 - 1) + G_2 \tag{2-19}$$

The noise ratio if two amplifiers in cascade, it follows that

$$NR_{system} = \frac{N_{o2}/G_1G_2}{N_{th}} = \frac{N_{o2}}{N_{th}G_1G_2} = 1 + (NR_1 - 1) + \frac{(NR_2 - 1)}{G_1} \tag{2-20}$$

Hence, the final result of system operates in cascade is

$$NR_{system} = NR_1 + \frac{(NR_2 - 1)}{G_1} \tag{2-21}$$

If one extends this procedure to n amplifiers, the system noise figure

$$NR_{system} = NR_1 + \frac{(NR_2 - 1)}{G_1} + \frac{(NR_3 - 1)}{G_1G_2} + \cdots + \frac{NR_n - 1}{G_1G_2 \cdots G_{n-1}} \tag{2-22}$$

is acquired and it is also known as *Friss Formula.* Therefore, the first stage noise figure is the most important. The noise figure contribution of subsequent stages is degraded by the gain of the preceding stage. In fact, the receiver systems ordinarily have low-noise amplifier placed

the closest possible right at the antenna output point to obtain the signal up out of the noise prior further losses in coaxial cable or transmission line.

2.7. Bandwidth Improvement of RF signal

A received signal is essential part of designing the receiver for low noise figure in order to develop signal-to-noise ratio. While passing the entire information bandwidth, unnecessary noise is eliminated by using narrowest possible filters [24]. In the receiver, there are fundamental limitations to improvement achievable by a narrowing the bandwidth. The essential problem is in the difficulty of building stable narrow-band filters.

From Figure 2.7-1, The system circuit bandwidth must exceed the information bandwidth, or the information power and spectrum will be reduced. When the filter is not symmetrical, signal is distorted additionally. The noise-bandwidth improvement factor, BI, is to compute the bandwidth exchange as follows: $BI(dB) = 10 \log\left(\frac{B_{RF}}{B_{IF}}\right)$.

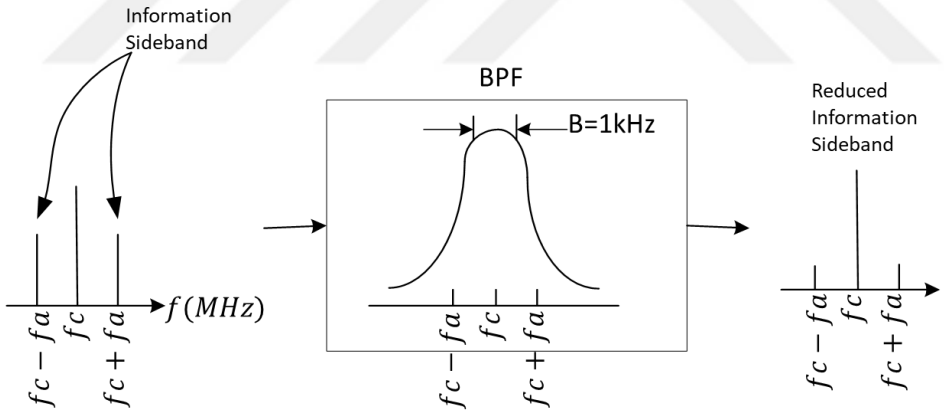


Figure 2.7-1 A filter bandwidth narrower than the information bandwidth, with resulting reduced information power [24]

2.8. Single Stage Amplifier Design

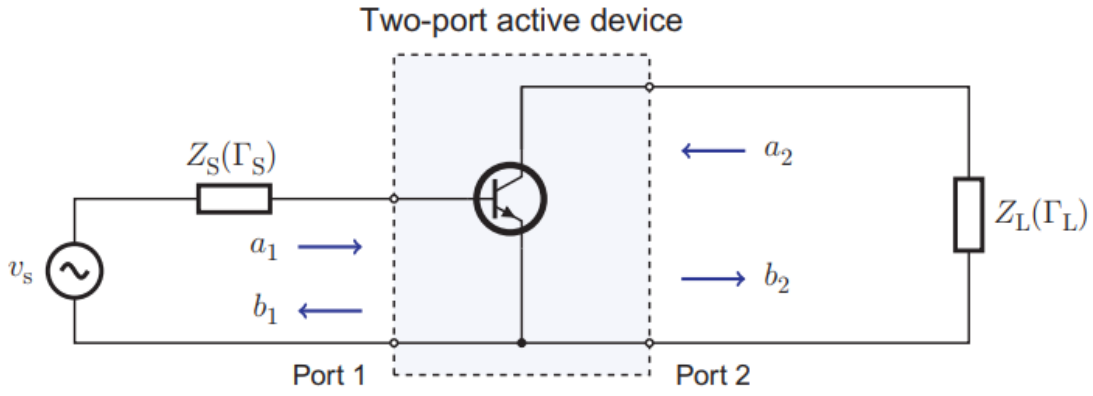


Figure 2.8-1 A single stage amplifier with source and load impedance [43]

One can write expression for the delivered and reflected power waves at the input and output port of amplifier in Figure 2.8-1:

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2-23}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2-24}$$

If no power entering at port 2 and then $a_2 = 0$, one can write expression for the power gain of this circuit is proportion power incident port 1 to power obtaining from port 2, as follows:

$$G = \frac{|b_2|^2}{|a_1|^2} = |S_{21}|^2 \tag{2-25}$$

This is known as power gain G.If one writes an expression for this situation with source and the load termination Z_S and Z_L. From Figure 2.8-1, the reflection coefficient seen looking toward the load is

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2-26}$$

whereas the reflection coefficient seen looking toward to source is

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \tag{2-27}$$

We have to rewrite this equation, as follows:

$$G_T = M_S \times |S_{21}|^2 \times M_L \tag{2-28}$$

where M_S and M_L is source mismatched and load mismatched factor, respectively because of impedance mismatch [44].These demonstrates ratio of power delivered respective loads and power available respective source, it can be written as

$$M_S = \frac{P_{in}}{P_{AVS}} \; and \; M_L = \frac{P_L}{P_{AVN}} \tag{2-29}$$

The M_S and M_L can be written in terms of reflection coefficient terms:

$$M_S = \frac{(1 - |\Gamma_{in}|^2)(1 - |\Gamma_S|^2)}{|1 - \Gamma_{in}\Gamma_S|^2} \tag{2-30}$$

$$M_L = \frac{(1 - |\Gamma_{out}|^2)(1 - |\Gamma_L|^2)}{|1 - \Gamma_{out}\Gamma_L|^2} \tag{2-31}$$

Where P_{AVS} is the power available from the source and P_{AVN} is power available output port. Thus, amplifier power gain can be written as:

$$G_T = \frac{|S_{21}|^2(1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|1 - \Gamma_S\Gamma_{in}|^2|1 - S_{22}\Gamma_L|^2} \tag{2-32}$$

or

$$G_T = \frac{|S_{21}|^2(1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|1 - S_{11}\Gamma_S|^2|1 - \Gamma_{out}\Gamma_L|^2} \tag{2-33}$$

From above equations (36), if we assume $S_{12} = 0$, and then $\Gamma_{in} = S_{11}$ and $\Gamma_{out} = S_{22}$,we can reduce to expression for simple unilateral amplifier power gain:

$$G_{TU} = \frac{(1 - |\Gamma_S|^2)|S_{21}|^2(1 - |\Gamma_L|^2)}{|1 - S_{11}\Gamma_S|^2|1 - S_{22}\Gamma_L|^2} \tag{2-34}$$

It consists of the following terms

$$G_S = \frac{|1 - |\Gamma_S|^2|}{|1 - S_{11}\Gamma_S|^2} \tag{2-35}$$

$$G_O = |S_{21}| \tag{2-36}$$

$$G_L = \frac{|1 - |\Gamma_L|^2|}{|1 - S_{11}\Gamma_L|^2} \tag{2-37}$$

This G_S and G_L do not depend each other so that the input and output port of the device can be independently matched. The maximum gain delivering occurs when $\Gamma_S = S_{11}^*$ and $\Gamma_L = S_{22}^*$, then maximum unilateral gain defined as

$$G_{TUmax} = \frac{|S_{21}|^2}{|1-|S_{11}|^2||1-|S_{22}|^2|} \tag{2-38}$$

2.9. Circle of Constant Unilateral Gain

The $G_O = |S_{21}|^2$ is the fixed value from equation (36,37,38) for given device. Therefore, G_S and G_L values are adjustable. G_S value reach a peak when the input port conjugately matched, which means $\Gamma_S = S_{11}^*$ .Then, it can be rewritten as

$$G_{Smax} = \frac{1}{1-|S_{11}|^2} \tag{2-39}$$

The normalised unilateral gain parameter,

$$g_{Su} = \frac{G_S}{G_{Smax}} = \frac{|1-|\Gamma_S|^2|}{|1-S_{11}\Gamma_S|^2}(1-|S_{11}|^2) \tag{2-40}$$

The equation below forms a circle on the Γ_S:

$$\left|\Gamma_S - C_{gu}\right| = R_{gu}^2 \tag{2-41}$$

Then, we can write expression for centre and radius of the source plane constant unilateral gain circle, as follows:

$$C_{Su} = \frac{g_{Su}S_{22}^*}{1-|S_{22}|^2(1-g_{Su})} \tag{2-42}$$

$$R_{Su} = \frac{\sqrt{1-g_{Su}}(1-|S_{22}|^2)}{1-|S_{22}|^2(1-g_{Su})} \tag{2-43}$$

where the centre C_{Su} and C_{Su} radius of circle. We can make same analysis for G_L.Therefore we can use same equation (40, 42, 43) with interchanging components S_{11} to S_{22} and S_{22} to S_{11} for G_L. These expressions can be used in a computer-aided design program for constant unilateral figure and it is computed more precisely.

2.10. Stability

A transistor amplifier must be stable. Unless either the input or output has a positive real part, which means that this would imply that $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$, oscillation is probable [23]. The amplifier stability depends on Γ_s and Γ_L as adjusting matching network, these values directly related to Γ_{in} and Γ_{out}.If $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for load impedance and all passive source, system unconditionally stable. However, these expressions are only certain range of passive source and load impedance, system is defined as conditionally stable or potentially unstable. Because of the input and output matching networks depends on frequency, it is probable that the amplifier is stable at desired frequency region, but it is unstable other regions.

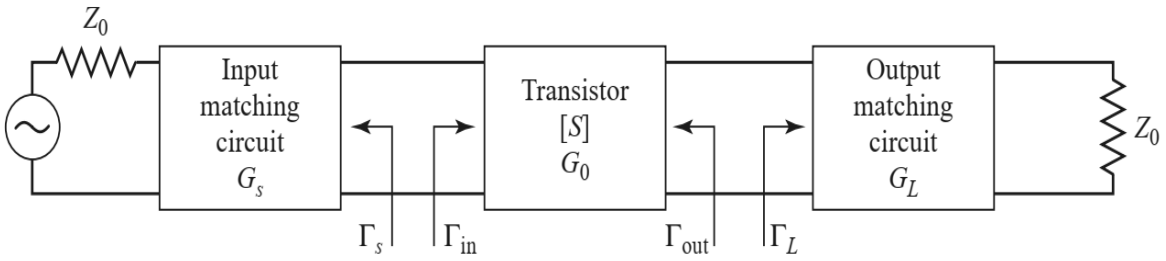
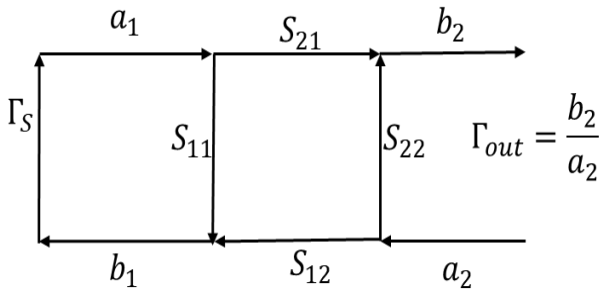


Figure 2.10-1 The general transistor amplifier circuit [23]

In order to an expression for Γ_{out} in terms of Γ_s.Using drawing of signal diagram looking into the output of transistor given Figure 2.10-2 below and from definition of scattering matrices and reflection coefficient $b_1 = S_{11}a_1 + S_{12}a_2$ and $b_2 = S_{21}a_1 + S_{22}a_2$.



$$\Gamma_{in} = \frac{b_1}{a_1} \quad \Gamma_S = \frac{a_1}{b_1}$$

$$\Gamma_L = \frac{a_2}{b_2}$$

Figure 2.10-2 Signal diagram looking into the output of the transistor

$$\Gamma_{out} = \frac{b_2}{a_2} = S_{22} + \frac{\Gamma_S S_{12} S_{21}}{1 - S_{11}\Gamma_S} = \frac{S_{22} - \Delta\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2-44}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$.

One knows that Γ_{out}=1 is the boundary between the stable and unstable region. Above equation (2-44) describes a bilinear transform. Since Γ_{out} is circle so that Γ_s must be circle. The centre and radius can be computed from bilinear transformation theory. If above equation (2-44) is substituted as follows:

$$|\Gamma_{out}|^2 = \Gamma_{out} * \Gamma_{out} = 1 \tag{2-45}$$

If equation is rearranged and note that

$$|\Gamma_S - C_S|^2 = |\Gamma_S|^2 - C_S\Gamma_S^* - C_S^*\Gamma_S + |C_S|^2 = R_S^2 \tag{2-46}$$

describe a circle at complex domain with centre C_S and of radius R_S. Thus, this defines the input stability circle

$$C_S = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \; and \; R_S = \left|\frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2}\right| \tag{2-47}$$

also output stability by interchanging S_{11} and S_{22}.

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \; and \; R_L = \left|\frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2}\right| \tag{2-48}$$

if $|S_{11}| < 1$, which means $|\Gamma_{in}| < 1$ so that Γ_L =0 must be stable region and centre of the Smith Chart stable region which is demonstrated in Figure 2.10-3 (a).On the other hand, if $|S_{11}| > 1$, then $|\Gamma_{in}| > 1$ for Γ_L =0 is the centre of the Smith Chart that must locate at region that is unstable, as illustrated in Figure 2.10-3 (b). These expressions can be used in a computer-aided design program for gain circle and it is computed more precisely.

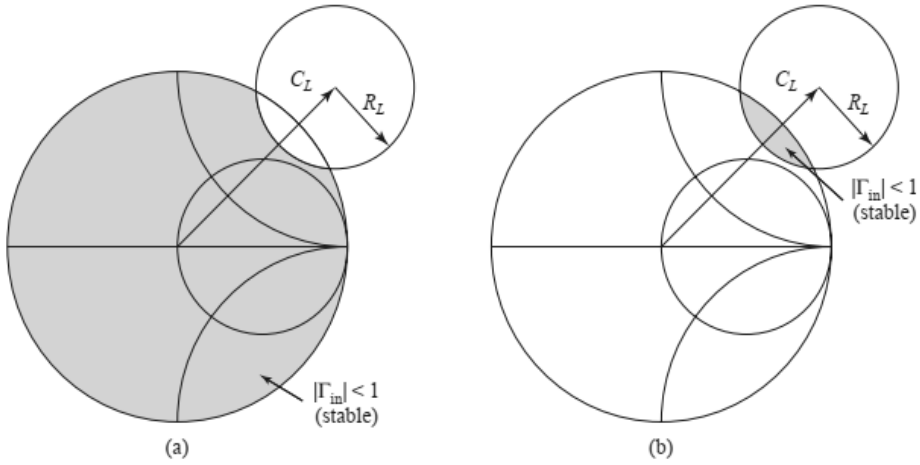


Figure 2.10-3 Output stability circles for conditionally stable device (a) $|S_{11}| < 1$ *(b)* $|S_{11}| > 1$ *[23]*.

2.11. Tests for Unconditionally Stability

The stability circle used to detect regions for Γ_S and Γ_L the amplifier circle will be conditionally stable. Another common stability criterion is the Rollet's stability condition, as defined follows

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2-49}$$

and $|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1$. For stability, $K > 1$ as well as $|\Delta| < 1$.

These expressions can be used in a computer-aided design program for stability and it is computed more precisely.

2.12. Design for Maximum Gain with Conjugate Matching

After stability regions for Γ_S and Γ_L have been accommodated on the Smith chart, the input and output matching section can be designed. When $\Gamma_{in} = \Gamma_S^*$ The maximum power transfer occurs from the input matching network to the amplifier, whereas if $\Gamma_{out} = \Gamma_L^*$ the maximum power transfer occur from the amplifier to output matching network [23].These conditions will maintain maximum power gain. This maximum power gain will be given

$$G_{T_{max}} = \frac{|S_{21}|^2(1 - |\Gamma_L|^2)}{(1 - |\Gamma_{in}|^2)|1 - S_{22}\Gamma_L|^2} \tag{2-50}$$

Besides, the input and output ports of the amplifier will be matched to Z_0. Hence,

$$\Gamma_S^* = S_{11} + \frac{\Gamma_L S_{12} S_{21}}{1 - S_{22}\Gamma_L} \tag{2-51}$$

$$\Gamma_L^* = S_{22} + \frac{\Gamma_S S_{12} S_{21}}{1 - S_{11}\Gamma_S} \tag{2-52}$$

One can solve for Γ_S by re writing these equations as

$$\Gamma_S = S_{11}^* + \frac{S_{12}{}^* S_{21}{}^*}{1/\Gamma_L^* - S_{22}{}^*} \tag{2-53}$$

$$\Gamma_L^* = \frac{S_{22} - \Delta\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2-54}$$

Where $\Delta = S_{11}S_{22} - S_{12}S_{21}$.Then, If one substitutes equation for Γ_L^* into expression for Γ_S and write quadratic equation for Γ_S using $|\Delta|^2 = \Delta(S_{11}^* S_{22}^* - S_{12}^* S_{21}^*)$, as follows

$$(S_{11} - \Delta S_{22}^*)\Gamma_S^* + (|\Delta|^2 - |S_{11}|^2 + |S_{22}|^2 - 1)\Gamma_S + (S_{11}^* - \Delta^* S_{22}) = 0 \tag{2-55}$$

The solution for Γ_S and the solution for Γ_L are referred as [44, 45]:

$$\Gamma_S = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \tag{2-56}$$

$$\Gamma_L = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \tag{2-57}$$

The variables expressions are B_1, B_2, C_1 and C_2 as follows

$$B_1 = 1 - |\Delta|^2 + |S_{11}|^2 - |S_{22}|^2, \tag{2-58}$$

$$B_2 = 1 - |\Delta|^2 - |S_{11}|^2 + |S_{22}|^2, \tag{2-59}$$

$$C_1 = S_{11} - \Delta S_{22}^*, \tag{2-60}$$

$$C_2 = S_{22} - \Delta S_{11}^* \tag{2-61}$$

If S_{12} is equal to 0, which means that $\Gamma_S = S_{11}^*$ and Γ_L=S_{22}^*, and maximum amplifier gain is described as

$$G_{TUmax} = \frac{1}{1 - |S_{11}|^2} |S_{21}|^2 \frac{1}{1 - |S_{22}|^2}, \tag{2-62}$$

If the amplifier unconditionally stable, the equation can be rewritten [43, 45, 46] as follows

$$G_{MAG=}\frac{|S_{21}|}{|S_{12}|}(K \pm \sqrt{K^2-1}) \quad (2\text{-}63)$$

Here the negative sign equation is used if $B_1 > 0$ and $B_2 > 0$. The more useful measurement is the maximum stable gain because device conditionally stable is so that conjugate matching source and load is probable at the same time, which $K < 1$, it is defined as the maximum amplifier power gain of with $K = 1$. Thus,

$$G_{MSG} = \frac{|S_{21}|}{|S_{12}|} \quad (2\text{-}64)$$

The maximum stable gain is simple way to calculate and compare the gain of amplifiers under stable operating conditions.

2.13. Constant Gain Circles and Design for Specific Gain

The specific value of amplifier gain is not obtainable to improve bandwidth. The input and output matching circuit can be designed less gain than expected one purposely. Moreover, the amplifier is on the verge of oscillation at this point since a source mismatched circuit the output reflection coefficient will have magnitude of one, then small changes in the device properties or component could be result in the circuit to oscillation.

It is beneficial to have a figure of merit associated with gain and load or source terminating impedance to determine compromise between gain and other performance. The input port will always be conjugately matched, which operating power gain, G_o, is a function of the load termination, as follows:

$$G_o = \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{|1-S_{22}\Gamma_L|^2-|S_{11}-\Delta\Gamma_L|^2} \quad (2\text{-}65)$$

This equation can be rewritten in the following form with denominator expansion

$$G_o = \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{1-|S_{11}|^2-|\Gamma_L|^2 D_2-2Re(C_2\Gamma_L)} \quad (2\text{-}66)$$

where C_2 and D_2 are described by:

$$C_2 = S_{22} - \Delta S_{11}^* \tag{2-67}$$

$$D_2 = (|S_{22}|^2 - |\Delta|^2) \tag{2-68}$$

The normalized operating power gain parameter, g_o as follows:

$$g_o = \frac{G_o}{|S_{21}|^2} \tag{2-69}$$

Then, using these equations, one can write

$$g_o = \frac{1 - |\Gamma_L|^2}{1 - |S_{11}|^2 - |\Gamma_L|^2 D_2 - 2Re(C_2\Gamma_L)} \tag{2-70}$$

One can rewrite equation of a circle

$$|\Gamma_L - C_{AV}|^2 = R_{AV}^2 \tag{2-71}$$

The solution for the circle is the centre C_{op} and the radius $R_{op,}$ as follows

$$C_{op} = \frac{g_o(S_{22} - \Delta S_{11}^*)^*}{1 - g_o(|S_{22}|^2 - |\Delta|^2)} \tag{2-72}$$

$$R_{op} = \frac{\sqrt{(1 - 2K|S_{12}S_{21}| + g_o|S_{12}S_{21}|^2}}{|1 + g_o(|S_{22}|^2 - |\Delta|^2)|} \tag{2-73}$$

The derivation of constant available power gain circle defines as same as the previous procedure derivation of circle of constant operating power gain. For the available power gain, the solutions for the circle is the centre C_{AV} and the radius $R_{AV,}$ as follows

$$C_{AV} = \frac{g_o(S_{11} - \Delta S_{22}^*)^*}{1 - g_o(|S_{11}|^2 - |\Delta|^2)} \tag{2-74}$$

$$R_{AV} = \frac{\sqrt{(1 - 2K|S_{12}S_{21}| + g_o|S_{12}S_{21}|^2}}{|1 + g_o(|S_{11}|^2 - |\Delta|^2)|} \tag{2-75}$$

These expressions can be used in a computer-aided design program for gain circles and it is computed more precisely.

2.14. Noise Figure and Circle for Low Noise Amplifier

Both the lowest noise figure and the highest gain for an amplifier cannot be obtainable at the same time. Thus, optimal selection must be made. This decision is made by using constant

circle of gain circles and constant noise figure circle to adjust a useful compromise between noise figure and gain.

From throughout the available literature [47] and [44], the noise figure of a two-port amplifier can be defined as

$$F = F_{min} + \frac{R_N}{G_S}\left|Y_S - Y_{opt}\right|^2, \tag{2-76}$$

where source admittance presented transistor,$(Y_S = G_S + jB_S)$, minimum noise figure of transistor, F_{min}, optimum source admittance, Y_{opt}, real part of source admittance, G_S, and equivalent noise resistance, R_N [23].

One uses the reflection coefficient Γ_S and Γ_{opt} instead of Y_S and Y_{opt} where

$$Y_S = \frac{1}{Z_0}\frac{1-\Gamma_S}{1+\Gamma_S} \tag{2-77}$$

$$Y_{opt} = \frac{1}{Z_0}\frac{1-\Gamma_{opt}}{1+\Gamma_{opt}} \tag{2-78}$$

We can now rewrite the quantity $\left|Y_S - Y_{opt}\right|^2$ in terms of Γ_S and Γ_{opt}

$$\left|Y_S - Y_{opt}\right|^2 = \frac{4}{Z_0^2}\frac{\left|\Gamma_S - \Gamma_{opt}\right|^2}{|1-\Gamma_S|^2\left|1-\Gamma_{opt}\right|^2} \tag{2-79}$$

Besides,

$$G_S = Re\{Y_S\} = \frac{1}{2Z_0}\left(\frac{1-\Gamma_S}{1+\Gamma_S} + \frac{1-\Gamma_S^*}{1-\Gamma_S^*}\right) = \frac{1}{Z_0}\frac{1-|\Gamma_S|^2}{|1+\Gamma_S|^2} \tag{2-80}$$

With using this equation provide the noise figure as

$$F = F_{min} + \frac{4R_N}{Z_0}\frac{\left|\Gamma_S - \Gamma_{opt}\right|^2}{(1-|\Gamma_S|^2)\left|1+\Gamma_{opt}\right|^2} \tag{2-81}$$

Rearranging this equation above gives

$$\frac{(F-F_{min})\left|1+\Gamma_{opt}\right|^2}{4\,R_N/C_N} = \frac{\left|\Gamma_S - \Gamma_{opt}\right|^2}{(1-|\Gamma_S|^2)} \tag{2-82}$$

that can be rewritten as

$$N(1-|\Gamma_S|^2) = |\Gamma_S|^2 + \left|\Gamma_{opt}\right|^2 - \Gamma_{opt}\Gamma_S^* - \Gamma_S\Gamma_{opt}^* \tag{2-83}$$

For an arranged figure F, this solution provides a circle in the Γ_S plane with noise figure parameter, N, as,

$$N = \frac{\left|\Gamma_S - \Gamma_{opt}\right|^2}{1-|\Gamma_S|^2} = \frac{F - F_{min}}{4\,R_N/Z_0}\left|1+\Gamma_{opt}\right|^2 \tag{2-84}$$

Rewriting equation provides

$$|\Gamma_S|^2 - \Gamma_S\frac{\Gamma_{opt}^*}{(1+N)} - \Gamma_S^*\frac{\Gamma_{opt}^*}{(1+N)} = \frac{N - \left|\Gamma_{opt}\right|^2}{(1+N)} \tag{2-85}$$

Adding $\frac{\left|\Gamma_{opt}\right|^2}{(1+N)^2}$ to both sides and describe a circle in the Γ_S plane, as follows

$$|\Gamma_S - C_F| = R_F^2 \tag{2-86}$$

Where

$$C_F = \frac{\Gamma_{opt}}{N+1} \tag{2-87}$$

and the radius is given by

$$R_F = \frac{\sqrt{N^2 + N(1-|\Gamma_{on}|^2)}}{1+N} \tag{2-88}$$

These expressions can be used in a computer-aided design program for noise figure and it is computed more precisely.

2.15. L Matching Network

Impedance matching is important because of reducing amplitude and phase error, improve SNR of antenna and LNA, and maximum power transferred when load is matched with line. Simple matching network generally cheaper and reliable. L-section matching network is designed with two reactive elements to match certain load impedance to a transmission line [23].

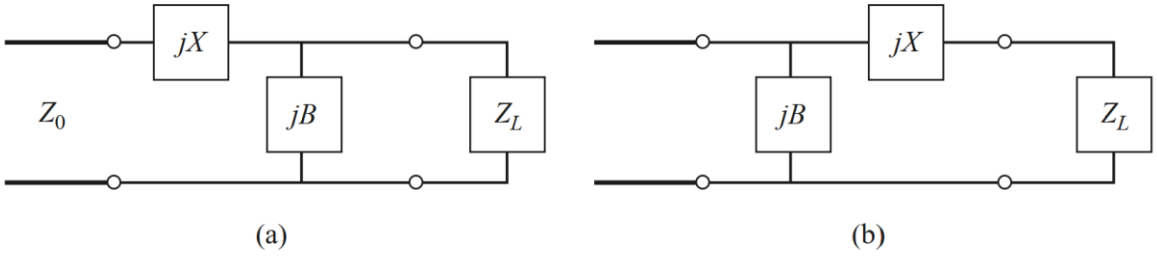


Figure 2.15-1 L-section matching networks (a) Network for z_L inside the 1+jx circle (b)Network for z_L outside the 1+jx circle [23]

Figure 2.15-1 (a) is used when normalised load impedance is inside the $1 + jx$ circle on the Smith chart, whereas Figure 2.15-1(b) is used when load impedance is outside the $1 + jx$ circle on the Smith chart. This circuit reactive element might be either inductor or capacitor [23].

For circuit Figure 2.15-1 (a), impedance Z_0 equation can be written with $Z_L = R_L + jX_L$ if inside the $1 + jx\ as$

$$Z_0 = jX + \frac{1}{jB + 1/(R_L + jX_L)} \tag{2-89}$$

Equation can be rewritten as

$$B(XR_L - X_L Z_0) = R_L - Z_0 \tag{2-90}$$

$$X(1 - BX_L) = BZ_0 R_L - X_L \tag{2-91}$$

The solution for B,

$$B = \frac{X_L \pm \sqrt{R_L/Z_0}\sqrt{R_L^2 + X_L^2 - Z_0 R_L}}{R_L^2 + X_L^2} \tag{2-92}$$

Then series reactance can be found as

$$X = \frac{1}{B} + \frac{X_L Z_0}{R_L} - \frac{Z_0}{BR_L} \tag{2-93}$$

Then, two solution can be possible for X and B. However, one solution is more reasonable in terms of component values. For Figure 2.15-1 (b), impedance Z_0 equation can be written with $Z_L = R_L + jX_L$ if outside the $1 + jx$ as

$$\frac{1}{Z_0} = jB + \frac{1}{R_L + j(X + X_L)} \tag{2-94}$$

Equation can be rewritten with rearranging B and X,

$$BZ_0(X + X_L) = Z_0 - R_L \tag{2-95}$$

$$(X + X_L) = BZ_0R_L \tag{2-96}$$

Solving for X and B gives

$$X = \pm\sqrt{R_L(Z_0 - R_L)} - X_L \tag{2-97}$$

$$B = \pm\frac{\sqrt{(Z_0 - R_L)/R_L}}{Z_0} \tag{2-98}$$

Again, two solutions can be possible for X and B. However, one solution is more reasonable in terms of component values. These expressions can be used in a computer-aided design program for L matching and it is computed more precisely than the Smith chart can give.

3. RECEIVER DESIGN AND SIMULATION

3.1. Receiver Specification

Since project only considering civilian application, for C/A code signal bandwidth $2.048\,MHz$. Then, the noise power within signal for $2.048\,MHz$ signal is about $-110\,dBm$ from eq. (1). Thus, received signal is $-19\,dB$ below noise floor.

$$N_{th}\,(dBm) = -174\,dBm + 10logB \tag{3-1}$$

Total receive noise figure is

$$N(dBm) = (-174dBm + 10logB) + NF(dB) \tag{3-2}$$

In order to find noise figure, we have to calculate

$$NR = \frac{SNR_{In}}{SNR_{Out}} \tag{3-3}$$

Therefore, we are able to recover signal because of the frequency spreading cause of using a pseudorandom binary sequence. Then, the chip rate is $1.023\,MHz$ and the symbol rate is $50\,Hz$ which result in processing gain $43.1\,dB$. Thus, after synchronization with bit stream, signal to noise ratio is $24.1\,dB$. One can assume the required signal the noise of front end by looking bit error rate E/N_0 curves. For BPSK with a BER of 10^{-5} requires a E/N_0 of $10\,dB$ [48]. For BPSK is the same as SNR. Since we have the input and output signal to noise, the signal to noise of the front-end can be calculated. With quantization noise for 1-bit ADC using wideband signal the SNR degrades by maximum $3.5\,dB$. Therefore, maximum noise figure of receiver is approximately $10.6\,dB$ [49].

Figure 3.1-1 demonstrates overall system structure GNSS front end receiver with multiple antenna. System include two LNA, saw filter, two mixers, two IF amplifier and two comparators for demodulation, and one PLL device for frequency synthesize.

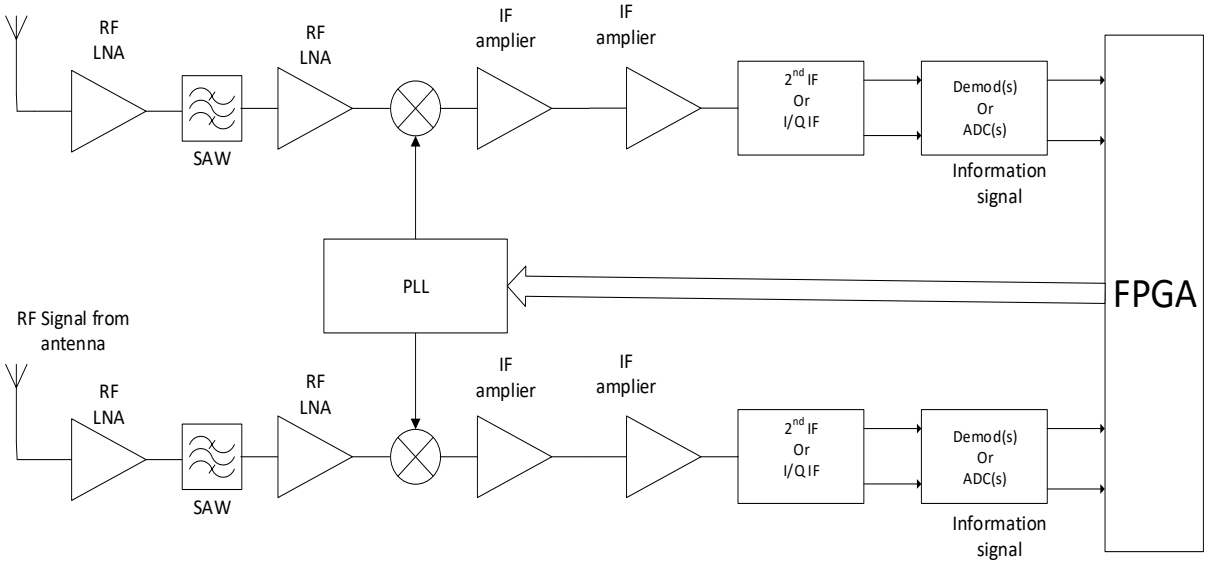


Figure 3.1-1 Overall system structure of receiver with multiple antenna

3.2. Low Noise Amplifier

The fundamental requirements for wide range of satellite communications require low noise amplifiers (LNAs) input stage to optimize the most critical performance parameter, such as the noise figure, low return loss, high gain, and high linearity. The LNA must be matched noise and impedance with the intention of low noise and low return noise. The system noise figure equation is derived in preceding stage. The first stage of receiver system is the most important.

$$NR = NR_1 + \frac{(NR_2 - 1)}{G_1} \tag{3-4}$$

From that equation, the first stage should have the lowest noise and the highest gain. The loss of preceding stage lossy transmission line and filters from antenna, add directly to the NR_1 term. There is compromise between minimum noise and high gain in low noise amplifier design, because the first stage gain is as high as possible, whereas the minimum noise figure needs the noise added by the first amplifier circuit that is the lowest. Hence, the first stage is optimized for minimum noise at moderate gain is the best trade-off, while subsequent stage is made more efficiently for higher gain and moderate noise. Several manufacturers produce high

performance transistors that are suitable for L1 frequency region and this particular design. Frequency range, minimum noise figure, maximum gain and linearity all considered active device selection process. Many devices were quickly eliminated measured s-parameters were not available from the particular manufacturers in electronic form and specifications that produce a design with the desired performance.

Table 3.2-1 Commercially available LNA for GPS receiver features at L1 frequency

Product	***Infineon BFP640 [50]***	***NXP BGU8052[51]***	***MAXIM MAX2679[52]***
Gain (dB)	*21*	*19.5*	*19*
NFmin (dB)	*0.6*	*0.5*	*0.95*
OP1(dBm)	*11.5*	*18*	*25*
OIP3	*25*	*36*	*17*
Icc (mA)	*5*	*50*	*1*
Price	*£0.35*	*£2.6*	*£0.45*

It can be seen from Table 3.2-1 that three different vender's LNAs have different types of features. For MAX2679 has the lowest current consumption, whereas BGU8052 the lowest noise figure. However, when the project aim is to consider, BFP640 is the most effective solution because it provides minimum cost with reasonably noise figure. It has also slightly larger gain at the desired frequency and this is crucial for second stage because it will optimise for higher gain than first stage. The BFP640 is a linear very low noise wideband NPN bipolar RF transistor.

3.3. Small Signal Model BJT

The small signal model of the BJT is shown Figure 3.3-1.The base, r_b, emitter, r_e, collector, r_c , resistance depends on device scale with inverse proportionality[53, 54].Because of buried layer of collector and heavy doping of the emitter, r_e and r_c values are low, however, r_b, is

considerably high because of low doping. Terminal base, C_{be}, emitter, C_{ce}, and collector, C_{bc} has a finite capacitance value, respectively. C_{bc} and C_{be} are often neglected with r_e and r_c because of smaller value. Therefore, the model can be simplified as shown in Figure 3.3-2.

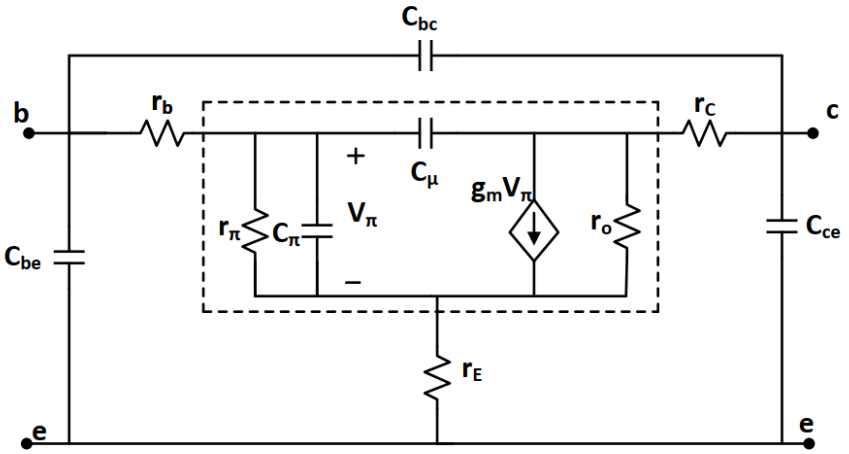


Figure 3.3-1 Small signal model of BJT [55]

The small signal model parameters r_π, c_π, g_m, r_b are related to biasing of transistor. The small signal model can be used to study the high frequency performance of bipolar transistor and to provide two useful parameters the cut off and transition frequency, f_t, and maximum oscillation frequency, f_{max} [53].

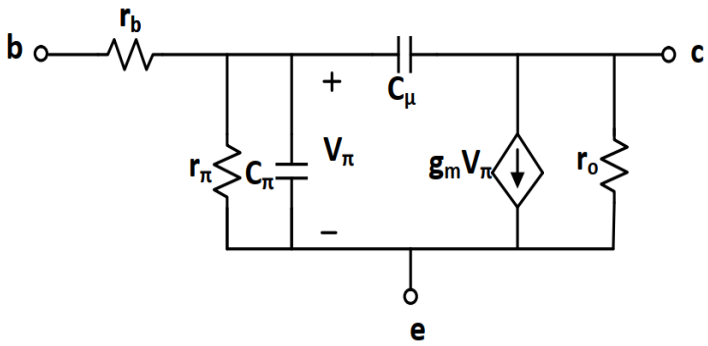


Figure 3.3-2 Simplified small signal model of BJT [55]

"The cut off and transition frequency f_t is frequency at which the magnitude of the AC current gain drops to unity for active device in common emitter configuration with an AC shorted collector" [56].The f_t is determined by

$$f_t = \frac{g_m}{2\pi(C_\pi + C_\mu)} \tag{3-5}$$

where transconductance g_m, and capacitance C_π that is associated with junction capacitor C_{je} and diffusion capacitance C_d. C_d and g_m depends on collector, however, C_{je} depends on voltage. The f_t rises with g_m that increases sharply as compared to C_d. Because of kirk effect and current crowding, f_t rolls off at higher current levels [53, 54]. Frequency response of transistor is shown in Figure 3.3-3.The typical transition frequency approximately 42 GHz, hence active device provides high power gain at frequencies up to 8 GHz.

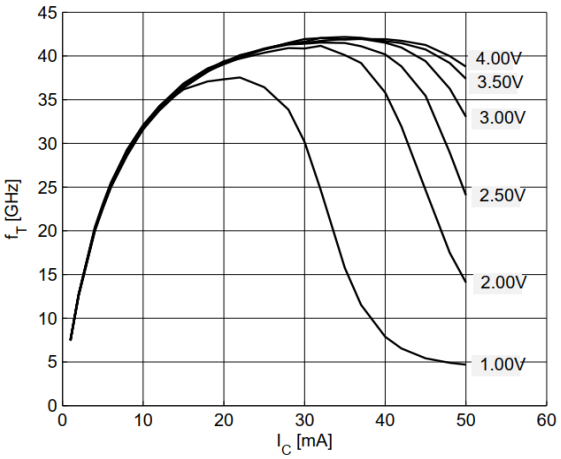


Figure 3.3-3 Transition frequency ft=(Ic), f=2 GHz, VCE= parameter in V [50]

Maximum oscillator frequency f_{max} at which power gain equals one and includes the effect of base resistance , r_b, that provides noise and speed information of transistor [53].The maximum oscillation frequency can be written as

$$f_{max} = \sqrt{\frac{f_t}{2\pi r_b C_\pi}} \tag{3-6}$$

3.4. Biasing

With its high linearity at currents as low as 10 mA the device provide energy efficient design shown in Figure 3.4-1.

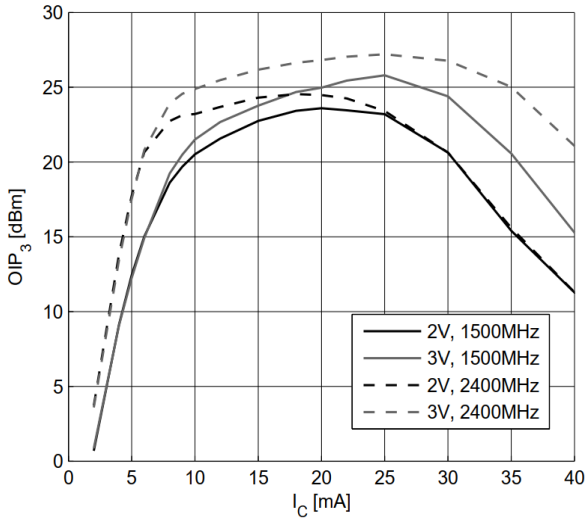


Figure 3.4-1 3rd Order Intercept Point at output $OIP3 = f(Ic)$, $Zs = ZL = 50\,Ohm$, *Parameters:* Vce *in V,* f *in MHz*

The BFP640 should be operated with $V_{CE} = 3V$, $I_C = 5mA$ because of minimum noise figure characteristic from Figure 3.4-3 and Figure 3.4-4.Therefore, amplifier has been designed to meet these specifications over the upper L frequency range. Thus, DC electrical characteristic simulated V_{BE} and I_B are adjusted 0.828 V and 20 μA, respectively for given collector voltage and current respectively and using ADS Keysight simulation at Figure 3.4-2.

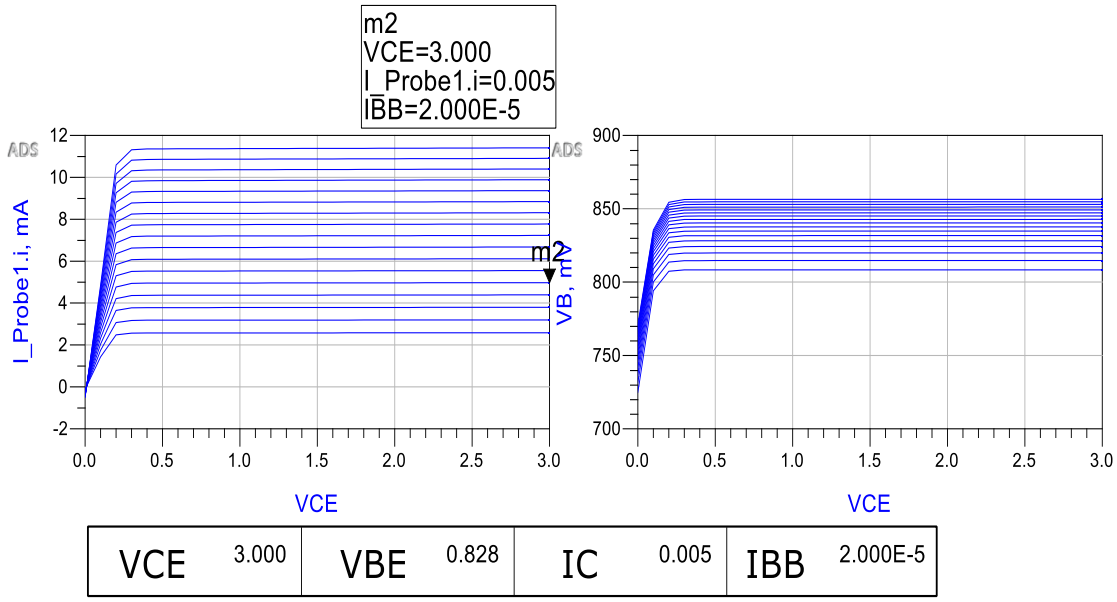


Figure 3.4-2 Collector current vs. collector emitter voltage, V_B *and* I_C

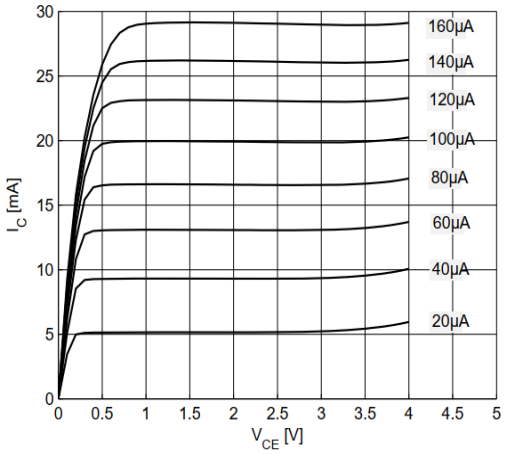


Figure 3.4-3 Collector current vs. collector emitter voltage $I_c = f(V_{CE})$, $I_b = parameter\ in\ \mu A$ [50]

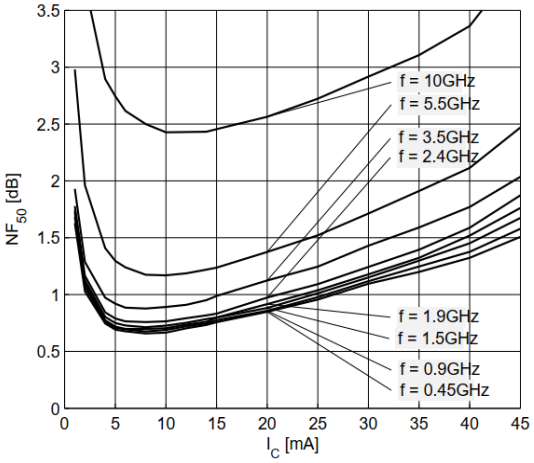


Figure 3.4-4 Noise figure $NFmin = f(I_C)$, $V_{CE} = 3V, I_C = 5\ mA$, $f = parameter\ in\ GHz$ [50]

3.5. LNA Passive Bias Network

The objective of amplifier biasing power efficiency, stability, noise, cost, and prevent thermal run away. In order to decrease receiver cost, passive network biasing scheme is selected. From Figure 3.5-1 (a), collector-feedback bias reduces sensitivity to variations of transistor parameters and thermal runaway. In addition, it is very low-cost biasing scheme for microwave circuits. Besides, other bias network is less sensitive to $\beta(h_{fe})$ variations. A resistor series with the base increase efficiency of thermal stability at Figure 3.5-1 (b).

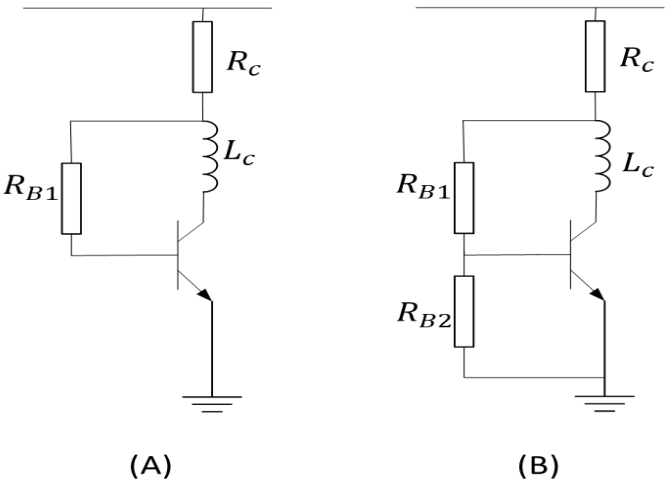


Figure 3.5-1 Transistor passive biasing networks

From DC bias parameters with supply voltage $V_{cc} = 5V$.

$$R_c = (V_{cc} - V_{CE})/I_{cc} \quad (3\text{-}7)$$

$$R_{B1} = \frac{V_{CE} - V_{BE}}{I_B} \quad (3\text{-}8)$$

$$Z_{Lc} = jwL = j2\pi f_{L1} Lc = 50\ \Omega \quad (3\text{-}9)$$

For collector feedback biasing with equations (5) and (6), R_c is $402\ \Omega$, R_{B1} is $107\ k\Omega$, and Lc is $5.6\ nH$ is selected for $50\ \Omega$ from equation (7). They are calculated with computer aided design tool with their real equivalent circuit in order to compute s-parameters precisely because of parasitic effects and their self-resonant frequency, respectively for $V_{CE} = 3V$ and $I_C = 5\ mA$. From DC simulation of collector feedback biasing

In order to determine passive parameters of second circuit $I_{RB2} = 10I_B$

$$R_{B2} = \frac{V_{BE}}{10I_B} \quad (3\text{-}10)$$

$$R_{B1} = \frac{V_{CE} - V_{BE}}{(11I_B)} \quad (3\text{-}11)$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_{CC}} \quad (3\text{-}12)$$

$$Z_{Lc} = jwL = j2\pi f_{L1} Lc = 50\ \Omega \quad (3\text{-}13)$$

For second one, passive circuit component parameters are selected with simulation as well. $R_c = 402\ \Omega$, R_{B1} is $9.76\ k\Omega$, R_{B2} is $4.12\ k\Omega$, and Lc is $5.6\ nH$.

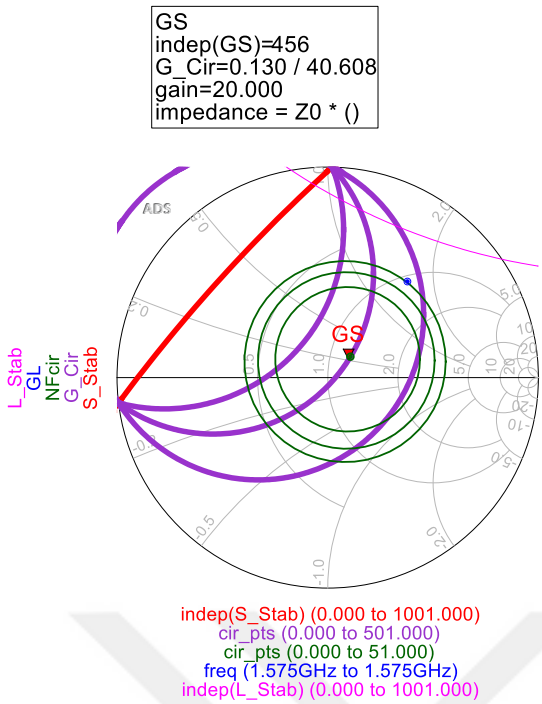


Figure 3.5-2 Collector-Feedback biasing Smith chart

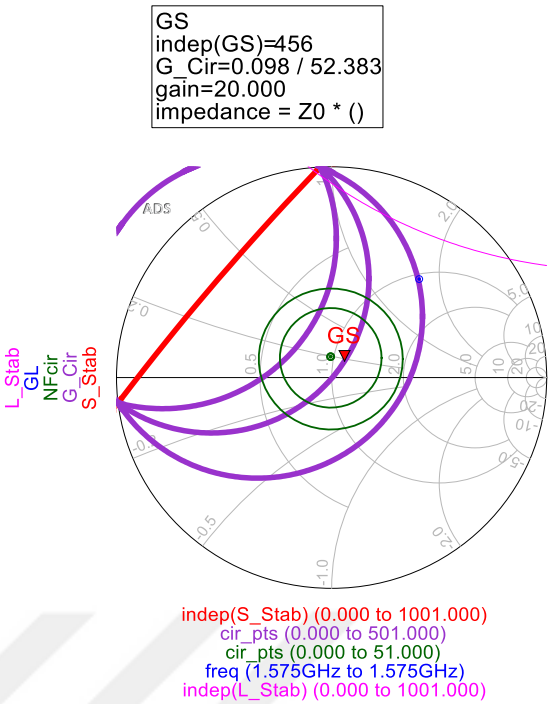


Figure 3.5-3 Base-Biased biasing Smith chart

$G_{max}(dB)$:	21.337	$G_{max}(dB)$:	21.337
NF_{min}:	0.628	NF_{min}:	0.810
Zin:	$60.01 - j10.37$	Zin:	$55.63 - j11$
$Zout$:	$54.55 - j76.70$	$Zout$:	$66.16 + j84.28$
Stability Region:	*Inside*	*Stability Region:*	*Inside*

Thus, when noise figure of two system considered, first system provides smaller noise figure than second one, which are 0.628 and 0.81 respectively. Hence, first one biasing considered for first stage because of importance noise figure of first stage, and second one is improved a slightly better gain for second stage from simulation. Both simulated with real components of AVX 0603 package F tolerance resistors and AVX 0603 package D tolerance inductor to get high precision s-parameters. Both of them must be matched input and output network by L matching network to get reasonable S_{21} with minimum noise and high gain and reasonable

noise figure, respectively. Therefore, matching circuit is designed with L matching analytic solutions for given input and output impedance by Smith chart and simulation tools. Thus,

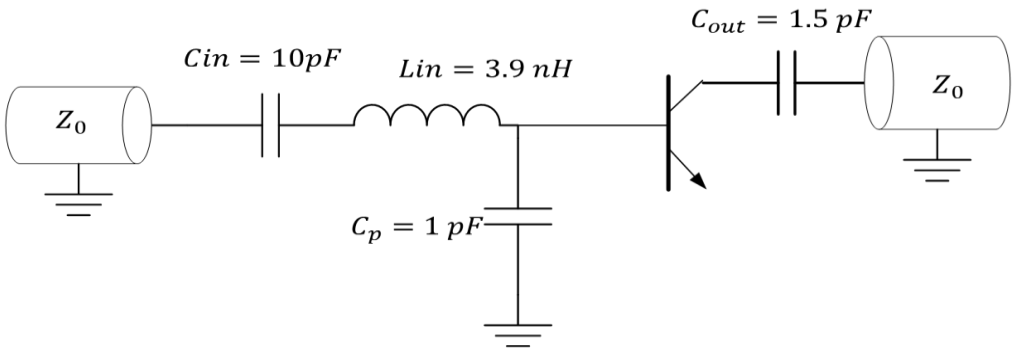


Figure 3.5-4 Collector-feedback biasing input and output matching

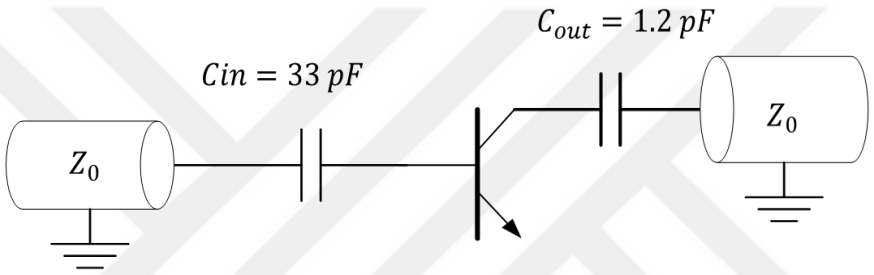


Figure 3.5-5 Base-biased input and output matching

From Figure 3.5-4, collector-feedback biasing networks' input and output matching have capacitor $10\ pF$ series with inductor $3.9\ nH$ and one parallel capacitor $1\ pF$ and one series capacitor $1.5\ pF$ respectively. Again, Figure 3.5-5 Base-biased input and output matching these values used with real equivalent in order to achieve accurate design. For second one, impedance matching network designed with $33\ pF$ input series capacitor and $1.2\ pF$ series output capacitor and it is simulated real component, as well.

The simulated gain, noise figure and reflection are shown Figure 3.5-6, Figure 3.5-8, and Figure 3.5-10 and, respectively. The simulated gain of the amplifier is $18.80\ dB$ at $1.575\ GHz$ and noise figure 0.722 at $1.575\ GHz$. The input reflection coefficient with output terminated with matched load is bigger than $-3.6\ dB$, whereas output reflection coefficient matched with input terminated with matched load is bigger than $-24\ dB$ certain bandwidth. For second stage, the simulated gain of amplifier is demonstrated in Figure 3.5-7 and 19.87 dB for the upper L

frequency centred signal, which has 20 MHz bandwidth. Figure 3.5-9 shows noise figure is 0.856 for given bandwidth. Simulated input and output reflection coefficient are shown in Figure 3.5-11 and Figure 3.5-13 NF of stage 1 and stage 2. The measured input reflection coefficient is over $-4\ dB$, and output reflection coefficient is $-26.6\ dB$, respectively.

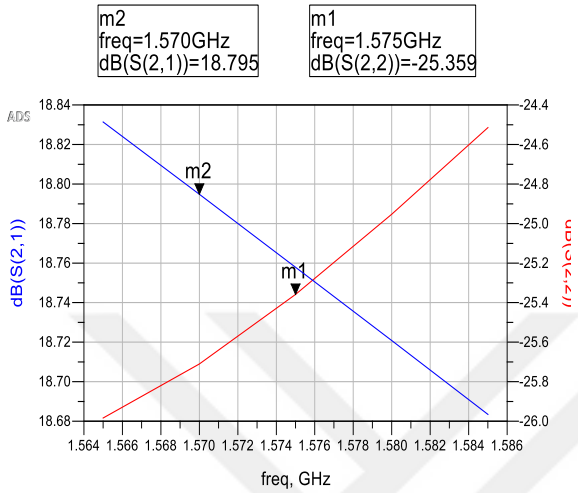


Figure 3.5-6 LNA stage 1 S21 and S22 simulation

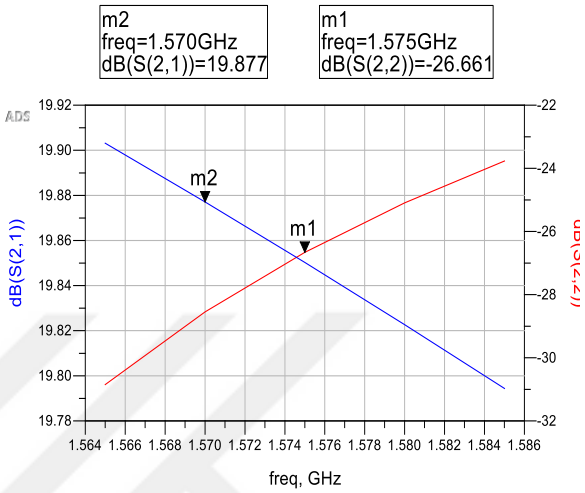


Figure 3.5-7 LNA stage 2 S21 and S22 simulation

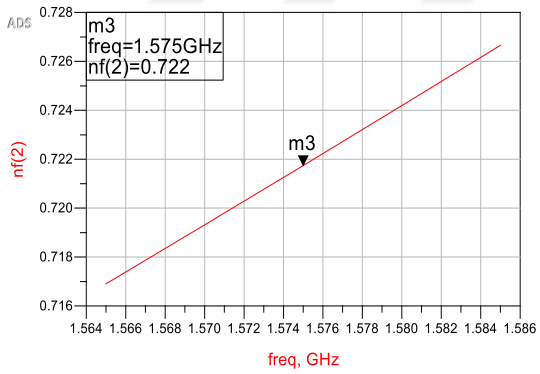


Figure 3.5-8 LNA first stage NF

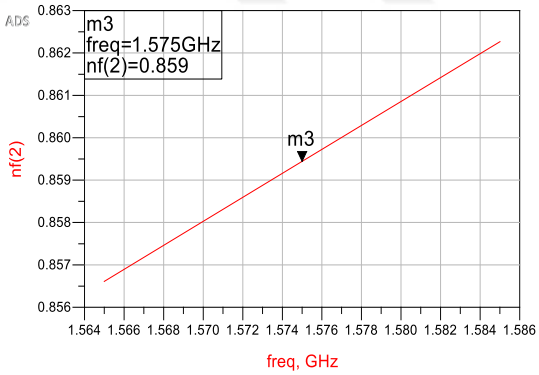


Figure 3.5-9 LNA second stage NF

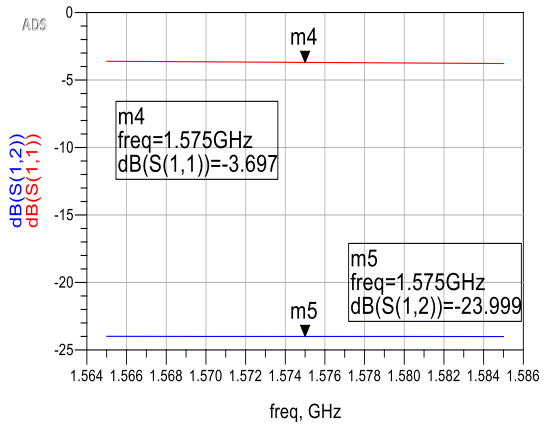


Figure 3.5-10 LNA stage 1 S11 and S12

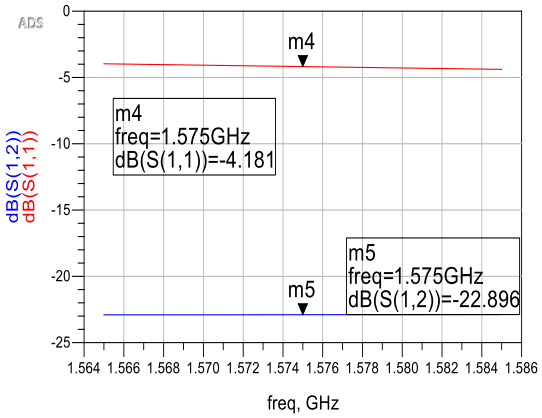


Figure 3.5-11 LNA stage 2 S11 and S12

The simulated overall two stage gain and noise figure are shown in Figure 3.5-12 and Figure 3.5-13.The simulated gain of combined amplifier is 35.90 *dB* and noise figure is 0.748 at certain frequency range. The noise figure is closed enough to first stage as described preceding sections.

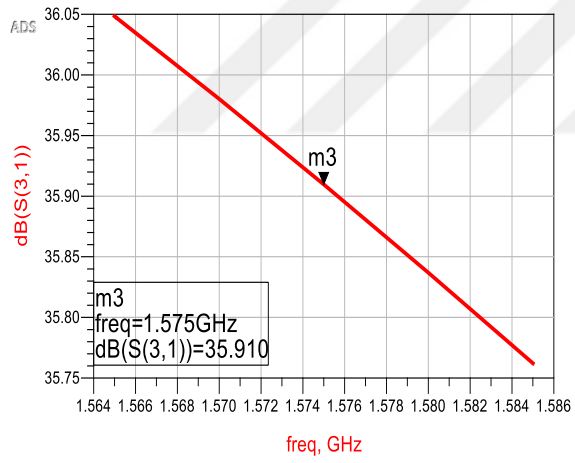


Figure 3.5-12 Gain of stage 1 and stage 2

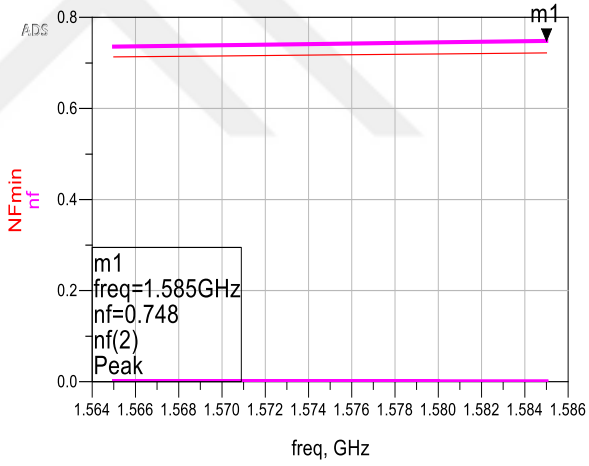


Figure 3.5-13 NF of stage 1 and stage 2

3.6. SAW Filter

According to *Friss Formula*, if first stage is LNA, it dominates noise figure with respectable gain. However, if the strong spectral component interferers in the amplifier bandwidth, LNA goes saturation and yields spurious frequencies [21, 22]. This drawback can be overcome by filter positioned before LNA to attenuates out of band components and it works well when strong signal interferes adjacent to upper L frequency carrier [1]. However, this solution

increase noise figure of front end approximately 2 or 3 dB because of insertion loss and decrease overall gain first stage. Thus, SAW filter is placed between two LNA amplifier because it is desired not only low noise figure but also gain as possible.

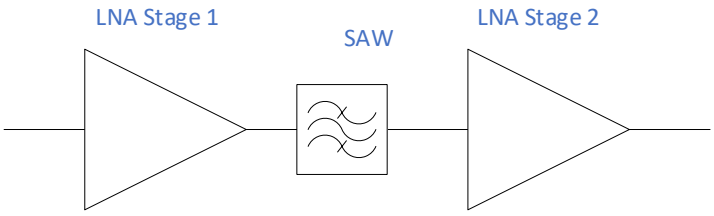


Figure 3.6-1 Construction of RF stage

The receiver must be able to process desired while sufficiently rejecting strong neighbouring signal. These kinds of filters usually efficient to determine at RF frequencies and their cut off requirements. The Filter attenuation is approximately 1.6 dB from Figure 3.6-2. As explained chapter 2, bandwidth narrowing improve SNR and decrease the noise figure. There are several manufacturers are available and they sell similar characteristic system same price, which is £1.5. Therefore, the TDK RF360 is selected for availability reason. Reference to Figure 3.6-1, RF stage provides high gain and low noise distortion. From Figure 3.6-3 Gain of stage1 and 2 with a SAW filter and Figure 3.6-4, RF stage provides 1.5 dB more gain without affecting noise figure from simulation by using saw filter between two stages.

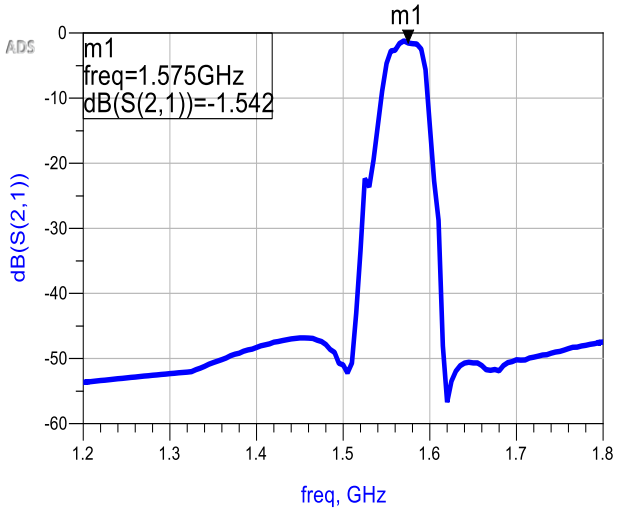


Figure 3.6-2 Transfer function SAW RF360

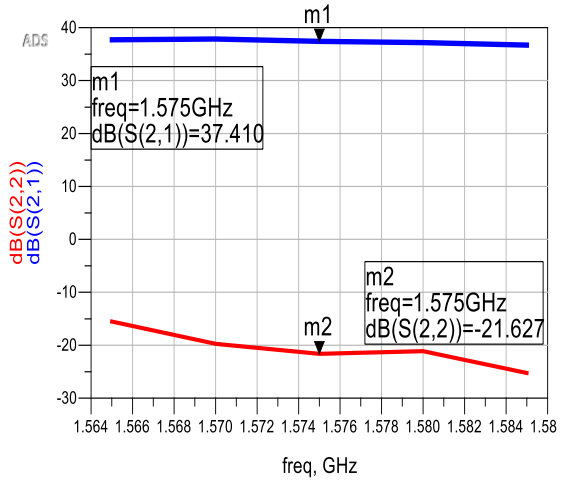


Figure 3.6-3 Gain of stage1 and 2 with a SAW filter

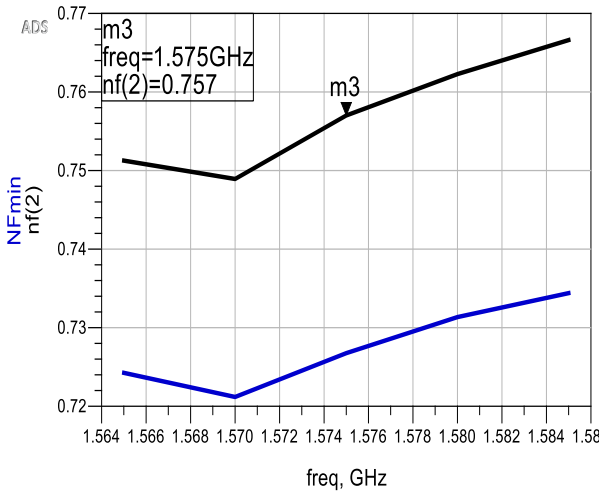


Figure 3.6-4 NF of gain of stage 1 and 2

3.7. MIXER

Generally, every high frequency receiver uses a mixer to down converter the received RF signal to an intermediate frequency (IF) signal[24]. A mixer in RF systems is a circuit that has nonlinear component result in sum and difference frequencies to be produced [24]. An RF mixer needs a nonlinear circuit component, which is expressed mathematically by a power series and the nonlinearity generated in switching or sampling mixers, as follows:

$$i_o = I_o + av_i + bv_i^2 + cv_i^3 + \cdots + nv_i^n \tag{3-14}$$

The magnitude of LO signal is much greater than that of the RF signal and is represented as unity and substituting equation is given by reference to [24]:

$$i_o = I_D + acosw_{LO}t + aAcosw_{RF}t + b(cosw_{LO}t + Aacosw_{RF}t)^2 \tag{3-15}$$

$$i_o = I_D + acosw_{LO}t + aAcosw_{RF}t + b(cosw_{LO}t)^2 + 2bAcosw_{LO}tcosw_{RF}t + b(Acosw_{RF}t)^2$$

By using trigonometric identities,

$$i_o = I_D + (input\ signal\ and\ 2nd\ harmonic\ current) + 2bAcosw_{LO}tcosw_{RF}t \tag{3-16}$$

$$I_D = (I_o + \frac{b}{2} + \frac{bA^2}{2})$$

where term of the mixer product

$$2bAcosw_{LO}t \times cosw_{RF}t \quad (3\text{-}17)$$

By using trigonometric identity

$$2bAcosw_{LO}t \times cosw_{RF}t = bA(cosw_{LO} + w_{RF)}t + bA(cosw_{LO} - w_{RF})t \quad (3\text{-}18)$$

We have intermediate frequency of $f_{IF} = f_{RF} - f_{LO}$. If it is generalised, the higher-power terms may be treated as a compound of second power.

$$cv^3 = c(v^2 \times v) = c[(v_{LO} + v_{RF})^2(v_{LO} + v_{RF})] \quad (3\text{-}19)$$

These produces the polarities of each cross product

$$f_{RF} \pm f_{LO}, 2f_{LO}, 2f_{RF}, 2f_{LO} \pm f_{RF}, 2f_{RF} \pm f_{LO}, 3f_{LO}, 3f_{RF} \quad (3\text{-}20)$$

In decibels, the conversion loss is

$$C_{loss} = 10log_{10}(\frac{Pin(RF)}{Pout(IF)}). \quad (3\text{-}21)$$

Table 3.7-1 Commercially suitable mixer for GNSS receivers

	Maxim ***MAX2680[57]***	***Analog Devices*** ***ADL5811[58]***	***Texas Instrument*** ***TRF37x32[59]***
Technology	*Double Balanced*	*Double balanced*	*Dual Downconverter*
Noise Figure	*8.3 dB*	*10.7 dB*	*9.5 dB*
Conversion Loss	*7.6 dB*	*7.5 dB*	*10 dB*
RF Maximum frequency	*2500 MHz*	*2800 MHz*	*2700 MHz*
RF Minimum frequency	*400 MHz*	*700 MHz*	*700 MHz*
IF maximum	*500 MHz*	*450 MHz*	*600 MHz*
IF minimum	*10 MHz*	*30 MHz*	*30 MHz*
Price	*£ 1.32*	*£ 14.16*	*£ 16.31*

Several manufacturers produce high performance mixers that are suitable for L1 frequency region and this particular design. Frequency range, minimum noise figure, and conversion loss all considered active device selection process. Many devices were quickly eliminated measured s-parameters were not available from the manufacturers in electronic form and specifications that produce a design with the desired performance.

From Table 3.7-1, since fundamental product characteristics are considered, all of them have similar to each other, MAX2680 is selected for this particular design because of the lowest price and easy of design and low conversion loss.

In order to achieve maximum performance, RF input port and IF output port matched with L matching network with manufacturer measured s parameter file. From Figure 3.7-1, RF input port of mixer is matched with a series inductor 8.2 nH and a parallel capacitor 1.5 pF by simulating real surface mount package of ADS software in order to degrade unpredictable effects. Thus, reflection coefficient of input port is 28 dB at desired frequency range in Figure 3.7-2.

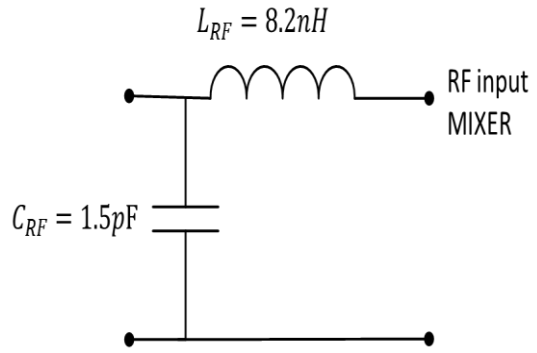


Figure 3.7-1 RF input matching network of mixer

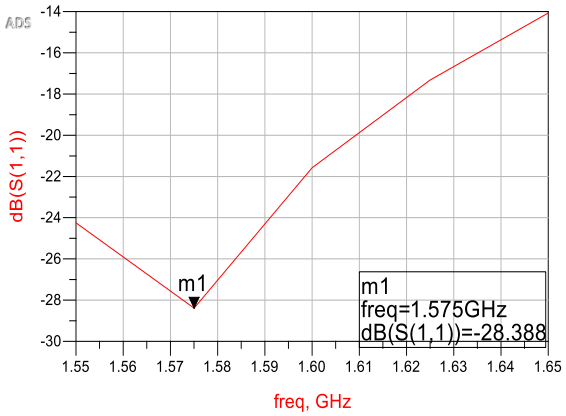


Figure 3.7-2 S11 value of RF input mixer

Besides, IF output port also matched with a parallel inductor 1.2 uH and a series capacitor 27 pF at 26 MHz in Figure 3.7-3. Reference to Figure 3.7-4, reflection coefficient of output port matched with 50 ohm is -24 dB at 26 MHz. Again, output port also matched with real component equal to compute design values more precisely.

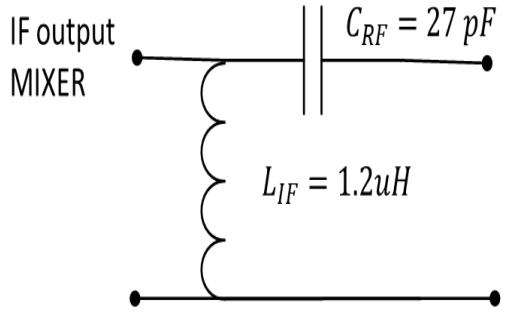


Figure 3.7-3 IF output matching network of mixer

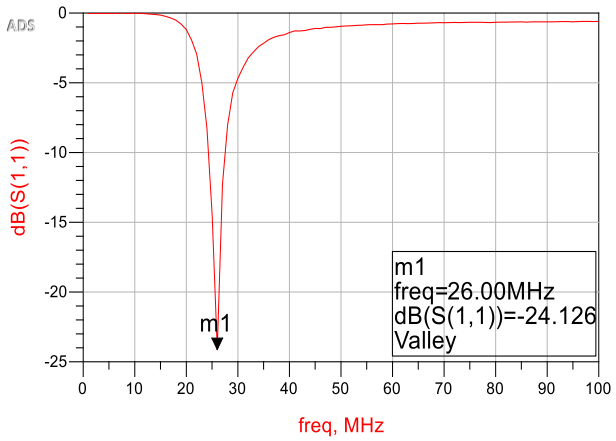


Figure 3.7-4 S11 value of IF output of mixer

3.8. IF Stage Design

IF stage provide amplification until analogue-to-digital converter. One of the main benefits of using differential amplifier is that they have high noise immunity when the signal is applied [60]. Common-mode rejection ratio (CMRR) is the ratio of response of normal-mode signal to response of common-mode signal of same amplitude and can be written in [60, 61] as follows

$$CMRR = \frac{A_d}{A_c} \tag{3-22}$$

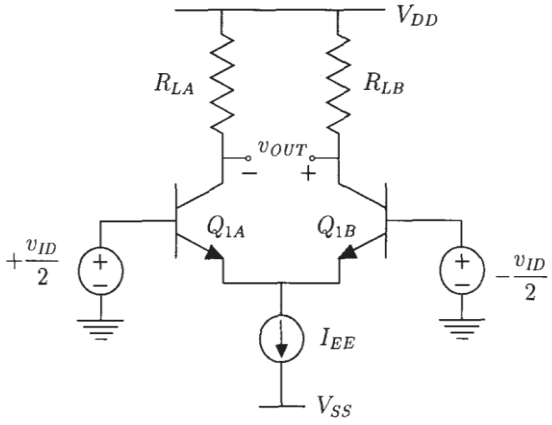


Figure 3.8-1 Bipolar differential amplifier [61]

The common mode ratio increases noise immunity of amplifier. Therefore, for small noise figure the common mode gain have to be low ,however, differential mode gain should be high

[60]. In order to calculate gain of IF stage, power level of system at mixer output must be calculated, as follows

Table 3.8-1 Gain and NF of LNA, SAW filter and mixer

	LNA	***SAW***	***Mixer***
Gain	*35.9 dB*	*-1.6 dB*	*-7.6 dB*
NF	*0.8 dB*	*1.6 dB*	*+7.6 dB*

The mixer resistively terminated with $50\ ohms$ and subsequent stages work higher impedance The IF stage has a gain at $66\ dB$ so comparator in input level at is $34.6\ mV$ with reference to Table 3.8-1. With LVDS adds $59\ dB$ of gain making a total of $125\ dB$ for the whole IF stage. Adding lots of gain at one frequency was risk so that PCB layout has to solid ground plane same length transmission line to provide stability. Several manufacturers produce high performance videos that are suitable for certain IF band. Frequency range, gain, common mode rejection ratio all considered active device selection process.

Table 3.8-2 Commercially available video amplifiers

	ON Semiconductor NE592 [62]	***Maxim MAX4313 [63]***	***Analog Devices 830ADS [64]***
Gain Bandwidth	*120 MHz*	*265 MHz*	*85MHz*
Open Loop Gain	*45 dB*	*59 dB*	*69 dB*
Common-Mode Rejection	*65 dB*	*73 dB*	*75 dB*
Price	*£0.665*	*£5.63*	*£ 7.36*

From Table 3.8-2, NE595, which is a monolithic, two stage, differential, output video amplifier is the best option compared the prices and it provides reasonable values in terms of others. Therefore, it is connected IF chain to generate 66 dB gain at intermediate frequency 26 MHz reference to Figure 3.8-2.

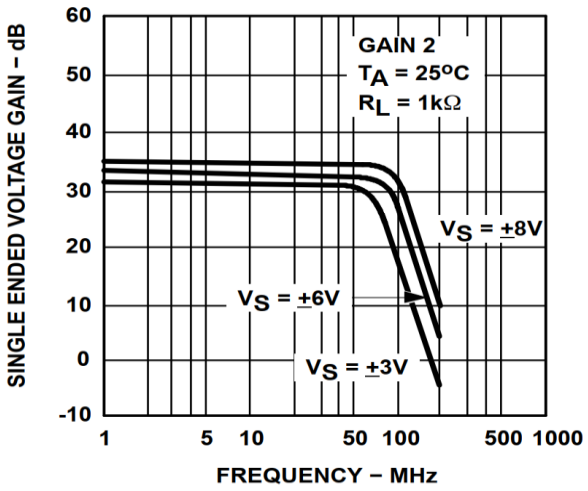


Figure 3.8-2 Video amplifier single ended voltage gain [62]

3.9. ADC stage

As we mentioned Chapter 1 Receiver section, IF chain must be sampled by ADC in order to produce in-phase and quadrature value. The digital side of receiver has a wide range of aspects, which allows a wider choice of option. These options consist of achieving lower noise figure with oversampling, or down conversion with method of under sampling.

3.9.1. Frequency Conversion using Under sampling

Sampling a signal with much lower than Nyquist rate is known as under sampling. The under sampling is a crucial approach as it effectively provide mixer function on the input signal when it is being sampled [65].At first, signal is converted to baseband, and then it is sampled same as baseband signal. The process can be written as follows:

$$f_{BB} = Rem(\frac{f_{IF}}{f_s}) \tag{3-23}$$

where f_{IF} is the intermediate input frequency to the ADC, f_s is sampling rate, and f_{BB} is the resulting baseband frequency. The rem function yields the remainder that results from dividing operands intermediate frequency by sampling frequency.

Table 3.9.1-1 Effect of under sampling on input [65]

Nyquist Zone of input signal	***Frequency Range of Zones***	***Spectrum Reversed***	***Frequency Translation***
First	$DC - f_s/2$	*No*	*None*
Second	$f_s/2 - f_s$	*Yes*	$f_s - f_{IF}$
Third	$f_s - 3\,f_s/2$	*No*	$f_{IF} - f_s$
Fourth	$3\,f_s/2 - 2f_s$	*Yes*	$2f_s - f_{IF}$
Fifth	$2f_s - 5\,f_s/2$	*No*	$f_{IF} - 2f_s$
Sixth	$5f_s/2 - 3\,f_s/2$	*Yes*	$3f_s/2 - 2f_{IF}$
Seventh	$3f_s/2 - 7\,f_s/2$	*No*	$2f_{IF}/2 - f_{IF}$

The remainder must be inside first Nyquist zone and if result does not accommodate this zone, then it must be subtracted from sample rate to produce accurate baseband frequency [65]. Spectrum reversal also be resulted from the process of aliasing, this is also considered when processing baseband signal according to look up table in Table 3.9.1-1

3.9.2. Achieving Processing Gain Using Oversampling

It is an important technique as it allows an improvement signal to noise ratio in digital domain and antialiasing filter is crucial for preventing SNR degradation. It is probable to design a receiver frequency plan with relatively wide IF filter which adequately suppresses images, however, it passes noise in the second Nyquist zone. This noise will be aliased into wanted band and will reduce the SNR by 3 dB. Besides, an efficient anti-aliasing filter can help to reduce this figure. The converter noise figure given by

$$N_C = 1.8 + 6.02N + 10\log\left(\frac{f_s}{2}\right) dBc/Hz \tag{3-24}$$

where N is the converter resolution. Therefore, if sampling rate is doubled, the converter noise power spectral density degraded by 3 dB.

The processing gain achieved by oversampling can be found from (30), and If a digital filter is performed to remove undesired noise around wanted signal.

$$G_{SNR} = 10\log\left(\frac{B_{IF}}{f_s}\right) dB \tag{3-25}$$

The signal-to-noise ratio of an ideal N-bit ADC is given in [65]by

$$SNR_{ideal} = 6.02N + 1.76 \tag{3-26}$$

The effective number of bits for converter is in [65],and calculated by

$$ENOB = \frac{SNR_{measured} - 1.76}{6.02} \tag{3-27}$$

Noise figure of ADC is given in [65] by

$$NF_{ADC,dB} = 10\log\left(\frac{V_{ADCrms}^2}{Z_{in}10^{-3}}\right) - SNR_{ADC} - 10\log\left(\frac{f_S}{2B}\right) - 10\log\left(\frac{kTB}{10^{-3}}\right) \tag{3-28}$$

where V_{ADCrms} is the rms value of the ADC input voltage range, f_S is the sampling frequency, Z_{in} is the converter input impedance, SNR_{ADC} is the signal to noise ratio of the converter, and is bandwidth, B.

With the intention of testability of our receiver with different conditions, a LVDS and an ADC is wanted to connect IF stage to compare results. Therefore, two components must be selected price, efficiency, availability. Several manufacturers produce high performance transistors that are suitable for IF frequency region and this particular design.

It can be seen from Table 3.9.2-1 that four different vendors have similar features. The TI LMH7220 provide a highest speed and low power comparator with an operating supply voltage range of 2.7 V to 12 V and at minimum price point (£ 4.71) and it was selected for this design. Similarly, A wide range of manufacturers yield high performance ADC that are suitable for IF

frequency region and this design. Frequency range, effective number of bits, and sampling rate all considered integrated circuit selection process.

Table 3.9.2-1 Commercially available LVDS

	TI LMH7220 [66]	***Maxim MAX903ESA [67]***	***Analog Devices ADCMP601BK [68]***	***Linear Technology LT1116 [69]***
Response time	*2.9 ns*	*8 ns*	*3.5 ns*	*10 ns*
Supply Voltage	*2.7 V to 12 V*	*5 V to 10 V*	*2.5 V to 5 V*	*4.6 V to 5.4 V*
Price	*£ 4.71*	*£ 8.71*	*£ 5.20*	*£ 6.10*

Because of the lowest price and expected supply voltage range and reasonable sampling frequency, which is three times higher than IF frequency, TI ADS831EG4 is optimum choice compared others for this particular design reference to Table 3.9.2-2. As we explained, IF stage is connected ADC stage, we have to add one extra stage NE592 buffer for 8-bit ADC because of difference between input range of 1-bit ADC and 8-bit ADC. Thus, 1V pk-pk input voltage is provided, thanks to IF stage amplifier has an adjustable gain with choice of resistor. We have processing gain approximately 11 dB processing gain. Besides, effective number of bits for 8-bit ADC is 7 bit and noise figure of ADC is approximately 51 for 1kohms and 2 V pk-pk voltage ADC.

Table 3.9.2-2 Commercially available 8-bit ADC

	TI ADC831[70]	***TI ADC08200 [71]***	***Analog Devices ADS9283BRSZ [72]***
Resolution (Bits)	*8*	*8*	*8*
Sampling Rate (Msps)	*80*	*200*	*100*
Supply Voltage	*4.75 V to 5.25 V*	*2.4 V to 3.6 V*	*2.7 V to 3.6 V*
Price	*£ 8.88*	*£ 14.43*	*£ 10.34*

Therefore, this system provides designer opportunity to compare results over- and under-sampling and effective number of bits. Therefore, one can also make a decision looking at these final results.

3.10. Phase-Lock Frequency Synthesizer

For frequency-tracking filter application, the phase-locked loop include a phase detector, a loop filter, and a voltage-controlled oscillator (VCO) respectively [24]. The loop is yielded to phased locked when the VCO frequency f_o is equal to the loop input signal frequency f_i, and only a phase difference between the VCO and input signal exists[24]. Without an input signal the VCO is free-running at frequency f_R [24]. A system enters an acquisition mode when a signal arrives. The tracking mode occurs when $f_i = f_o$, the range of frequencies over which the VCO will track the input [24]. The range of frequencies over which the VCO will track the input signal is called *hold-in range* is determined by the PLL loop and linearity [24].

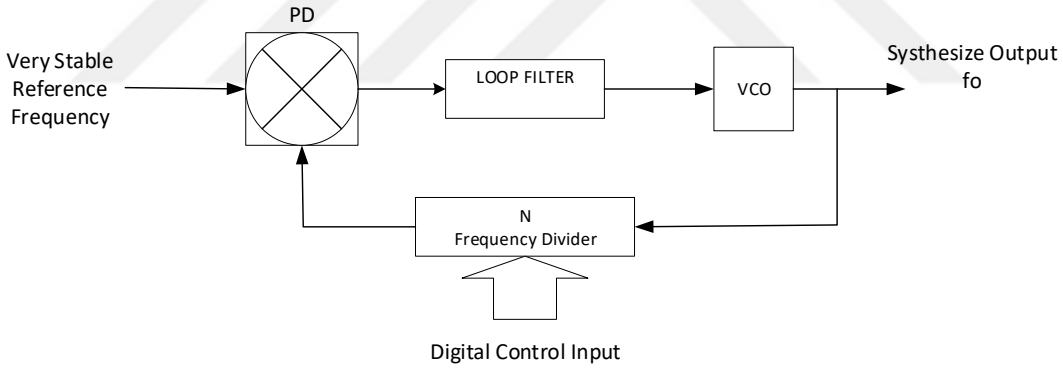


Figure 3.10-1 Phase-Locked frequency synthesiser[24]

The reference to Figure 3.10-1 Phase-Locked frequency synthesiser is used to lock the output of a VCO to a more stable crystal oscillator. The loop maintains two frequencies of the phase detector are the same[24]. The output frequency can be changed by making the frequency divider programmable[24]. The digitally programmable frequency-divider output, f_o/N, is adjusted by the value of N selected by designer and compared to the reference signal detector in phase detector (PD) and then when the loop is locked for a specific value of N, the $f_o/N =$

f_{ref} by definition of phase locked, therefore, synthesizer output is $f_o/N = f_{ref}$ [24]. At fractional-N PLL, division ratio dynamically changer between N and $N + 1$ [24].

Several manufacturers produce high performance PLL that are suitable for L1 frequency region. Frequency range, input clock frequency, jitter and phase detector frequency all considered active device selection process. Many devices were quickly eliminated because of very expensive price range, availability and specifications that produce a design with the desired performance. The LMX281 is a low noise wide band synthesizer that integrates a delta-sigma fractional PLL at £ 9.8 price, which is half of the other manufacturer products [73]. All registers can be programmed through serial peripheral interface SPI interface with available read back interface. It has also two differential output which is required for twin antenna design.

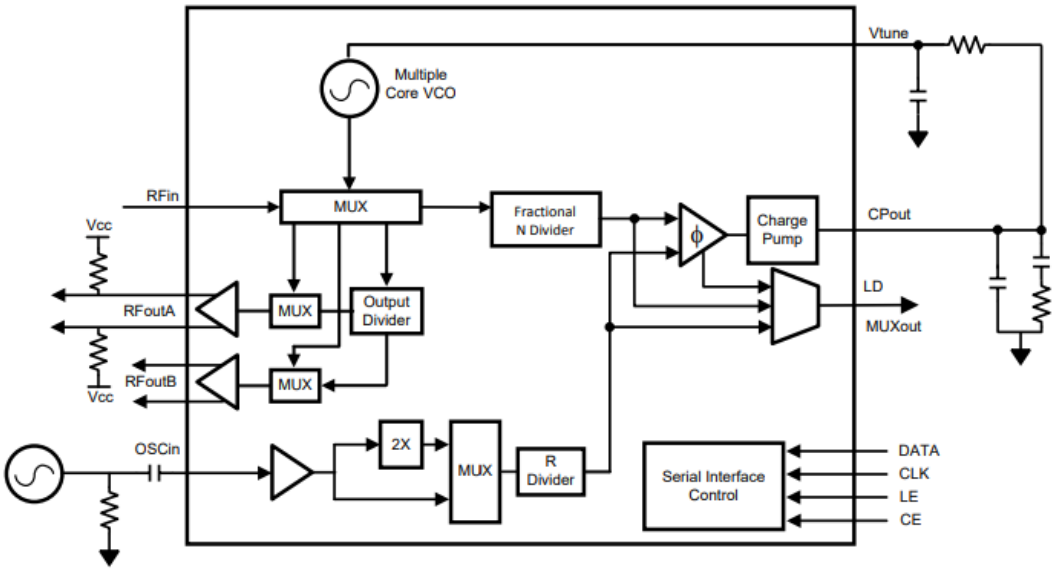


Figure 3.10-2 Simplified schematic of PLL [73]

Figure 3.10-2 shows that the LMX2581 is a synthesizer, phase detector and charge pump, including a reference input and R divider, and two programmable output buffers, and VCO and high frequency (N) divider [73]. According to datasheet LMX2581, output frequency can be calculated as follows:

$$f_{OUT} = f_{OSC} \times PLL_R \times (PLL_N + \frac{PLL_{NUM}}{PLL_{DEN}})/VCO_{DIV} \quad (3\text{-}29)$$

where f_{OSC} is oscillator frequency, PLL_R is R divider value, PLL_N is N divider value, PLL_{NUM} is fractional numerator, PLL_{DEN} fractional denominator, VCO_{DIV} divider value. PLL has 15 registers, which are 32bit interface, to adjusting output frequency. In addition, Texas Instrument uses their graphical user interface and code loader applications to transfer registers bits from PC to PLL. PLL signal generation interface and associated value of registers are given appendix A.1 and appendix A.2.

3.11. Surface Mount Antenna

Although GPS signals are right hand circularly polarised signal (RHCP), signal may change to and left hand circularly polarized (LHCP) in dense multipath environments [74]. This cause a weak signal from environment cause to lose acquisition lock. Dual polarized antennas overcome this problem with suitable algorithm. The several manufacturers produce high performance antennas that are suitable for L1 frequency region and this particular design. Operation frequency, return loss, maximum gain and gain at zenith all considered device selection process. Many devices were quickly eliminated parameters were not available from the particular manufacturers in electronic form and specifications that produce a design with the desired performance. Taoglas SGGP.25.2 was selected because of $70\,\%$ efficiency at reasonable price range, which is approximately 4 pounds. The return loss is lower than $-10\ dB$ and gain approximately $3.5\ dB$ reference to Figure 3.11-1 and Figure 3.11-2.

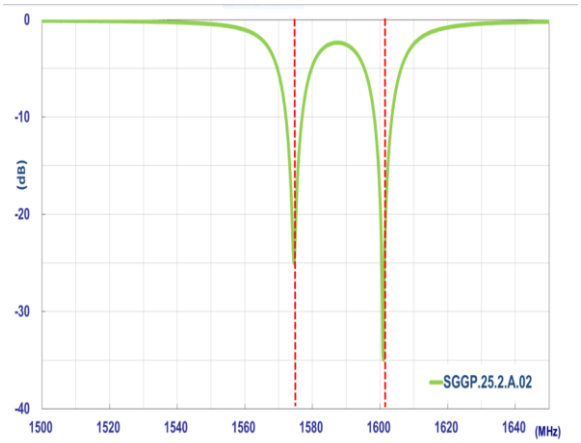


Figure 3.11-1 Return loss SMT antenna [75]

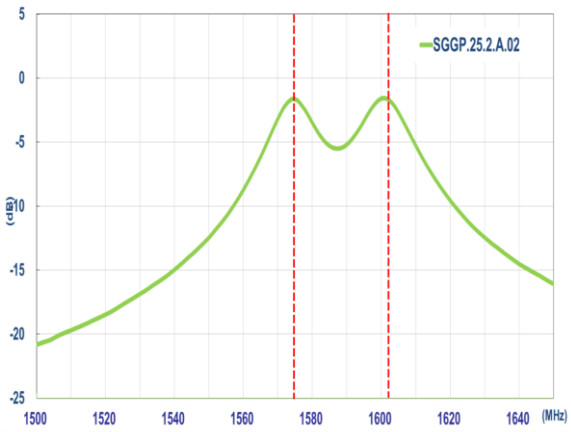


Figure 3.11-2 Gain SMT antenna [75]

Although SMT pack antenna is selected the upper L frequency, we did not add printed circuit board purposely because we wanted to test with oscilloscope and other testing equipment with different condition. Therefore, SMA connector accommodated instead of SMT antenna place. The measurement also made with using patch antenna that suitable for this region.

4. PCB LAYOUT ISSUES

4.1. Decoupling Capacitor

Most active devices suffer performance degradation o if there is ripple and noise power supply pins. These networks yield a low impedance path to ground for noise incident on supply voltage, and it is local energy storage close to the device being decoupled. Therefore, without causing voltage rail, high frequency current is supplied. Low frequency noise needs larger electrolytic capacitor which have ability to charge store and supply. However, high frequency power supply noise is degraded by low inductance surface mount ceramic capacitor capacitance connected directly power supply the active elements [76].

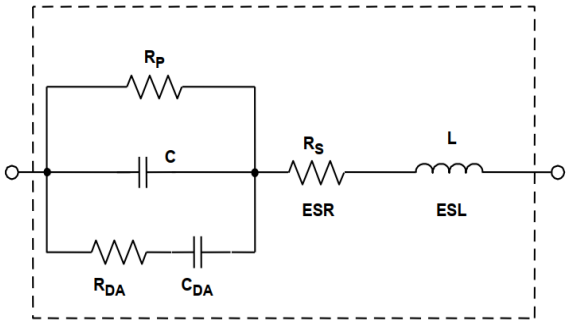


Figure 4.1-1 A real capacitor equivalent circuit include transmission line [76]

Figure 4.1-1 illustrates a model of non-ideal capacitor that the nominal capacitance C, leakage resistance Rp , equivalent series resistance Rs, equivalent inductance L, R_{DA} and C_{DA} are the dielectric absorption. Dielectric absorption is not significant importance decoupling.

Therefore, it works as a resistance much smaller frequency, whereas at higher frequency, it has an inductive behaviour. The self-resonant frequency of capacitor is the frequency that the reactance of capacitor is equal to the reactance of the ESL. Therefore, self-resonant frequency can be written as

$$f_{res} = \frac{1}{2\pi\sqrt{ESL.C}} \tag{4-1}$$

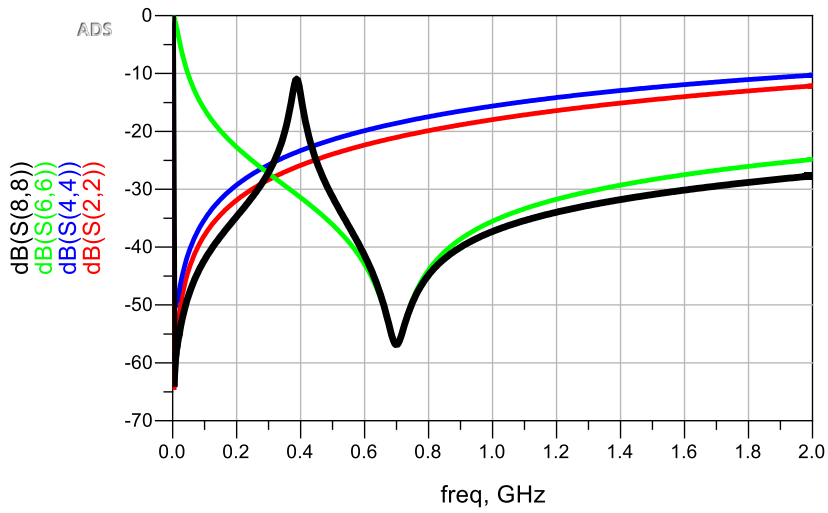


Figure 4.1-2 Self-Resonance frequency of various $10\ uF, 100\ nF$ *and* $100\ pF$ *capacitors at PLL part of PCB*

Figure 4.1-2 shows decoupling capacitors that are $10\ uF$ red line, $100\ nF$ blue line and $100\ pF$ is green line, and black line is parallel connections of these. These shows that low impedance level over wide frequency band. The higher value capacitance shows inductive behaviour so that the smaller value of capacitor has lower ESL and continue to behave as a capacitor at higher frequencies. Thus, the parallel connection of these capacitor extends frequency range. Target impedance can be written as the highest transient current, value of voltage supply be decoupled and the allowable ripple of voltage, as follows:

$$Z_{target} = V \times \frac{\max(V_{ripple})}{I_{trans}} \tag{4-2}$$

All decoupling capacitors must be connected to directly low impedance ground plane to work effectively. Short traces and vias are needed for decoupling connection in order to degrade series inductance [76]. The ferrite bead at PCB add extra high frequency noise isolation and decoupling [77]. When PCB designing stage, the high frequency decoupling capacitor must be as close the active device as possible because trace inductance that have a negative impact on effectiveness decoupling.

When PCB designed, the lowest value capacitor placed as closed as possible to active device in order to degrade inductance capacitance of trace. Decoupling capacitance generally connected ground plane with two or three vias to obtain low-impedance connection to ground. According to Figure 4.1-2, we use 100 pF closed LNA power supply possible and placed 100 nF and 10 uF closed possible power supply pin of circuit to provide board level decoupling. In order to filter power supply high frequency noise, which is result from linear voltage regulator and power plane, inductor connected next to capacitor. We add high frequency filter, which has constructed with series 27nH inductor to parallel 100 pf capacitor with additional 10 ohms resistor, in order to increase selectivity of our filter.

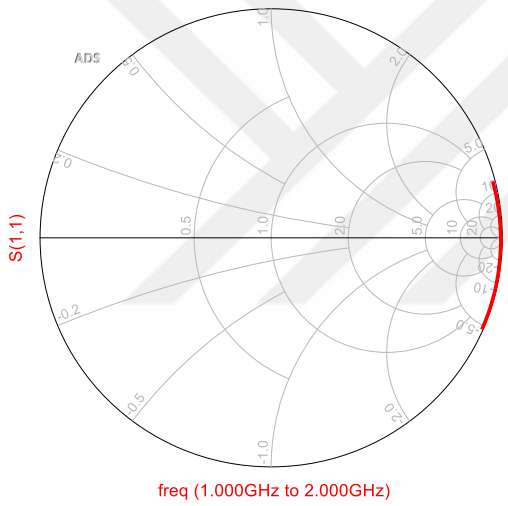


Figure 4.1-3 S11 of decoupling from 1 GHz to 2 GHz

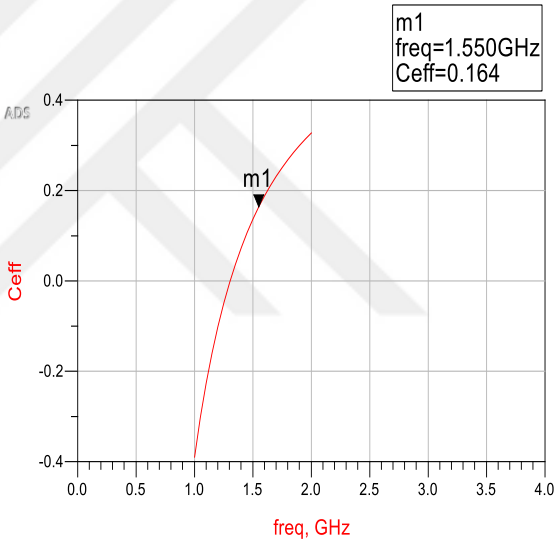


Figure 4.1-4 Capacitive effective decoupling LC filter

Reference to Figure 4.1-3, S_{11}value of is outside smith chart so that high frequency noise does not affect overall system and it has small value of capacitance as we expected at Figure 4.1-4. Thus, this design provides band reject filtering at high frequency and low frequency noise. From Figure 4.1-5, priority of component placement should be given to termination resistor and discrete filtering capacitor, medium value and high frequency filtering capacitor over decoupling capacitors close tor to the device.

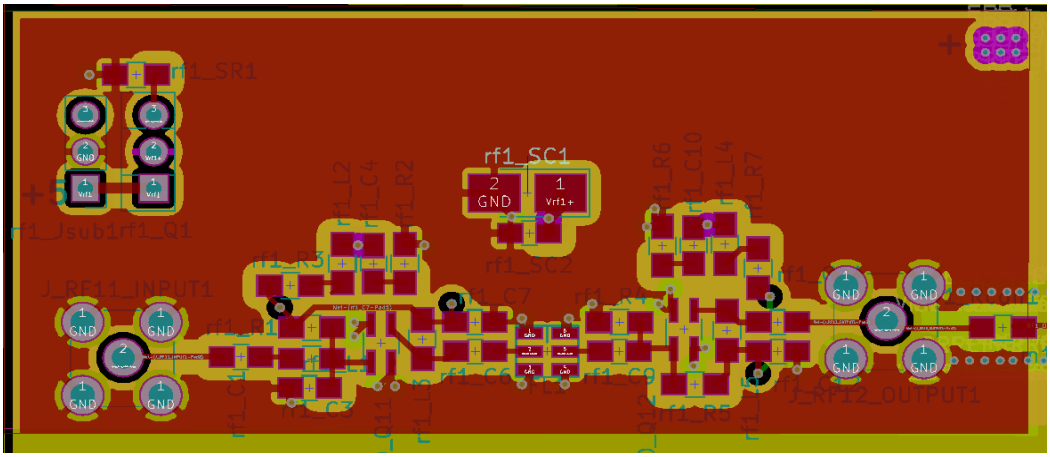


Figure 4.1-5 PCB layout of LNA stage

4.2. PCB Components: Microstrip and Strip line

50 ohms is the best trade-off between power handling and low loss [78]. For coaxial cable provide best power handling and 75 ohms lowest lost. Therefore, the selection of $50\ ohms$ can considered the best compromise between signal loss per unit length and power handling capability.

The PCB consist of layers of metal and insulator and can include several layers that the length of trace, x, the width of trace, w, height of traces, h, thickness of traces, and PCB permittivity. A signal trace placed on an outside layer of the PCB with reference plane below it, constitute a micro strip line at Figure 4.2-1.

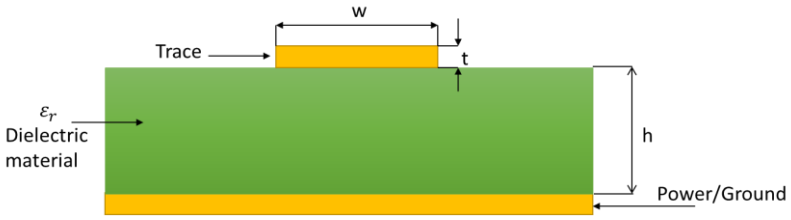


Figure 4.2-1 Microstrip transmission line [76, 77]

According to [76], the characteristic impedance,

$$Z_0(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \log\left(\frac{5.98h}{0.8w + t}\right) \tag{4-3}$$

where line thickness, t, trace width, w, height above the ground, h, and relative substrate permittivity of substrate, ε_r, and microstrip transmission line,

$$T_{PD} = 85\sqrt{0.475\varepsilon_r + 0.67}.s \quad (4\text{-}4)$$

where length of trace, s and these formulas is used when $0.1 < w/h < 0.2$ and also when $1 < \varepsilon_r < 1.5$. Similarly, the strip line trace route on an inside layer of the PCB with two-low voltage reference plane constitutes a strip line layout.

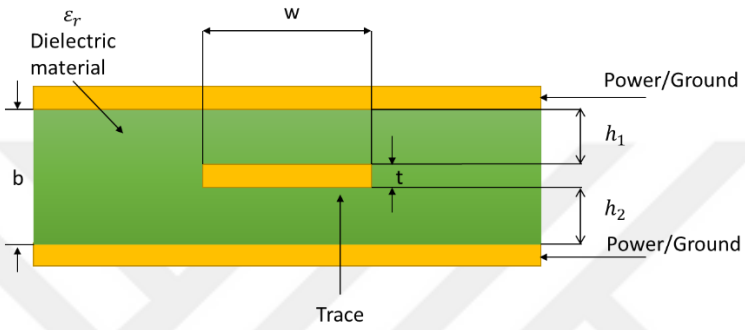


Figure 4.2-2 Strip line transmission line [76]

Reference to [76], the characteristic impedance can be calculated as follows

$$Z_0(\Omega) = \frac{60}{\sqrt{\varepsilon_r}}\log\left(\frac{1.9b}{(t + 0.8w)}\right) \quad (4\text{-}5)$$

where trace height above lower plane, h_2, trace headroom below upper plane, h_1, separation between ground planes, b, trace width, w, trace thickness, t, trace length, s, and the strip line layout propagation delay

$$T_{PD} = 85.\sqrt{\varepsilon_r}.s \quad (4\text{-}6)$$

These formulas are applicable when $w/b < 0.35$ and also when $t/b < 0.25$.

When circuit designing stage on CAD, although a microstrip line impedance $50\ \Omega$ for $0.35\ mm$ with ε_r which is 4.5, controlled impedance value of PCB train manufacturer is used. According to this manufacturer, a top layer microstrip of $0.40\ mm$ width will have an impedance of $50\ ohms$ with respect to a solid ground plane at second layer and second layer microstrip of

$1.64\ mm$ width will have an impedance of $50\ ohms$ with respect to a solid ground plane on third layer [79].

4.3. Vias

Using via at signal traces cause problems because $0.4mm$ via with $1.6mm$ thick FR-4 PCB has inductance, $1.2nH$ and a $1.6\ mm$ clearance hole around $0.8\ mm$ pad has capacitance, $0.4\ pF$, with a material permittivity, 4.5. Therefore, when design stage, one should not use signal traces and also if one design differential pair signal, via must be used both of traces to reduce cross talk and degrade phase differences. IF stage differential pair use vias both trace and trace length hold as same as possible.

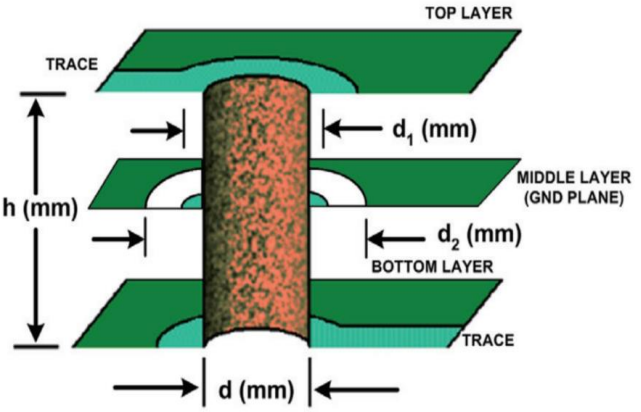


Figure 4.3-1 Interconnect traces on different layers [77]

The via inductance can be written as follows

$$L(nH) \approx 5.08h\left[1 + \ln(\frac{4h}{d})\right] \tag{4-7}$$

and capacitance can be described as follows

$$C(pF) \approx \frac{1.41\varepsilon_r h d_1}{d_2 - d_1} \tag{4-8}$$

where the diameter of clearance hole in ground planes (in.), d_2, diameter of pad surrounding via (in.), d_1, thickness of PCB (in.), h, and parasitic via inductance $(nH), L$, and capacitance $(pF), C$. Characteristic impedance is

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}} \tag{4-9}$$

4.4. Copper Planes

Reference to Figure 4.4-1, copper planes creates stray capacitance on signal traces and it can be written as follows

$$C(pF) \approx \frac{0.0886\varepsilon_r A}{h} \tag{4-10}$$

where h separation between planes (cm), area of common planes (cm^2), A, and ε_r is permittivity. Therefore, 1.6 mm thick PCB (FR-4) has 0.25 pF/cm^2. This capacitance can be degraded by reasonable number of vias. A solid ground plane act as a heat sink and degrades thermal levels of all circuit elements. However, this can cause problem for thermal sensitive component because of heat spreading. This approach is used thermal oscillator ground copper pour cleaned and it reduces electromagnetic interference at the same time. We use solid ground place in our circuit and cut out ground below oscillator that is thermal sensitive component.

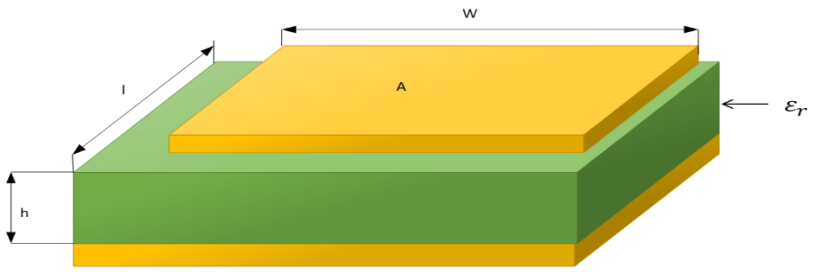


Figure 4.4-1 Copper planes of PCB [76]

4.5. Signal Integrity

The clock traces must be as straight as possible and have not vias, which cause impedance change and reflection [76]. The ground plane also used next to top signal layer to minimize noise [76]. In order to reduce reflection noise, place the differential traces $s \geq 3h$ and $s < w$ and must be kept the space between microstrip lines s constant over entire constant over the entire trace length [76]. According PCB Train separation between layer, h is equal to 0.22 mm

and then d is adjusted to 1.1 mm. Differential RF output of PLL's microstrip line placed 30 degrees angular separation between each other and same length to reduce crosstalk with covering minimum area on PCB. Similarly, IF stage microstrip differential input and output transmission lines had length that are closes as possible to reduce crosstalk, signal integrity and phase differences. In order to improve isolation and cross talk, vias placed around high frequency transmission lines, such as oscillator input and differential output of PLL.

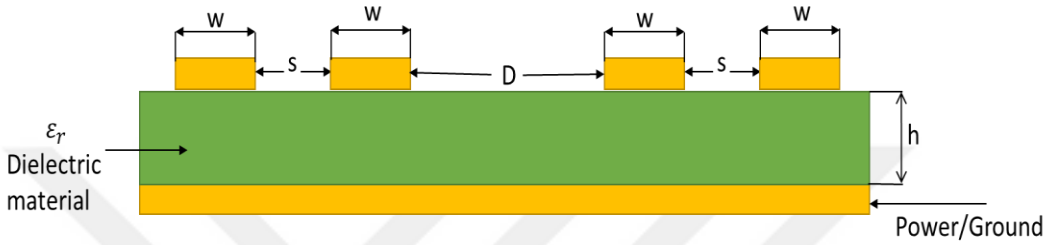


Figure 4.5-1 Separating traces for signal integrity[76]

4.6. Power Distribution

Power planes covers all PCB area and has very low DC resistance. The power planes supply voltage equally for all devices while providing, noise protection, heat current-sink capability, and shielding for the logic signals on the PCB[76]. With the intention of testing our circuit without possibility short circuit effect, we provide separate power planes and same ground plane. On ground plane layer, we keep out copper pour second plane oscillator input source and provide connection through top layer with ferrite bead so that this is reduce coupling effect of oscillator input at Figure 4.6-2. Similarly, we cut out power plane below the oscillator input to decrease any coupling effect input frequency. In this way, we provide to separate supply voltage way one of them for analogue parts and digital parts reference to Figure 4.6-1 .

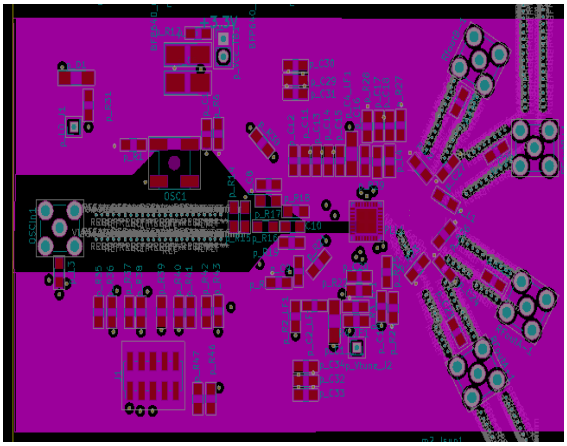


Figure 4.6-1 Power supply plane of receiver

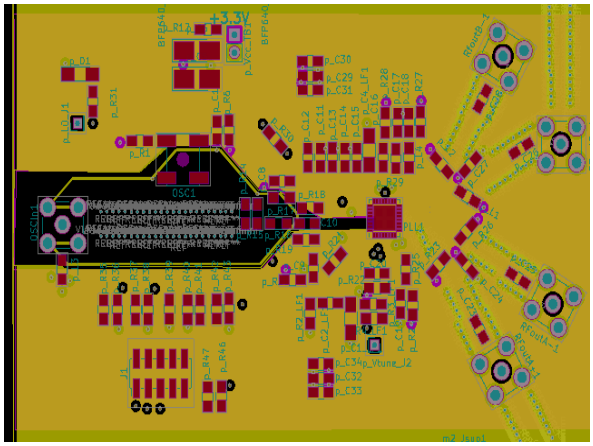


Figure 4.6-2 Ground plane of receiver

We also add PNP BD140 transistor connection at supply voltage pin to provide polarity protection because of consuming less power compared to diodes. Emitter pin is connected power supply and collector is connected to board so that when voltage is positive is open and it is closed when negative voltage is supplied. LVDS and 8-bit ADC need differential input signal to test for different input power. The balun, which provides isolation and works up to 200 MHz, was also added because of testability for our circuit. Vias also added PCB power planes to ease of test connection between separate voltages plane for each stage.

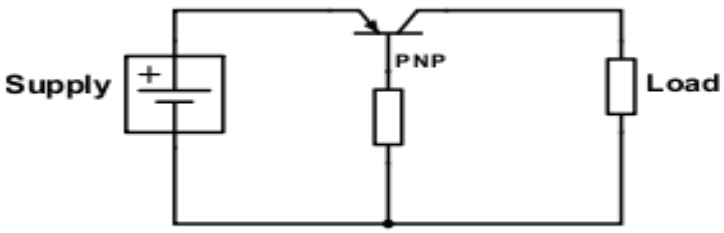


Figure 4.6-3 Reverse polarity protection with PNP transistor

5. EXPERIMENTAL RESULTS AND DISCUSSION

5.1. LNA Stage Experimental Results

Constructed PCB of front-end is shown in Figure 5.1-1 and schematic of RF stage is given appendix A.3 at page 84. The PCB have tested with Antritsu MG3681A signal generator and Antritsu MS8609A digital mobile radio transmitter. The test circuit has been connected with coaxial cables, which have approximately 1 dB insertion loss in total. Since front-end has been designed with separated stages, each stage has input and output testing connector. Firstly, RF1 stage have not provided gain since rf L3 inductor soldering pad had been lost so that inductor does not connector and transistor collector pin has not following current to emitter to amplify. In order to test different reflections, RF2 stage tested with 1 pF matching capacitor instead of 1.5 pF. Figure 5.1-2 demonstrates that gain of amplifiers increases gradually with respect to current and Figure 5.1-3 reveals that gain of amplifiers increases gradually with respect to supply voltages.

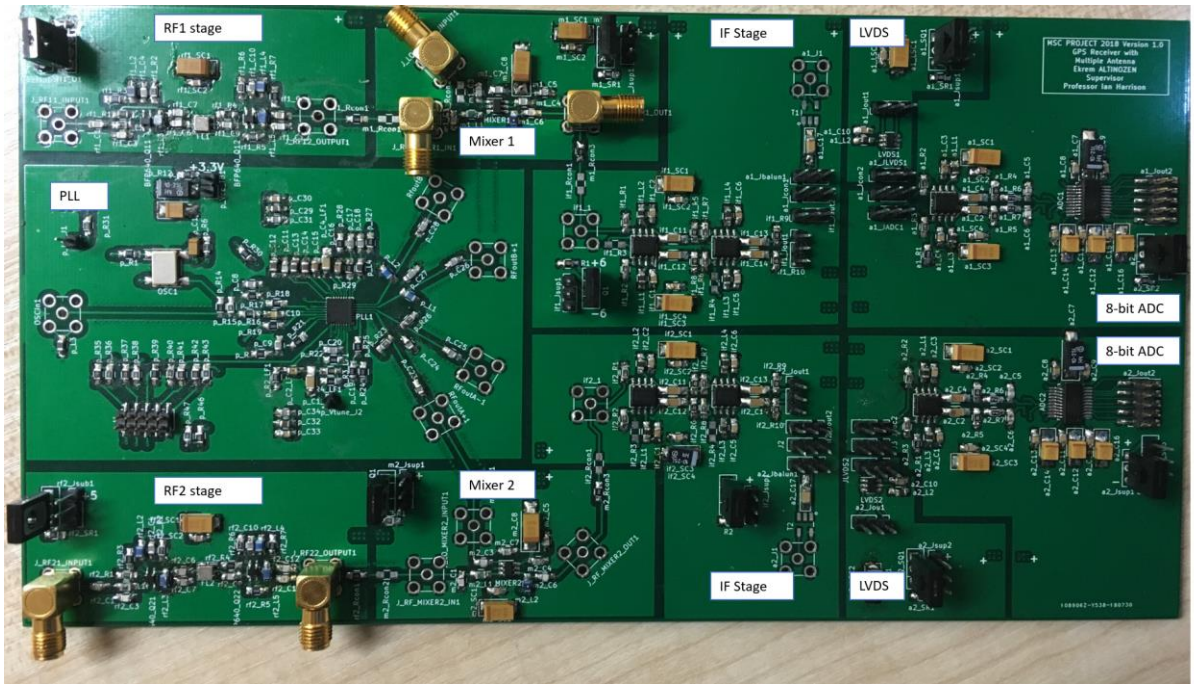


Figure 5.1-1 Constructed PCB of front-end

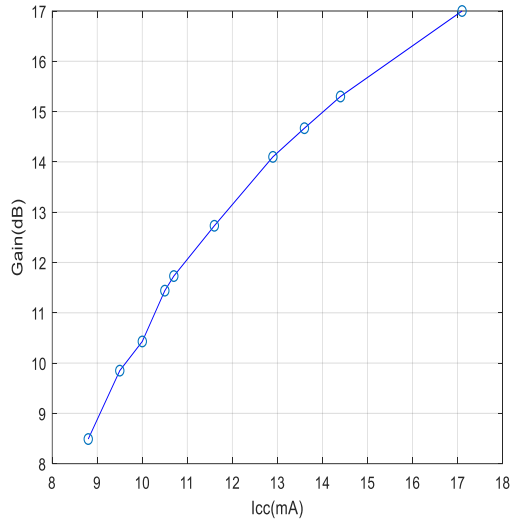


Figure 5.1-2 Gain versus Icc of RF2 with 1 pF matching

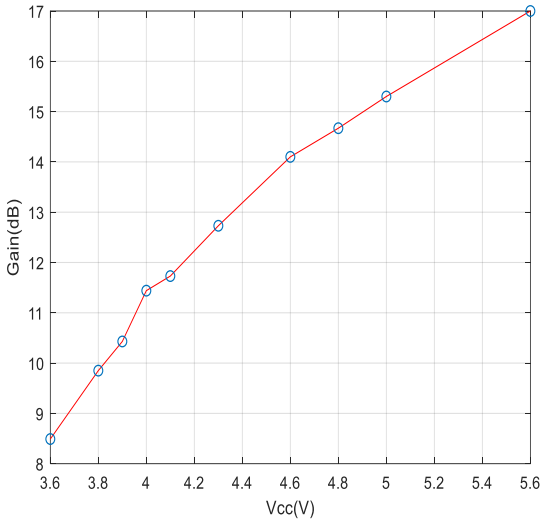


Figure 5.1-3 Gain versus Vcc of RF2 with matched 1pF

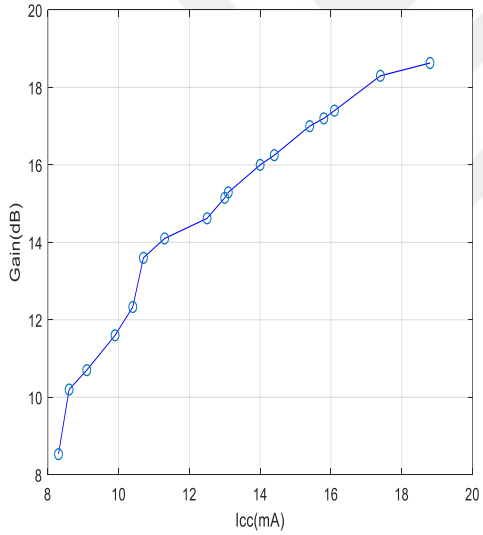


Figure 5.1-4 Gain versus Icc of RF2 with 1.2 pF matching

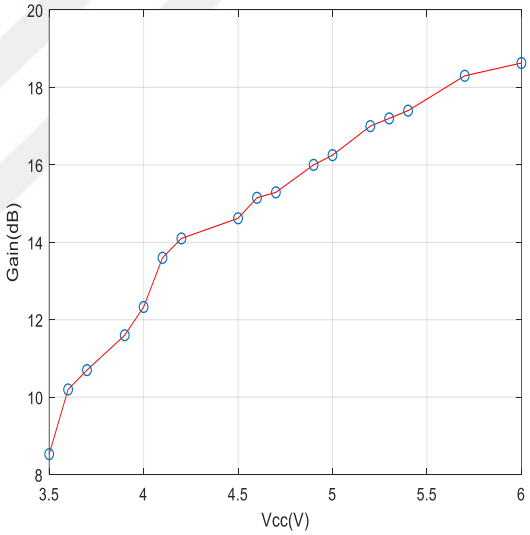


Figure 5.1-5 Gain versus Vcc of RF2 with matched 1.2 pF

Gain of the LNA stage matched with 1.2 pF capacitor versus supply current and voltage is given at Figure 5.1-4 and Figure 5.1-5, respectively. Thus, the circuit provides 2 dB more gain than ones matched with 1 pF at operating region. Gain of LNA with 1.5 pF capacitor versus Icc and Vcc is given Figure 5.1-6 and Figure 5.1-7, respectively. This reveals that gain of LNA with matched 1.5 pF has around 2 dB and 4 dB more gain than ones matched with 1.2 pF and 1 pF.

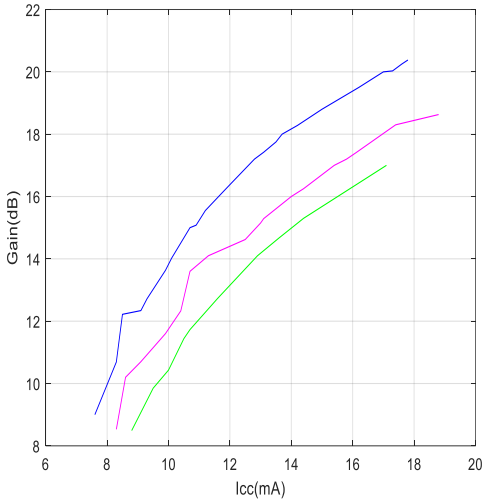


Figure 5.1-6 Gain versus Icc of RF2 matched with 1.5 pF

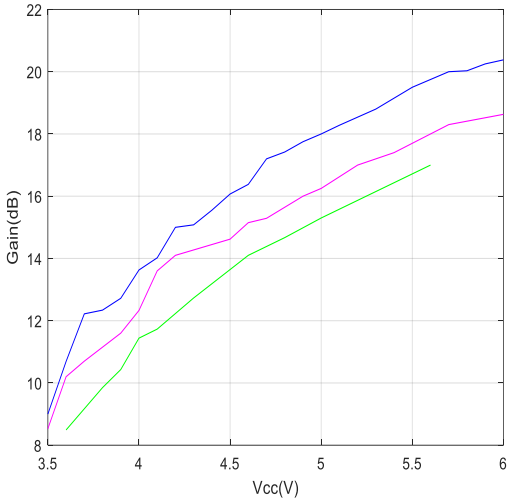


Figure 5.1-7 Gain versus Vcc of RF2 matched with 1.5 pF

Figure 5.1-8 demonstrates the output frequency spectrum of LNA2 matched with 1.5 pF with supply 5 V and 13.7 mA respectively and -40 dBm input source has provided -22.94 dBm output with coaxial cable loss both input and output connection, and amplifier 18 dB gain. Besides, frequency versus gain of RF2 is given in Figure 5.1-9. A more detailed looked graph reveals SAW filter has suppressed undesired frequency sharply as we expected and simulated bandwidth.

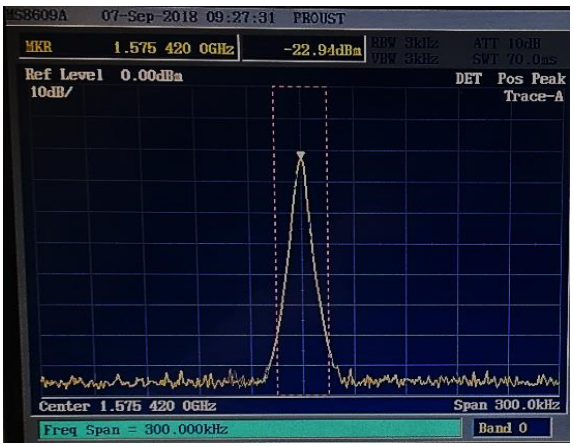


Figure 5.1-8 Frequency spectrum RF2 output

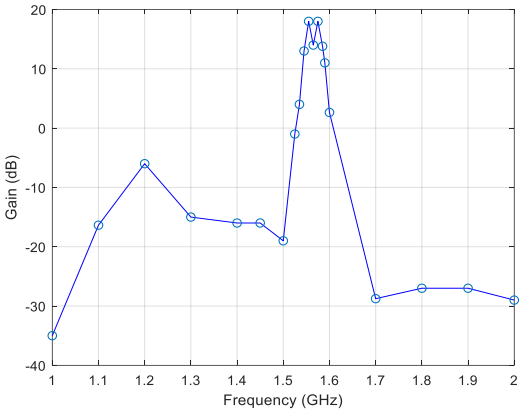


Figure 5.1-9 Gain versus frequency of RF2 stage at 5V and 13 mA

5.2. Mixer Stage Measurements

illustrates that first mixer down-converted from 1.575 42 GHz with $-25\ dBm$ gain to 26 MHz with -21.79 dBm by using local oscillator signal $-5\ dBm$ with Agilent E4421B signal generator. Therefore, mixer provides 3.2 dB insertion loss.

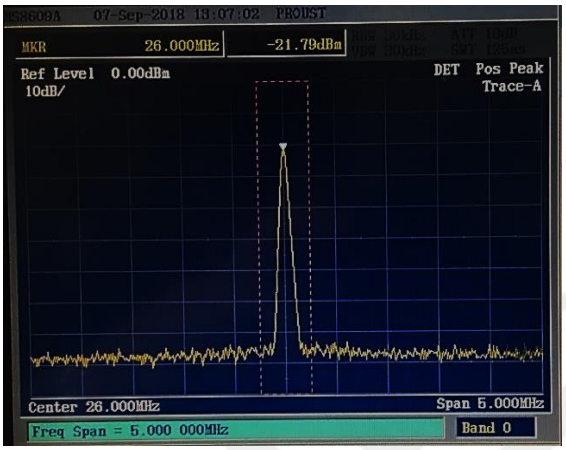


Figure 5.2-1 Frequency spectrum of first mixer output

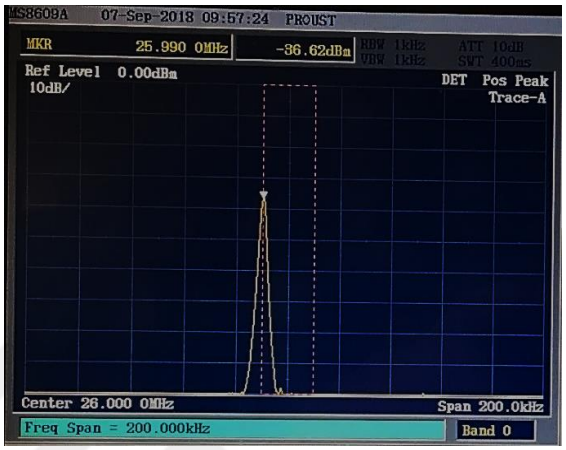


Figure 5.2-2 Frequency spectrum of second mixer output

Figure 5.2-2 illustrates that second mixer down-converted signal from 1.575 42 GHz with $-40\ dBm$ gain to $26\ MHz$ with $-36.62\ dBm$ by using local oscillator signal 1.549 42 GHz with $-5\ dBm$ with Agilent E4421B signal generator. Therefore, mixer provides 3.38 dB insertion loss.

5.3. IF Stage Measurements

Since we have not 26 MHz frequency generator with microvolt input voltage range and wideband oscilloscope, the output signal measurement of if stage with Gw instek GDS-1022, which has maximum frequency 25 MHz and input signal provided by Gw instek SFG-2104 synthesized function generator that produces 2 MHz maximum output source. Since IF stage has differential output, measurement made by connected one output signal and two output signals, respectively. Figure 5.3-1 reveals that channel 1 of oscilloscope is connected to the source and channel 2 is connected two the output. In addition, Figure 5.3-2 shows that IF stage

output differential connection with source (channel 1) and output (channel 2, which its ground connected to the second output). Moreover, it has amplified from signal 232 mV peak-to-peak to 6.24 V peak-to-peak.

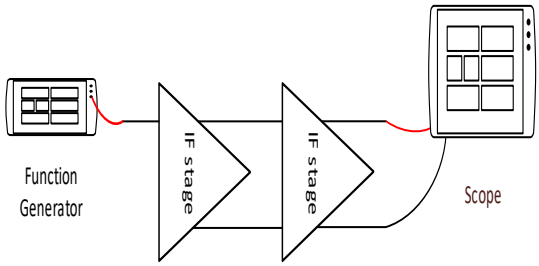


Figure 5.3-1 IF stage connected with input source (channel 1) and output (channel 2)

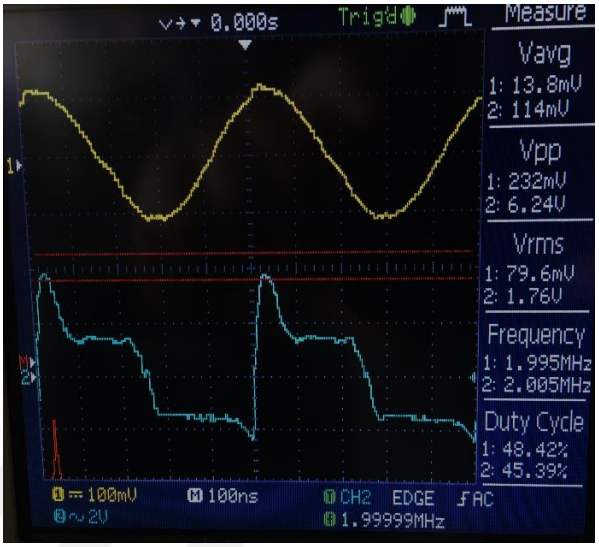


Figure 5.3-2 IF stage output differential connection with source (channel 1) and output (channel 2)

5.4. 1-bit ADC Measurements

Since baluns have not arrived in order convert single ended to differential ended at testing period, LVDSs have been tested 2 MHz sinusoidal input signal. Comparator provides high level if sinusoidal signal bigger than zero, else it provides low level square wave as we expected.

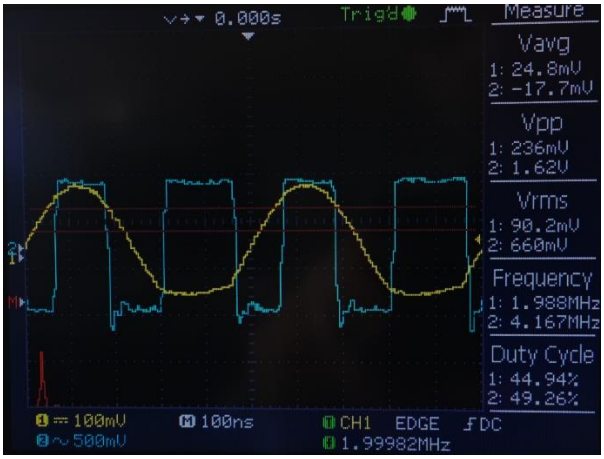


Figure 5.4-1 LVDS's input (channel 2) and output (channel 1)

PLL and 8-bit ADC have not been tested because they have special universal serial bus dongle, which have 10 pin connection and three wire SPI configurations. Due to the straight time constraint of project, it has not been ordered and the time limitation is not enough to write SPI and 8-bit ADC control software which is directly controlled PC with man-machine interface.

5.5. Discussion

Since RF front-end circuit designed with small package size passive discrete circuit components, there is requirement for two weeks advanced soldering training. Without this training, it is highly probable making soldering mistakes with surface mount component. Therefore, RF1 stages' 5.6 nH inductor pads lost so that circuit provides no gain only filter provide some insertion loss. Even if RF stage provides 36.5 dB gain, we have measured 18 dB gain from RF2 at operating condition. This error may well result from soldering error as well. In order to overcome misalignment error, hot air soldering has used to remove component, and because of limited number of components, removed components have placed same place without misalignment. This may also result in this measurement error. In addition, due to collector biasing, circuit may not provide thermal stability. We measured each amplifier collector to emitter voltage, which has 2.87 V and 2.99 V of LNA and gain, respectively, and if we arrange Vce of LNA at 3 V, Vce of gain stage is 3.30V. This also degraded performance

of RF stage of amplifier we have also approximately 5 percent measurement error because of multi-meter and voltage supply. The RF could be constructed again to understand in essence of this problem, but straight time constraint of project cannot allow this condition.

The mixer provides better performance than datasheet by optimizing input and output matching circuit, which is $3.2\,dB$ insertion loss. Since we are working at intermediate frequency stage at $26\,MHz$, function generator and oscilloscope are not capable of precise measurement due to maximum output, input frequency and maximum input voltage value rate, respectively. Due to video amplifier circuit model does not digitally available, IF chain is connected differentially and it provides testing voltage range $28\,dB$ gain. The results show that additional stage can be added, or balun should be used additional gain for IF stage. if low-Q parallel tuning circuit placed between differential output of each amplifier with the $-3dB$ bandwidth around $2.4\,MHz$, this circuit provides expected gain at given frequency region. Therefore, system provides expected gain at operating frequency region with additional band pass filtering.

Because of differential output signal is not available, baluns have been placed, however, these orders have not arrived planned time due to supplier stocks problems. Thus, circuit has been tested with $2\,MHz$ single sinusoidal voltage with connected other input to ground, and result reveals that it increases frequency of input two times and it has also yielded $16.73\,dB$ voltage gain. The overall constructed PCB costs £340, which components and PCB cost £150 and £190, respectively. Because of prototype extra header, bigger component size, and connectors are used, we can decrease to size half of PCB. Thus, we provide manufacturer opportunity with cost decline, and due to large number of productions, it is also cost less. However, manufacturer have to add patent price because it has already patented technology, which is explained at introduction section.

5.6. Time Management and Progress of Thesis

The detailed figure of project Gantt chart is given at appendix A.4 page 85. The project research and literature review have been finished at expected deadline. Besides, even if hardware design process pointed 4th June, we could start to design schematic because of exam schedule and meeting arrangements. Therefore, schematic design accomplished a few days later. Since complexity and four layers high frequency designed technique was used, PCB layout and hardware debugging via computer aided design tool achieved at 3 days later than organised time period. After that, PCB and component had ordered at 20th and 24th July, respectively. Order of PCB had been arrived at 15th of August and most of the discrete component arrived 1st September, which is approximately one month later after being ordered because of supplier stocks problems.

Even if we had a printed circuit board, we could not start to construct testing circuit, since surface mounts arrived two weeks later. These order and shipment time delay have not been forecasted and planned so that this have impacted testing milestones strongly. Due to these delays, thesis writing stages placed instead of testing process. When most of orders have arrived, we tried to narrow two weeks of PCB fabrication time to one week, however, these could not be possible because discrete and digital circuit elements were surface mount and small package sizes. Thus, these types of soldering needed special two weeks soldering training and this had also affected the production time of testable circuit. Hence, we learned that we have to calculate every stage and create optional and flexible time planning. For example, we can create for two bills of materials files for two different manufactures in case we will have problems about stocks issues and shipment time. It was also understood that every project starts slow progress and then it was increased sharply, however, the final period of project process raises gradually. We must add different risk and compromise point of the project into the time

plans. Probability of error must be calculated so that precise time plan and flexible progress options could be created.

6. CONCLUSION

The main objective of this project was to investigate and to propose an architecture which is capable to receive GPS signal upper L frequency with multiple antenna and low-cost. For this, RF stage is designed with two LNA. In this stage, the first LNA for designed was to optimized low noise figure reasonable gain, whereas second LNA designed to high gain with BFP640 transistor. the SAW filter between two LNA provided additional filtering of signal with fixed centred frequency and narrow bandwidth. Thus, RF stage provides simulated 37.5 dB gain and its noise figure (0.8 dB) has been optimised by appropriate matching and biasing. For down-conversion, double balanced MAX2680 is selected because of low cost and the ease of fabrication and input and output matched discrete components. The mixers' input and output port are matched with reflections 28 dB at 1.575GHz and 24 dB at 26 MHz, respectively. It provides 3.2 dB low insertion loss. The local oscillator of system provided by TI LMX2581 PLL that has low cost and two differential output.

The IF stage is designed with NE592 video amplifier with reasonable common mode rejection ratio due to high noise immunity with the lowest cost. At the final stage, since digital signal is required for acquisition stage, the LMH7220 1-bit ADC and 8-bit ADS831 have been placed final stage. Since the inputs of ADCs are differential, baluns have been used in interstages connection and provide test signal-end supply to differential input. Besides, due to testability reasons, surface mount antenna connecters have been accommodated in place of surface mount antenna that are appropriate for upper L frequency of GPS. In addition, in order to provide signal integrity and high crosstalk immunity, decoupling and bypass capacitors have been added every stage with suitable filtering structure and stages have been terminated series and parallel 50 ohms structure. For this design, PCB has been designed with 4-layer FR-4 board with continuous solid ground plane to low noise signal integrity and separated power plane with the intention of testing circuit at different conditions.

7. FUTURE WORK

This disadvantage of using differential amplifier at IF stage, it quite difficult to yield symmetrical operation. Currently, Because of testability, separate voltage plane and different voltage pin are used, however, linear voltage regulator provide low noise supply voltage for active devices. Since IF stages are supplied with differential voltage supply pins, supply voltage bus should be designed, and this design should include overvoltage and polarity protection circuit to protect system for user error. Secondly. Resonant low-Q with high selectivity should with – 3 dB bandwidth at 2.4 MHz should place between IF stages amplifier to degraded signal-to-noise ratio of systems. Surface Mount antenna should be added instead of SMA connector, which is placed for testability and not only 8-bit ADC but also header pins, SMA connectors and zero-ohm resistors should not put final design because these also placed for testing purpose. The SPI and ADC controller should be coded VHDL. Besides, the signal buffer can be coded at FPGA, temporarily hold data while moving from front-end device to personal computer. Then, because of hardware stage completed, real-time constraints signal processing software should be developed with high-level programming language accurately.

A. APPENDIX A

A.1. PLL CodeLoader GUI

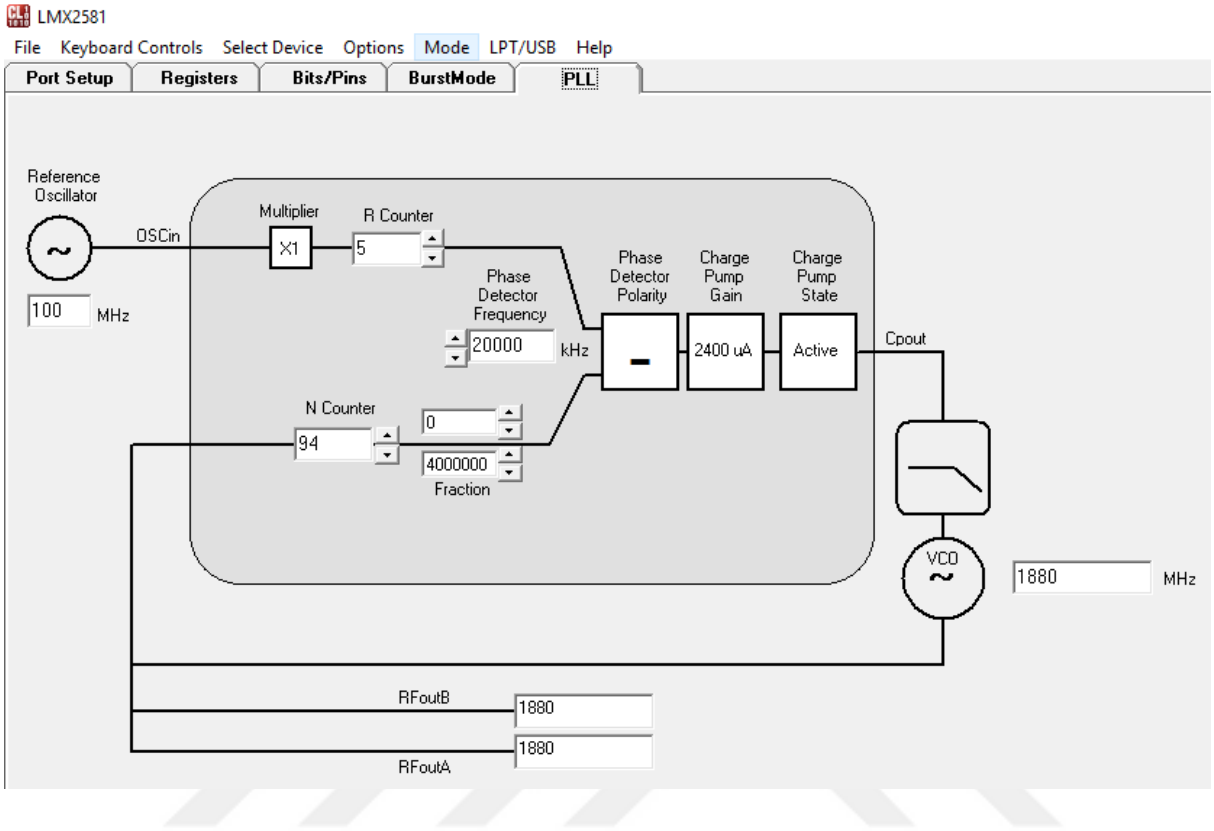


Figure A-1 PLL Codeloader

Figure A-1 demonstrates PLL control closed loop and adjusting coefficient for voltage-controlled output (VCO) with respect to given oscillator input. Moreover, phase polarity, charge pump gain and state are changeable through this interface.

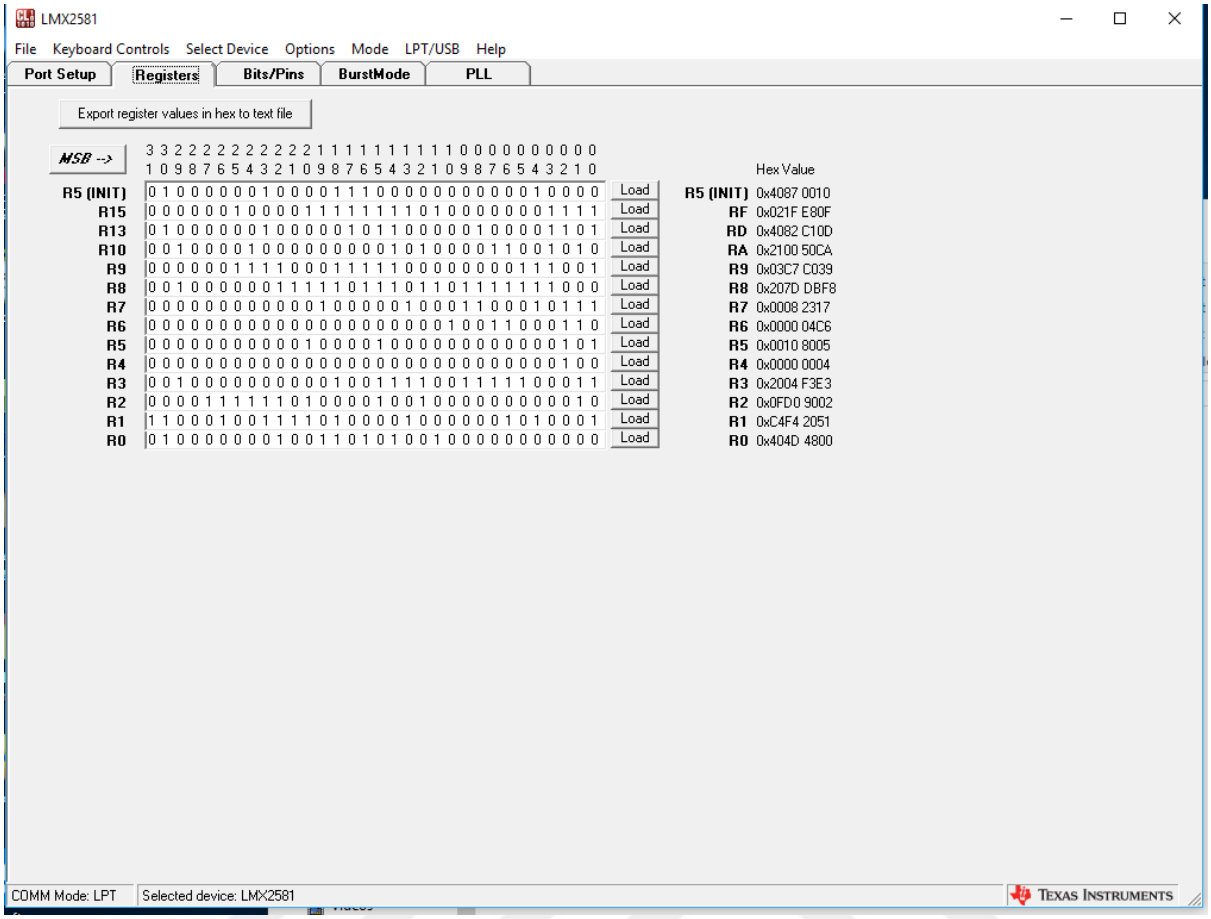


Figure A-2 Register value of PLL

Figure A-2 Register value of PLL reveals that PLL's registers value have been selected in order to generate 1549.42 MHz frequency output for local oscillator mixer input. Hence, signal have down-converted 26 MHz at mixer output.

A.2. Schematic of RF Stage

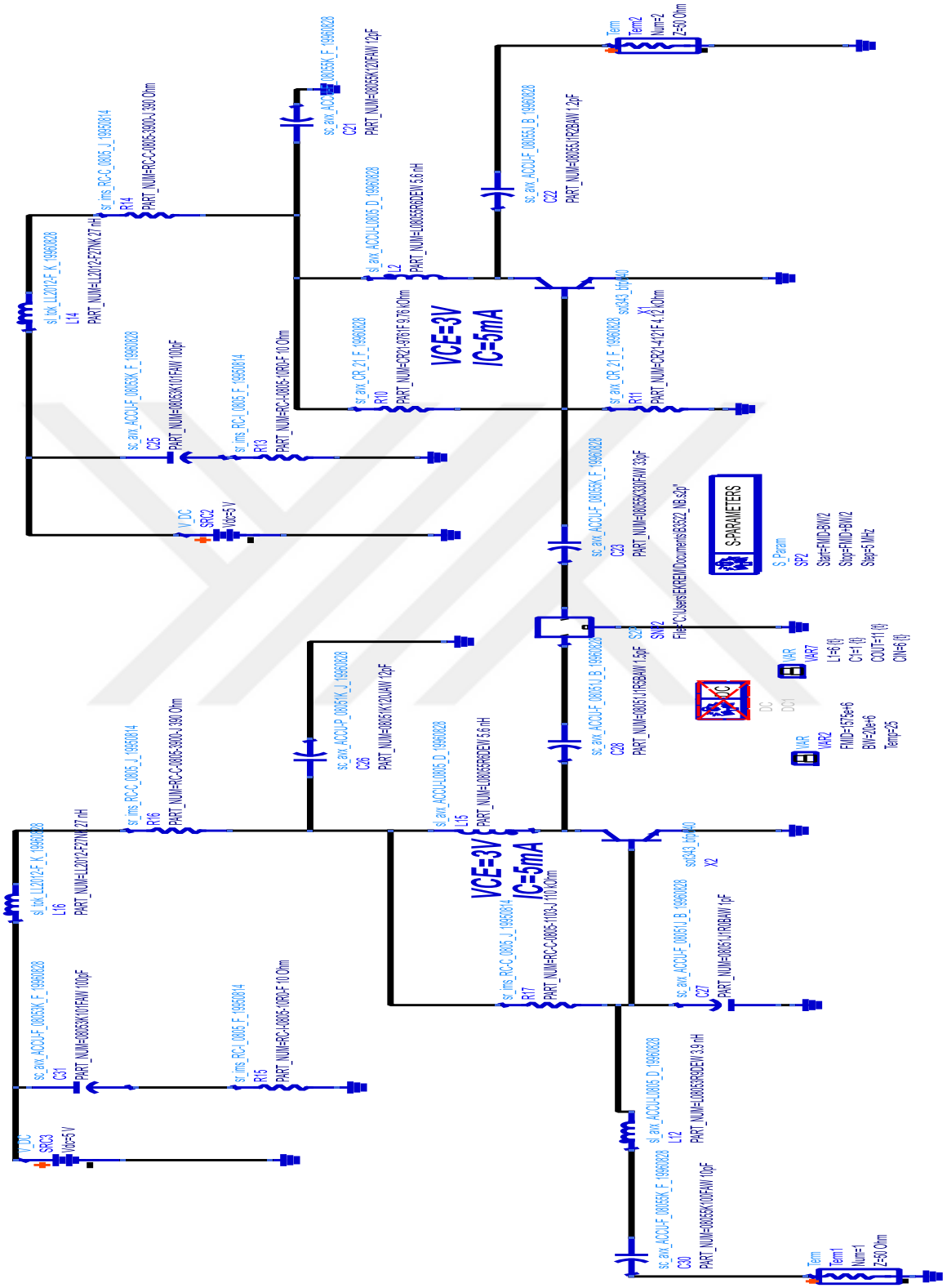


Figure A-3 Schematic of RF Stage

A.3. Gantt Chart of Project Plan

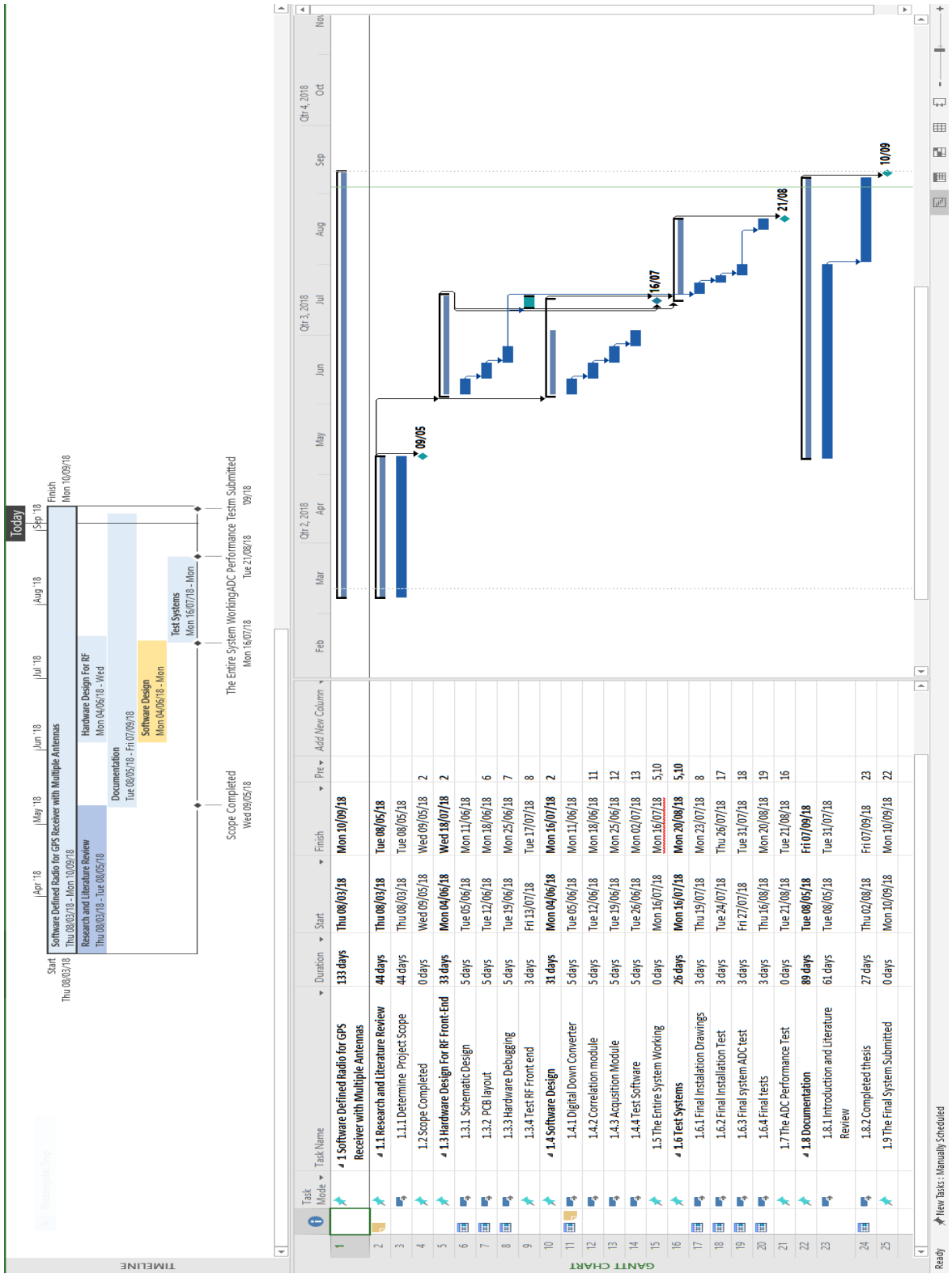


Figure A-4 Microsoft Project capture of project original time plan

GLOSSARY

ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
BB	Baseband
BER	Bit Error Rate
BOC	Binary Offset Carrier
BM	Base Model
CBOC	Composite BOC
CPU	Central Processing Unit
PLL	Phase-locked Loop
DSP	Digital Signal Processing
CDMA	Code Division Multiple Access
FDMA	Frequency Division Multiple Access
FFT	Fast Fourier Transform
FE	Front-End
GLONASS	Global Navigation Satellite Systems
GNSS	Global Navigation Satellite Systems
GPS	Global Positioning System
HW	Hardware
IF	Intermediate Frequency
LNA	Low Noise Amplifier
RHCP	Right Hand Polarized Signal
LHCP	Left Hand Polarized Signal
MBOC	Multiplexed BOC
PC	Personal Computer
PRN	Pseudorandom Noise
RF	Radio Frequency
SDR	Software Defined Radio
SNR	Signal-to-noise ratio
SW	Software
TDMA	Time Division Multiple Access
USB	Universial Serial Bus

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