ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

FIRST ORDER NOISE SHAPING SAR ADC WITH A NOVEL SC FILTER

M.Sc. THESIS

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

ÖZGÜN ANAHTARLAMALI KONDANSATÖR FİLTRELİ BİRİNCİ DERECE GÜRÜLTÜ ŞEKİLLENDİREN ARDIŞIL YAKLAŞIMLI ANALOGDAN SAYISALA DÖNÜŞTÜRÜCÜ

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TEMMUZ 2020

Hüseyin Ozan GÜLEÇ, an M.Sc. student of ITU Graduate School of Science Engineering and Technology 504171209 successfully defended the thesis entitled "FIRST ORDER NOISE SHAPING SAR ADC WITH A NOVEL SC FILTER", which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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FOREWORD

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July 2020 Hüseyin Ozan GÜLEÇ

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ABBREVIATIONS

ADC	**:** Analog-to-Digital Converter
DAC	**:** Digital-to-Analog Converter
LSB	**:** Least Significant Bit
SAR	**:** Successive Approximation Register
EF	**:** Error Feedback
NS	**:** Noise Shaping
PVT	**:** Process-Voltage-Temperature
OSR	**:** Oversampling Ratio
ENOB	**:** Effective Number of Bits
Qe	**:** Quantization Error
FOM	**:** Figure of Merit
STF	**:** Signal Transfer Function
NTF	**:** Noise Transfer Function
SNDR	**:** Signal-to-Noise and Distortion Ratio
CMOS	**:** Complementary Metal Oxide Semiconductor
SC	**:** Switched-Cap
MIM	**:** Metal-Insulator-Metal
MOM	**:** Metal-Oxide-Metal
DNL	**:** Differential Non-linearity
INL	**:** Integral Non-linearity
DFF	**:** D Flip-Flop
MSB	**:** Most Significant Bit

SYMBOLS

^oC	**:** Temperature in Celcius
k	**:** Boltzman constant in Joule·K^{-1}

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FIRST ORDER NOISE SHAPING SAR ADC WITH A NOVEL SC FILTER

SUMMARY

Increasing demand on energy efficient devices for bio-applications and portable devices ask for better solutions. Many of these applications require an analog-to-digital converter (ADC) in order to further process the recorded data. 0-10 kHz bandwidth is common for bio-applications and in this frequency range successive approximation register (SAR) ADC type is the most efficient architecture. The reason comes from the fact that this circuitry consists of mostly digital gates which control the switches connected to the capacitive digital-to-analog converter (DAC). However, SAR type converters lose both the area and energy efficiency very rapidly if signal-to-noise ratio (SNR) is pushed ahead of 70 dB.

In the similar frequency range delta-sigma ($\Delta\Sigma$) converters can provide much higher resolutions than 12 bits using low resolution quantization yet they rely on over conversion of the input signal therefore increasing the power consumption in exchange for extra resolution.

A prevailing approach in the recent years is to search for hybridization techniques for SAR and $\Delta\Sigma$ such that increased DAC size and comparator noise would not occur when SAR resolution is kept increasing. The most effective and easy to implement idea is found to be connecting a delaying low pass filter to the DAC and processing the quantization error at the end of each conversion. In this method, SAR is everything in a delta-sigma circuit except the delaying integrator block. Due to this reason this technique is more appropriately called "noise shaping SAR" instead of a delta-sigma converter.

A literature review of all passive and active noise shaping ideas for SAR is critiqued and active filtering option is chosen. There are several reasons for this, first most passive methods require an extra input pair for the comparator which increases its noise contribution, secondly they require extra timing slots at the end of the conversion and more importantly in active implementations the noise transfer function is more flexible and can be tailored to the on hand application's needs.

A novel switched-cap (SC) integrator solution is suggested and analyzed in detail. This idea is tested on a SAR circuit with an 8-bit DAC and a ultimate resolution of 70 dB SNR or more is targeted. After behavioral simulations are done in MATLAB and verilogA environment the circuit is designed using X-FAB 180 nm CMOS process. By doing careful calculations of the mismatch error from the capacitive DAC, a calibration circuit was not needed. Simulation results show that only for an oversampling ratio (OSR) of 8, 11.65 effective number of bits (71.95 dB SNDR) was achievable and careful calculations of the unit capacitance size of digital-to-analog converter used in the circuit resulted in tolerable mismatch error without any calibration circuit. The circuit has an efficieny of 231.7 fJ/conv. and consumes a total power of 15.18 μW.

ÖZGÜN ANAHTARLAMALI KONDANSATÖR FİLTRELİ BİRİNCİ DERECE GÜRÜLTÜ ŞEKİLLENDİREN ARDIŞIL YAKLAŞIMLI ANALOGDAN SAYISALA DÖNÜŞTÜRÜCÜ

ÖZET

Taşınabilir cihazların yayıngınlaşması ve gelişen biyo uygulamalar enerji verimliliği çok yüksek olan çözümler gerektirmektedir. Bu uygulamalar ölçülen datanın bir analogdan sayısala (A/S) dönüştürücü bloğu aracılığıyla farklı şekillerde işlenmesine ihtiyaç duyar. Biyo uygulamalar için 0-10 kHz bant genişliği tipik değerlerdir ve bu frekans aralığındaki en efektif çözüm ardışıl yaklaşımlı dönüştürücü mimarisi ile elde edilir. Bu mimarinin verimli çalışması büyük oranda bir kondansatörlü sayılsandan analoğa (S/A) dönüştürücü bloğuna uygulanacak anahtarları kontrol eden sayısal devrelerden oluşmasından kaynaklanmaktadır.

Ancak, referans gerilimlerinin üretilmesi ve dönüştürücü çıkışının giriş sinyalinden çıkarılması/toplanması adına kullandıkları kondansatörlü (S/A) dönüştürücülerinde her 1 efektif bit artışı için 2 kat alan artışı gerekir. Bu duruma ek olarak karşılaştırıcı devresinin transistör gürültüleri de 2 kat düşürülmek zorundadır ve bu durum hem güç tüketimini hem de artan transistör kapasiteleri yüzünden oluşacak iki yönlü sinyal sızıntılarını arttırarak devrenin istenilen efektif bit sayısına ulaşmasına engel olmaktadır. Bu nedenlerden ötürü ardışıl yaklaşımlı dönüştürücülerin çözünürlükleri 70 dB sinyal/gürültü oranı üzerine çıkartılmak istenildiğinde hem alan hem de enerji verimlilikleri hızlıca kaybolmaya başlamaktadır.

Aynı frekanslarda delta-sigma ($\Delta\Sigma$) tipi dönüştürücüler aynı giriş sinyalinin defalarca düşük çözünürlükteki dönüşümü ile 12 bit ve üzeri çözünürlükler sağlayabilmektedirler; fakat fazladan elde edilen çözünürlük için güç tüketimi arttırılmış olur. $\Delta\Sigma$ yapılarında her çevrim sonundaki hata çıkışın girişten çıkarılması sonucunda elde edilir. Bulunan hata değeri ise uygun bir gecikmeli alçak geçiren filtreden geçirilerek tekrardan (A/S) bloğuna sokulur. Bu operasyon sonucunda çevrim hatasından oluşan gürültü spektrumu yüksek frekanslara itilerek gürültü spektrumu şekillendirilmiş olur. Bu tip yapılarda çıkışın anlık değeri dönüşüm sonucu niteliğine sahip değildir. Gürültünün bastırıldığı bant içi bölgedeki sinyale ulaşabilmek için çıkışın fazladan dönüşüm oranında bir alınacak ortalaması çıkışın nihai değeri olarak kabul edilir. Başka bir deyişle çıkışın kendisi değil ortalaması gerçek çıkış olarak düşünülmelidir.

Bu yapının dezavantajı düşük çözünürlükteki çevrim hatasının referans gerilimiyle karşılaştırılabilecek büyük bir değer olmasından dolayı bu hata gerilimini işleyecek alçak geçiren (integratör) filtre bloklarının da çok güç harcamasını gerektirmesidir. Ek olarak, işlenmiş çevrim hatasını (A/S) dönüşümünden sonra giriş sinyalinden çıkartılabilmesi için fazladan bir (S/A) bloğu ile tekrar dönüşüme uğraması gerekliliğidir. Bütün bu sebepler $\Delta\Sigma$ devrelerinin enerji verimliliğini kötü etkilemektedir.

Ardışıl yaklaşımlı dönüştürücülerdeki hızla artan (S/A) dönüştürü boyutu ve karşılaştırıcı gürültüsü sorunlarının hiç yaşanmaması adına son yıllarda öne çıkan $\Delta\Sigma$ ile ardışıl yaklaşımlı yapıların hibritleştirilmesi ile sentez bir yapı ortaya çıkarma

çabaları gözlemlenmiştir. En etkili ve kolay yöntem olarak her çevrim sonunda oluşan nicemleme hatasının (S/A) dönüştürücüden örneklenip gecikmeli bir alçak geçiren filtreden geçirilmesi ile elde edilebildiği görülmüştür. Bu metot içinde ardışıl yaklaşımlı dönüştürücü bir ΔΣ devresindeki gecikmeli integratör bloğu dışındaki her şeyi kapsamaktadır. Bu nedenle de ΔΣ dönüştürücü yerine "gürültü şekillendiren ardışıl yaklaşımlı dönüştürücü" olarak isimlendirilmesi daha doğrudur.

Bu yaklaşım dönüşümler sonucunda ardışıl yaklaşımlı yapıların çevrim sonunda kondansatörlü (S/A) dönüştürücüsünde çevrim hatasını bulundurmasını avantaja çevirip bu hata geriliminin bir alçak geçiren filtre aracılığıyla bir sonraki çevrimde karşılaştırıcıya uygulanması ile hali hazırda bulunan dönüştürücüye delta-sigma operasyonu yaptırılarak bant içinde gürültü bastırması şeklindedir.

Tezin konusu olarak bu tarz yapıların incelenmesi ve bu sayede ardışıl yaklaşımlı dönüştürücü yapıların enerji verimliliğinin 10 bit ve üzeri efektif çözünürlüklerde de korunması hedeflenmiştir. Bu yapının temel avantajı çok bitli operasyonu ile çevrim hatasının referans gerilimine oranla çok daha küçük bir değer olması bu yüzden de basit bir alçak geçiren filtre ile kolaylıkla gerçelenebiliyor olmasıdır. Devrenin yüksek verimliliğini koruduğu bir çözünürlükte tasarım yapabilmek adına 8 bitlik ardışıl yaklaşımlı devre tercih edilmiştir. Frekans aralığı içinse az alan ve düşük güç tüketimi gerektiren biyo uygulamalar düşünülerek 0-10 kHz aralığı seçilmiştir.

Gürültü şekillendiren ardışıl yaklaşımlı yapılar kayıplı (pasif) veya kayıpsız (aktif) integratörler ile gerçeklenmektedirler. Literatürdeki bütün aktif ve pasif gürültü şekillendiren ardışıl yaklaşımlı dönüştürücü yapıları tarandıktan sonra pasif yerine aktif filtreli olarak çalışılması tercih edildi. Bunun başlıca sebepleri öncelikle pasif gerçekelemelerin çoğunlukla karşılaştırı devresinde fazladan bir adet giriş transistörü ikilisine ihtiyaç duyması ile karşılaştırıcı yapısının gürültü katkısının artması, çevrim sonunda pasif integral alımı işleminin gerçekleşebilmesi için fazladan saat darbeleri ekleniyor olması ve en önemlisi gürültü transfer fonksiyonunun parametrelerinin uygulamalara spesifik olarak yeterince serbestçe ayarlanamamasıdır.

Bu tezde aktif devrelerin güç tüketimini düşürecek ve oluşacak 1/f gürültüsünü de zayıflatacak özgün bir anahtarlamalı kondansatör filtre çözümü ortaya atılmıştır. Bu yapıyı diğer yapılardan ayıran özellikleri girişte tampon yapı kullanmak yerine örnekleme kapasitesini her daim (S/A) dönüştürücüye bağlı bulundurarak sabit bir yükleme yapmaktadır; ayrıyetten çok güç tüketen işlemsel kuvvetlendirici blokları yerine tipik bir evirici devresini filtrenin lineer kuvvetlendiricisi olarak değerlendirmektedir.

Ortaya atılan yapının parazitik kapasitelerden ötürü olan yük paylaşımları ve kuvvetlendiricinin sonlu kazancı gibi idealsizlikleri göz önünde bulundurularak detaylı teorik analizi yapılmıştır. Bu analizde ortaya atılan yapının sadece küçük çevrim hatası gerilimini işleyeceğinden ötürü sonlu frekans cevabı ve sonlu çıkış akımından kaynaklanabilecek potansitel sorunlar göz ardı edilmiştir. Bu fikir 8 bitlik (S/A) dönüştürücülü bir ardışıl yaklaşımlı devre üzerinde test edilmiştir. Nihai çözünürlük olarak ise 70 dB sinyal/gürültü oranı hedeflenmiştir. VerilogA ortamında yapılan davranışsal modellerin ardında devre X-FAB 180 nm CMOS prosesinde transistör seviyesinde gerçeklenmiştir.

İlk olarak filtrede kullanılacak olan eviricinin sağlaması gereken minimum DC kazancı üretim varyasyonlarına rağmen sağlayabilecek bir evirici tasarlanıp beklenen

performansı gösterdiği teyit edilmiştir. Daha sonra ise filtrenin bağlanacağı 8 bit ardışıl yaklaşımlı dönüştürücünün tasarlanılmasına geçilmiştir. Dönüştürücü kontrol bloğu ve bu bloğun zamanlama diyagramı belirlenen bütün bitlerin mutlaka (S/A) dönüştürücü bloğuna uygulanacağı şekilde tasarlanmıştır. Karşılaştırıcı devresinin çalışma frekansında düzgün çalıştığı gözlenip herhangi bir meta-stabilite sorununa sahip olmamasına dikkat edilmiştir. (S/A) dönüştürücünün birim kapasite boyutu filtre ile olan yük paylaşımı, termal gürültüsü ve üretim varyasyonlarından gelecek hataları göz önünde bulundurularak tasarlanılmış olup CSAtool adı verilen MATLAB temelli bir algoritma ile diferansiyel/integral doğrusalsızlıkları gözlemlenmiştir. (S/A) dönüştürücüye bağlanacak olan anahtarlar ise kondansatörler ile RC yapıları oluşturarak sonlu yükselme davranışı göstermektedirler. Bu nedenle de anahtarların üretim ve sıcaklık varyasyonlarına rağmen maksimum dirençlerinin 8 bitlik operasyon için gereken yükselme/oturma süresini sağlayacakları düşüklükte olmalarına dikkat edilerek geçiş kapısı transistörleri uygun şekilde boyutlandırılıp gerekli simülasyonları yapılmıştır.

Önce ardışıl yaklaşımlı yapının blokları 8 bit çözünürlük hedeflenerek gerektiği şekilde tasarlanmıştır. (S/A) dönüştürücünün birim kondansatör değeri uyumsuzluk şartları üzerinden 8 bitlik operasyona uygun olarak seçilmiştir; bu sayede herhangi bir kalibre edici ek devreye ihtiyaç kalmamıştır. Gürültü bastırılması operasyonundan gelecek ekstra çözünürlük için gerekli olacak (S/A) dönüştürücü lineerliği için uygun bir kalibrasyon tekniğinin uygunlaması kapasite boyutlarını büyültmektense alan tüketimi açısından daha verimli olacağı görülmüştür. Ardışıl yaklaşım mantığının gerçeklenmesinde ise bütün bitler belirlendikten sonra yine de son bit değerini (S/A) dönüştürücüye uygulayacak şekilde kurgulanmıştır ki gürültü bastırma operasyonu için gerekli geçerli artık gerilim elde edilebilsin. (S/A) anahtarlanması içinse alt plaka anahtarlaması daha iyi lineerliğinden ötürü üst plaka anahtarlamasına tercih edilmiştir.

Bu çalışma ile sadece basit bir evirici devresi kullanan anahtarlamalı kondansatör integratör devre ile alan tüketimindeki minimal bir artışla ekstra çözünürlük elde edilmiştir.

Simülasyon sonuçlarında görülmektedir ki fazladan dönüşüm oranının sadece 8 olması ile 11.65 efektif bit çözünürlük (71.95 dB sinyal/çözünürlük) elde edilebilmektedir. Ortaya atılan filtrenin örnekleme kapasitesi ile ana (S/A) dönüştürücü kapasite arasındaki yük paylaşımından dolayı giriş gerilimi referans gerilimine kadar arttırılsa da sistemin doymaya girmediği gözlenmiştir. Birim kondansatör değerinin uyumsuzluk hataları göz önünde bulundurularak dikkatlice boyutlandırılmasını sonucunda devrenin üretim varyasyonlarına rağmen hedef çözünürlük değerini sağlayabildiği görülmüştür. Devrenin 231.7 fJ/dönüşüm enerji verimliliği sahip olup 15.18 μW toplam güç tüketmektedir.

İleri çalışma olarak ise ortaya atılan özgün filtrenin ikinci dereceden gürültü bastıran versiyonu geliştirilecektir. İhtiyaç görülürse devreden elde edilecek çözünürlükle paralel olarak (S/A) dönüştürücünün lineerliği çeşitli kalibrasyon teknikleri ile arttırılabilir. Karşılaştırıcı bloğunun gürültüsünün nasıl şekillendiği ve fazladan giriş ikilileri eklenmesi durumda oluşabilecek sorunların giderilmesine yönelik çözümler aranacaktır. Son olarak ise, çok bitli operasyonlarda daha iyi çalışan "dithering" tekniği de ortaya atılan gürültü şekillendiren ardışıl yaklaşımlı yapıya entegre edilmek istenmektedir. Bu sayede harmonik frekansları zayıflatılmış daha temiz ve yüksek dinamik aralığa sahip bir çıkış spektrumu elde edilmiş olacaktır.

1. INTRODUCTION

Currently the integrated circuit (IC) industry is driven into more and more integration. The need comes from the demand for more compact and portable devices. Moreover, internet-of-things (IoT) and bio-sensor applications also build-up the need for circuits with less area and lower power consumption.

An analog-to-digital converter (ADC) is a must in many of these application in order to convert the recorded input to a digital form which can be processed in the digital domain. The main ADC types are summarized in the Fig. 1.1. The ΔΣ ADC dominate high resolutions but they are power hungry architectures. They use oversampling and noise shaping (NS) which requires over conversion of the input and consumes more power by doing so. On the other hand, successive-approximation-register (SAR) ADCs are the most effective solution in mid-resolution range (7-10) for low bandwidth operations. The main reason SAR is the most effective is that it has fewer number of analog blocks compared to other ADC architectures. It is made up of an array of switches and capacitances in order to create the reference voltages needed for the digital-to-analog converter (DAC) and all these switches are controlled by a digital circuity which consumes much less power relative to other analog sub-circuits, such as comparators, integrators and etc..

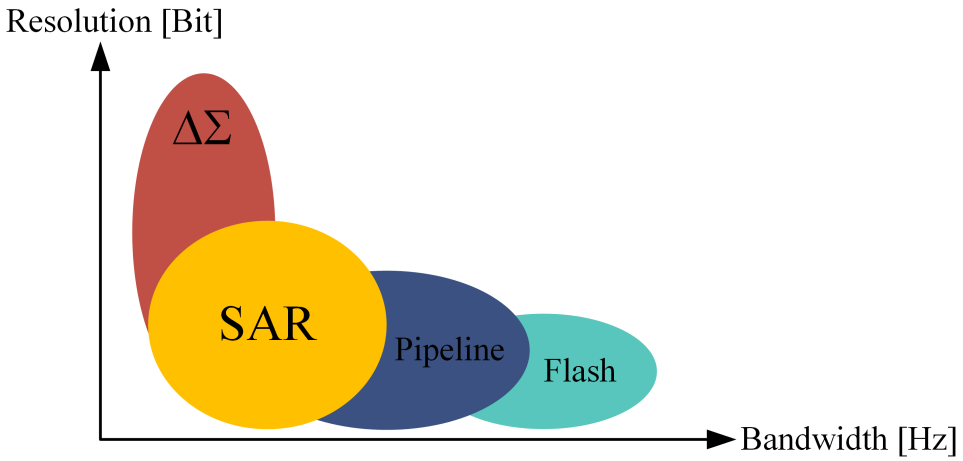


Figure 1.1 : Usefulness range of main ADC types.

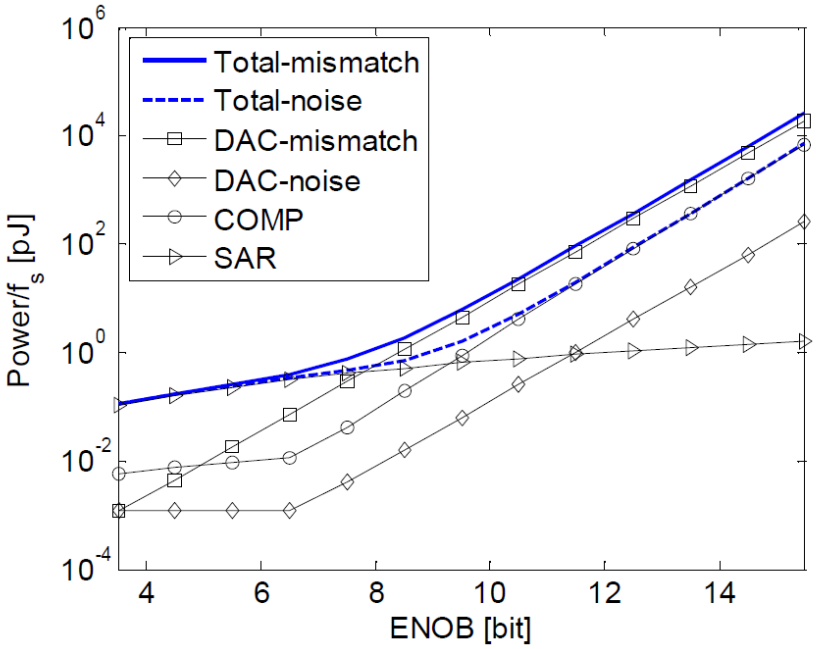


Figure 1.2 : SAR ADC power boundaries for mismatch and other noise sources [1].

An important challenge arises when applications require power efficient solutions but demand higher resolutions in a small chip area. Although, SAR ADCs are succeeding in the former hallmarks Fig. 1.2 shows that they begin to fail if the resolution is pushed far ahead (>10 bits). There are two main reasons for this:

- First, the total DAC capacitance exponentially grows as the resolution is increased which increases the area exponentially and quadruples the power consumption in mid to high resolution applications. Also, the degradation from mismatch requires additional solutions to calibrate and make sure the linearity of the DAC is on par with the final ADC resolution.

- Secondly, the input-referred comparator noise requirement gets more rigorous and hard to achieve. This also increases the power consumption and because of the larger input transistors the kick-back noise of the comparator degrades the conversion even further.

A suitable solution to increase the resolution without increasing the DAC size is to convert the on hand SAR converter into a multi-bit $\Delta\Sigma$ conversion scheme. This idea can prevent the complexities arise from exponentially increasing DAC size and increasing comparator noise.

1.1 Literature Review

The prevailing technique is using the residue voltage left at the top plate of the DAC at the end of each conversion as a measure of error and feeding this voltage back to the circuit for the next conversion via a loop filter. It should be noted that in this case the SAR circuitry is not the quantizer in a ΔΣ loop and no additional DAC is required as the SAR circuitry is everything except the delaying integrator block in a ΔΣ circuit. Therefore, this type of operation is called noise-shaping SAR (NS-SAR) as it describes the situation more appropriately.

This idea alleviates the problem of more resolution in small area at the expense of increased power consumption. Nevertheless, compared to traditional SAR ADCs ,especially when SNDR is intended to be pushed to 75 dB or higher, Fig. 1.3 shows that it is evidently more benefical to implement noise shaping into SAR rather than increase the DAC size for more resolution.

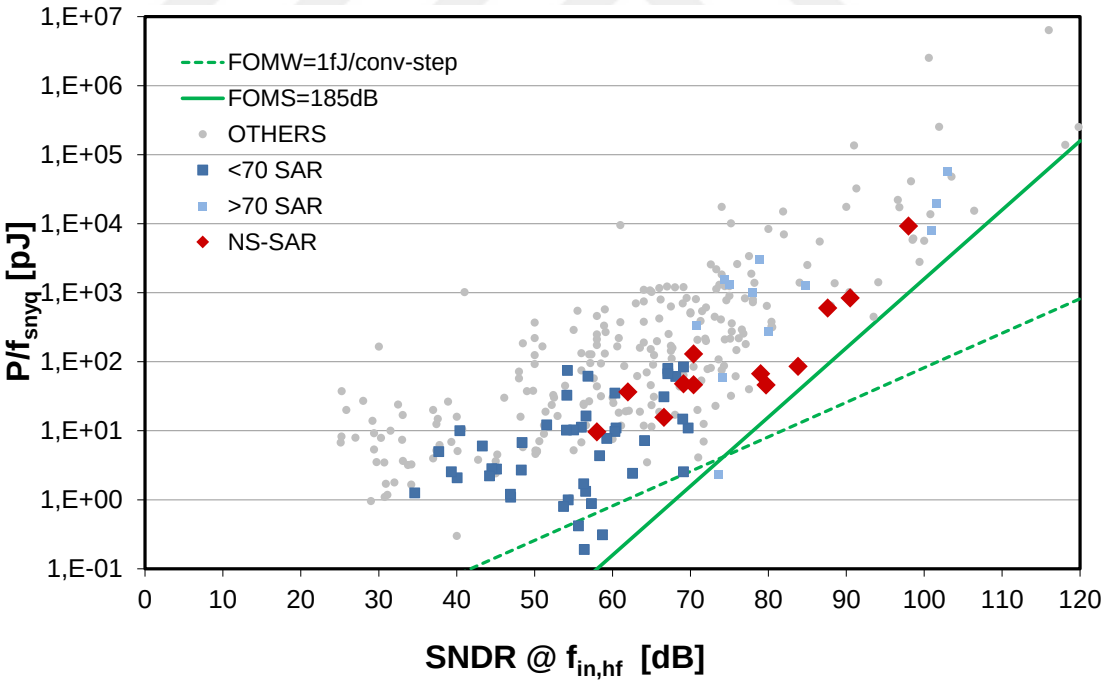


Figure 1.3 : Survey for SAR and NS-SAR ADCs [2].

The idea of hybridization of SAR and ΔΣ properties start with [3] which uses SAR as the low power quantizer of the ΔΣ and [4] subtracts the delayed residue from the input before a new conversion begins. The second method is referred as the error feedback (EF) scheme and is carried by [5]. However, an important drawback of this technique

is that kT/C noise constraint of the circuit is determined by the unit capacitance instead of the total DAC capacitance which can degrade the area advantage [6].

The technique adopted in this thesis originates from [7]. The idea is to create a loop with a feed-forward path by sampling the residue voltage left on the DAC at the end of the conversion and connecting it to the comparator via a delaying filter as shown in the Fig. 1.4. This idea is easier to implement than error feedback schemes as subtracting the residue using the neutral input of the comparator is more straightforward than subtracting it in the sample-and-hold phase.

As mentioned before this type of operation uses a single DAC for both the quantization and acquisition of the residue voltage so it reduces the power consumption immensely compared to ΔΣ converters. In addition to the quantization noise, comparator's input referred noise also will be shaped. Unfortunately, DAC mismatch error needs additional measures and thermal noise will be reduced by the inherit oversampling in the noise shaping action.

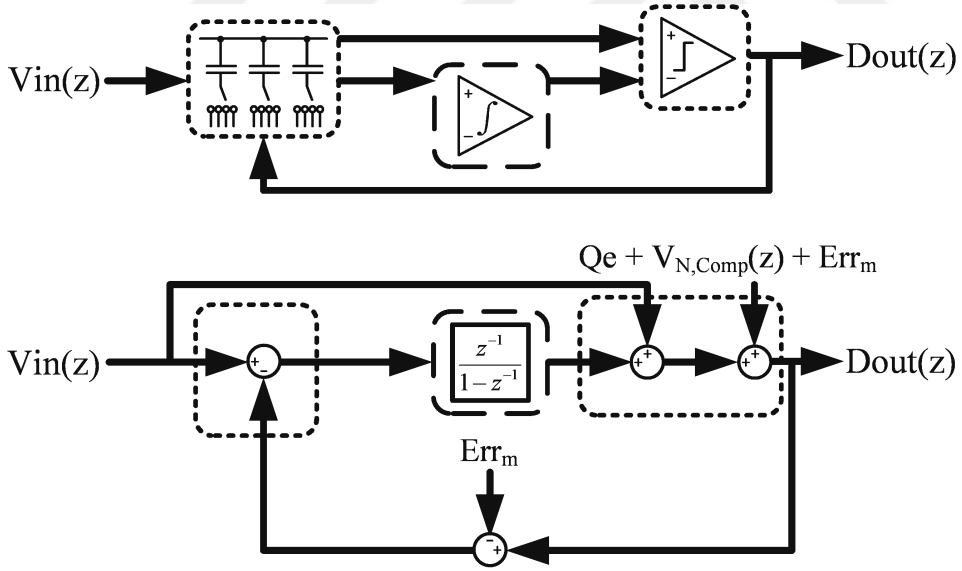


Figure 1.4 : Primary noise shaping idea for SAR.

The biggest advantage comes from the fact that when SAR ADC's multi-bit operation and the feed-forward path are combined it greatly reduces the effective chance of saturation at the output of the loop filter as only the small residue voltage will be processed by the loop filter H(z). This feature simplify the specifications of the loop filter as it becomes easier to design the filter and reduce its power and area consumption.

Two opposing approaches can be found in the literature as it is possible to process the residue voltage passively (lossy) or actively (without loss) and there are several benefits to both of them.

When residue sampling and integration is done passively the charge is shared between series of capacitors. This type of operation is devoid of transistors except switches (which also work passively) and only depends on the capacitor ratios therefore (as [8] points out) it is basically insensitive to process, voltage and temperature (PVT) variations. Additionally, those type of filters do not generate flickr noise which otherwise would be required to be removed by an implementation of chopping or auto-zeroing.

On the other hand, due to its lossy operation the zero/s of the transfer function can not be placed at $z = 1$ and the frequency response of the NTF levels way before DC, as shown in Fig. 1.5. This limits the maximum oversampling (OSR) number as it loses its efficiency to lower quantization noise while OSR is kept increased. Relating to the sample rate and bandwidth, passive implementations require additional clock pulses at the end of conversion which also limits the achievable maximum sample rate. This limit is not necessarily a problem for the efficiency of the conversion rather that it limits the maximum effective number of bits (ENOB) achievable from the circuit. Lastly, more often passive noise shaping requires an additional input pair for the comparator which leads to performance loss due to additional noise and mismatch [9].

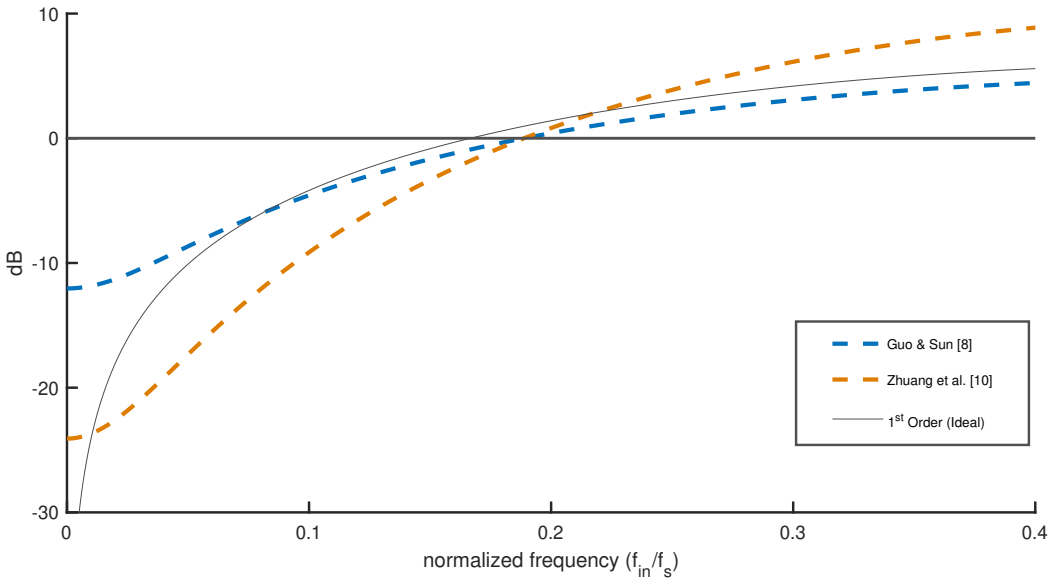


Figure 1.5 : Noise transfer functions from passive integrations.

Active integrating solutions on the other hand, allow for more arbitrary capacitor sizing as the losses from capacitive charge sharings can be compensated by the active amplifier in the circuit. Although, this implies increased power consumption it decreases the capacitance area (and save power consumption by doing so). As mentioned, the zero/s of the noise transfer function will be placed closer to $z = 1$ and this permits higher OSR values and SNDR can be pushed even higher as a result. By using the advantage of capability to adjust the zero and pole placement more freely, power consumption of the amplifier can be decreased when targeted resolution is achieved by lower gains. This lets the designer to optimize every aspect of the noise shaping custom to their needs. Downside of active integration is that they can react more poorly to technology-scaling than passive implementations and [10] mentions that passive implementations can be better suited for low duty-cycle sensor applications as they can power up instantly and do not require any guard time for bias circuits to settle.

1.2 Motivation

The goal is to increase the resolution while maintaining the fair trade-off between resolution and power consumption. Complex solutions for sub-blocks will be avoided as possible in order to decrease the device count for lower power consumption and similarly circuit will not use additional time slots at the end of the conversion. Capacitive DAC will be carefully sized so that any additional calibration will be necessary.

Design targets are shown in Table 1.1. Using multi-bit nature of the SAR an inverter will be used as the linear amplifier ,similar to [11], in order to have active integration with minimal power and area consumption.

Table 1.1 : Design targets.

Specification	SAR	Bandwidth	ENOB	Input Range	Technology	Power Consumption
Target	8 bit	10 kHz	11	$0 - 1.2V$	180 nm	Low as Possible

2. Background Theory

2.1 Quantization Noise

An analog-to-digital converter works by comparing the analog input signal with already defined reference voltages (quantization levels). The caveat is that there are finite number of quantization level and the digital representation of the input signal will be an estimate of the original signal as shown in the Fig. 2.1. At the end of each conversion an ideal ADC will converge to the applied signal with an error always less than 1 LSB. The total quantization noise power for an ideal ADC in the Nyquist interval is given in (2.2). This noise has a uniformly distributed noise density in the band from 0 to fs/2.

$$\Delta = \frac{V_{FS}}{2^N} \tag{2.1}$$

$$P_{Qe} = \frac{1}{\Delta} \int_{\varepsilon=-0.5\Delta}^{\varepsilon=0.5\Delta} \varepsilon^2 d\varepsilon = \frac{\Delta^2}{12} \tag{2.2}$$

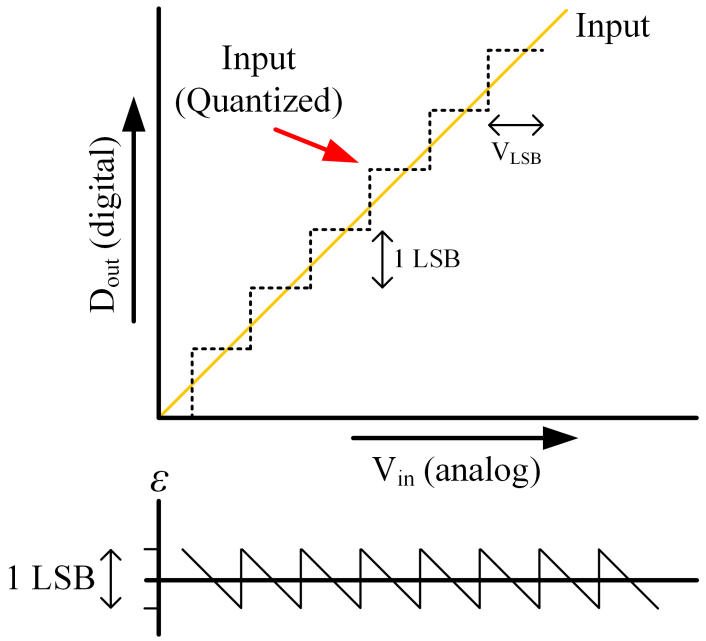


Figure 2.1 : Definition of quantization noise.

2.2 Ways of Improving Resolution

2.2.1 Oversampling

A signal sampled at the Nyquist rate can be reconstructed by using the recorded samples. However, in the case where the sampling rate is higher than the Nyquist rate "oversampling" occurs. This over conversion of the input signal spreads the quantization noise spectrum to a larger frequency interval as shown in the Fig. 2.2. When the oversampling ratio (OSR) is defined as (2.3) the signal-to-noise ratio will be increased as in (2.4). Similar to Fig. 2.3 a digital low pass circuit for filtering the out-of-band noise is necessary and a decimation filter is needed in order to return to the intended Nyquist operating frequency. By choosing the OSR value as a power of two makes the design of such digital blocks easier.

$$\mathrm{OSR} = \frac{fs/2}{fbw} \tag{2.3}$$

$$\mathrm{SNR}_{\mathrm{oversampled}} = \mathrm{SNR} + \log_{10}(\mathrm{OSR}) \tag{2.4}$$

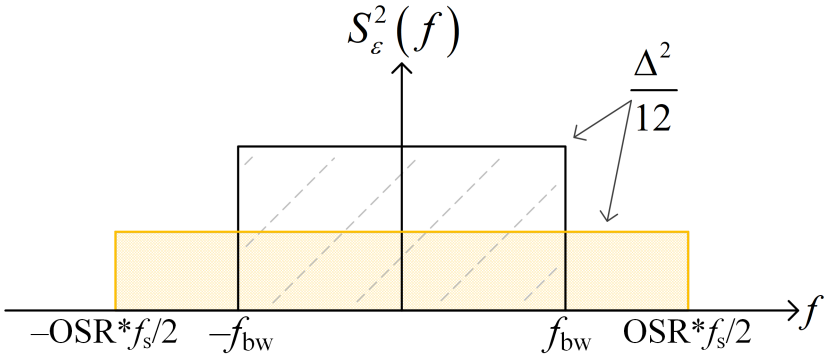


Figure 2.2 : The effect of oversampling on quantization noise.

2.2.2 Noise shaping

Another approach is to construct a ΔΣ loop (similar to Fig. 1.4) so that the quantization noise will be shifted towards the out-of-band high frequencies as shown in (2.5). In order to form such a loop the error of each conversion must be fed through a delaying integrator (low pass filter) and subtracted from the next input.

$$Dout(z) = Vin(z) + \left(1 - z^{-1}\right) Q_e \tag{2.5}$$

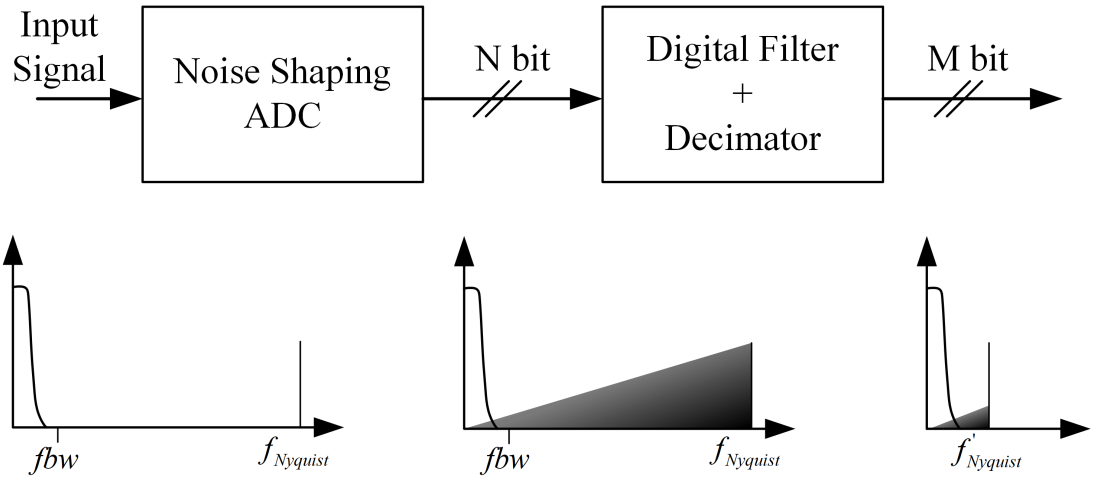


Figure 2.3 : Noise shaping ADC diagram.

In this approach instantaneous values of the output can be misleading but when the output is decimated as illustrated in Fig. 2.3 the circuit can converge to a less noisy representation of the input after it is being quantized. As given in (2.6), the signal transfer function (STF) of the example in Fig. 1.4 is an all pass function and the noise transfer function (NTF) is an ideal first order high pass function.

$$\text{STF} = 1 \quad , \quad \text{NTF} = \left(1 - z^{-1}\right) \tag{2.6}$$

It is important to ensure stability in ΔΣ loops. Therefore, all poles of the NTF must reside inside the unit circle and low pass filters used in loop should be designed carefully so that their outputs do not saturate during the operation. However, using a feed-forward path in the loop and multi-bit quantization notably reduces the change of saturation at the output of the integrators as they require only to process the small residue voltage. Although this idea is harder to realize in conventional ΔΣ architectures (because it becomes harder to reliably convert the multi-bit digital output to a continuous signal which can be subtracted from the input) it will be shown in next section that this idea is very much feasible when a delaying low pass filter is connected to the DAC and feed the integrated residue voltage of the previous conversion to the comparator in order to subtract this value from the next sampled input signal.

3. Proposed NS-SAR

This thesis proposes an active integration noise shaping architecture. The idea is shown in Fig. 3.1. This circuit does not use a buffer circuit and the sampling capacitor Cs is always connected to the DAC even during the operation in order to have a constant effect on the circuit. The filter do not integrate any charge during conversion and its input and output is close to the inverter-based amplifier's switching point because of the unit feedback connection. After the conversion is done and all logic outputs are determined, the filter switches to integration mode and only integrates the small ($\leq$1 LSB) residue voltage left on the top plate of the DAC at the end of each conversion.

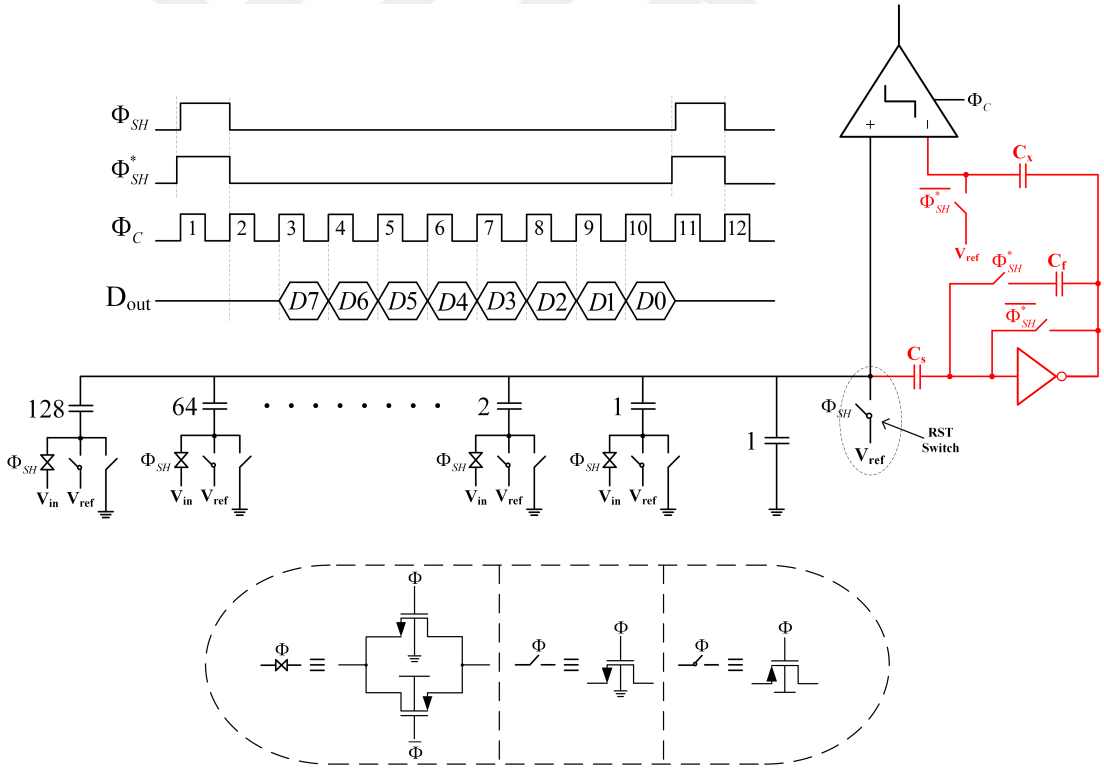


Figure 3.1 : Noise shaping SAR.

The comparator has only a single input transistor pair. This is a very desired feature as [9] pointed out having more than one input pair results in an increased input-referred noise (and kick-back) and also eventually more power consumption. Additionally, Cx capacitance will be equally sized as the sum of total DAC capacitance and Cs for

equalizing kick-back on both sides. Owing to the fact that due to bottom sampling the top plate voltage of the DAC returns to Vref (by an error of 1 LSB) in each conversion comparator ensures roughly the same amount of kick-back before the integration starts thus do not spoil the noise shaping operation and bottom plate subtraction on Cx capacitance put away the need of an extra input on the comparator circuit as the integrated residue charge will be conveyed and stored on the top plate of Cx during the subsequent conversion. The SC filter uses an inverter as the linear amplifier rather than a power hungry operational amplifier and as it can be seen from the timing diagram the filter is made sure to be ready to encounter the residue voltage before the system resets itself.

3.1 Sub-circuits of NS-SAR

3.1.1 Capacitive DAC

For the capacitive DAC an 8-bit single-ended binary DAC is preferred rather than a differential one in order to save power and space. 8-bit is chosen as above this value the fair trade-off between power consumption and resolution starts to breaks off in SAR converters and power consumption has to be increased more than 2 times for each added bit resolution. Low density $\left(1.0\ \text{fF} \cdot \mu m^{-2}\right)$ metal-insulator-metal (MIM) capacitance type is preferred over the metal-oxide-metal (MOM) capacitance for better mismatch performance and linearity.

An analysis has been done in [12] for unit capacitance selection for a binary-weighted DAC consists of 2^N unit capacitors with a common centroid layout. It is concluded, for a confidence level of 99.7% (3σ) the error from mismatch is given by (3.2) and kT/C noise constraint is given by (3.4). The Pelgrom coefficient for the preferred technology X-FAB 0.18 μm is $k_c = 0.28\% \cdot \mu m$. An LSB$/16$ of ADC error is reserved for mismatch error (so that at the targeted ENOB of 11 mismatch loss will be approximately LSB$/2$), unit capacitance value for mismatch errors 23.7 fF is sufficient.

$$\sigma\left(\frac{\Delta C_{nom}}{C_{nom}}\right) = \frac{k_C}{\sqrt{C/k_P}} = \frac{0.28\,\% \cdot \mu m}{\sqrt{C/1fF \cdot \mu m^{-2}}} \tag{3.1}$$

$$Err_m = \frac{3\sigma\left(\sqrt{2^N}-1\right)}{\left(\sqrt{2}-1\right)\left(2^N-3\sigma\sqrt{2^N}\right)}\text{Vref} < \frac{LSB}{16} \tag{3.2}$$

$$Cunit = 23.7\,fF \tag{3.3}$$

It is observed that for 12 or higher ENOB values increasing the unit capacitance value for mismatch gives rise to very large total DAC size. Therefore, for higher resolutions further mismatch improvement should come from a calibration circuit so that area advantage is preserved.

The kT/C noise constraint is given by (3.4). For a target resolution of 11 ENOB with a minimum OSR of 4, unit capacitance of 0.7 fF is adequate.

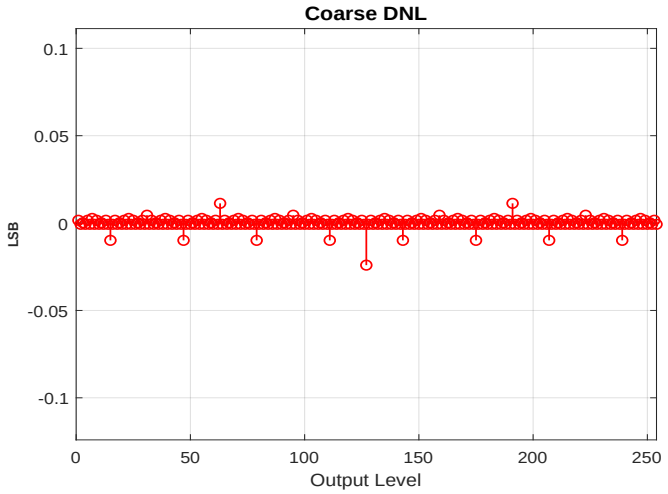
$$Err_t = 2\sqrt{\frac{\text{kT}}{2^N Cunit \cdot OSR}} \leq \frac{\text{LSB}}{4} \tag{3.4}$$

$$Err_t = 2\sqrt{\frac{1.38x10^{-23}\cdot 300\text{K}}{2^8 Cunit \cdot 4}} \leq \frac{Vref}{2^{(2+11)}} \tag{3.5}$$

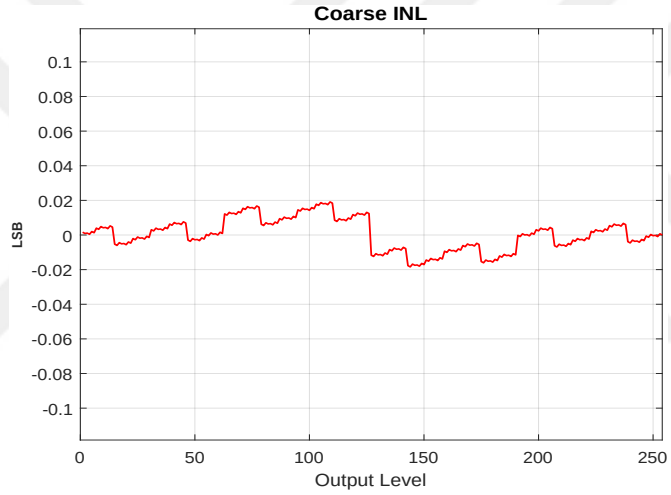
$$Cunit = 0.7\,fF \tag{3.6}$$

A safe value 28.4 fF (5μm x 5μm) as the unit capacitance is chosen; which gives a total DAC capacitance of $\sim$ 7.27 pF.

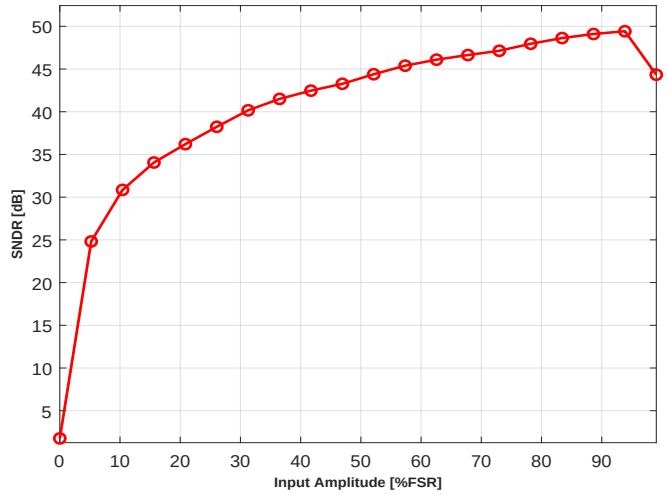
As mismatch simulations take too much time a MATLAB based solution is derived by [13] which utilizes the mathematical and statistical properties related to capacitive DAC architectures. From Fig. 3.2 it can be seen that when just the 8-bit DAC is simulated DNL and INL performance losses are less than 0.1 LSB for both cases and the circuit permits a resolution very close to 8-bit even when a 100 μV input noise is applied in 3.2c. This desirable performance is expected as the DAC is over designed in the expectation of a higher effective resolution.



(a)



(b)



(c)

Figure 3.2 : a) DNL performance. b) INL performance.
c) SNDR vs. Input Amplitude.

3.1.2 Switches

DAC capacitance forms an RC circuit with the switches connected to the input signal during the sampling phase. A particular amount of time is required for the DAC to settle to that input voltage with a certain precision. For 8-bit precision (3.8) must be satisfied.

$$\tau = R_{ON} C_{DAC} \tag{3.7}$$

$$\mathrm{t} = \ln\left(\frac{1}{1/(2^8-1)}\right)\tau \tag{3.8}$$

$$\mathrm{t} = 5.5\,\tau \tag{3.9}$$

For Cdac $\simeq$ 7.27 pF and Fs = 20 kHz (Fclk = 10xOSRxFs = 1.6 MHz),

$$\mathrm{t} = 5.5\,\tau < (1.6\ \mathrm{MHz})^{-1} = 625\,ns \tag{3.10}$$

$$5.5\,x\,R_{ON}\,x\,7.27\,pF < 625\,ns \tag{3.11}$$

$$R_{ON} < 15.63\,k\Omega \tag{3.12}$$

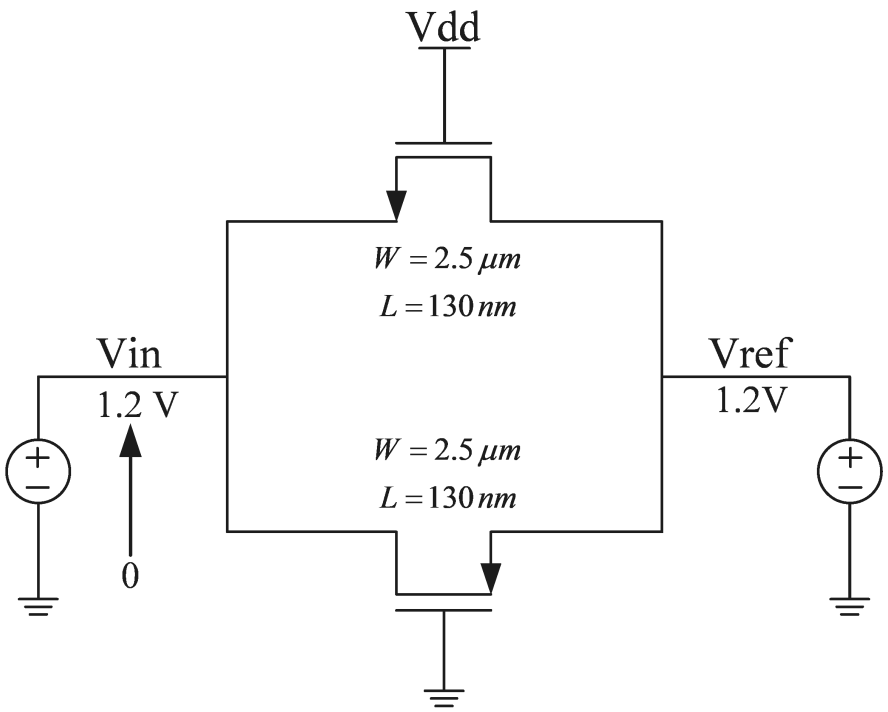


Figure 3.3 : Switch resistance test bench.

N-type and p-type transistors are sized the same such that equal clock feed-through in both the rising and falling clock will cancel out.

The test bench shown in Fig. 3.3 is used to validate the settling time constraints. Fig. 3.4 shows that for all the process corners and temperature ($0 - 80^oC$) the switch resistance never exceeds 1.9 kΩ which satisfies (3.12). It is also examined that the transmission gate have enough linearity when a DAC sized capacitor is connected at the output of the transmission gate it can give an SNDR more equal to 80 dB.

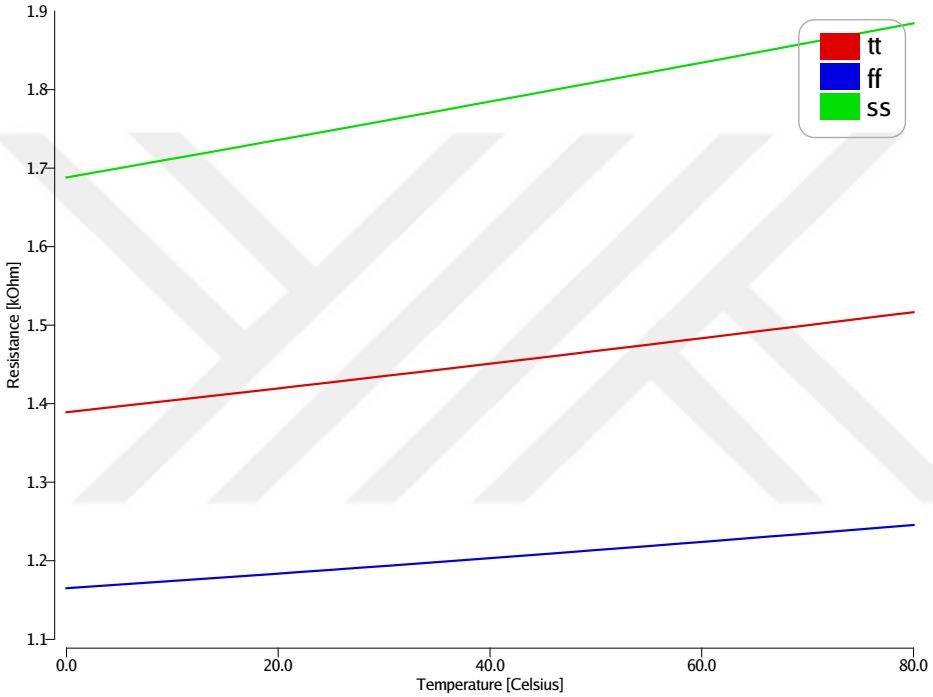


Figure 3.4 : PVT variations for the sampling switch.

3.1.3 Comparator

For the comparison operations a dynamic comparator shown in Fig. 3.5 is used as this circuit only draws current during transitions and does not have a static power current. It consists of only a single input pair which does not put additional burden on the noise shaping operation.

For the dynamic latch comparator Differential Pair Comparator type is preferred over Resistive Divider Comparator implementation as latter is more sensitive to transistor mismatches [14]. Even though constant (or static) offset does not become an issue for SAR ADCs the input transistors of comparator are enlarged as they contribute the most to the offset of the comparator.

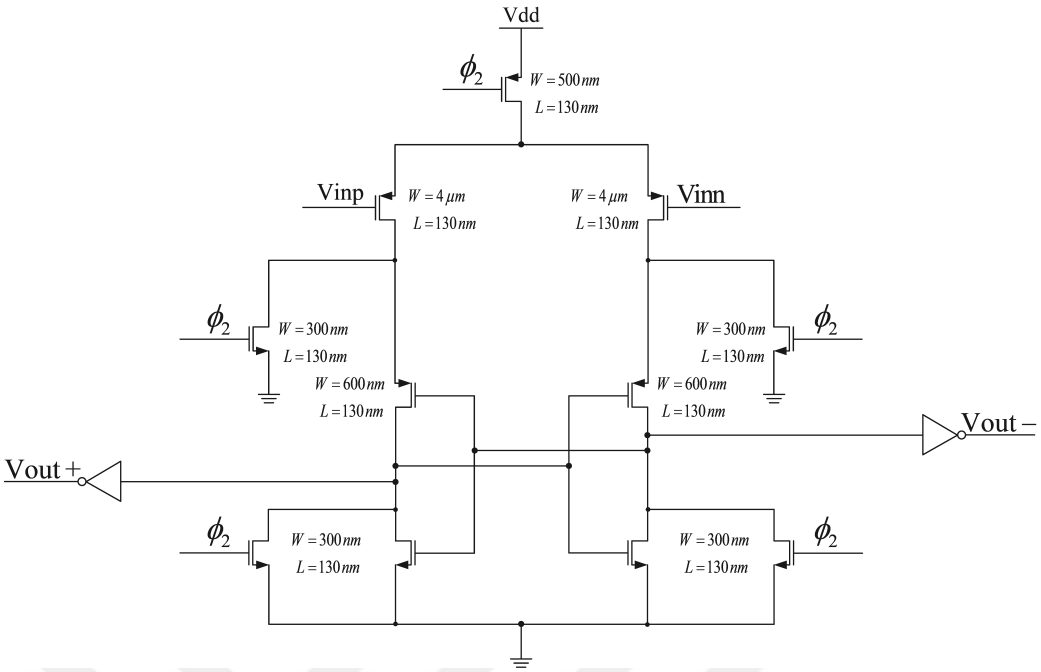


Figure 3.5 : Dynamic latch comparator.

At Fclk = 1.6 MHz the circuit has no metastability issues as shown in Fig. 3.6 and it has a sensitivity less than 20 μV at all input common voltage levels.

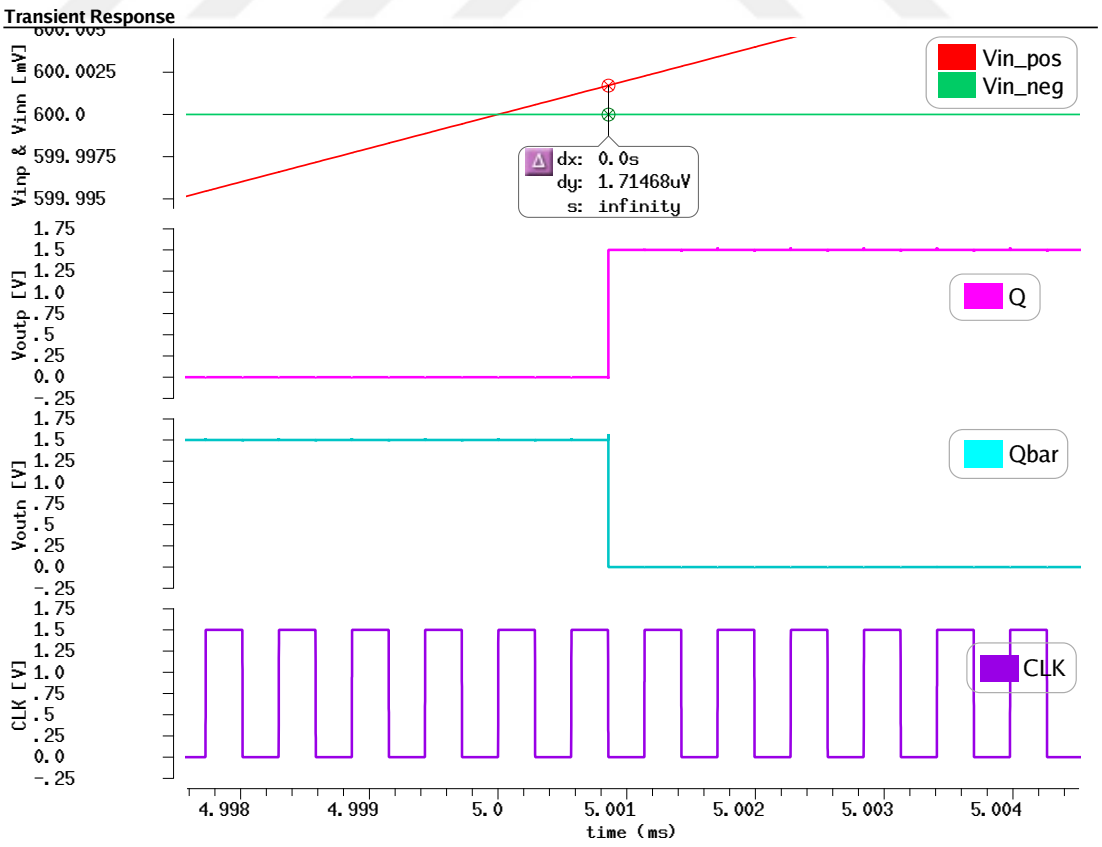


Figure 3.6 : Comparator sensitivity.

3.1.4 SAR logic

When it comes to logic design it is important to realize the logic with minimum device count for better power efficiency. For this reason, a commonly used shift register controlled code register circuit from [15] using minimum device count is utilized.

The SAR logic shown in Fig. 3.7 consists of a shift register and back to back tied D flip-flop (DFF) blocks working as the code register. Starting by the most significant bit (MSB) control signal (D7) the logic first assumes every bit as logic 1 and keeps or inverts this value depending on the comparator decision. DAC voltage is updated at the first and comparisons are done at second half of the main clock pulse.

As charge injection is dependent on the input voltage, top plate switching creates dynamic offset and degrades the linearity. Therefore, a bottom plate switching scheme is exploited instead. This type of operation uses sampling switches for every DAC capacitance in return for better linearity. During the sampling/reset phase all switches ,except Vin switches, are made sure to be in cut-off by the logic independent of the comparator output.

Also, because of bottom plate sampling top plate of the DAC returns to the same reset voltage (V_{ref}) at the end of each conversion which results in the same amount of kick-back from the comparator. This ensures a constant variation on the residue voltage and do not spoil the noise shaping operation.

An often utilized practise is to not apply the last least significant bit (LSB) decision to the DAC after it is determined by the converter. However, this would occasionally corrupt the residue voltage as it might be 1 LSB off from the right conversion error voltage and should be omitted for noise shaping SAR applications.

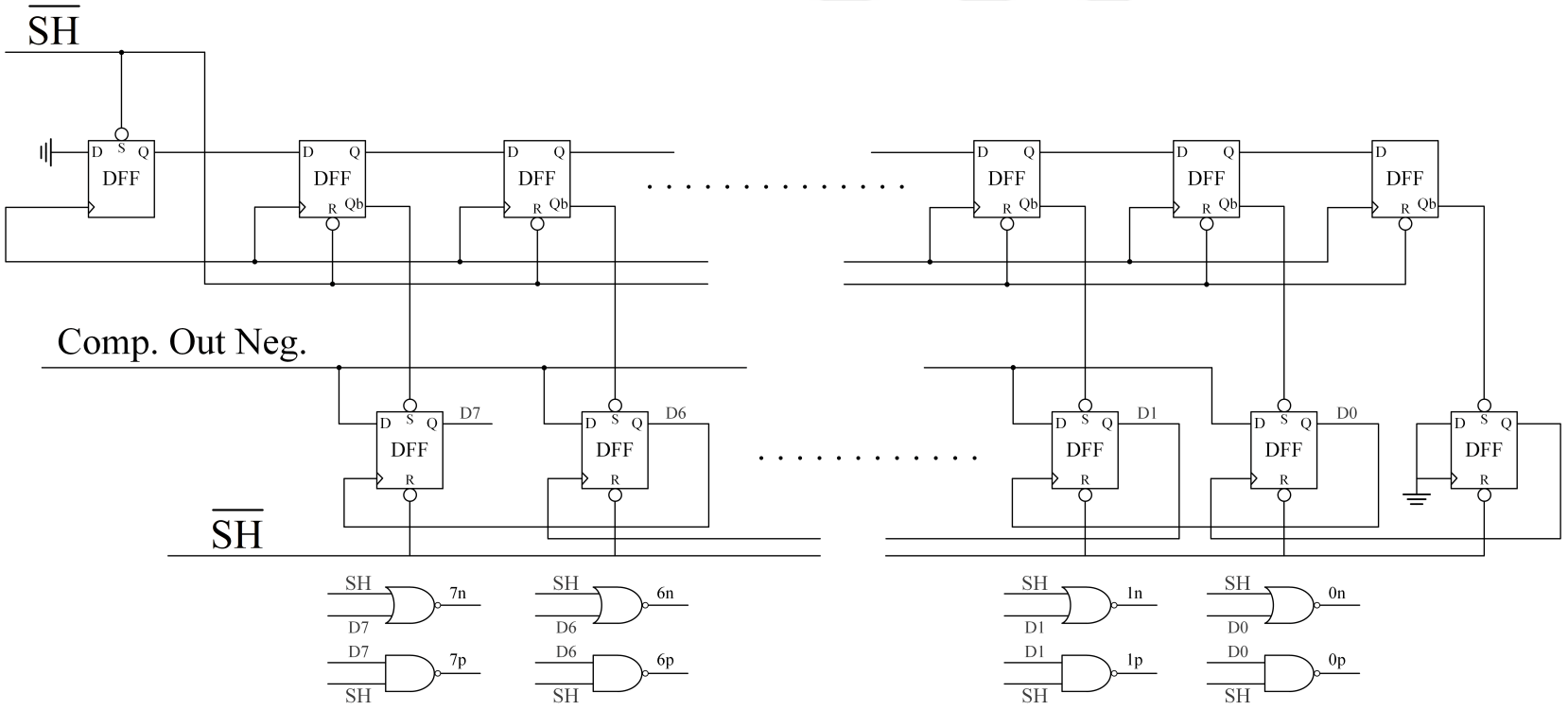


Figure 3.7 : SAR logic.

3.2 First Order NTF Realization

In this section ideal operation of the filter will be explained and all non-idealities such as finite amplifier gain, finite bandwidth and circuit parasitics will be handled in the next sections.

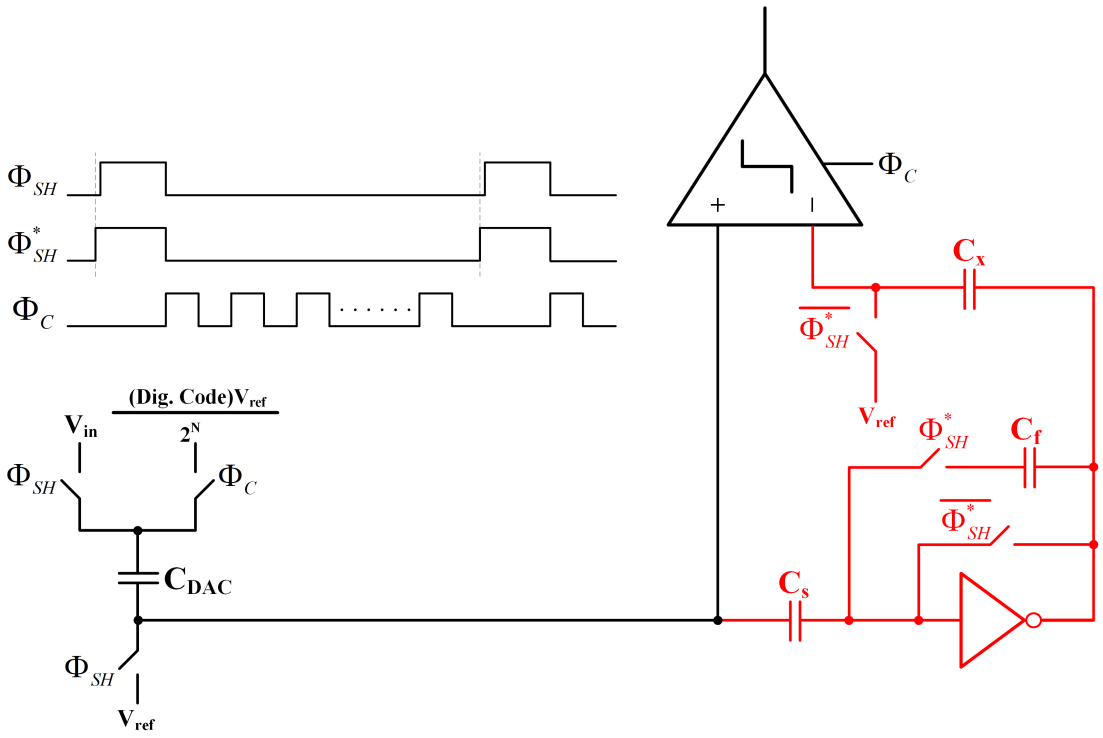


Figure 3.8 : Proposed 1^{st} order noise shaping converter.

- During Conversion $(n-1)$

$$Q_{Cs}[n-1] = \left(V_{SP} + \overline{V_{n,fl}}[n-1] - V_{ref} + \alpha\left(V_{in}[n-1] - Dout[n-1]\right)\right) Cs \quad (3.13)$$

$$Q_{Cf}[n-1] = Q_{Cf}[n-3/2] \quad (3.14)$$

$$V_{+}[n-1] = V_{ref} - \left(V_{in}[n-1] - Dout[n-1]\right)\alpha \quad (3.15)$$

$$V_{-}[n-1] = V_{ref} + V_{SP} - V_{\text{int}}[n-3/2] \quad (3.16)$$

$$\alpha = C_{DAC}/(C_{DAC} + C_S) \quad (3.17)$$

- During Sampling/RST $(n-1/2)$

$$Q_{Cs}[n-1/2] = \left(V_{SP} + \overline{V_{n,fl}}[n-1/2] - V_{ref}\right) Cs \tag{3.18}$$

$$Q_{Cf}[n-1/2] = \left(V_{SP} + \overline{V_{n,fl}}[n-1/2] - V_{\text{int}}[n-1/2]\right) Cf \tag{3.19}$$

$$V_{+}[n-1/2] = V_{ref} \tag{3.20}$$

$$V_{-}[n-1/2] = V_{ref} \tag{3.21}$$

Sum of all currents entering a node should be zero:

$$\Delta Q_{Cs} + \Delta Q_{Cf} = 0 \tag{3.22}$$

$$\Delta Q_{Cs} = Q_{Cs}[n-1/2] - Q_{Cs}[n-1] \tag{3.23}$$

$$\begin{aligned}\Delta Q_{Cs} = &\left(V_{SP} + \overline{V_{n,fl}}[n-1/2] - V_{ref}\right) Cs \\ &- \left(V_{SP} + \overline{V_{n,fl}}[n-1] - V_{ref} + (V_{in}[n-1] - Dout[n-1])\,\alpha\right) Cs\end{aligned} \tag{3.24}$$

$$\Delta Q_{Cf} = Q_{Cf}[n-1/2] - Q_{Cf}[n-3/2] \tag{3.25}$$

$$\begin{aligned}\Delta Q_{Cf} = &\left(V_{SP} + \overline{V_{n,fl}}[n-1/2] - V_{\text{int}}[n-1/2]\right) Cf \\ &- \left(V_{SP} + \overline{V_{n,fl}}[n-3/2] - V_{\text{int}}[n-3/2]\right) Cf\end{aligned} \tag{3.26}$$

$$\begin{pmatrix} \text{flickr noise process correlates well for close samples} \\ \overline{V_{n,fl}}[n-1/2] - \overline{V_{n,fl}}[n-1] \simeq 0 \\ \overline{V_{n,fl}}[n-1/2] - \overline{V_{n,fl}}[n-3/2] \simeq 0 \end{pmatrix}$$

$$\Delta Q_{Cs} = -\alpha\,(V_{in}[n-1] - Dout[n-1])\,Cs \tag{3.27}$$

$$\Delta Q_{Cf} = (V_{\text{int}}[n-3/2] - V_{\text{int}}[n-1/2])\,Cf \tag{3.28}$$

$$-(V_{in}[n-1] - Dout[n-1])\,\alpha Cs + \left(V_{\text{int}}\left[n - {}^{3}/_{2}\right] - V_{\text{int}}\left[n - {}^{1}/_{2}\right]\right) Cf = 0 \tag{3.29}$$

Performing a z-transform and re-arranging the equation above gives us,

$$V_{\text{int}}(z) = -\alpha \frac{Cs}{Cf} \frac{z^{-1/2}}{(1-z^{-1})} (V_{in}(z) - Dout(z)) \tag{3.30}$$

SAR operation will equalize both comparator inputs with an error Qe:

$$Qe = V_{+}[n] - V_{-}[n] \tag{3.31}$$

$$Qe = V_{ref} - (V_{in}[n] - Dout[n])\,\alpha - V_{ref} - V_{SP} + V_{\text{int}}[n-1/2] \tag{3.32}$$

Performing a z-transform and substituting 3.30 into equation (3.32),

$$Qe = -(V_{in}(z) - Dout(z))\,\alpha - V_{SP} + \alpha\frac{Cs}{Cf}\frac{z^{-1}(V_{in}(z) - Dout(z))}{(1-z^{-1})} \tag{3.33}$$

$$Qe = -(V_{in}(z) - Dout(z))\,\alpha - \frac{V_{SP}(1-z^{-1})}{(1-z^{-1})} - \alpha\frac{Cs}{Cf}\frac{z^{-1}(V_{in}(z) - Dout(z))}{(1-z^{-1})} \tag{3.34}$$

$$\begin{pmatrix}\text{delayed Vsp is still Vsp}\\ \\ V_{SP}(1-z^{-1}) = 0\end{pmatrix}$$

$$Qe = -(V_{in}(z) - Dout(z))\,\alpha - \alpha\frac{Cs}{Cf}\frac{z^{-1}(V_{in}(z) - Dout(z))}{(1-z^{-1})} \tag{3.35}$$

At the end, transfer function the proposed noise shaping SAR can be seen in (3.36).

$$Dout(z) = V_{in}(z) + \frac{(1-z^{-1})}{\alpha\left(1-\left(1-\frac{Cs}{Cf}\right)z^{-1}\right)}Qe \tag{3.36}$$

The STF of this equation is all-pass unity gain function and its NTF is a high-pass function where at low frequencies the quantization noise (and also the comparator noise) is attenuated. The NTF function has a zero at DC. This is another desired feature as this ADC is intended for low frequency applications and also it has an adjustable pole which can be controlled as a trade-off between more noise shaping or more bandwidth.

As this circuit operates in multi-bit mode with a feed-forward path the residue voltage integrator has to handle small inputs and as long as the pole location of the NTF is kept inside the unit circle the circuit is stable.

3.2.1 SC filter

In this section, a more elaborate analysis will be done on the proposed switched-cap filter implementation. Fig. 3.10 and 3.9 shows the finite gain effect on node voltages. Charge sharings due to parasitic capacitances will be modeled as such:

$$\alpha = \frac{Cdac}{Cdac + Cp_1 + Cs} \quad , \quad \beta = \frac{Cx}{Cx + Cp_2}$$

Although it is not shown in the figures, the flickr noise terms cancel each other out as previously. Hence, the circuit maintains its flickr noise reduction effect. Also, the finite bandwidth and slew rate effects are not analyzed in detail. There are several justifications for this besides the fact that the circuit operates at a relatively low frequency:

- The loop filter processes only the sampled residue voltage which is less than 1 LSB, so there will be minor output swings at the output of inverter-based amplifier.
- As the inverter is in a negative feedback structure, its bandwidth will be multiplied by the loop gain.
- Lastly, when the integration starts the inverter operating point is around its switching point where it can provide high DC-gain and during the transition one transistor enters saturation and thus can provide high slew rate [11].

The charge sharing between the output capacitance of the inverter and Cf, Cx capacitances also affect the integration but this issue is not put into the analysis, rather the capacitance values are chosen sufficiently large in order avoid any problems.

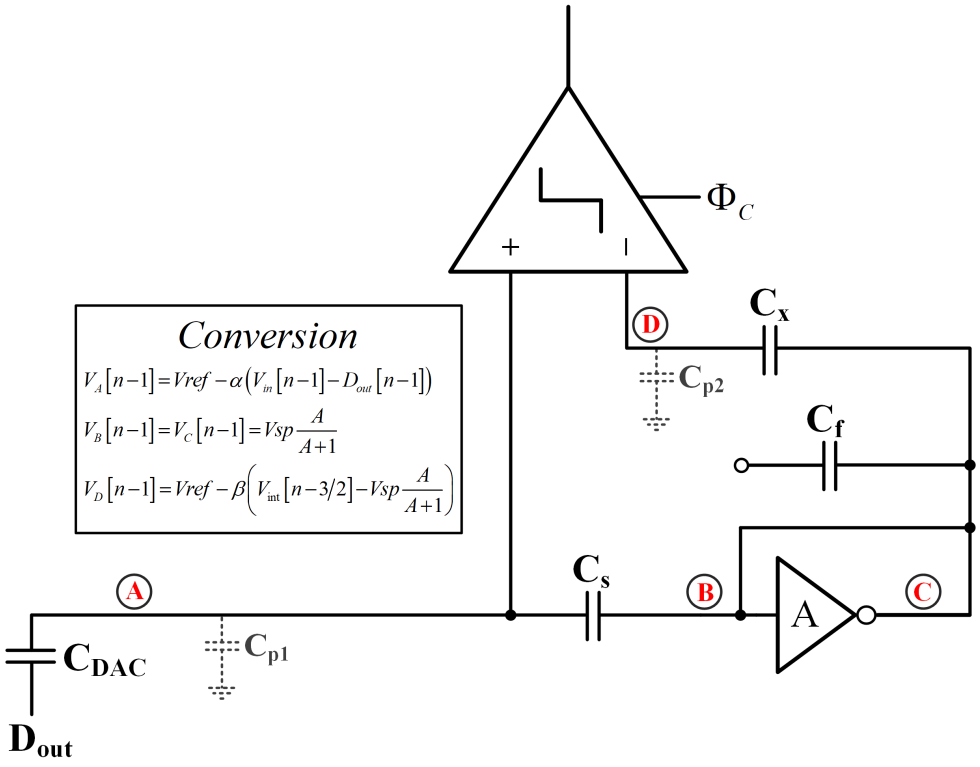


Figure 3.9 : SC filter during the conversion phase.

$$Q_{Cs}[n-1] = \left(Vsp\frac{A}{A+1} - Vref + \alpha\left(V_{in}[n-1] - D_{out}[n-1]\right)\right)Cs \tag{3.37}$$

$$Q_{Cf}[n-1] = Q_{Cf}[n-3/2] \tag{3.38}$$

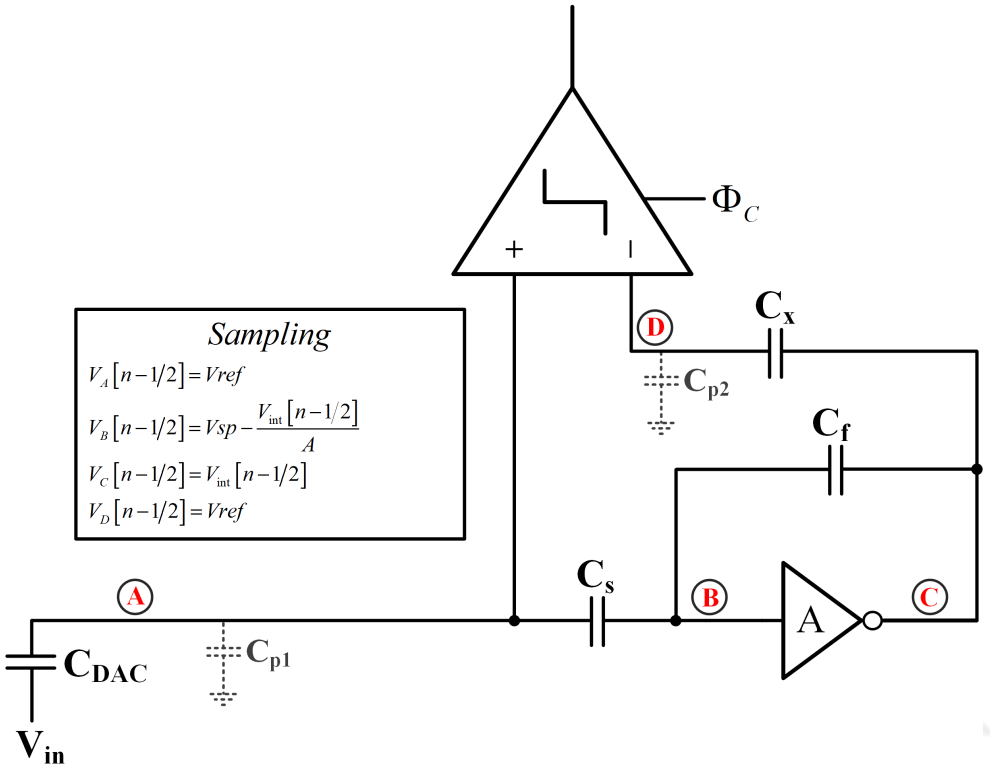


Figure 3.10 : SC filter during the sampling phase.

$$Q_{Cs}[n-1/2] = \left(Vsp - \frac{V_{\text{int}}[n-1/2]}{A} - Vref\right)Cs \tag{3.39}$$

$$Q_{Cf}[n-1/2] = \left(Vsp - \frac{V_{\text{int}}[n-1/2]}{A} - V_{\text{int}}[n-1/2]\right)Cf \tag{3.40}$$

Sum of all currents entering the node 'B' must be zero:

$$\Delta Q_{Cs} + \Delta Q_{Cf} = 0 \tag{3.41}$$

Which leads to,

$$V_{\text{int}}(z) = \frac{-Cs\cdot z^{-1/2}}{Cf\frac{A+1}{A} + \frac{Cs}{A} - Cf\frac{A+1}{A}z^{-1}}\left(\alpha\left(V_{in}(z) - D_{out}(z)\right) - \frac{Vsp}{A+1}\right) \tag{3.42}$$

It can be seen that 3.30 and 3.42 are the same if $A \to \infty$.

Finally,

$$V_D[n] = V_-[n] = Vref - \beta\left(V_{\text{int}}[n-1/2] - Vsp\frac{A}{A+1}\right) \tag{3.43}$$

At the end of the conversion both comparator inputs will be equalized with an error Qe by the SAR operation:

$$Qe = V_{+}[n] - V_{-}[n] \tag{3.44}$$

$$Qe = V_{ref} - (V_{in}[n] - Dout[n])\,\alpha - V_{ref} - \beta\left(V_{\text{int}}\left[n - {}^{1}/_{2}\right] - V_{SP}\frac{A}{A+1}\right) \tag{3.45}$$

Performing a z-transform and substituting 3.42 into equation 3.45,

$$Dout(z) = V_{in}(z) + \frac{1}{\alpha}\frac{\frac{(1+A)}{A}Cf\left(1-z^{-1}\right) + Cs/A}{Cf\frac{(1+A)}{A}\left(1-z^{-1}\right) + Cs/A\ + z^{-1}\beta Cs}Qe + Vsp\cdot\xi^{*} \tag{3.46}$$

3.2.2 Behavioral simulations

In order to estimate the needed gain and capacitance ratios several high level simulations will be executed. First, the finite gain of the loop filter will move away the NTF zero from $z = 1$. It can be seen from 3.11 that the quantization noise attenuation at low frequencies becomes degraded and limited. In return, this also limits the maximum usable OSR value. Furthermore, the pole location gets shifted slightly towards $z = -1$ where stability issues can arise. Although a gain of 60 dB is preferred in order to minimize the gain error resulting from the input capacitance of the inverter even with a gain as low as 10 (20 dB) can provide substantial noise shaping and working with low gain can be leveraged to decrease the power consumption of the loop filter and ease its design.

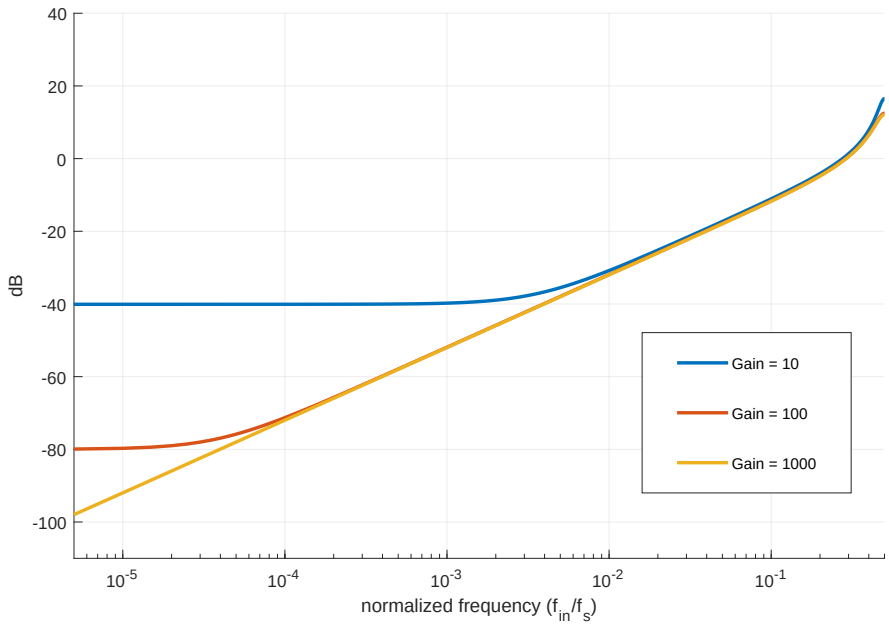


Figure 3.11 : Finite gain effect on NTF of (3.46).

In order to simulate and evaluate the performance of the proposed loop filter for different coefficients a VerilogA based ideal tesh bench is utilized as shown in Fig. 3.12. This test bench has an advantage over a MATLAB simulink loop of its lineer model is that the quantization noise is assumed to be gaussian distributed (or uniformly distributed) in lineer models but it is in fact a signal dependent phenomenon and the quantization in the structure of Fig. 3.12 will represent the expected quantization noise from circuit simulations better[1].

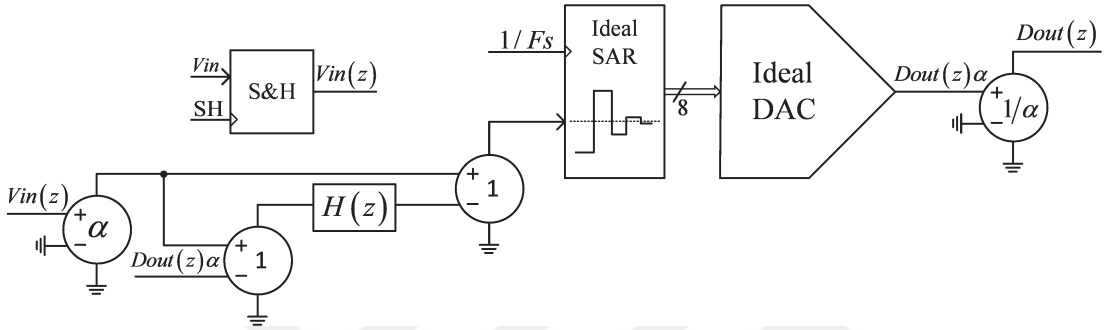


Figure 3.12 : NTF performance test bench.

This configuration realizes the transfer function given in (3.47). Therefore, by choosing $H(z)$ as (3.48) obtains the NTF same of (3.46).

$$Dout(z) = V_{in}(z) + \frac{1}{\alpha}\frac{Qe}{1 - z^{-1}H(z)} \tag{3.47}$$

$$H(z) = \frac{-\beta Cs}{Cf\frac{A+1}{A} + \frac{Cs}{A} - z^{-1}Cf\frac{A+1}{A}} \tag{3.48}$$

In order to mitigate any complication from charge sharing at the output of the inverter-based-amplifier Cf is chosen as 500 fF and from the characterization simulations of the NTF, Cs is chosen to be 775 fF[2].

The charge sharing modeled by α degrades the operation and that higher the α the better. When the parasitic top plate capacitance C_{p1} is thought as 200 fF and using Cdac = 7.27 pF gives sufficient α for the noise shaping operation.

$$\alpha = \frac{7.27pF}{7.27pF + 200fF + 775fF} \geq 0.85 \tag{3.49}$$

[1]Model shown in Fig. 3.12 runs an 8192 point fft analysis in less than a minute.

[2]Because Cx has the size of Cdac+Cs (for equal kick-back) $\beta > 0.95$ is readily satisfied.

Table 3.1 : Appointed filter coefficients.

Parameter	α	β	Cs	Cf	OSR	Inverter DC-Gain
Value	0.85≤	0.95≤	775 fF	500 fF	8	-1000 V/V

60 dB DC gain is chosen for the inverter as this gain ensures an NTF close to ideal case shown in Fig. 3.11. This gain value is tested in the proposed behavioral test bench which shows that nearly 11.5 bit ENOB can be achieved. Table 3.1 summarizes the optimum coefficients needed to achieve more than 11 ENOB from an 8-bit SAR circuit. Resulting NTF performs as shown in Fig. 3.13a and 3.13b. Because OSR is not high and the gain is only increased as it is required the zero sits on $z = 1$ but at close proximity. Pole location is kept inside the unit circle for stability and on the left hand plane for improved noise shaping performance. Fig. 3.13b further shows that in-band noise is much more alleviated than plain oversampling (indicated by the orange line)[3].

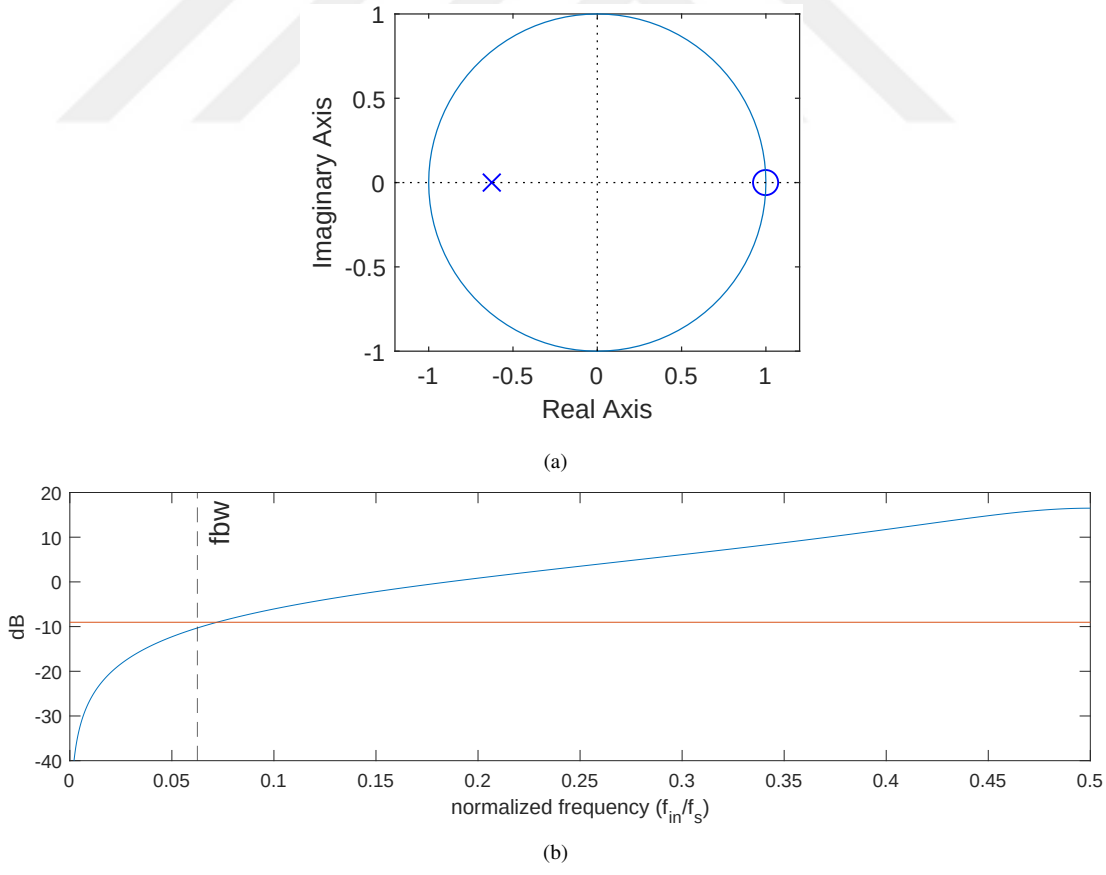


Figure 3.13 : a) Pole-zero placement b) and frequency response of the final NTF.

[3]Another advantage of noise shaping is that the comparator noise is also being shaped in addition to the quantization noise which is not the case for oversampling.

3.2.3 Inverter amplifier

Typically an integrator circuit consists of an operational amplifier which consumes too much power. However, due to its multi-bit nature of the NS-SAR, the residue voltage at the end of each conversion is a small quantity. Using this as an advantage this circuit uses a simple inverter as the linear amplifier by making sure its biased around its switching point with a unity feedback connection in the integrator scheme. The inverter size is kept small so that it consumes minimal power and its output capacitance is small ($C_{dd,p}+C_{dd,n} \simeq 22fF$) this ensures integration operation is compromised due to charge sharing at the output of the inverter and Cf-Cx capacitances). As a last point, opposite to a two-stage operational amplifier this circuit does not need any compensation to work in stability. From Table 3.2 can be seen that gain is always sufficient (more than 60 dB) and the power consumption never exceeds 14.5 μW for 1.8 V supply voltage.

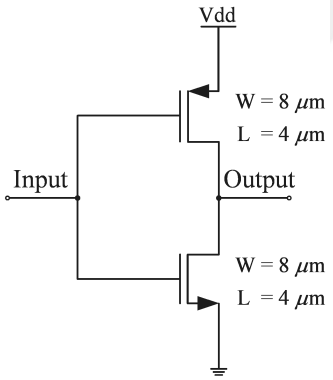


Figure 3.14 : The CMOS inverter sizes.

Table 3.2 : Inverter summary.

Process Corner	Gain	Unity-gain Frequency	Static Power Consumption
Typical	63.4 dB	680 MHz	10.3 μW
ss	62.9 dB	975 MHz	14.5 μW
ff	63.9 dB	465 MHz	7.13 μW

Although inverter has bad PSRR performance by having a low pass behavior for supply related noises it is shown in [11] that auto-zeroing applied for flickr noise also diminish low frequency supply noise and because inverter-based amplifier is in the loop its supply noise will also be shaped by the NS-SAR.

4. SIMULATION RESULTS

ADC performance is evaluated better in the frequency spectrum. For accurate and valid evaluations coherent sampling rules are followed. It is made sure that nth FFT bin corresponds to Fs/(# of FFT points). As explained in [16] Hanning is the optimum windowing function to minimize the magnitude of the error resulting from the convolution and also because of oversampling and windowing it is important to ensure that the input signal occupies less than 20% of the FFT bins. Thus, number of FFT points is chosen N = $64 \cdot OSR$ as advised.

The circuit is first simulated without the proposed noise shaping filter, Fig. 4.1 shows the frequency performance and Fig. 4.2 shows the output spectrum of the SAR only circuit. As summarized in Table 4.1, the 8-bit SAR circuit performs close to ideal for the Nyquist scenario and for the chosen bandwidth of 10 kHz the oversampled SAR achieves 1.36 bit extra resolution. This is the expected result as only oversampling adds $10\log(OSR)$ which adds 9 dB (1.5 bit) for OSR = 8. After that, the filter is attached and now the circuit performs the noise shaping which can be seen from Fig. 4.3. The circuit performs just as expected from the behavioral simulations (72 dB) as in the VerilogA case. Final results shows that 3.5 extra bits can be achieved by the novel noise shaping architecture which is more advantageous than plain oversampling.

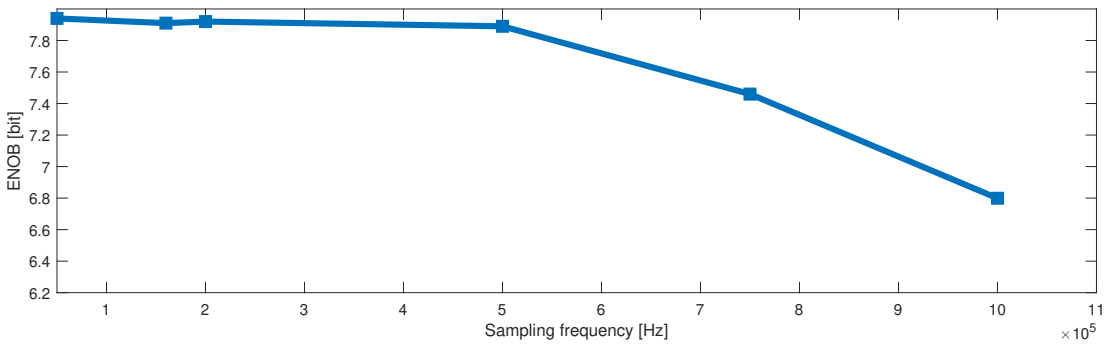


Figure 4.1 : SAR performance.

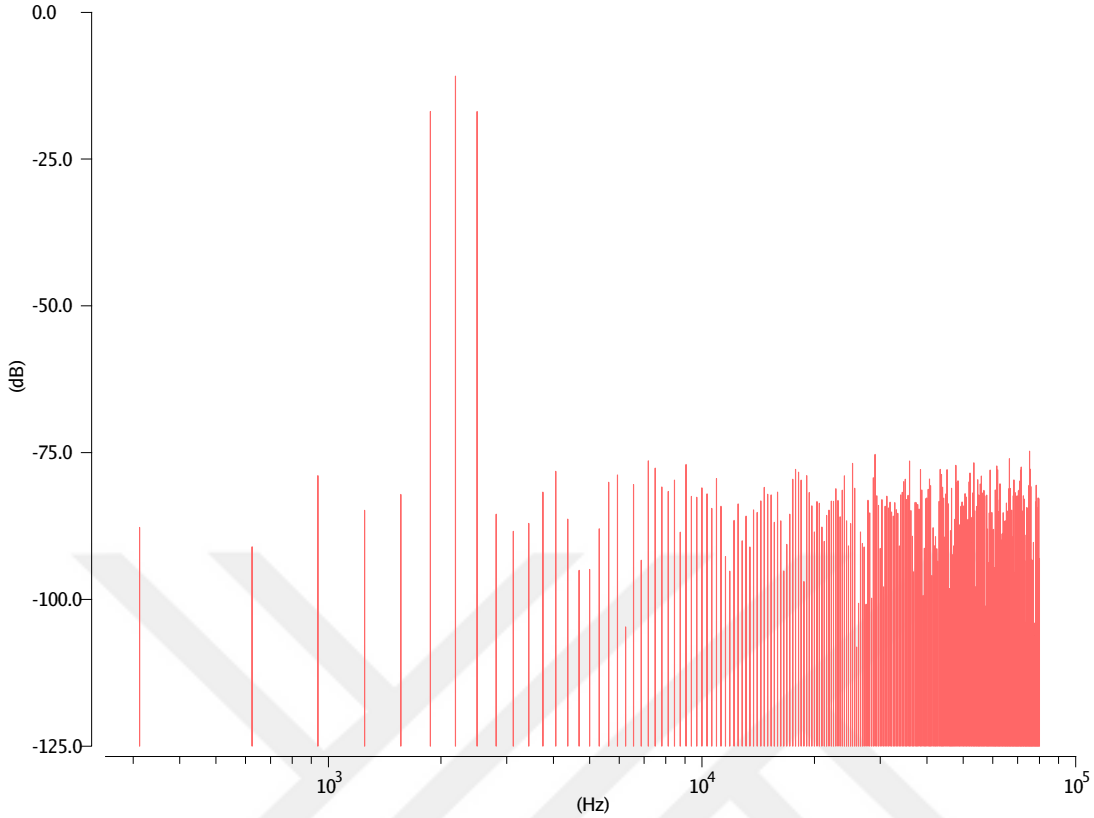


Figure 4.2 : SAR output spectrum.

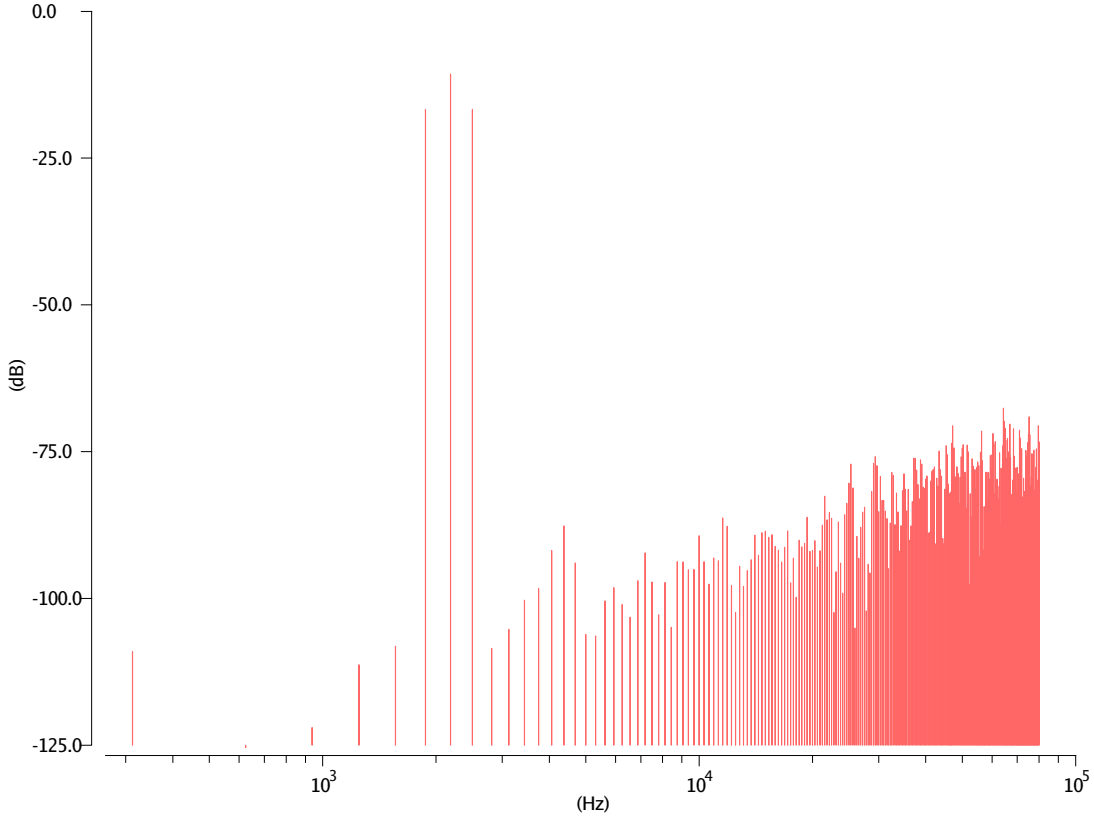


Figure 4.3 : Proposed NS-SAR output spectrum.

Table 4.1 : SAR vs. NS-SAR comparison.

Circuit	Fs	Fin	Bandwidth	SNDR	ENOB	SFDR
SAR	160 kHz	2.1875 kHz	80 kHz	49.39 dB	7.91	63.88 dB
SAR	160 kHz	2.1875 kHz	10 kHz	57.56 dB	9.27	65.55 dB
NS-SAR	160 kHz	2.1875 kHz	10 kHz	71.95 dB	**11.65**	75.60 dB

Power consumption of the different blocks of the proposed noise shaping converter is shown below in Table 4.2. It can be seen that the capacitive DAC is the most power hungry block as it is oversized to accommodate for the extra resolution. SC filter consumes 2.1 times of the total SAR power while providing extra 3.5 ENOB. It should be noted that, as slew rate analysis of the inverter-based amplifier is not incorporated its static current is kept at a safe value so that circuit operates consistently with the expected analytical results.

Table 4.2 : Power consumption breakdown of NS-SAR.

Block	Power Consumption	% of total
Comparator	316.4 nW	2.08 %
DAC	2.99 μW	19.7 %
SAR Logic	1.577 μW	10.4 %
SC Filter	10.3 μW	67.8 %
Total	15.18 μW	100 %

Lastly, Table 4.3 below shows that in all process corners the circuit can provide more than 11 ENOB and in same process corners circuit becomes more energy efficient if the temperature is dropped.

Table 4.3 : Corner results of NS-SAR.

	Typical	FF, 0 ^oC	SS, 0 ^oC	FF, 80 ^oC	SS, 80 ^oC
B_w	10 kHz	10 kHz	10 kHz	10 kHz	10 kHz
F_s	160 kHz	160 kHz	160 kHz	160 kHz	160 kHz
OSR	8	8	8	8	8
ENOB	11.65	11.84	11.54	11.62	11.40
Power	15.18 μ	18.23 μ	11.22 μ	21.31 μ	13.42 μ
FoM	231.2 f	249.8 f	187.2 f	338.6 f	239.9 f

5. CONCLUSION

An up to date literature review of the noise shaping SAR is done. The advantages and disadvantages of passive and active integrating NS-SAR circuits are discussed. It is explained that active integration lets the designer to change NTF parameters more freely and it is better suited for low frequency applications when the zero of the transfer function should be at $z = 1$.

The proposed novel circuit is shown and analyzed in dept with all the non-idealities its realistic noise transfer function is derived. Using these models as an advantage minimum oversampling ratio and capacitance ratios are determined. Pole location of the NTF is kept inside the unit circle to ensure stability. Following this the sub-circuits for the 8-bit SAR are designed. The unit capacitance is chosen by the DAC mismatch error as this puts a higher bound than the thermal noise consideration and the DAC is oversized for the targeted resolution rather than 8 bit scenario. The sampling switches are sized to made sure that voltage settling in adequate time can be expected during the operation. Comparator is also made sure to have stability and enough sensitivity so the operation runs smoothly. The SAR logic is designed such that the outcome of each decision is applied back to the DAC in order to left with the correct residue voltage.

Lastly, results of the proposed circuit is compared with the SAR only circuit. It is shown that even with a simple inverter-based amplifier first order noise shaping can be achieved by utilizing the multi-bit nature of the SAR architecture. Proposed circuit is shown to achieve 11.65 ENOB (71.95 dB SNDR) using a 8 bit SAR-ADC as the basis.

5.1 Discussion

Design summary and comparison with the ADCs having similar effective resolution is exhibited in Table 5.1. As the inverter-based amplifier used in the filter works as an AB class amplifier the circuit may have better efficiency at higher sampling rates but in order to increase the speed of operation a detailed analysis of the SC circuit parasitics and the amplifier's slew rate is paramount. After that, both the sampling

Table 5.1 : Performance summary and comparison.

* Measurement Results ** Simulation Results

Specification	VLSI' 12 [17]*	ISSCC' 20 [18]*	ESSCIRC' 16 [8]*	CICC' 17 [19]*	This Work**
Architecture	ΔΣ	SAR	NS-SAR	NS-SAR	NS-SAR
Technology (nm)	130	350	130	28	180
Supply Voltage (V)	1.2	4	1.2	0.8	1.8
Oversampling Ratio	8	1	8	8	8
Nyquist Rate (kS/s)	10000	25	250	3500	20
SNDR (dB)	70.7	54.1	74	68.1	71.95
Power (μW)	8100	0.82	61	70.5	15
FoM (fJ/conv.)	289.2	78.6	59.6	9.8	231.7

rate and the power consumption of the circuit can be further optimised to yield better energy efficiency. Mismatch results in Fig. 5.1 shows us that the circuit have $3\sigma = 0.41$ bits variation which is consistent with the DAC sizing strategy in the section 3.1.1 as the unit capacitance size is selected to establish mismatch error less than half an LSB at targeted resolution of 11 bits. Therefore, an additional calibration solution is not needed in this case.

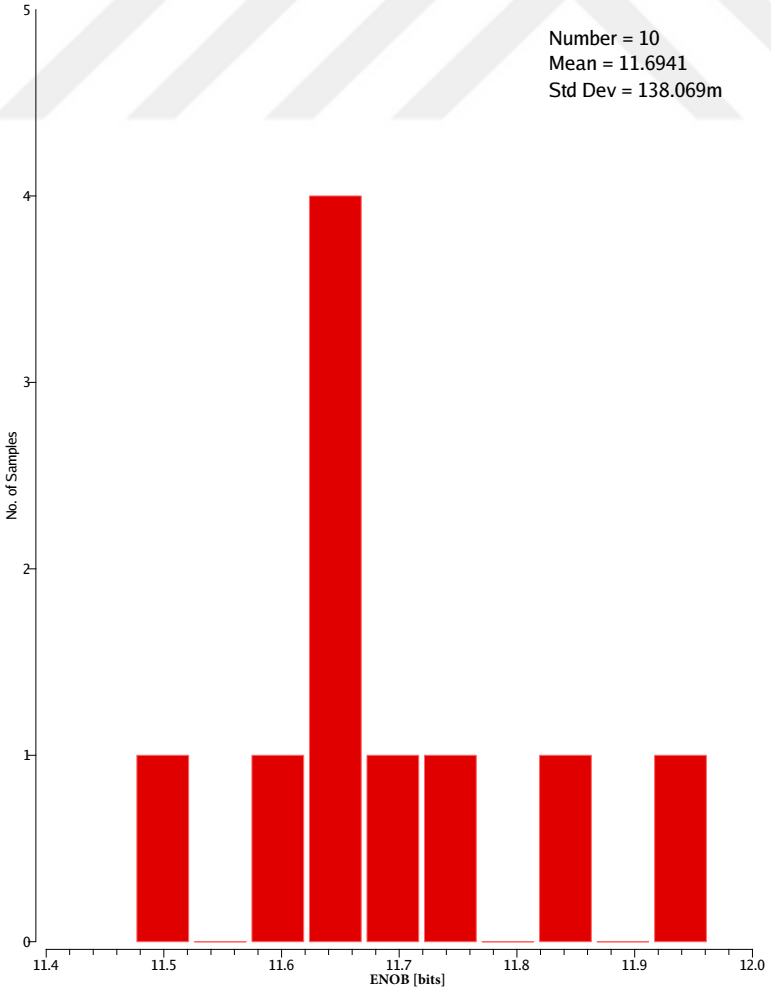


Figure 5.1 : Monte Carlo results (mismatch only).

5.2 Future Work

The ongoing research on the topic will be for the second order realization of the same SC filter idea and a calibration circuit for the DAC will be implemented so that the area advantage of the ADC will preserved and SNDR can be pushed even further.

Same design will be realized in a sub 100 nm technology using a lower supply voltage at a higher sampling frequency in order to achieve better energy efficiency.

By exploiting the multi-bit operation ‘dithering’ will be utilized for a cleaner output spectrum and higher dynamic range.

More detailed analysis will be done including the effects of inverter-based amplifier parasitics on the gain and speed error of the SC circuit so that optimum sizing of the inverter can be done possessing the minimum static current.

REFERENCES

[1] **Zhang, D.**, **Svensson, C. and Alvandpour, A.** (2011). Power consumption bounds for SAR ADCs, *2011 20th European Conference on Circuit Theory and Design (ECCTD)*, IEEE, pp.556–559.

[2] **Murmann, B.** ADC Performance Survey 1997–2020, 2020, *URL http://web. stanford. edu/murmann/adcsurvey. html*.

[3] **Kim, K.S.**, **Kim, J. and Cho, S.H.** (2010). nth-order multi-bit ΣΔ ADC using SAR quantiser, *Electronics letters*, *46*(19), 1315–1316.

[4] **Chen, Z.**, **Zhang, P.**, **Wei, H.**, **Sin, S.W.**, **Seng-Pan, U.**, **Martins, R.P. and Wang, Z.** (2011). Noise shaping implementation in two-step/SAR ADC architectures based on delayed quantization error, *2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, IEEE, pp.1–4.

[5] **Shahghasemi, M.**, **Inanlou, R. and Yavari, M.** (2014). An error-feedback noise-shaping SAR ADC in 90 nm CMOS, *Analog Integrated Circuits and Signal Processing*, *81*(3), 805–814.

[6] **Inanlou, R. and Yavari, M.** (2015). A simple structure for noise-shaping SAR ADC in 90 nm CMOS technology, *AEU-International Journal of Electronics and Communications*, *69*(8), 1085–1093.

[7] **Fredenburg, J.A. and Flynn, M.P.** (2012). A 90-ms/s 11-mhz-bandwidth 62-db sndr noise-shaping sar adc, *IEEE Journal of Solid-State Circuits*, *47*(12), 2898–2904.

[8] **Guo, W. and Sun, N.** (2016). A 12b-ENOB 61μW noise-shaping SAR ADC with a passive integrator, *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, IEEE, pp.405–408.

[9] **Lin, Y.Z.**, **Lin, C.Y.**, **Tsou, S.C.**, **Tsai, C.H. and Lu, C.H.** (2019). 20.2 A 40MHz-BW 320MS/s Passive Noise-Shaping SAR ADC With Passive Signal-Residue Summation in 14nm FinFET, *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*, IEEE, pp.330–332.

[10] **Zhuang, H.**, **Guo, W.**, **Liu, J.**, **Tang, H.**, **Zhu, Z.**, **Chen, L. and Sun, N.** (2019). A second-order noise-shaping SAR ADC with passive integrator and tri-level voting, *IEEE Journal of Solid-State Circuits*, *54*(6), 1636–1647.

[11] **Chae, Y. and Han, G.** (2009). Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator, *IEEE Journal of Solid-State Circuits*, *44*(2), 458–472.

[12] **Yue, X.** (2013). Determining the reliable minimum unit capacitance for the DAC capacitor array of SAR ADCs, *Microelectronics Journal*, *44*(6), 473–478.

[13] **Brenna, S.**, **Bonetti, A.**, **Bonfanti, A. and Lacaita, A.L.** (2015). A tool for the assisted design of charge redistribution SAR ADCs, *2015 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, IEEE, pp.1265–1268.

[14] **Pinto, A. and Fernandes, J.d.S.R.** (2013). A study on the offset voltage of dynamic comparators, *Proc. Des. Circuits Integr. Syst. 28th Ed*, pp.347–352.

[15] **Anderson, T.O.** (1972). Optimum Control Logic for Successive Approximation Analog-to-Digital Converters.

[16] **Pavan, S.**, **Schreier, R. and Temes, G.C.** (2017). *Understanding delta-sigma data converters*, John Wiley & Sons.

[17] **Oh, T.**, **Maghari, N. and Moon, U.K.** (2012). A 5MHz BW 70.7 dB SNDR noise-shaped two-step quantizer based ΔΣ ADC, *2012 Symposium on VLSI Circuits (VLSIC)*, IEEE, pp.162–163.

[18] **Jia, Y.**, **Guler, U.**, **Lai, Y.P.**, **Gong, Y.**, **Weber, A.**, **Li, W. and Ghovanloo, M.** (2020). 26.8 A Trimodal Wireless Implantable Neural Interface System-on-Chip, *2020 IEEE International Solid-State Circuits Conference-(ISSCC)*, IEEE, pp.414–416.

[19] **Garvik, H.**, **Wulff, C. and Ytterdal, T.** (2017). An 11.0 bit ENOB, 9.8 fJ/conv.-step noise-shaping SAR ADC calibrated by least squares estimation, *2017 IEEE Custom Integrated Circuits Conference (CICC)*, IEEE, pp.1–4.

APPENDICES

APPENDIX A.1 : Schematics
APPENDIX A.2 : Matlab and VerilogA Code

APPENDIX A.1 - Schematics

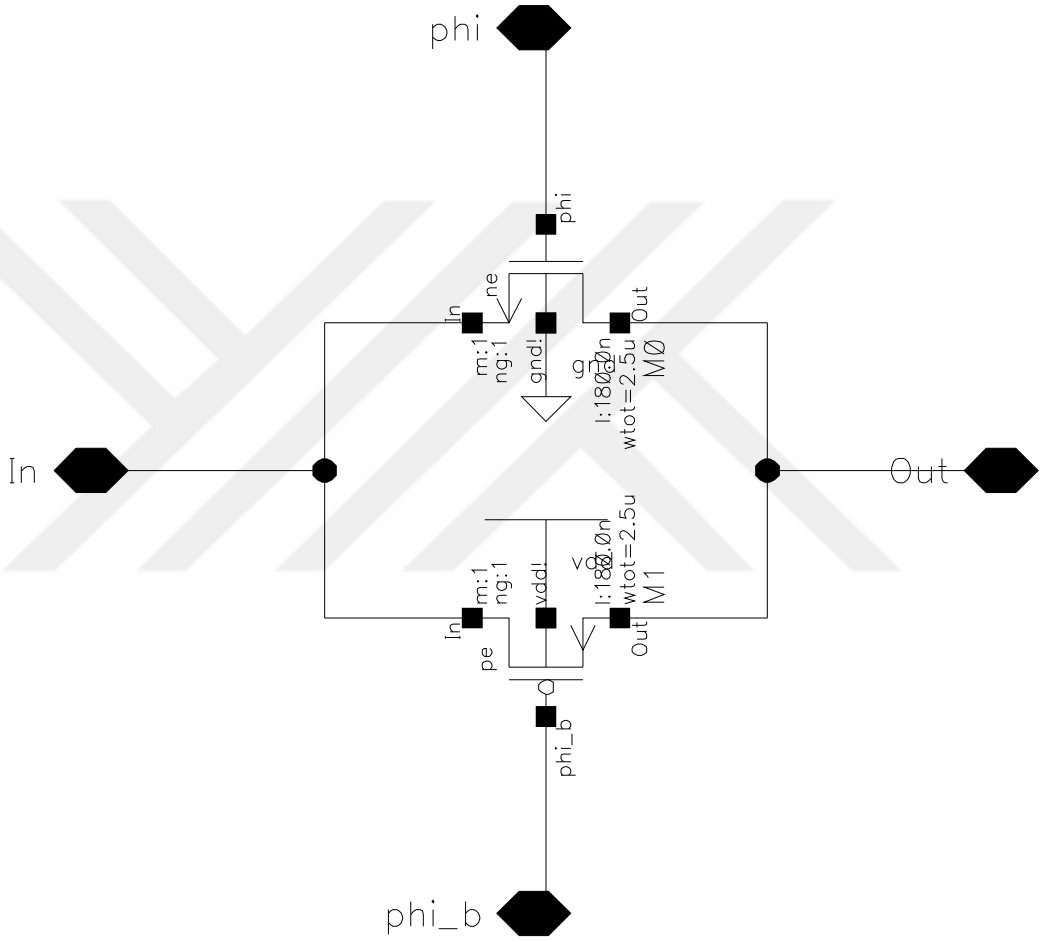


Figure A.1 : Transmission gate used as the switch.

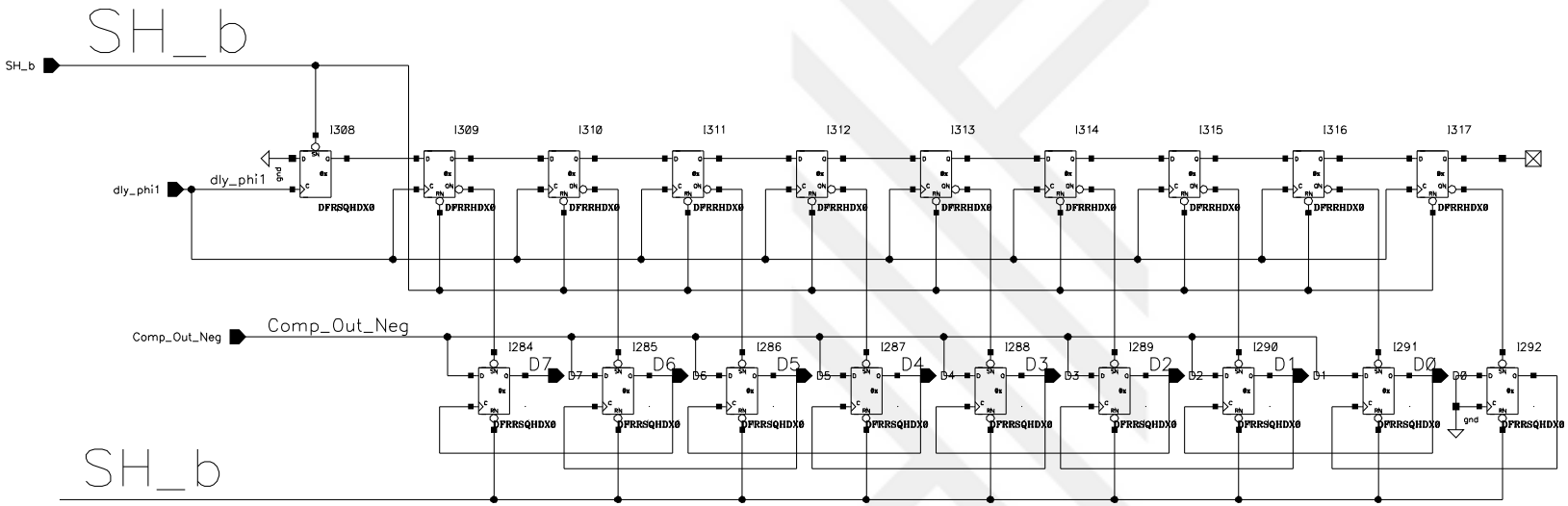


Figure A.2 : SAR logic schematic.

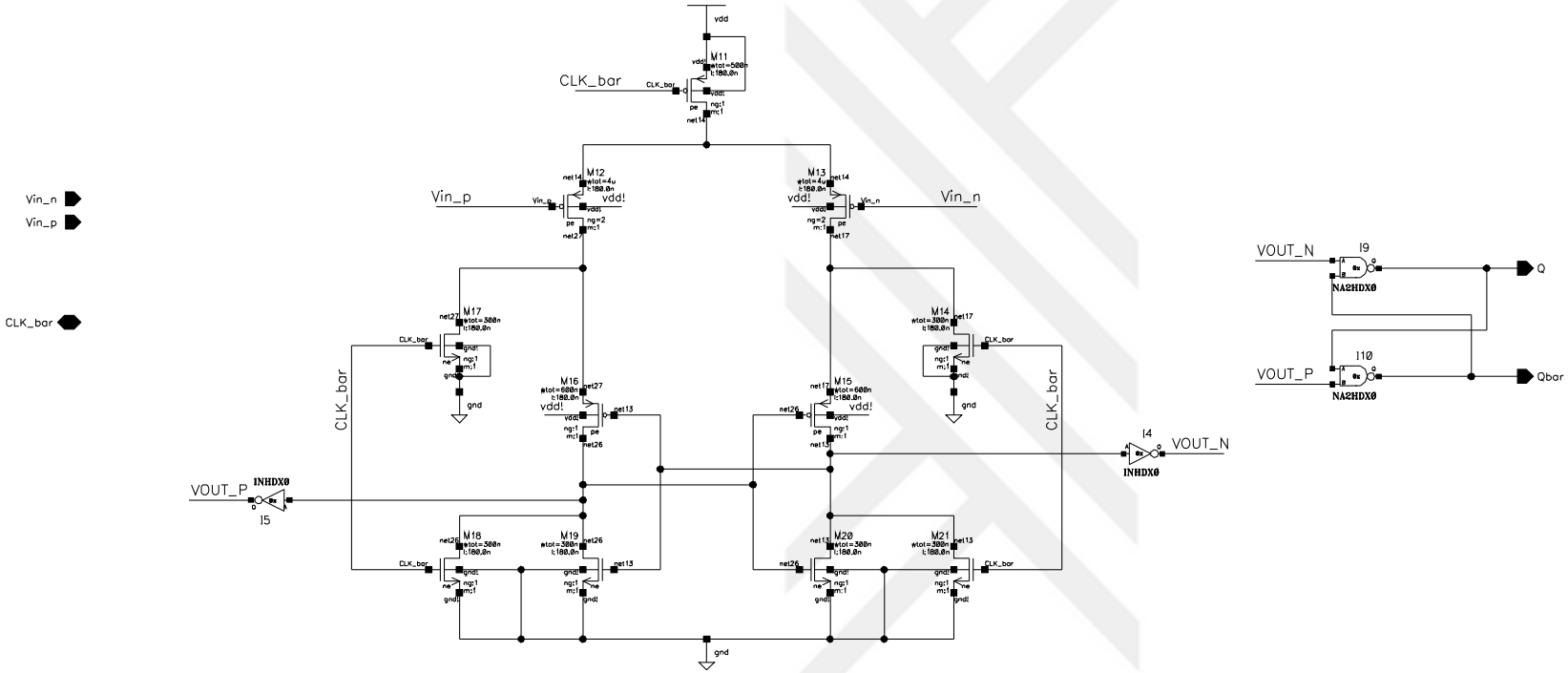


Figure A.3 : Comparator and NAND latch schematic.

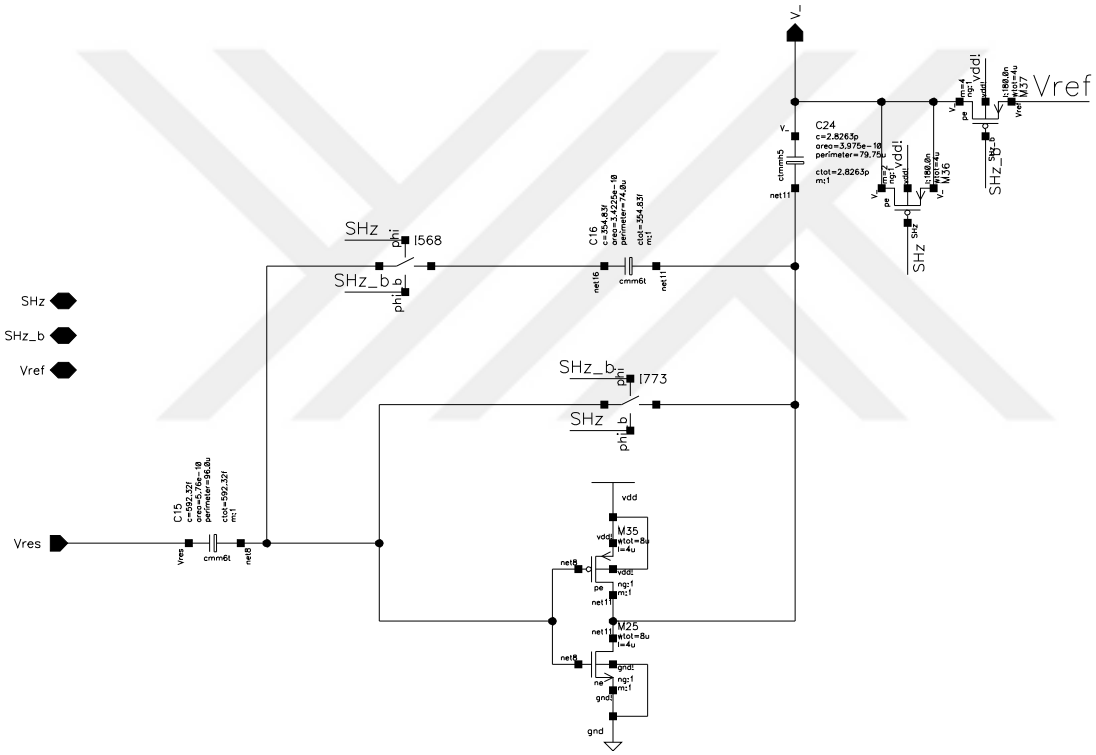


Figure A.4 : Proposed loop filter schematic.

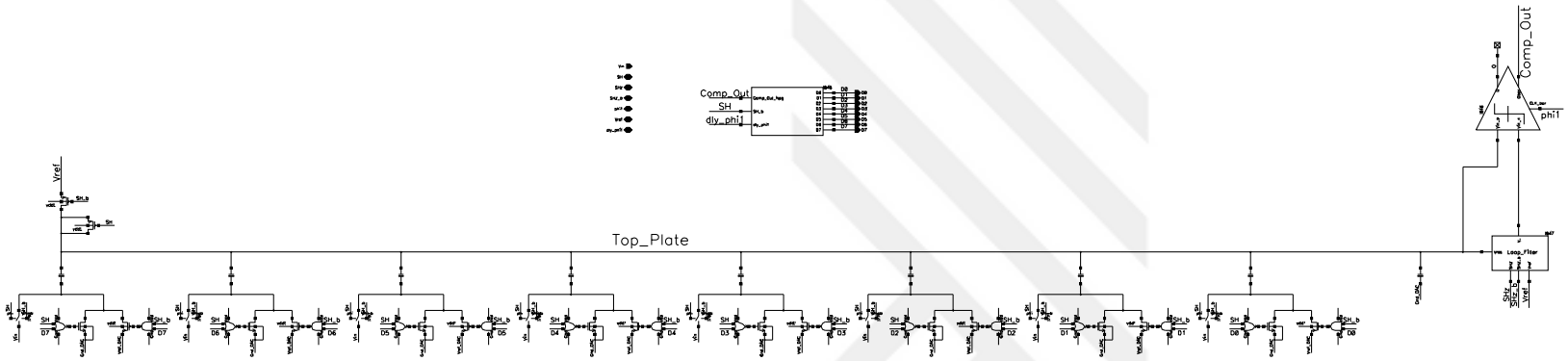


Figure A.5 : Proposed noise shaping SAR circuit.

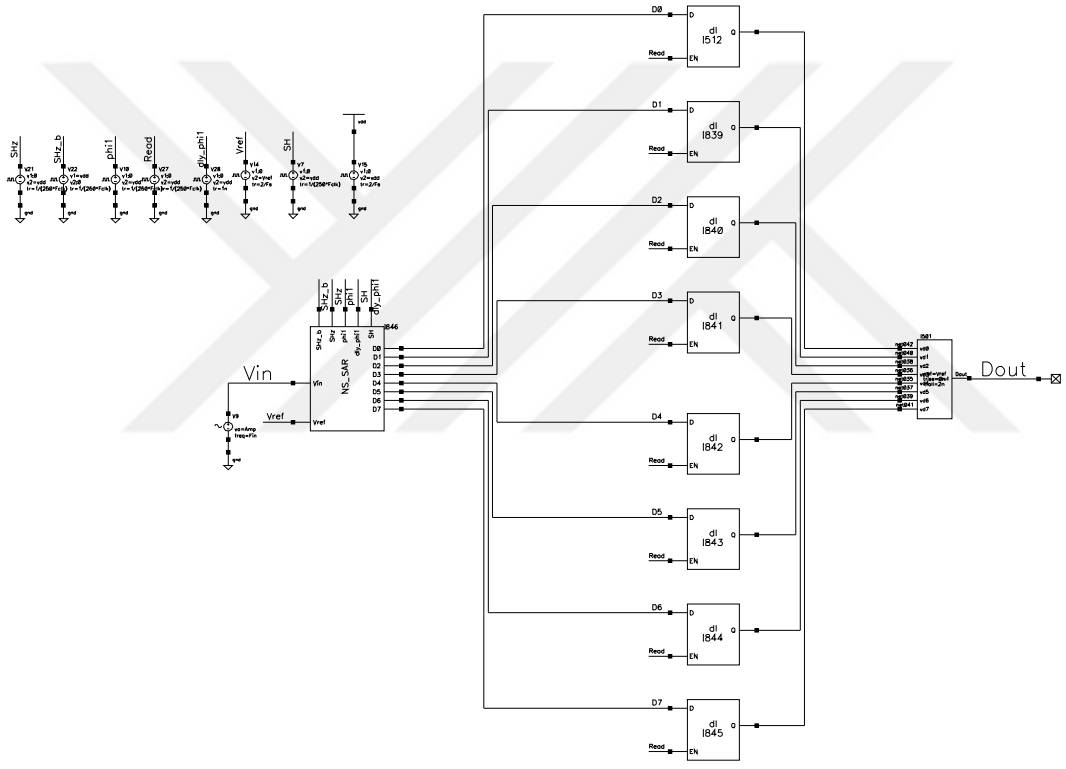


Figure A.6 : Test bench for the designed NS-SAR.

APPENDIX A.2 - Matlab and VerilogA Code

```
%Method in Determining the reliable minimum unit capacitance for the
%DAC capacitor array of SAR ADCs

%This analysis assumes a common centroid layout using 2^N unit caps

syms C

Kp = 0.0028; %Pelgrom Coefficient [um] x2 of this value can be used for
             %an imperfect or poor layout
Kc = 1e-15; %Capacitance per area [fF/um^2]
N = 8;  %Capacitive DAC Resolution [bits] (not target resolution)
sigma = Kp/sqrt(C/Kc);
extrabits = 3;
OSR = 8;
Vref = 1.2;
k = 1.38064852e-23; % [J/K]
T = 300; % Kelvin

Err_mismatch = ( (3*sigma*(sqrt(2^N)-1)) / ((sqrt(2)-1)*((2^N)-3*...
               sigma*sqrt(2^N))) )* Vref;

Err_thermal = 2*sqrt((k*T)/((2^N)*C*OSR));

eqn = Err_mismatch== Vref / (2^(N+1+extrabits));

Sol = solve(eqn,C);
Sol_double = double(Sol);
Mismatch = Sol_double(1,1)


eqn = Err_thermal == Vref / (2^(N+2+extrabits));

Sol = solve(eqn,C);
Sol_double = double(Sol);
Thermal = Sol_double(1,1)
```

```
% MATLAB Code for NTF Simulation %

Fs = 160e3; %Sampling Frequency
Ts = 1/Fs;
fbw = 10e3; %Input bandwidth
OSR = (Fs/2)/fbw; %Oversampling ratio

% NTF Parameters %
Alpha = 0.88;
```

```
Beta = 0.95;
Cs = 775e-15;
Cf = 500e-15;
Gain = 1000;

z = zpk('z', Ts);

numerator = ((Gain+1)/Gain)*Cf*(z-1)+(Cs/Gain)*z;
denominator = ((Gain+1)/Gain)*Cf*z+(Cs/Gain)*z-(((Gain+1)/Gain)*Cf-...
              Beta*Cs);
ntf = numerator/(Alpha*denominator);

Oversampling = -10*log10(OSR);

figure(1); clf;
set(gcf,'Position',[100 100 800 800])
subplot(2,1,1);
plotPZ(ntf);
f=linspace (0,0.5,10000); z=exp(2i*pi*f);
subplot(2,1,2);
plot(f, dbv(evalTF(ntf,z))); ylim([-40 20]); xlim([0 0.5])
xlabel('normalized frequency ($f_{in}/f_{s}$)'); ylabel('dB');
hold on;
plot(f,ones(size(f)) * Oversampling);
xline((fbw/Fs),'--',{'fbw'},'Fontsize',14);
```

```
// VerilogA for Ozan_NS_SAR, Z-domain_Integrator, veriloga

`include "constants.vams"
`include "disciplines.vams"

module Z_domain_Integrator(In,Out);

input In;
output Out;
electrical In, Out;

parameter real Beta = 1;
parameter real Gain = 100;
parameter real Cs = 10e-15;
parameter real Cf = 10e-15;
parameter real Ts = 10u from (0:inf);
parameter real firstSample = 1u;

analog begin

    V(Out) <+ (zi_nd((V(In)),{-Beta*Cs},{(Cs/Gain)+Cf*((Gain+1)/Gain),-Cf
    *((Gain+1)/Gain)},Ts,2n,firstSample));

end
endmodule
```

CURRICULUM VITAE

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PUBLICATIONS, PRESENTATIONS AND PATENTS ON THE THESIS:

OTHER PUBLICATIONS, PRESENTATIONS AND PATENTS:

- Güleç, H.O. and Yelten, M.B. (2019). A Cryogenic LC VCO Utilizing Cryogenic Models of Active Devices, *2019 6th International Conference on Electrical and Electronics Engineering (ICEEE)*, pp. 220-224. IEEE.