ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

A 65 nm CMOS LOW-POWER PHASE-LOCKED LOOP DESIGN FOR 5G NR78 MOBILE APPLICATIONS

M.Sc. THESIS

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Department of Electronics and Communications Engineering

Electronics Engineering Programme

JUNE 2025

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5G NR78 MOBİL UYGULAMALARI İÇİN 65 NM CMOS DÜŞÜK GÜÇ TÜKETİMLİ FAZ KİLİTLEMELİ DÖNGÜ TASARIMI

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To my mother and my grandmother,

FOREWORD

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ABBREVIATIONS

5G **:** The fifth generation
CP **:** Charge pump
CMOS **:** Complementary metal oxide semiconductor
dB **:** Decibel
dBc **:** Decibel relative to carrier
FoM **:** Figure of merit
GHz **:** Gigahertz
GPS **:** Global positioning system
KHz **:** Kilohertz
LF **:** Loop filter
MHz **:** Megahertz
NR **:** New radio
PFD **:** Phase frequency detector
PLL **:** Phase-locked loop
RF **:** Radio frequency
RMS **:** Root mean square
TDD **:** Time division duplexing
VCO **:** Voltage controlled oscillator

SYMBOLS

C	**:** Capacitance
L	**:** Inductance
P	**:** Power
t	**:** Time
R	**:** Resistance
W	**:** Watt
Ω	**:** Ohm
$\mathbf{g_m}$	**:** Transistor transconductance
Q	**:** Quality factor

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A 65 nm CMOS LOW-POWER PHASE-LOCKED LOOP DESIGN FOR 5G NR78 MOBILE APPLICATIONS

SUMMARY

The increasing demand for high-speed, low-latency communication in modern mobile systems necessitates the development of energy-efficient and high-performance frequency synthesizers. This thesis focuses on the design and analysis of a low-power phase-locked loop (PLL) architecture optimized for fifth-generation (5G) new radio (NR) n78 frequency band applications. The design is implemented using the Taiwan semiconductor manufacturing company (TSMC) 65nm complementary metal-oxide-semiconductor (CMOS) process and simulated via the Cadence Virtuoso.

The study begins with an overview of the fundamental importance of PLLs within radio frequency (RF) transceiver systems. Subsequently, the necessary background information regarding the targeted 5G NR n78 band standards for the design is provided. A theoretical background is also developed to establish a solid understanding of PLL operation, including loop dynamics and stability criteria. In the sequel, mathematical noise modeling and time- and frequency-domain analysis are used to study system behavior. Additionally, several other analysis are discussed to observe and enhance the performance of the loop. The design methodology involves constructing individual PLL building blocks, including the phase-frequency detector, charge pump, loop filter, voltage-controlled oscillator and frequency divider. Individual block analyses are discussed to improve overall system performance, with a particular focus on reducing the phase noise of the loop. Trade-offs among power consumption, phase noise, and supply sensitivity are also examined.

Following the successful design and simulation of each block, the components are integrated into a complete PLL loop. System-level simulations are conducted to verify functionality and evaluate performance against typical 5G standards. The design demonstrates effective trade-offs between power efficiency and noise performance. The implemented CMOS PLL effectively covers the n78 band with a 500 MHz tuning range and meets all the standard's requirements. This work is motivated by the lack of existing studies on CMOS-based PLLs explicitly designed for the n78 band in 5G NR systems according to literature review. The outcomes of the design architecture confirms the suitability for 5G n78 band applications. The final design achieves a phase noise of -116.8 dBc/Hz at 1 MHz offset and the total power consumption of 6.7968 mW.

5G NR78 MOBİL UYGULAMALARI İÇİN 65 nm CMOS DÜŞÜK GÜÇ TÜKETİMLİ FAZ KİLİTLEMELİ ÇEVRİM TASARIMI

ÖZET

Modern mobil sistemlerde yüksek hızlı ve düşük gecikmeli iletişim ihtiyacının artması, enerji açısından verimli ve yüksek performanslı frekans sentezleyicilerinin geliştirilmesini zorunlu kılmaktadır. Kablosuz haberleşmede artan kullanıcı sayısı ve talep edilen hızlı haberleşme, kararlı sistem dinamikleri ve düşük gecikme ihtiyacı yakın dönemde artmıştır. Bu kapsamda haberleşme sektöründe beşinci nesil (fifth generation, 5G) teknolojisini kullanan sistem sayısı artmıştır. Arz adeline zorlu sistem ihtiyaçları, 5G altyapısını kullanan kablosuz radyo frekansı (radio frequency, RF) alıcı sistemlerinin tasarımını zorlaştırmaktadır. Hem veri iletimi hem de veri alımı sırasında kullanılan faz kilitlemeli çevrim bloğu alıcı sistemlerinin en önemli bloklarından biridir. Faz kilitlemeli çevrim devreleri kablosuz sistemler ve 5G haberleşme uygulamalarında geniş kullanım alanına sahiptir. Kablosuz haberleşme sistemlerindeki ana görevi yerel osilatörün geniş bir frekans aralığında çalışmasını mümkün kılmaktır. Bu tez çalışması, 5G yeni radyo (new radio, NR) n78 frekans bandında çalışan uygulamalar için optimize edilmiş, düşük güçlü bir faz kilitlemeli çevrim mimarisinin tasarımına ve analizine odaklanmaktadır.

5G NR sistemlerinde n78 frekans bandı, 3300–3800 MHz aralığını kapsayan orta bant spektrumunda yer almakta olup, hem geniş kapsama alanı hem de yüksek veri iletim hızı arasında dengeli bir performans sunmaktadır. Özellikle yoğun kentleşmiş bölgelerde, n78 bandı sayesinde kullanıcı başına düşen bant genişliği artırılarak servis kalitesi iyileştirilebilmektedir. Ayrıca, bu frekans bandı küresel ölçekte birçok ülke tarafından benimsenmiş olup, cihaz ve altyapı uyumluluğu açısından da avantaj sağlamaktadır.

Faz kilitlemeli çevrim devreleri 5G haberleşme sistemlerinde, özellikle RF alıcı-verici yapılarında temel bir bileşen olarak görev yapmaktadır. Sinyal sentezleyici olarak işlev gören faz kilitlemeli çevrim sistemleri, hedef frekansta kararlı ve düşük gürültülü bir osilatör sinyali üretmekte kullanılır. Bu yönüyle, hem taşıyıcı frekans üretimi hem de kanal seçiminde yüksek doğruluk sağlar. n78 gibi yüksek frekanslı bantlarda, frekans kararlılığı ve spektral saflık gereksinimleri daha da belirgin hâle geldiğinden, faz kilitlemeli çevrim tasarımı doğrudan sistemin genel performansını etkiler. Ayrıca, 5G alıcı-verici mimarisinde farklı modlara hızlı geçiş ve geniş frekans kapsama alanı gerekliliği göz önüne alındığında, hızlı frekans ayarlama, düşük faz gürültüsü ve düşük güç tüketimi gibi kriterler doğrultusunda optimize edilmiş faz kilitlemeli çevrim yapıları, sistemin güvenilirliği açısından kritik rol oynamaktadır.

Faz kilitlemeli çevrim, geri beslemeye dayalı çalışan, sinyalin frekans ve fazını kontrol etmek amacıyla kullanılan temel bir elektronik sistemdir. Bu yapı faz algılayıcı, döngü filtresi, gerilimle kontrol edilen osilatör ve bir frekans bölücüden oluşur. Faz algılayıcı, referans sinyali ile osilatörden elde edilen çıkış sinyali arasındaki faz farkını tespit eder ve bu farkı temsil eden bir hata sinyali üretir. Üretilen bu sinyal, alçak geçiren filtre aracılığıyla düzeltilerek gerilimle kontrol edilen osilatör bloğuna yönlendirir. Bu giriş sinyali, osilatör frekansının değişmesine sebebiyet olur. Bu süreç, çıkış frekansının referans sinyali ile faz uyumu sağlayana kadar devam eder.

Çalışma içerisinde faz kilitlemeli çevrimin çalışma prensibini sağlam temellere oturtmak amacıyla kuramsal bir arka plan oluşturulmuştur. Döngü dinamikleri ve kararlılık kriterleri detaylı biçimde ele alınmıştır. Sistemin davranışı, zaman ve frekans düzleminde analizler ile birlikte matematiksel gürültü modellemeleri kullanılarak incelenmiştir. Sistemin performansını gözlemlemek ve iyileştirmek amacıyla çeşitli analizler gerçekleştirilmiştir. Tasarım metodolojisi; faz-frekans detektörü, şarj pompası, döngü filtresi, gerilim kontrollü osilatör ve frekans bölücü gibi faz kilitlemeli çevrim sistemlerinin ana bloklarının tasarımlarını içermektedir. Faz kilitlemeli çevrim sisteminin faz gürültüsünü azaltmak ve çalışma performansını iyileştirmek amacıyla her bir blok için ayrı analizler yapılmıştır. Güç tüketimi, faz gürültüsü ve besleme hassasiyeti gibi konular arasındaki tasarımda birbirine bağlı olan ilişkiler tartışılmıştır.

Faz kilitlemeli çevrim yapısında en kritik bloklardan biri olan indüktans-kapasitans (inductor-capacitor, LC) tabanlı gerilim kontrollü osilatör tasarımı, hem yüksek frekans doğruluğu hem de düşük faz gürültüsü sağlamak açısından büyük önem taşımaktadır. Ancak LC osilatör tasarımında karşılaşılan temel zorluklar, yüksek kalite faktörüne (quality, Q) sahip pasif bileşenlerin entegre devre düzeyinde gerçekleştirilmesi ve bu bileşenlerin oluşturduğu parazitik etkilerin azaltılmasıdır. Osilatörde kullanılan değişken kapasite elemanları, geniş frekans ayar aralığı sağlamak için vazgeçilmezdir; ancak bu yapı aynı zamanda faz gürültüsünü artırma riski taşır. Bu nedenle çalışmada, osilatör tasarımında düşük kazançlı ve ters çalışma bölgesinde çalışan N-kanallı metal-oksit yarı iletken (N-channel metal-oxide-semiconductor, NMOS) transistörler tercih edilerek hem frekans ayar genişliği artırılmış hem de faz gürültüsü iyileştirilmiştir. Ayrıca, sabit kapasitörlerin azaltılması ve indüktans değerinin yükseltilmesiyle güç tüketimi düşürülmüş; bu sayede performans ve enerji tüketimi arasında bir denge sağlanmıştır.

Şarj pompası ve faz-frekans detektörü, geri beslemeli döngünün kararlılığını ve kilitlenme süresini doğrudan etkileyen temel bileşenlerdir. Bu çalışmada, basit yapılı bir şarj pompası mimarisi tercih edilerek devre karmaşıklığı azaltılmış ve yüksek anahtarlama hızı ile düşük akım kullanımı sağlanmıştır. Döngü filtresi olarak ikinci dereceden ve hem tip II hem de tip III yapıya uyumlu bir analog filtre kullanılmıştır. Filtre, kararlılık açısını artırarak daha geniş bir faz marjı elde edilmesine olanak tanımaktadır. Faz-frekans detektörü, dinamik aralık ve düşük kilitlenme süresi açısından optimize edilmiş, sıfır gecikmeli çıkış üretimi hedeflenerek tasarlanmıştır. Tüm bu bloklar arasındaki sinyal bütünlüğünü sağlamak adına, düğüm kapasiteleri ve zaman sabitleri dikkatle belirlenmiştir. Böylece, düşük jitter ve hızlı kilitlenme performansı için tüm bileşenler arasında uyumlu bir çalışma sağlanmıştır.

Faz kilitlemeli çevrim sisteminin önemli bir bloğu olan frekans bölücü yapısı özellikle osilatörden gelen yüksek frekanslı sinyallerin daha düşük frekanslara dönüştürülmesinde temel rol oynamaktadır. Bu bağlamda kullanılan tasarım hem gecikme süresi hem de gürültüsüz bir sinyalin üretimi tasarım açısından çeşitli zorluklar içermektedir. Özellikle yüksek frekanslı sinyallerin doğru şekilde işlenebilmesi için giriş işaretine duyarlı hızlı tepki süresi ve en önemlisi yüksek frekansı bölücüden izole edebilecek yapılar tercih edilmelidir. Bu çalışmada, yarı saydam tetikleme yapıları ile donatılmış D tipi latch mimarileri kullanılarak bölücünün performansı artırılmıştır. Ayrıca osilatör ile bölücü arasına izolasyon devresi tercih edilmiştir. Dengeli yük paylaşımı ve simetrik geçiş süreleri sağlanarak, yüksek frekanslarda kararlı bir bölme işlemi gerçekleştirilmiştir.

Her bir bloğun başarılı bir şekilde tasarımı ve simülasyonunun ardından tüm bloklar tamamlayıcı bir faz kilitlemeli çevrim sistemi için entegre edilmiştir. Tasarım, Tayvan yarı iletken üretim şirketi (Taiwan semiconductor manufacturing company, TSMC) 65 nm tamamlayıcı metal-oksit yarı iletken (complementary metal-oxide-semiconductor, CMOS) teknolojisi kullanılarak gerçekleştirilmiş ve Cadence Virtuoso aracı ile simüle edilmiştir. Sistem seviyesinde simülasyonlar gerçekleştirilerek genel işlevsellik doğrulanmış ve tasarımın 5G standartlarıyla uyumu değerlendirilmiştir. Mevcut akademik çalışmalar incelendiğinde, n78 frekans bandı için özel olarak geliştirilmiş CMOS tabanlı faz kilitlemeli çevrim çalışmasına rastlanmamıştır. Tasarım, güç tüketimi ile gürültü performansı arasında etkili bir denge sağlamaktadır. Tasarlanan CMOS faz kilitlemeli çevrim sistemi 500 MHz ayarlanabilir frekans aralığını çalışarak n78 bandını etkin şekilde kapsamaktadır ve ilgili standartların tüm gerekliliklerini karşılamaktadır. Elde edilen sonuçlar, tasarlanan mimarinin 5G n78 bandı uygulamaları için uygunluğunu doğrulamaktadır. Nihai tasarım, 1 MHz sapma frekansında -116.8 dBc/Hz faz gürültüsü ve 6.7968 mW toplam güç tüketimi ile başarılı performans göstermektedir.

1. INTRODUCTION

This chapter outlines the objectives and motivation of the thesis. Additionally, it presents the literature review and the structure of the thesis.

1.1 Purpose of Thesis

Wireless communication systems for mobile applications have been developing rapidly, becoming more robust, power-efficient, and capable of maintaining low latency. Advancements in the technology have enabled significantly higher data rates, improved connectivity and faster response times. To meet these performance targets, the telecommunication industry has advanced into the fifth-generation (5G) mobile systems. The 5G era introduces a wide range of frequencies, including sub-6 GHz and millimeter-wave bands, to facilitate enhanced mobile broadband. Specifically, 5G mobile applications in Europe mainly operate within the new radio (NR) frequency band n78. This band, as defined by the 3rd Generation Partnership Project (3GPP), employs in the frequency range of 3.3 GHz to 3.8 GHz [1]. These frequency allocations requires advanced radio frequency (RF) front-end architectures. The RF transceivers ensure the signal integrity and synchronization to transmit and receive across the designated frequency bands. One of the core building blocks in such systems is the phase-locked loop (PLL), which provides precise frequency synthesis and timing control. In particular, PLLs are essential for generating stable local oscillator signals which enables frequency translation in both transmitters and receivers. The PLL directly impacts the overall transceiver efficiency and spectral compliance in such applications. Therefore, a deep investigation of PLL design is vital in 5G mobile systems is vital due to its crucial role inside RF chain.

PLLs must exhibit low phase noise and fast settling time to ensure stable communication within the medium and it must provide minimal signal distortion. Phase noise affects the purity of the carrier signal and can degrade system performance that leads to increased bit error rate and reduced modulation accuracy. Settling time, on the other hand, is a critical parameter that must be minimized to enable fast channel

switching and reliable synchronization in high-speed 5G systems. Thus, optimizing PLL structure for low phase noise and fast settling time is essential to support the requirements of 5G communication.

Power consumption is another crucial consideration in PLL design for 5G mobile applications. Energy-efficient circuits without sacrificing performance are vital in mobile devices as they rely on battery power. Moreover, 5G network elements such as small-cell base stations require low power systems while supporting targeted performance metrics. Due to the challenging implementation environment of 5G components, the power budget enforces stringent constraints on each components within the RF chain, including the PLL; therefore, the need for energy-efficient design without compromising performance becomes imperative.

Furthermore, 5G applications demand multi-band transceivers capable of switching between different frequency bands either in transmitting or receiving mode. These switching modes between frequencies arise from the ability of 5G to support multiple devices simultaneously. Therefore, PLLs must operate efficiently over wide frequency ranges. This increases the complexity in the design stage as the loop must remain stable and responsive across a wide range of frequencies.

To address these challenges, various circuit strategies have been proposed in recent years. Phase noise performance in PLLs is analyzed by investigating each building blocks. The primary contributor to phase noise in PLLs is the voltage-controlled oscillator (VCO), a core building block which is responsible for generating the oscillation signal.

An analog PLL, as studied in [2], offers an effective noise reduction method. The proposed design lowers the gain of the LC VCO to mitigate the noise arises from AM-to-FM conversion in varactors. Furthermore, the topology recommends reducing the fixed capacitors in the LC tank to decrease both power consumption and phase noise. However, this approach results in an increase in the inductor size to maintain the desired resonance frequency. Therefore, a trade-off between noise performance, power consumption, and component sizing is required.

Another approach utilizing LC VCO studied in [3] employs a complementary cross-coupled VCO which uses an efficient noise filtering technique to alter the phase noise issue. The structure provides a good tuning range while exploiting a current reuse

mechanism to alter the power consumption. Additionally, the overall phase noise is also altered by placing a high Q common-mode harmonic resonance.

On the other hand, [4] proposes the use of a ring oscillator within the PLL. The ring oscillator benefits from reduced sizing and offers an increased tuning frequency range. Moreover, the methodology provides the advantage of generating multi-phase output signals by employing a 5-stage differential ring oscillator. The increased number of stages in ring oscillator also contributes to phase noise reduction. However, this configuration results in higher power consumption due to the inherent characteristics of ring oscillators.

Although ring oscillator-based VCOs offer advantages such as reduced area consumption and lower production costs, LC-based VCOs provide significantly better phase noise performance. According to the study in [5], LC VCOs exhibit superior trade-offs between phase noise and power consumption compared to ring oscillators. Despite their inherently lower tuning range, LC VCOs achieve improved phase noise performance under similar power consumption conditions.

Furthermore, the study in [6] introduces an additional noise suppression technique for LC oscillators, which employs a high-Q resonator inductor with a fixed capacitor and a noise filter tuned to the second harmonic of the VCO. This configuration effectively reduces phase noise and provides an enhanced conversion gain. In contrast, the topology introduces complexity in designing stage and increases overall power consumption.

An LC VCO design studied in [7] suggests utilizing capacitor banks to increase the frequency tuning range. The inclusion of capacitor banks within the LC tank results in a wider tunable range. However, incorporating these capacitors introduces additional parasitic effects, which can degrade the phase noise performance and increase power consumption. Although the design effectively addresses phase noise and power constraints by biasing the MOSFETs in the inversion region, this approach leads to a longer settling time.

The settling time in PLL is mainly controlled by the loop bandwidth and the damping factor which are determined by the parameters from the loop filter and charge pump (CP). As studied in [8], designing a second-order loop filter for a PLL contributes to a faster settling time compared to first-order filters. Moreover, second-order filters can

better optimize the trade-off between settling time and phase noise thus, ensuring robust performance under the stringent demands of 5G communication systems.

The loop bandwidth of a PLL can be expanded through the adaptive scheme proposed in [9]. In this study, a gear-shifting approach is implemented within the PLL architecture to dynamically adjust the reference frequency which enhances the loop bandwidth. This adaptive increase in reference frequency leads to a faster settling time, improving the overall responsiveness and performance of the PLL. However, the approach relies on a dual-divider topology, one for the reference path and another for the VCO, which introduces additional design complexity and increases power consumption due to the extra divider circuitry introduced in the reference path.

Frequency divider within PLLs are also among the most power-hungry building blocks. In conventional PLL architectures, the frequency divider operates near the VCO output frequency. Since the divider is often partially or fully digital in nature, they undesirable consume high power. Furthermore, the requirement for fractional division to achieve frequency resolution further increases the power demand. To reduce the power consumption of the divider while maintaining fast and accurate frequency division, [10] proposes the use of a multi-modulus prescaler which enables flexible division ratios and efficient operation at high frequencies. The pre-scaler stage performs a digital division by 2 within the feedback loop, effectively reducing the overall power consumption of the frequency divider to some extent.

Another notable approach, presented in [11], introduces a pulse-swallow frequency divider that incorporates an injection-locked frequency divider (ILFD) as the initial stage of the feedback loop. This method achieves lower power consumption compared to conventional digital alternatives.

Dividing the high-frequency output of a VCO down to the reference frequency level can be challenging due to potential delays introduced by the division speed. The approach presented in [12] offers a balanced solution by combining dynamic charge-sharing logic dividers with fully static architectures. Dynamic dividers demonstrate superior performance at high frequencies, enabling higher operating speeds. In contrast, a fully static architecture is employed at the lower frequency stages to reduce overall power consumption compared to dynamic dividers.

In summary, a PLL is a crucial building block in advanced RF front-end architectures. The design of PLLs for 5G applications must address strict requirements for low phase noise, fast settling time, and minimal power consumption. Meeting these demands is essential for ensuring reliable frequency synthesis and stable signal generation in high-speed mobile communication systems.

This thesis focuses on the design of a low-power PLL architecture optimized for 5G NR band n78 mobile communication systems. The academic contribution of this thesis lies in addressing a gap in the literature, where no CMOS-based PLL designs have been explicitly developed for the n78 band within the context of 5G NR systems. The primary objectives of this work are to achieve low phase noise, minimal power consumption, and fast settling time behavior while ensuring compatibility with 5G requirements. The design considers practical trade-offs between noise performance, power, and stability, and aims to contribute to the development of reliable and efficient RF front-ends for next-generation wireless communication.

The organization of this thesis begins with an overview of 5G communication standards in Chapter 2. This chapter focuses on the frequency allocations and system requirements for the n78 band. In addition, it provides fundamentals of RF transceiver architectures and highlights the critical role of the PLL. Chapter 3 presents the theoretical background of PLLs. It includes PLLs types and loop dynamics by analyzing the transfer functions of the loop. It also provides stability analysis in s-domain using Bode plots and root locus. In Chapter 4, a detailed phase noise modeling of PLL components is provided, emphasizing design considerations and performance metrics. Chapter 5 introduces the circuit implementations of the PLL core blocks, such as the Phase-Frequency Detector, Charge Pump, Loop Filter, VCO, and Frequency Divider. This section also includes the simulation results corresponding to each block that is individually examined. Chapter 6 presents the integration of the individual blocks into a complete PLL system, along with the simulation results, performance evaluations, and comparisons with existing designs. Finally, Chapter 7 concludes the thesis by summarizing the key findings, discussing potential improvements and suggesting directions for future research.

2. COMMUNICATION BACKGROUND

Wireless communication in 5G has been utilized in market in recent years. High-speed wireless data transmission supports various frequency bands within standards of system performance. This chapter aims to build general background about the targeted 5G standard. The frequency allocations within 5G will be discussed and system requirements of the n78 band will be presented. Finally, the fundamental information about the importance of PLL in RF tranceiver systems will be covered as well.

Compared to previous generations such as 3G and 4G, 5G offers significantly higher spectral efficiency, reduced end-to-end latency, and support for a broader variety of use cases. While earlier generations primarily focused on voice and mobile data services, 5G is designed as a flexible and scalable platform to address both consumer and industrial demands in a unified network architecture. These applications include enhanced mobile broadband (eMBB), ultra-reliable low-latency communication (URLLC), and massive machine-type communication (mMTC). In practical use, 5G enables seamless user experiences in applications such as augmented reality (AR), autonomous vehicles, industrial automation, and user equipment (UE)-level services such as Internet of Things (IoT) applications and mobile applications.

Mobile applications developed for 5G telecommunication systems are standardized by the 3GPP in [1]. These standards define the framework for achieving higher data throughput, ultra-reliable low latency communication and expanded frequency spectrum. 5G operates across two main frequency bands called frequency range 1 (FR1) and frequency range 2 (FR2) which cover sub-6 GHz bands and milimeter waves respectively. These bands are also divided into multiple frequency ranges named NR frequency bands defined by the 3GPP [1]. The low-band spectrum of FR1, frequency range below 1 GHz, is used for broad coverage which is suitable for wide-area and rural deployments. The mid-band spectrum of FR1, ranging from 1 GHz to 6 GHz, provides a balanced trade-off between coverage and capacity. These ranges are widely adopted in urban and suburban areas for enhanced data rates. Lastly, FR2 operates above 24 GHz which enables ultra-high-speed data transmission and massive network capacity however it suffers from limited range.

NR bands also define the operating frequencies for the targeted applications along with the duplex schemes. The duplex schemes are used to define the seperation of transmission and reception paths required for continuous two-way data communication. In a communication system, data transmission and receiving must occur without interfering with each other to ensure reliable biderectional communication. 5G systems utilize various duplexing techniques: Supplementary downlink (SDL), supplementary uplink (SUL), frequency division duplexing (FDD) and time division duplexing (TDD). In SDL, additional downlink frequency bands are allocated without a corresponding uplink band. SDL is used for the applications which are suffering from heavy downlink traffic. Conversely, SUL provides extra uplink bandwidth without a paired downlink channel to enhance uplink coverage. This is particularly beneficial for devices with limited transmission power.

FDD assigns separate frequency bands for uplink and downlink hence allowing simultaneous transmission and reception. This method is particularly effective for symmetric data communication. In contrast, TDD utilizes a single frequency band for both uplink and downlink by dividing the communication over time slots in the time domain. This technique benefits applications using asymmetric data traffic patterns. TDD also offers flexibility in adjusting uplink and downlink time slots based on traffic demand, therefore it allows dynamic resource allocation. FR1 is elligiable for all duplex schemes mentioned above whereas FR2 supports only TDD due to its suitability for short-range microwave applications. While FDD is still prevalent in lower frequency bands due to its suitability for symmetric traffic, TDD has gained wider adoption in higher frequencies, particularly where data traffic is more asymmetric and bursty.

These duplexing techniques are tied to the allocation and utilization of NR frequency bands. Cellular applications within 5G commonly utilizes TDD for both FR1 and FR2 [1] which is standardized to support various deployment scenarios across regions. The usage of NR bands within FR1 for mobile applications varies depending on the regional requirements and restrictions of the targeted area. For instance, deployments within Europe utilize specific NR bands as presented in Table 2.1. These bands provide coverage for 5G networks, as well as support for 4G and LTE applications. The selection of these bands ensures compatibility with regional spectrum allocations and regulatory requirements.

Table 2.1 : 5G NR bands utilized in cellular networks in Europe with corresponding frequency allocations.

NR Band	Uplink (MHz)	Downlink (MHz)
n1	832-862	791-821
n3	1920-1980	2110-2170
n7	1710-1785	1805-1880
n20	2500-2570	2620-2690
n78	3300-3800	3300-3800

The final key specification for 5G applications is the channel bandwidth which affects the data throughput and overall efficiency of the communication system. In the 5G NR standard, flexible channel bandwidth configurations are defined to accommodate various deployment scenarios across different frequency ranges.

Within FR1 channel bandwidths allows reliable service in both low and mid-band spectrums as it can range from 5 MHz to 100 MHz. On the contrary, the channel bandwidth for FR2 can extend from 50 MHz up to 2000 MHz. This expansive bandwidth capability enables ultra-high-speed data transmission. The adaptability in bandwidth configurations ensures that 5G networks can be tailored to meet diverse performance requirements and spectrum allocations across regions. These wider bandwidths are critical for achieving the peak data rates and low-latency performance targeted by 5G. Furthermore, the channel bandwidth configuration must be compatible with TDD schemes to ensure fast and accurate switching between uplink and downlink transmissions. For design considerations, this implies that the oscillator and filtering components must deliver stable performance and low phase noise across the entire operating frequency spectrum.

Wide-range frequency allocations in 5G requires advanced RF front-end architectures. Traditional RF transceivers are designed to transmit and receive signals across the designated frequency bands. RF transceiver block presented in Figure 2.1 which consists of power amplifiers (PAs), low-noise amplifiers (LNAs), filters, mixers, a PLL for local oscillation and modulation units.

PAs is used for boosting the strength of the transmitted RF signal to ensure it can travel over long distances. On the receiver side, LNAs are used to amplify weak incoming signals from the antenna while minimizing the noise. Mixers in the transmitter path up-convert the baseband signals to the desired RF transmission frequency, while in the receiver path, they down-convert the high-frequency RF signals to lower frequencies

suitable for demodulation and further processing. As a critical building block of RF transceiver, PLL generates stable oscillation signals for both transmitter and receiver chains. Lastly, modulation units are responsible to modulate the baseband signal in the transmiting path and processes the filtered baseband signal in the receiver path.

The inevitable need of PLLs in both transmiting and receiving paths makes accurate PLL designs fundamental to ensure that the targeted frequency band is synthesized reliably and efficiently. The design of each block inside RF transceiver can vary in accordance to 3GPP NR bands standards. The PLL needs to support wide frequency bands, operate under channel conditions, and maintain power and noise trade-off.

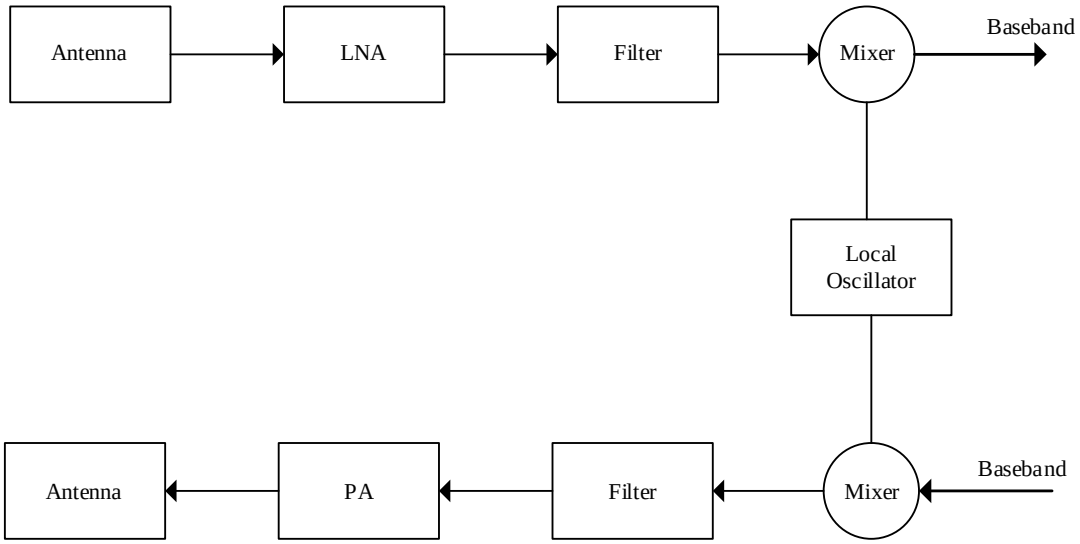

Figure 2.1 : High-level block diagram of an RF transceiver.

As stated in Chapter 1, this thesis focuses on designing a PLL architecture suitable for the n78 band which operates between 3.3 GHz and 3.8 GHz with a 500 MHz bandwidth under FR1. The n78 band utilizes TDD duplex scheme. The duplex scheme directly influences the design requirements of RF front-end components, including the PLL, as it affects frequency planning, and interference management.

Apart from that, the supported channel bandwidths include 10, 15, 20, 30, 40, 50, 60, 70, 80, 90, and 100 MHz. These channel bandwidths for a PLL system determine the frequency of reference signal. Hence, the preferred channel bandwidth is 10 MHz selected. Table 2.2 summarizes the specifications required to design a PLL for 5G NR band n78.

Table 2.2 : The design specifications.

Parameter	Specification
Band Name	n78
Operating Frequency	3.3 GHz – 3.8 GHz
Duplex Mode	Time Division Duplex
Channel Bandwidth	10 MHz
Phase Noise	<-100 dBc/Hz at 1 Mhz
Power	<10 mW
Settling Time	< 10 μs
Output Jitter (rms)	<500 fs (10 kHz – 100 MHz)

3. PLL LOOP DYNAMICS

This chapter presents background information about phase-locked loop (PLL) covering its working principle, types and performance analysis.

3.1 Overview of Phase-Locked Loop

PLLs are feedback loop systems that operate on the excess phase of nominally periodic signals. PLL circuits provide voltage-controlled oscillation to RF transceivers in one or multiple different frequency ranges. PLL systems, as depicted in Figure 3.1, are composed of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO) and a frequency divider (FD).

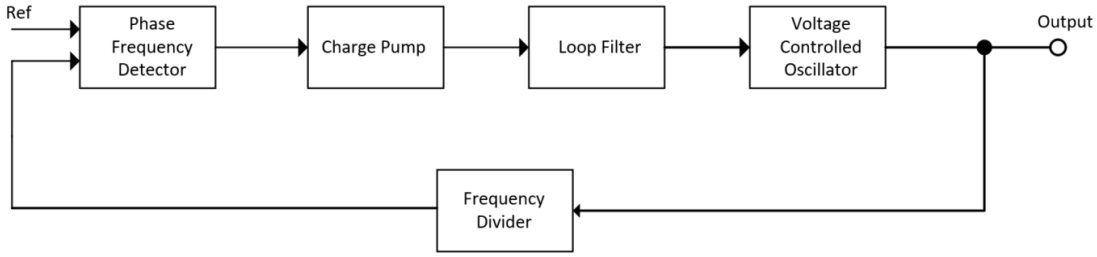

Figure 3.1 : Phase-locked loop block diagram.

The PFD detects the phase and the frequency of the feedback loop signal and compares with the applied reference signal. The feedback loop signal is a portion of the VCO signal which is divided into the desired reference frequency by FD and is fed back to the PFD. If there exists any phase or frequency difference between the feedback loop signal and the reference signal, the PFD generates an output which is proportional to the relative phase or frequency difference of these signals. This error signal is then applied to CP to provide necessary voltage level to VCO. The CP either raises or lowers the voltage levels to differentiate phase or frequency leading or lagging information, thus the oscillation is controlled. The output of CP is filtered by LF and applied to the VCO. This signal controls the VCO to increase or decrease its output frequency until when the error signal from PFD is constant which results that the phase and frequency of the reference signal and the feedback loop signal match each other and the loop considered locked.

3.2 Transfer Functions

PLL circuits are non-linear control systems because PLLs have non-linear blocks such as PFD and VCOs. Even though the non-linearity behaviour of PLLs exists, a linear approximation can be used to understand PLLs' performance. Figure 3.2 presents the transfer function of a simple PLL block diagram. Each building block represented with its linear models. The divider is excluded for simplicity purpose.

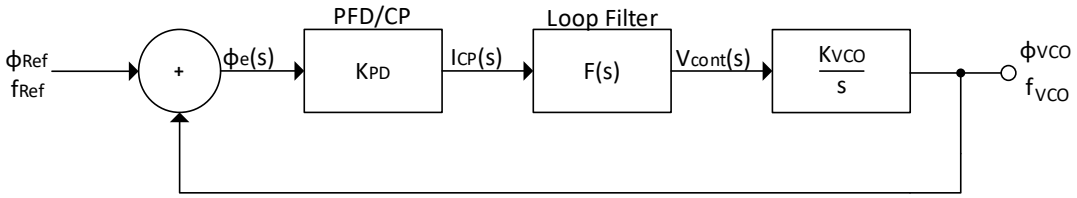

Figure 3.2 : Linear representation of a phase-locked loop.

The output signal of PFD is proportional to its inputs coming from reference signal and output of VCO and is given by

$$V_{PD} = K_{PD}(\varphi_{REF} - \varphi_{VCO}) \tag{3.1}$$

where K_{PD} is called the phase-detector gain factor and has a unit of V/rad.

A low-pass filter commonly is used as a loop filter in a typical PLL circuits in order to smooth the control signal and reduce the noise. The transfer function of the loop filter is F(s). The filtered output voltage, V_{cont}, is applied to VCO to control the oscillation. An ideal VCO generates a periodic output signal with a frequency of which is a linear function of its control voltage V_{cont} and depicted as

$$\omega_{VCO} = \omega_0 + K_{VCO}V_{cont} \tag{3.2}$$

where ω_{out} is the output frequency of VCO, K_{VCO} is called the gain of VCO and ω_0 is the center frequency. K_{VCO} is expressed in rad/s/V.

The change in frequency in PLL is provided by the controlled voltage V_{cont}. We can develop a relationship between the V_{cont} and the frequency deviation of the VCO from its center frequency as

$$\Delta\omega = K_{VCO}V_{cont}. \tag{3.3}$$

Given that frequency is the time derivative of phase, the output phase deviation of the VCO may be represented as follows

$$\Delta\omega = \frac{d\,\varphi_{VCO}}{dt} = K_{VCO}V_{cont} \tag{3.4}$$

Bearing in mind that K_{VCO} is not a time-dependent function so that taking Laplace transform of (3.4) provides the transfer function of VCO easily and given by

$$L\left[\frac{d\,\varphi_{VCO}}{dt}\right] = s\,\varphi_{VCO}(s) = K_{VCO}V_{cont}(s) \tag{3.5}$$

where $\varphi_{VCO}(s)$ can be written as

$$\varphi_{VCO}(s) = \frac{K_{VCO}V_{cont}(s)}{s} \tag{3.6}$$

The equation (3.6) proves that the phase of the VCO output is linearly proportional to the integral of the control voltage V_{cont}(s). The control voltage can expressed as

$$V_{cont}(s) = F(s)V_{PD}(s) \tag{3.7}$$

Using the equation (3.1), we can compute the closed-loop transfer function of PLL as

$$\frac{\varphi_{VCO}(s)}{\varphi_{REF}(s)} = H(s) = 1 - \frac{V_{PD}(s)}{V_{PD}(s) + \varphi_{VCO}(s)} \tag{3.8}$$

Using the equations (3.6) and (3.7)

$$H(s) = \frac{\frac{K_{PD}K_{VCO}V_{cont}(s)}{s}}{\frac{sV_{cont}(s)}{F(s)} + \frac{K_{PD}K_{VCO}V_{cont}(s)}{s}} \tag{3.9}$$

Simlifying the equation (3.9) gives $\frac{\varphi_{VCO}(s)}{\varphi_{REF}(s)}$ as

$$H(s) = \frac{K_{PD}K_{VCO}F(s)}{s + K_{PD}K_{VCO}F(s)} \tag{3.10}$$

The transfer function of PLL help us understand the loop behaviour, performance and dependency on each block diagram inside the loop. For example, we can compute the

DC gain of PLL using the transfer function. With aid of the control theory, the open-loop transfer function of PLL is equal to

$$G(s) = \frac{H(s)}{1 - H(s)} = \frac{K_{PD}K_{VCO}F(s)}{s} \tag{3.11}$$

Such that the DC gain of the loop is computed when s=0

$$K_{DC} = K_{PD}K_{VCO}F(0) \tag{3.12}$$

DC gain of the loop is an important criteria as a design aspect of PLL as it directly affect the phase error. We return to this point later in this chapter.

3.3 Loop Dynamics

PLLs are designed in accordance to loop-order and and loop types. The loop orders and the loop types affect various performance specifications of PLL such as stability. The highest-order in the denominator defines the loop-order. The loop orders are dependent to the order of loop filter used in the loop. As the closed-loop and open-loop transfer functions of PLL depicted in the equations (3.10) and (3.11), the loop filter function F(s) determines the dynamic behaviour of PLL.

Secondly, the loop-type is defined as how well the number of integrators within the loop. The term loop-type arises from the nature behaviour of VCO within the loop. Depicted in the 3.6, the phase of VCO can be viewed as an integrator. This integrator determines how perfect the VCO operates. The integrator can be viewed from the open-loop function of PLL. Assuming F(s) = 1 so that there is no loop filter deployed in the PLL and using the equation (3.11)

$$G(s) = \frac{K_{PD}K_{VCO}}{s} \tag{3.13}$$

Therefore this type of PLL is called type-I due to the ideal integrator function.

3.4 First-Order Loops

When F(s) = 1, we assumed that the loop does not contain the loop filter. The closed-loop transfer function of the PLL can be obtained as,

$$H(s) = \frac{K_{PD}K_{VCO}}{s + K_{PD}K_{VCO}} = \frac{K_{gain}}{s + K_{gain}} \tag{3.14}$$

where K_{gain} is the loop gain that is equal to $K_{PD}K_{VCO}$. The closed-loop transfer function concludes that the PLL is in the first-order. The PLL is also called type-I because of the VCO.

The first-order type-I PLLs' stability performance can be analyzed by using root locus analysis and Bode plots. The root locus analysis using the equation 3.14 is plotted in the Figure 3.3.

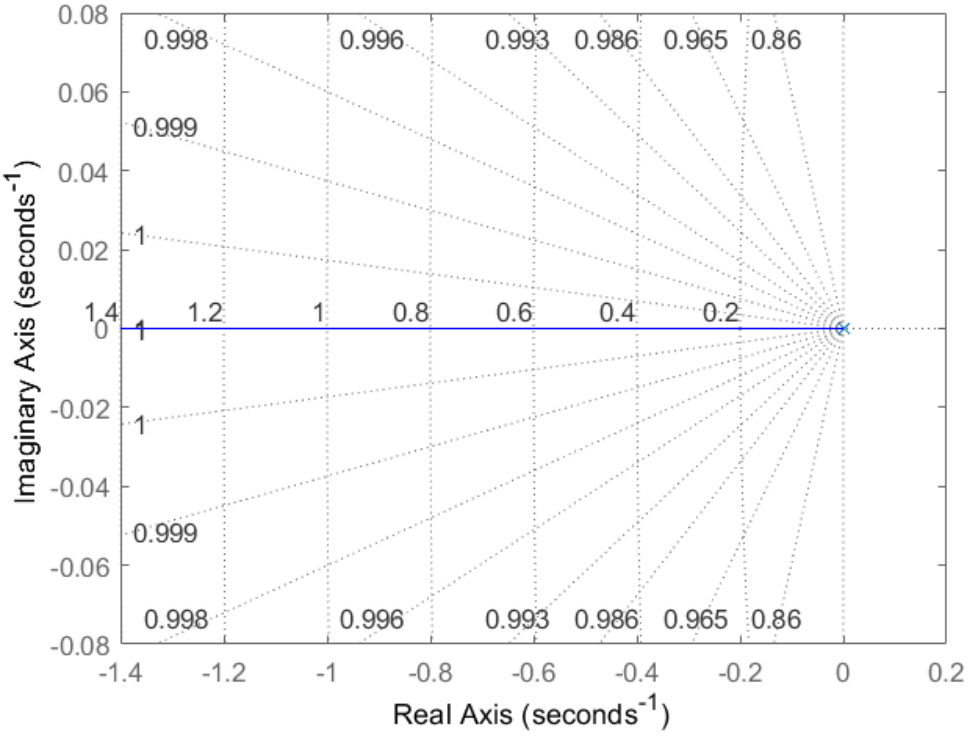

Figure 3.3 : Root locus analysis of a first-order type-I PLL.

The open-loop pole at zero is pointed as cross mark. We can state our analysis according to K_{gain} value. If K_{gain} is 0, the loop gain is zero so that the closed-loop pole is equal to the open-loop pole. As the gain increases, the closed-loop pole moves towards infinity and its location is equal to the gain. As a nature of the system, the closed-loop pole is always at the left-half plane so that the loop is stable.

The Bode plot of open-loop transfer function of a first-order type-I PLL is shown in Figure 3.4. The figure suggests that the integration behaviour of the VCO is the only part frequency dependency arises. As the pole is at zero, the system is at a 90° phase shift. The magnitude of the system has a slope of -20 db/decade and it crosses by the

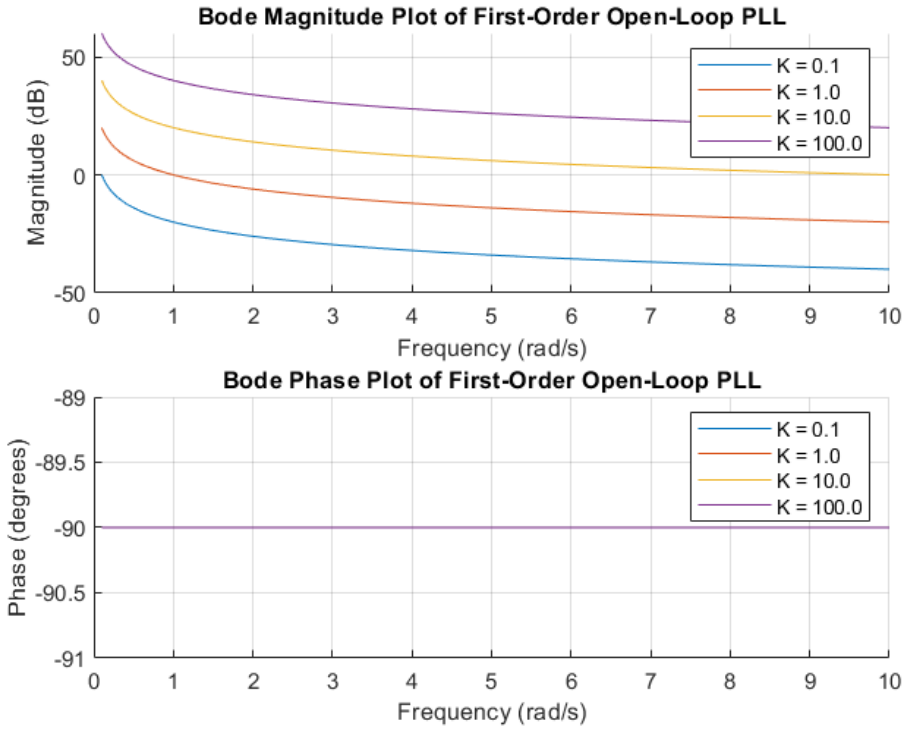

Figure 3.4 : Bode plot of open-loop transfer function of a first-order type-I PLL.

0 dB line thus the crossover frequency is equal to K_{gain}. We can conclude from this Bode plot that the loop gain determines the linear dynamics of the loop.

The Bode plot of the closed-loop response is shown in the Figure 3.5 where x-axis is normalized to natural frequency.

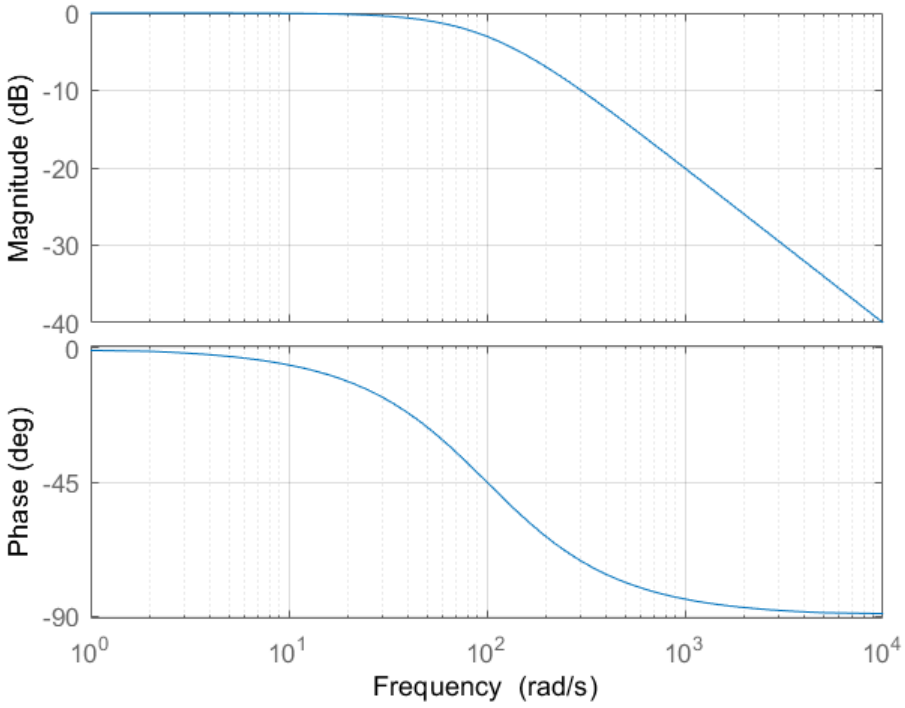

Figure 3.5 : Bode plot of closed-loop transfer function of a first-order type-I PLL.

3.5 Second-Order Loops

PLL design can be implemented using second-order loops. It is beneficial to use second-order loops in terms of its performance. The second-order loops can be configured using an active filter element or a passive filter element.

3.5.1 Second-order type-II loop

The second-order loops using active filters is called type-II loops and compose of at least two ideal integrators which provide two poles at zero. We require an active filter to realize two poles at zero. The transfer function of the filter can be defined as

$$F(s) = \frac{s\tau_2 + 1}{s\tau_1} \tag{3.15}$$

In the loop filter, there is a pole at ω=0 and a zero at ω $=-\frac{1}{\tau_2}$. We require to have a pole to make the loop to have second-order and a zero to stabilize the system which we will mention it in this chapter later.

Using (3.11) , the transfer function of the open-loop PLL becomes

$$G(s) = \frac{K_{PD}K_{VCO}(s\tau_2 + 1)}{s^2\tau_1} \tag{3.16}$$

The closed-loop transfer function from (3.10) is found as

$$H(s) = \frac{sK_{PD}K_{VCO}\tau_2 + K_{PD}K_{VCO}}{\tau_1 s^2 + K_{PD}K_{VCO}\tau_2 s + K_{PD}K_{VCO}} \tag{3.17}$$

We can simplify the loop gain in (3.17) as

$$K_{gain} = \frac{K_{PD}K_{VCO}\tau_2}{\tau_1} \tag{3.18}$$

We prefer to express the denominator in the form of $s^2 + 2\zeta\omega_n s + \omega_n^2$ where ζ and ω_n are the damping factor and the natural frequency respectively because we want to use the control theory depicted in (3.19).

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.19}$$

Dividing the denominator of (3.17) by τ_1, the closed-loop transfer function becomes

$$H(s) = \frac{sK_{PD}K_{VCO}\tau_2 + K_{PD}K_{VCO}}{s^2 + \frac{K_{PD}K_{VCO}\tau_2}{\tau_1}s + \frac{K_{PD}K_{VCO}}{\tau_1}} \tag{3.20}$$

The quantities ζ and ω_n can be obtained substituting (3.20) into (3.19) as follows

$$w_n = \sqrt{\frac{K_{PD}K_{VCO}}{\tau_1}} \tag{3.21}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{K_{PD}K_{VCO}\tau_2^2}{\tau_1}} \tag{3.22}$$

The root locus plot of the open-loop transfer function of second-order PLL found in (3.16) is shown in Figure 3.6. There are two zero crossing poles and a zero at s $= -\frac{1}{\tau_2}$. When K_{gain}= 0, the poles break away from the real axis at s=0 and become complex

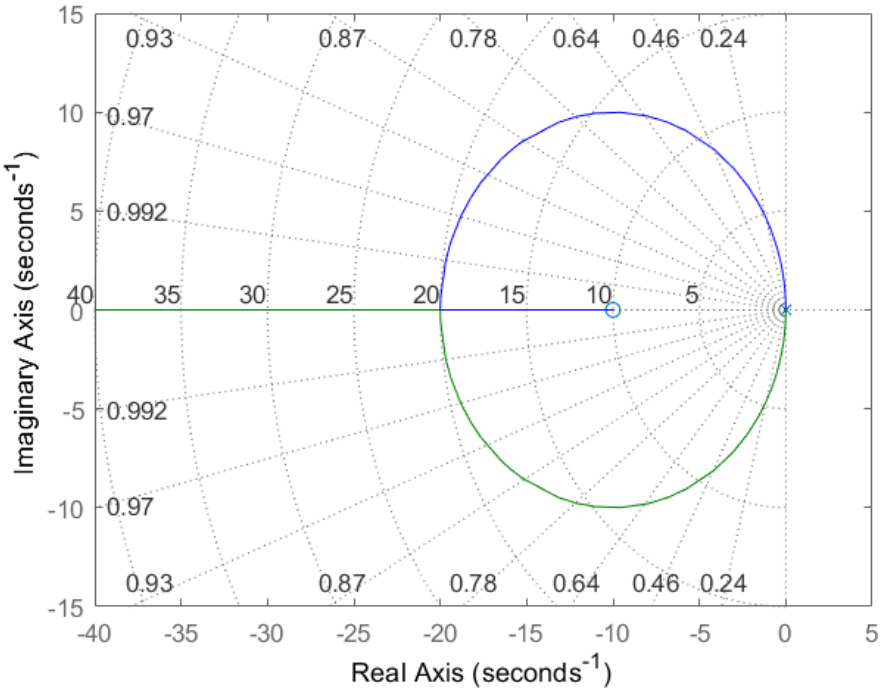

Figure 3.6 : Root locus of open-loop transfer function of a second-order type-II PLL.

conjugate. As K_{gain} increases, the poles follow an elliptical path and they cross the real axis at s $= -\frac{2}{\tau_2}$. When K_{gain} further increases and approaches to infinity, one pole approaches to s $= -\frac{1}{\tau_2}$. and the other tends to the infinity. The poles remain in the left-half s-plane for all values of K_{gain} so the system is stable. Figure 3.7 shows the Bode response of the open-loop transfer function from (3.16). At low frequencies, the amplitude slope is -40 dB/decade and the phase shift is -180° because there are two poles in the transfer function. As frequency increases, the zero contributes to the amplitude slope and it stays at -20 dB/decade. Additonally, the phase degrades and stay at -90°.

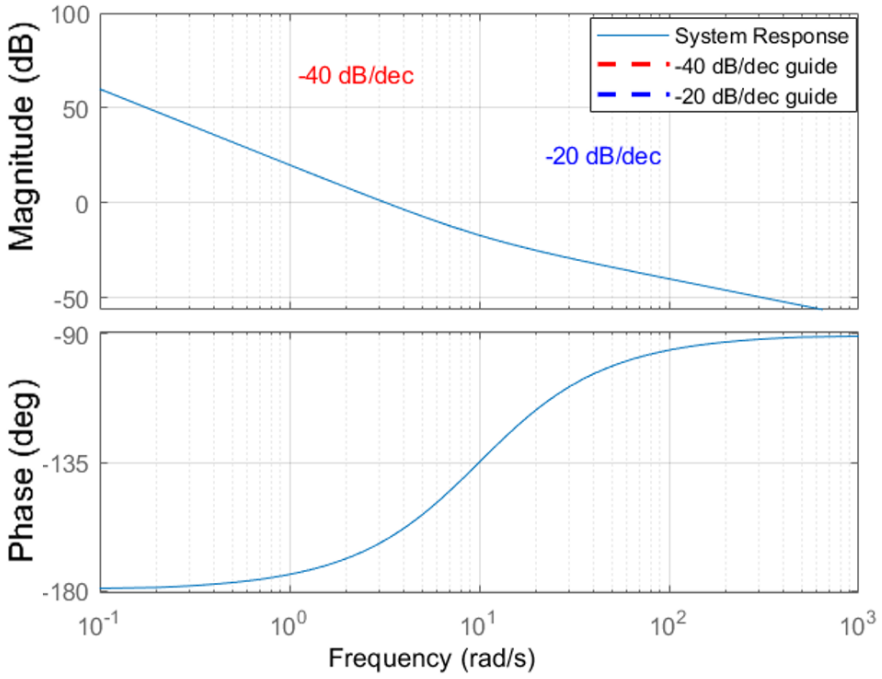

Figure 3.7 : Bode plot of open-loop transfer function of a second-order type-II PLL.

This contribution from the zero helps to system more stable as it increases phase margin. Without a zero, the magnitude plot crosses the frequency axis the natural frequency w_n. Thus, the location of zero matters. If the location of zero is placed after the crossover frequency, it will have no significant effect on the phase margin.

The closed-loop Bode plot of the second-order type-II PLL is shown in Figure 3.8. The Bode plot contains different damping values. The distortion occurs at low values of damping factor however there is also peaking at the maximum flat response ζ = 0.707 due to the zero located close to the crossover frequency.

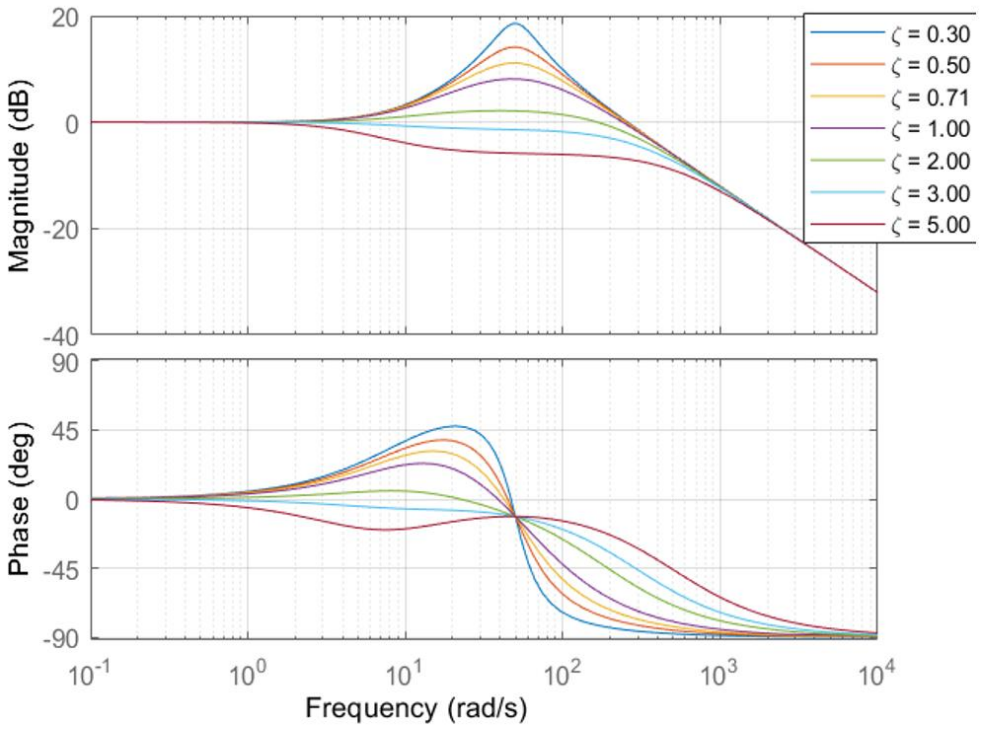

Figure 3.8 : Bode plot of closed-loop transfer function of a second-order type-II PLL for different damping factors.

The phase error response of this system is calculated as

$$\frac{\varphi_{error}(s)}{\varphi_{REF}(s)} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.23}$$

is shown in Figure 3.9. For different damping factors in the plot, we can conclude that ζ = 0.707 is maximally flat as the response does not contain a zero close to the crossover frequency.

3.5.2 Second-order type-I loop

Second-order PLL system using a passive filter with transfer function given in (3.24) is called second-order type-I loop. The selected filter type with the transfer function in (3.24) is called lag-filter.

$$F(s) = \frac{1}{s\tau + 1} \tag{3.24}$$

The transfer function of the loop filter contains one additional pole which make the PLL have two open-loop poles located at ω=0 and ω = -1/τ. The open-loop transfer function becomes

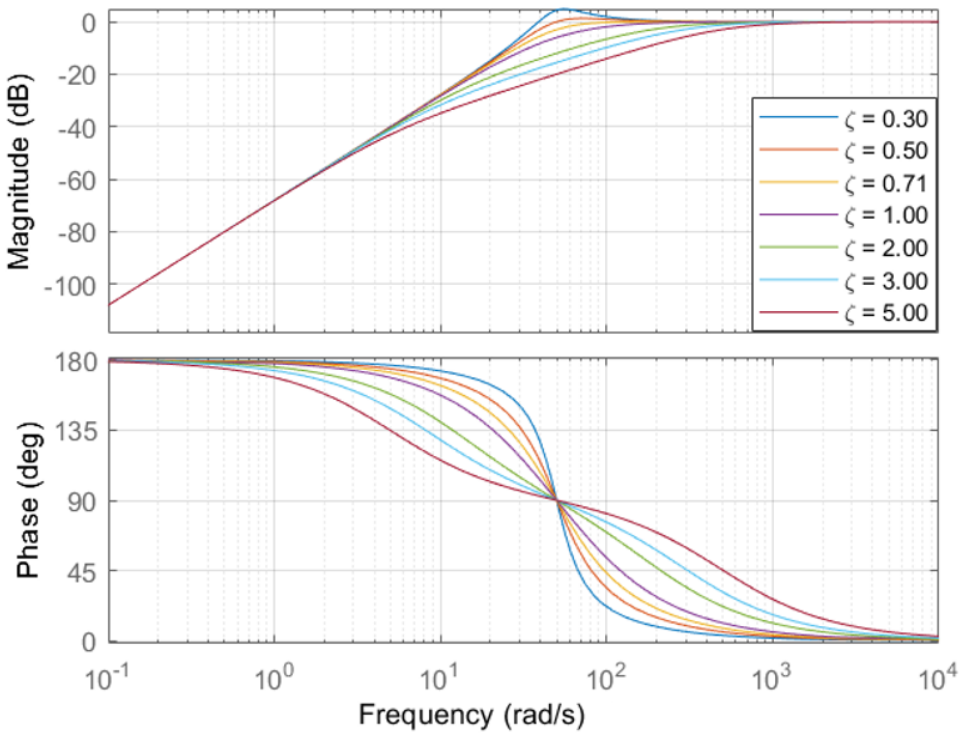

Figure 3.9 : Bode plot of phase error response of a second-order type-II PLL for different damping factors.

$$G(s) = \frac{K_{PD}K_{VCO}}{s(s\tau + 1)} \tag{3.25}$$

where the loop gain is $K_{gain}=K_{PD}\,K_{VCO}$. We can calculate the closed-loop transfer function as

$$H(s) = \frac{\frac{K_{gain}}{\tau}}{s^2 + s\frac{1}{\tau} + \frac{K}{\tau}} \tag{3.26}$$

The closed-loop transfer function can be re-written using the control theory in a common form to extract the damping factor and the natural frequency. The transfer function then becomes

$$H(s) = \frac{w_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.27}$$

where ζ and ω_n are called the damping factor and the natural frequency respectively. We can substitute (3.26) and (3.27) to calculate these values and represented in (3.28) and (3.29).

$$w_n = \sqrt{\frac{K_{PD}K_{VCO}}{\tau}} \tag{3.28}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{1}{K_{PD}K_{VCO}\tau}} \tag{3.29}$$

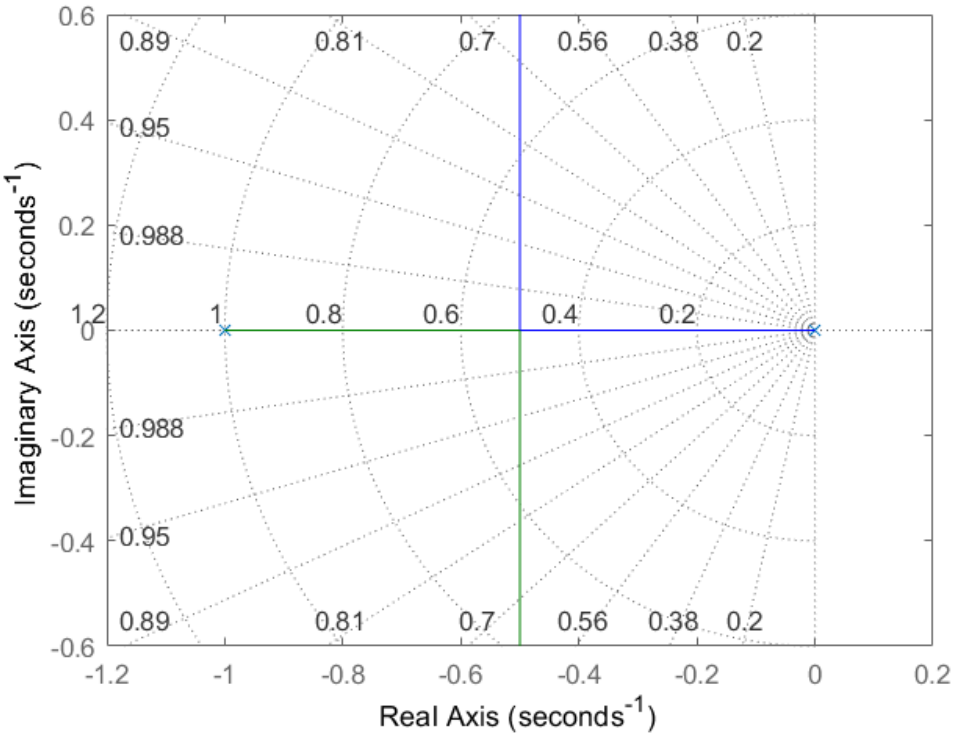

Figure 3.10 : Root locus of open-loop transfer function of a second-order type-I PLL using lag filter.

The open-loop transfer function in (3.25) is shown in Figure 3.10. The open-loop poles start at s=0 and s=-1/τ when K_{gain}=0. As the K_{gain} increases, the poles move toward each other on the real axis. When they meet at the middle, they conjugate each other and move toward infinity parallel to the imaginary axis. These poles are called conjugate pairs.

The Bode plot of open-loop transfer function can be plotted in Figure 3.11. The magnitude degrades with a slope of -20 dB/decade due to the pole at ω = 0. The phase shift of the system starts with -90° because of this pole. As the frequency increases, the crossover occurs before the second pole of the system at ω = K_{gain}. After the ω=1/τ, the phase shift becomes -180° and the magnitude starts to decrease with a slope of -40 dB/decade. We can conclude that the system is stable.

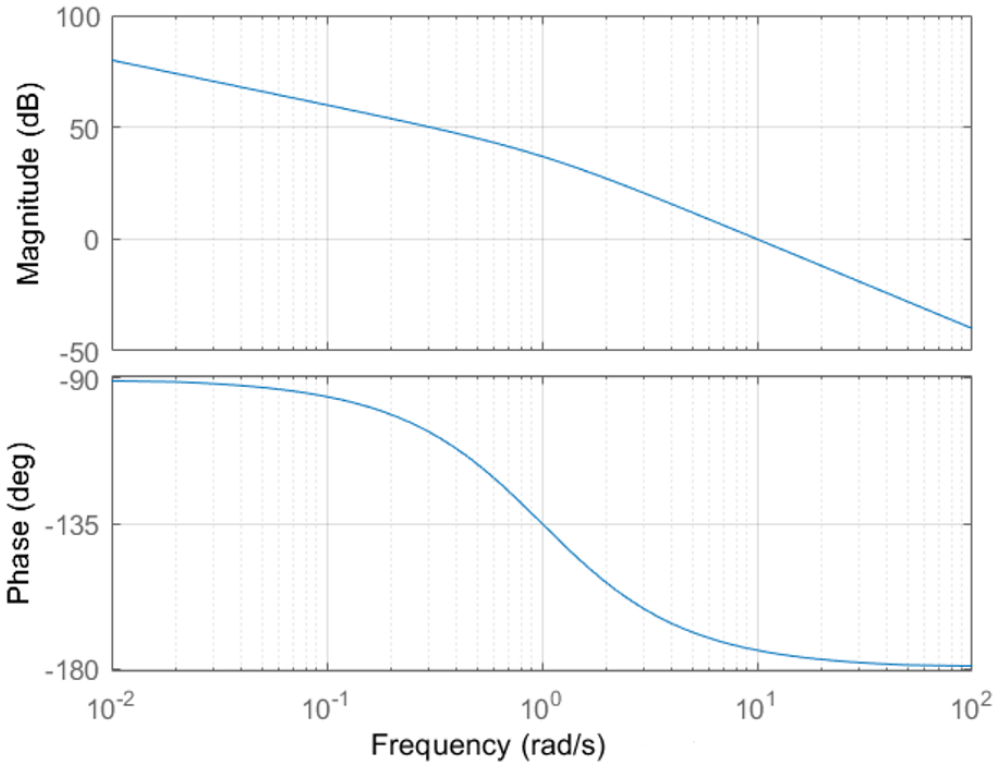

Figure 3.11 : Bode plot of open-loop transfer function of a second-order type-I PLL using lag filter.

The closed-loop response of the system using (3.26) is shown in Figure 3.12 for different damping factors. The damping factor at $\zeta = 0.707$ provides the maximally flat response as there is no zero in the system.

The phase error response of the system is given as

$$\frac{\varphi_{error}(s)}{\varphi_{REF}(s)} = \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.30}$$

As can be seen from the phase error response that is plotted at Figure 3.13, the distortion at low damping values occurs as a result of existence of a zero.

To eliminate the distortions seen at magnitude and phase error response of second-order type-I loop, we can deploy second-order passive filter called a lag-lead filter with haVINg additional zero in its transfer function and shown in (3.31).

$$F(s) = \frac{s\tau_2 + 1}{s\tau_1 + 1} \tag{3.31}$$

The open-loop transfer function the becomes

$$G(s) = \frac{K_{PD}K_{VCO}(s\tau_2 + 1)}{s(s\tau_1 + 1)} \tag{3.32}$$

where the loop gain is

$$K_{gain} = \frac{K_{PD}K_{VCO}\tau_2}{\tau_1} \tag{3.33}$$

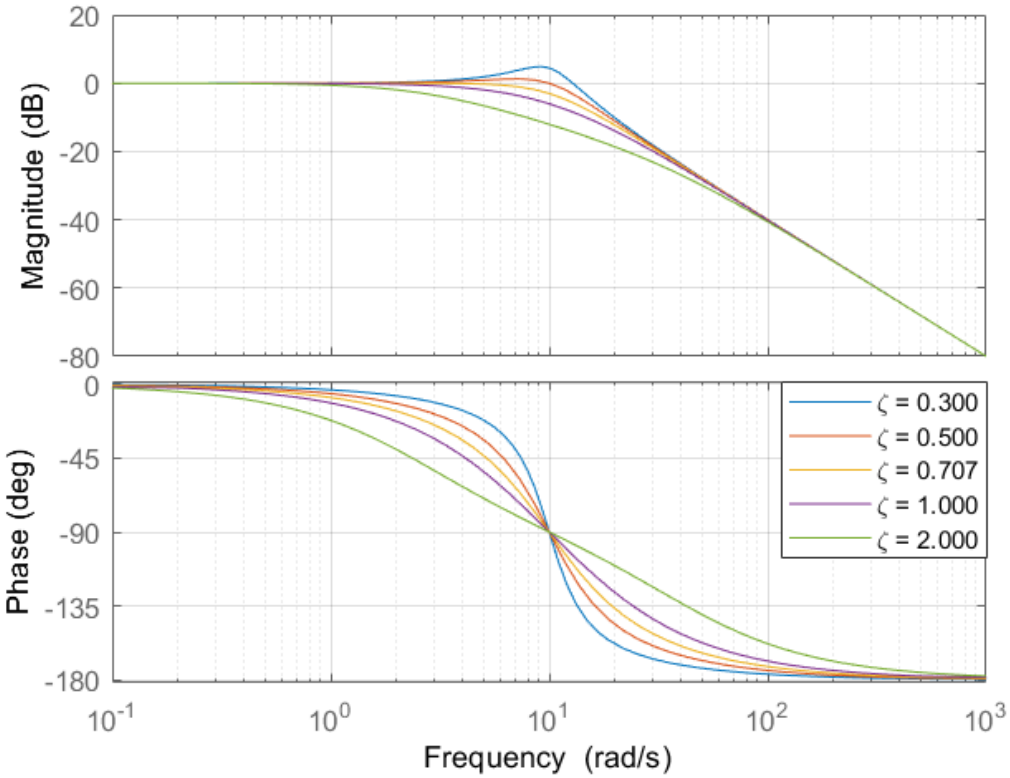

Figure 3.12 : Bode plot of closed-loop transfer function of a second-order type-I PLL for different damping factors.

We can calculate the closed-loop transfer function as

$$H(s) = \frac{sK_{gain} + \frac{K_{gain}}{\tau_2}}{s^2 + s\left(\frac{1}{\tau_1} + K_{gain}\right) + \frac{K_{gain}}{\tau_2}}. \tag{3.34}$$

If we re-write the closed-loop transfer function in the common form

$$H(s) = \frac{K_{gain}s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.35}$$

where ζ and ω_n are called the damping factor and the natural frequency respectively. We can substitute (3.34) and (3.35) to calculate these values and represented in (3.36) and (3.37).

$$w_n = \sqrt{\frac{K_{PD}K_{VCO}}{\tau_1}} \tag{3.36}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{K_{PD}K_{VCO}}{\tau_1}}(\tau_2 + \frac{1}{K_{PD}K_{VCO}}) \tag{3.37}$$

As can be seen that the damping factor and the natural frequency are independent of each other due to which the lag-lead filter has two independent time constants. This feature is the major advantage of using lag-lead filter inside PLL.

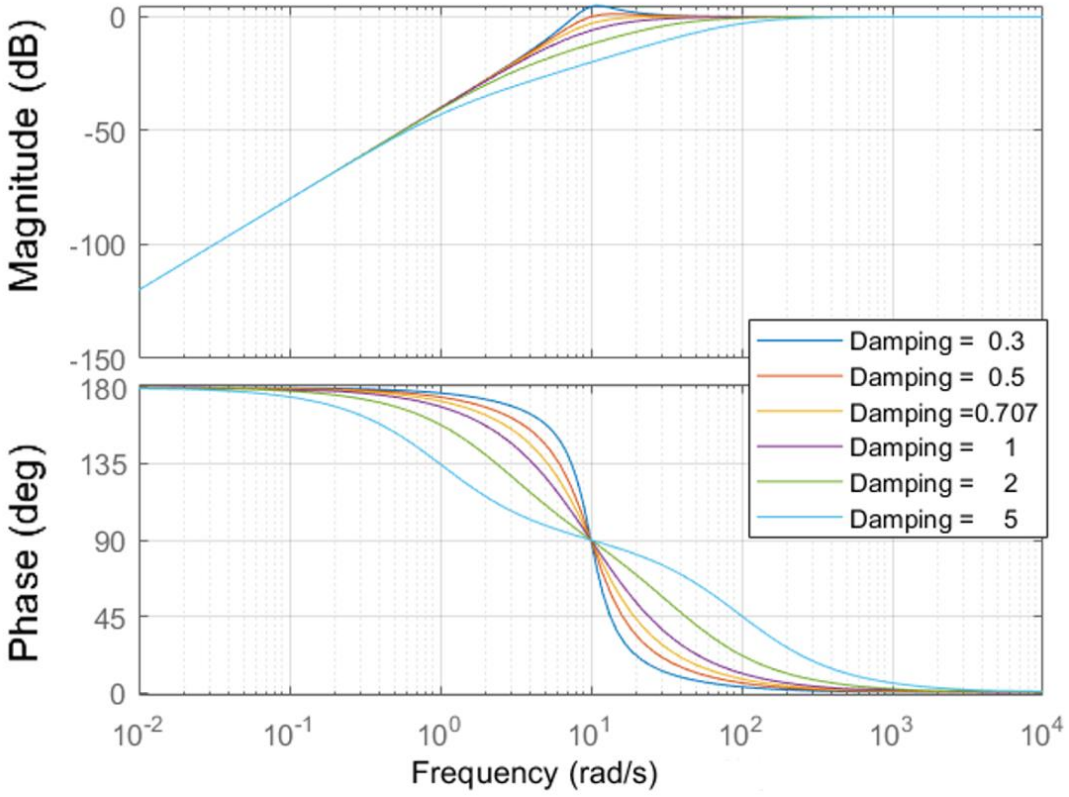

Figure 3.13 : Bode plot of phase error response of a second-order type-I PLL for different damping factors.

Root-locus of a second-order type-I PLL with lag-lead filter is shown in Figure 3.14. When K_{gain} = 0, there are two poles at s=0 and s=-1/τ_1. There also exists a zero located at s=-1/τ_2. As the gain increases, two poles move toward each other and they meet at

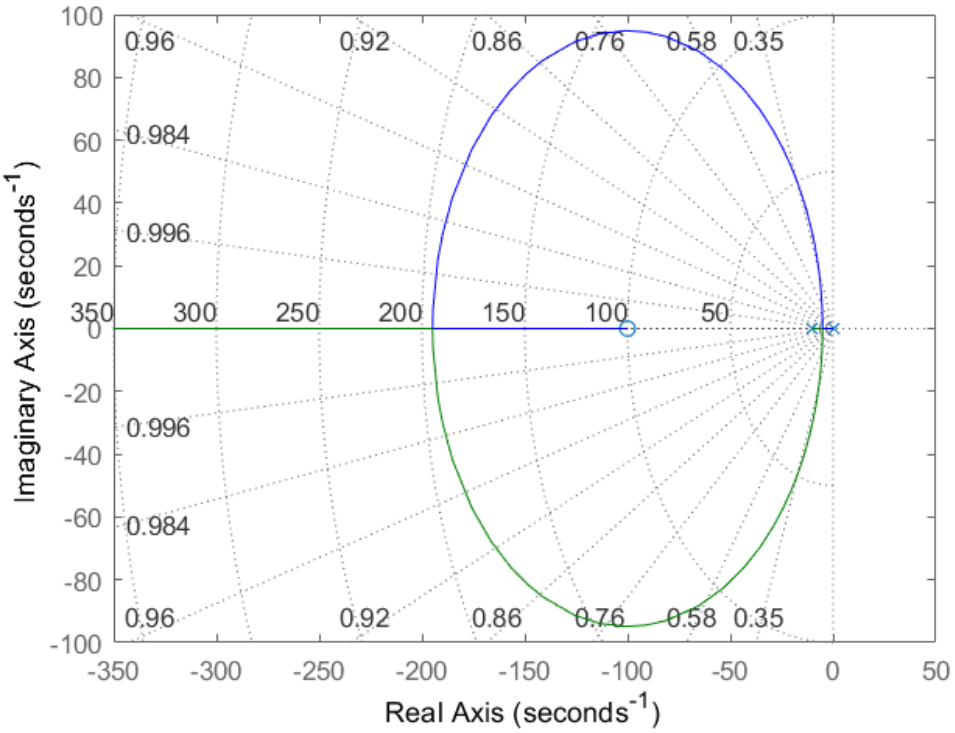

Figure 3.14 : Root locus of open-loop transfer function of a second-order type-I PLL using lag-lead filter.

the middle where they become complex conjugate of themselves. The zero in the system forms a circle centered at s=-1/τ_2. As a side effect, the damping factor increases linearly with the increase in the gain. If the gain further increases, the complex conjugate poles cross the real axis and the loop becomes overdamped as the damping factor is greater than one at this location. Last but not least, when the gain approaches to infinity, one pole also approaches to infinity but the other diverts to the zero. The entire root locus is on the left half s-plane so the system is stable.

The Bode plot of the system is shown in Figure 3.15. Due to the pole at ω=0 that is contributed by VCO, the magnitude has a slope of -20 dB/decades at low frequencies. The system has a -90° phase shift because of this pole. The pole of the filter introduces a -45° phase shift when ω=1/τ_1 and the magnitude starts to decrease -40 dB/decades from this frequency point. Finally, when the frequency reaches to the zero which is located after the poles, the zero contributes 45° phase shift and the magnitude has again a slope of -20 dB/decades. The magnitude crosses the frequency axis so the crossover frequency is obtained by using the loop gain K_{gain}.

$$w_{corner} = \frac{K_{PD}K_{VCO}\tau_2}{\tau_2} = K_{gain} \tag{3.38}$$

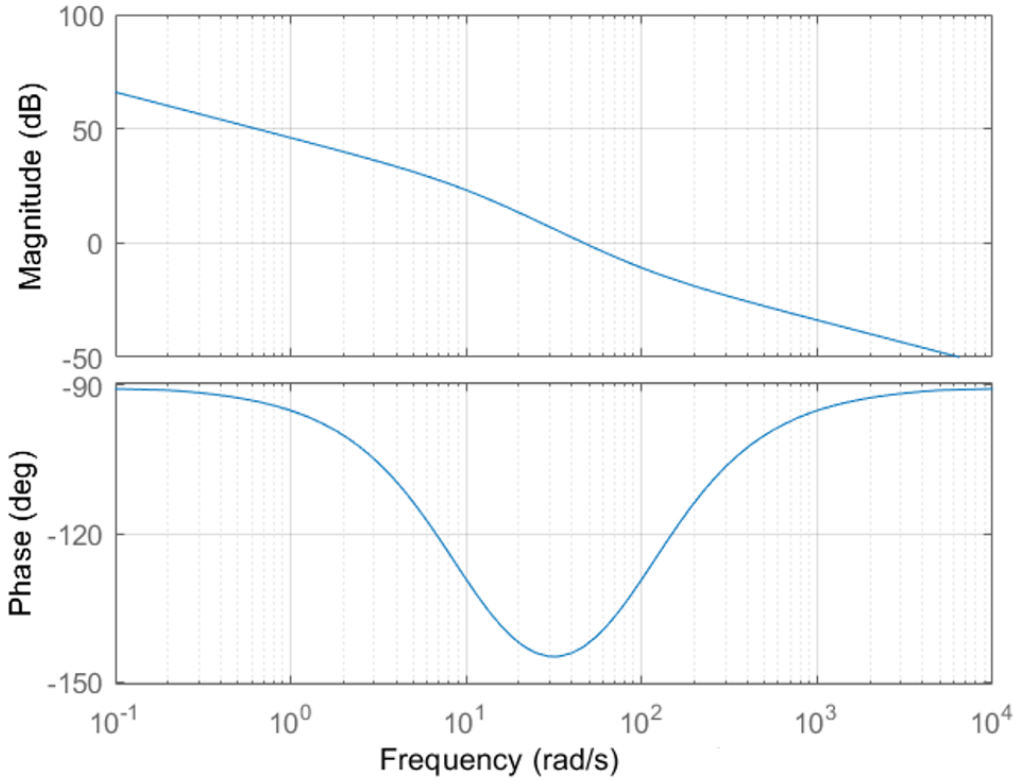

Figure 3.15 : Bode plot of open-loop transfer function of a second-order type-I PLL using lag-lead filter.

3.6 Third-Order Loop

Although it is useful to use first- and second-order PLLs for basic applications with advantages mentioned in the previous sections, more demanding systems such as those requiring faster settling times and tighter control over loop dynamics necessitate the use of third-order PLLs. A third-order PLL typically introduces an additional pole in the loop filter, which improves loop stability and offers a trade-offs between bandwidth, phase margin and noise performance of the system. The addition of the pole can be configured using either third-order of a filter or additional filter to the existing second-order loop design.

3.6.1 Third-order type-II loop

An additional first-order filter to the existing second-order type-II PLL loop configures a third-order type-II loop. The choice of the additional filter is applied after the crossover frequency because the high frequency components supplied from phase detector will be filtered while maintaining the loop dynamics. In other words, placing

the additional filter after the crossover frequency does not provide significant effect on the loop bandwidth, damping factor and natural frequency.

The filter transfer function in (3.15) can be modified with the additional pole placed after the crossover frequency as follows

$$F(s) = \frac{s\tau_2 + 1}{s\tau_1(s\tau_3 + 1)} \tag{3.39}$$

The filter has a zero at s=-1/τ_2 and pole at s=0 and s=-1/τ_3. Bearing in mind that the pole at s=-1/τ_3 should be placed far behind the crossover frequency not to interfere with the second-order characteristics.

The open-loop transfer function then becomes

$$G(s) = \frac{K_{PD}K_{VCO}(s\tau_2 + 1)}{s^2\tau_1(s\tau_3 + 1)} \tag{3.40}$$

The root locus of (3.40) is plotted in Figure 3.16. There are two poles at s =0 and one pole at s = -1/τ_3. The zero is at s = -1/τ_2. The poles at s = 0 are complex conjugate of each other and form a contour shown in the figure. The pole at s = -1/τ_3 approaches towards to zero at s = -1/τ_2. There is no zero or pole at the right half s-plane thus the system is stable.

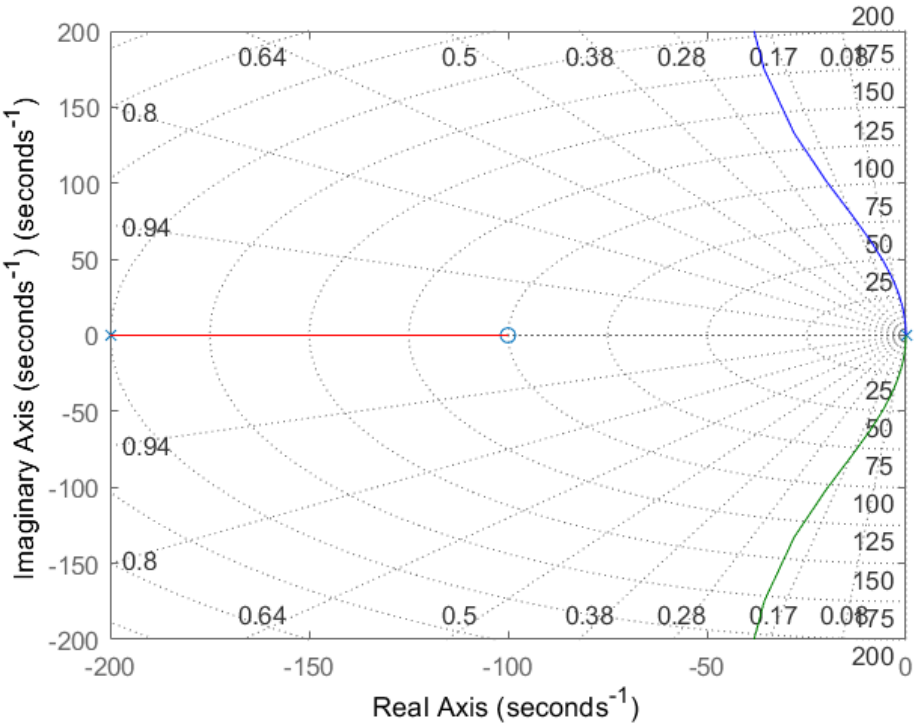

Figure 3.16 : Root locus of open-loop transfer function of a third-order type-II PLL.

The Bode plot of the system is given in Figure 3.17. As a result of two poles at ω = 0, the magnitude starts with a slope of -40 dB/decades for low frequencies. By the same reason, the system has a phase shift of -180°. When the frequency reaches to the zero at ω =1/τ_2, the magnitude slope changes to -20 dB/decades and the phase shift is -135° and follows a contour through -90°. The system once again sees a pole at ω =1/τ_3 thus the magnitude slope changes to -40 dB/decades and the phase shift starts to decrease and reaches to -180° when the frequency further increases. As can be seen that the system unconditionally stable.

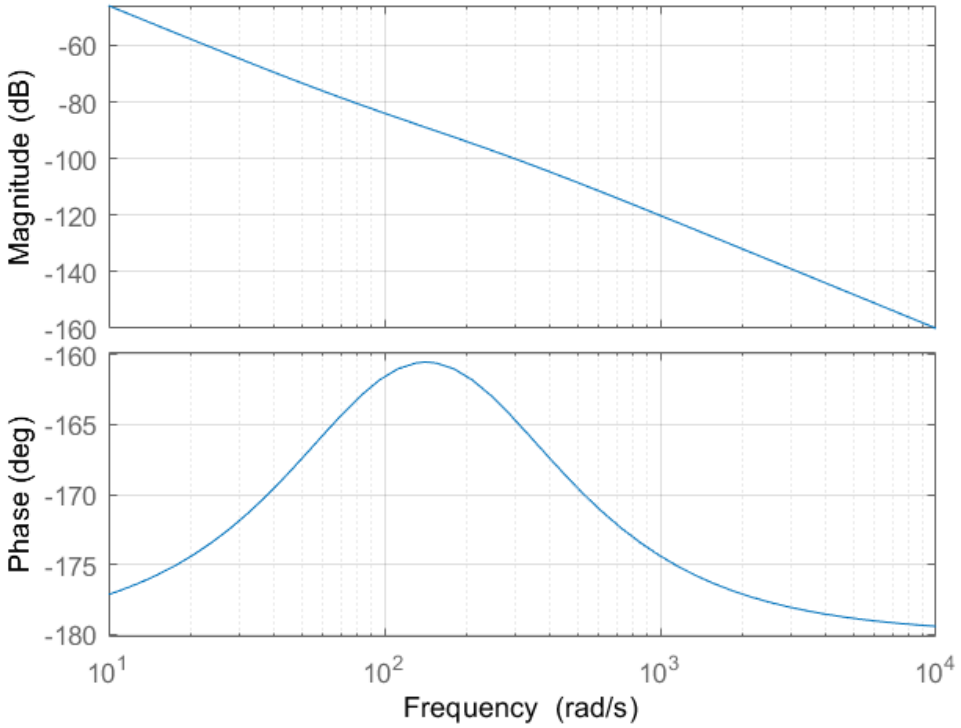

Figure 3.17 : Bode plot of open-loop transfer function of a third-order type-II PLL.

3.6.2 Third-order type-III loop

A third-order, type-III PLLs are employed to meet stringent performance requirements such as fast settling time, low jitter, and robust stability. A type-III PLL contains a filter whos poles are at the origin so that it is characterized by haVINg three integrators in its open-loop transfer function. We require two zeros at the same frequency or close to each other to have a stable loop. Assuming the zeros are at s = -1/τ_2, the filter transfer function becomes

$$F(s) = \frac{(s\tau_2 + 1)^2}{(s\tau_1)^2} \tag{3.41}$$

The filter has two poles at s = 0 and two zeros at s = -1/τ_3. Using this filter, we can construct the open-loop transfer function as

$$G(s) = \frac{K_{PD}K_{VCO}(s\tau_2 + 1)^2}{s(s\tau_1)^2} \tag{3.42}$$

where the loop gain can be written as in (3.43).

$$K_{gain} = \frac{K_{PD}K_{VCO}\tau_2^2}{\tau_1^2} \tag{3.43}$$

The root locus of (3.42) is plotted in Figure 3.18. There are three poles at s =0 and two zeros at s =-1/τ_3. The poles at s = 0 move away from each other when the loop gain, K_{gain}, increases. Two of the poles become complex conjugate of each other and enter the right half s-plane. The poles depart from the real axis with 60° angle and form a circular path. The third pole approaches to the zero at s =-1/τ_3.

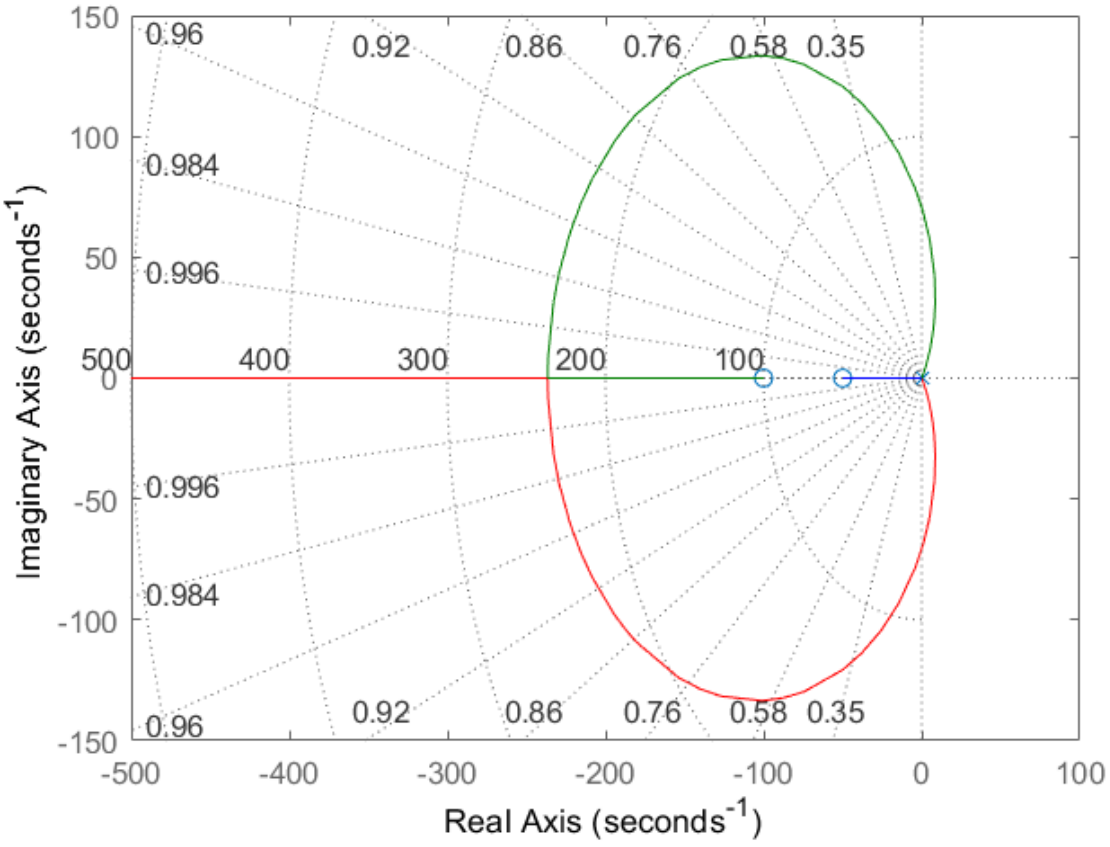

Figure 3.18 : Root locus of open-loop transfer function of a third-order type-III PLL.

When K_{gain} becomes 1/2τ_2, the poles cross the imaginary axis at s = ±1/τ_2 and enter to the left half s-plane. In other words, the loop is unstable for the values of the loop gain lower than 1/2τ_2 and becomes stable for the greater values of 1/2τ_3. This is

distinguishing feature of third-order type-III loops from the other loops previously visited in this chapter which are unconditionally stable for all values of the loop gain.

If the gain increases further, the conjugate poles continue to reach to the negative real axis in the left half s-plane whereas the third pole still continues to approach to the zeros.

Substituting (3.43) in (3.42) and solving for the conjugate poles to cross the negative real axis in (3.42), we arrive a loop gain with a value of $27/4\tau_3$. The conjugate poles cross the negative real axis at $s = -3/\tau_2$ and become real valued. At this point, one of the conjugate pole starts to move towards to the zeros whereas the other pole approaches to infinity. The third pole moves towards to the zeros as well. In conclusion, the system is conditionally stable for the loop gain values greater than $1/2\tau_3$.

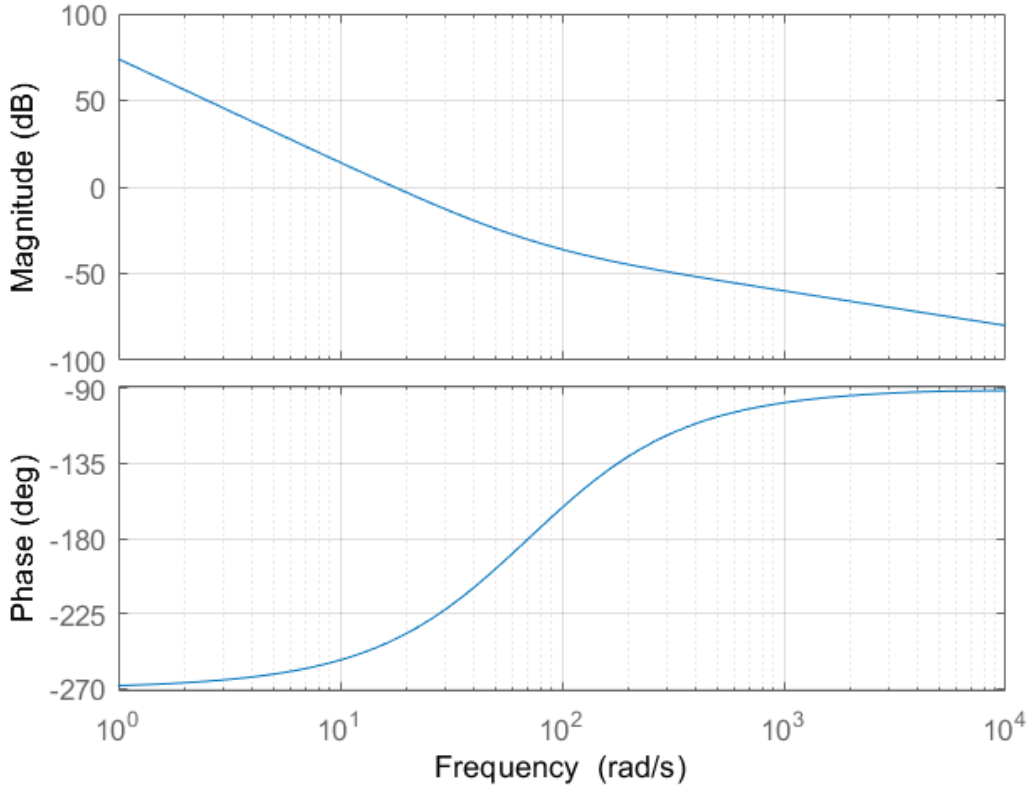

Figure 3.19 : Bode plot of open-loop transfer function of a third-order type-III PLL.

The Bode plot of the system is given in Figure 3.19. As a result of three poles located at $\omega = 0$, the magnitude starts with a slope of -60 dB/decades for low frequencies. By the same reason, the system has a phase shift of -270°. When the frequency reaches to the zero at $\omega = 1/\tau_2$, the magnitude slope changes to -20 dB/decades and the phase shift is -180° and follows a contour through -90°. When the frequency reaches to $\omega = K_{gain}$,

the magnitude plot crosses the x-axis. This crossover frequency is defined by the loop gain once again.

3.7 Other Loop Orders

While third-order PLLs offer improved performance in terms of phase tracking and distortion, certain advanced applications such as high-resolution frequency synthesis or agile radar systems may require higher-order and higher-type PLLs. The concept of having high-order or high types of PLLs is as same as previously discussed. Additional poles and/or integrators are introduced into the loop transfer function. However, the main drawback of such designs is their increased complexity and reduced robustness. Higher-order loops are more sensitive to process, voltage, and temperature (PVT) variations and can become unstable if not carefully compensated. Besides, having a higher-order loops require more elements compared to lower-order loops which increase the power consumption of the system. In practical implementations, higher-order loops are used as second-order equivalents with added filtering stages. In summary, while higher-order PLLs can offer performance benefits, they demand careful design trade-offs between complexity, stability and power consumption.

4. NOISE

In modern electronic and communication systems, noise analysis is a critical part of evaluating signal performance. This significance stems from the fact that noise can severely impact the functionality of applications. It can reduce accuracy, and disrupt the reliable transmission of data.

Noise can be described as any unwanted disturbance that interferes with the desired signal. In the context of PLLs in 5G, the impact of noise is particularly critical as it directly degrades the performance of the entire communication system. The stringent requirements of 5G for high data rates, low latency, and massive connectivity necessitate that clean and stable clock signals. This chapter delves into characteristics of noise mechanisim required to analyze CMOS PLL design for 5G applications as well as exploring their effects on key PLL parameters such as phase noise and jitter. A thorough understanding of these noise mechanisms is essential for developing robust and high-performance PLL architectures capable of meeting the demanding specifications of 5G wireless communication.

4.1 Introduction to Noise Mechanisms

Noise is a random process unlike a deterministic signal. Its exact value at any point in time is unknown. While we can analyze its statistical properties over time, predicting its instantaneous amplitude is simply not possible. Since the instantaneous value of noise is inherently unpredictable, analysis of noise over the frequency domain can be achieved. Power spectral density or shortly spectrum quantifies how the power of a signal is distributed as a function of frequency. It is defined as the noise power contained within a 1-Hz bandwidth centered at a given frequency, effectively representing the power per unit frequency. This normalization to a 1-Hz bandwidth enables consistent comparisons of noise levels at different frequencies regardless of the specific measurement or analysis bandwidth.

(4.1) represents the voltage noise spectrum of a resistor, illustrating how the ambient thermal energy is converted into a random voltage across the resistor terminals.

$$\bar{V}_n^2 = 4k_B TR \quad \mathrm{V}^2/\mathrm{Hz} \tag{4.1}$$

where $k_B = 1.38 \cdot 10^{-23}$ J.K^{-1} is the Boltzmann constant and T is the absolute temperature. The noise in a resistor is called white noise because its spectrum is constant across a wide range of frequencies. This means that the resistor generates noise power equally at all frequencies which is similar to how white light contains all visible wavelengths in equal proportion where the name comes from.

MOS transistors are sources of two primary types of noise, namely flicker noise (also known as 1/f noise) and thermal noise. Flicker noise is mainly dominant at low frequencies and arises due to charge trapping and detrapping at the oxide-semiconductor interface which causes fluctuations in the current [8]. Its power spectral density is inversely proportional to frequency, hence the name 1/f noise. The flicker noise is shown in Figure 4.1 and expressed as

$$S_{1/f}(f) = \frac{K}{WLC_{ox}} \frac{1}{f} \quad \mathrm{V}^2/\mathrm{Hz} \tag{4.2}$$

where K is a process-dependent parameter, W is the width of the transistor, L is the length of the transistor, and C_{ox} is the oxide capacitance per unit area. The inverse frequency dependence of flicker noise presents a significant challenge when operating at low frequencies. As the frequency decreases, the power spectral density of flicker noise increases thus MOS transistors contribute greater noise. This behavior can degrade signal integrity and limit the precision of analog and RF front-end designs.

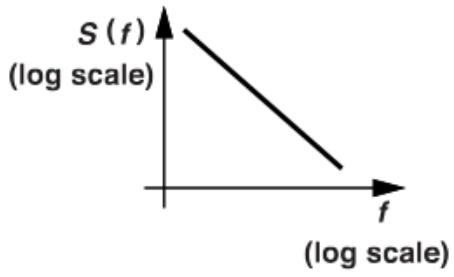

Figure 4.1 : Flicker noise model in MOS devices.

On the other hand, thermal noise in MOSFETs originates from the random motion of carriers in the channel which is similar to the thermal noise in resistors. It is modeled as a white noise current source with a flat power spectral density over frequency and can be derived as

$$I_n^2 = 4k_B T\gamma g_m \quad A^2/Hz \tag{4.3}$$

where γ is a process-dependent coefficient and g_m is the transconductance of the MOSFET. Process-dependent coefficient is typically 2/3 for long channel devices and can vary depending on the fabrication process. The thermal noise is not frequency-dependent hence is present across all frequencies.

4.2 Noise Analysis in Time Domain

Even though noise signals are inherently random, time-domain models are possible to characterize them. Time-domain noise analysis focuses on modeling noise as a statistical nature of noise process, one possible noise modeling approach analyzed in [8]. Statistical model allows to evaluate system stability, jitter, and transient response more intuitively.

Figure 4.2 represents a periodic signal $V_1(t)$ and noise added to this signal $x_1(t)$. The average power that a periodic signal can deliver is given as

$$P_{ave} = \frac{1}{T}\int_0^T V_1^2(t)dt \tag{4.4}$$

where $V_1(t)$ is a periodic signal without noise and T is the its period. In contrary, a period of a random signal is not defined. Typically, the period is defined as time

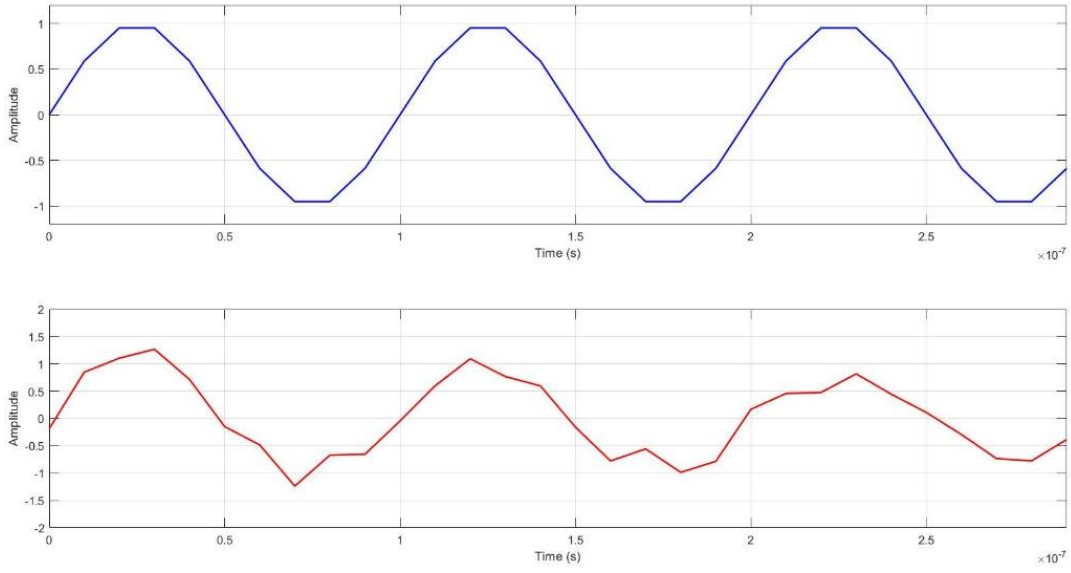

Figure 4.2 : Clean and noisy sinusoidal signal.

interval that can average the signal during the time of occurring in this situation. In other words, the average power of the signal can be computed if the signal is observed for a long time. This averaging process can be mathematically expressed using a limit function.

$$P_{ave} = \overline{x_1^2(t)} = \lim_{T\to\infty} \frac{1}{T} \int_0^T x_1^2(t)dt \tag{4.5}$$

where $\overline{x_1^2(t)}$ is the random noise signal represented with a bar sign which indicates the mean-square time average of the signal.

4.2.1 Jitter

Jitter refers to variations in the timing of a signal from its ideal positions in time. In nominally periodic signals, jitter is defined as deviations in the zero-crossing points. Figure 4.3 represents a basic example where a periodic sine wave is expected to finish its first cycle at t=100ns but due to the jitter present in the signal, it occurs slightly earlier. The jitter can be caused by noise, power supply fluctuations, or imperfections in the oscillator or clock generation circuit.

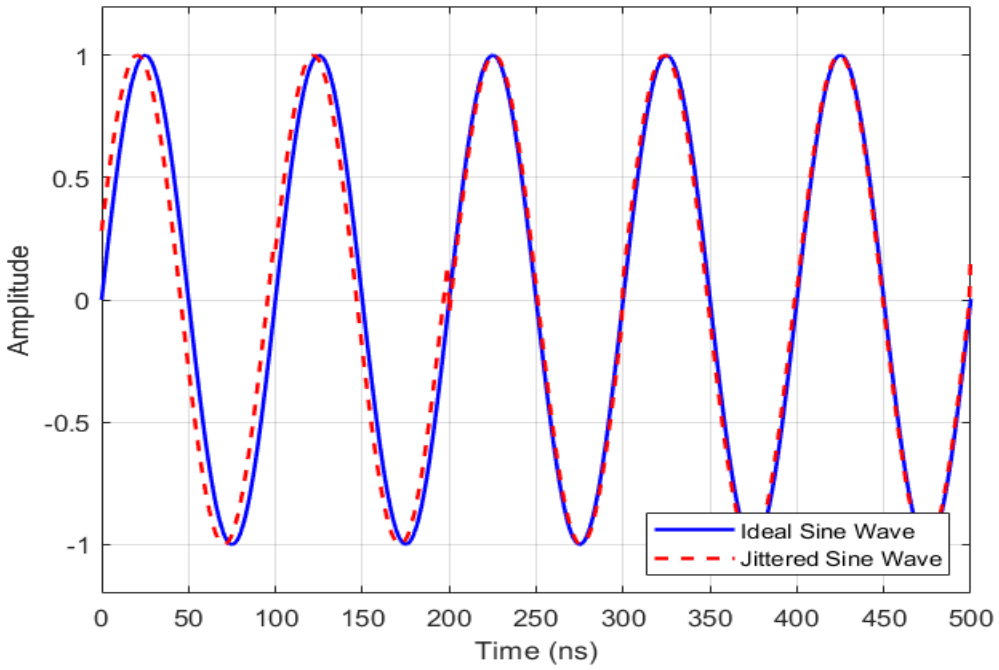

Figure 4.3 : Ideal signal with a jittered edge.

We can define a general approach to the output signal with an additive noise that may arise from amplitude and phase modulation and can be expressed as

$$V_{out}(t) = V_0(1 + \mathrm{A(t)})\cos(\omega_0 t + \alpha(t)) \tag{4.6}$$

where A(t) represents an amplitude modulation noise and $\alpha(t)$ introduces a phase modulation noise. Figure 4.4 shows a comparison of a clean signal and its noisy counterpart in the time domain in 10 MHz with blue and red colors respectively. Since jitter is caused specifically to timing variations of a signal, amplitude modulation noise does not directly contribute to jitter as it only affects the signal's magnitude.

On the other hand, phase modulation noise alters the zero-crossing instants of the signal, which translates directly into timing uncertainty thus it contributes to jitter. Therefore, the jitter is the result of the phase noise between the baseband and noisy signal. This phase noise can be expressed as

$$\alpha(t) = \alpha_m \sin(\omega_m t). \tag{4.7}$$

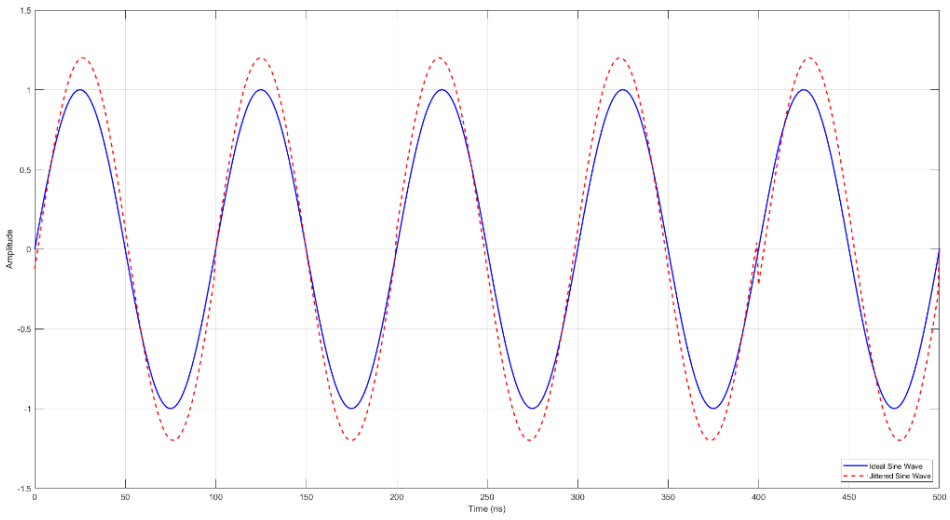

Figure 4.4 : Amplitude and phase modulated noise added to sine wave.

These timing deviations can degrade the performance of communication systems by introducing bit errors, reducing signal integrity, or impairing synchronization.

Jitter can be visualized using a graph commonly referred to as an eye diagram, which presents a cumulative graphical representation of the signal over many cycles. The main idea behind an eye diagram is to overlay multiple cycles of a periodic waveform to observe variations in timing and amplitude.

Figure 4.5 illustrates the eye diagram of a sine wave signal with period T, as analyzed in [B]. The eye diagram is synthesized by dividing the time axis into segments of T/2. These segments are then overlaid and summed into a single composite diagram, where the horizontal axis spans exactly T/2. When the merging of signal segments begins at t=0 aligned with a zero crossing, the resulting pattern resembles the shape of an eye hence the term eye diagram. This visual representation provides insight into timing variations and signal integrity with the openness of the eye indicating the degree of jitter and noise present in the signal. For instance, a well-opened eye indicates low jitter and good signal integrity as depicted in Figure 4.5b. In the presence of jitter such as in Figure 4.5c, the edges of the waveform do not align perfectly, causing the eye in the diagram to appear partially closed or blurred. The peak-to-peak jitter, ΔT_{PP}, is shown to indicate the deviation distance from the zero crossing.

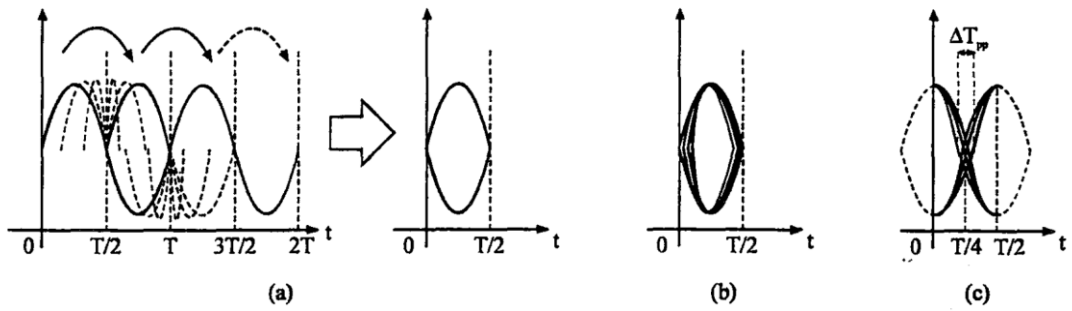

Figure 4.5 : (a) Obtaining an eye-diagram, (b) Eye-diagram of a sine wave with jitter, (c) Eye-diagram for peak-to-peak jitter calculation.

4.3 Noise Analysis in Frequency Domain

Noise analysis in the frequency domain provides valuable insights into how noise power is distributed across different frequency components of a signal. Frequency-domain techniques allow for a structured interpretation by identifying the spectral content of the noise. This is particularly useful in analog and RF circuit design, where different frequency components of noise can affect circuit performance.

To illustrate the frequency-domain characteristics of noise, consider the simple RC network shown in Figure 4.6, which forms a low-pass filter. This circuit provides an intuitive example of how noise behaves when passed through a system with frequency-selective properties.

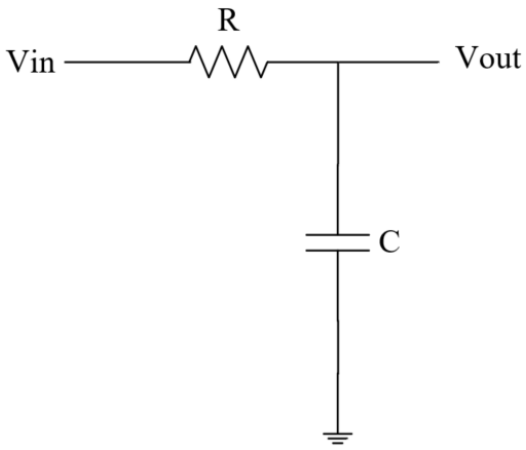

Figure 4.6 : Noise analysis of a low-pass filter.

Figure 4.7 represents the behavior of RC network in frequency spectrum. Thermal noise generated by the resistor is spread uniformly across frequencies however RC network introduces a corner frequency that the higher-frequency components are attenuated. As a result, the output noise spectrum reflects the transfer function of the filter even though the thermal noise is normally flat within the spectrum indicated with a red line, the output of the RC network filters the high frequency components. This example underscores the practical significance of frequency-domain noise analysis in predicting the frequency of interest and optimizing circuit performance accordingly.

4.3.1 Phase noise

Another approach to noise analysis in the frequency domain can be established through phase noise. The term phase noise arises especially in oscillators, the output signal is not a perfect sine wave at a single frequency due to the presence of noise sources within the circuit. These noise contributions introduce random variations in the phase of the signal therefore the spectral energy is spread around the carrier frequency. This spread is commonly referred to as phase noise. Accurate modeling and understanding of phase noise in the frequency domain are essential for evaluating oscillator performance and minimizing its impact on system-level behavior.

To demonstrate a phase noise analysis, a sinusoidal signal with additive noise can be expressed as

$$V(t) = Asin(2\pi ft) + n(t) \tag{4.8}$$

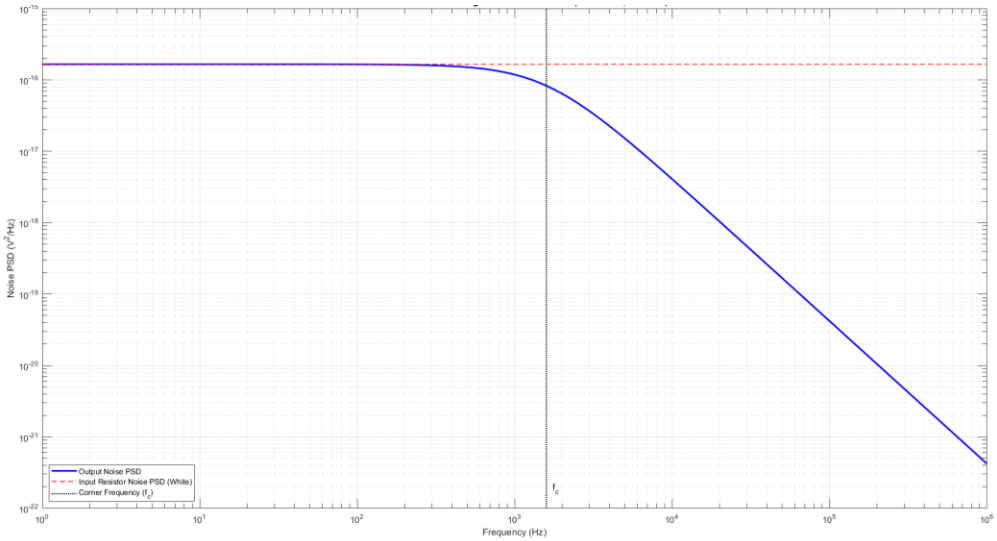

Figure 4.7 : Thermal noise PSD through RC low-pass filter.

where A is the amplitude and n(t) is the noise component. Figure 4.8 shows a comparison of a clean signal and its noisy counterpart in the time domain in 10 MHz with blue and red colors respectively. The lower plot in the figure clearly illustrates the instantaneous amplitude fluctuations imposed by the noise, causing the waveform to deviate from its ideal sinusoidal shape. While these amplitude variations are visible, the impact on the phase of the signal is often more critical.

The effect of noise on the signal's spectral purity can be observed by analyzing its representation in frequency domain. As illustrated in Figure 4.9, for an ideal sinusoidal signal, the spectrum would consist of a single impulse at the carrier frequency. However, with the addition of noise, a noise floor appears around the carrier tone, indicating the presence of unwanted frequency components.

The term, phase noise results from random fluctuations in frequency. We analyze the noise power at a specific offset, Δf, from the carrier frequency. The noise power within a 1 Hz bandwidth at this offset is measured and then normalized to the carrier power. This ratio defines the phase noise and is commonly expressed in units of dBc/Hz, where dBc denotes decibels relative to the carrier, and Hz indicates the bandwidth over which the noise power is measured.

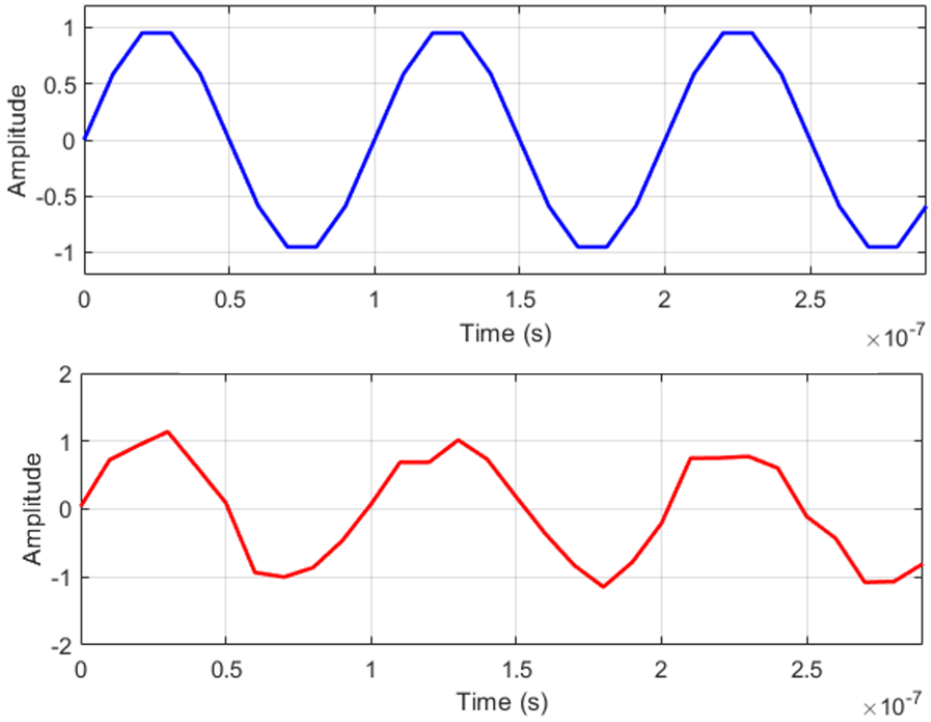

Figure 4.8 : Clean and noisy sinusoidal signal.

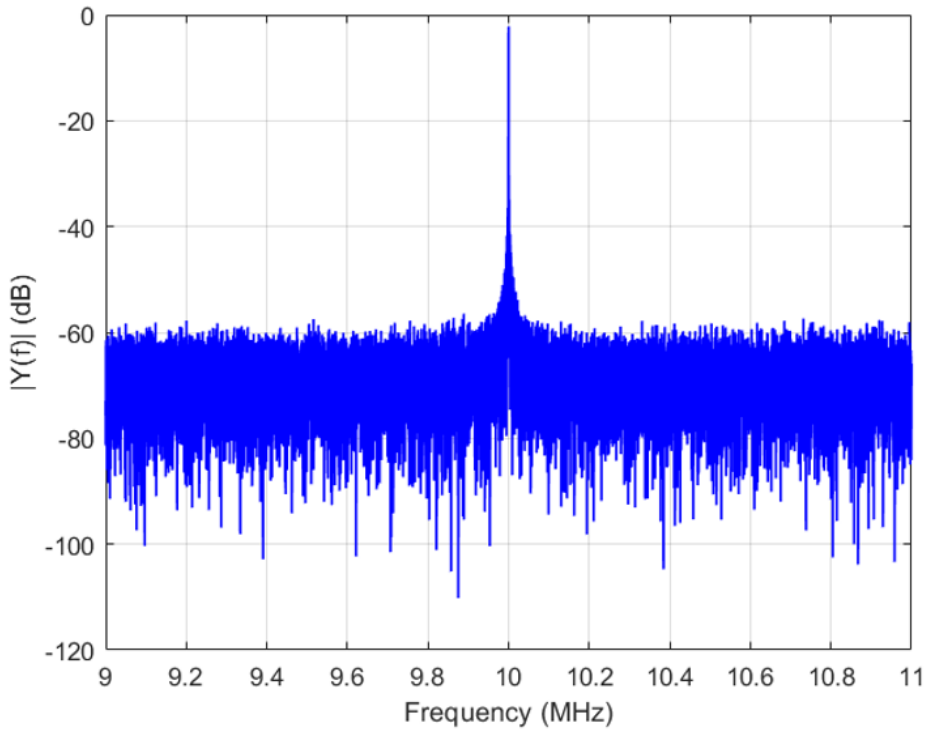

Figure 4.9 : The spectrum of noisy sinusoidal signal.

The phase noise for the current example is plotted in Figure 4.10 and is expressed as

$$L(\Delta f) = 10\log(\frac{P_{noise}(\Delta f)}{P_{carrier}}) \tag{4.9}$$

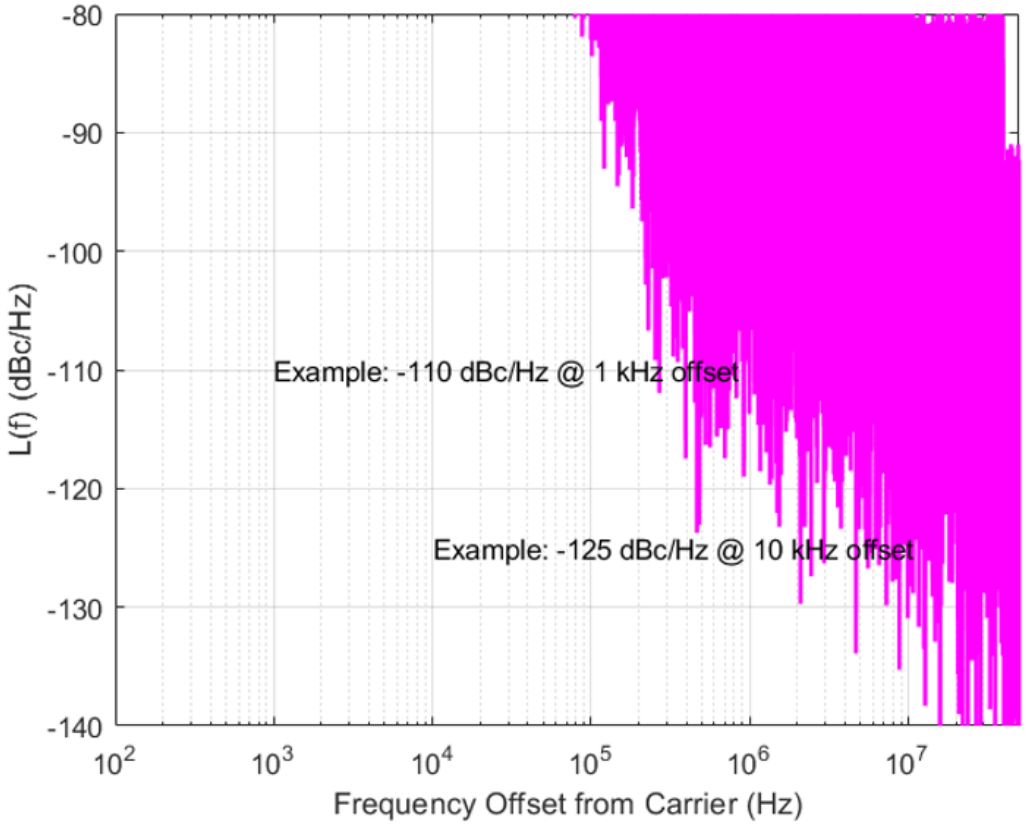

Figure 4.10 : The phase noise analysis on the sinusoidal signal.

where $L(\Delta f)$ is the phase noise at offset Δf from the carrier frequency and $P_{noise}(\Delta f)$ is the noise power measured in a 1 Hz bandwidth at the offset frequency Δf.

As shown in Figure, the phase noise is measured at -110 dBc/Hz at a 1 kHz offset and -125 dBc/Hz at a 10 kHz offset. The choice of offset frequency and the bandwidth of interest can vary depending on the requirements of the specific application.

5. ANALYSIS AND SIMULATION RESULTS OF LOOP COMPONENTS

All necessary analyses required to design a PLL system have been presented in the previous chapters. The transfer function of different orders and types of PLLs have been discussed along with the detailed noise analysis, highlighting the key performance considerations. This chapter focuses on the circuit topologies of the core components of PLL including the phase-frequency detector (PFD), the charge pump (CP), the loop filter, the voltage-controlled oscillator (VCO) and the frequency divider. The circuit blocks presented in this chapter which simulated by Cadence Virtuoso in TSMC 65 nm CMOS technology, will serve as the foundation for constructing the complete PLL system in the next chapter.

5.1 Voltage-Controlled Oscillator

Designing a VCO within a PLL environment poses significant challenges, particularly if the PLL functions as a frequency synthesizer in high frequency spectra. The design requirements must be addressed with careful attention to ensure optimal performance. VCO design begins with constructing a local oscillator. We can build a background for generating an oscillation using a simple negative-feedback system analyzed in [13] and shown in Figure 5.1 where the system is observed in s-domain. The response of the system to a low-frequency sinusoidal input is depicted in Figure 5.2.

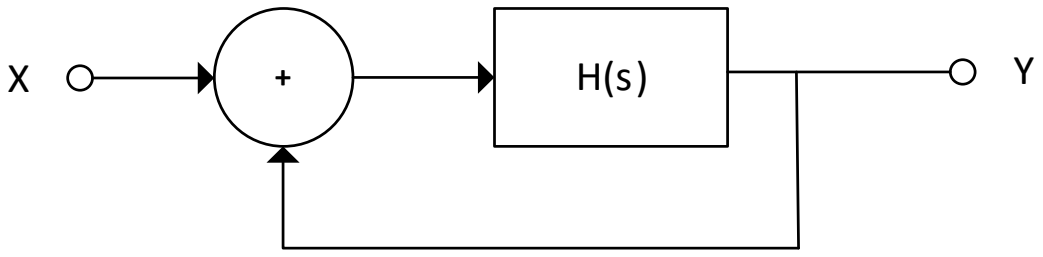

Figure 5.1 : A simple feedback system.

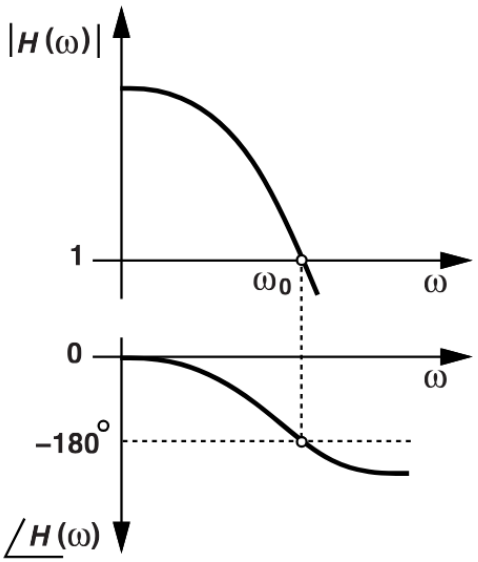

Figure 5.2 : Open-loop frequency response.

To achieve sustained oscillation in such a system, Barkhausen's criteria must be satisfied. These criteria define two fundamental conditions for an oscillatory system: the loop gain must be equal to unity and the total phase shift around the loop must be either 0° or an integer multiple of 360°. Writing the closed-loop transfer function of the negative feedback loop as

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 + H(s)} \tag{5.1}$$

If $H(s) = -1$, the denominator falls to zero. If the applied input is a sinusoid in this system, then s = jω_0 and $H(s) = -1$ indicating a unity magnitude with a 180^o phase shift at ω_0. The loop contains 180^o phase shift due to the nominally negative feedback and another 180^o phase shift which arises from H(s). Therefore, the total phase shift of 360^o proves that the signal reinforces itself as it propagates through the feedback loop. Therefore, the system satisfies Barkhausen's criteria. We can note that $H(s) = -1$ is a startup condition and the total phase shift of the system should be 360^o.

In summary, the fundamental conditions for oscillation are established by Barkhausen's criteria, which state that a system must exhibit a loop gain equal to or greater than one and a total phase shift of 0° or 360° for sustained oscillation. These criteria form the theoretical basis for designing stable oscillators. There are two primary oscillator topologies utilized in integrated circuit design: LC oscillators and ring oscillators. While LC oscillators are often selected for their superior phase noise

characteristics, ring oscillators are widely adopted in digital and low-power systems due to their compact layout and broad tuning range [8].

5.1.1 Ring oscillators

A ring oscillator consists of a chain of delay stages, typically inverting amplifiers, connected in series. The output of each stage is fed into the next stage which creates a chain. The output of the final stage is looped back to the input of the first stage, forming a closed feedback loop. Oscillation occurs as each stage introduces a phase delay in accordance to the number of stages used in the loop. The total phase shift around the loop achieves 180°, the other 180° phase shift provided by the feedback path hence the Barkhausen criterion is satisfied, resulting in sustained oscillation. To begin a basic analysis of the ring oscillator, a representative example examined in [8] is illustrated in Figure 5.3. The ring oscillator consists of multiple common-source amplifier stages, each functioning as an inverting element. These stages invert the input signal, resulting in the transfer function of $H(s) = -1$ which is indicated as $-H(s)$ block in the figure.

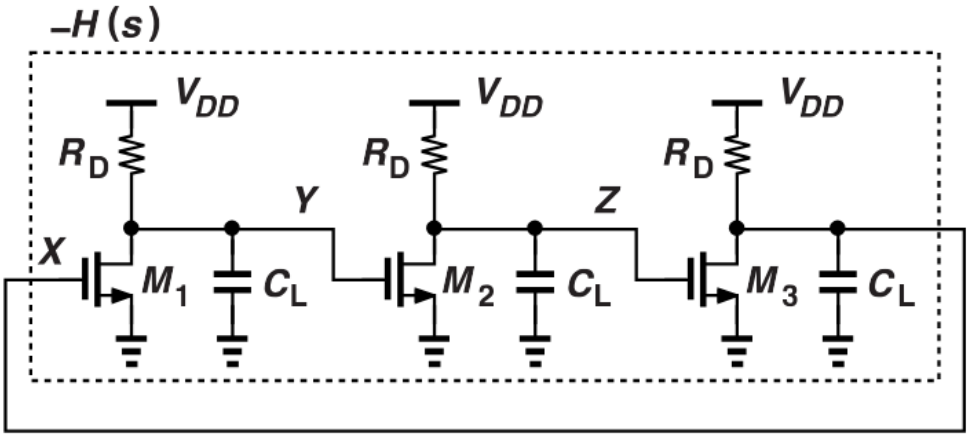

Figure 5.3 : Three stage simple ring oscillator.

Each identical chain connected in series results in a transfer function as follows.

$$H(s) = \left(\frac{g_m R_d}{R_d C_L s + 1}\right)^3 \tag{5.2}$$

where g_m represents the transconductance of the each transistors M_1, M_2 and M_3 that are assumed identical. The corresponding magnitude and phase behavior is shown in Figure 5.4. Having three poles in the system results -30 dB/decade in the slope of the magnitude plot and -270^o phase difference. It is worth to note that each stage

contributes a phase shift of 60^o arising from its output pole plus 180^o phase shift due to the nature of the inversion in the loop results in a 240^o phase seperation between each stages. For $|H(j\omega_0)|$ = 1, the transfer function becomes as in (5.3). The loop follows the unity loop gain condition in Barkhausen's criteria.

$$\left(\frac{g_m R_d}{\sqrt{R_d C_L j\omega_0 + 1}}\right)^3 = 1 \tag{5.3}$$

Solving (5.3) for ω_0, it becomes

$$\omega_0 = \frac{\sqrt{g_m^2 R_d^2 - 1}}{R_d C_L} \tag{5.4}$$

We can also analyze the phase shift of -180^o as

$$\tan^{-1}(R_d C_L \omega_0) = \frac{180^\circ}{3} = 60^o \tag{5.5}$$

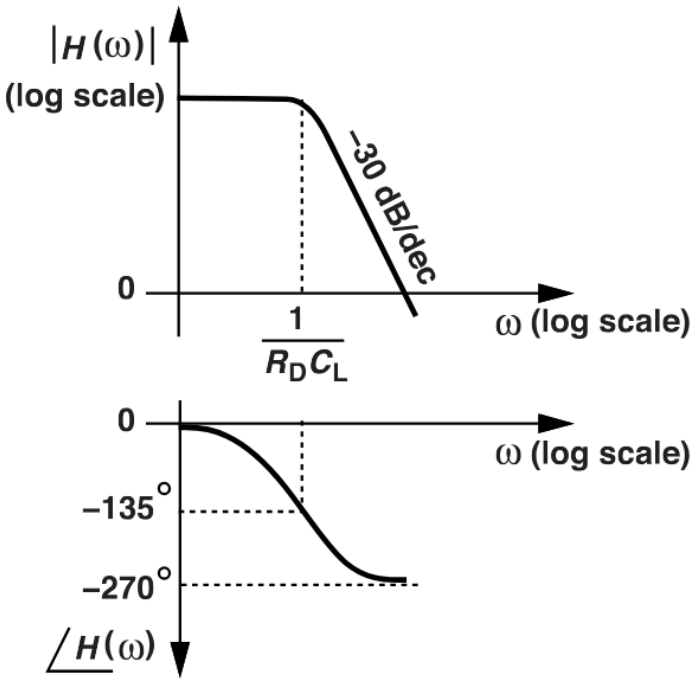

Figure 5.4 : Magnitude and phase response of a ring oscillator.

Hence,

$$\omega_0 = \frac{\sqrt{3}}{R_d C_L} \tag{5.6}$$

Additionally, combining (5.4) and (5.6) results in (5.7) which suggests that each stage must provide a voltage gain of 2 to ensure oscillation. Besides that using (5.4) and (5.5), we can generalize the oscillation criteria for N-stage ring oscillator as depicted in (5.8) where N is the number of stages in the ring oscillator.

$$g_m R_D = 2 \tag{5.7}$$

$$g_m R_D = \sqrt{\tan^2 \frac{180^o}{N} + 1} \tag{5.8}$$

N-stage ring oscillator must consist of an odd number of stages because the phase shift contributed by the stages must be 180°. However, even number of stages provide 360° phase shift which results in no inversion around the loop, hence failing to satisfy the Barkhausen's criteria for oscillation in a purely inverting ring structure.

Ring oscillators can be implemented using CMOS inverters instead of common-source amplifiers in gain stages. Figure 5.5 illustrates a three-stage inverter-based ring oscillator. In this architecture, oscillation is sustained through the cumulative propagation delay, t_d, of the stages. The propagation delay introduces the necessary phase shift in this architecture. Thus, the number of inverter stages directly influences the phase shift required per stage to satisfy the oscillation condition.

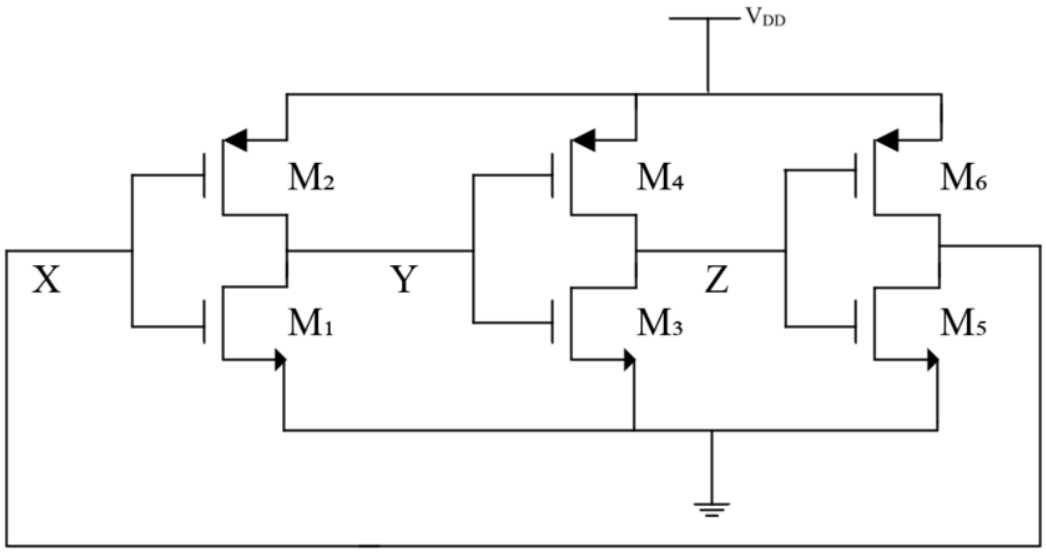

Figure 5.5 : Three-stage inverted-based ring oscillator.

Since the phase shift of 180° is necessary from the stages for sustained oscillation, each stage in Figure 5.5 must contribute a 60° phase shift. As the other 180° is provided by the loop itself, the oscillation frequncy can be calculated as

$$f_{osc} = \frac{1}{2Nt_d} \tag{5.9}$$

where N is the number of stages which is 3 for the topology in Figure 5.5. The propagation delay, td, can be interpreted as the time it takes for a signal transition to propagate through a single inverter stage.

We can define the propagation delay time as the maximum time interval required for the input signal to reach its 50% threshold level and cause the output signal to cross its own 50% threshold level. Then, t_d can be calculated

$$t_d = \frac{C_L V_{th}}{I_{out}} \tag{5.10}$$

where I_{out} is the output current, C_L is the capacitor load and V_{th} is the threshold voltage of the device. The excess phase noise of this structure modelled in [8] is

$$\varphi_{n,osc}(t) = \int 2\pi \frac{f_{osc}}{\pi}\, \varphi_{n,d}(t)dt \tag{5.11}$$

where $\varphi_{n,osc}(t)$ is the total excess phase noise of the oscillator and $\varphi_{n,d}(t)$ is the total excess phase noise of the delay contributed by each stage.

In CMOS inverter-type ring oscillator, the delay of an inverter decreases if the supply voltage increases as (5.10) is directly proportional to the transistor's current leading a dependency on the supply voltage. Combining (5.09) and (5.10) suggests that the oscillation frequency is inversely proportional to the supply voltage. Therefore, the supply dependency is leading to a significant challenge for many applications due to its impact on frequency stability [8]. Secondly, each inverter consumes an average power of $f_0 C_L V_{DD}^2$. Consequently, for an n-stage ring oscillator, the total power consumption becomes $nf_0 C_L V_{DD}^2$. Lastly, inverter-type ring oscillators suffer from phase noise due to their inherently low quality factor as mentioned in [8]. Additionally, (5.11) implies that the noise contributed by each stage accumulates over time, resulting in $\varphi_{n,d}(t)$, a cumulative increase in the total excess phase noise of the oscillator which

degrades the overall output signal. One method used in [8] is to mitigate this issue is increasing the number of stages. However, this approach leads to higher power consumption and resulting a trade-off between phase noise and power dissipation. Another widely used alternatives over inverted-based ring oscillator is the differential ring oscillator. Unlike single-ended designs, differential ring oscillators utilize pairs of differential delay stages. This architecture allows for better common-mode noise rejection. Moreover, the symmetric structure of differential ring oscillators contributes to more balanced signal propagation. Figure 5.6 presents three-stage differential ring oscillator where each stage provides 60° of phase shift. As a result, the circuit generates six output phase in 6 steps. This benefits for the applications require phase seperation.

The differential ring oscillator exhibits supply voltage dependence only due to the drain-substrate junction capacitances of the transistors. Fluctuations in the supply voltage influence the common-mode level at each output stage, which are then transferred through these capacitances. However, the supply sensitivity in differentialring oscillators is significantly lower than in inverted-type ring oscillator because the drain current in each differential stage is provided by a supply-independent constant current source.

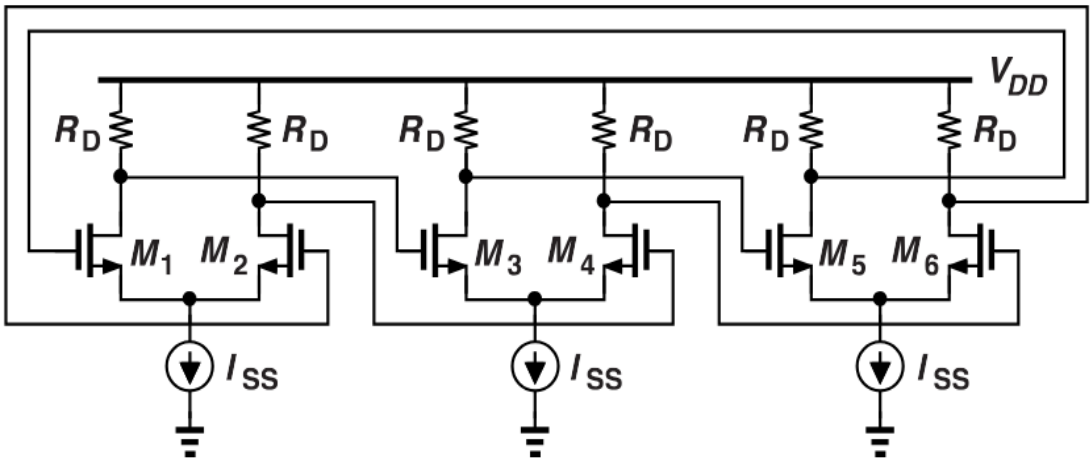

Figure 5.6 : Three-stage differential ring oscillator.

The comparison between inverter-type and differential-type ring oscillators is studied in [8] which shows that inverter-type ring oscillators offer a better trade-off between phase noise and power consumption whereas differential-type ring oscillators demonstrate greater resilience to supply voltage fluctuations. Therefore, inverted-type ring oscillator are oftenly preferred in applications where optimizing phase noise and power consumption is more critical and the supply noise is either negligible or can be

effectively filtered. The differential-type ring oscillators are well-suited for environments with high supply noise.

5.1.2 LC oscillators

LC oscillators are a widely used type of oscillator that can generate periodic signals by exploiting the natural resonance frequency of an inductor-capacitor (LC) tank circuit. The resonant nature of LC oscillators allows them producing cleaner and more spectrally pure signals compared to ring oscillators operating under similar power condition. However, they typically require more chip area and can be more complex to design. A design of a LC oscillator begins with establishing a resonating LC tank which compose of a parallel inductor and capacitor. As shown in Figure 5.7, an ideal parallel LC tank exhibits an impedence that behave inductively at low frequencies and capacitively at high frequencies. At the resonance frequency, the inductive and capacitive reactances cancel each other out and the impedance approaches infinity.

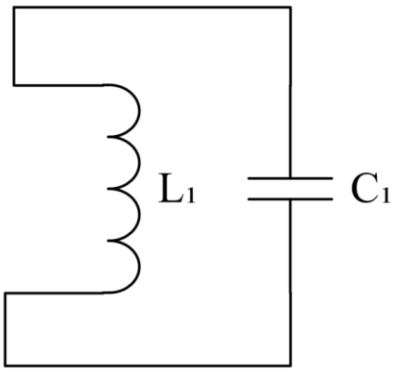

Figure 5.7 : An ideal parallel LC tank.

The impedance of an ideal LC tank at the resonance frequency can be expressed as

$$Z_1(j\omega_0) = \frac{j\omega_0 L_1}{1 - \omega_0^2 L_1 C_1} \tag{5.12}$$

where ω_0 is the resonance frequency and is shown in Figure 5.8.

The imaginary part of impedance at resonance frequency cancel each other out, thus the resonance frequency becomes

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}}. \tag{5.13}$$

If we model the inductor with practical values, it includes a series resistance, R_S, with L_1, making the tank lossy. This resistance arises from the parasitic losses of the inductor due to the finite conductivity of the inductor's winding material. Figure 5.9 represents the circuit implementation of the lossy LC tank. We can interpret L_1 and R_S in terms of parallel representation of each other as L_P and R_P respectively in

$$L_1 s + R_S = \frac{L_P R_P s}{L_P s + R_P}. \tag{5.14}$$

Calculating R_P and L_P from (5.14) assuming $s = j\omega$

$$R_P = \frac{L_1^2 \omega^2}{R_S} \tag{5.15}$$

$$L_P = \frac{R_S^2}{L_1 \omega^2} + L_1^2 \tag{5.16}$$

where the ideal LC tank has R_S and R_P which are approximated as zero and infinity. Therefore, a lower R_S or a higher R_P leads the tank more ideal.

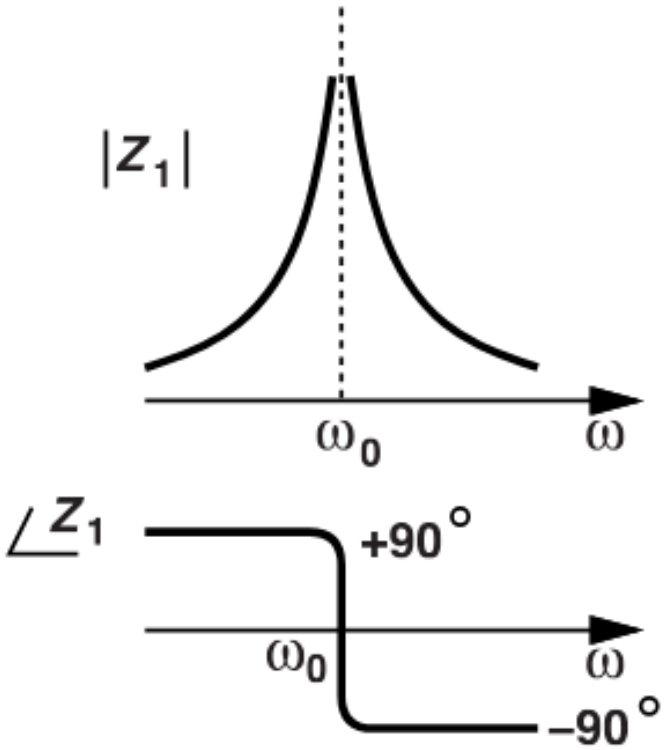

Figure 5.8 : Impedance characteristics of an ideal parallel LC tank.

We now calculate the impedance of the lossy LC tank at the resonance frequency as

$$Z_1(j\omega_0) = \frac{j\mathrm{R_P}L_1\omega_0}{R_P(1 - L_1C_1\omega_0^2) + jL_1\omega_0}. \tag{5.17}$$

In the absence of the resistance, the ideal circuit would oscillate indefinitely once initiated. The presence of R_S leads to thermal dissipation of energy. Thus, the quality factor (Q) of the tank reduces and therefore the oscillation amplitude decays over time if not compensated. This impacts the oscillator's performance, therefore, high-Q component selection is essential when designing LC oscillators.

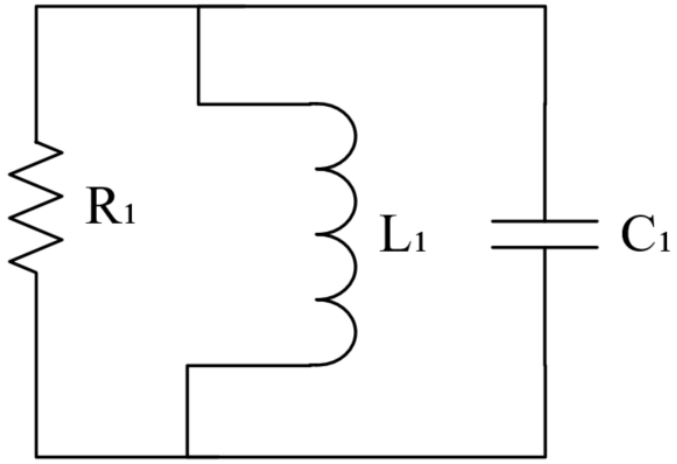

Figure 5.9 : A lossy LC tank.

The quality factor determines how efficiently an inductor stores energy relatively how much it dissipates. A higher Q indicates a lower energy loss and thus a better inductor performance. Q can be defined as

$$Q = \frac{L\omega}{\mathrm{R_S}} = \frac{R_P}{L\omega}. \tag{5.18}$$

Q is linearly proportional to the frequency of interest. If the relationship between R_S and the frequency of interest are independent, Q increases when the frequency increases. Thus, inductors operating at high frequencies exhibits higher quality factors.

This tank configuration serves as the foundation for high-performance oscillator topologies due to its frequency selectivity characteristics. However, real components introduce losses as a characteristics. To lower the effect, we require an active circuit to compensate for the energy. Besides that, this LC tank topology only provides 180°

of phase shift as depicted in Figure 5.10. According to Barkhausen's criteria mentioned previously, we must establish 360° of phase shift.

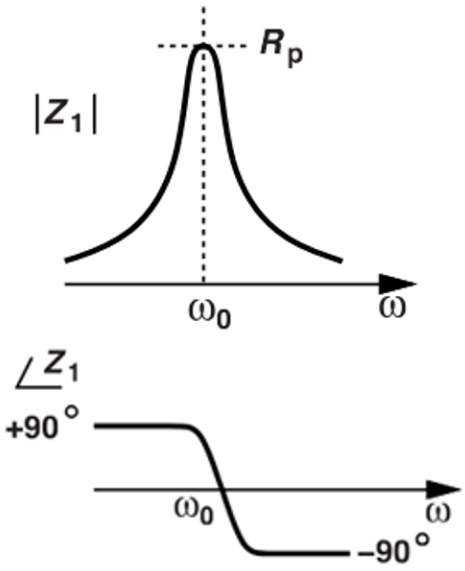

Figure 5.10 : Impedance characteristics of a lossy LC tank.

One method is to cascade two identical LC tanks as shown in Figure 5.11. The output resistance of the cross-coupled pair is -2/gm which cancels out part of the undesired positive resistance at the inductor's end. This configuration exhibits 180° of phase shift each stage, resulting 360° of phase shift around the loop.

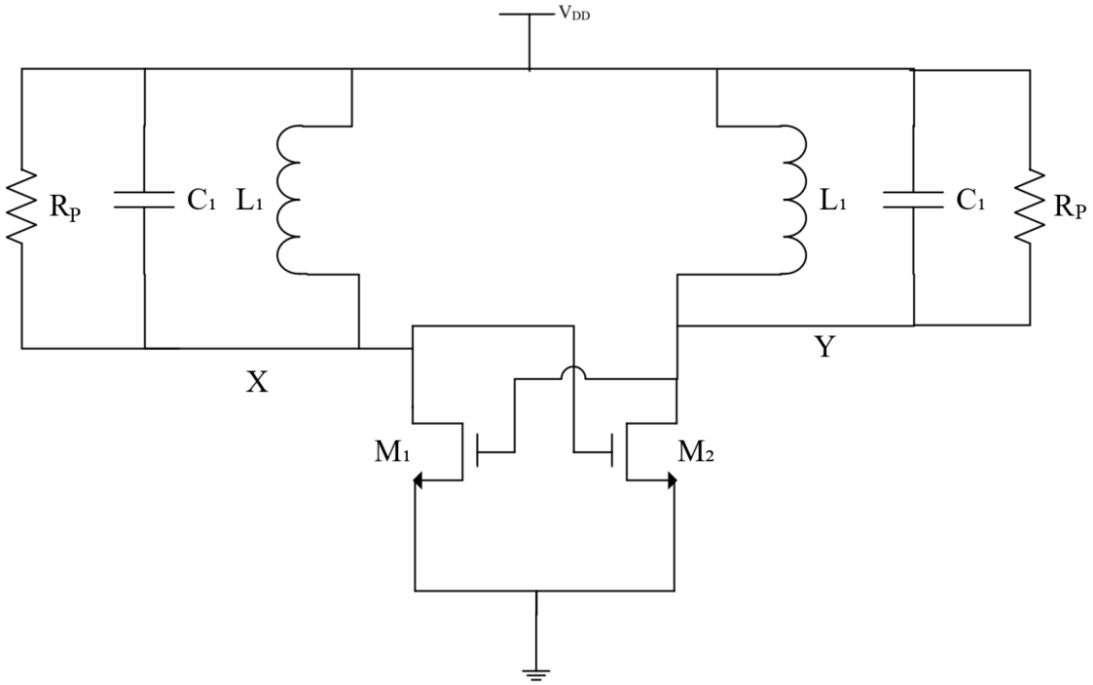

Figure 5.11 : Two cascaded LC tank in a loop with cross-coupled amplifiers.

Additionally, each stage contributes the gain of g_mR_P, thus the magnitude of the open-loop transfer function is $(g_mR_P)^2$ at the resonance frequency. For this topology to oscillate, we require the total gain, $(g_mR_P)^2$, must be greater or equal to 1 which can be achieved. Thus, this topology follows Barkhausen's criteria.

To examine the impedance of this topology, we can draw the small-signal model in Figure 5.12. The small-signal model shows the current injected by the tanks is zero. Therefore, summation of the dependent current sources becomes

$$g_m V_X + g_m V_Y = 0. \tag{5.19}$$

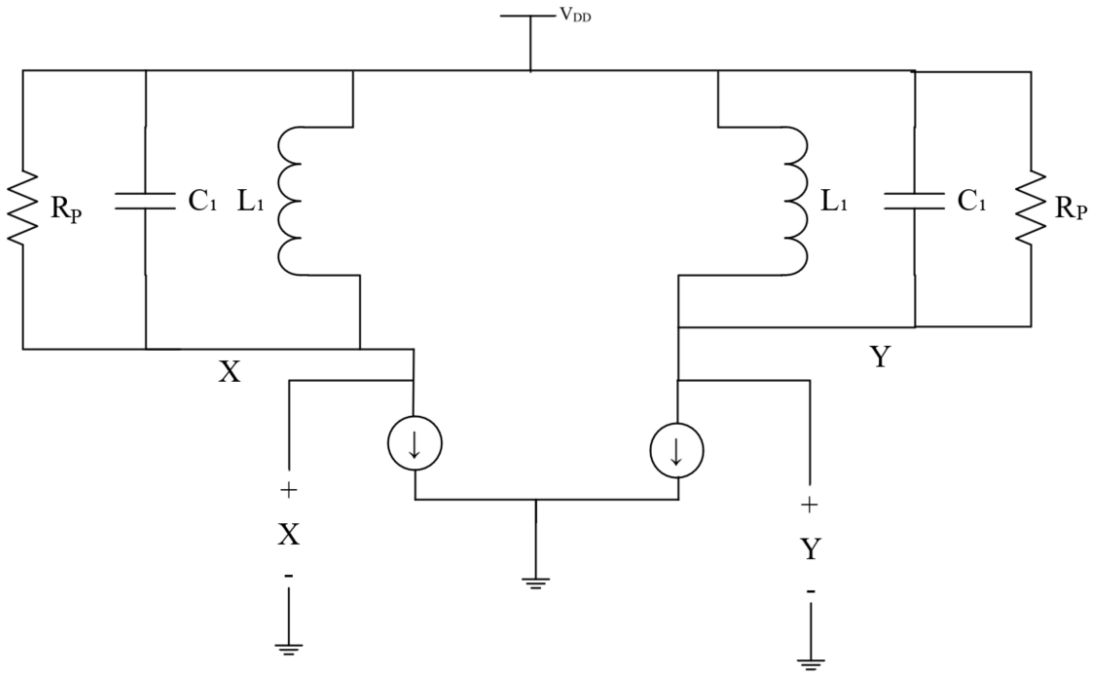

Figure 5.12 : Small-signal model of two cascaded LC tank.

For oscillation to occur, the total impedance seen by the LC tank must approach infinity at the resonance frequency like in the ideal case scenario shown in Figure 5.8. In the ideal LC tank, the inductive and capacitive reactances cancel each other, resulting in theoretically infinite impedance. Thus, the total impedance can be written as

$$Z(j\omega) = \frac{j(2L_1\omega)}{1 - L_1C_1\omega^2 + \frac{j(L_1\omega)(1 - R_P g_m)}{R_P}}. \tag{5.20}$$

The total impedance approaches infinity if $\omega = 1/\sqrt{L_1 C_1}$ and $1 - R_p g_m = 0$. As a result, this condition satisfies Barkhausen's criteria for the gain as $g_m R_P = 1$. However, the transconductance is dependent to the supply voltage as

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{th}). \tag{5.21}$$

Thus, any change or fluctuation in the supply voltage influences g_m, leading the gain degrade and may fail the oscillation. To solve this issue, a tail current source added in this topology. The primary purpose of the tail current source is to provide a stable and bias-controlled current to the differential pair. We can calculate the peak output voltage swings of this topology. The fundamental harmonic of the oscillation primarily sees the high impedance of the structure which is dominated by the series resistance R_S, whereas other harmonics encounter significantly lower impedance paths. Therefore, focusing on the fundamental harmonic defines the output voltage as depicted in (5.22). The noise analysis of this topology arises from the unideal model of the inductor in the LC tank and cross-coupled pairs.

$$V_0 = \frac{4}{\pi} R_P I_{SS} \tag{5.22}$$

As analysed in [8], the trade-off between phase noise and power consumption of this topology is

$$S_{\varphi n}(f)P = \frac{\frac{\sqrt{2}}{2}\gamma + 1}{\alpha} 2\pi k_B T \left(\frac{f_0}{2Qf}\right)^2 \tag{5.23}$$

where $S_{\varphi n}(f)$ is phase noise, $P = I_{total} V_{DD}$ is the power consumption, I_{total} is the total current and α is assumed as a fraction parameter where $V_0 = \alpha V_{DD}$.

5.1.3 Comparison of ring and LC oscillators

Ring and LC oscillators are analyzed extensively due to their fundamental importance in oscillator design. These two types exhibit fundamentally different characteristics in terms of phase noise, power consumption, and output voltage swing. Understanding these trade-offs is critical in selecting the appropriate oscillator architecture for this thesis. LC Oscillators typically exhibit significantly lower phase noise compared to

ring oscillators. This advantage stems from the presence of a high-Q resonant tank, which filters out noise components and stores energy efficiently. As depicted a design project in [8], the ring oscillator performs around -100 dBc at 1 MHz offset however, the LC oscillator performs around -110 dBc at 1MHz offset. Another study in [16] results that LC oscillators are more power efficient than ring oscillators.

To conclude, the analysis and the literature lead that LC oscillator have more advantages than ring oscillators for this thesis. As phase noise and power consumption are essential in the scope of work, this thesis utilizes LC VCO.

5.1.4 Voltage-controlled LC oscillator

After establishing oscillation in the system, it becomes essential to control the output frequency. A common challenge in oscillator circuits is frequency drift over time, which can result from variations in the supply voltage or other environmental factors [8]. Additionally, noise becomes a significant concern, especially if the oscillator operates at high frequencies which potentially causes unwanted frequency deviations at the output. To address these issues, oscillators employed with a controlled voltage, enabling dynamic control of the oscillation frequency through an input control voltage.

There are multiple methods to control the frequency of oscillation in the circuit. One commonly used approach is to incorporate a voltage-controlled capacitance element, known as a varactor. The varactor adjusts its capacitance in response to changes in the control voltage thus the resonant frequency of the oscillator circuit can be modified. This variation in capacitance directly results in a shift in the oscillation frequency, enabling precise tuning of the output signal.

Voltage applied to a varactor versus capacitance of varactor is simulated using the Cadence Virtuoso tool. Figure 5.13 illustrates the capacitance characteristics of moscap_rf component with a neutral capacitance of 48 fF available under TSMC 65 nm PDK library. The figure represents the variation in capacitance as a function of the applied DC voltage with the variations are shown. As observed in the figure, the capacitance of the varactor exhibits a variation across the full supply voltage range.

Notably, the region between 200 mV and 610 mV shows a significant change, making the varactor a strong candidate for tuning the resonance frequency of the LC tank. Furthermore, the slope of the capacitance–voltage characteristic, denoted as 's' in the

figure, indicates that the capacitance variation between 401 mV and 610 mV is the most efficient. In this range, the slope is relatively linear, making it an ideal operating region for control voltage selection in VCO design.

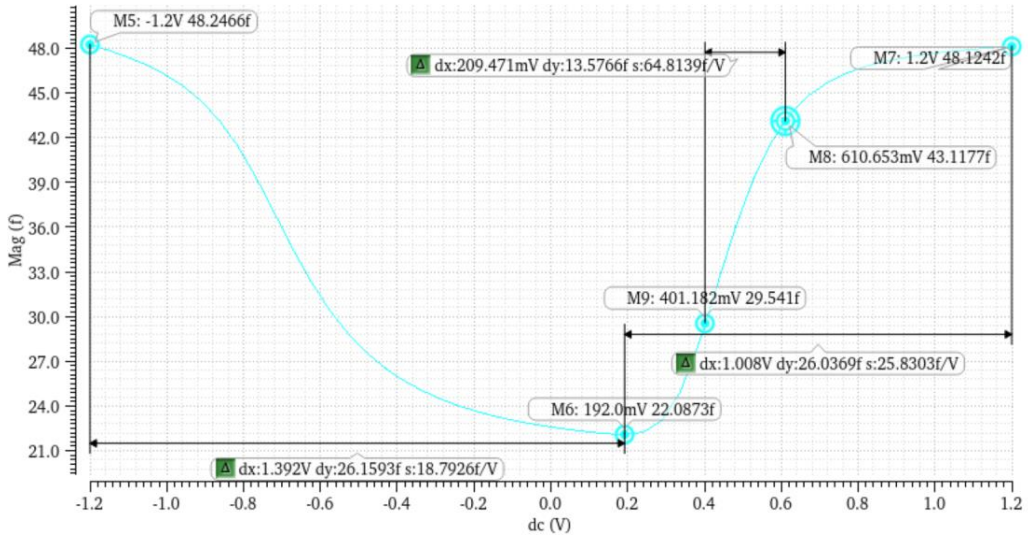

Figure 5.13 : Capacitance-voltage curve of a varactor.

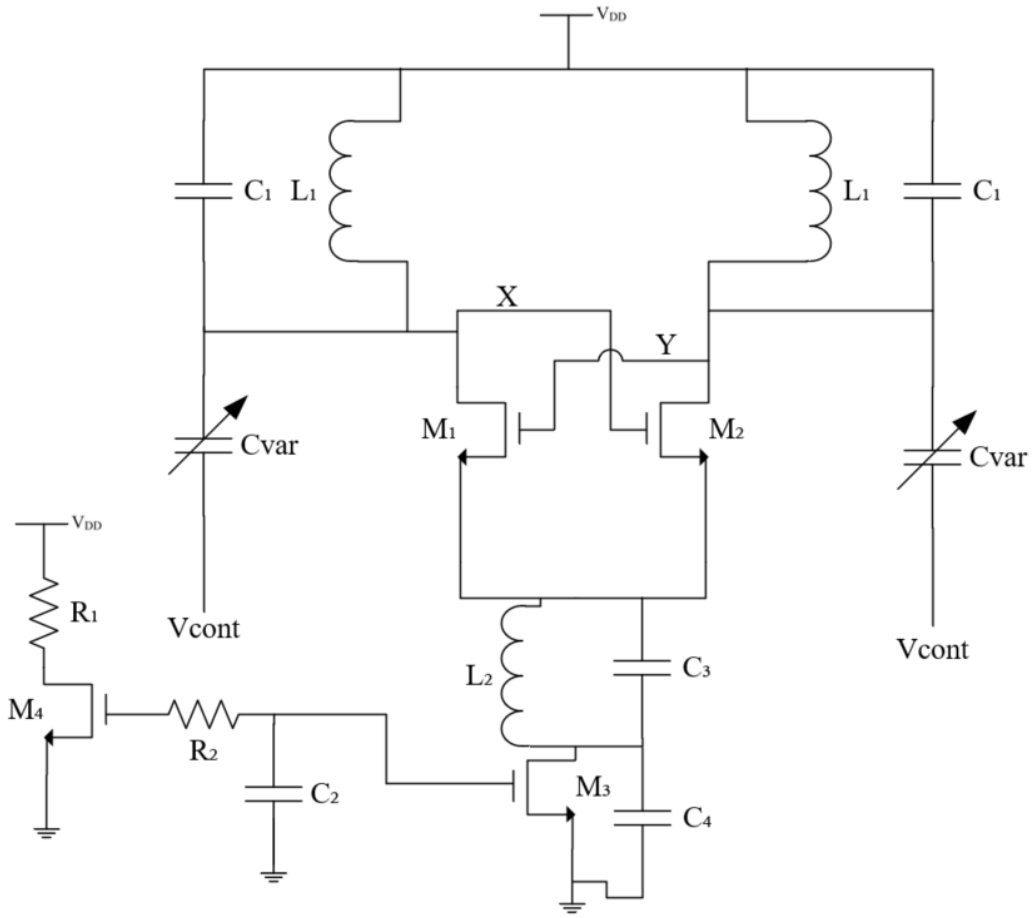

Figure 5.14 : Circuit implementation of the VCO.

5.1.5 The design of LC VCO

The design of the VCO builds upon the preceding discussions and is illustrated in Figure 5.14. The current- and voltage-limited regions are tested for this design. Choosing the current-limited region provides a suitable switching mechanism for the transistor to avoid entering triode region. The current- and voltage-limited regime is simulated and illustrated as Figure 5.15. The VCO enters to voltage-limited region where tail current reaches to 2 mA. Therefore, the tail current needs to be selected below 2 mA to ensure VCO is operating in current-limited.

The minimum and maximum peak output voltages are chosen as 1 V and 1.4 V, respectively. To meet the power budget constraints and operating regime, the tail current I_{SS} is set to 1.4 mA. Using (5.22), the equivalent parallel resistance R_P is calculated as 901.28 Ω. To achieve an output frequency of 3.8 GHz, a suitable inductor must be selected that not only supports this frequency but also minimizes chip area. Within the TSMC 65 nm technology, three types of inductors are available: standard spiral, symmetric spiral, and symmetric spiral with center tap. Based on the inductor parameters and valid values provided in [17], a symmetric sprial inductor is selected.

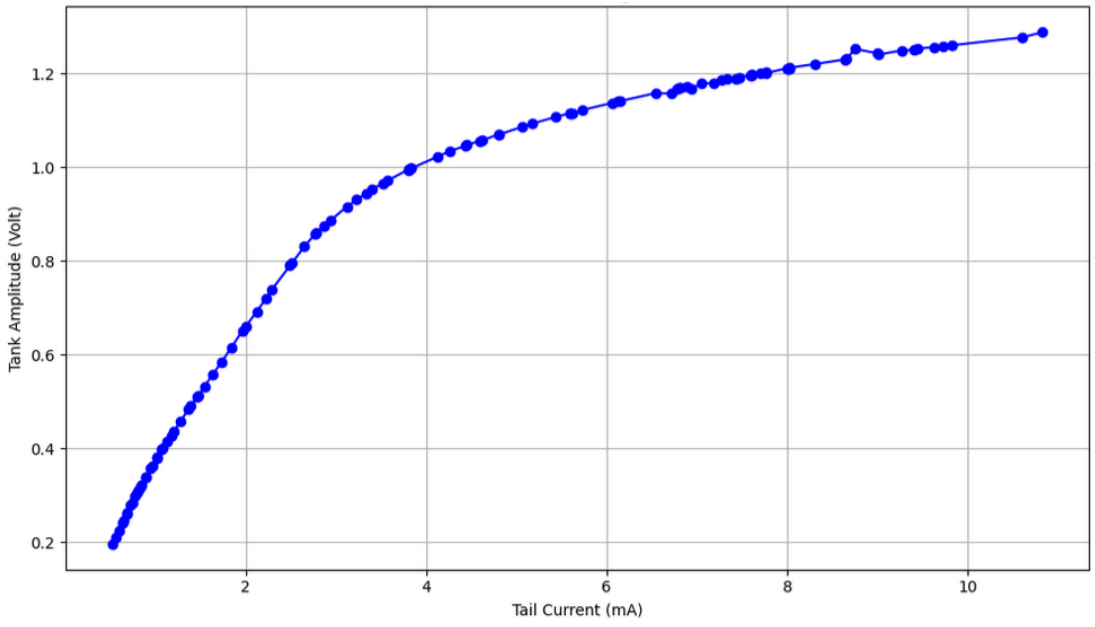

Figure 5.15 : Oscillator amplitude versus tail current to indicate current- and voltage-limited regimes.

This choice is motivated by the observation that it offers relatively stable quality factor performance across a range of frequencies, which is advantageous for ensuring consistent oscillator performance across the n78 band. Assuming a quality factor of 13

and applying Equation (5.15), the required inductance is calculated as 2.242 nH. Using this value and respecting the resonance condition given by Equation (5.13), the corresponding tank capacitance is derived as 0.9221 pF. To provide the required capacitance, the total effective capacitance seen by the LC tank is implemented as a combination of the varactor, the intrinsic capacitances of the cross-coupled pair, and additional fixed capacitors. As discussed in the previous section, the varactor's voltage capacitance characteristic plays a crucial role in tuning the oscillation frequency. Therefore, the frequency adjustment is primarily achieved through the varactor.

Additionally, the phase noise performance of the circuit is enhanced using L_2 and C_3, which suppress the noise introduced by cross-coupled transistor pairs at $2\boldsymbol{\omega_o}$. Moreover, C_4 is employed to reduce the noise contribution of the tail current source, while a low-pass filter centered at 10 MHz is incorporated into the biasing network of the tail current source to further suppress noise originating from that branch.A varactor with a neutral capacitance of 643 fF is selected. The varactor provides 850 fF capacitance at 3.5 GHz therefore, utilizing 53 fF static capacitors in the LC tank provide the resonance frequency. The free-running frequency of 3.5 GHz can also be achieved in steady state. The tuning range of VCO is illustrated in Figure 5.16. The control voltage between 422 mV to 1.16 V is required to tune the VCO in the desired n78 band. Bear in mind that cross couple pair also contributes to the total capacitance thus it must be taken into consideration as well.

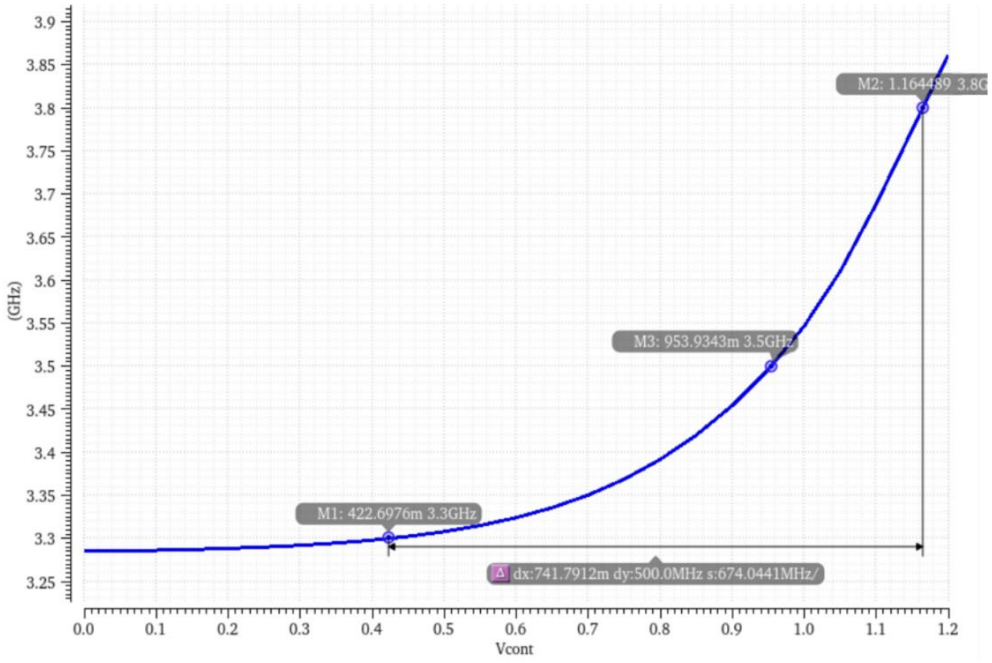

Figure 5.16 : Tuning range of the VCO.

The current output of VCO is illustrated in Figure 5.17. As I_{SS} assumed as 1.4 mA, the peak to peak current in one of sides reaches to 1.4 mA, the full I_{SS} current. Other side of the tail stays in cut-off region.

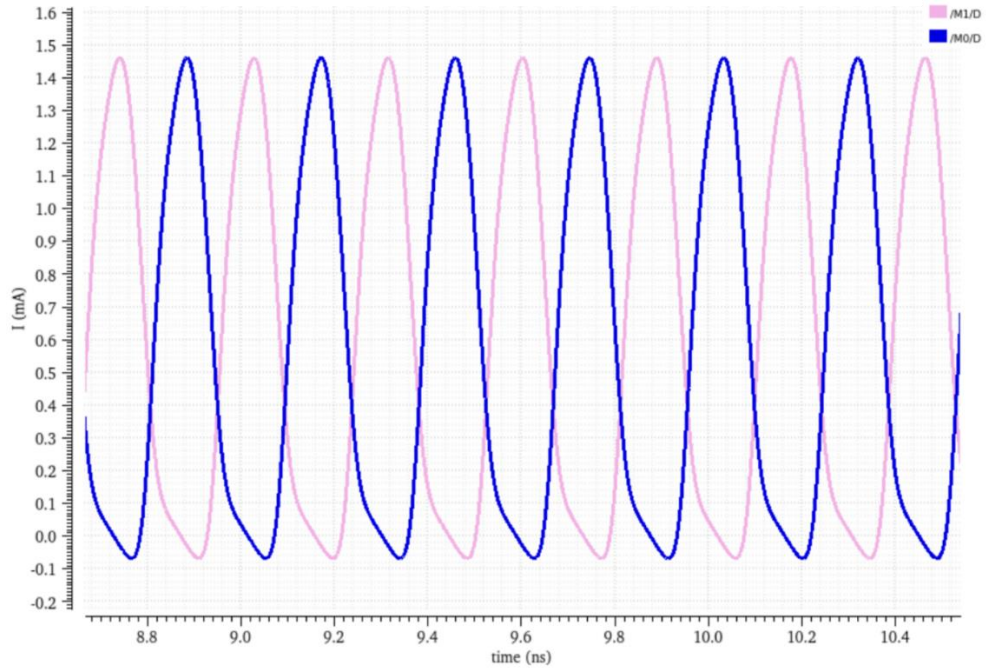

Figure 5.17 : The transient response of the cross coupled currents.

The phase noise of the designed VCO is measured as -120.2 dBc/Hz at a 1 MHz offset. It is illustrated in Figure 5.18.

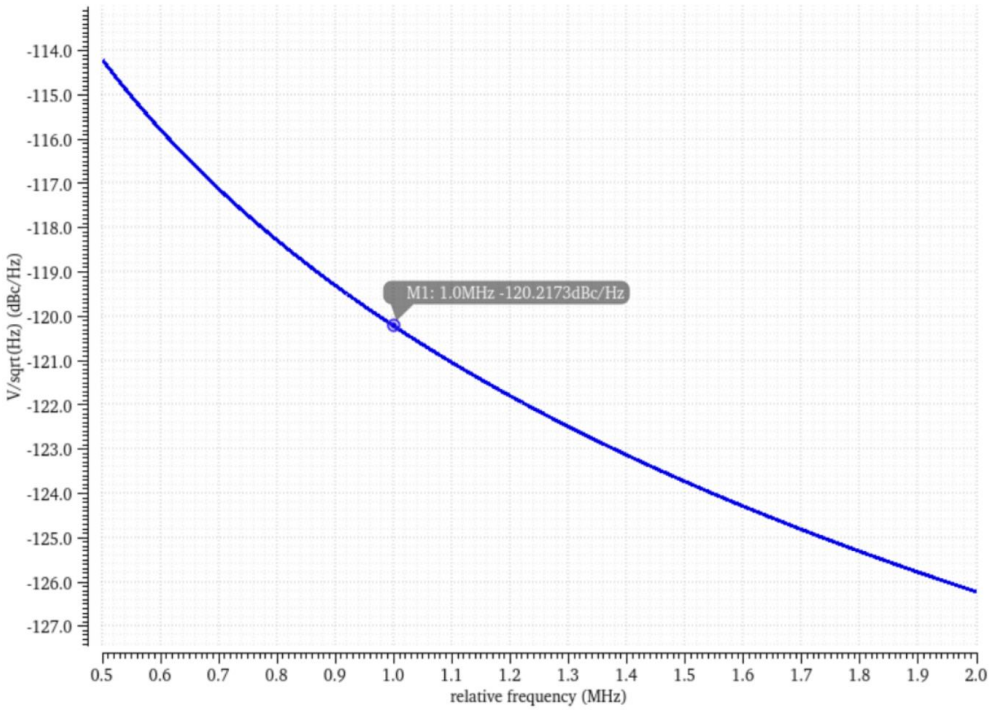

Figure 5.18 : The phase noise analysis of the VCO.

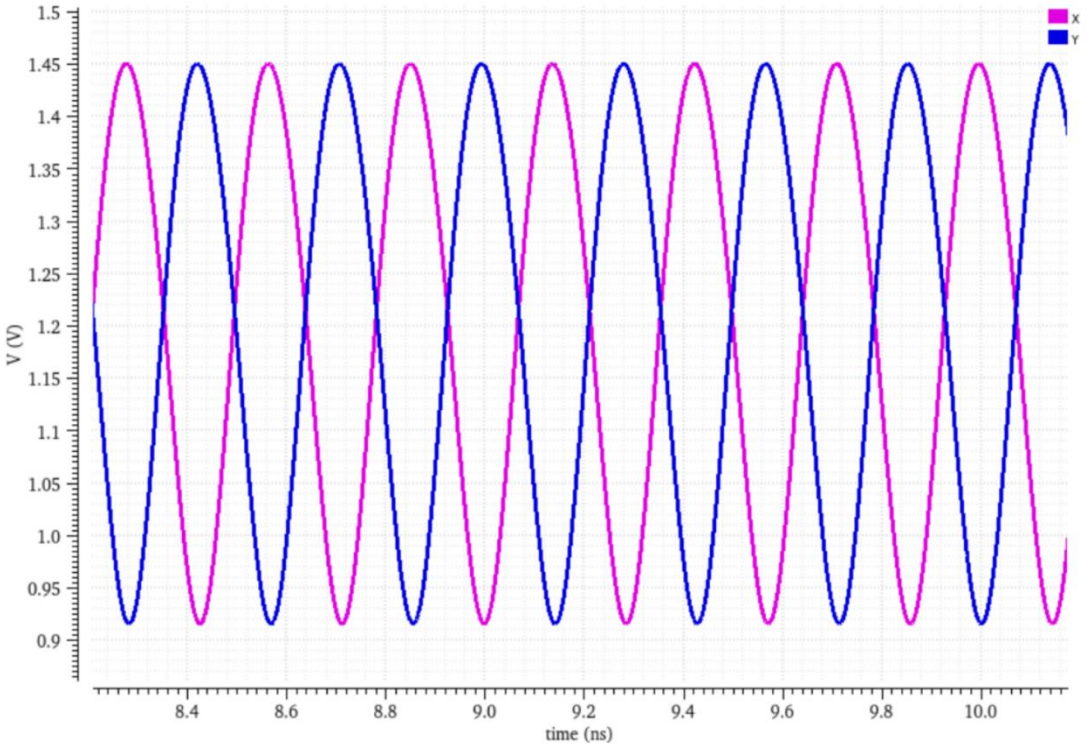

Figure 5.19 : The output voltage swing of the VCO.

Finally, the output voltage swing of the VCO ranges from 1.45 V to 0.92 V, successfully achieving the targeted output swing specification as shown in Figure 5.19.

5.2 Charge Pump and Loop Filter

The second essential building block in a PLL system is the charge pump. It serves as the interface between the PFD and the loop filter, converting digital phase or frequency error signals into corresponding analog current pulses. These current pulses are then integrated by the loop filter to adjust the control voltage of the VCO. A well-designed charge pump for a PLL system is crucial for achieving fast settling time and maintaining loop stability. In this section, the operational principles, design considerations, and performance metrics of charge pumps are explored, with an emphasis on current matching, switching behavior, and non-idealities that influence overall PLL performance.

5.2.1 Charge pump basics

A basic charge pump topology is shown in Figure 5.20 where V_{b1} and V_{b2} are the bias voltage required to keep M_1 and M_2 operating in saturation region. The signals $\overline{Up}$ and

Down are digital control signals generated by the PFD. Up emphasizes that M_3 turns on when Up is high and Down turns on M_4 when it is high. Therefore, we call M_3 and M_4 a switch where M_1 and M_2 are the current sources for them. Therefore, transistors M_3 and M_4 are referred to as switching transistors. Meanwhile, M_1 and M_2 act as the current sources that supply or draw current when the corresponding switches are activated. This configuration allows to control the current sources and switches to charge or discharge the capacitor C_1 called a loop filter which serves as the output node of the charge pump.

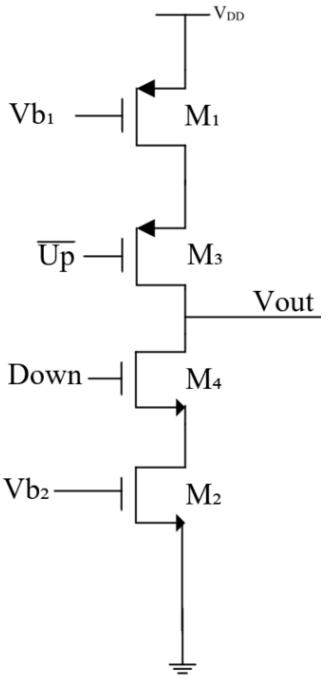

Figure 5.20 : Basic charge pump topology.

When both control signals, $\overline{\text{Up}}$ and Down, are at a low logic state, transistors M_3 and M_4 are turned off. As a result, there is no conduction path for current from either the upper current source or the lower current source to the output node. Consequently, transistors M_2 and M_4 cannot conduct, and V_{out} remains in a high-impedance state. Thus, this condition essentially holds the voltage at V_{out} constant.

When $\overline{\text{Up}}$ signal produces high while Down remains in low, M_1 and M_3 conducts whereas M_2 and M_4 are cut off thus the current in upper-side charges the capacitor. This charging current can be expressed as

$$I_{charge} = I_p = \frac{1}{2}\mu_p C_{ox}\frac{W_{M_1}}{L_{M_1}}\left(V_{b1} - |V_{th,M_1}|\right)^2 \tag{5.24}$$

where channel-modulation is neglected.

In a same fashion, when Down signal produces high while $\overline{\mathrm{Up}}$ remains in low, C_1 discharges through M_2 and M_4 creating discharge current only on the lower-side.

Then the current is expressed as

$$I_{discharge} = I_n = \frac{1}{2}\mu_n C_{ox}\frac{W_{M_2}}{L_{M_2}}\left(V_{b1} - V_{th,M_2}\right)^2 \tag{5.25}$$

where channel-modulation is also neglected.

The output voltage can be determined by the charging of the capacitor C_1 by the current, I_p, during the time interval, $\frac{\Delta\varphi_1}{2\pi}T_1$, when only the $\overline{\mathrm{Up}}$ signal is high. The resulting control voltage is calculated as

$$\Delta V_{cont} = \frac{\Delta\varphi_1}{2\pi}T_1\frac{I_p}{C_1} \tag{5.26}$$

where $\Delta\varphi_1$ represents the phase step difference of input signals' of PFD during which $\overline{\mathrm{Up}}$ signal is active and $\frac{I_p}{2\pi}$ is called the gain of charge pump, K_{PD}. In other words, $\frac{\Delta\varphi_1}{2\pi}T_1$ is the pulse width of the $\overline{\mathrm{Up}}$ signal. We will later explain in the PFD section that $\overline{\mathrm{Up}}$ is triggered for the exact duration of time the phase difference of PFD signals occurs. This time duration is translated to the pulsewidth of the signal $\overline{\mathrm{Up}}$. We can therefore express the transfer function of the charge pump for the input $\Delta\varphi_1$.

$$\frac{V_{cont}}{\Delta\varphi_1}(s) = \frac{I_p}{2\pi C_1 s} \tag{5.27}$$

As depicted in (5.27) that the transfer function contains a pole at the origin thus it functions as an ideal integrator. As discussed in Chapter 3, the loop filter increases the number of order and changes the type of a PLL. (5.27) shows that this architecture is called type-II PLL.

5.2.2 Loop filter

With the aid of Chapter 3, we know that the strategic placement of poles and zeros in a system's transfer function is crucial for achieving desired stability and dynamic performance. While increasing the number of zeros in a general control system can

indeed contribute to stability, the preference for Type-III passive loop filters in PLLs stems from their ability to offer zero steady-state phase error and improved noise performance, which are critical requirements for accurate frequency synthesis and tracking. Depicted in Figure 5.21, the transfer function for such a system is given as

$$\frac{V_{cont}}{\mathrm{I_{cp}}}(s) = \frac{s^2 R_1 R_2 C_1 C_2 + s(R_1 C_1 + R_2 C_2) + 1}{s^2(\, R_1 C_1 C_2 + R_2 C_1 C_2) + s(C_1 + C_2)}. \tag{5.28}$$

The presence of a pole at the origin, characteristic of a Type-II loop filter, provides integrator action. This integration ensures that any sustained phase error from the PFD,

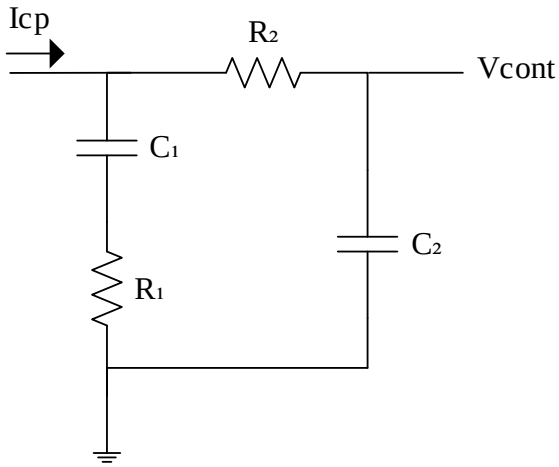

Figure 5.21 : Implementation of loop filter circuit described in (5.28).

which would otherwise produce a non-zero average charge pump current, is continuously integrated. As long as charge pump exists, the control voltage will continuously change, forcing the VCO frequency to adjust. This process continues until the phase difference detected by the PFD is driven to zero, at which point the average I_{CP} becomes zero. Consequently, the control output voltage stabilizes at a constant value, holding the VCO at the exact frequency required to maintain zero phase difference. The primary function of zero in (5.28) is to provide phase lead compensation. At frequencies above the zero's corner frequency, it contributes a phase lead of up to 90°. This phase lead effectively counteracts a portion of the phase lag introduced by the integrator pole which increases the overall phase margin of the PLL.

The careful placement of this zero is crucial for optimal loop performance. By positioning the zero's frequency strategically within the desired loop bandwidth, the phase margin can be significantly improved.

Beyond the critical pole at the origin and the primary zero, the transfer function of a typical type-II passive loop filter includes a second-order term in the numerator which arises directly from the specific network topology of the loop filter as it involves multiple reactive components. This term doesn't typically represent a second zero in the sense of providing additional phase lead, rather it is a consequence of the algebraic manipulation required to derive the overall transfer function from the interconnected passive components.

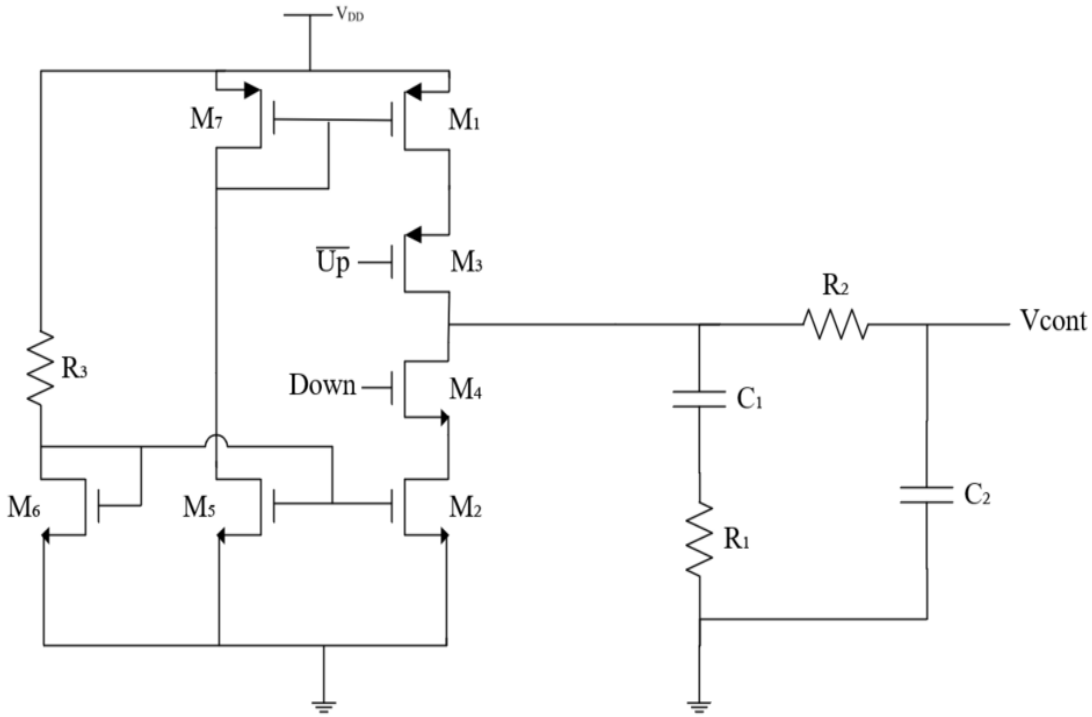

Figure 5.22 : The design of charge pump and loop filter circuit.

5.2.3 The circuit implementation of charge pump and loop filter

Figure 5.22 illustrates the implementation of the charge pump circuit along with its loop filter. The values of the capacitors C_1, C_2, R_1, R_2 are chosen by 18.1 pF, 9.7 pF, 100 kΩ and 25 kΩ, respectively. These components were chosen as such to meet the desired loop dynamics and stability criteria of the PLL system. Additionally, the output voltage is considered to meet the targeted control voltage value represented in the VCO design, as shown in Figure 5.15. Specifically, a control voltage of 445 mV is required to synthesize 3.3 GHz, while 1.13 V is necessary to reach 3.8 GHz. The free-running frequency of 3.5 GHz corresponds to a control voltage of approximately 940 mV. The output of the control voltage is illustrated in Figure 5.23 at idle state. The output voltage remains at 937 mV when Up and Down signals are logic zero.

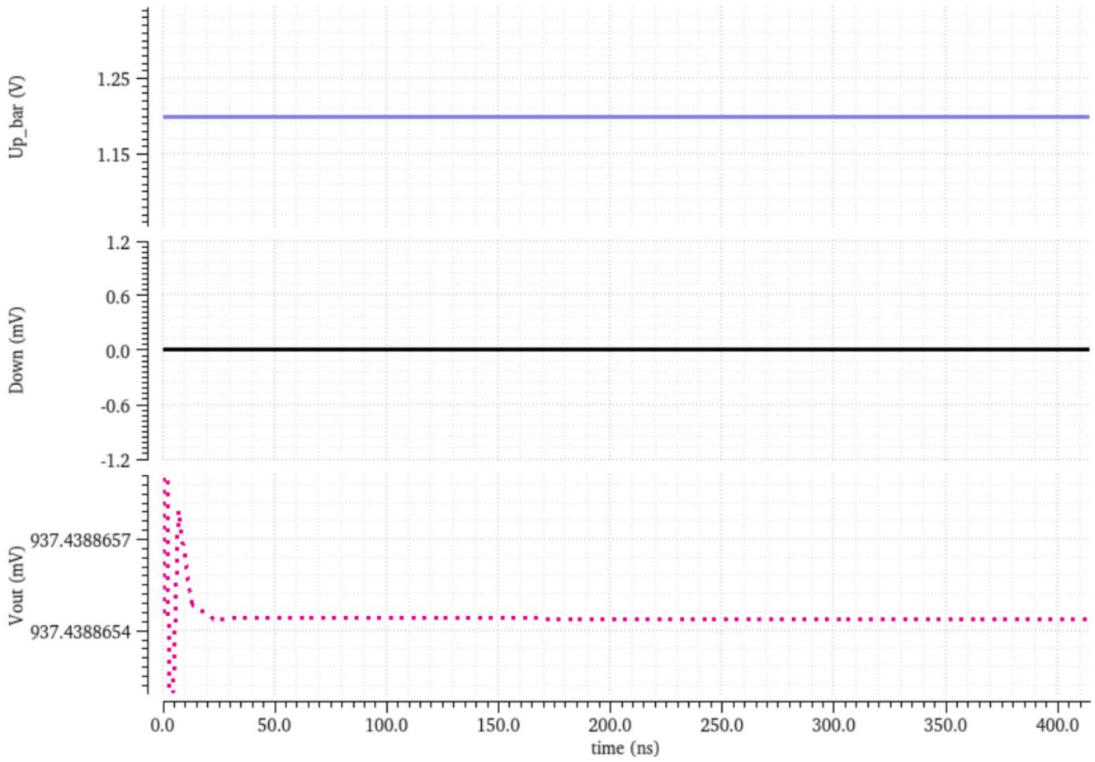

Figure 5.23 : The inputs and the output of the design of the charge pump and the loop filter at idle state.

If Up pulse generated from the PFD, the information passed through the transistor M_3, the pmos transistors turn on and the up side of the circuit conduct. However, M_4 is in off stage, only I_p is generated to charge the loop filter. Figure 5.24 represents the input voltages and the output voltage of the charge pump. The pulse widths of the Up signal translates into ramps in the output voltages. This indicates that there exist a phase or frequency difference of the reference and the feedback signals such that the VCO must increase its output frequency.

On the other hand, if the reference signal lags in phase or frequency to the feedback signal, Down is generated while Up remains low. In this case, M_4 turns on in saturation region, activating the down side of the charge pump to discharge the loop filter. The duration of time when Down is at high state is again translated into ramps in the control voltage as shown in Figure 5.25. The control voltage decreasing which decreases the capacitance of the varactor in the VCO design therefore the output frequency of VCO decreases until the time the loop locks.

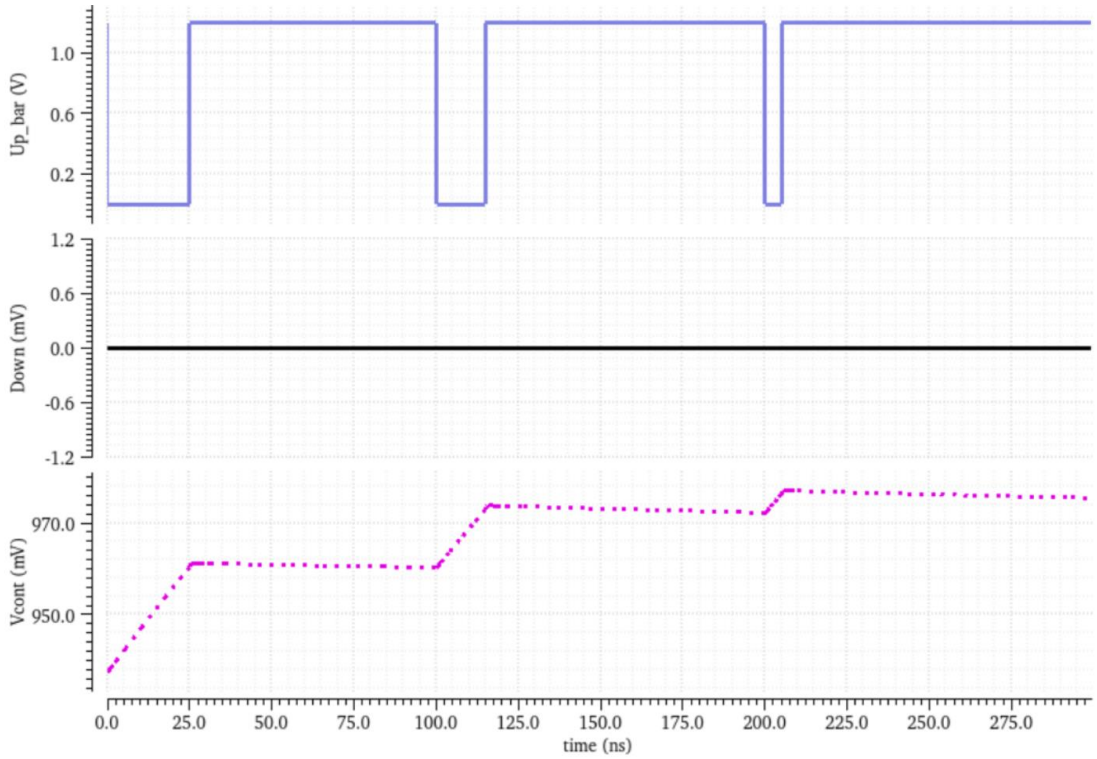

Figure 5.24 : The inputs and the output of the charge pump and the loop filter when Up is high and Down remains low.

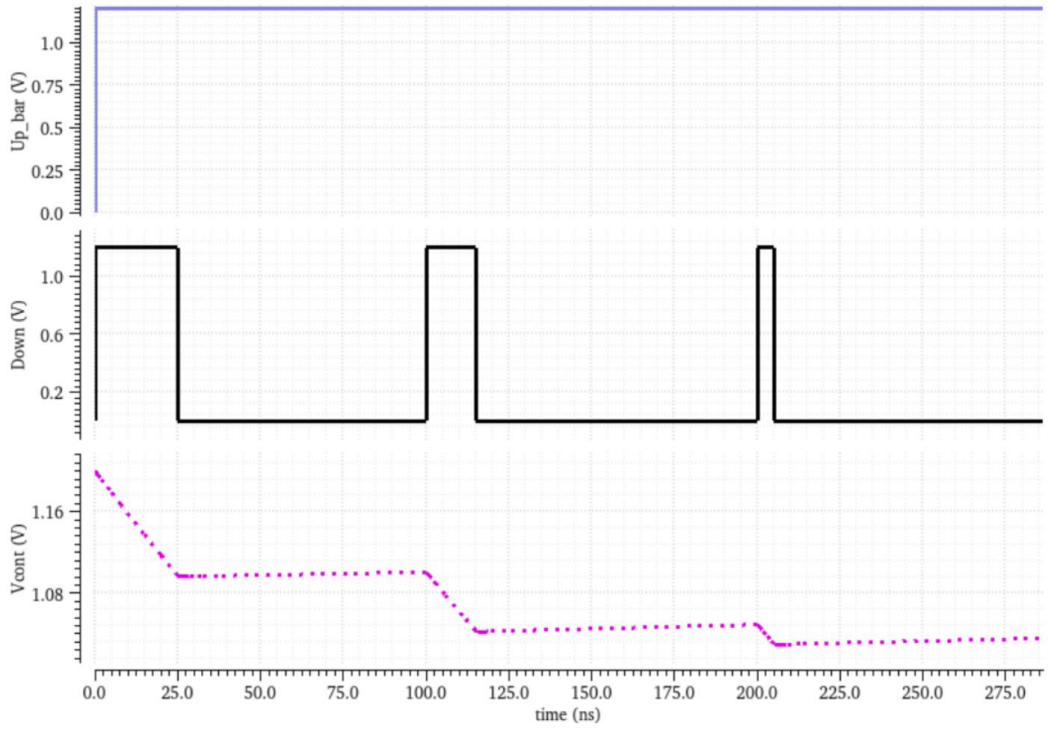

Figure 5.25 : The inputs and the output of the charge pump and the loop filter when Down is high and Up remains low.

5.3 Phase-Frequency Detector

PFDs are essential block in every PLL. A PFD compares the applied input signals and generates a DC output if there exists any phase or frequency difference between the applied input signals. Based on the transfer function analysis discussed in Chapter 3, a suitable PFD topologies can be proposed. For a fundamental understanding of this block, we begin with a basic PFD topology which is shown in Figure 5.26 where V_{Ref} is the applied reference signal, V_{Fb} is the feedback signal obtained by dividing the VCO output by N, Up is the output of PFD when V_{Ref} leads in phase or frequency to V_{Fb} and Down is the output of PFD when V_{Ref} lags V_{Fb}. There are two D flip-flops with their D inputs tied to logic high. The outputs of the flip-flops generate two non-overlapping signals called Up and Down which indicate whether the feedback signal

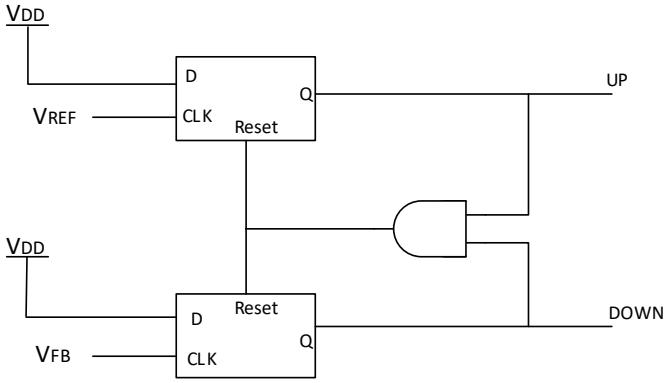

Figure 5.26 : A schematic diagram of a conventional PFD structure.

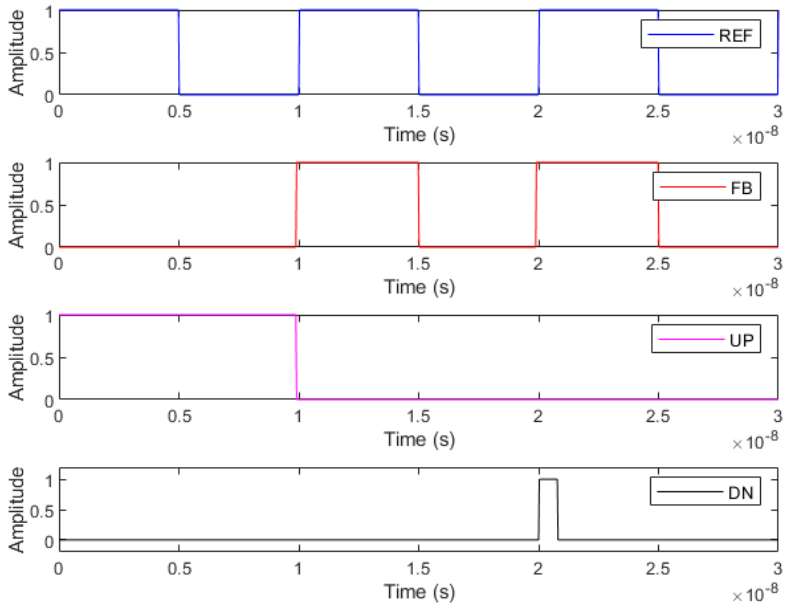

Figure 5.27 : Dead zone problem of a conventional PFD structure in near zero phase difference.

is leading or lagging the reference signal in phase or frequency. When either signal arrives first, the corresponding output goes high. This output is also used to feed AND gate that resets the flip-flops. Altought the simplicity of this architecture is beneficial from a design perspective, the reset procedure introduces an increase in the dead zone. The dead zone in a PFD is an important specification as it can lead to increase phase noise in the PLL. An example of dead zone behaviour in this architecture is illustrated in Figure 5.27. As shown, the Up signal is generated when the phase difference is close to zero. This is a falsely triggered output of PFD that can

element can be added at the reset path as shown in Figure 5.28. Even though adding the delay element helps eliminate the dead zone problem, it also reduces the maximum operating frequency of the PFD. As depicted in (5.29), increasing the duration of the reset path decreases the maximum operating frequency. This limitation arises because longer reset time reduce the speed at which the PFD can respond to input signal changes, hence constraining the overall performance of the PLL at higher frequencies.

$$f_{max} = \frac{1}{2T_{reset}} \tag{5.29}$$

Another issue in a PFD with a reset feedback path is the blind zone which occurs near a 2π phase difference between the input signals. In this condition, the PFD may produce an Up output even in the absence of the Fb signal. When the rising edge of the Fb signal finally occurs, the PFD immediately enters the reset stage. If the rising edge of Ref occurs during the reset stage, the PFD loses this rising edge and generates wrong information. Additionally, when both outputs of the PFD remain at logic low,

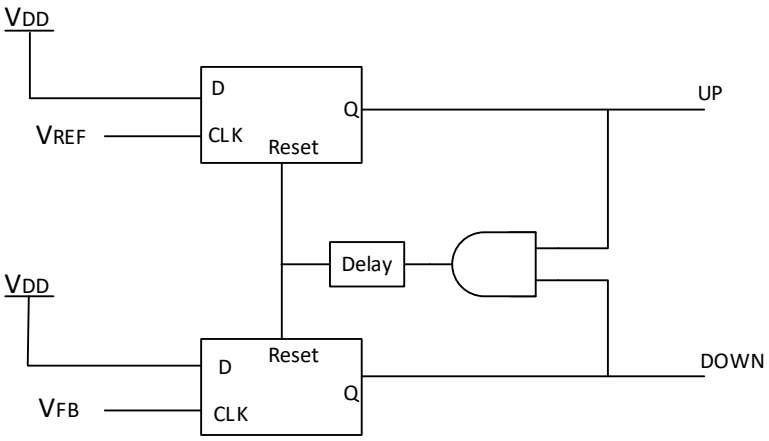

Figure 5.28 : A schematic diagram of a conventional PFD structure with delay cell added.

PFD can even generate a wrong output signal Down during the near 2π phase differences. Hence, the detection range of PFD decreases when the blind zone is present.

Several PFD architectures are used to resolve main PFD problems such as dead zone and blind zone. A PFD may experience a region of near-zero phase difference around phase locking when it is unable to detect this small phase difference and it can cause an increase in phase noise of PLL. The PFD is unable to respond to voltage variations when the phase difference is near zero, a phenomenon known as the dead zone issue. The dead zone is an important specification as it limits operating frequency and introduces jitter to the PLL system. One solution is to introduce a delay at the PFD output to ensure proper reset operation [19]. However, some random glitches occur in this structure. Furthermore, the reset pin limits the maximum operating frequency as depicted in (5.29). Another solution can be to provide delay in both input signals [20]. Although the dead zone is eliminated since it is no longer dependent on the reset signal, power consumption increases significantly.

The second common issue in PFDs is the blind zone, which occurs near a 2π phase differences when the rising edge of V_{Ref} appears moderately after V_{In} while the reset feedback path is activated. Then, PFD misses this rising edge phase differences and produces a wrong output. The blind zone reduces the PLL acquisition speed, enhances the linearity of PFD, increases energy consumption and degrades phase noise. To solve this issue, the reset path is removed, as designed in [21]. Although this architecture obliterates the blind zone, it leads to an increase in both the dead zone and power consumption.

5.3.1 High-level overview of the design of PFD

The PFD for this thesis is designed in reference to the architecture presented in [14] to eliminate the known issues in the conventional PFD structure. The design of PFD, shown in Figure 5.29, effectively reduces both the dead zone and blind zone while maintaining a satisfactory operating frequency. Additionally, the PFD also eliminates glitches and reduces reference spurs. The PFD architecture integrates INV1 and T_{d1} (INV6 and T_{d2}) to introduce controlled delays to the input signals. The delays enable proper transition timing for nodes T or S. These transitions allow M_6 or M_{13} to conduct, which in turn pulls node X or Y to the logic high state. To prevent both outputs from

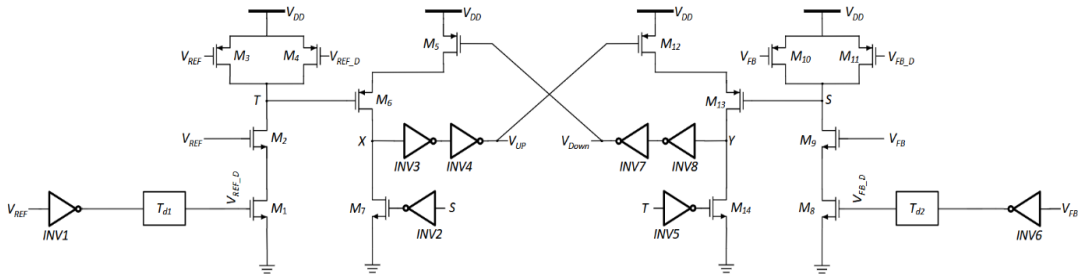

Figure 5.29 : The design of PFD architecture.

being high simultaneously, M_5 and M_{12} are employed. Additionally, M_7 and M_{14} facilitate the reset mechanism by checking if node T or S is either pulled up or down. The reset mechanism ensures that reliable operation and consistent of PFD output behavior can achieve.

It is crucial to emphasize that the time delays, T_{d1} and T_{d2}, are essential in the design, ensuring that the applied V_{Ref} and V_{Fb} signals are sufficiently delayed to drive M_6 and M_{13} respectively. Additionally, the duration of these delays must be shorter than the reset pulse width to trigger switching pulse width spikes at the nodes in PFD.

The operation of the PFD is discussed in both frequency-aligned and non-aligned frequency scenarios under the following conditions: (1) V_{Ref} leads V_{Fb} in phase (2) V_{Ref} lags V_{Fb} in phase and (3) V_{Ref} is in-phase with V_{Fb}. The working principle of the design of the PFD for each case is analyzed in the following sections.

5.3.2 V_{Ref} leads V_{Fb} in phase when frequency-aligned

The operation of the PFD when V_{Ref} leads V_{Fb} in phase under frequency-aligned condition is illustrated through the simulation result presented in Figure 5.30. The T node is in the logic high state as the switch M_3 pulls this node to V_{DD} when both inputs are logic low. If a rising edge of V_{Ref} occurs at t = 0.1 us while V_{Fb} remains in logic zero, the node T is pulled down to ground by M_1 and M_2 thus the node X reaches the high logic state as M_6 turns on. After the time delays in T_{d1} and INV1, V_{Ref_D} goes to the logic low state hence, it turns off M_1. This forces the T node to reach V_{DD} again. M_6 also turns off at this moment due to the node T. As a result, the node X holds the logic high state. INV3 and INV4 are implemented to ensure that the output voltage levels are properly restored to meet standard logic level requirements.

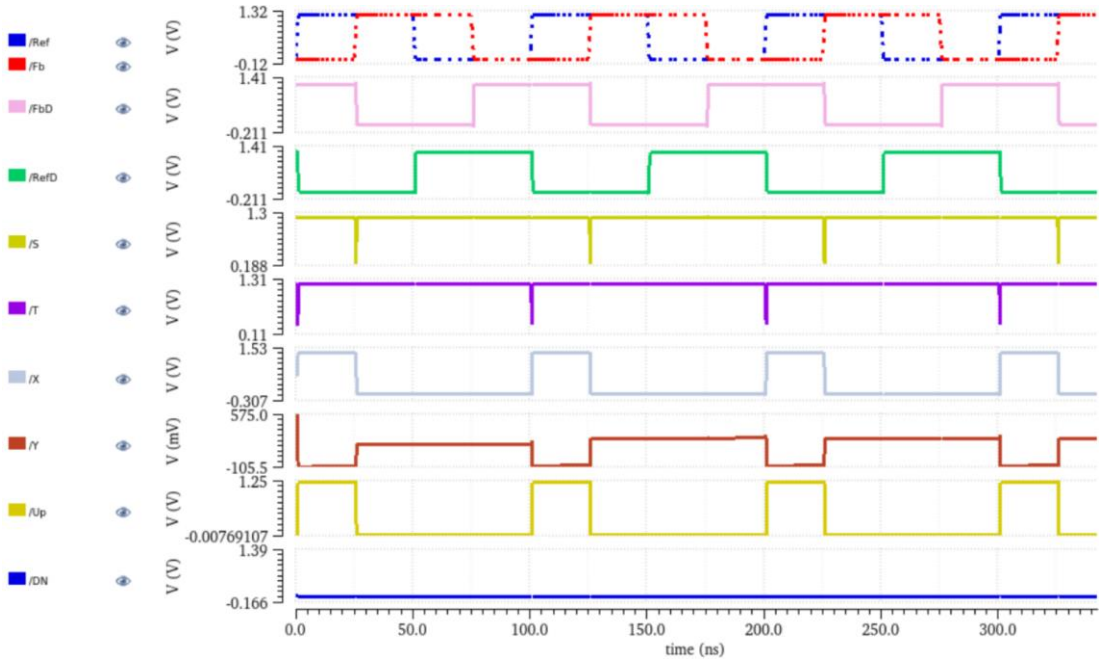

Figure 5.30 : Transient response of key nodes in the design of PFD under V_{Ref} leading V_{Fb} in phase at the same frequency.

When V_{Fb} goes to the logic high state at t = 0.125 us, the node S is triggered to be pulled down by M_8 and M_9. During this transition, M_{13} turns on; however, it cannot pull the node Y to reach to logic high because M_{12} remains off at this stage.

Since the Up signal is applied to the gate of M_{12}, it prevents M_{12} from turning on, hence the node Y stays at logic low. After the time delays in T_{d2} and INV6 occurs, V_{Fb_D} goes to logic low. Therefore, M_8 turns off and forces the S node to reach V_{DD} again. At this moment, the PFD is reset by the inverted output of S node, which is applied to the gate of M_7.

5.3.3 V_{Ref} lags V_{Fb} in phase when frequency-aligned

The PFD generates digital outputs when V_{Ref} lags V_{Fb} in phase under frequency alignment. The same operational principle is implemented in the circuit. In particular, Figure 5.31 presents transient simulation of the key nodes in the design of PFD. The S node is pulled down to ground by M_8 and M_9 when the rising edge of V_{Fb} occurs while V_{Ref} remains in logic zero. Thus, node Y reaches the high logic state as M_{13} turns on during the transition of node S. After the time delays in T_{d2} and INV6, V_{Fb_D} goes logic low due to which the rising edge of the reference signal occurs. Therefore, M_8 turns off and forces the S node to reach V_{DD} again. M_{13} turns off, and the node Y holds the

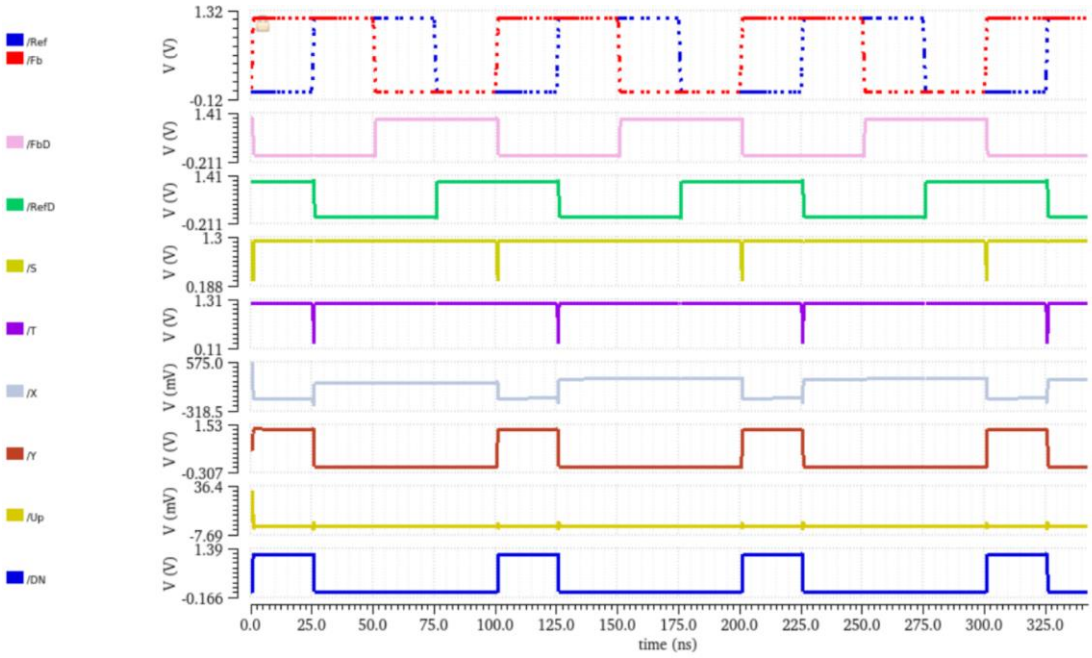

Figure 5.31 : Transient response of key nodes in the design of the PFD under V_{Ref} lagging V_{Fb} in phase at the same frequency.

logic high. Two inverters, INV7 and INV8, are applied at the output node Y in order to ensure that the voltage level is V_{DD}. Hence, Down is generated when t = 0.1 us.

If the rising edge of V_{Ref} occurs at the time t = 0.125 us, node T is triggered to be pulled down by M_1 and M_2. During this time, the node X cannot change the state to logic high and remains in logic low because M_5 is off as Down was applied to its gate. After the time delays occurs in T_{d1} and INV1, V_{Ref_D} goes to logic low allowing M_1 to turn off which forces the T node to reach V_{DD} again. At this moment, the PFD is reset by the inverted output of T node, which is applied to the gate of M_{14}. As a result, the node Y changes its state to logic as it is pulled down by M_{14}.

5.3.4 V_{Ref} in-phase with V_{Fb} when frequency-aligned

Finally, the PFD circuit is able to operate under the desired scenario where both input signals have zero phase difference when frequency is aligned. In this locked state, the PFD does not generate any output pulses, indicating that the loop is locked in both phase and frequency.

The transient analysis of the key circuit nodes is presented in Figure 5.32. When the rising edge of both input signals occurs simultaneously, nodes T and S pulled low by the M_1-M_2 and M_8-M_9 transistor pairs, respectively. During this transition, the inverted

outputs of nodes T and S are applied to M_7 and M_{14} respectively to turn them on in a purpose for pulling nodes X and Y to ground. Although M_6 and M_{13} are also triggered into conduction region, they are unable to pull nodes X and Y to high logic state due to M_7 and M_{14}, resulting in logic-low output at both X and Y nodes. This information is further translated into clear logic state signals by the inverter pairs INV3-INV4 and INV7-INV8.

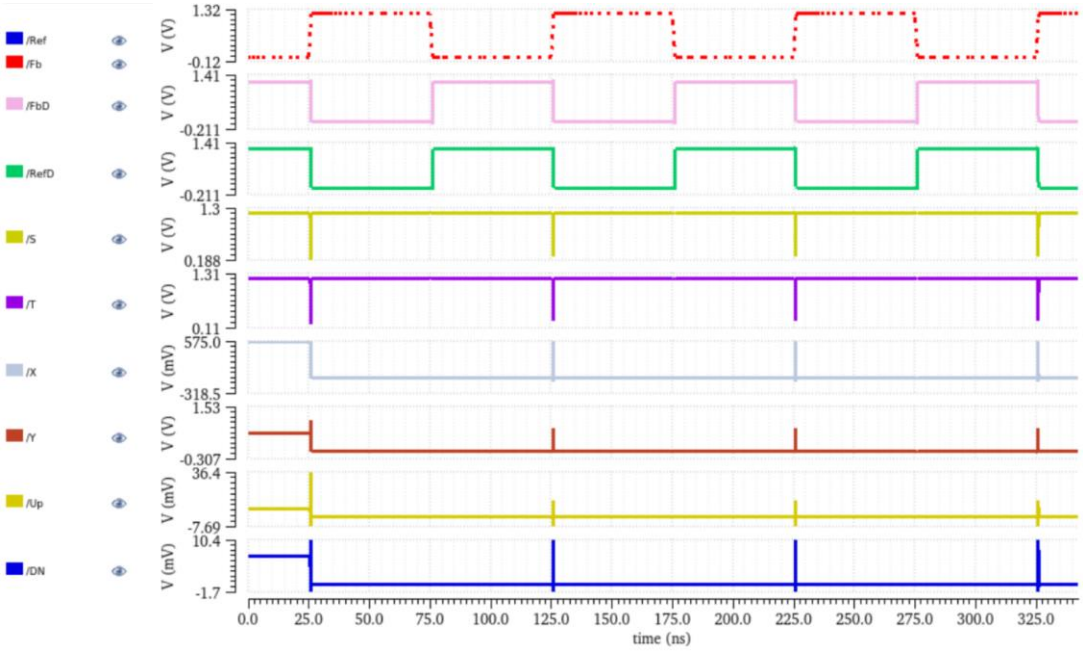

Figure 5.32 : Transient response of key nodes in the design of the PFD under V_{Ref} in-phase with V_{Fb} at the same frequency.

5.3.5 Circuit implementation and simulation results of the design of the PFD

The frequency in the input of the PFD, V_{Ref} is considered to be 10 MHz as discussed in Chapter 2. In addition to, the frequency of V_{Fb} signal can differ between 9 MHz to 11 MHz depending on the choice of divider used in the PLL structure. The underlying cause of this difference belongs to 5G NR 78 standard as VCO generates its output signal within a frequency range between 3.3 GHz to 3.8 GHz. Thus, the circuit is also tested for this frequency range. The latency applied by T_{D1} and T_{D2} introduces delays of 14.2 ps to each input signals, V_{Ref} and V_{Fb}. The Aspect ratios are adjusted to force this architecture to be compatible for 10 MHz input signals and are provided in Table 5.1. The fundamental idea here is focused on transition time of NMOS devices to voltage changes. Taking as an example, when V_{Ref} is leading V_{Fb} and its rising edge occurs, M_1 and M_2 needs to react to this change in order to pull node T to ground. M_1

and M_2 need slow transition time to its input signal therefore smaller aspect ratios are used. Figure 5.33 illustrates the dead zone analysis of the design of the PFD, where V_{Ref} leads V_{Fb} by 25 ps when the equal 10 MHz frequency signals applied. In this dead zone, the PFD is able to generate correct output signals.

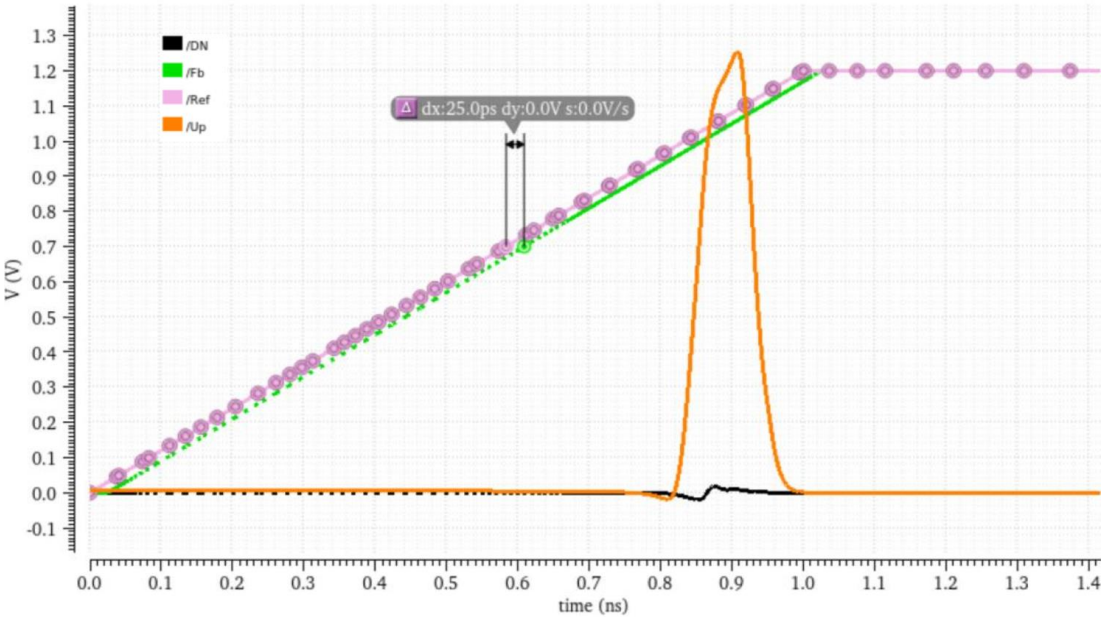

Figure 5.33 : Dead zone analysis of the design of the PFD when V_{Ref} leads V_{FB} by 25 ps.

Table 5.1 : Aspect ratio of transistors used in the design of the PFD.

Device	W/L
M_1, M_2, M_8, M_9, PMOS transistor of: (INV_3, INV_4, INV_7, INV_8)	1.2 µm/65 nm
M_3, M_4, M_{10}, M_{11}	8 µm/65 nm
M_5, M_6, M_{12}, M_{13}	4.8 µm/65 nm
M_7, M_{14}	1.8 µm/65 nm
PMOS transistor of: (INV_1, INV_6, Td_1, Td_2)	2.2 µm/240 nm
NMOS transistor of: (INV_1, INV_6, Td_1, Td_2)	1.5 µm/240 nm
NMOS transistor of: (INV_2, INV_5)	8 µm/130 nm
NMOS transistor of: (INV_3, INV_4, INV_7, INV_8)	12 µm/130 nm

The blind zone analysis of the design of the PFD is performed. For better view of blind zone analysis, V_{Ref} leads V_{Fb} by 1 ns and it is shown in Figure 5.34. The simulations resulted that the blind zone of the PFD is 39.46 ps.

The maximum operating frequency of design of the PFD is limited by (5.29). To determine the frequency, we must consider the maximum delays during the charging and discharging durations of node X. The charging duration of node X is the sum of the maximum delays in INV1, T_{d1}, INV3, INV4 and the required time to charge X node through M_5 and M6. Similarly, the discharging duration of node X is the sum of

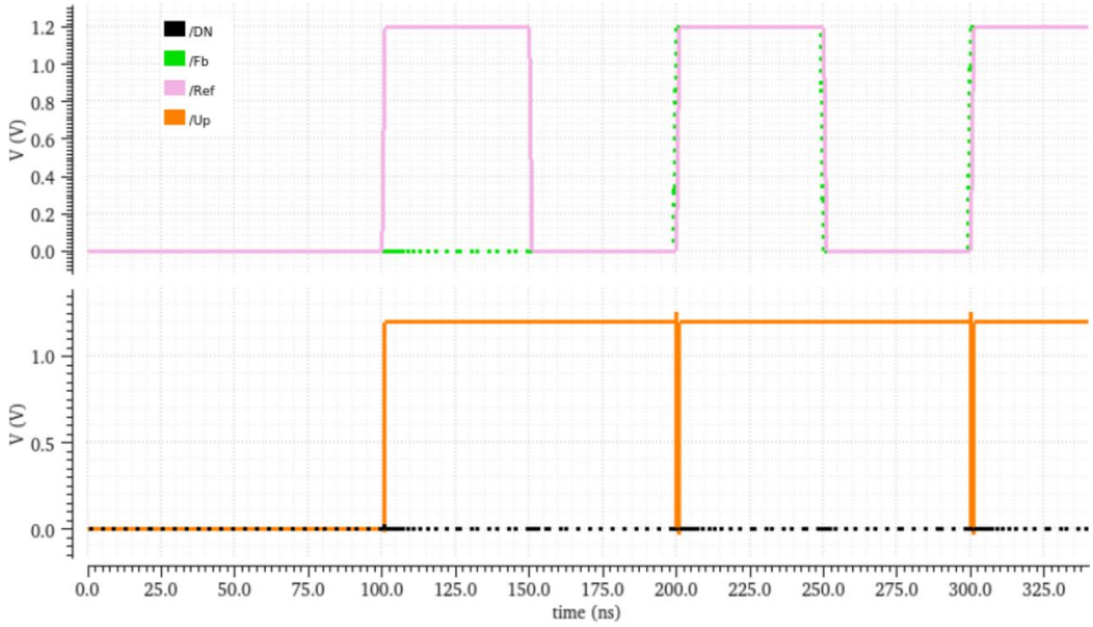

Figure 5.34 : Blind zone analysis of the design of the PFD when V_{Ref} leads V_{FB} by 1 ns.

the maximum delays in INV2, INV3, INV4, and the required time to discharge X node through M_7. The same analysis applies to the calculation of node Y. Although calculating the duration of reset time is an option, it can be derived by the following:

$$f_{max} = \frac{1}{4 \times \max\{T_{dead\ zone},\ T_{blind\ zone}\}} \tag{5.30}$$

where $T_{dead\ zone}$, $T_{blind\ zone}$ are dead zone and blind zone durations, respectively. The maximum operating frequency is calculated as 6.34 GHz and applied to V_{Ref} and V_{Fb} signals, considering the phase delay that arises in the blind zone. Figure 5.35 shows when the rising edge of V_{Ref} occurs, Up transitions to logic high while Down maintains logic low state. The reset of Up occurs on the rising edge of V_{Fb}.

Lastly, power consumption is an important specification in the design and is closely managed. Power hungry devices in this architecture are M_5, M_6 and M_7 (M_{12}, M_{13} and M_{14}). When the node T (S) is grounded, M_7 (M_{14}) conducts current and creates logic high at node X (Y). If the width of M_7 (M_{14}) is reduced, using the width and drain current relationship in (5.31), the drive current also decreases. In (5.30); I_D, μn, C_{ox}, W, L, V_{GS} and V_{th} are the drain current of the NMOS transistor, electron mobility, oxide capacitance per unit area, width of the NMOS transistor channel, length of the NMOS transistor channel, gate-source voltage, and threshold voltage of the NMOS transistor, respectively.

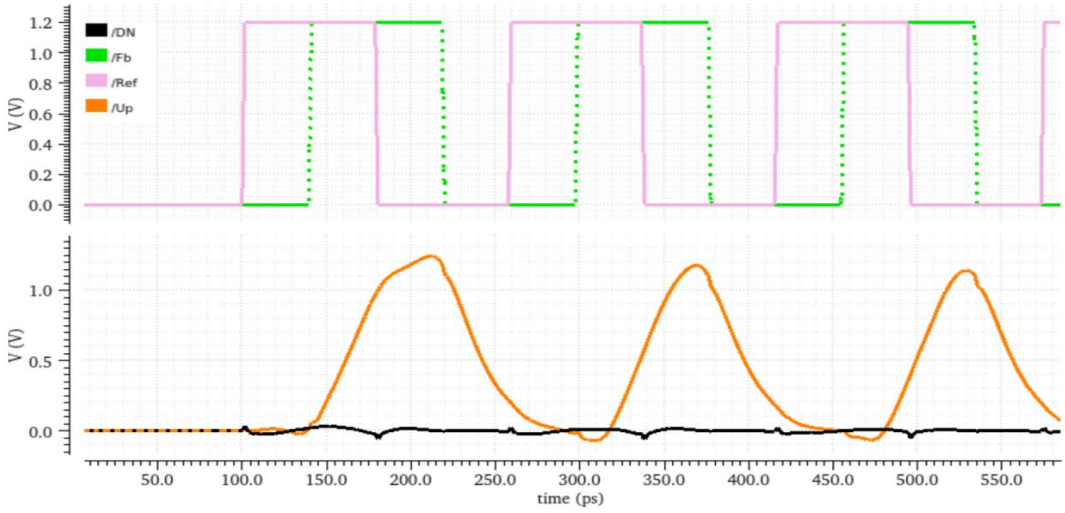

Figure 5.35 : Performance of the design of the PFD at 6.34 GHz when V_{Ref} leads V_{FB} by 39.46 ps.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \tag{5.31}$$

The power consumption reduction is managed while ensuring that the correct switching of Up (Down) occurs. Additionally, the aspect ratios of the inverters are lowered to reduce power consumption while ensuring that sufficient invertor gain and bandwidth are maintained within the topology. As a result, the design PFD consumes 50.88 µW, which benefits to the power budget of PLL.

In conclusion, the design of the PFD is compatible with 5G NR 78 mobile applications and operates with a reference signal at 10 MHz. The design of the PFD consumes 50.88 µW, achieves 25 ps dead zone and 39.46 ps blind zone durations under $\pm 2\pi$ detection range. The simulation results validate the benefits of the design, demonstrating improvements in power consumption and the efficiency of dead zone and blind zone.

5.4 Frequency Dividers

Following the design and analysis of the VCO, charge pump, loop filter, and PFD, the final critical block in a PLL is a frequency divider which are able to scale down the frequency output of the VCO to a lower frequency compatible with the reference clock. This enables the PLL to compare frequencies accurately and maintain a stable lock condition. A frequency divider typically operates in the digital domain and can be

implemented using flip-flops, counters, or logic gates depending on the desired division ratio and power versus speed trade-offs [10]. This section provides an overview of the frequency divider architecture design and discusses its role and performance considerations within the overall PLL design.

Frequency divider is implemented using two different strategies: the master-slave (MS) latch divider and the injection-locked frequency divider (ILFD). MS divider consists of two differential latch stages configured to achieve divide-by-2 frequency division. On the other hand, the ILFD exploits the concept of injection pulling, where the divider is tuned to lock onto half the output frequency of the VCO, enabling efficient frequency division at high speeds.

MS divider generally exhibits lower power consumption compared to ILFD. However, the initial frequency division stage at the VCO output, particularly for milimeter waves, is more effectively implemented using the ILFD topology [11] due to its superior speed performance and ability to operate reliably at higher input frequencies.

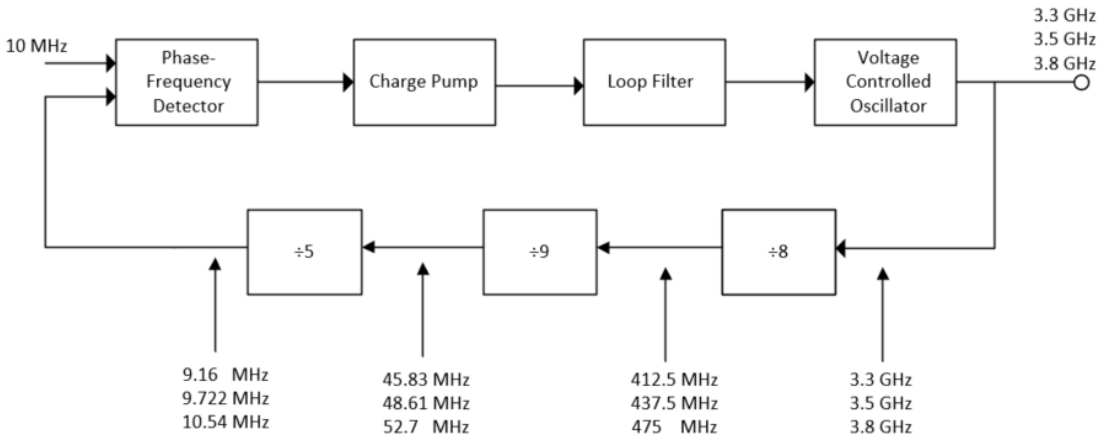

Figure 5.36 : 3.5 GHz PLLfrequency synthesizer illustrating the design of the frequency divider architecture

In sub-6 GHz applications, the VCO output frequency is relatively moderate for a direct MS divider approach without the need for an ILFD. This strategy contributes to reducing the power consumption of the divider chain as ILFDs exhibit higher power demands due to their analog complexity. Moreover, the required loop bandwidth can be maintained using MS divider since ILFD topologies suffers from a narrower bandwidth. As a result, the MS-based architecture offers a more efficient solution for frequency division in sub-6 GHz systems.

For the n78 band PLL system utilizing a 10 MHz reference signal, the frequency divider architecture is designed using a combination of 5-8-9 division ratios. To better illustrate the division process, Figure 5.36 presents a high-level view of the divider block within the PLL system. The output signal from the VCO is first fed into a divide-by-8 block to reduce the frequency from the GHz range to the MHz domain. This is followed by a divide-by-9 stage, which further decreases the frequency. Finally, a divide-by-5 block is employed to scale the signal's frequency down further to match the reference frequency of 10 MHz. This composite frequency division structure enables fast division with minimal delay, ensuring the loop maintains synchronization while optimizing for power and performance.

5.4.1 Circuit implementation of the divide-by-2 block

As previously mentioned, utilizing MS divider in the division chain is the focus of implementation of the divider chain. MS divider can be realized using D-type flip-flops (D-FFs), as presented in [10]. A typical D-FF structure consists of two sequentially connected D flip-flops with complementary clock signals that aim to synchronize each other. The design is generally constructed by a positive feedback memory structure that allows a data storage within the flip-flops and transition at each clock cycle. This architecture generates a robust divide-by-2 functionality with relatively low power consumption [10] and sufficient speed for integration into the PLL system [22].

The circuit implementation of the true single-phase clock (TSPC) architecture is illustrated in Figure 5.37. The topology follows the architecture proposed in [22], optimized for high-speed and low-power operation. The TSPC architecture offers significant advantages by operating with only a single global clock signal. This approach simplifies the clock distribution network and eliminates the necessity for complementary clock phases typically required in conventional D-FF implementations. The reduction in clock complexity not only decreases overall power consumption and silicon area but also enhances operational speed. This improvement is achieved through reduced clock loading and minimized clock skew, making TSPC a highly efficient and scalable solution for high-performance and low-power digital circuit applications.

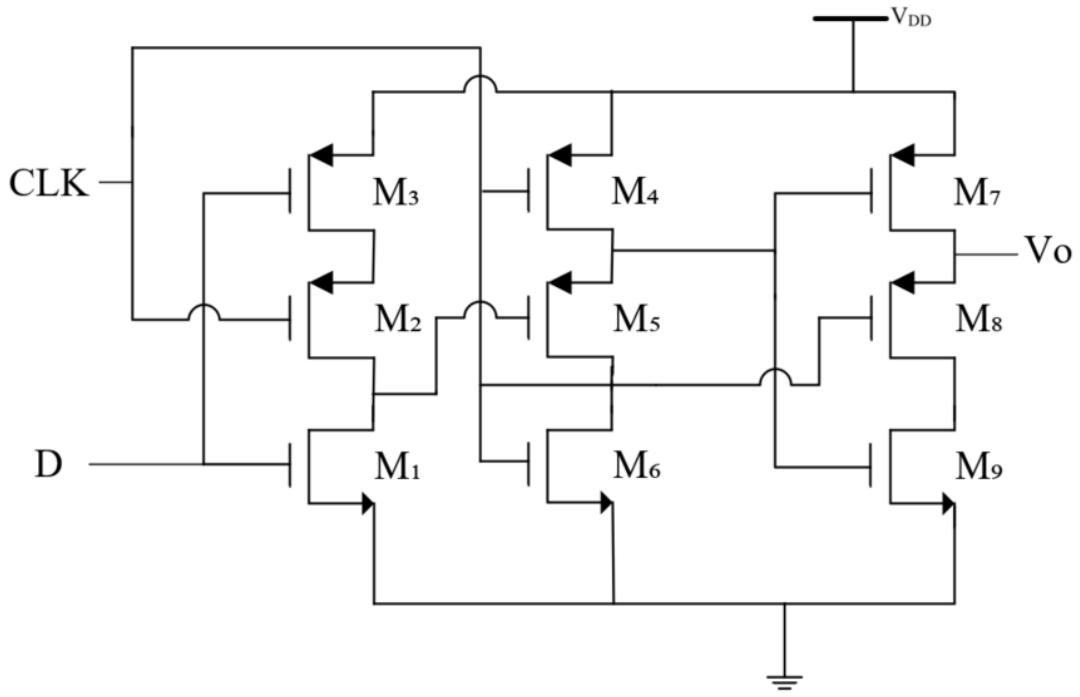

Figure 5.37 : TSPC circuit implementation.

A key feature of this design is its fast reset mechanism, which is realized using an NMOS transistor connected to a pre-charged small capacitive node. This configuration allows the NMOS device to quickly discharge the node to ground, thus the resetting the TSPC is accomplished efficiently.

The high-frequency output signal from the VCO is applied as the clock input. During each clock cycle, TSPC samples and store the applied data and transfers to the output just before the reset phase begins. Additionally, the output of the TSPC is fed back to the data input to create a divide-by-2 operation which accomplishes the master-slave divider functionality. This configuration ensures robust frequency division at high operating speeds while maintaining low power consumption, making it suitable for use in the PLL frequency synthesizer chain. However, directly connecting the divider to the VCO output can introduce undesired loading effects, which may degrade the oscillation amplitude, frequency stability, and overall performance of the VCO. To mitigate these issues, a buffer stage is introduced in Figure 5.38 between the VCO and the divider. This buffer acts as an isolating interface for VCO to operate in a minimally disturbed environment. It provides the necessary drive strength to feed the divider while maintaining the integrity of the oscillation signal. Morever, the buffer stage utilizing resistors helps in reducing phase noise degradation by minimizing the back-injection of noise from the divider circuits into the sensitive analog core of the VCO.

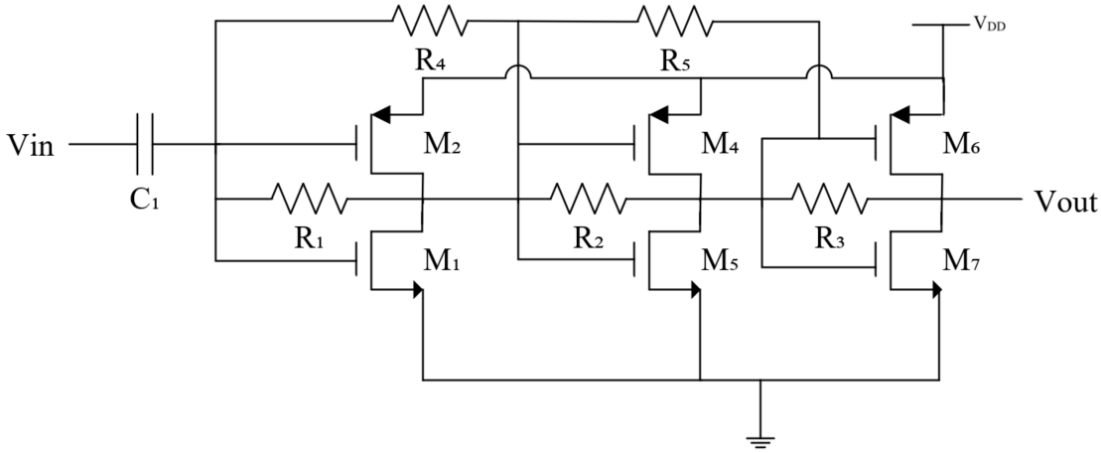

Figure 5.38 : VCO buffer circuit implementation.

This structure also converts the output of VCO to an eligible peak voltage range for the efficient operating of first stage of TSPC. However, the precense of resistors affects the voltage swing from the ideal CMOS inverter levels of 0 V to 1.2 V to approximately 0.2 V to 1 V. This not only affects signal integrity but also introduces additional power consumption within the frequency divider block.

Moreover, incorporating a buffer stage at the output of the TSPC provides advantages as well. The reason is that the output of TSPC operates at a high-frequency level, which can introduce significant capacitive loading effects on subsequent circuit stages. These loading effects may degrade signal integrity, slow down transitions, and potentially compromise the performance of the frequency divider. The buffer effectively isolates the TSPC output from the next stage and preserves the signal strength and transition speed. As illustrated in Figure 5.39, a standard 3-stage CMOS buffer is implemented. This buffer architecture employs progressively increasing transistor sizing in each stage to optimize signal drive strength. By scaling the device ratios, the design effectively reduces dynamic power consumption and mitigates capacitive loading effects [23]. The ratio of scaling factor of is selected to avoid increasing the drive current of CMOS inverters further hence, the structure remains power efficient.

5.4.2 Circuit implementation of the divide-by-8 block

The division by 8 can be realized by cascading three divide-by-2 stages. In this configuration, the output of each divide-by-2 stage serves as the clock input for the subsequent stage, effectively halving the frequency at each step. The simplicity of the

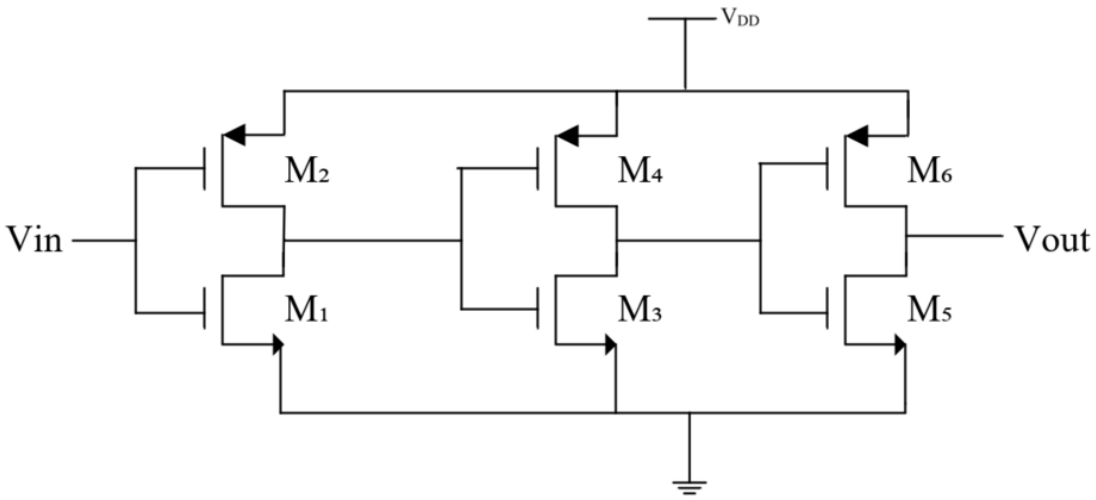

Figure 5.39 : Buffer for divider circuit implementation.

structure also benefits to low power consumption and ease of synchronization. The circuit achieves a stable and accurate divide-by-8 operation as simulation result shown in Figure 5.40.

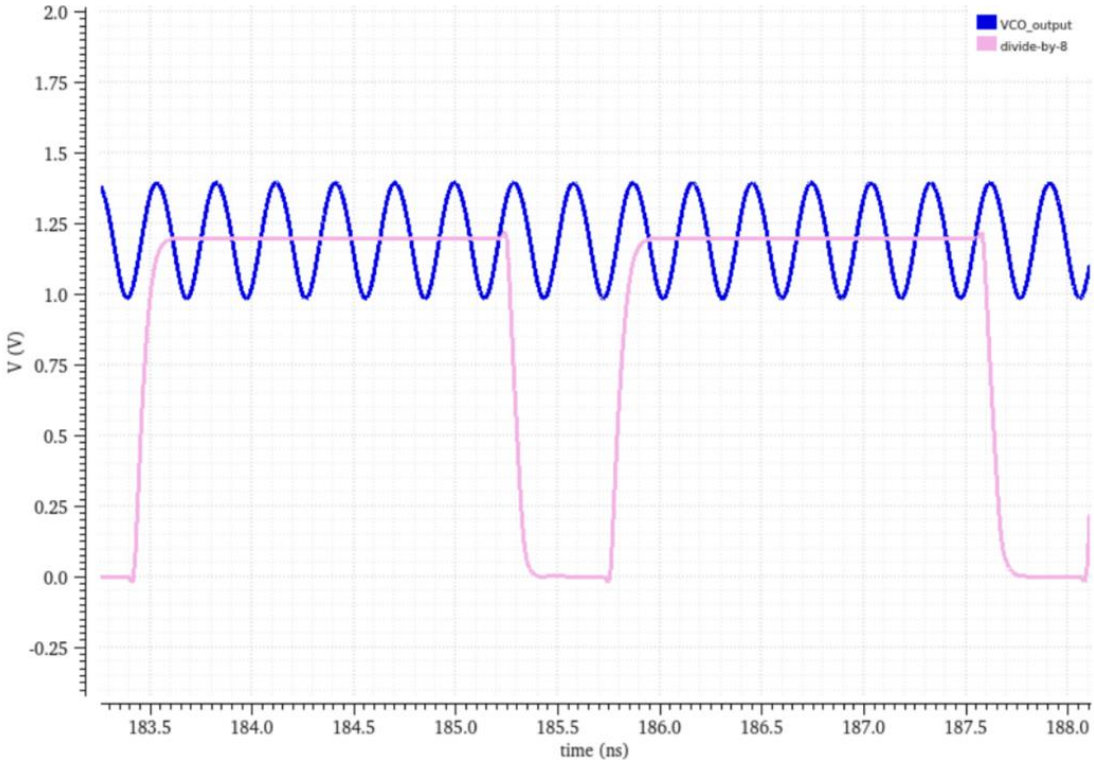

Figure 5.40 : The output waveform of divide-by-8 block.

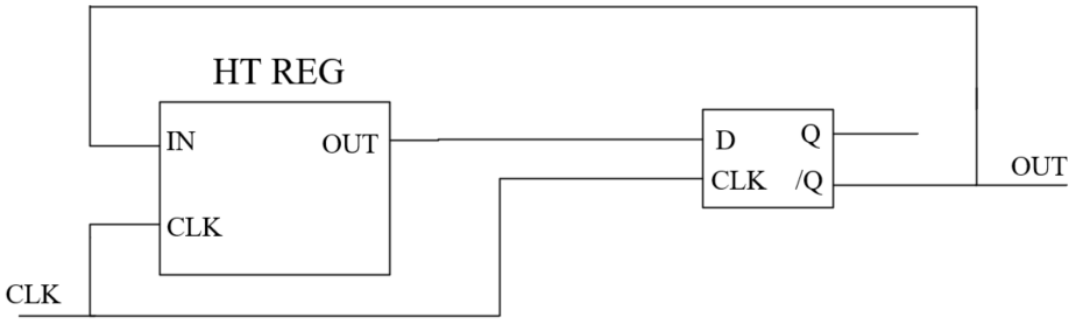

Figure 5.41 : The block diagram representation of divide-by-3.

5.4.3 Circuit implementation of the divide-by-3 block

Divide-by-3 operation cannot be estabhlished utilizing TSPC circuit topology. It is because TSPC topology allows only power of 2 division. We can utilize the suggested approach in [27] which consists of a half-transparent register and a D-latch topology. This approach provides a consept of achieving divide-by-3 as well divide-by-5 therefore, it provides simplicity in the design procedure. The structure is illustrated in Figure 5.41 which is cascading 2 half-transparent registers in front of the D-Latch element to achieve a divide-by-3 frequency divider. The topology differentiates the behavior of the feedback loop depending on the output logic value. The half-transparent register provides different delays to the clock signal in accordance to each logic levels of in its input signal that is the feedback signal of the structure. It provides 1 clock cycle delay when the feedback logic level is 1 and 2 clock cycle delays when the feedback logic level is 2. Therefore, the structure accomplishes divide-by-3 concept. In other words, we can emphasize that we require at least $n-2$ half-transparent registers to accomplish a division of n.

The circuit implementation of the half-transparent register is illustrated in Figure 5.42. The corresponding D-latch block, used within the D-FF structure shown in Figure 5.43, supports this register design. Unlike the implementation presented in Figure 5.37, the design of divide-by-3 block does not require a reset signal for correct operation within the frequency divider. This makes it particularly suitable for divide-by-2 architectures, where a continuous and periodic division is sufficient. In contrast, the use of a reset signal becomes essential in more complex division schemes such as divide-by-3 and divide-by-5, where specific timing control and initialization are necessary to maintain correct sequencing and synchronization. The circuit implementation of the complete divide-by-3 block is illustrated in Figure 5.44

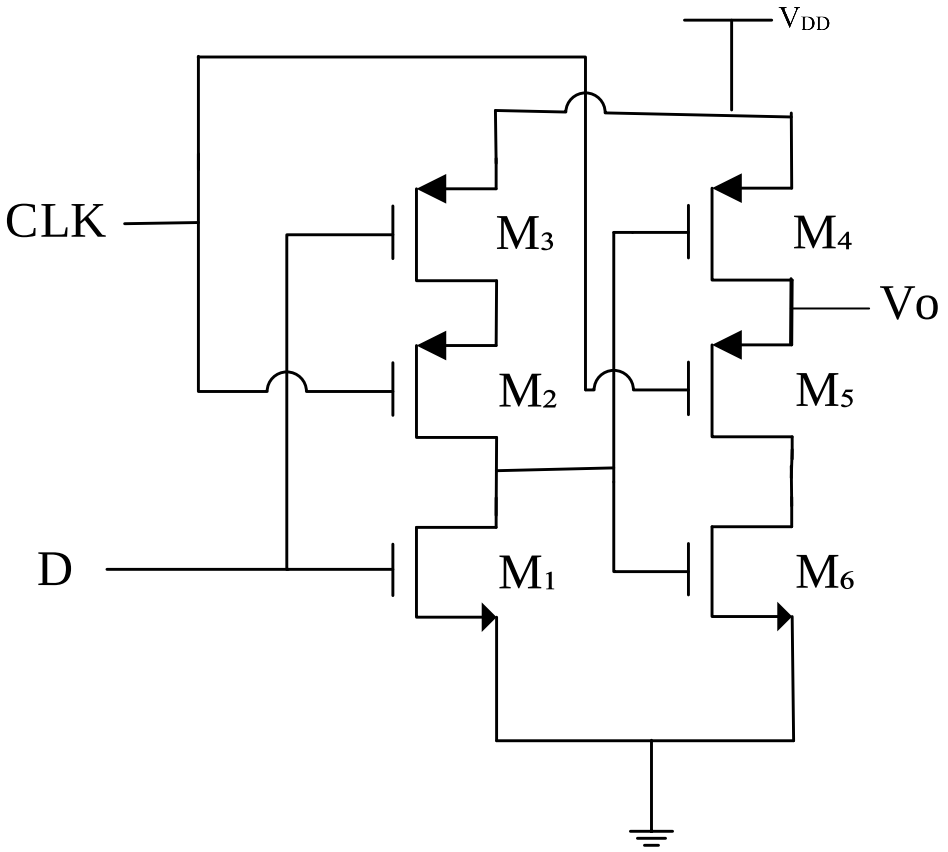

Figure 5.42 : Half-transparent register circuit implementation.

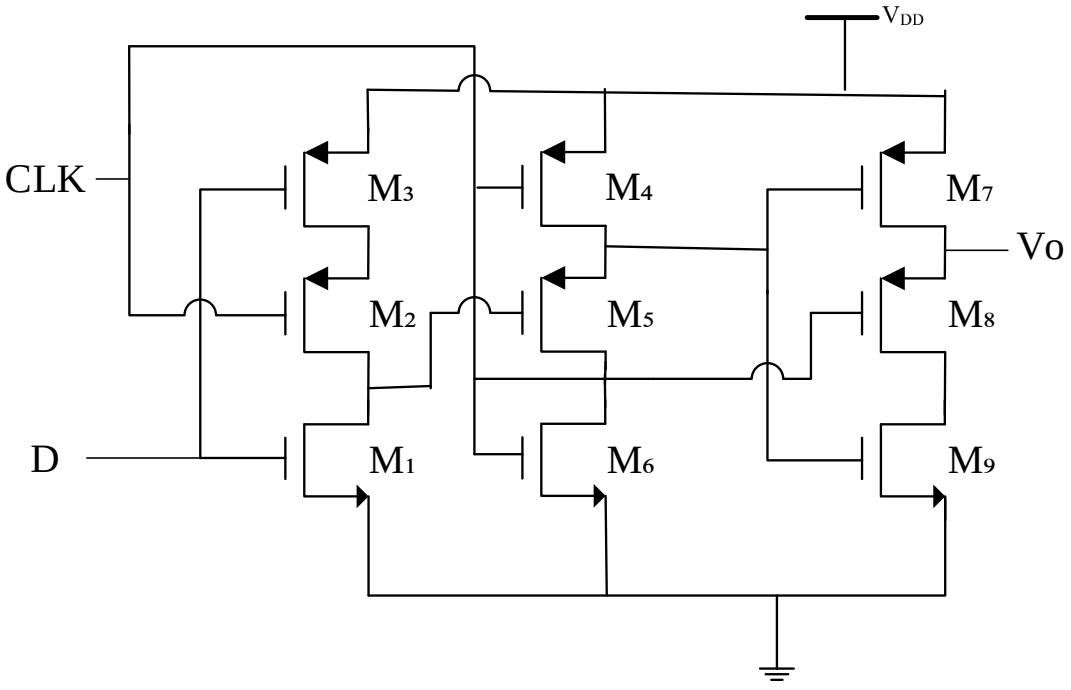

Figure 5.43 : Circuit implementation of D-FF utilized in divide-by-3 and divide-by-5 frequency divider stages.

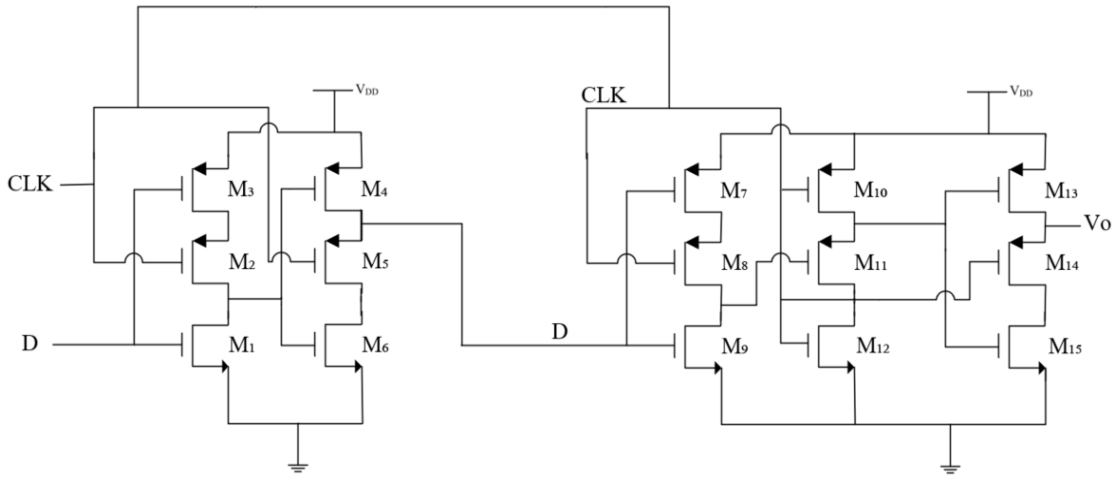

Figure 5.44 : The circuit implementation of divide-by-3.

5.4.4 Circuit implementation of the divide-by-9 block

The division by 9 can be realized by cascading two divide-by-3 stages as shown in Figure 5.45. In this configuration, the output of each divide-by-3 stage serves as the clock input for the subsequent stage which divides the frequency into 3 at each step. The simplicity of the structure also benefits in the design procedure as well. The circuit achieves a stable and accurate divide-by-9 operation as simulation result shown in Figure 5.46.

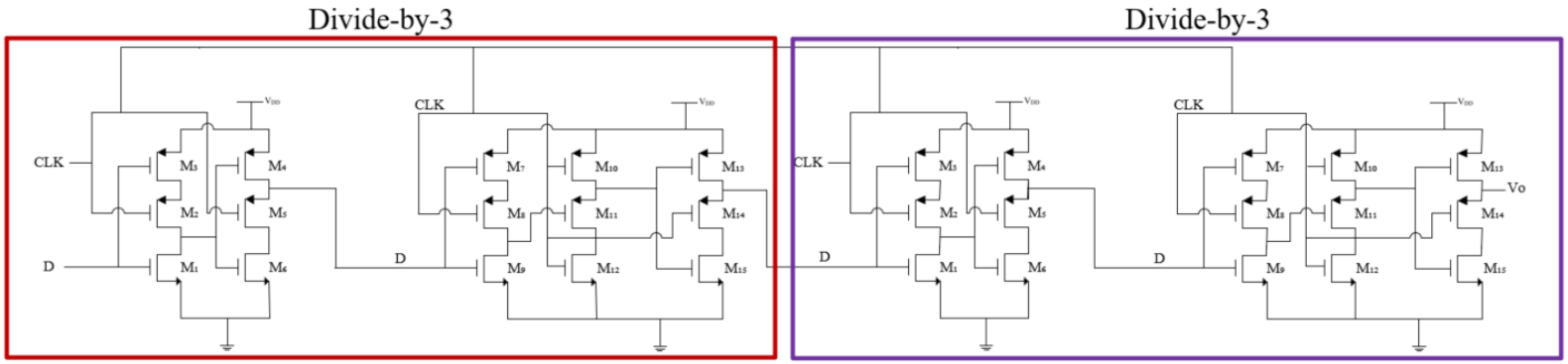

Figure 5.45 : The circuit implementation of divide-by-9.

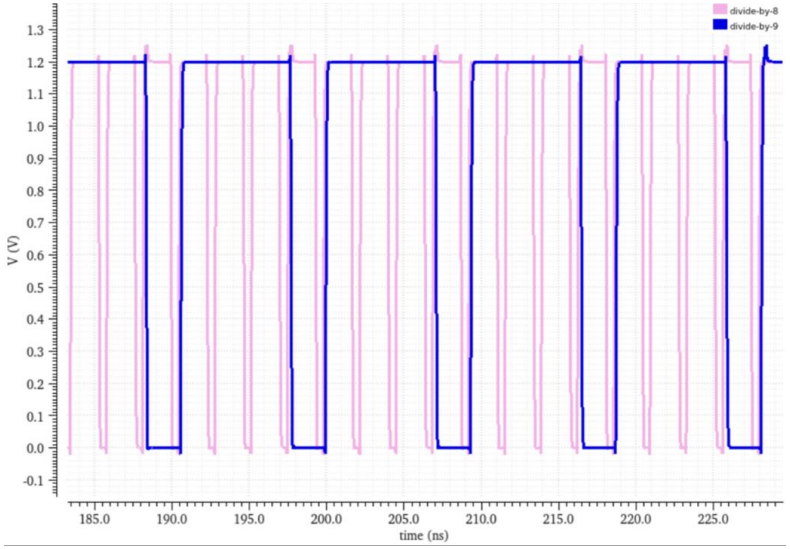

Figure 5.46 : The output waveform of divide-by-9.

5.4.5 Circuit implementation of the divide-by-5 block

The final stage in the frequency divider chain is the divide-by-5 block. As discussed in Section 5.4.3, the same fundamental circuit concept is employed. This block consists of three cascaded half-transparent registers along with an additional D-latch. Each register introduces a delay, which collectively enables the correct timing to achieve the divide-by-5 operation. The waveform of the input of the divide-by-5 block which is divide-by-9 and the output of the divide-by-5 block are shown in Figure 5.47. The circuit implementation of the divide-by-5 is illustrated in Figure 5.48. The output frequency is reduced to 10 MHz. The result aligns with the expected output frequency based on the VCO frequency input illustrated in Figure 5.36.

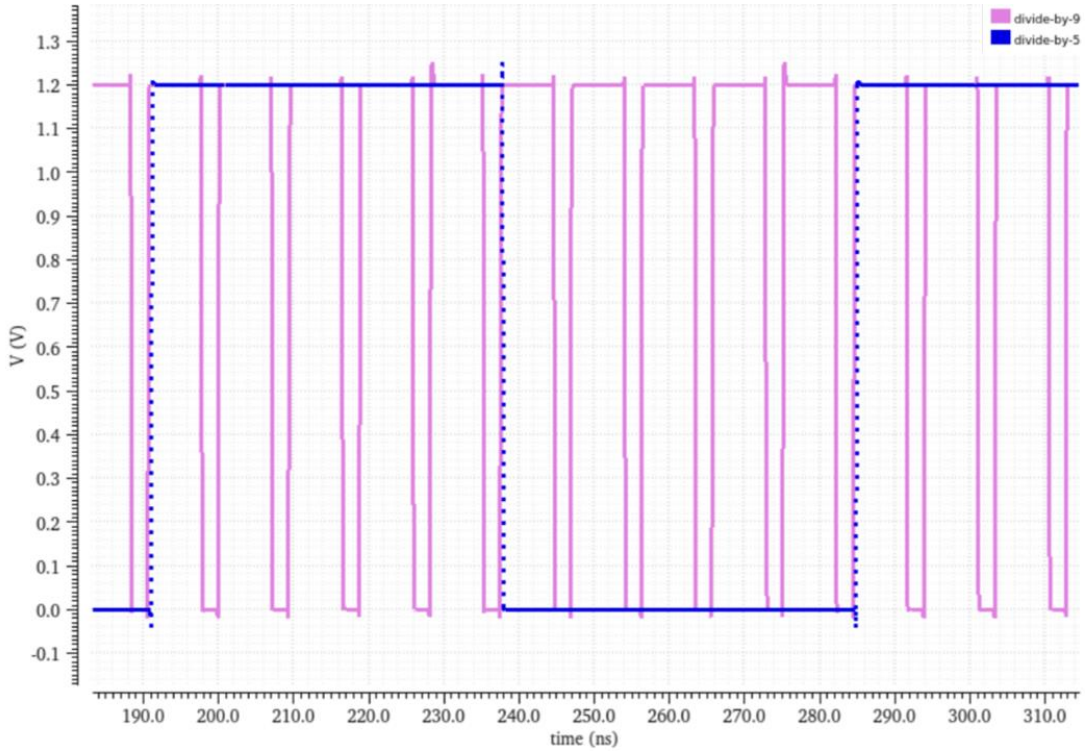

Figure 5.47 : The output waveform of divide-by-5.

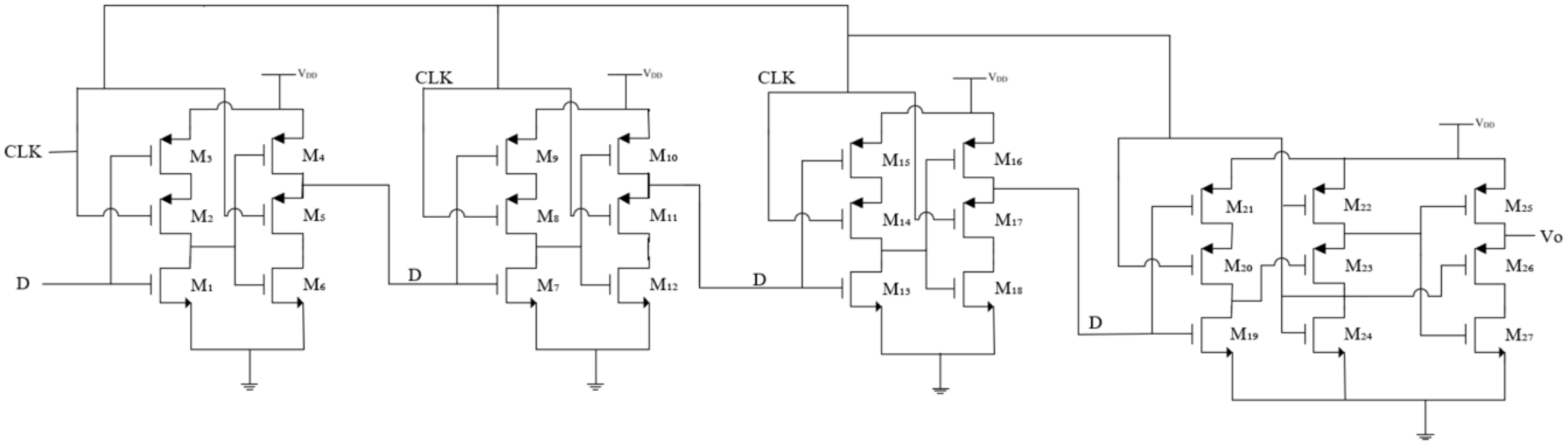

Figure 5.48 : The circuit implementation of the divide-by-5.

6. SIMULATION RESULTS OF COMPLETE PLL DESIGN

In this section, the complete design of the PLL structure is presented by integrating all loop blocks developed in Chapter 5. These individual blocks are combined to form a functional PLL system. The integrated structure is subjected to a series of simulations to evaluate its performance across key metrics set by 5G NR 78 standard. The resulting performance characteristics are then discussed and compared with prior research in the literature.

6.1 Introduction

This thesis focuses on the design of a CMOS PLL that is compatible with the 5G NR n78 standard. The design of the PLL architecture is tailored to operate within the n78 frequency band and adheres to the specifications outlined in Chapter 2. The system is designed with an input of 10 MHz reference frequency and implemented using the TSMC 65 nm CMOS technology. All simulations are conducted using the Cadence Virtuoso design environment. The PLL operates at a supply voltage of 1.2 V and is intended to cover an output frequency range from 3.3 GHz to 3.8 GHz. The supported bandwidth is targeted at 500 MHz in accordance with the n78 band requirements. The free-running frequency of the VCO is centered at 3.5 GHz. The target specifications for the design include a output jitter better than 500 fs, a phase noise performance better than –100 dBc/Hz at a 1 MHz offset, and a total power consumption of less than 10 mW as illustrated in Table 2.2.

The block diagram of the design of the PLL and a high-level overview of its circuit implementation are shown in Figure 6.1 and Figure 6.2, respectively. The overall design of the PLL consists of 177 transistors. The design includes a LC VCO that generates oscillation frequencies ranging from 3.3 GHz to 3.8 GHz, based on the schematic architecture discussed in Figure 5.14. A divide-by-360 frequency divider chain is used to scale down the VCO output frequency before feeding it back to the PFD which compares this feedback signal with the reference signal to detect any phase and frequency discrepancies. According to this comparison, the design of the PFD

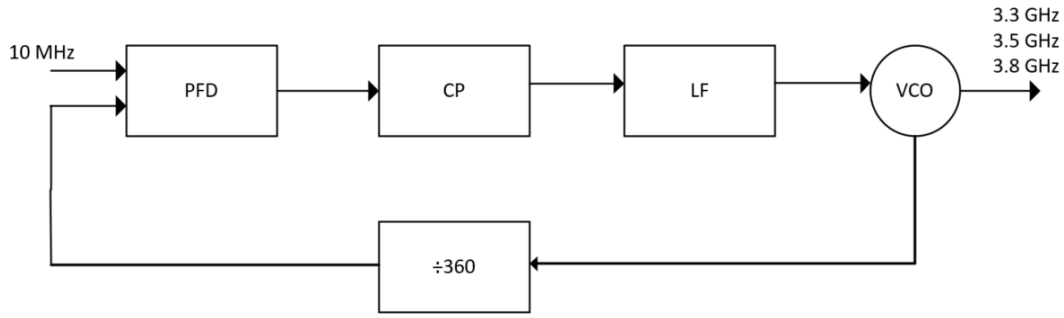

Figure 6.1 : The design of the CMOS PLL frequency synthesizer block diagram.

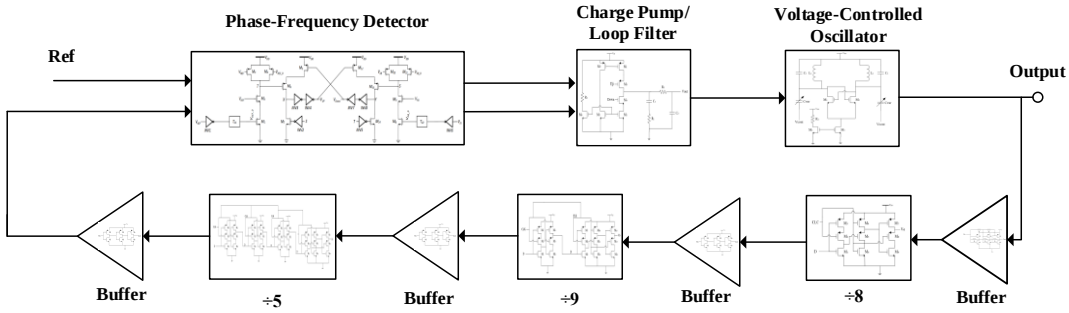

Figure 6.2 : High-level overview of CMOS PLL frequency synthesizer.

structure in Figure 5.29 generates corresponding Up and Down pulses. These pulses are used to charge or discharge the loop filter. The loop filter ensures the overall loop stability, adjusts the loop bandwidth, and produces a control voltage. The structured of the charge pump and loop filter are presented in Figure 5.22. The control voltage is applied to the varactors in the LC VCO schematic, allowing dynamic tuning of the oscillation frequency based on the feedback mechanism.

6.2 Simulation Results

The simulation results presented in this chapter comprehensively evaluate the performance of the proposed PLL architecture designed for 5G NR n78 band applications. The analysis begins with an examination of the key node voltages in transient analysis of Cadence to demonstrate the PLL's ability to lock after the start up. Phase margin is discussed by evaluating the open-loop transfer function of the design of the PLL. This is followed by an evaluation of the settling time to assess the loop’s dynamic response and locking behavior. Subsequently, jitter performance is investigated in the time domain to ensure timing stability. The eye diagram of the design of the PLL system is also analyzed. Phase noise characteristics are then analyzed to verify the spectral purity of the output signal, which is critical for

communication system performance. The total power consumption of the PLL is measured to confirm the design's suitability for low-power mobile applications. Finally, each simulation metric is compared against standard requirements and relevant prior works.

6.2.1 Top-level analysis of the designed PLL

The top-level simulation of the designed PLL in transient analysis is computed in Cadence Virtuoso and shown in Figure 6.3. The reference signal of 10 MHz operates with a 1 pf rise time and fall time. V_{Ref} and V_{Fb} presents the reference signal and the feedback signal, respectively. The output of phase frequency detector generates the Up and Down signal presented in V_{up} and V_{down} in the figure. The output voltage of the charge pump represented with V_{CP} to show up and down reaction of the circuit. Finally, the control voltage V_{cont} provides information on how the loop reacts to the phase and frequency signal. Thus, the capacitance of varactors are adjusted according to this signal.

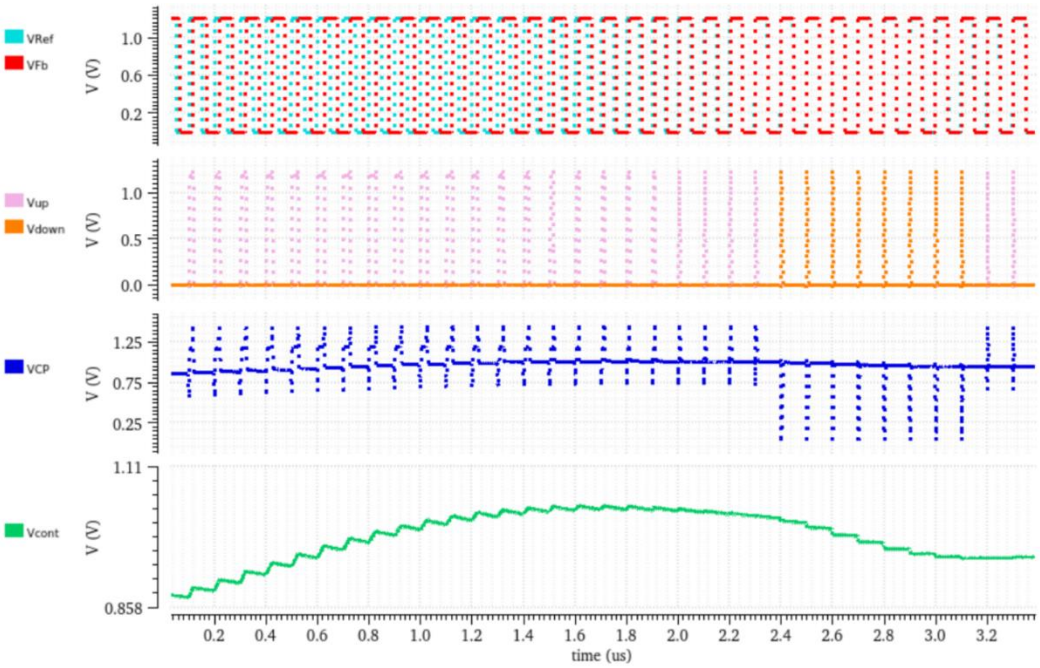

Figure 6.3 : Top-Level PLL simulation.

6.2.2 Phase margin

Phase margin analysis presents how stable the structure is in the presence of feedback. A sufficient phase margin ensures that the system can handle disturbances in the

feedback without oscillating or becoming unstable. This crucial metric is derived from examining the open-loop transfer function of the system. The open-loop transfer function can be calculated using (3.11) which requires K_{PD}, K_{VCO} and the transfer function of the loop filter. K_{PD} is calculated as 2.3170 mA/rad. K_{VCO} is 674.0441 MHz/V as derived from Figure 5.15. The loop filter transfer function in (5.28) is used. Finally, (6.1) presents the open-loop transfer function of the design of the PLL.

$$G(s) = \frac{I_{CP}K_{VCO}}{2\pi N} \frac{s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2) + 1}{s^3(R_1C_1C_2 + R_2C_1C_2) + s^2(C_1 + C_2)}. \tag{6.1}$$

The design of the PLL demonstrates a phase margin of 39.2113°. While typical design guidelines for PLLs often target a phase margin between 45° and 60° to achieve optimal damping and settling times, the phase margin of the design of the PLL still indicates a stable system. The stability can also be observed from the Bode plot of the open-loop transfer function which is generated using Matlab and is illustrated in Figure 6.4. The loop bandwidth is calculated as 228 MHz.

We can also derive the closed loop transfer function of the system in (6.2) and its Bode plot generated in Matlab in Figure 6.5.

$$T(s) = \frac{G(s)}{1 + G(s)}$$

$$= \frac{K_{gain}(s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2) + 1)}{s^3(R_1C_1C_2 + R_2C_1C_2) + s^2(C_1 + C_2 + K_{gain}R_1R_2C_1C_2) + K_{gain}(s(R_1C_1 + R_2C_2) + 1)} \tag{6.2}$$

where K_{gain} is the system's gain which is equal to $\frac{I_{CP}K_{VCO}}{2\pi N}$.

In the closed-loop analysis of the PLL system, there exists two complex conjugates poles and one real pole of the closed-loop transfer function. The damping ratio of the system using (3.29) for the second-order type-II PLL system is approximately 0.418 which suggests that the PLL exhibits an underdamped system. Moreover, the Q-factor of the designed system is equal 1.2. The damping ratio and the Q-factor indicates that the loop performs a fast transient response while maintaining stability. The damping ratio in this range results in a controlled overshoot which is suitable for 5G applications requiring both quick lock times and robust phase tracking. The Q-factor of 1.2 implies a mild resonance near the loop's natural frequency, without excessive gain peaking that could compromise jitter performance which can be seen from Figure 6.5.

We can conclude that Bode plots of open-loop and closed-loop of the design of the PLL exhibit a second-order type II PLL characteristics which Bode plots of open-loop and closed-loop transfer function of such a system was in Figure 3.7 and Figure 3.8, respectively. Despite the system's stability, the obtained phase margin suggests an overshoot in the system's which is discussed in the following section.

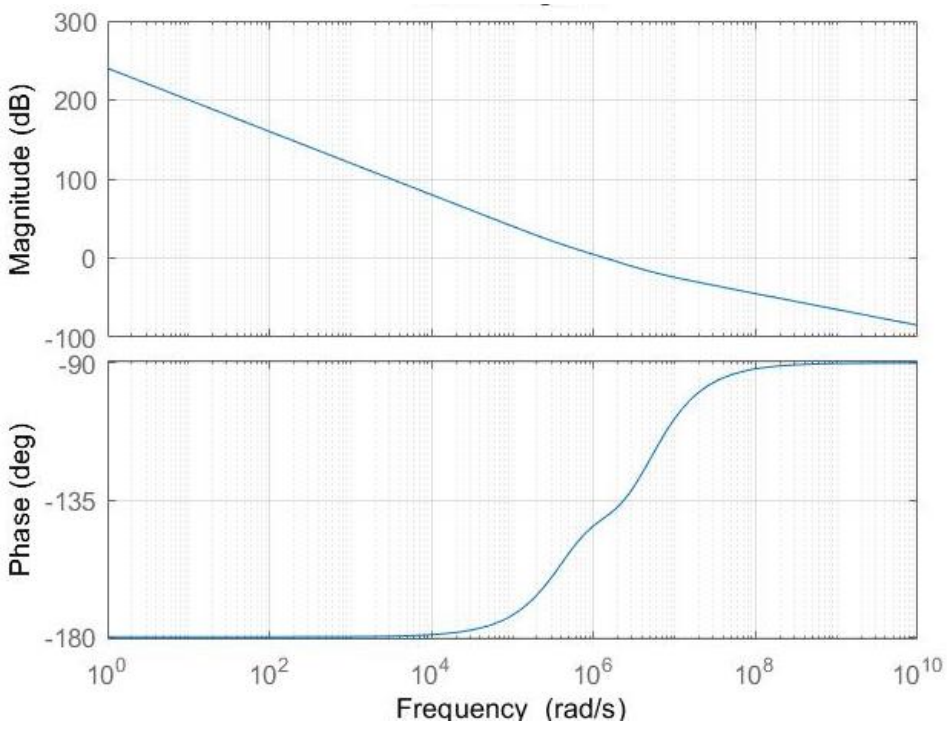

Figure 6.4 : Bode plot of open-loop transfer of the PLL.

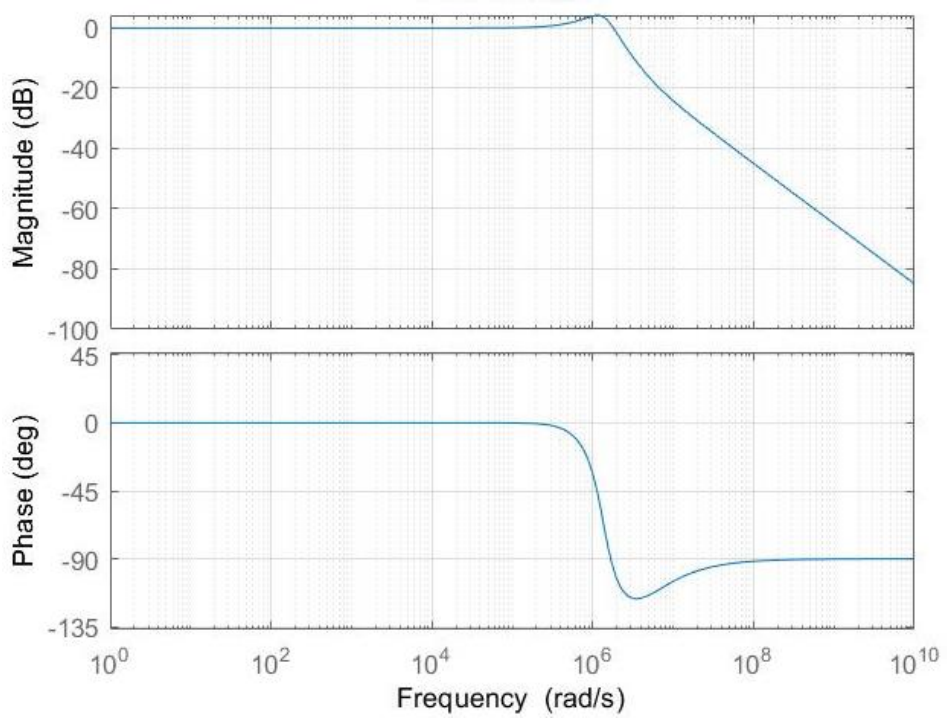

Figure 6.5 : Bode plot of closed-loop transfer of the PLL.

6.2.3 Settling time

To evaluate the dynamic performance of the loop, settling time is an crucial analysis for feedback systems. The settling time indicates how quickly the PLL can lock onto the desired frequency after a disturbance or frequency change. The analysis of settling time setup is set when a step ideal step input with amplitude from -1 V to 1 V with a 10 ps rising time is applied. The simulation results as shown in Figure 6.6, the loop exhibits a 2.44942 ns of settling time. The stability of the loop can also be observed from the figure. As shown in the previous section, Figure 6.6 confirms that the loop is stable. However, the system exhibits an overshoot 1.91455 V. In summary, the PLL demonstrates fast and stable locking behavior.

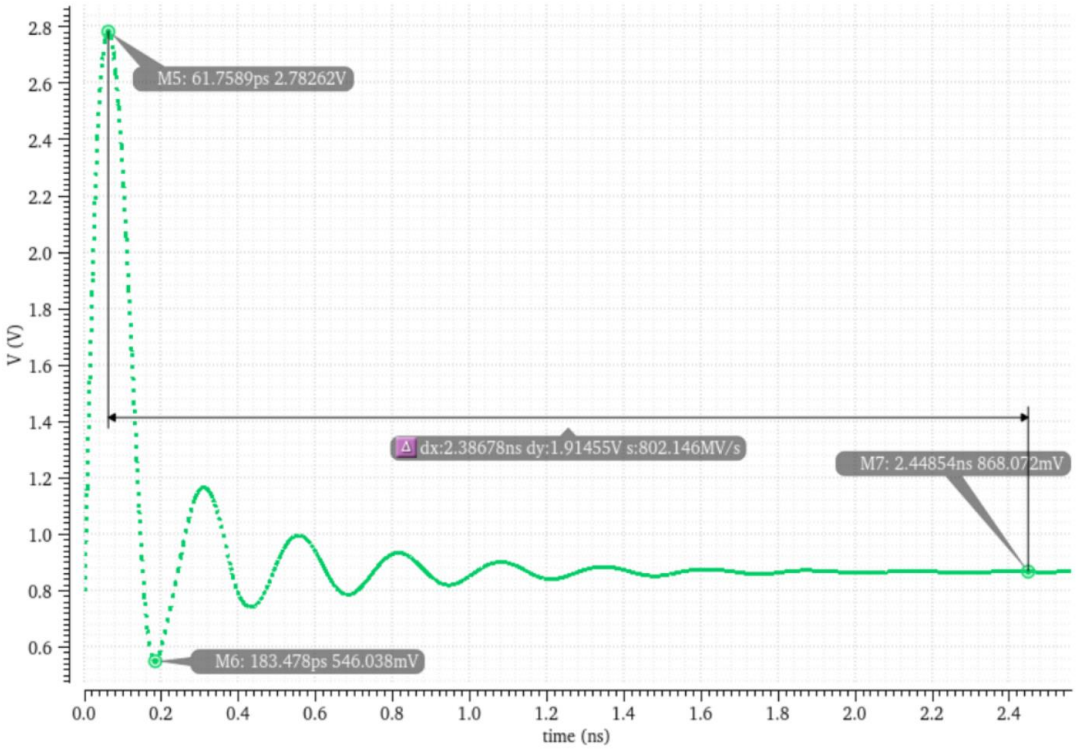

Figure 6.6 : The settling time of the PLL.

6.2.4 Jitter

Jitter is a critical performance metric in PLL systems, particularly for high-speed communication standards like 5G NR. It represents the short-term variations in the output signal's timing, which can degrade system performance and lead to data integrity issues. The simulated output RMS jitter value is computed in Matlab by using each block's noise data in addition to the loop characteristic. RMS jitter of the PLL is 240.904 fs. The result is also confirmed from the Figure 6.7 which represents the eye-

diagram analysis of the PLL. The figure indicates that the PLL output exhibits 53.53961 ps zero crossing time jitter with an eye height of 423.18 mV. The eye width of the eye-diagram is 89.44626 ps which shows that the PLL requires such an amount of time to synthesize the oscillation correctly.

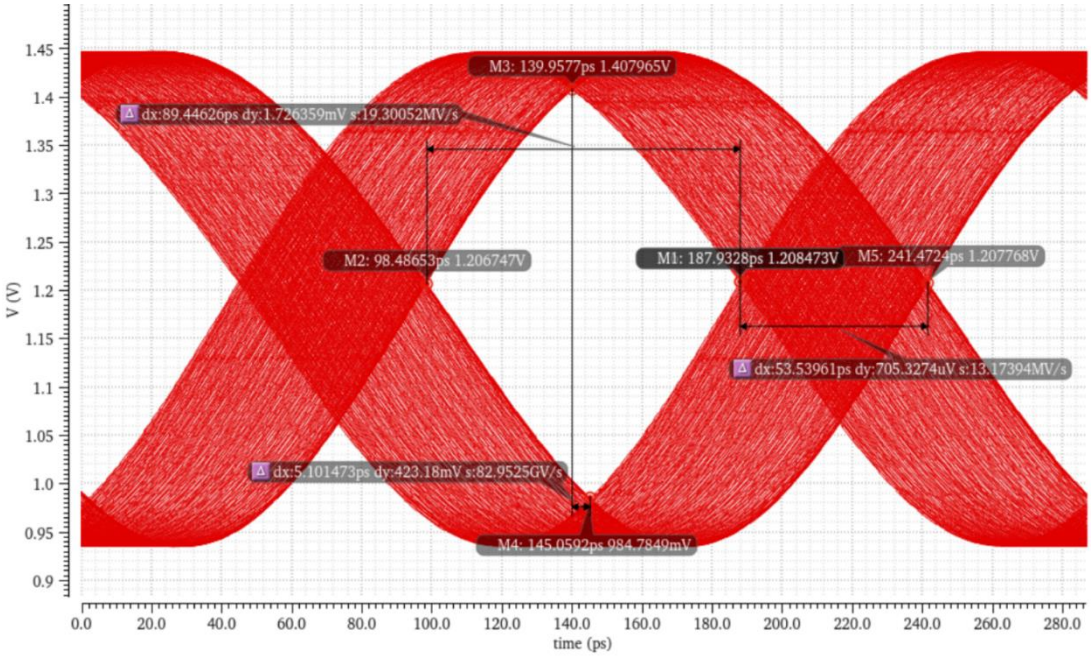

Figure 6.7 : The eye-diagram of the PLL.

6.2.5 Phase noise

Phase noise is a critical performance metric in PLL design, particularly for high-frequency applications such as 5G communications. A low phase noise level ensures minimal interference with adjacent channels and enhances overall system performance. The phase noise analysis of the PLL are conducted to evaluate the spectral stability of the output signal over frequency offsets, with a particular focus on the 1 MHz offset point. To find the overall phase noise of the PLL, a compherensive work in [13] which focuses on calculating each block's phase noise shaped by the loop is followed. The phase noise of each block is simulated individually using the Cadence Virtuoso environment. The simulation results are collected to calculate the overall PLL phase noise shaped by the input/output transfer function of the each block. Then, the individual phase noise contributions to the overall PLL phase noise from each block are summed.

We can define the VCO phase noise shaped by the transfer function as

$$S_{\varphi,out_{VCO}} = \frac{\omega^4(D^2 + \omega^2 C^2)}{\left[-\omega^2 D + K_{gain}(1 - \omega^2 A)\right]^2 + \left[-\omega^3 C + K_{gain}\omega B\right]^2} S_{\varphi,VCO} \tag{6.3}$$

where $A = R_1R_2C_1C_2$, $B = R_1C_1 + R_2C_2$, $C = R_1C_1C_2 + R_2C_1C_2$, $D = C_1 + C_2$.

Using the same methodology, the contributions of the charge pump, phase-frequency detector and loop filter to the overall PLL phase noise are evaluated as

$$S_{\varphi,out_{fwd}} = \frac{K_{VCO}^2\omega^2(D^2 + \omega^2 C^2)}{\left[-\omega^2 D + K_{gain}(1 - \omega^2 A)\right]^2 + \left[-\omega^3 C + K_{gain}\omega B\right]^2} S_{\varphi,fwd} \tag{6.4}$$

where $S_{\varphi,fwd}$ is denoted as the phase noise contributions from the charge pump, phase-frequency detector and loop filter that are grouped as forward-path noise.

As illustrated in Figure 6.8, the PLL achieves a phase noise -116.8 dBc/Hz at 1 MHz offset, meeting the target for 5G NR n78 band requirements. Additionally, the simulations derives that the main contributor to the phase noise is VCO with -120.2 dBc/Hz at 1 MHz offset.

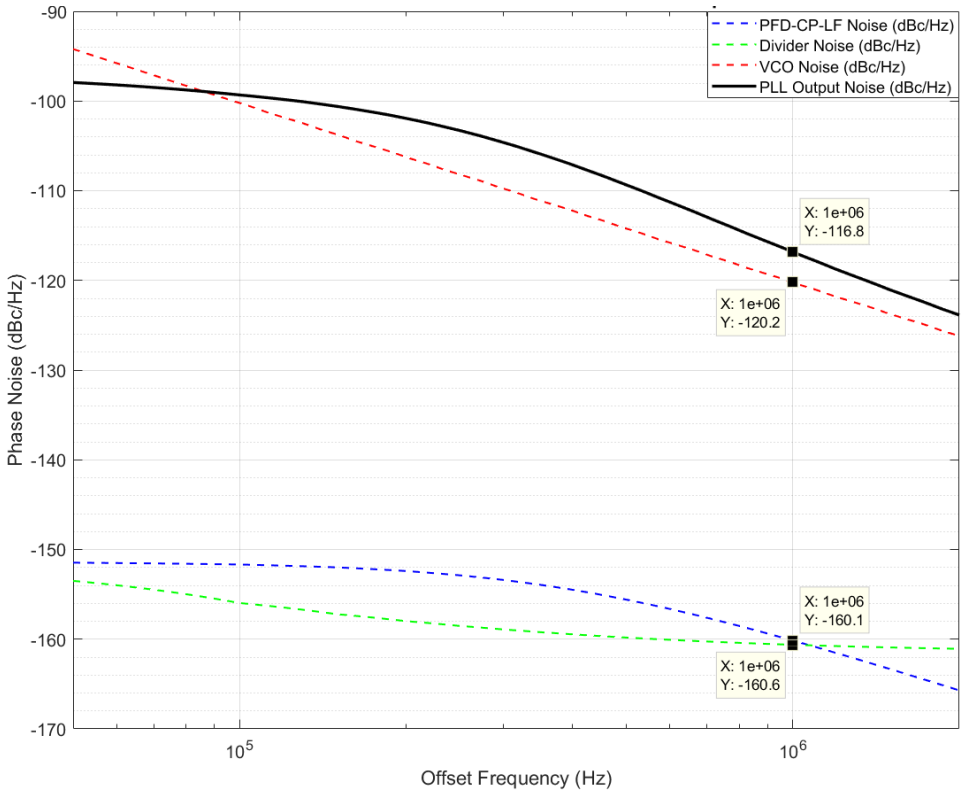

Figure 6.8 : The phase noise of the PLL.

6.2.6 Power consumption

Power consumption is a key consideration in PLL design, especially for mobile and battery-powered applications like 5G NR systems. The total power consumption of the PLL is carefully optimized through the use of low-power circuit techniques and efficient block-level implementations. The total current drawing from the supply voltage is illustrated in Figure 6.9. The average current drawing from the supply is equal to 5.664 mA. The power consumption is equal to 6.7968 mW at a supply voltage of 1.2 V. In conclusion, the PLL aligns with power requirements for the 5G NR n78 band.

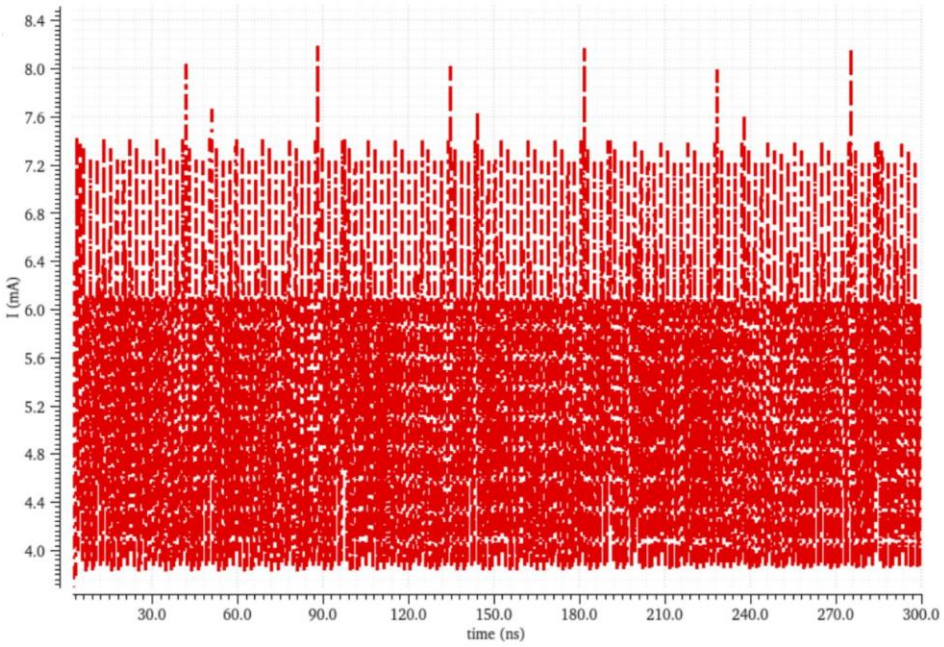

Figure 6.9 : The supply current drawing for power constumption analysis.

6.3 Comparison of the PLL Against Prior Art

The results of the PLL structure are compared with the prior works and summarized in Table 6.1. The design PLL is compared with the fractional-N PLL based dual-feedback loop reported in [29], our design results similar power consumption however phase noise and jitter performance of [29] worse than our design. The jitter even is in the edge of acceptible zone of 5G. On the other hand, this phase noise is introduced by the fractional-N divider whereas our design employs an integer divider.

Another study in [30] results a phase noise performance with -111 dBc/Hz at 1 MHz. However, the power consumption and RMS jitter are higher than the PLL for this

work. This work performs a better FoM with a 6 dB. Another analog PLL studied in [31] results a low-power consumption with a trade-off phase noise an jitter prior. However, this trade-off only makes 4 dB FoM performance difference compared to the PLL in this thesis.

Other report focuses on a constant loop bandwidth in PLL that represented in [32]. The study introduces a servo loop to ensure the charge-pump current scales inversely with the square of the oscillation frequency. This work uses 130 nm technology with a power supply of 1.5 V therefore the power consumption is increased unwillingly. This would be reflected on the FoM, however the study does not provide a jitter analysis. Even though power is willingly sacrificed, the study achieves less than $\pm 4\%$ variation in the loop gain.

Table 6.1 : Summary and comparison table of the design PLL.

Performance parameter	This work[2]	[29][3] 2020	[30][3] 2016	[31][3] 2013	[32][3] 2019
Technology (nm)	65	65	65	65	130
Power supply (V)	1.2	N/A	1.2	1.2	1.5
Tuning range (GHz)	3.3-3.8	3.2 - 3.8	2.2-3.2	3.0 - 4.0	3.1 – 3.9
Reference frequency	10 MHz	77 MHz	40 MHz	40 MHz	16 MHz
Phase noise (dBc/Hz)	-116.8@ 1 MHz	-108@ 1 MHz	-111@ 1 MHz	-128@ 20 MHz	-110.4@ 1 MHz
RMS jitter(fs)	240.904	503	345	463	N/A
Power (mW)	6.7968	6.9	11.7	5	48
FoM[1](dB)	-244.04	-237.58	-238	-239.7	N/A

[1] $FoM = 10\log\left(\frac{jitter^2}{1s^2}\frac{power}{1mW}\right)$

[2] $Simulation$

[3] $Measured$

7. CONCLUSIONS AND RECOMMENDATIONS

This thesis has presented necessary analyses for the design of a phase-locked loop system optimized for 5G New Radio operating in the n78 frequency band. According to literature review, there seems to be no CMOS-based PLL design specifically developed for the n78 band within 5G NR systems. The study begins by establishing a solid theoretical foundation for PLL operation, covering its dynamic behavior, loop stability, and noise characteristics in both time and frequency domains. The fundamental trade-offs among phase noise, power consumption, settling time, and frequency tuning range are examined in detail. Later, the design specifications are introduced and circuit topologies of the design is discussed in detailed. The necessary analyses are performed to ensure the design performs within the targeted specifications.

The PLL designed in this thesis is implemented using the TSMC 65 nm CMOS technology and is simulated using Cadence Virtuoso tool. The topology operates at a supply voltage of 1.2 V. The complete design achieves a phase noise of -116.8 dBc/Hz at 1 MHz offset and the total power consumption of 6.7968 mW. The PLL architecture was compared against literature and it demonstrates that competitive or improved performance in key metrics. The results also confirm that the design meets the stringent requirements of 5G NR n78 band specified in Table 2.2, offering a practical balance between noise performance and power consumption.

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