



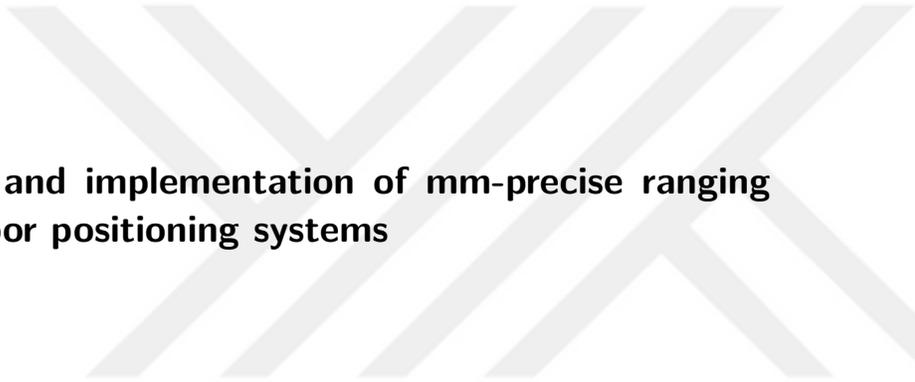
Design and implementation of mm-precise ranging for indoor positioning systems

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Dissertation presented in partial
fulfillment of the requirements for the
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Science:
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Preface

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Tuba
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Abstract

A very precise and fast wireless indoor positioning system becomes necessary for multiple applications such as industrial automation, robot navigation and inventory tracking. The precision of an RF based positioning system can be improved by increasing the bandwidth and the carrier frequency of the signal, as proven by the theoretical studies on estimation precision. However, on the practical side, not only the theoretical concerns but also the hardware design constraints and signal propagation related limitations should be taken into account, which exactly suffer from high bandwidth and carrier frequency. This work enhances the precision of an RF based indoor positioning system, while keeping both theoretical performance and practical limitations into account.

To this end, a range estimation scheme, consisting of both an efficient hardware implementation of a novel phase-based range estimation algorithm and a hardware friendly ranging signal, is proposed. The phase-based range estimation algorithm is designed to exploit the advantages of a wideband signal, while keeping the complexity of the necessary receiver components low. Towards an efficiently implementable estimator, the range estimation algorithm is broken into 3 computational steps. The step-wise approach provides benefits for FPGA implementation as well as flexibility on choosing between transmitted signal energy, computational cost and precision of the ranging algorithm. The proposed ranging algorithm also enables sub-Nyquist sampling which helps to reduce the power consumption of the preceding ADC.

The discrete carrier ranging signal, the second component of the ranging scheme, is designed to relax the design constraints of the transmitter and comply with the sub-Nyquist sampling. By carefully designing the ranging signal, also the baseband signal generation is simplified allowing efficiently generating a wideband signal. Moreover, the power amplifier efficiency is increased by reducing the peak-to-average power ratio of the signal.

Designed to cope with the hardware and environmental imperfections, the

ranging scheme is tested together with a custom designed transmitter and receiver. The tests report a mm-level precision performance of the ranging scheme under real-world conditions. Moreover, they prove the validity and benefits of the sub-Nyquist sampling and baseband signal generation concepts. The ranging scheme, the transmitter and the receiver are finally integrated to obtain a complete indoor positioning system.

Besides this custom made positioning system, an alternative ranging framework compatible with the communication standard IEEE802.11ad is proposed. The phase-based range estimation algorithm is therefore adapted to process the communication packet, and further enhanced against multipath fading by utilizing the channel estimation field provided by the package.

This thesis proposes two ranging systems, highly focusing on the first one, which is optimized for very high precision and used together with custom designed analog and RF components towards a complete positioning system. Developing the core of the first ranging system, a standard-compliant ranging system is also obtained.

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List of Abbreviations and Symbols

Abbreviations

A/D	Analog to Digital Converter
AoA	Angle-of-Arrival
a.u.	Arbitrary unit
AWGN	Additive white Gaussian Noise
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
CE	Channel Estimation
CF-FFT	Common Factor FFT
CORDIC	COordinate Rotation DIGital Computer
CRLB	Cramér-Rao Lower Bound
CRT	Chinese Remainder Theorem
CS	Coarse Step
CT-FFT	Cooley Tukey FFT
CW	Correlation Window
DCM	Digital Clock Manager
DFT	Discrete Fourier Transform
DIF	Decimation in Frequency
DIT	Decimation in Time
EIRP	Equivalent Isotropic Radiated Power
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FPGA	Field Programmable Gate Array
FS	Fine Step
Gbps	Gigabyte per second
GDOP	Geometric Dilution of Precision
GNSS	Global Navigation Satellite Systems

GPS	Global positioning system
GLONASS	GLObal NAVigation Satellite System
I and Q	In-phase and Quadrature
IC	Integrated Circuit
IF	intermediate Frequency
ILS	Incremental Least Squares
IP	Intellectual Property
IR	Infra-ref
ISM	Industrial Scientific and Medical
LMS	Least Mean Squares
LS	Least Squares
LNA	Low Noise Amplifier
LO	Local Oscillator
LoS	Line-of-Sight
LTE	Long Term Evolution
LUT	Look-Up table
MAC	Medium Access Control
ML	Maximum Likelihood
MSE	Mean Square Error
NF	Noise Figure
NLoS	Non-Line-of-Sight
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	peak-to-average power ratio
PF-FFT	Prime Factor FFT
PHY	Physical Layer
PN	Pseudo-Noise
ppm	parts per million
QPSK	Quadrature Phase Shift Keying
RAM	Random Access Memory
RF	Radio Frequency
RMSE	Root Mean Square Error
Rx	Receiver
SFS	Super Fine Step
SH	Sample-and-Hold
SNR	Signal to Noise Ratio
SS	Synchronization Sequence
STD	Standard Deviation
STF	Short Training Field
STS	Short Training Symbol
SVD	Singular Value Decomposition
ToA	Time-of-Arrival

TDoA	Time difference-of-arrival
ToF	Time-of-Flight
Tx	Transmitter
ULA	Uniform Linear Array
UW	Unwrapping
UWB	Ultra-wideband
VCO	Voltage Controlled Oscillator
WSN	Wireless sensor network
ZZLB	Ziv-Zakai Lower Bound

Symbols

B	Bandwidth
c	Speed of light
d_i	Distance between the tag and the i th base station
$E[\cdot]$	Expected value operator
E	Signal energy
$\exp(x)$	e^x , with e is the Euler's number
f	frequency
f_c	Center frequency
f_{clk}	Clock frequency
f_{NYQ}	Nyquist frequency
f_{RX}	Receiver clock
f_{TX}	Transmitter clock
f_s	Sampling frequency
Ga, Gb	Two sequences forming a Golay pair
$H(f)$ and $h(t)$	Channel frequency and time response
j	Imaginary unit ($\sqrt{-1}$)
k_{ss}	Sub-Nyquist sampling factor
LB	Lower bound
N	Number of sub-carriers
$N_0/2$	Power spectral density of noise
N_{kT}	Thermal noise
N_s	Number of symbols
N_{STS}	Number of Short Training Symbols
N_{TS}	Number of training symbols
P_L	Free space path loss
P_{in}	Input power (to the PA)
P_{out}	Output power (of the PA)
$r(t)$	Received waveform
$r_i(t)$ and $r_q(t)$	Received waveform, in-phase and quadrature

R_{max}	Maximum range covered by the ranging system
$S(f)$	Signal power spectral density
t	used for time index
t_f	Signal transmit time
t_i	Arrival time of the signal to the i th base station
t_{si}	Sampling start time in the i th base station
T	Signal duration
T_C	Chirp rate
T_{CW}	Correlation Window length
T_p	Period duration
T_{SYM}	Symbol duration
UB	Upper bound
$v(t)$	Additive noise
w_c	Center radial frequency, $2\pi f_c$
$\hat{\cdot}$	Estimation operator
α_i	Gain of the i th signal path
β^2	Effective (Gabor) bandwidth
$\delta(t)$	Dirac delta function
λ	Carrier wavelength
ϕ_n	The phase of the n th sub-carrier
ϕ_n^r	The phase of the n th sub-carrier, relative to θ_1
σ	Standard deviation (is used for precision)
τ	Signal delay
$\hat{\tau}_1$	Delay estimation by the coarse step
$\hat{\tau}_2$	Delay estimation by the fine step

Appendix A

FFT implementation for LTE systems

The FPGA implementation of the 1536 point FFT with output pruning is expanded to be used for the emerging communication standard LTE (long Term Evolution). An output pruning enabled varying length FFT as proposed in [Ayh14] will be briefly explained in this Appendix.

The LTE requires 128-2048/1536 size FFT, providing a flexible spectrum support from 1.4 up to 20 MHz [Gho11]. Moreover, output pruning would be a nice asset since the information is transmitted in resource blocks. One resource block contains 12 subcarriers and occupies 1.4 MHz of bandwidth. Number and position of the resource block in the spectrum can be altered online by the resource block allocation principle of LTE. Considering this energy saving principle, an online input size programming scheme and an efficient output pruning method would be two nice assets for an FFT implementation to be used in the LTE systems.

The FFT architecture is introduced in Section A.1. The hardware implementation of this architecture is presented and compared with two implementations that tackle similar challenges in Section A.2.

	128~2048/1536 point pruning with	128~2048 point	128~512 point
Occupied slices	787	728	581
DSP48Es	30	14	14
Total Memory (kb)	612	594	252
RAM Blocks	22	22	9

Table A.1: Resources for variable length FFT

A.1 Architecture

The FFT architecture of this work is a combination of the widely used CF-FFT with a DFT as explained in Chapter 4. The main extension to the proposed architecture is the variable input length, provided by the 128 point FFT blocks used as the core of the architecture.

A 128 point FFT has 7 stages which comprises the 7 stages close to the FFT output for the 256~2048 point FFT. For a 2^M point FFT, $2^M/128$ times the 128 point FFTs and $M - 7$ input stages are needed. With the programmable twiddle factors for both the input stages and the 128 point FFT, CF-FFT size can be changed online. The architecture given in Figure 4.10 is used with 4 extra input stages which can be turned off when the FFT size less than 2048.

This architecture enables output pruning as well, which is the second asset aimed for this FFT implementation.

A.2 Hardware implementation and comparisons

Implementation is done on a Xilinx Virtex-5 (XC5VFX130T-2FFG1738CES) FPGA. The resource usage is given in Table A.1.

The implementation performance is compared with two hardware efficient and high throughput FFT architectures for LTE systems given in [Pat13] which is synthesized on 130 nm ASIC technology and [Che12] which is implemented on Virtex-5 FPGA. Both of these designs employ radix-3 support to compute 1536 point FFT.

These proposed implementations are compared by resource utilization and

	[Ayh14]	[Pat13]	[Che12]
LUTs (Virtex-5)	3148	NA	23807
Total Memory (kb)	612	NA	224
Area (kgates)	NA	109	NA
Computation clk cycles (2048 pnt)	8195	12345	3072
Computation clk cycles (1536 pnt, 60-900 subcarriers)	1646-2906	9324	4224

Table A.2: Comparison

computation time in clock cycles in Table A.2. Using PF-FFT instead of a mixed-radix architecture, leads to a significant increase in throughput in typical LTE workloads because it enables output pruning.

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Biography

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