DOKUZ EYLÜL UNIVERSITY

GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

MITIGATION OF SURGE CURRENT, VOLTAGE AND PARASITIC OSCILLATIONS IN POWER ELECTRONIC CIRCUITS

by

Buket TURAN AZİZOĞLU

October, 2014

İZMİR

MITIGATION OF SURGE CURRENT, VOLTAGE AND PARASITIC OSCILLATIONS IN POWER ELECTRONIC CIRCUITS

A Thesis Submitted to the
Graduate School of Natural and Applied Sciences of Dokuz Eylül University
In Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy in Electrical and Electronics Engineering,
Electrical and Electronics Program

by
Buket TURAN AZİZOĞLU

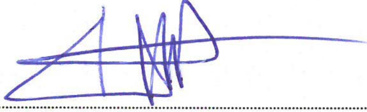
October, 2014
İZMİR

Ph.D. THESIS EXAMINATION RESULT FORM

We have read the thesis entitled "**MITIGATION OF SURGE CURRENT, VOLTAGE AND PARASITIC OSCILLATIONS IN POWER ELECTRONIC CIRCUITS** " completed by **BUKET TURAN AZİZOĞLU** under supervision of **PROF. DR. HALDUN KARACA** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Doctor of Philosophy.

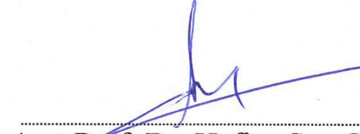
Prof. Dr. Haldun KARACA

Supervisor



Prof. Dr. Uğur ÇAM

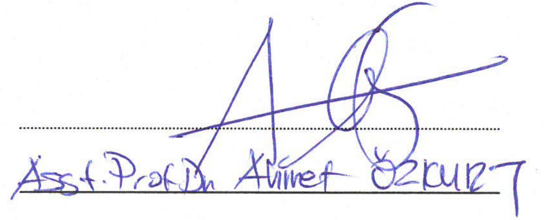
Thesis Committee Member



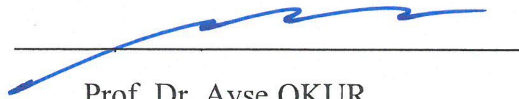
Asst.Prof. Dr. Hafize Şen ÇAKIR

Thesis Committee Member

Examining Committee Member



Examining Committee Member



Prof. Dr. Ayşe OKUR
Director
Graduate School of Natural and Applied Sciences

ACKNOWLEDGMENTS

First and foremost, I express my deepest gratitude to my advisor Prof. Dr. Haldun KARACA for his guidance and advices at every stage of this dissertation.

I would like to thank the members of my thesis committee, namely Prof. Dr. Uğur ÇAM and Asst. Prof. Dr. Hafize Şen Çakır for their useful comments and suggestions.

I am also very grateful to Asst. Prof. Dr. Serkan Günel, Asst. Prof. Dr. Hacer Şekerci and Research Assistants Dr. Abdül Balıkçı and Şebnem Seçkin Uğurlu for their scientific advices and knowledges and many insightful discussions and suggestions.

I express my gratitude to my family for their patience, supportive and moral support encouragement. I always knew that they believed in me and wanted the best for me. And, most of all for my loving and patient husband Serkan Azizoğlu whose faithful support during the all stages of this Ph.D. is so appreciated. And I would also like to thank my little daughter, Selin Azizoğlu for the joy and inspiration she brings to me, filling me with energy and teaching me that life does not consist of only career.

I would also like to express my gratitude to my teachers and all friends (they know who they are) for their support and helping me get through difficult times.

Buket TURAN AZİZOĞLU

MITIGATION OF SURGE CURRENT, VOLTAGE AND PARASITIC OSCILLATIONS IN POWER ELECTRONIC CIRCUITS

ABSTRACT

Parasitic oscillations and sudden increase in voltage and current may cause power electronic active devices to break down or to be destroyed. This occurs more obviously during switching and possibly causes serious failures. The factors causing these cases should be carefully observed and analyzed in design stage of power electronic circuit. Possible precautions can be taken by this way before the damage occurs.

In this thesis, behaviors of MOSFETs and diodes used especially at transitions and problems occurred in inverter circuits during switching, solutions offered in the literature like zero voltage switching and using Snubber circuits have been also studied both with simulation and practical work.

Two new methods have been offered in design stage of power switching circuits to detect the problems especially occurred at switching intervals. The first method, in which 3D electromagnetic simulation model is used, S-parameters of circuit including parasitic effects have been involved in direct model with the actual size and the same material. Thus, the same case as in application was created in design phase.

To detect the problems in design stage of power switching circuits especially occurred at switching intervals, two new methods have been offered. This proposed model consists the effects of the properties of MOSFET's all conduction stage regions (cut off, active and saturation) and parasitic inductive effects on circuit's operation by using the parameters of MOSFET's manufacturer's datasheet. This proposed technique assumes non-linear MOSFET capacitors as linear. In fact, this assumption causes some errors in simulation results since MOSFET capacitor values are operating point dependent. However, convergence errors nearly always disappear

by using this modeling technique. Hereby, proposed modeling and simulation techniques could be used to verify the results of more advanced simulation software or at least to obtain approximated simulation results.

Keywords: Switching power circuits, zero voltage switching, snubber circuit, MOSFET modelling

GÜÇ ELEKTRONİĞİ DEVRELERİNDE AŞIRI AKIM, AŞIRI GERİLİM VE PARAZİTİK OSİLASYONLARIN AZALTILMASI

ÖZ

Parazitik osilasyonlar, akım ve gerilimin ani yükselmesi güç elektroniği devrelerinin yanmasına veya bozulmasına yol açabilmektedir. Anahtarlama anında çok daha belirgin bir şekilde oluşmakta ve muhtemelen ciddi hatalara sebep olmaktadır. Bu durumların ortaya çıkmasına neden olan faktörler tasarım aşamasındayken dikkatlice gözlenip analiz edilmelidir. Ancak bu sayede devrede tahribata yol açmadan olası önlemler alınabilir.

Bu tezde, ayrıca özellikle geçiş anında kullanılan MOSFET, diyot gibi yarı iletken elemanların davranışları, bazı çevirici devrelerinde anahtarlama anında oluşan sorunlar ile sıfır voltaj anahtarlama ve snubber devreleri kullanma gibi literatürde önerilen çözümler hem benzetim hem de uygulama yapılarak incelenmiştir.

Özellikle anahtarlama zamanında güç anahtarlama devrelerinde oluşan problemlerin tasarım aşamasında saptanabilmesi için iki yeni metot önerilmiştir. Üç boyutlu elektromanyetik benzetim modelinin kullanıldığı birinci metot, devredeki yolların uygulamada kullanılan ölçüde ve malzemede tasarlanarak devrenin parazitik etkilerini içeren S-parametreleri yardımı ile direk modelde yer alması sağlanmıştır. Böylelikle uygulamanın birebir aynı durumu tasarım aşamasında yaratılmaktadır.

Önerilen diğer yöntem, çok düşük anahtarlama zamanı için avantajlarından dolayı çok yaygın olarak kullanılan bir MOSFET sürüce devresine uygulanmıştır. Bu önerilen model MOSFET üretici firma veri sayfasındaki parametreler kullanılarak MOSFET'in iletime geçmesi aşamasındaki tüm (kesim, aktif ve doyum) bölgelerinin özelliklerinin ve parazitik endüktif etkilerin devrenin çalışmasına etkilerini içermektedir. Bu önerilen basit teknik lineer olmayan MOSFET kapasitelerine lineer olarak var sayar. Aslında bu varsayım, benzetim sonuçlarında hataya neden olur çünkü MOSFET kapasite değerleri çalışma noktasına bağlıdır. Fakat bu modelleme

tekniği kullanılarak, yaklaşım hataları neredeyse her zaman yok olur. Böylelikle, önerilen modelleme ve benzetim teknikleri daha gelişmiş benzetim yazılımı sonuçların doğrulamak veya en azından yaklaşık benzetim sonuçları elde etmek için kullanılabilir.

Anahtar kelimeler: Anahtarlamalı güç çeviricileri, sıfır voltaj anahtarlama, snubber devresi, MOSFET modellenmesi,

CONTENTS

Page

THESIS EXAMINATION RESULT FORM ii
ACKNOWLEDGEMENTS iii
ABSTRACT.. iv
ÖZ v
LIST OF FIGURES vi
LIST OF TABLES vii

CHAPTER ONE – INTRODUCTION 1

1.1 Historical View of Power Electronic Devices 2

1.2 Thesis Objectives.. 3

CHAPTER TWO – CHARACTERISTICS OF POWER ELECTRONIC DEVICES 6

2.1 Electrical Properties of Power Electronic Devices............................ 6
2.2 Diode’s Characteristics.. 9
2.2.1. Soft and Snappy Recovery.. 10
2.3 Power Diode Models 12
2.3.1. SPICE Diode Model Parameters 13
2.3.2 Reverse Recovery Simulations 15
2.3.3 Forward and Reverse Recovery Calculations............................. 18
2.4 Evaluating Some of the MOSFET Switching Parameters by Implementing of a Boost Converter... 21
2.4.1 Operating Principle of the Driver Circuit 22
2.4.2 Power Stage 24
2.4.3 Failure of the Driver Circuit 25
2.4.4 Dynamical Behavior Effects of Diode Parameters on Transient Waveforms... 26
2.4.5 Selection of the Inductance value 29

CHAPTER THREE – POWER MOSFET'S AS SEMICONDUCTOR SWITCHES AND THEIR DRIVING CONSIDERATIONS.............................. 33

3.1 MOSFET Characteristics 33
3.2. The MOSFET Switching Test Circuit for the Resistive Load Case............... 35
3.2.1 Derivation of Miller Effect 35
3.2.2 Simulation Work of the Switching Test Circuit with a Resistive Load .. 38
3.3 Analyzing a MOSFET Switching Circuit with an Inductive Load 42
3.3.1 Simulation and Calculation of a Switching Test Circuit with an Inductive Load 43
3.3.2 Reverse Recovery Phenomena in Circuits with an Inductive Load 48

CHAPTER FOUR – ZERO VOLTAGE SWITCHING TECHNIQUE AND WAVEFORMS IN HIGH FREQUENCY POWER PROCESSING CIRCUITS…. 49

4.1 Studying a Series Resonant Inverter Operation 50
4.1.1 The Resonant and Operating Frequencies of a Resonant Inverter 54
4.1.2 Simulation and Practical Results of a ZVS Inverter Implemented.......... 56
4.1.3 Simulation and Experimental Results of Lower Side MOSFET Drain-Source Voltage and Current Above and Below Resonant Frequencies 59

CHAPTER FIVE – INVESTIGATION OF PARASITIC EFFECTS OF A BOOST CONVERTER 63

5.1 A Practical Study on a Boost Converter Circuit and Layout Model............... 65
5.2 Mathematical Calculations of Ideal case of Boost Converter 67
5.3 Analysis of the MOSFET Turn-on Switching Behaviour With Parasitics...... 70
5.4 Comparison of Simulation and Experimental Results 74
5.4.1 Diode Current Waveform 74
5.4.2 MOSFET Voltage Waveform... 76
5.4.3 Load Current Waveform.. 78

5.4.4 Inductor Current Waveform 80

CHAPTER SIX – SNUBBER CIRCUIT DESIGN FOR MITIGATION OF MOSFET TURN-OFF OVERSHOOT VOLTAGE IN A BOOST CONVERTER 83

6.1 RCD Snubber Circuit and Application for the Purpose of Snubbing Overvoltage 84

6.2 Simulation and Experimental Results Revealing Snubber Circuit Effectiveness 88

CHAPTER SEVEN – EXPERIMENTAL WORKS ON MOSFET DRIVER (BUFFER) CIRCUIT 91

7.1 Topology of the CMOS Buffer Circuit 92

7.1.1 Equivalent Circuit Model of the CMOS Buffer Circuit 92

7.1.2 Equivalent Circuit Model of the Buffer Circuit for the high to low Input Transition 93

7.2 Proposed Analytical Model of the CMOS Buffer Circuit 95

7.2.1 Parameters Used in the Proposed Analytical Model 95

7.2.2 Proposed Analytical Model for the Switching Behaviour of the MOSFET with Capacitive Load 98

7.2.2.1 Distinctive Features for Interval Two 101

7.3.2.2 Distinctive Features for Interval Three 102

7.2.3 Analytical, Simulation and Experimental Model Results 103

CHAPTER EIGHT – CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK 113

8.1 Conclusion 113

8.2 Suggestions for Future Work 115

REFERENCES **116**
APPENDICES **123**

LIST OF FIGURES

Page

Figure 2.1 Scheme of the cubic unit cell of the diamond crystal structure. 2-5 are the nearest neighbors of atom 1 and the tetrahedral bonding between them is shown. 8
Figure 2.2 Cross section of a Pin diode. Depletion region gets wider and the capacitance of the diode is reduced due to the intrinsic layer. 9
Figure 2.3 Reverse recovery current waveform 10
Figure 2.4 Recovery characteristics of diodes a) Soft recovery b) Abrupt recovery..11
Figure 2.5 Turn-on behavior of a power diode, here a current pulse with a limited di/dt is applied to diode in forward directions and then a forward recovery voltage waveform is obtained. 12
Figure 2.6 Diode a) symbol b) SPICE model with reverse biased............................ 13
Figure 2.7 Schematic of the simulated buck converter. 15
Figure 2.8 Diode current waveforms of a) GI571 b) BYT28-300 c) UG10DCT d) MBRF1660.. .17
Figure 2.9 Circuit schematic of the implemented basic boost converter circuit. Note that, capacitor C3 is a part of driver circuit.. 22
Figure 2.10 a) Current flowing path during the start-up of the driver circuit (V_{ss} is turning on) b) Model of the transient driving current flow c) Transient drive current path of Q3 and Q2 at start up 25
Figure 2.11 Collector Currents of Q2 and Q3 of Figure 2.10 Simulation Results when just at V_{ss} supply voltage is connected to circuit, pulse input of the circuit is shorted to ground. Note that nearly the same currents flow both transistors. 26
Figure 2.12 Waveforms associated to Boost Converter implemented with BA157 fast recovery diode a) MOSFET gate- source driving voltage waveform b) anode voltage (referenced to ground) waveform, 2 volt/div, 2µs time/div 27
Figure 2.13 Waveforms associated to Boost Converter implemented with BYV08 ultra fast recovery a) MOSFET gate-source driving voltage waveform

b) Anode voltage (referenced to ground) waveform, 2 volt/div, 2 µs time/div. 27
Figure 2.14 Waveforms associated to Boost Converter implemented with MBR745 Schottky Diode a) MOSFET gate voltage waveform b) Anode voltage referred to ground of MBR745 (Schottky) diode, 2 volt/div, 2 us time/div. Note that diode turn-on spike occurs hardly ever. 27
Figure 2.15 Reverse recovery current waveform for the diodes are measured via a current probe with 1 mA/mV scaling factor, 0, 2 volt/div a) Current waveform of the diode for the BA157 fast diode b) Current waveform of the diode for the BYV08 ultra fast diode c) Current waveform of the diode for the MBR745 Schottky diode .... .28
Figure 2.16 Current waveform of the inductor 1 value measured by current probe 1 mA/mV, 0.2 volt/div and diode anode voltage 2 volt/div. Note that diode reverse recovery tails disappeared... 30
Figure 2.17 Diode anode voltage waveform when high inductance value (inductor 2) is used... 30
Figure 2.18 a) Measurement results of inductor 1 b) Measurement results of inductor 2 31
Figure 2.19 Equivalent circuit parameters for a) inductor 1 b) inductor 2. 31
Figure 3.1 Model of a MOSFET with lumped elements. 34
Figure 3.2 Common source switching circuit with resistive load for studying Miller Effect. 35
Figure 3.3 a) Small signal equivalent circuit of the circuit seen in Figure 3.2 at switching instant b) Small signal equivalent circuit of the common source amplifier circuit using Miller approximation 37
Figure 3.4 MOSFET gate-source voltage waveforms of the circuit seen in Figure 3.2 for a) V_{DC}=20 Volt b) V_{DC}=200 Volt 39
Figure 3.5 Drain voltage and current waveforms of the MOSFET seen in Figure 3.2 for a) V_{DC}=20Volt b) V_{DC}=200 Volt. 40
Figure 3.6 Gate current waveforms of the MOSFET seen in Figure 3.2 for a) V_{DC}=20Volt b) V_{DC}=200 Volt.. 41

Figure 3.7 Switching test circuit with an inductive load used for simulation purposes 42
Figure 3.8 Simulation results of the MOSFET gate-source voltage during a) turn-on b) turn-off, drain-source voltage during c) turn-on d) turn-off 43
Figure 3.9 Simulation results of the MOSFET a) drain turn-on current b) drain turn-off current c) gate turn-on current c) gate turn-off current. 44
Figure 3.10 Simulation waveforms of circuit of Figure 3.7 a) gate voltage b) drain voltage c) gate current d) drain current 48
Figure 4.1 Resonant load circuit model (a current source) for only very short time duration (due to series inductance).. 51
Figure 4.2 Schematic of the prototype circuit a) driving signal underlapping circuit b) floating driver and power stage 51
Figure 4.3 a) Driving signal simulation waveforms b) Driving signal experimental waveforms, 2 μs time/div, of the MOSFETs' driving signals of the circuit given in Figure 4.2 56
Figure 4.4 Commutation scheme of half- bridge Resonant Inverter switches a) Power stage with internal capacitance and diodes of the MOSFET b) Current commutates from M1 to M2 by turning on M1 and turning of M2 c) Current flowing path when the voltage of the lower side MOSFET capacitance (C2) voltage decreases to zero voltage d) Current path when resonant load current reversals 57
Figure 4.5 a) Current flowing path during charging and discharging of the MOSFETs' internal capacitances b) Current flowing path when the voltage of the upper side MOSFET's capacitance (C1) decreases to zero voltage c) Current path when gate voltage is applied to the upper side MOSFET 58
Figure 4.6 a) Simulation waveforms of resonant capacitor current and voltage of the load above resonant frequency b) Experimental waveforms of resonant capacitor current and voltage, 2 μs time/div 59
Figure 4.7 a) Simulation results of lower side MOSFET drain-source voltage and drain current b) Experimental results of lower side MOSFET drain-

source voltage and current, $f_{switching}$ =124 kHz, and $f_{resonant}$ =105.7 kHz, 2 µs time/div 61
Figure 4.8 a) Simulation waveforms of lower side MOSFET drain-source voltage and drain current b) Experimental waveforms of lower side MOSFET drain-source voltage and Drain current $f_{switching}$ =70.3 kHz, and $f_{resonant}$ =105.83 kHz , 2 µs time/div 62
Figure 5.1 Circuit schematic of the implemented Boost Converter 66
Figure 5.2 Layout designed in CST MW STUDIO 67
Figure 5.3 CST DESIGN STUDIO Schematic 68
Figure 5.4 Circuit model with inductive wiring parasitic and MOSFET intrinsic capacitances. Here, component parasitics and layout stray capacitance are neglected…... 71
Figure 5.5 Diode current waveform a) Simulation with SPICE (without taking into account physical connections parasitics) b) Co-simulation with CST MW STUDIO and DESIGN STUDIO c) Practical result, frequency is 101.5 KHz, 1 amp/div, 2 µs time/div 76
Figure 5.6 MOSFET drain voltage waveforms a) Simulation with SPICE (without taking into account physical connections parasitics) b) Co-simulation with CST MW STUDIO and DESIGN STUDIO c) Implementation result, 10 volt/div, 2 us time/div d) Simulation with CST MW STUDIO for one period e) Implementation result for one period 78
Figure 5.7 Complete current path of the load when MOSFET is a) ON b) OFF...... 79
Figure 5.8 The load current waveforms a) SPICE simulation result (without considering physical connection parasitics) b) Co-simulation with CST MW STUDIO and DESIGN STUDIO c) Measurement result , 1 amp/div (due to current probe scaling settings) , 2 µs time/div. 80
Figure 5.9 Inductor current a) Simulation with SPICE (without taking into account physical connections parasitics) b) Co-simulation with CST MW STUDIO and DESIGN STUDIO c) Implementation result, 1 amp/div, 2 µs time/div. 82
Figure 6.1 Boost Converter with turn-off Snubber Circuit 86

Figure 6.2 Test circuit designed for determining experimentally the load parasitic inductance value 89
Figure 6.3 MOSFET drain-source voltage waveforms without snubber circuit a) simulation results b) Experimental results 5volt/div, 2μsec/div 90
Figure 6.4 MOSFET drain-source voltage waveforms with snubber circuit a) simulation results b) Experimental results 5volt/div, 2μsec/div 91
Figure 7.1 The partially analyzed CMOS buffer circuit, the transistor N_2 behavior is analyzed for output transition high to low, and load is assumed a simple capacitor element with an initial charge of Q 94
Figure 7.2 Figure 7.2 Practical waveforms of MOSFET driver (buffer) circuit, output voltage waveform 5 volt/div (red one), load current waveform measured with P6022 current probe 1A/ div (blue one) 95
Figure 7.3 Output of the driver stage's equivalent circuit model, Buffer circuit 2nd stage's model for its output transition 1 to 0. 96
Figure 7.4 Current flowing paths when MOSFET is in cut-off region. 101
Figure 7.5 Closed loops of the circuit when MOSFET is in saturation region 103
Figure 7.6 Closed loops of the circuit when MOSFET is in ohmic region 104
Figure 7.7 MOSFET gate –source voltage waveforms with 2.2 Ω gate resistance a) CST Design STUDIO b) Proposed model c) Experimental result (500 ns/div, 5 volt/div). 106
Figure 7.8 MOSFET gate –source voltage waveforms with 47 Ω gate resistance; a) CST Design STUDIO b) Proposed model c) Practically obtained results (500 ns/div, 5 volt/div) 107
Figure 7.9 MOSFET gate-source voltage waveforms with 220 Ω gate resistance; a) CST Design STUDIO b) MATLAB c) Implemented result (500 ns/div, 5 volt/div).. 108
Figure 7.10 Capacitive load voltage waveforms with 2.2 Ω gate resistance a) CST Design STUDIO b) MATLAB c) Practically obtained result (500 ns/div, 10 volt/div) 109
Figure 7.11 Capacitive load voltage waveforms with 47 Ω gate resistance a) CST Design STUDIO b) MATLAB c) Practically obtained result (500 ns/div, 10 volt/div) 110

Figure 7.12 Capacitive load voltage waveforms with 220 Ω gate resistance a) CST Design STUDIO b) MATLAB C) Practically obtained result (500 ns/div, 10 volt/div) 111
Figure 7.13 MOSFET drain-source voltage waveforms with 2.2 Ω gate resistance a) CST Design STUDIO b) MATLAB/Simulink C) Practically obtained result (500 ns/div, 5 volt/div) 112
Figure 7.14 MOSFET drain-source voltage waveforms with 47 Ω gate resistance a) CST Design STUDIO b) MATLAB/Simulink C) Practically obtained result (500 ns/div, 5 volt/div) 113
Figure 7.15 MOSFET drain-source voltage waveforms with 220 Ω gate resistance a) CST Design STUDIO b) MATLAB C) Practically obtained result (500 ns/div, 5 volt/div) 114

LIST OF TABLES

Page

Table 2.1 Diode SPICE Parameters. Note that, “*” means the parameter is effected by the area 14
Table 2.2 SPICE parameters of the diodes used in simulations................................ 15
Table 2.3 Diode peak reverse recovery currents obtained from simulations............. 18
Table 7.1 Parameters and abbreviations used in analysis 99

,

CHAPTER ONE
INTRODUCTION

Switching power converters with high efficiency, more reliable and fast transient response systems are provided by the developments in the power electronic industry. Also, increasing the power density and decreasing the size and cost are expected because of choosing relatively high frequencies in designs of those systems. To achieve these goals, high frequency is generally chosen in designs of those systems. However, high frequency applications have some drawbacks such as high driver losses, serious current/voltage stresses and oscillatory waveforms. Additionally, high di/dt and dv/dt produced by the switching action creates high Electromagnetic Interference (EMI). In order to achieve these demands and to prevent the failures, all influencing factors should be considered to observe the behaviour of the power circuit especially during switching action analysis.

Switch mode power converter circuits generally have a higher efficiency than their linear power conversion counterparts. However there are various loss mechanisms in these types of circuits. The aim of this work is to investigate the causes of the losses, main failure mechanisms and discuss some mitigation.

Layout of the Printed Circuit Board (PCB) and wiring characteristic properties of the power semiconductor devices play an important role for determining the efficiency of power electronic circuits and risks of the failures. Dimensions, speeds and operating frequency of the power semiconductor devices should be taken into account as well.

Power semiconductor devices are divided into subcategories according to the terminal number and performance of the power semiconductor devices. Beside the terminal classification, power electronic devices divided into two groups with respect to the performance; majority and minority carrier devices (Hummel, 2004; Erickson, 2000). Minority carrier devices have lower on-resistance than majority carrier devices. On the other hand, switching speed of minority carrier devices is lower than

majority carrier devices since controlling the minority charges in minority carrier devices takes longer time than the charge required controlling equivalent majority carrier devices. Thus, majority carriers are more appropriate than minority carriers due to controlling the charges for applications including low voltage levels and high switching frequencies (Erickson, 2000). Minority carrier devices are PIN diodes, IGBT, BJT and thyristors and majority carrier devices are Schottky diodes, power MOSFETs and JFETs.

1.1 Historical View of Power Electronic Devices

In 1906, Lee De Forest invented Vacuum Tube device to rectify alternating currents. But this had limitations in conducting electricity and had low current capacity, and it required more space. Mercury Arc Tubes were used from 1920 to 1940, since they could be used at power levels of hundreds of kilowatts. However, large space and low efficiency were the disadvantages of the Mercury Arc Tubes. From late 1940s to late 1960s, selenium rectifiers became popular since they had smaller size, longer life, lower drop or loss which intended that DC voltages were higher than tubes. On the other hand, Selenium had some disadvantages such as getting dangerous and toxic in higher amounts and being flammable when the units get older and run hotter (Bonkowski, 2007). Russell Ohl discovered the p-n junction and photovoltaic effects in silicon in 1940. This allowed for the development of junction transistors and solar cells and it also offered an insight into the design of semiconductor devices. Silicon Transistors (BJTs) were introduced in Bell Telephone Laboratories by Dr. William Shockley, Dr. John Bardeen and Dr. Walter H. Brattain in 1948. These transistors have no warm-up delay since they have no vacuum, glass envelope, grid, plate, and cathode (Bell Telephone Laboratories, 1948). In the late 1950s Semiconductor power diodes were available. Silicon controlled rectifier (SCR) were demonstrated in 1956 by General Electric. Large levels of current are switched using only a small control current and also high voltage can be switched by SCR. But then, they are not suitable for high-power DC circuits since they cannot be easily turned off. Jack Kilby invented the Integrated Circuit that could work function as transistors, diodes, resistors, and capacitors,

formed from a single crystal (monolithic) actually constructed on germanium rather than silicon in 1958, since he could not find a suitable piece of silicon at the time. Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) for integrated circuits were introduced by John Atalla and Dawon Kahngv in 1959. Power MOSFETs become commercially available in 1976 as alternatives to bipolar transistors. MOSFETs have the advantage in current and heating since no current flows through their gates and they can be switched at higher frequencies. In 1982 Insulated Gate Bipolar Transistor (IGBT) was introduced (Baliga, Adler, Gray, & Love, 1982). Recently, the size, speed and performance of the power electronic devices are developing rapidly.

1.2 Thesis Objectives

The main goal of this thesis is to determine the reasons of failures in power electronic circuits such as surge current, voltage and parasitic oscillations especially during switching transitions and to find solutions for these unwanted events. To overcome these failures operating principle, component characteristic and layout characteristics should all be investigated in the design stage. For this aim, analytical and simulation models are proposed and implementation analysis of different power electronic circuits are compared with the proposed models.

In the second chapter brief information about electrical properties of power electronic devices is given. Electrical properties include insulators, semiconductors, conductors and superconductors. Semiconductors play an important role during switching. One of the critical semiconductor materials is diode and is especially emphasized in this chapter. Main types of diodes, specific properties and diode models are summarized. Diode model characteristics such as reverse recovery time, reverse recovery current and forward recovery voltage are compared with different types of diode by using CST DESIGN STUIDO software. MOSFET switching parameters of a Boost Converter are investigated for different diode models by implementing the circuit with a high speed driver. Effects of the converter's operating mode are presented in details as well.

MOSFET is preferred rather than Bipolar Junction Transistor as switching element in power electronics. The intrinsic capacitances of the MOSFET effect the switching time in high frequencies. Increment in the effective value of the gate drain capacitance of the MOSFET is called “Miller Effect” which is very critical for the switching time. The internal structure of the MOSFET and effect of the internal capacitances are investigated in the third chapter. Basic power circuit with a resistive load and an inductive load is simulated with SPICE simulation program and shown in this chapter. Also, reverse recovery effect on power circuit switching inductive load is investigated.

Some techniques are used to mitigate over-voltage, over-current and losses in switching applications. Soft switching techniques are widely used one and divided into zero voltage switching (ZVS) and zero current switching (ZCS) (Perret, 2009). Implementation and simulation results of Half-Bridge Series Resonant Inverter in zero voltage switching are explained in the fourth chapter. Resonant frequency is an effective parameter to prevent the MOSFET’s body diode’s losses. Simulation and experimental results of lower side MOSFET drain-source voltage and current above and below resonant frequencies are compared to see the MOSFET’s body diode’s effect.

Beside these, as known EMI (Electromagnetic Interferece) becomes a critical issue in switched mode power supplies since there exist pulse shaped power signals. To observe these undesired issues in debt it is necessary to take circuit active component parasitics and also parasitic effects due to layout at the design level. Not only the characteristic properties of the elements are important but also the physical geometry and placement of the components are important for the EMI. Simulation programs such as SPICE do not give satisfactory results for the Electromagnetic Interference (EMI), since the exact layout can not be integrated to the simulation. Co-simulation techniques simulating both full-wave modeling and voltage and current based modeling are necessary. To achieve this, one of the 3D electromagnetic field simulation programs, called Computer Simulation Technology (CST) Microwave Studio, is used. Basic boost converter design is made by using both CST

Microwave Studio and CST Design Studio and it is implemented in the laboratory. MOSFET voltage, diode and inductor current waveforms are compared with each other and analyzed in the fifth chapter.

In the sixth chapter, an RCD snubber circuit is designed to mitigate the overshoot voltage of the boost converter's MOSFET during turn-off transition. RCD snubber circuit is a passive snubber circuit having less complexity and cost in comparison to active snubber circuits. Actually, snubber circuits are used to mitigate overshoots, but they cause some losses during transitions in reality. A diode is connected parallel to the RC snubber circuit to reduce these losses.

In the seventh chapter, a new analytical model is proposed by extracting from datasheet of the MOSFET for the CMOS buffer circuit given in the literature. This proposed model is used to observe the ringing of the capacitive input load of the driving MOSFET during the transition of the output of the driver stage from positive voltage level to the zero voltage level. Gate drive resistance, wiring parasitic of the PCB layout and the characteristic properties of the MOSFET are all taken into account in the analysis. Although some elements are neglected in the proposed analytical model, most efficient parameters are taken into account. The analytical model, simulation and implementation results are all compared with each other. With respect to this, proposed analytical model gives realistic approach to the circuit behavior.

In the eighth chapter, conclusions are made, the contributions of thesis are briefly summarized and recommendation for future works is given.

CHAPTER TWO
CHARACTERISTICS OF POWER ELECTRONIC DEVICES

2.1 Electrical Properties of Power Electronic Devices

The ratio of the electrical conductivity of the material is related to the free electron production capability. Power electronic devices are divided into four groups depending on the electric current conduction capacity; insulators, semiconductors, conductors and superconductors. If the energy gap between the conduction band and valence band is large, and electrons can not pass easily from valance band to the conduction band by the heat and radiation, is called insulator. An insulator requires a large amount of energy to move the electron from the valence band to the conduction band and obtain a small amount of current. If there is an almost overlap for the valence band with the conduction band, it is called conductor (Lutz, Schlangenotto, Scheuermann, & Doncker, 2011). In terms of electrical conductivity, semiconductors are between metals and insulators. Superconductors have zero resistance in only limited situations. They depend on the temperature, current and magnetic field. In high current and magnetic field, they do not behave as superconductor. Also, temperatures for superconductors vary approximately between 0.01 Kelvin (for tungsten) and 125 Kelvin (for ceramic superconductors) (Hummel, 2004). Due to these reasons, implementing superconductors is very difficult and using in power electronic circuits is almost impossible in recent conditions.

Electrical phenomenon occurs only in the outer orbital of the atoms. Observing the outer shell of the atoms is more important in determining how the atom reacts chemically and behaves as a conductor. Electrons are distinct on different energy levels and the highest level of electron filling within a band is called the Fermi energy level (Hummel, 2004). Classical free electron model (Drude model) explained that all free electrons would contribute to the current, but this model does not give any information about how many of the valance electrons can be considered to be free. Quantum theory explained the unanswered questions for the conduction process of the classical free electron model. Quantum theory is the jumping of the

energy levels of the electrons on the atom's orbits. With respect to the quantum theory; materials that possess partially filled electron bands are capable of conducting an electric current, electrons that are close to the Fermi energy collaborate in the electric conduction and the number of electrons near the Fermi energy depend on the density of available electron states (Hummel, 2004).

Power electronic devices can be grouped according to their similar properties by using Periodic Table. Materials of the atoms in a semiconductor can be from Group IV, or from Group III and Group V compounds, or Group II and Group VI Compounds. Group IV semiconductors are called elemental semiconductors and have diamond crystal structure. Great numbers of atoms are laid together and bond one to another to build up a crystal structure. This connection occurs by sharing of valance electrons in the outer orbital and it is called covalent bonding. Atoms in monocrystal structure forms diamond crystal structure as it is shown in Figure 2.1 (Lutz et al, 2011). Diamond crystal has two tetrahedral bonded atoms in each primitive cell, separated by 1/4 of the width of the unit cell in each dimension. Furthermore compound semiconductors have zinc blend structure or wurtzite structure.

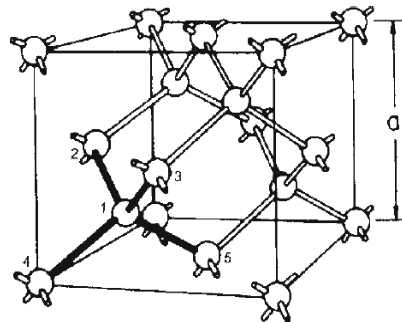


Figure 2.1 Scheme of the cubic unit cell of the diamond crystal structure (Lutz et al, 2011). 2-5 are the nearest neighbors of atom 1 and the tetrahedral bonding between them is shown.

Compared to normal electronic devices, power semiconductor devices require large voltages in the off state, high current capability in the on state and low leakage current, which demand geometry differences from the low-power devices. To satisfy these requirements, group IV silicon semiconductor structure or a group IV polytype, silicon carbide are used in production of the circuit elements after purifying from

other substances and reducing single crystal form (monocrystalline). In 1940s, Germanium was widely used in the production of the power devices. In 1950s, Germanium was replaced by Silicon. Germanium releases electron even at room temperature and this causes increment of the leakage currents. Conductivity of the germanium increases fairly by the temperature, and this material becomes behaving like a conductor. On the other hand, Si behaves as an insulator at room temperature. Operating temperature for Ge is lower than Si; band gap of Ge is only 0.67eV ($\approx 70^{\circ}C$) and Si is 1.1eV. For these reasons Si is chosen rather than Ge for the production of the diodes, transistors, thyristors and integrated devices. Gallium arsenide (GaAs) has a band gap of 1.4eV allows high switching frequencies and proper for microwave devices and suitable for high voltage schottky diodes (Lutz et al, 2011). Beside this, GaAs has some limitations over high voltages and large drive currents, in high frequency, and at high temperatures. To overcome these limitations SiC is used since, SiC materials have large energy band gap, can withstand a voltage gradient (or electric field) over eight times greater than Si and GaAs without undergoing avalanche breakdown, have high saturation electron velocity and are better thermal conductors (Takahashi, Yoshikawa, & Sandhu, 2007).

2.2 Diode's Characteristics

Ohl was invented p-n junction in 1940 to provide an improved light-sensitive electric device (Ohl, 1946) . The theory for the *p-n* junction diode was developed by William Shockley (1949). When an n-type region in a silicon crystal is adjacent to p-type region in the same crystal, p-n junction is occured. The p and n type semiconductor joined together at the vicinity of the junction surface. Density of the holes is much than density of the electrons and holes are the majority carriers in the p-region. On the other hand density of the electrons is much than density of the holes and so electrons are the majority carriers in the n-region. Some of the majority carriers diffuse toward the opposite side where their densities are low. The fixed acceptors stay behind without compensation, a negative space charge arises in the p-region and a positive space charge of uncompensated donors remains in the n-region

near the junction. After junction of the layers, donor atoms become positive ion and acceptor atoms become negative ion in the depletion region.

On the other side, pin diodes acts like p-n jnction diodes fundamentally. But, there are some specifications that differs each other. Pin diodes have three layers, highly doped P^+ region , highly doped N^+ region and very lowly doped intrinsic layer between them. Cross section of a basic pin diode is seen in Figure 2.2 .

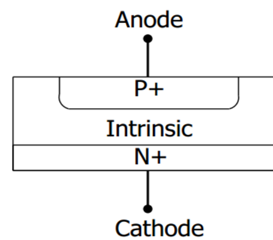


Figure 2.2 Cross section of a Pin diode. Depletion region gets wider and the capacitance of the diode is reduced due to the intrinsic layer.

Pin diodes are preferred in high power , RF switch and photodetector applications rather than p-n junction diodes, since they have larger breakdown voltages and higher conductivity when diode is forward biased. In pin diodes, the width of the depletion layer is higher and thus, the value of the capacitance of the diode is lower than p-n junction diode.

2.2.1 Soft and Snappy Recovery

If a forward biased diode is suddenly switched to reverse bias, the diode could not block the reverse bias instantly. The conduction will continue in the reverse direction for a short time due to the stored charge in the diode.

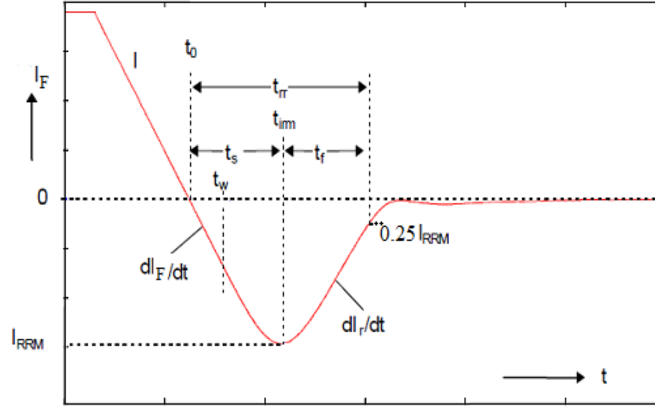


Figure 2.3 Reverse recovery current waveform (Dhariwal et al, 1992; Lauritzen, 1993)

I_{RRM} = the maximum reverse recovery current

t_0 = the moment of the current drop to zero

t_w = transition time from forward bias to the reverse bias

t_{irm} = the time that the reverse current is at its maximum value

t_s = the time between the zero crossing and the maximum reverse recovery current, storage time

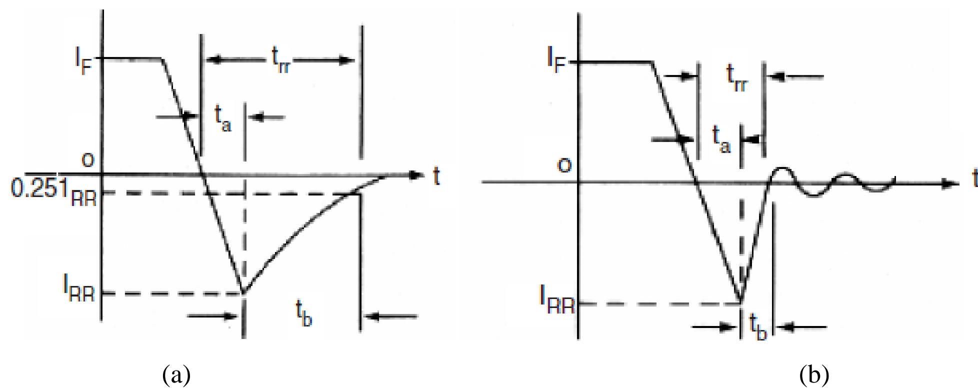
t_f = the time between the maximum reverse recovery current and 0.25 of the maximum reverse recovery current

The time interval between the moment of the current dropt to zero and the 25% (or 10%) of the maximum reverse recovery current is called reverse recovery time (t_{rr}). Figure 2.3 shows the reverse recovery current waveform of a diode (Ma & Lauritzen, 1993; Dhariwal et al., 1992; Wolley & Dell, 1988). For ideal diodes this time is equal to zero, but in practice this could not be zero.

$$S = \left| \frac{-\left.\frac{dI}{dt}\right|_{i=0}}{\left(\frac{dI_r}{dt}\right)_{\max}} \right| \tag{2.1}$$

The ratio of the derivative of forward current at the zero crossing and the derivative of the reverse current at the maximum value is called softness factor (S) as

given in Equation 2.6 (Lutz et al, 2011). Reverse recovery phenomena of the diodes are divided into two types depending on the softness factor. If the diode's softness factor is equal to or higher than 1 ($S \geq 1$), it is called a soft recovery diode. On the other hand, if the diode's softness factor is smaller than 1 ($S < 1$), it is called a fast recovery diode, snappy recovery diode or abrupt recovery diode. As it is seen in Figure 2.4, in soft recovery diode, reverse current decreases more slowly and smoothly before reaching its steady state value (Rashid, 2007). On the contrary in abrupt recovery diode, reverse current decreases very quickly and cross the zero axes and oscillations or ringing occurs. Abrupt recovery also results large reverse overvoltage and excessive Electromagnetic Interference.



(a) (b)

Figure 2.4. Recovery characteristics of diodes a) Soft recovery b) Abrupt recovery (Rashid, 2007)

When the slope of the reverse current is large and peak voltage increases to excessively high values, wide oscillations occur on the waveform, and it is called snap-off (Cova, Menozzi, Pasqualetti, Portesine, Scicolone, & Zerbinati, 1999). Once the diode has snapped-off, softness factor can not describe the diode's behavior and oscillations seen in the reverse recovery waveform become dangerous, and overvoltage across the diodes are destructive. This is an important parameter especially for higher voltages (>2000V) (Lutz et al., 2011).

2.3 Power Diode Models

Reverse recovery and forward recovery voltages, curents and times are the critical characteristic properties for power diodes.

During turn-on transition, anode to cathode voltage of a diode increases to a maximum forward recovery value (V_{FRM}) before the steady state forward voltage value. If the rising time of the triggering pulse is long, this voltage cannot be necessarily taken into account. But, when the switching time is fast, this voltage become an important issue and must be considered in the design stage. Although this value is an important issue for high speed transitions of the diode, manufacturer datasheets are generally do not give any value for this. The time between the 10% of the forward voltage and 1.1 of the steady state forward voltage is called turn-on time. A typical turn-on behavior of a power diode is shown in Figure 2.5 (Lutz et al, 2011).

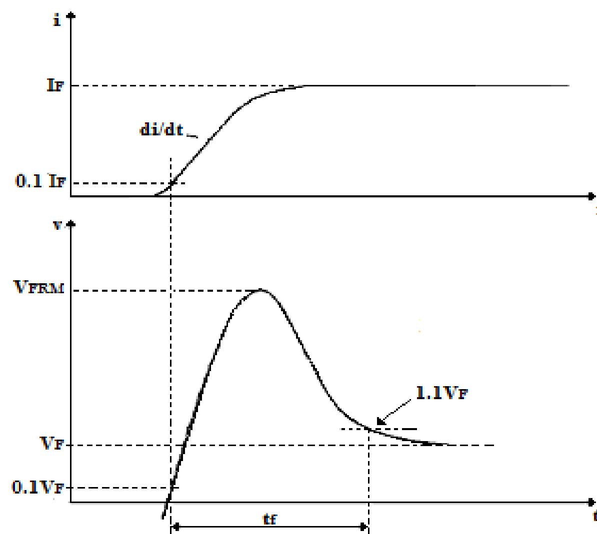
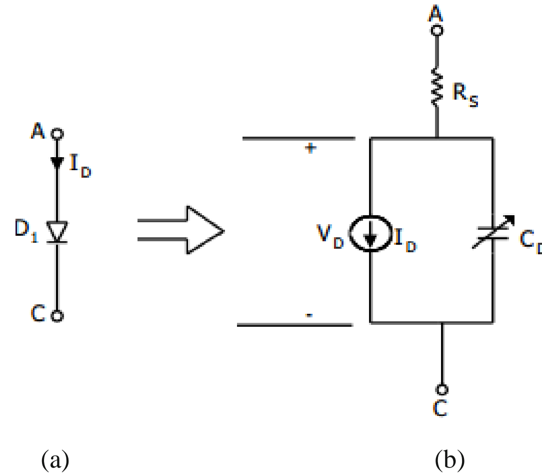


Figure 2.5 Turn-on behavior of a power diode (Lutz et al., 2011), here a current pulse with a limited di/dt is applied to diode in forward directions and then a forward recovery voltage waveform is obtained.

When a sufficiently large reverse bias voltage is applied to the diode, it conducts a very large reverse current and voltage cause destructions unless insufficient heat sink is used, this is considered to undergo avalanche breakdown. Peak inverse voltage (PIV) is the maximum voltage that can be applied to a diode not to cause breakdown in reverse biased condition (Baliga, 2008). Furthermore, when the temperature increases, the ionization rate will decrease and the breakdown voltage due to avalanche multiplication will increase (Ng, 2006).

2.3.1 SPICE Diode Model Parameters

A semiconductor diode can be modeled by using SPICE program. Static diode model for conventional SPICE with reverse biased is shown in Figure 2.6 (M. Rashid & H. Rashid, 2006). In this model diode current is represented by a current source. C_D is the junction capacitance of the diode and R_s is the parasitic ohmic resistance.



(a) (b)

Figure 2.6 Diode a) symbol b) SPICE model with reverse biased (M. Rashid & H. Rashid, 2006).

Parameter used in SPICE model of the diode is given in Table 2.1 (M. Rashid et al., 2006). If diode parameters are not specified, default values are taken into account. The reverse saturation current, emission coefficient and the ohmic resistance determine the DC characteristic of a diode. Reverse saturation current depends on the cross-sectional area and temperature, not the reverse voltage (Dorf, 1993). Transit time given in Table 2.1 is the ratio of the reverse recovery stored charge to the forward current of the diode as follow;

$$\tau_D = \frac{Q_{RR}}{I_F} \qquad (2.2)$$

Default value of the transit time is zero, but it can not be obtained zero in practical applications.

Table 2.1 Diode SPICE Parameters. Note that, "*" means the parameter is effected by the area

Symbol	Name	Area	Parameter	Units	Default	Example
I_S	IS	*	Saturation current	A	1E-14	1E-14
R_S	RS	*	Parasitic resistance (series resistance)	Ω	0	10
n	N		Emission coefficient, 1 to 2	-	1	1
τ_D	TT		Transit time	s	0	0.1ns
$C_D(0)$	CJO	*	Zero-bias junction capacitance	F	0	2pF
φ_0	VJ		Junction potential	V	1	0.6
m	M		Junction grading coefficient	-	0.5	0.5 (abrupt junction) 0.33 (linearly graded junction)
E_g	EG		Activation energy	eV	1.11	1.11(Si), 0.67(Ge), 0.69(Schottky)
p_i	XTI		IS temperature exponent	-	3.0	3.0 (pn junction), 2.0 (Schottky)
k_f	KF		Flicker noise coefficient	-	0	0
a_f	AF		Flicker noise exponent	-	1	1
FC	FC		Forward bias depletion capacitance coefficient	-	0.5	0.5
BV	BV		Reverse breakdown voltage	V	∞	50
IBV	IBV	*	Reverse breakdown current	A	1E-10	1E-3

Even though conventional SPICE diode model involves reverse biased condition and provides a basis for analysis, it does not reflect reverse recovery phenomenon and turn-on voltage spike associated with any diode in transient analysis exactly (Zhang & Pappas, 2001; Ma & Lauritzen, 1991; Ma & Lauritzen, 1993). In such a way that an abrupt recovery occurs during transition from on to off state and vice versa. Some models are proposed to overcome these transition problems for power diodes such as analytical, numerical, hybrid and empirical models. Brief information of these proposed models for power diodes are given in Appendix A (Tan & Tseng, 1999). Some more studies are given in the literature about the modeling of power diodes until today (Steadmn 1986; Zhang et al, 2001; Jones & Erickson, 2013). All these researches give insight into the modeling of a diode in high voltage high current applications. However, analyzing reverse and forward recovery phenomena, and solving the issues are not completed yet.

2.3.2 Reverse Recovery Simulations

In this part, a simplest buck converter circuit is simulated by using CST DESIGN STUDIO program to observe the diode reverse recovery and transit time characteristics. This program has very high accuracy and overshoots can be obtained in comparison to other SPICE programs. Circuit schematic is shown in Figure 2.7. IRF530 MOSFET is used as switching element. V_{pulse} is a square wave pulse voltage varied between 0 and 20 Volts is applied to the MOSFET to behave as a switching element. 2 Ω load resistor is used in the analyses.

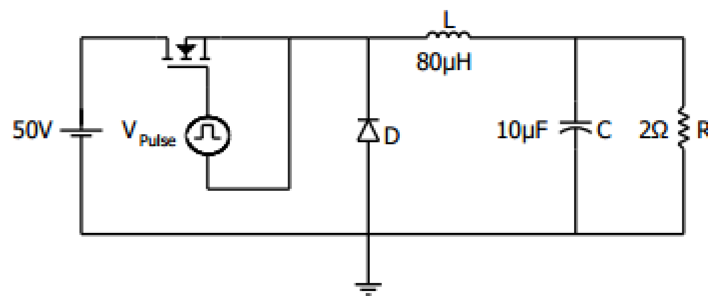


Figure 2.7 Schematic of the simulated buck converter

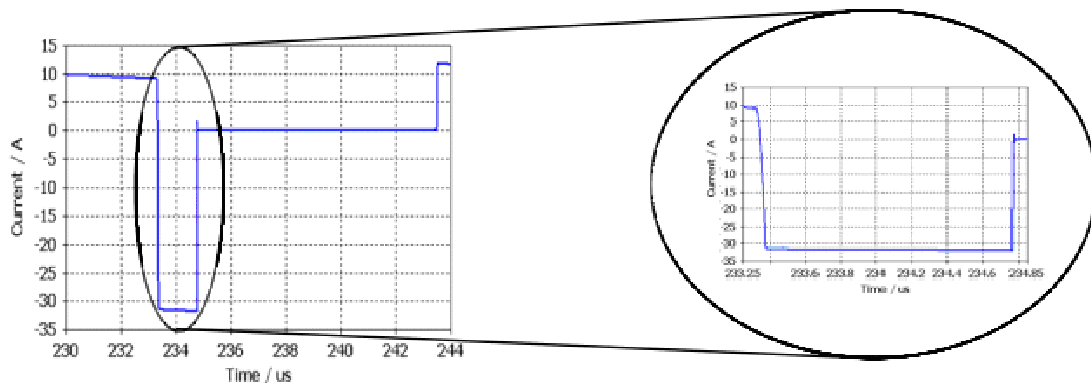
Ultrafast Soft Recovery Rectifiers (GI751, BYT28-300, UG10DCT) and schottky diode (MBR1660) are used in simulations and compared the waveforms with each other. The SPICE model libraries are taken from the manufacturer website and values are given in Table 2.2.

Table 2.2 SPICE parameters of the diodes used in simulations

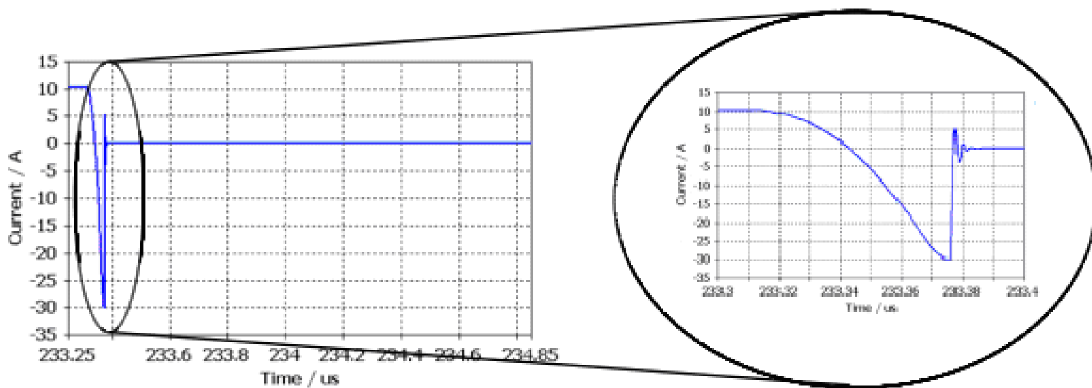
Symbol	**Name**	**Value**			
		GI751	**BYT28-300**	**UG10DCT**	**MBRF1660**
I_S	IS	3.5539E-011	5.94225E-006	8.13876E-08	4.94635E-07
R_S	RS	0.00202675	0.0126217	0.0244057	0.0119983
n	N	1.23	2.84843	1.72178	1.05695
τ_D	TT	6.16576E-006	7.76886E-008	3.32951E-08	1E-09
$C_D(0)$	CJO	2.574E-010	1.48242E-011	1.60575E-11	1.42758E-09
φ_0	VJ	0.7	3	2	1.49076
m	M	0.414814	0.33	0.1	0.581162
E_g	EG	1.79773	1.27681	1.21207	0.698901
p_i	XTI	3.57113	1.49785	1.2	3.84702
k_f	KF	0	0	0	0
a_f	AF	1	1	1	1
FC	FC	0.5	0.5	0.5	0.5
BV	BV	110	330	240	80
IBV	IBV	0.25	10	0.0001	0.0001

Period of the square wave pulse applied to the circuit is 10 μ seconds. Transit time that is defined in Equation 2.3 is an important parameter for reverse recovery characteristics of diode. The importance of the transit time arises because of the time required of the diffusion charge during biasing. Although GI751, BYT28-300, UG10DCT are all Ultrafast Soft Recovery Rectifiers, GI571 has highest transit time as shown in table 2.2.

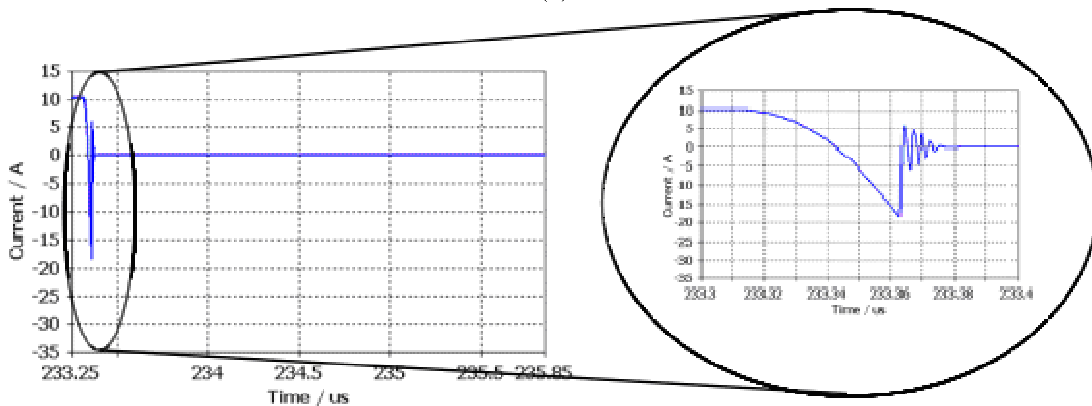
Reverse recovery current waveforms are shown in Figure 2.8. GI751 Ultrafast Soft Recovery Rectifiers has highest reverse recovery time. Transit time is directly proportional to the reverse recovery time when waveforms and transit time values are compared.



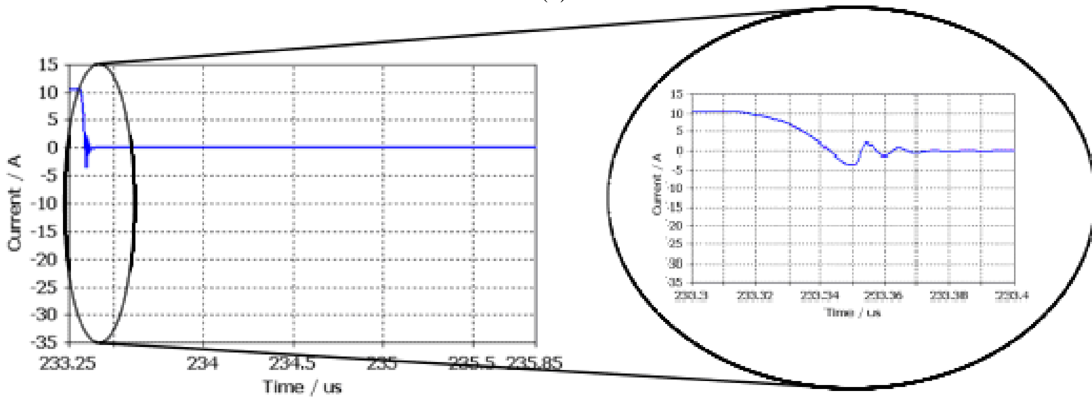
(a)



(b)



(c)



(d)

Figure 2.8 Diode current waveforms of a) GI571 b) BYT28-300 c) UG10DCT d) MBRF1660

Maximum reverse recovery current depends on the diode characteristics as well. Schottky diode has lowest reverse recovery current value in the same simulation conditions such as forward current, switching frequency and load values as seen in Table 2.3. The reason for this is the lack of the minority carrier storage and so fast switching of schottky diodes. Although no minority carriers, schottky diodes have little reverse recovery current since they have larger space charge capacitance.

Table 2.3 Diode peak reverse recovery currents obtained from simulations

Diode Name	**Peak reverse recovery current value**
GI571	-32 Ampere
BYT28-300	-30 Ampere
UG10DCT	-18 Ampere
MBRF1660	- 3 Ampere

Diode forward voltage is another critical parameter of the diode during transition. Voltage increases to the maximum forward recovery value and then decreases to the steady state forward voltage value when it turns on in actual fact. In simulation with conventional SPICE model this value can not be observed.

2.3.3 Forward and Reverse Recovery Calculations

Although reverse recovery phenomenon is one of the major sources of losses, calculating the exact reverse recovery time and reverse recovery losses is impossible, approximate calculations give an insight to understand the effects of the reverse recovery time (Kazimierczk, 2008). For a diode carrying forward current , when the minority carriers reach steady state, the excess stored charge is:

$$Q_F = \tau I_F \tag{2.3}$$

τ = Carrier life time

Carrier life time is the avarage time of the recombination of the minority carriers.

Reverse current jumps to a negative value and flows until all charge is removed. The equation of the reverse current is;

$$I_R = \frac{V_R - V_{ON}}{R} \tag{2.4}$$

Since the charge is conserved, the charge continuity equation describes the reverse recovery process of p^+n junction diodes during the storage time interval:

$$i_{total} = \frac{Q_p(t)}{\tau_p} + \frac{dQ_p(t)}{dt} + C_j \frac{dv}{dt} \tag{2.5}$$

$Q_p(t) =$ the excess minority hole charge stored in the n-bulk region adjacent to the depletion region edge

τ_p = the mean hole lifetime in the n-region

C_j =junction capacitance

The junction capacitance in the above equation can be ignored, since it is much smaller than the difussion capacitance. Then, the equation becomes;

$$I_R = \frac{V_R - V_{ON}}{R} = \frac{Q_p(t)}{\tau_p} + \frac{dQ_p(t)}{dt} \tag{2.6}$$

The charge initial value is equal to $Q_p(0) = \tau_p I_F$ since that the excess charge waveform has reached the steady-state value before the turn-off transition is assumed. The Laplace of the above equation is ;

$$Q_p(s) = \frac{\tau_p I_F}{s + \frac{1}{\tau_p}} + \frac{I_R}{s^2 + \frac{s}{\tau_p}} \tag{2.7}$$

And in the time domain, equation becomes;

$$Q_P(t) = \tau_p I_F e^{-\frac{1}{\tau_p}} + \tau_p I_R (1 - e^{-\frac{1}{\tau_p}}) \quad (2.8)$$

Since $Q_p(t_s) = 0$, the storage time is;

$$t_s = -\tau_p \ln(\frac{I_R}{I_R - I_F}) = -\tau_p \ln(1 - \frac{I_R}{I_F}) \quad (2.9)$$

It is seen from the above equation that when $\frac{I_R}{I_F}$ decreases , the storage time decreases too (Kazimierczuk, 2008).

Some assumpstions are made for the calculations of the reverse recovery current waveforms of the figure given in Figure 2.7, such as slopes of the forward current and reverse current are linear , thus softness factor is equal to t_f / t_s . Due to this reason , the exact numerical value for the reverse recovery current of a diode can not be calculated, but the calculations show the way to maintain an opinion (Kazimierczuk, 2008; Rashid, 2007; Mohan, Undeland & Robbins, 1995). The storage charge (Q_{RR}) can be calculated from the area enclosed by the path of the recovery current, and aproximately equal to ;

$$Q_{RR} \approx \frac{1}{2} I_{RRM} t_{rr} \quad (2.10)$$

Storage time can be written as;

$$t_s = t_{rr} - t_f = \frac{t_{rr}}{S+1} \quad (2.11)$$

Maximum reverse recovery current value is ;

$$I_{RRM} = \frac{dI_F}{d_t} t_s = \frac{dI_F}{d_t} \frac{t_{rr}}{S+1} \quad (2.12)$$

And when Equation (2.9) is used in Equation (2.11), maximum reverse recovery current is obtained;

$$I_{RRM} = \sqrt{\frac{2Q_{rr}(\frac{dI_F}{dt})}{(S+1)}} \tag{2.13}$$

And reverse recovery time is found ;

$$t_{rr} = \sqrt{\frac{2Q_{rr}(S+1)}{(\frac{dI_F}{dt})}} \tag{2.14}$$

Equations indicate that the slope of the forward current is important for the reverse recovery current. This is because of the storage charges that depends on the forward current of the diode. Also reverse recovery time, which is a critical parameter for the switching depends on the storage charges, diode junction temperature, forward current just before the reverse biased condition and rate of the fall of the forward current.

2.4 Evaluating Some of the MOSFET Switching Parameters by Implementing of a Boost Converter

A basic boost converter is implemented to observe its current and voltage spikes if any. The realized circuit schematic is shown in Figure 2.9. In the circuit, IRF510 N-Channel Power MOSFET is used as a switching element. Driver circuit for the MOSFET of the prototype is selected a fast discrete driver found in the literature (Kazimierczuk, 1988). The operating frequency of the circuit is selected as around 120 kHz. In the practical circuit, as a diode BA157 (Fast Recovery Diode), BYW29-200 (Ultrafast Rectifier), MBR745 (Schottky Rectifier) are utilized in the power stage of the circuit each time and the results are compared.

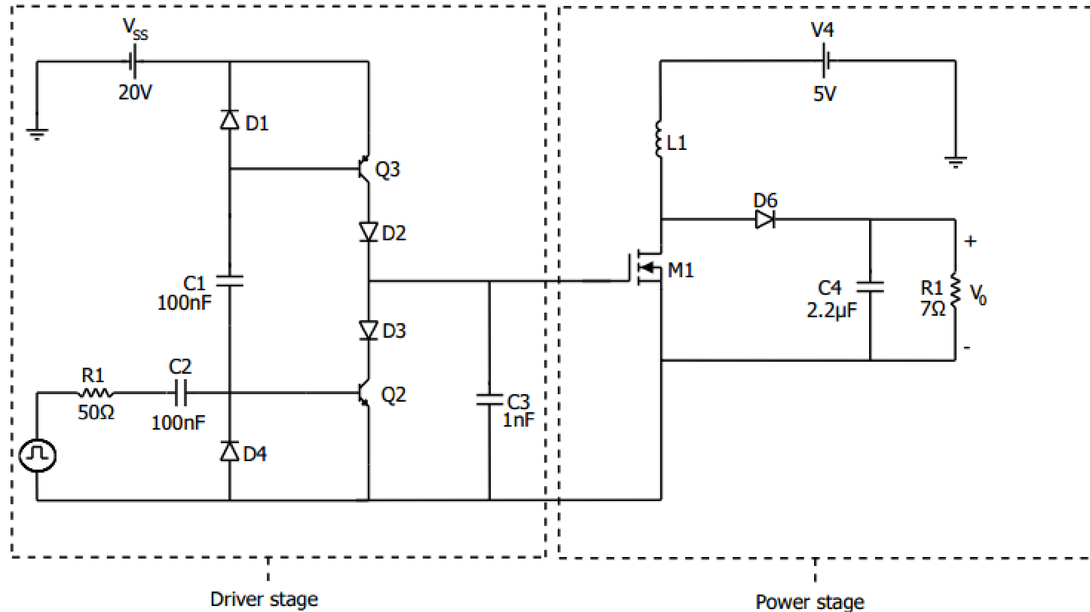


Figure 2.9 Circuit schematic of the implemented basic boost converter circuit. Note that, capacitor C3 is a part of driver circuit

The circuit schematic is composed of two stages, driver and power stages. A fast driver stage is used for driving the MOSFET to commutate it rapidly. 2N2222 NPN transistor (Q2), Q2N2905 PNP transistor (Q3) and 1N4148 diodes (D1, D2, D3, D4) are used in the driver stage.

2.4.1 Operating Principle of the Driver Circuit

Driver stage of the circuit proposed by Kazimierczuk (1988) is used in Figure 2.9 as driver block. Obtaining a high speed switching is difficult because of the time required to establish voltage changes across input capacitances of the MOSFET is longer than the calculations. Due to the charging and discharging of the input capacitances turn-on delay and turn-off delay times are occurred.

When the source voltage goes to high, the MOSFET behaves like a closed switch but MOSFET voltage does not reduce exactly to zero due to its channel ON-resistance (R_{DS_on}) value. This resistance value is varied with different MOSFET characteristics. In this region PNP transistor (Q3) is in the cut off region and NPN transistor (Q2) is in the active region until the output voltage is decreased to the collector emitter saturation voltage. The output current is equal to the collector

current of the Q2 transistor, since the capacitance at the output is discharged by this collector current.

$$I_0 = -I_{CQ_2} = C_3 \frac{dV_0}{dt} \tag{2.15}$$

The boundary condition of the output voltage of the driver stage is equal to the ($V_o(0) = V_{ss} - V_{CES}$), where V_{CES} is the collector-emitter saturation voltage. Then it is obtained as;

$$V_o = -\frac{I_{CQ_2}}{C_3} t + V_{ss} - V_{CES} \tag{2.16}$$

When the source voltage goes to low, the MOSFET behaves like an open switch. In this region Q2 is in the cut off region and Q3 is in the active region. The output current is equal to the collector current of the Q3, since the capacitance at the output is charged by this collector current.

$$I_0 = I_{CQ_3} = C_3 \frac{dV_0}{dt} \tag{2.17}$$

When the boundary condition of the output voltage ($V_o(transition) = V_{CES}$) is used for solving the Equation (2.17). Output of the driver stage is as follow;

$$V_o = \frac{I_{CQ_3}}{C_3} t + V_{CES} \tag{2.18}$$

Detailed analysis of the driver stage is given in reference (Kazimierczuk, 1988).

2.4.2 Power Stage

As known, average value of the output voltage of a boost converter is always higher than supply voltage. When the MOSFET is in the on state, diode turns off and current flows through the power supply, inductance and MOSFET. Inductance is charged at this interval and output capacitor is discharged through the load. When MOSFET turns off, load is energized through the diode. Ideally, these transitions are occurred at the same time, but in practice the turn-off recovery and turn-on recovery phenomena of all types of diodes should be taken into account.

2.4.3 Failure of the Driver Circuit

During the experimental work with the circuit proposed by Kazimierczuk (1988) an important problem of the circuit is recognized. This problem is indicated in the paper as current hogging (Kazimierczuk, 1988). The leakage current may occur in one of the transistor, while the other one is in conduction, this cause a decrease in the output current. Although D2 and D3 diodes are used to minimize the decrease in leakage current and it is given as notably improved in the paper, problem appears as failures of transistors Q2 or Q3 and sometimes both. The problem occurs when the circuit is just energized namely V_{SS} supply voltage is connected to the circuit. Both analytical and simulation works show that at start-up capacitor charges to voltage around to V_{SS} through base-emitter junctions of both Q2 and Q3. During this transient interval both transistors Q2 and Q3 carry shoot through currents and DC supply V_{SS} is nearly short circuited through these transistors. This current flows through the Q3 transistor, C1 capacitor and Q2 transistor as shown in Figure 2.10.a. Collector (also base) currents of these transistors are limited only by parasitics (especially connection inductance parasitic) of the circuit. Model of the transient driving current flow is shown in Figure 2.10.b. The value of the shoot through current at start up exceeds the absolute maximum ratings which are given in datasheets of the transistors. Due to this reason, the transistors could not pass this current value reliably and may be damaged as soon as the driver circuit is energized by turning on the V_{SS} source.

At start up (when capacitor C1 has no charge) transistors Q2 and Q3 behave as short circuit and a huge shoot through current (I_{st}) flows until V_{C1} charges to a voltage approximately to V_{SS}. Due to our experiments whether the pulse generator is previously connected to circuit or not, it does not change the problem nature. In these circuits, C1 capacitor should not be too much to overcome this failure. Actually this phenomenon is not dealt a lot with in indexed of scientific literature but it may be a crucial failure for the circuits. In Figure 2.10.b model of the transient driving current flow is seen. In addition to this, transient drive current path of Q3 and Q2 at start up is seen in Figure 2.10.c.

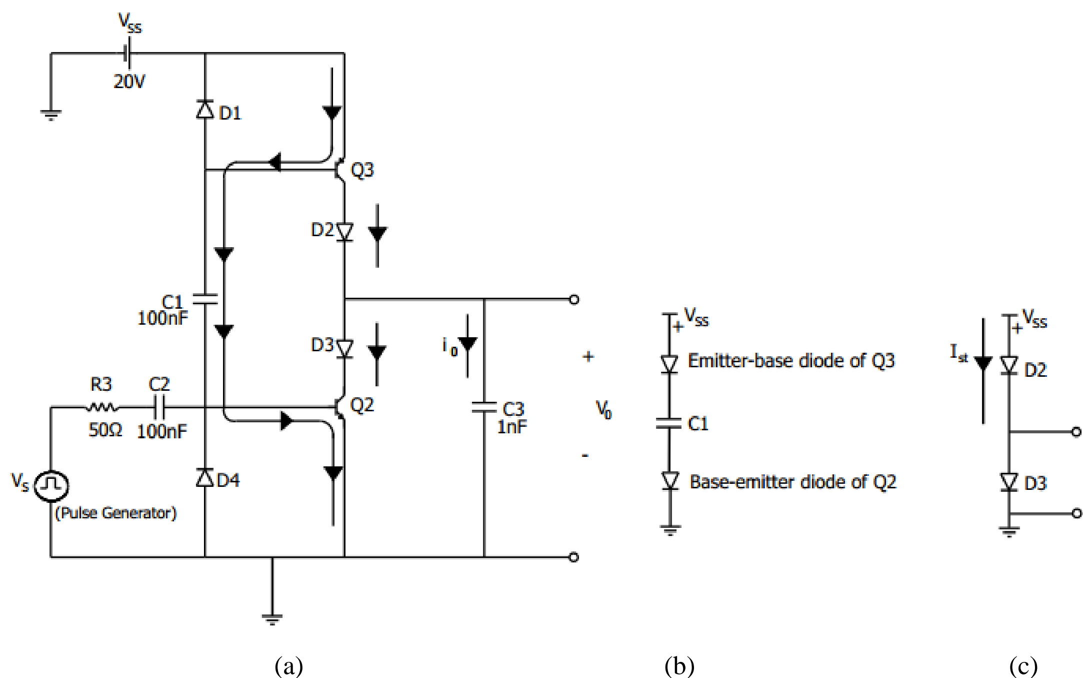


Figure 2.10 a) Current flowing path during the start-up of the driver circuit (V_{ss} is turning on) b) Model of the transient driving current flow c) Transient drive current path of Q3 and Q2 at start up

The simulation result of the emitter current of the Q3 is shown in Figure 2.11. The supply voltage is triggered; a huge current approximately 12.4 Ampere is occurred in the emitter node of the Q3. This current flows through the collector terminals of both BJTs, and this current value can causes failures and damages in the transistors.

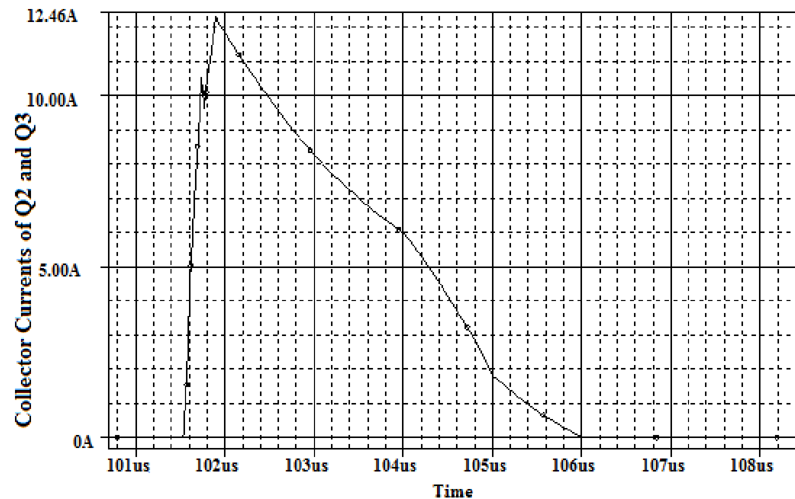
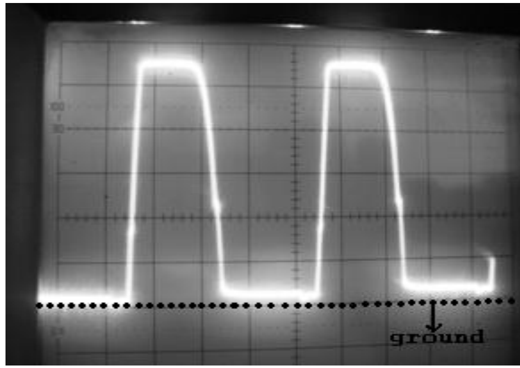


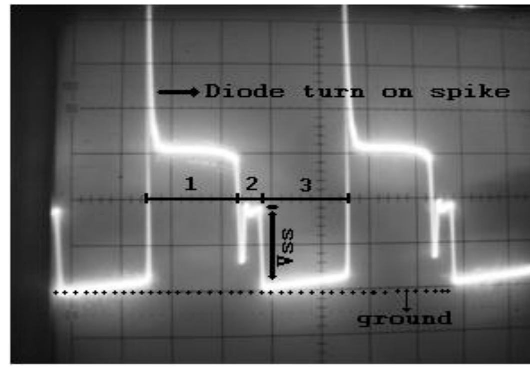
Figure 2.11 Collector Currents of Q2 and Q3 of Figure 2.10 Simulation Results when just at V_{SS} supply voltage is connected to circuit, pulse input of the circuit is shorted to ground. Note that nearly the same currents flow both transistors.

In the figure above V_{SS} is connected to the circuit at t=101.5 μs. And, huge current occurs right after the connection of the supply voltage.

2.4.4 Dynamical Behavior Effects of Diode Parameters on Transient Waveforms

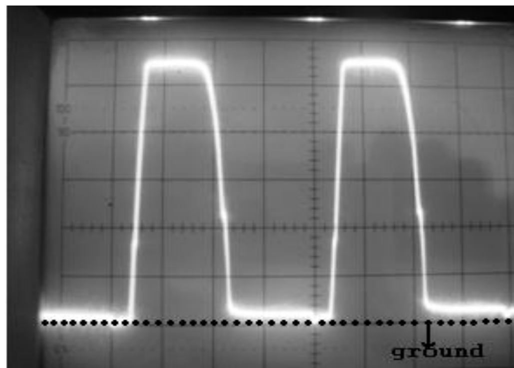
There are some physical limitations of a diode fabrication and design techniques. These limitations have an influence on the turn-on spikes and reverse recovery current. Fast, ultra fast and Schottky diodes are used in comparison with reverse recovery times to investigate the turn-on spikes and reverse recovery times of these diodes. Gate voltages of MOSFET and anode to ground voltages of the diodes are shown in Figures 2.12, 2.13 and 2.14. When diode is in turn-on duration, BA157 fast recovery diode's overshoot voltage is fairly high compared with BYV08 and MBR745. When we look into results for MBR745 Schottky diode, it is seen that the decrease in overshoot voltage is in a quite important level and it approaches the desired results.

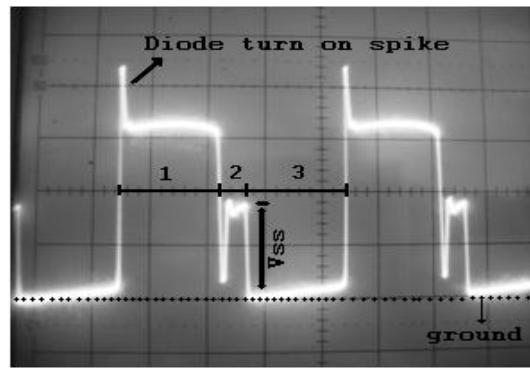




(a) (b)

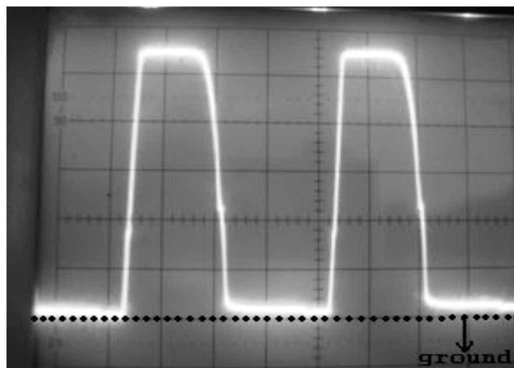
Figure 2.12 Waveforms associated to Boost Converter implemented with BA157 fast recovery diode a) MOSFET gate-source driving voltage waveform b) anode voltage (referenced to ground) waveform, 2 volt/div, 2 µs time/div.

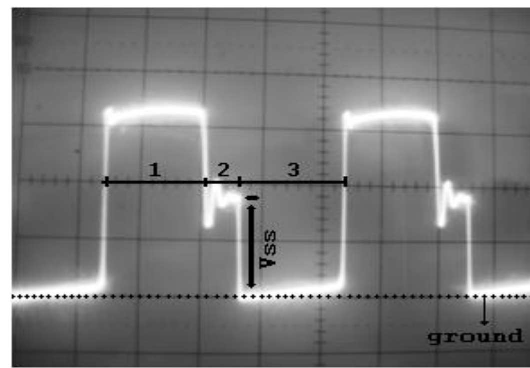




(a) (b)

Figure 2.13 Waveforms associated to Boost Converter implemented with BYV08 ultra fast recovery a) MOSFET gate-source driving voltage waveform b) Anode voltage (referenced to ground) waveform, 2 volt/div, 2 µs time/div.



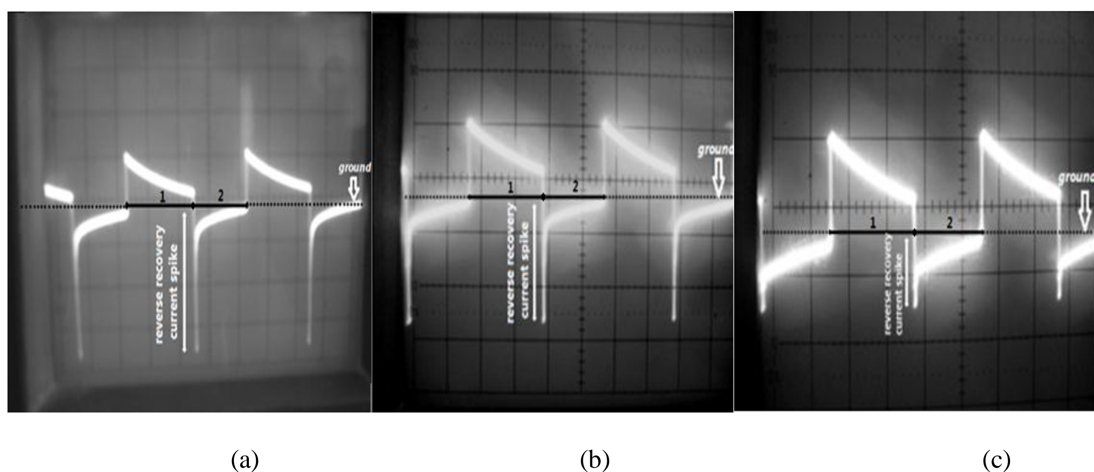


(a) (b)

Figure 2.14 Waveforms associated to Boost Converter implemented with MBR745 schottky diode a) MOSFET gate voltage waveform b) Anode voltage (referenced to ground) waveform, 2 volt/div, 2 µs time/div. Note that diode turn-on spike occurs hardly ever.

There are three intervals in Figures 2.12.b, 2.13.b and 2.14.b. In the first interval MOSFET is at its OFF state and diode is ON state. Diode was OFF state before the first interval. Diode turns on at the beginning of the first interval and current becomes to flow through the diode. The time required to turn-on is called forward recovery time. The dynamic resistance of the diode should be considered in determining the forward recovery time. It has an inductive effect at the instant of the diode to become ON. There is a voltage spike in this interval and it has higher value in fast recovery diode as seen in Figure 2.12.b. In the second interval, both MOSFET and diode is OFF state. The inductor current decreases to zero level at the beginning of this interval, no current flows through the inductor during this interval. Hence diode anode voltage is equal to V_{SS} of converter input supply voltage during this interval. In the third interval MOSFET is in ON state and diode is in OFF state, anode voltage of the diode is equal to approximately zero level.

The turn-on spike in the waveform of MOSFET with MBR745 schottky diode of Figure 2.14.b is too small and this shows that parasitic inductance does not effect all measured results very much in current set up in this circuit configuration, otherwise a voltage spike should be observed as seen in the Figures 2.12.b and 2.13.b due to the stray inductance of MOSFET drain connection.



(a) (b) (c)

Figure 2.15 Reverse recovery current waveform for the diodes are measured via a current probe with 1 mA/mV scaling factor, 0, 2 volt/div a) Current waveform of the diode for the BA157 fast diode b) Current waveform of the diode for the BYV08 ultra fast diode c) Current waveform of the diode for the MBR745 Schottky diode

Reverse recovery waveforms of diodes are shown in Figure 2.15. The MOSFET is in OFF state and diode is in ON state in the first interval of Figure 2.15. In the second interval, MOSFET is in ON state and diode is in OFF state. During the transition of the diode from ON state to the OFF state, reverse recovery current spike occurs because of the reverse recovery time of the diode. The magnitude of the reverse recovery time is the result of the charge distribution of the diode. The reverse recovery time for BA157 diode is 0.4 μs, for BYV08 diode is 0.35 μs and for MBR745 is 0.2 μs. If the Figure 2.15 is investigated, it is observed that the reverse recovery current spike is changed allied with the diode. The reverse recovery current spike value for BA157 fast diode is equal to the 750 mA, for BYV08 the value is 540 mA. For MBR745 schottky diode which has lowest reverse recovery time, it is seen that the decrease in current spike is in a quite important level and is equal to the 300 mA.

The experimental results show that the diode reverse current spikes (caused by diode reverse recovery phenomenon) and voltage spikes (caused by diode forward recovery) that may appear in switching converter waveforms must be taken into account during the semiconductor switch selection process in design phase.

2.4.5 Selection of the Inductance Value

In the implementation of the boost converter circuit of Figure 2.9, both with low and high inductance values of the converter are used. When low valued inductance is selected (inductor 1) and MOSFET enters cut off region, voltage does not go to zero directly. In Figure 2.16, input voltage is seen in diode's anode for a short time, since no current passes through the coil L1 of Figure 2.9 during this time. Then, coil's current starts to increase and diode's anode voltage decreases to approximately zero value. Since current probe is a current transformer based probe it can not reflect actual current waveform but it shows erroneously in both negative and positive directions current flows. Also note that since waveform seen in Figure 2.16 is for discontinuous current mode of converter, no reverse recovery current spike occurs as expected.

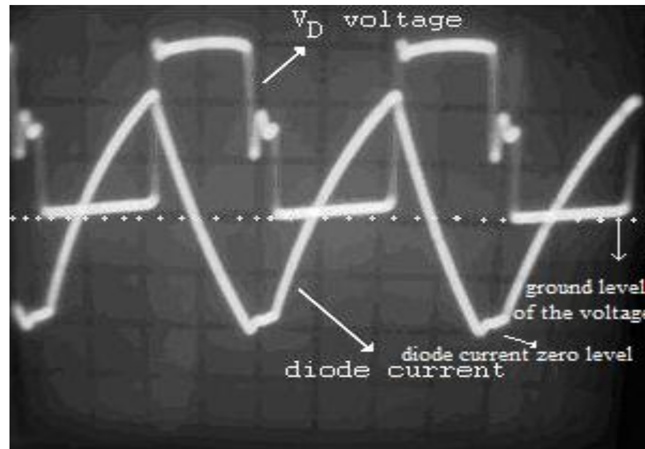


Figure 2.16 Current waveform of the inductor 1 value measured by current probe 1 mA/mV, 0.2 volt/div and diode anode voltage 2 volt/div. Note that diode reverse recovery tails disappeared.

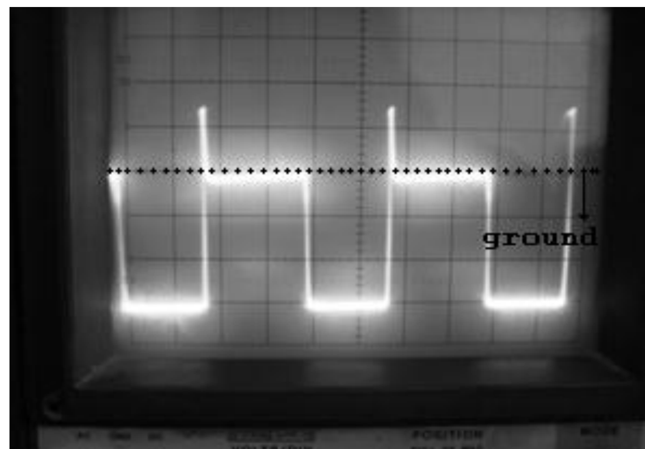
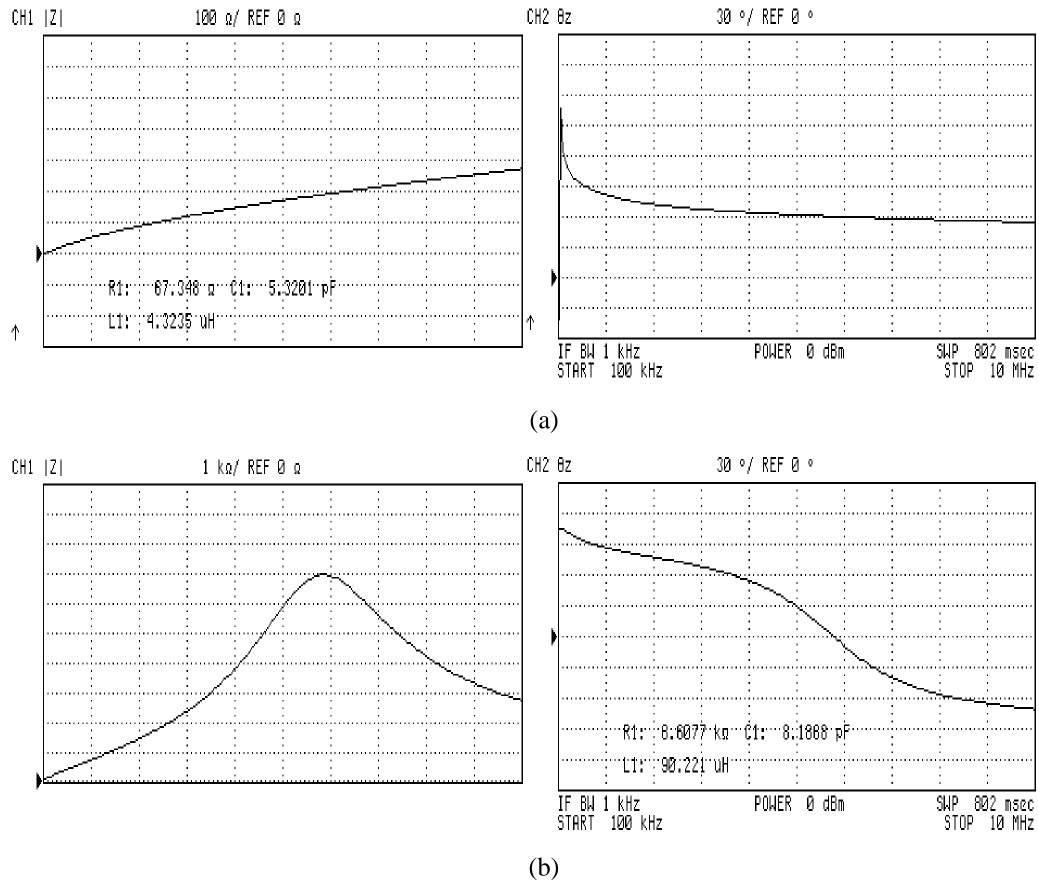


Figure 2.17 Diode anode voltage waveform when high inductance value (inductor 2) is used.

Inductor 1 is measured 4.3 μH and Inductor 2 is measured 90.2 μH. For the converter including inductor 2 rather than inductor 1, inductor current does not fall to zero value during the MOSFET OFF interval (converter's continuous current work) and interval 2 of Figure 2.14.b disappears. In Figure 2.17, it is seen that V_D voltage stays at the V_O output voltage throughout the MOSFET off period due to continuous current working scheme of the converter. Coil current is decreased during diode's forward biased condition, and increased during diode's reverse biased condition.

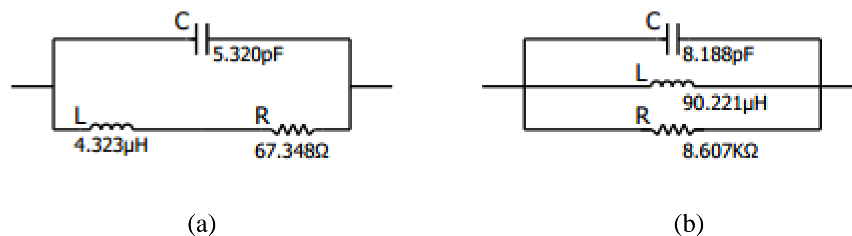


(a)

(b)

Figure 2.18 a) Measurement results of inductor 1 b) Measurement results of inductor 2

Network analyzer measurement results of the inductors used in the converter are given in Figure 2.18. The graphs shown in Figure 2.18 are taken in the frequency band of 100 kHz (lower limit of Agilent 4395A Network Analyzer) and 10 MHz. The graphs also indicate that inductor 1 (low valued inductance) performed nearly ideal inductor in the measurement band on the other hand inductor 2 (high valued inductance) exhibit parallel resonance behavior at about 6 MHz frequency.



(a) (b)

Figure 2.19 Equivalent circuit parameters for a) inductor 1 b) inductor 2

The measurement results give the equivalent circuit parameter values of the inductors shown in Figure 2.19. In addition to this parameter values, the measurement results also show the inductors impedance magnitude value and phase of the impedance versus frequency.

It is practically seen that the inductor value is an important parameter for determining the continuous or discontinuous mode of the converter for a constant load in a boost converter circuit.

CHAPTER THREE
POWER MOSFET'S AS SEMICONDUCTOR SWITCHES AND THEIR DRIVING CONSIDERATIONS

In this chapter, MOSFET internal elements and their effects to switching circuits are throughly discussed. Basic switching circuits with resistive and inductive load's gate drain voltage, gate current and drain voltage are investigated by simulating with SPICE. Analytical calculation during transition of the MOSFET is given for the inductive load when the parasitic elements are neglected. Another important parameter occurring due to the transition is the reverse recovery time of the diode. The effect of the long reverse recovery time of the diode in the switching converter is searched for the inductive load circuit as well. Waveforms are compared for the cases of usages of pin diodes or schottky diodes.

3.1 MOSFET Characteristics

Power MOSFETs are preferred as switching elements in high frequencies, since they operate mainly as majority carrier devices. They do not have storage time phenomenon oppose to bipolar transistors. Due to the voltage controlled property of the MOSFET, no gate current flows except during the transitions from on to off or off to on when the gate capacitance is being charged or discharged.

Even though power MOSFETs have benefits for obtaining high efficiency in high frequencies, some characteristic properties of the MOSFETs and issues caused by these properties must be eliminated during switching. Major MOSFET characteristic factors that affect the turn-on and turn-off times are the three interelectrode capacitances those are gate-drain capacitance (C_{GD}), gate-source capacitance (C_{GS}) and drain-source capacitance (C_{DS}) , the inductances of the drain lead (L_D) and source lead (L_S), the (distributed) resistance of the polycrystalline silicon gate (R_G) and MOSFET body diode as seen in Figure 3.1 (Grand & Gowar, 1989).

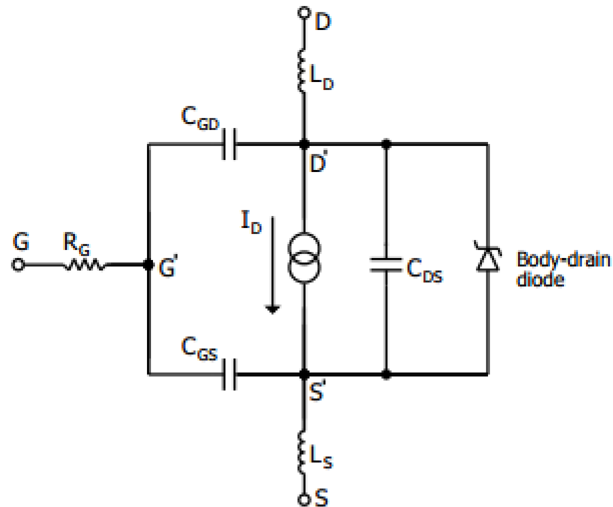


Figure 3.1 Model of a MOSFET with lumped elements (Grand & Gowar, 1989)

MOSFET intrinsic capacitances do not affect the circuit so much in low frequencies. On the other hand, when the frequency gets in higher level, the effect of them are the dominating factor for the analysis of switching time. Due to the switching in high frequency, drain source voltage of the MOSFET swings between zero and high voltage level. Effective value of the gate drain capacitance become much larger than expected, depending on the swing of the drain source voltage of the MOSFET; since gate drain capacitance is a non-linear capacitance and function of the voltage affect its dynamic value.

Beside the intrinsic capacitances, inductances of the drain and source leads of the MOSFET effect the frequency and magnitude of the ringings in high frequency switching. Another parasitic element is the gate resistance (R_G). Gate resistance allied with gate-source capacitance affects the turn-on delay time and the charge and discharge times of the gate-source and gate-drain capacitances of the MOSFET. Due to these switching times, switching losses and gate drive losses increase or decrease. Rising of the losses causes an increment in temperature of the MOSFET and driver, they may cause the circuit damage too.

3.2 The MOSFET Switching Test Circuit for the Resistive Load Case

3.2.1 Derivation of Miller Effect

Increment in the gate drain capacitance effect of the MOSFET is called "Miller Effect" (Laker & Sansen, 1994; Howe & Sodini, 1997). This increment is not in the physical manner. Miller Effect was first introduced by John M. Miller and studied in an electronic amplification device with three active electrodes called vacuum tube triode amplifier (Miller, 1919).

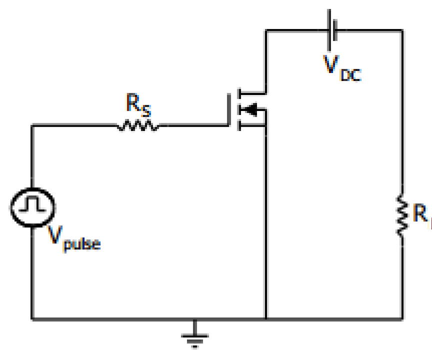


Figure 3.2 Common source switching circuit with resistive load for studying Miller Effect

Miller theorem is a useful, simplified circuit analyses method, since analyzing the high frequency effects of an amplifier circuit is complex due to the capacitor connected between input and output nodes. While using this theorem, parasitics caused by the MOSFET and PCB layout are neglected. Even though there are not completely exact results, neglecting these parasitics create an aspect to observe the effect of internal capacitances in the linear region. The basic circuit schematic of a common source switching circuit with resistive load is seen in Figure 3.2.

Small signal equivalent circuit of the switching circuit is seen in Figure 3.3.a. This circuit is calculated by Miller approximation method. In Figure 3.3.b, equivalent circuit using the Miller approximation method is seen (Laker & Sansen, 1994; Howe & Sodini, 1997). During the on-off or off-on transition of a semiconductor power switch such as a MOSFET; there is a small time interval in which the switch behaves as an active element of a linear circuit. This circuit in fact works as an amplifier circuit and Miller Theorem could be used to get a viewpoint about operation of a

switch in these intervals. The expressions for the capacitances of the MOSFET model given in Figure 3.1 are:

$$C_{iss} = C_{GS} + C_{GD}$$

$$C_{oss} = C_{DS} + C_{GD}$$

$$C_{rss} = C_{GD}$$

C_{iss} = input capacitance of the gate terminal when drain and source terminals are shorted

C_{oss} = output capacitance of the gate terminal when gate and source terminals are shorted

C_{rss} = reverse transfer capacitance

C_{iss}, C_{oss} and C_{rss} capacitances are used as reference point for choosing the other components' values of the circuits.

Charging and discharging of the C_{GD} and C_{GS} capacitances plays an important role during switching because of the "Miller Effect" (Grand et al, 1989; Vithayathi, 1995; Rashid, 2007). To prove the Miller Effect, common source amplifier gain should be calculated. Kirchoff's Current Law is applied to both input and output node of the equivalent circuit seen in Figure 3.2.

$$I_{input} = \frac{V_{GS}}{\frac{1}{jwC_{GS}}} + \frac{V_{GS} - V_{DS}}{\frac{1}{jwC_{GD}}} = V_{GS}\,jwC_{GS} + jwC_{GD}(V_{GS} - V_{DS}) \tag{3.1}$$

$$(V_{GS} - V_{DS})\,jwC_{GD} - g_{fs}V_{GS} + \frac{V_{DS}}{Z} = 0 \tag{3.2}$$

Drain current in active region is equal to;

$$I_d = g_{fs}V_{GS} \tag{3.3}$$

g_{fs} is the slope of the i_d versus V_{GS} curve of the power MOSFET and calculated:

$$g_{fs} = \frac{(di_D/dV_{GS})}{I_d} \quad (3.4)$$

When combine both equations, the input current becomes;

$$I_{input} = jwV_{GS}\left[C_{GS} + C_{GD}\left[\frac{1+g_{fs}Z}{1+jwZC_{GD}}\right]\right] \quad (3.5)$$

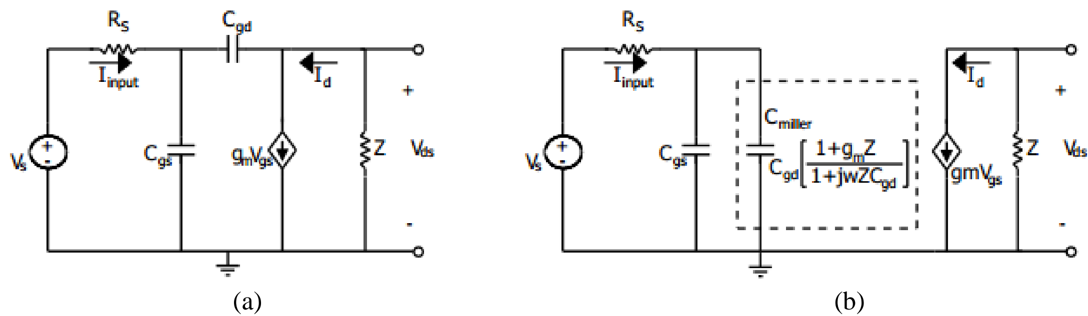
Current gain of the circuit is;

$$\frac{I_d}{I_{input}} = \frac{g_{fs}V_{GS}}{jwV_{gs}\left[C_{GS} + C_{GD}\left[\frac{1+g_{fs}Z}{1+jwZC_{GD}}\right]\right]} \quad (3.6)$$

Note that these expressions are valid for incremental conditions, in transition intervals and while neglecting the drain and source and layout parasitic inductances.

The total impedance seen from input is the sum of the gate-source capacitance and gate-drain capacitance with Miller Effect as seen in the input current Equation (3.4). Therefore, miller capacitance is;

$$C_{miller} = C_{GD}\left[\frac{1+g_{fs}Z}{1+jwZC_{GD}}\right] \quad (3.7)$$



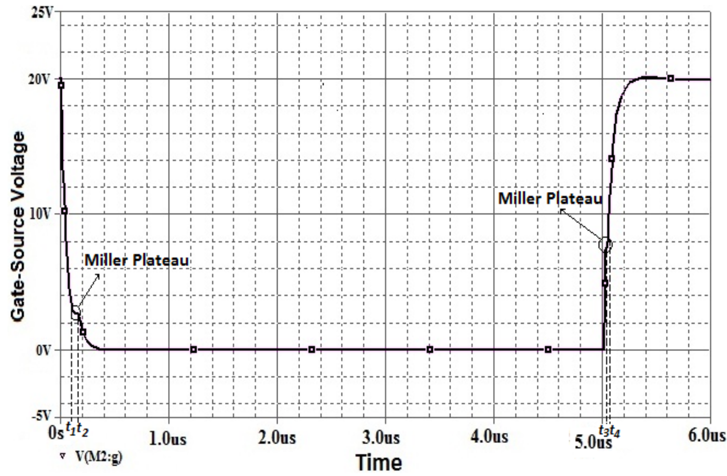
(a) (b)

Figure 3.3 a) Small signal equivalent circuit of the circuit seen in Figure 3.2 at switching instant b) Small signal equivalent circuit of the common source amplifier circuit using Miller approximation (Laker & Sansen, 1994; Howe & Sodini, 1997).

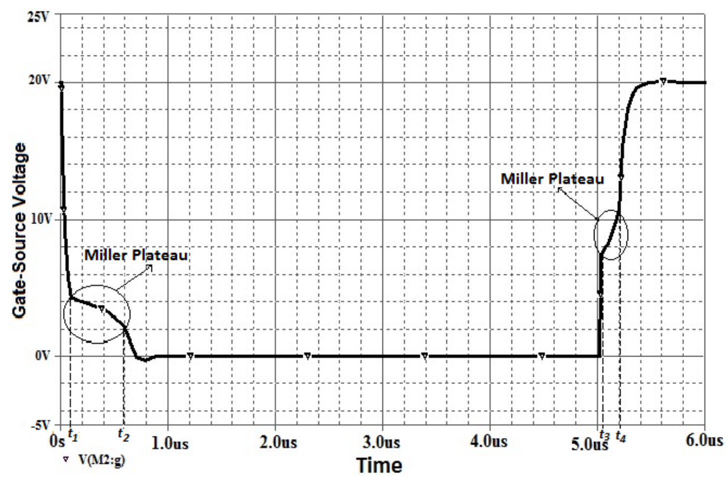
Value of the miller capacitance that indicates the time spent in the Miller plateau is crucial in switching losses of the MOSFET. With the increment in the capacitor effective value, voltage across the capacitor is forced to be high and this high voltage causes an increment in the current flowing through the capacitor as well. The C_{GD} and C_{DS} internal capacitances are highly nonlinear and exponential whereas C_{GS} capacitance is approximately linear (Kazimierczuk, 2008).

3.2.2 Simulation Work of the Switching Test Circuit with a Resistive Load

Drain source voltage is an effective parameter in the occurrence of the Miller Effect. With respect to this, a switching test circuit given in Figure 3.2 with 20 Volts and 200 Volts DC supply voltage is simulated by PSPICE. Since drain source inductance and wiring parasitics are neglected, the source is considered at almost ground potential and the body diode effect is neglected. In this part, voltages and currents of the gate-source and drain-source terminals with defined supply voltages are simulated and the waveforms are compared. Miller plateau is an interval where the gate-source voltage is constant due to the miller effect. Miller plateaus for both defined DC supply voltages are especially emphasized. Pulse signal applied to the MOSFET is 20 Volt square wave.



(a)

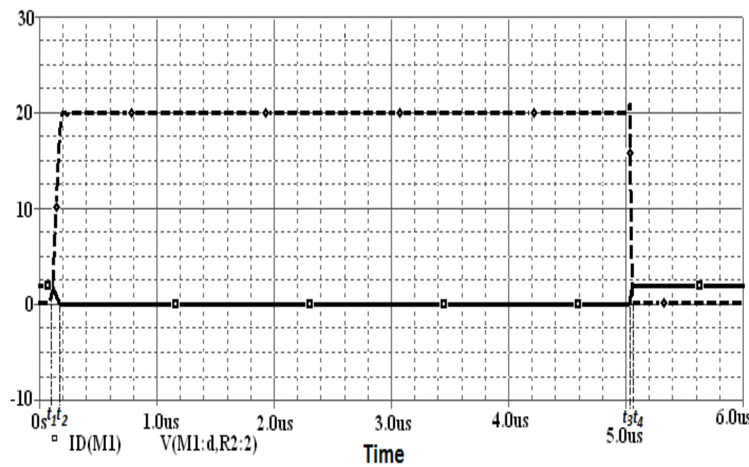


(b)

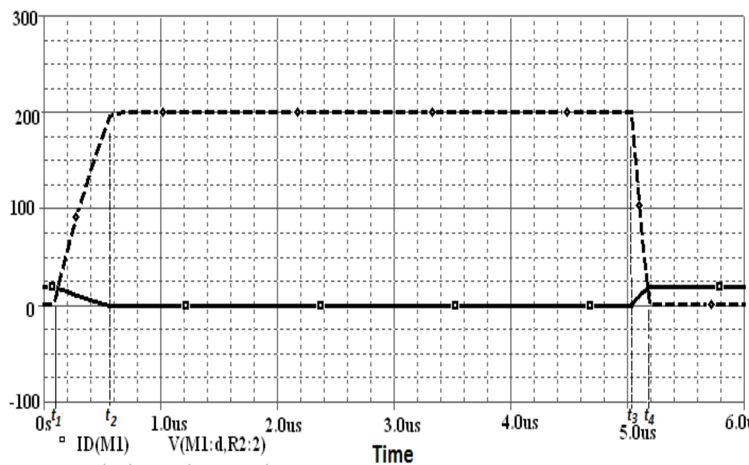
Figure 3.4 MOSFET gate-source voltage waveforms of the circuit seen in Figure 3.2 for a) V_{DC}=20 Volt b) V_{DC}=200 Volt

In Figure 3.4, Miller plateaus consisted in gate-source voltages are given. Gate-source voltage begins to fall from zero second until the MOSFET enters the linear mode of operation. In the linear region, falling time rate of the gate source voltage significantly slows down when the supply voltage is increased as seen in Figure of 3.4 between t_1-t_2 time intervals. Gate-source voltage of the MOSFET begins to increase whenever V_{pulse} falling edge occurs at t_3=5 μseconds. Once again, rate of the rise of the gate source voltage slows down in between t_3 and t_4. Miller plateau, which occurs during the falling and rising of the gate-source voltage affected from the increasing of the DC supply voltage value. While the increasing of the DC supply voltage level, charging and discharging time of the C_{GD} gets longer and the length of

the Miller plateau is also widen. This variation tends to increase the current passing through the MOSFET, means an increment in the slope of the i_d versus V_{GS}. Thus, C_{GD} is charged to high value and discharged from this high value inherently and charging and discharging time of the C_{GD} is increased.



(a)



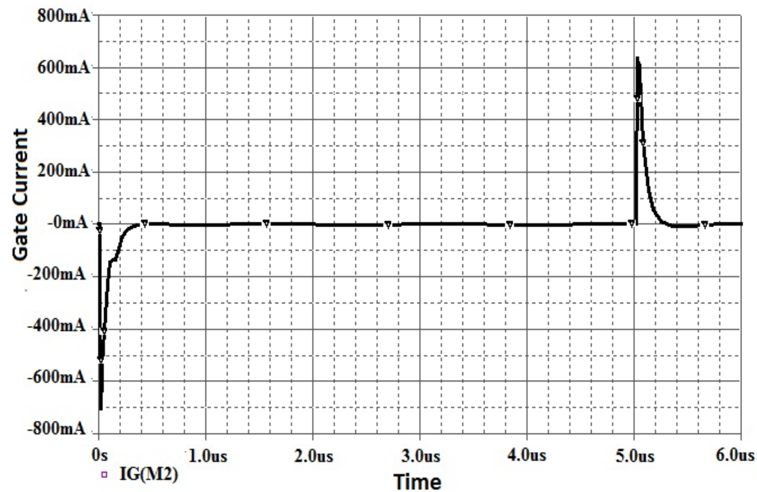
(b)

-- Drain Voltage — Drain Current

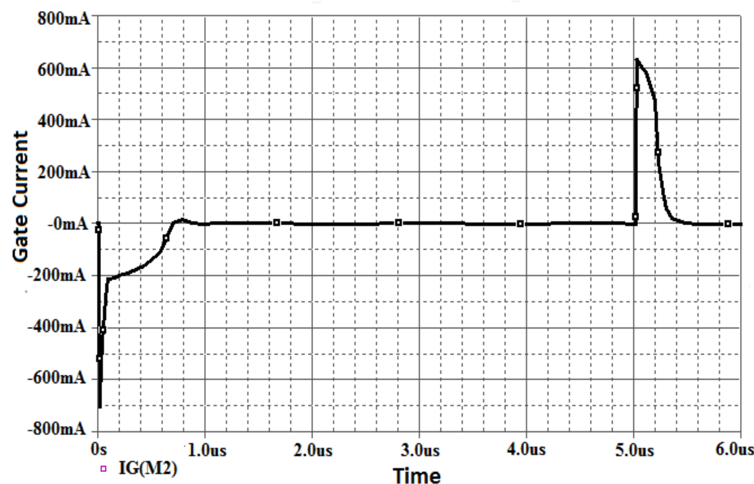
Figure 3.5 Drain voltage and current waveforms of the MOSFET seen in Figure 3.2 for a) V_{DC}=20Volt b) V_{DC}=200 Volt

When gate-source voltage of the MOSFET begins to decrease, drain-source voltage begins to increase, and drain current begins to decrease as seen in Figure 3.5 between t_1-t_2. On the other hand, when V_{GS} voltage of the MOSFET reaches to the threshold value, MOSFET becomes on and drain-source voltage begins to decrease.

Since the drain current is inversely proportional to the drain-source voltage, current becomes to increase to the load current value level as shown in Figure 3.5 between t_3–t_4. Some current begins to flow through the gate-drain capacitance in the opposite direction. And consequently, gate-drain capacitance charges into the input during this interval as well. It is concluded that from Figure 3.5 rise and fall times of both drain current and voltage get longer by the increment of the DC voltage source.



(a)



(b)

Figure 3.6 Gate current waveforms of the MOSFET seen in Figure 3.2 for a) V_{DC}=20Volt b) V_{DC}=200 Volt

Gate current waveforms of the MOSFET for 20 Volts and 200 Volts supply voltage values are seen in Figure 3.6. Charging and discharging time of the C_{GD} capacitance is changed with the variation of the drain source voltage, affects the time

constant of the gate current. It takes much longer time for the gate current to reach to the zero level when high DC voltage is applied as seen in Figure 3.6.b. Although, it affects the time constant, the magnitude of the current is same for both conditions.

As it has mentioned before, Miller capacitances affect the circuit in the linear region of the operating condition. Due to the Miller Effect rate of rise and fall of the gate-source voltages decreases slowly. By inspecting simulation waveforms it is understood that Miller capacitance is particularly an important problem in high voltage switching circuit.

3.3 Analyzing a MOSFET Switching Circuit with an Inductive Load

Switching circuit including an inductive load is used very commonly in power electronics such as motors, transformers, electromechanical relays. A basic power switching circuit with inductive load is shown in Figure 3.7.

A DC current source represents the model of the inductive load in Figure 3.7. In this Figure, D is the free-wheeling diode and has a part number of MBR1045. 100 Volt supply voltage is applied and IRF540 Power MOSFET is driven with a pulse source V_{pulse}. Value of the gate resistance (R_G) is 20Ω and DC current source represents the inductive load is 10 Amperes.

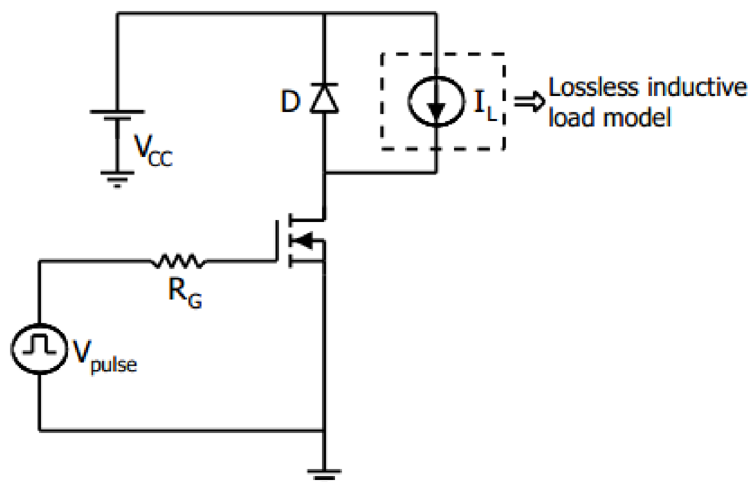


Figure 3.7 Switching test circuit with an inductive load model for simulation purposes

The equivalent circuit model of the MOSFET is same as in Figure 3.1, the only difference for the calculations is the drain and source leads inductances are neglected in the analyzes (Perret, 2009).

3.3.1 Simulation and Calculation of a Switching Test Circuit with an Inductive Load

Switching power circuit with an inductive load is simulated to observe the delay times, and emphasize the Miller Effect for turn-on and turn-off switching. Simulation results of the MOSFET gate-source voltage, drain-source voltage, drain and gate currents during switching are shown in Figure 3.8 and Figure 3.9. Analytical calculation for the inductive load is given in this chapter. In these calculations the parasitic elements are neglected.

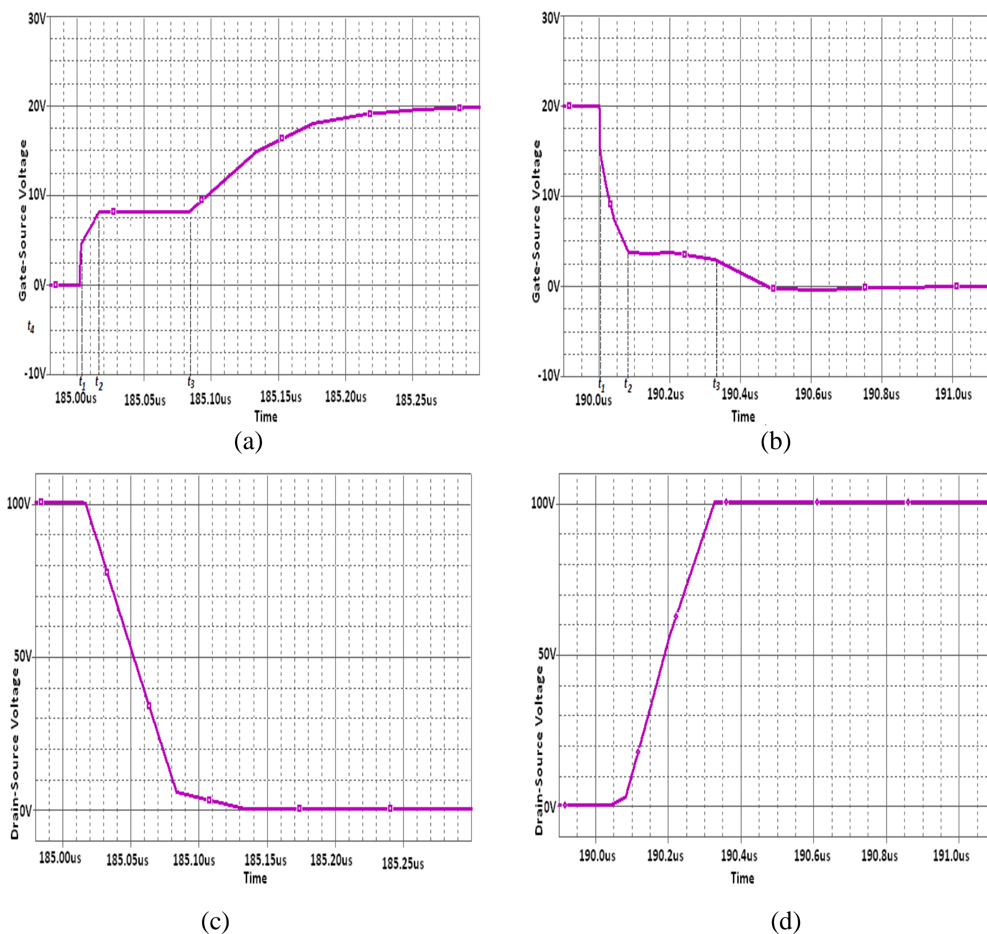


Figure 3.8 Simulation results of the MOSFET gate-source voltage during a) turn-on b) turn-off, drain-source voltage during c) turn-on d) turn-off

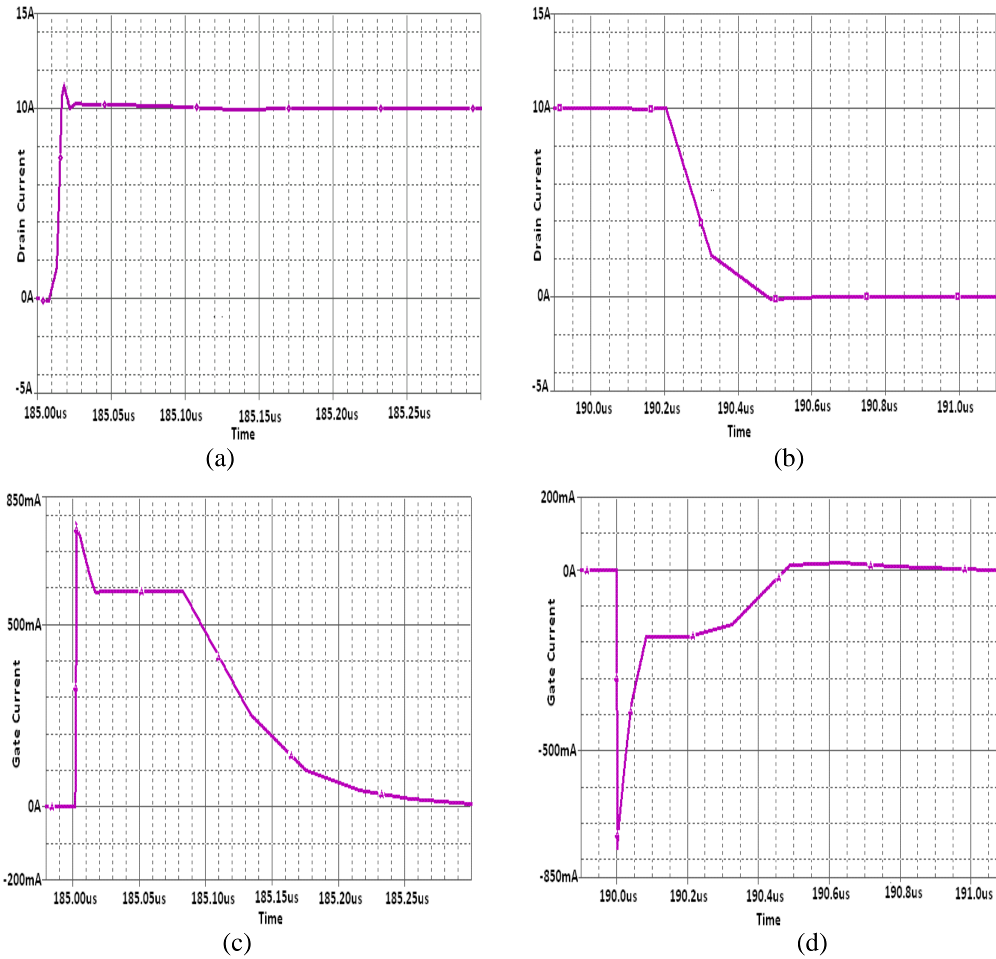


Figure 3.9 Simulation results of the MOSFET waveforms a) drain turn-on current b) drain turn-off current c) gate turn-on current c) gate turn-off current

MOSFET turn-on switching operation could be divided into four intervals. In the first period (before t_1), MOSFET is in the cut-off region and drain current is equal to zero until the gate-source voltage (V_{GS}) reaches the threshold level. Gate current decreases in this period. Gate source capacitance is charged and gate-drain capacitance is discharged. Gate source voltage increases with a time constant;

$$\tau_1 = R_G(C_{GS} + C_{GD}) = R_G C_{iss} \tag{3.8}$$

Gate- source voltage is;

$$V_{GS}(t) = V_{pulse}[1 - 2e^{-\frac{t_1}{\tau_1}}] \tag{3.9}$$

Delay time for the first period is equal to;

$$t_1 = (C_{GD} + C_{GS}) \ln\left(1 - \frac{V_{th}}{V_{pulse}}\right)^{-1} \tag{3.10}$$

MOSFET drain source voltage is almost constant and the value is the sum of the DC supply voltage (V_{CC}) and diode forward voltage (V_D);

$$V_{DS} = V_{CC} + V_D \tag{3.11}$$

Substrate doping, gate oxide thickness, source-to-substrate voltage bias, gate material, and surface charge density are the determining factors of the threshold level that is given in the datasheets of the MOSFET (Baker, 2005). When the gate- source voltage of the MOSFET is equal to the threshold level, it starts to be on and the drain current begins to increase; in the circumstances second period starts (between t_1 and t_2). In this interval, V_{GS} continues to increase until it reaches the Miller plateau level $(V_{TH} + I_L / g_m)$. Miller plateau level is shown in Figure 3.8.a and 3.8.b. Equation for the V_{GS} and delay time for this period is same as in the first period. And, the intrinsic capacitances; C_{GS} continues to be charged and C_{GD} continues to be discharged. Gate current goes on decreasing. Diode becomes off at the end of the second period. Drain current rises from zero to the load current by the equation;

$$I_d(t) = g_{fs}(V_{pulse} - V_{Th})[1 - e^{-\frac{t_2}{R_G(C_{GS}+C_{GD})}}] \tag{3.12}$$

The time for the drain current to reach the load current is;

$$t_2 = -R_G(C_{GS} + C_{GD}) \ln\left(1 - \frac{I_L}{g_{fs}(V_{pulse} - V_{th})}\right) \tag{3.13}$$

In the third period, drain current becomes constant in steady state condition and equal to the load current. V_{DS} falls down from $V_{CC} + V_D$ to $I_L r_{ds(on)}$(low on state

voltage). The attenuation ratio of the V_{DS} is equal to the increase rate of the V_{GD} ($\frac{dV_{GD}}{dt} = \frac{dV_{DS}}{dt}$). Miller Effect becomes effective in this period (Kazimierczuk, 2008). Due to V_{GS} remains stable at Miller plateau level, gate current begins to flow through the C_{GD} which is also called reverse transfer capacitance and C_{GD} starts charging. Therefore, gate current is equal to;

$$I_G = C_{GD} \frac{dV_{GD}}{dt} = C_{GD} \frac{dV_{DS}}{dt} \tag{3.14}$$

Time interval is obtained by taking the integral of the equation according to the variation of the drain source voltage between $V_{CC} + V_D$ and $I_L R_{ds_on}$.

$$\frac{C_{GD}}{I_G} = \frac{dV_{DS}}{dt}\Bigg|_{I_L R_{ds_on}}^{V_{CC}+V_D} \tag{3.15}$$

$$t_3 = \frac{C_{GD}}{I_G}(V_{CC} + V_D - I_L R_{ds_on}) \tag{3.16}$$

Input capacitance of the MOSFET is increased by C_{GD} due to Miller effect. Voltage gain is obtained;

$$A_v = \frac{dV_{DS}}{dV_{GS}} \tag{3.17}$$

When voltage gain is integrated into the C_{GD}, total input capacitance becomes;

$$C_{iss} = C_{GS} + (1 - A_v)C_{GD} \tag{3.18}$$

The time required to turn-on switching is the sum of the three intervals given above. Hence,

$$t = t_1 + t_2 + t_3 = \left[(C_{GD} + C_{GS}) \ln\left(1 - \frac{V_{th}}{V_{pulse}}\right)^{-1} \right] + \left[-R_G (C_{GS} + C_{GD}) \ln\left(1 - \frac{L_L}{g_{fs}(V_{pulse} - V_{th})}\right) \right] + \left[\frac{C_{GD}}{I_G} (V_{CC} + V_D - I_L R_{ds_on} \right] \quad (3.19)$$

In the fourth interval, turn-on switching of the MOSFET occurs completely. V_{DS} maintains being in the low on state voltage. V_{GS} increases to the V_{pulse} value. Drain current is still equal to the load current. Diode is in the off state.

MOSFET turn-off switching transients can be analyzed in four intervals as well. When driver voltage goes to zero, the first interval starts. Gate voltage begins to decrease up to the Miller plateau in this period. Also, drain current is constant and V_{DS} increases with a very slow rate since only the increment of the channel resistance is effective on V_{DS} .

$$V_{DS} = I_L R_{ds_on} \quad (3.20)$$

Delay time for the first period is equal to;

$$t_1 = R_G (C_{GD} + C_{GS}) \ln\left(\frac{V_{GS_ON}}{V_{plateau}}\right) \quad (3.21)$$

In the second interval, Miller Effect occurs. Drain voltage increases quite a lot. Gate voltage and drain current become constant.

$$V_{DS}(t) = \left(\frac{g_{fs} V_{GS(th)} + I_d}{(1 + g_{fs} R_G) C_{GD} + C_{DS}} \right) (t - t_2) \quad (3.22)$$

where t is the instant time.

In the third interval, the Miller Effect disappears. Diode begins to conduct in this period. Gate source voltage decreases exponentially to the level of threshold voltage.

In the last interval, drain current decreases to zero and drain voltage reaches to the source voltage value.

3.3.2 Reverse Recovery Phenomena in Circuits with Inductive Load

When MOSFET turns off, diode becomes forward biased and current flows through this diode. Although diode is used to protect the circuit from possible damages, some failures can cause due to the long reverse recovery time of the diode. Simulation with a schottky diode, has very low reverse recovery time compared to the switched mode power rectifier, is given in section 3.3. In this part, switched mode power rectifier is used to observe the reverse recovery effect of the diode to the circuit during turn-on.

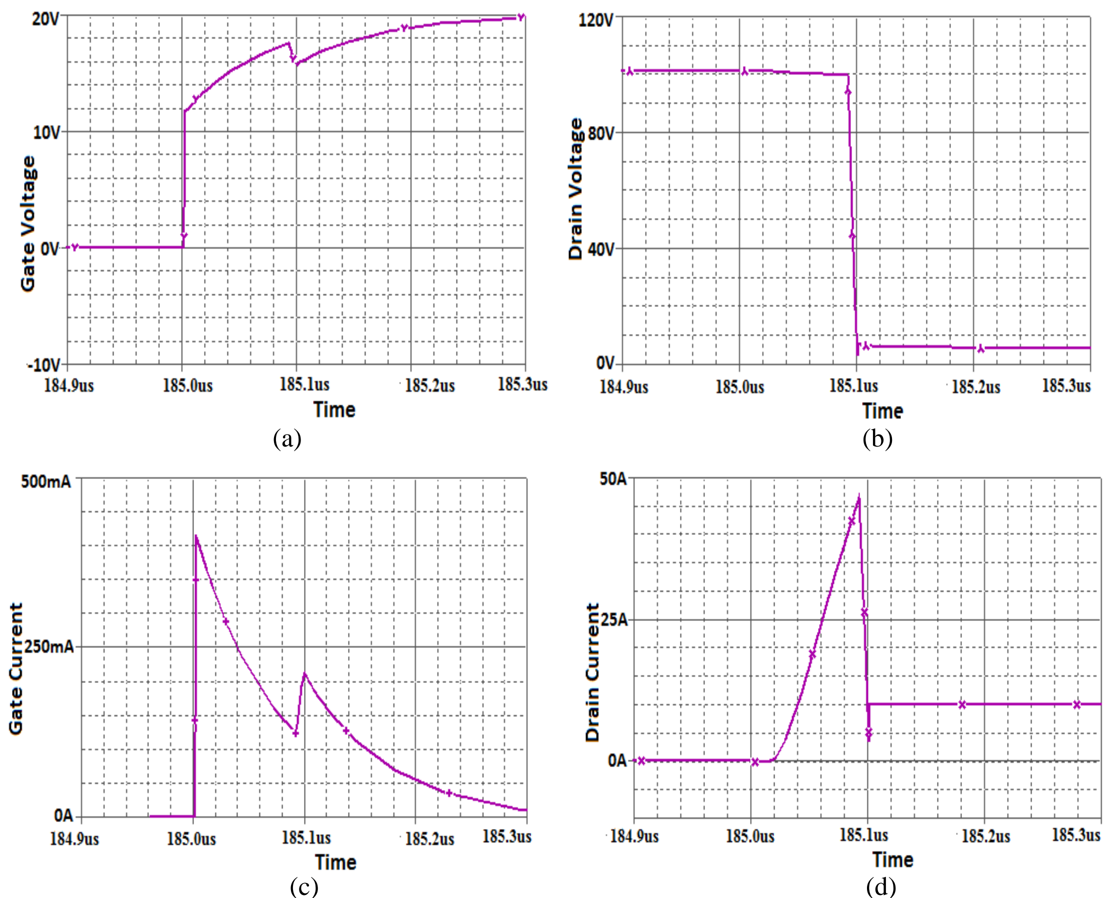


Figure 3.10 Simulation waveforms of Circuit of Figure 3.7 a) Gate Voltage b) Drain Voltage c) Gate Current d) Drain Current

Gate and drain voltage and current waveforms are seen in Figure 3.10. Drain current increases to 47 Amperes level rapidly and drain voltage is constant in the meantime. Power gets higher under the circumstances and this increment can cause heating failures.

CHAPTER FOUR
ZERO VOLTAGE SWITCHING TECHNIQUE AND WAVEFORMS IN HIGH FREQUENCY POWER PROCESSING CIRCUITS

Increasing switching frequency of the power processing circuits (converters, inverters) has some advantages, such as smaller size, lower cost, and higher power density. On the other hand, high switching losses, current/voltage stresses, oscillations and high Electromagnetic Interference (EMI) caused by high current and voltage peaks during switching actions are the failures that can be caused by the switching frequency increment.

Soft switching techniques are used in the design stage of the circuits for minimizing the losses that depend on the increment of the high frequency (Jitaru, 1992; Duarte & Barbi, 2000; Zhang & Sen, 2003). There are two types of soft switching techniques. These are zero voltage switching (ZVS) and zero current switching (ZCS). In zero current switching, the current across the switch is zero or close to zero before the device begins the switching condition. However, the voltage across the switch is zero or close to zero before the device begins the switching condition in zero voltage switching. Zero voltage switching is commonly used in constant load applications.

A resonant inverter using MOSFETs as switching elements working in zero voltage switching scheme designed and is realized to investigate possible surge current and voltage levels. In resonant inverter circuits, turn-on or turn-off transitions of semiconductor devices can occur at zero or close to zero crossings of voltage or current by the help of the LC resonance circuits whose voltage and current waveforms vary sinusoidal during one or more subintervals of each switching period. This technique minimizes the switching losses, improve the efficiency, and reduce the current/voltage stresses and the difficulty of implementation (Mohan, Undeland & Robbins, 1989; Wilamowski & Irwin, 2011).

Generally, ZVS is preferred at high switching frequencies since the internal capacitance of the semiconductor switch is discharged when the voltage of this capacitor is very low (zero in ideal case). This charge in fact gets out as heat during turn-on. This loss becomes serious at very high switching frequencies. It seems to be not easy practically to diagnose this surge current waveform (Jovanovic, Wojciech, & Fred, 1988; Mohan, et al., 1989), since it flows just in MOSFET die or chip.

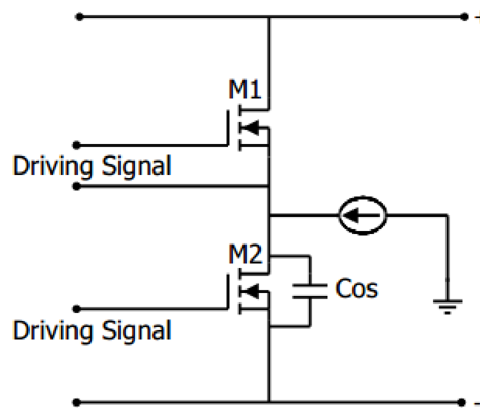
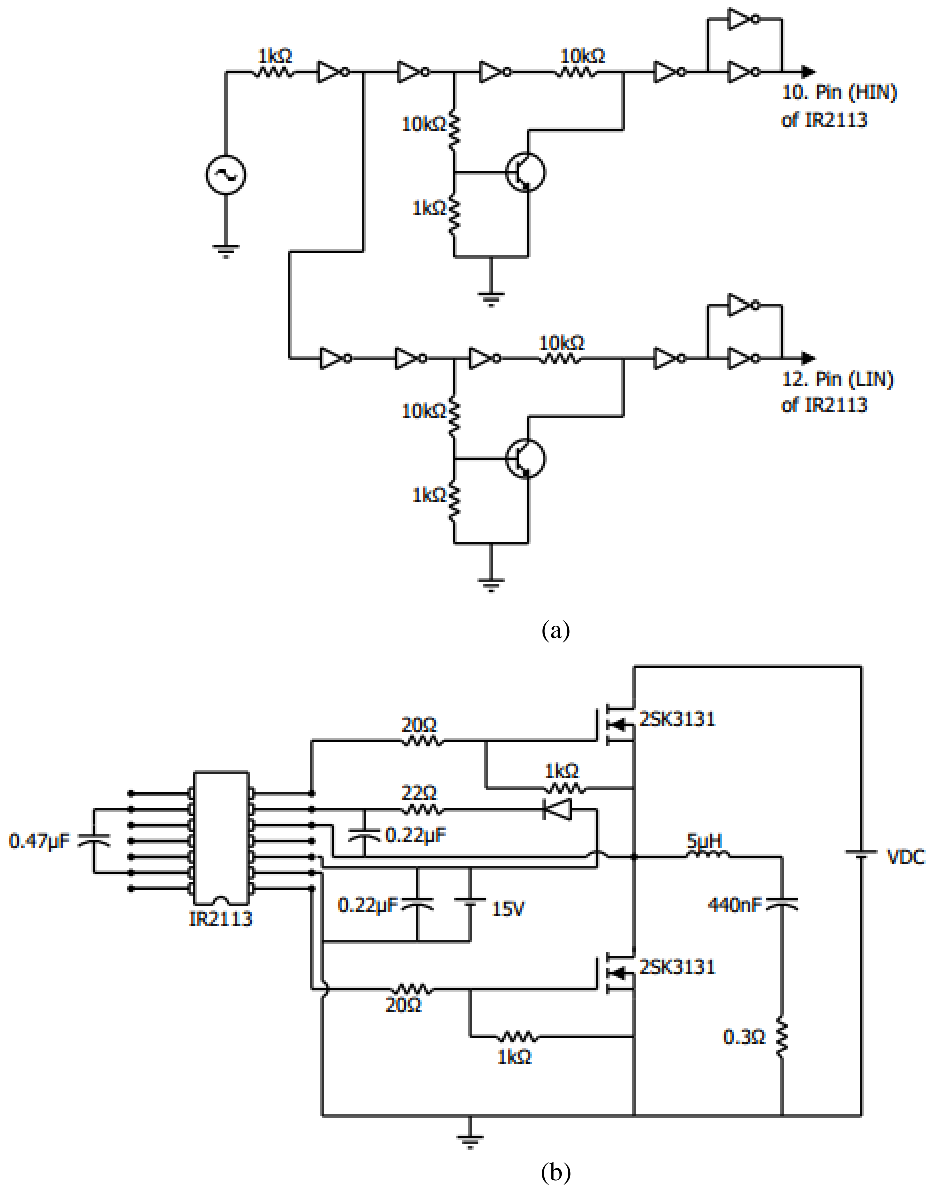


Figure 4.1 Series resonant load circuit model (a current source) for only very short time duration (due to series inductance of the resonant load)

Consider both M1 and M2 are off at t_1 instant (underlap switching strategy). When some time elapse lets indicate as t_2 at that instant, a voltage of ΔV appears across the terminals of M2 (also C_{DS} capacitor). When M2 is turned on, a surge current would pass through the body of the M2 and to diagnose this current using a single experimental set up seems to be not possible.

4.1 Studying a Series Resonant Inverter Operation

A high frequency zero voltage switching series resonant inverter which uses two MOSFETs as switching elements is shown in Figure 4.2 is realized and then simulated. Simulation is performed using ORCAD 9.1 software. In this circuit an IR2113 chip is utilized as a MOSFET Driver circuit, CD4069 is used as gate driver and pulse shaping circuit to prevent cross conduction of the totem-pole connected main switches; SK3131 N Channel MOSFETs are used as switching elements.



(a)

(b)

Figure 4.2 Schematic of the series-resonant inverter circuit prototype a) Driving signal underlapping generation circuit b) Floating driver and power stage

The driving signal shaping part of the circuit, seen in Figure 4.2.a, is designed to provide underlapping logic inputs to IR2113 IC. Underlapping input signals are required to prevent both output MOSFET transistors from becoming ON otherwise shoot-through current spikes may occur. A CD4069 IC, each has six logic inverters are used in this circuit. A resistor of 1kΩ value connected series to the laboratory signal generator in Figure 4.2.a ensures not to apply any excessive voltage level outside the supply voltage range. This resistor together with clamping diodes inside of each inverter block in CD4069 chip limits input voltage to levels of (0–$V_{\text{diode forward}}$

$_{voltage}$) and (15V+ $V_{diode\ forward\ voltage}$). Pulse should reach at least “Input High Voltage” level for transition of inverter from off to on state, so as to obtain high voltage at the output and the time elapsed to reach this level is called delay time. Likewise, pulse should not exceed “Input Low Voltage” level for transition of inverter from on to off state and the time needed to reach this level is equal to the delay time too. Time delay from “ON” to “OFF” state does not occur since 2N2222 BJT transistors in the circuit of Figure 4.2.a are used. Due to the high voltage applied to the base of the transistor, it will be turn-on and acts as a closed switch, by this means output of the inverter is abruptly withdrawn to zero. As a consequence, underlap switching is provided.

The IR2113 IC is a MOSFET driver chip that has independent high and low-side output channels with different reference points. Although a MOSFET transistor is a majority carrier device, its intrinsic body diode is a minority carrier device. The slope of the current flowing through the body diode and the amount of charge stored in the body diode during the conduction stage determine the reverse current peak value (Korec, 2011). And so, its stored minority charges must be removed before turning off the MOSFET as long as the reverse recovery time of the MOSFET body diode is fast. Otherwise, $C\frac{dv}{dt}$ shoot through current might produce a large current overshoot and can cause important failures in ZVS circuits (Redl & Dierberger, 1998; Fie, Wu & Saro, 2001). To overcome these failures and obtain fast reverse recovery, high speed freewheeling body diode especially at lower reverse voltage is needed. At this point SK3131 power MOSFET that has fast recovery body diode is used in the implementation. In fact, using MOSFET with fast intrinsic diode is necessary but not sufficient to prevent reverse recovery induced losses. Operating frequency of the circuit is an important factor for reducing those losses as well.

Another important parameter for the MOSFET is on state resistance (R_{ds_on}). Voltage of the drain-source terminals of the MOSFET after turn-on transient depends on R_{ds_on} resistor’s value and current passing through it. If the resistor R_{ds_on} has a small value, the voltage of the drain source terminal is also low. Hence, R_{ds_on}

determines the power loss in the on state too. Power loss that arises from on state resistance is named as conduction loss and calculated by $I_{rms}^{2} \times R_{ds_on}$. I_{rms} is the RMS value of the drain current. Also, intrinsic capacitances of the MOSFET are important for the switching action. Charging and discharging of the intrinsic capacitances of a MOSFET determines the switching response time. The gate drain capacitance C_{gd} varies with the potential across its terminal, called "Miller", affects the negative feedback from input to output and increases the apparent input capacitances (Kazimierczuk, 2008). In Miller plateau level, drain current is constant and nearly equals to the load current and V_{gs} is constant as well, hence gate current is discharged through the gate-drain capacitance with a rate of $C_{gd}\dfrac{dV_{ds}}{dt}$ (Baliga, 2008). Due to the increase of the apparent value of the C_{gd} on account of the Miller Effect, rate of the discharging of the gate current is small. If the turn-on or turn-off transition of the MOSFET is performed while the drain source voltage is equal or close to zero, Miller Effect will be reduced. This is an effective method to reduce the Miller Effect since energy storage of the capacitances does not occur during zero voltage switching. Zero voltage is obtained by the resonant circuit. At zero voltage switching, current is already flowing through the MOSFET body diode.

In the implemented circuit, 20 Ω resistors are connected to the input of the gates of the both low and high side MOSFETs. The value of these resistors should be enough to prevent the ringing and not as much as to reduce the switching speed.

In the IR2113 chip, a bootstrap circuit is used to supply power to drive the high side N-channel MOSFET. It is charged when the lower side MOSFET is turned on and the output pin is below the supply voltage. Bootstrap capacitor has to charge up very quickly thus, diode used in bootstrap circuit should be schottky diode which has very small reverse recovery. When the low side MOSFET turn-off, the voltage of the bootstrap capacitor come up to the supply voltage level thus voltage for driving the high side MOSFET is obtained. Otherwise, bootstrap capacitor is discharged only when the high side MOSFET turns on. The negative voltage occurs at the source of the switching device during turn-off causes load current to suddenly flow in the low

side freewheeling diode. The inductive parasitic elements, turn- off speed, di/dt of the MOSFET and gate-source capacitance and Miller capacitance affect the occurrence of the negative voltage (Fairchild, n.d.).

4.1.1 The Resonant and Operating Frequencies of a Resonant Inverter

The load impedance is resistive at resonant frequency. In order to drive the circuit at resonant frequency, the magnitudes of the inductor, resistor and capacitor forming a series circuit are determined by the resonant frequency equation for obtaining zero in imaginal part. Then, series resonant frequency is equal to;

$$f_{resonant} = \frac{w}{2\pi} = \frac{\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}}{2\pi} \tag{4.1}$$

Element values in implemented series inverter are chosen as;

Inductor (L): 5 μH

Capacitor (C): 440 nF

Resistor (R): 0.3 Ω

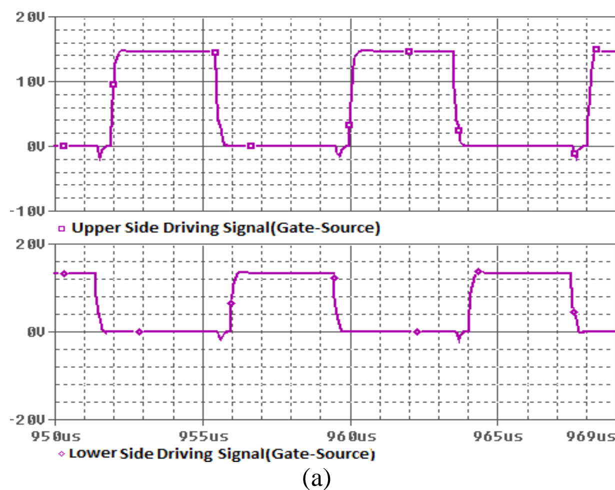
with these values, series resonant frequency is calculated as;

$$f = \frac{w}{2\pi} = 106.7kHz \tag{4.3}$$

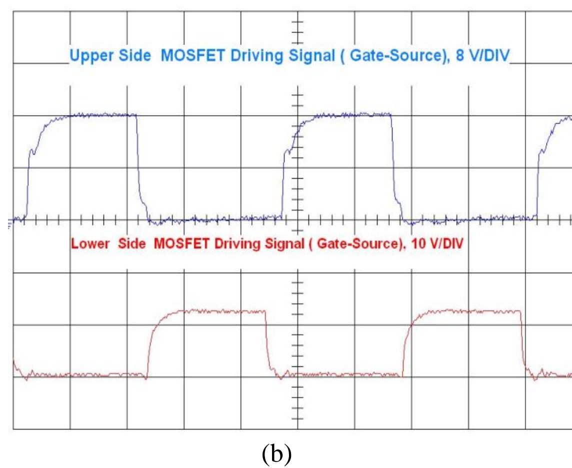
Operating frequency is a distinctive parameter for reducing losses and increasing the efficiency of the performance in resonant inverter circuits. The switching frequency is chosen as 124 kHz for working above resonance frequency. The impedance is inductive and output current lags the voltage at this frequency. Switching above the resonant frequency is preferred to get rid of the MOSFET's body diode's reverse recovery current induced losses. Because, in this case no freewheeling diode current flows.

4.1.2 Simulation and Practical Results of a ZVS Inverter Implemented

MOSFET driving signals and resonant capacitor voltage and currents waveforms are observed with a scope. A Tektronix P6022 AC Current Probe is used to observe current waveforms. Since this current sensing equipment is a current transformer based that contains toroidal core, L_S/R_S exponential decay arises out of the probe inductance loading the source impedance (Tektronix, 2013). Here, L_S is the secondary winding inductance and R_S is the secondary winding resistance. The output of probe inherently does not give any information on the measured current's DC value thus the current waveforms have been shifted towards upward or downward on the oscilloscope screen to any level for the best viewing purpose along with the other.



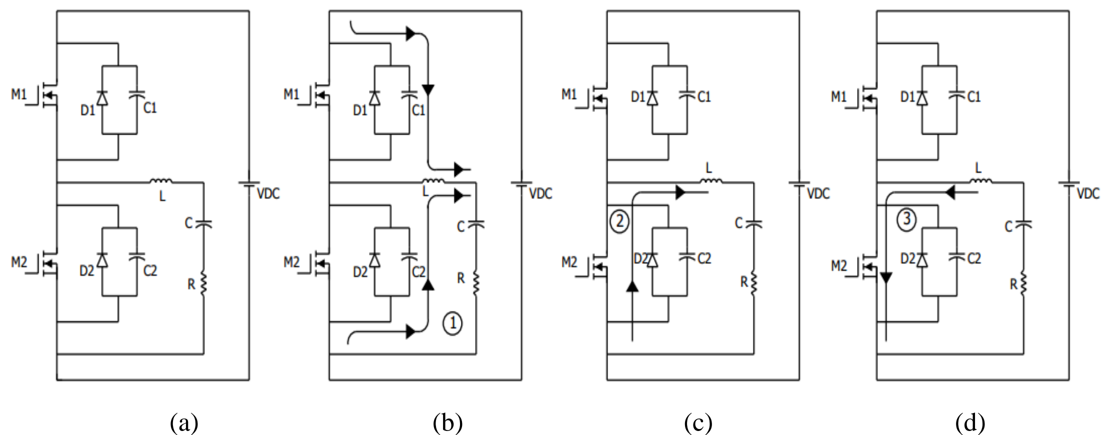
(a)



(b)

Figure 4.3 a) Driving signal simulation waveforms b) Driving signal experimental waveforms, 2 µs time/div, of the MOSFETs' driving signals of the circuit given in Figure 4.2

Driving signals of the upper and lower side MOSFETs simulation and practical results are shown in the Figure 4.3. While MOSFET on the upper side is passing from turn-on to turn-off, lower side MOSFET is enabled to stay in turn-off for approximately 0.5 μs by giving delay time as known. This is called underlap switching. During switching, logic propagation delay and the time required for charging or discharging power FET gate capacitance should be taken into consideration. The dead time should not be too long, since at that time conduction losses will occur. The reason is necessity to prevent a shoot through current and short circuit of the upper and lower switches. If both MOSFETs were in the on state, higher power dissipation and failures were occurred in the circuit due to short term excessive current.



(a) (b) (c) (d)

Figure 4.4 Commutation scheme of half- bridge resonant inverter switches a) Power stage with internal capacitance and diodes of the MOSFET b) Current commutates from M1 to M2 by turning on M1 and turning of M2 c) Current flowing path when the voltage of the lower side MOSFET capacitance (C2) voltage decreases to zero voltage d) Current path when resonant load current reversals

Initially, upper side MOSFET (M1) is in the ON state, then the internal capacitance voltage value of the upper side MOSFET is equal to zero. Lower side MOSFET (M2) is in the OFF state, and the internal capacitance voltage value of the lower side MOSFET is equal to V_{DC} at this time and current is flowing through the body diode of the lower side MOSFET. When zero voltage is applied to the gate of the upper side MOSFET, it turns off and the internal capacitance of the upper side MOSFET starts to be charged from zero volt to V_{DC}. And, the capacitor of the lower

side MOSFET is discharged from V_{DC} to zero volts at this interval. The current flowing paths are shown in Figure 4.4.b. The current flowing through the series resonant inverter must have both positive and negative value at every switching period in order to obtain a zero voltage switching. Although the current decreases to a negative value in the series resonant inverter leg, it can not decrease below zero value at the lower side of the MOSFET due to the body diode of the MOSFET. When the voltage of the lower side internal capacitance reaches the zero voltage value, the current goes to zero as well, since the capacitor's voltage can not change very quickly. At this point current starts to flow through the body diode of the lower side MOSFET, as shown in Figure 4.4.c. Afterwards, gate voltage is applied to the lower side MOSFET, and it turns on. Hence, current become to flow through the channel of the MOSFET as shown in the Figure 4.4.d.

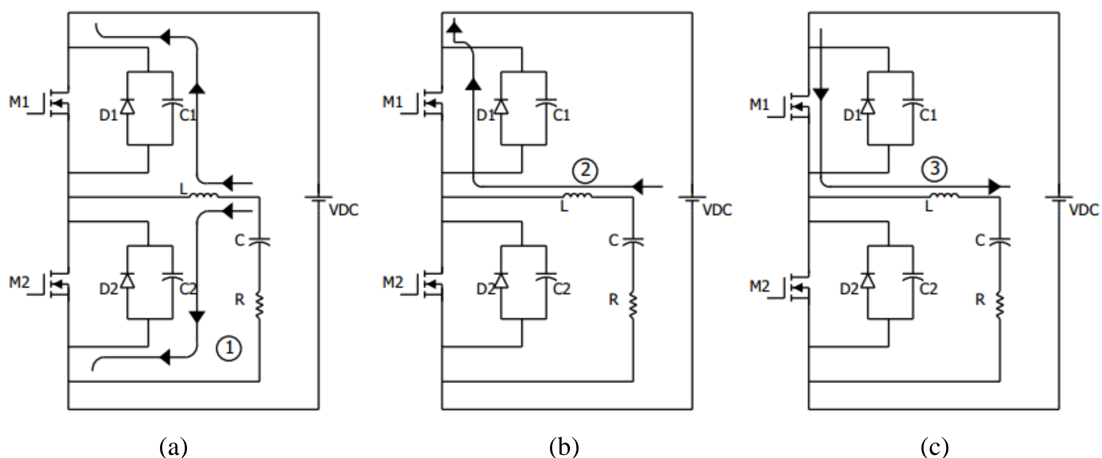
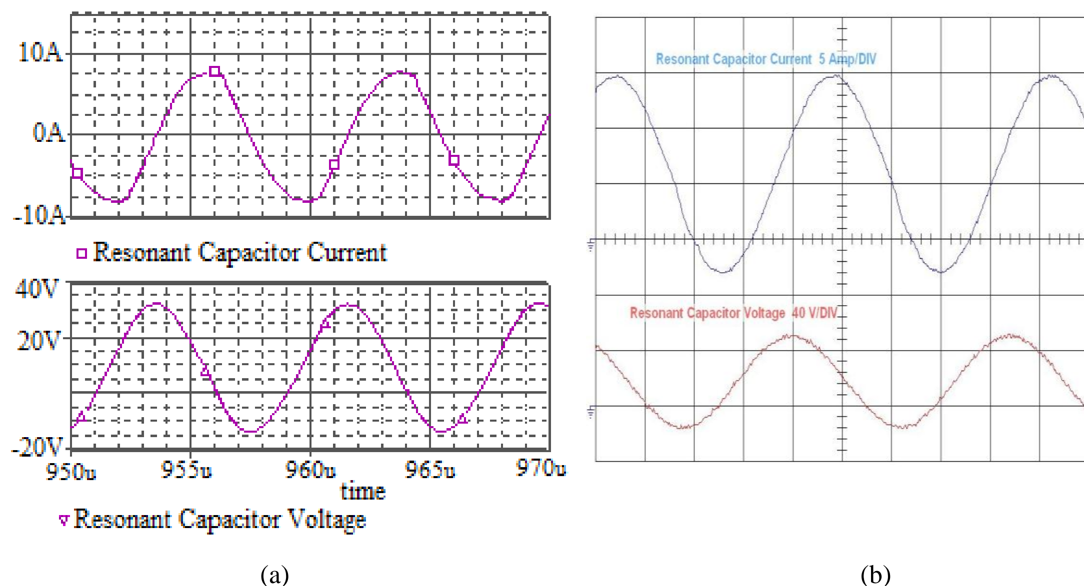


Figure 4.5 a) Current flowing path during charging and discharging of the MOSFETs' internal capacitances b) Current flowing path when the voltage of the upper side MOSFET's capacitance (C1) decreases to zero voltage c) Current path when gate voltage is applied to the upper side MOSFET

Additionally, when the upper side MOSFET turns on transition process is investigated, conditions of the MOSFETs, their body diodes and internal capacitances are explained as follows:

Lower side MOSFET (M1) is in the ON state, then the internal capacitance of the lower side MOSFET is equal to zero at the beginning. Upper side MOSFET is in the OFF state, and the internal capacitance of the lower side MOSFET is equal to

V_{DC} within this period. When zero voltage is applied to the gate of the lower side MOSFET, it turns off. Current flows through the internal capacitances of the MOSFETs, and causes the lower side MOSFET's internal capacitance to be charged up to the V_{DC} voltage level and upper side MOSFET's internal capacitance to be discharged up to the zero voltage level as shown in Figure 4.5. a. Later, body diode of the upper side MOSFET become conducting and current starts to flow through this diode as seen in Figure 4.5.b. When gate voltage is applied to the upper side MOSFET, current begins to flow through the channel of this MOSFET as given in Figure 4.5. c. And consequently, switching is occurred at zero voltage level.



(a) (b)

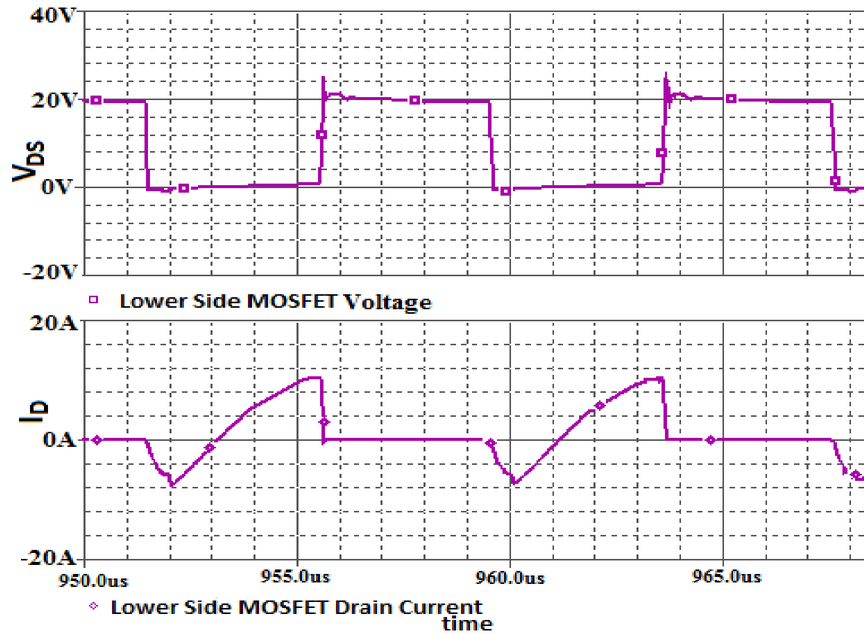
Figure 4.6 a) Simulation waveforms of resonant capacitor current and voltage of the load above resonant frequency b) Experimental waveforms of resonant capacitor current and voltage, 2 µs time/div

Current and voltage of the resonant capacitor is shown in the Figure 4.6. During the change in the status of the switches, the current flowing through the series resonant circuit is forced to change the direction. There is an inductor in the series resonant circuit. Due to the characteristic properties of the inductor, current flowing through it cannot change its direction suddenly. It must be zero before flowing in the reverse direction. Hence, the change in current path is obtained by the capacitor in the series leg of the resonant circuit. Instantaneous changes effect the magnitude of the capacitors current for series resonant inverter. Current lags voltage when the

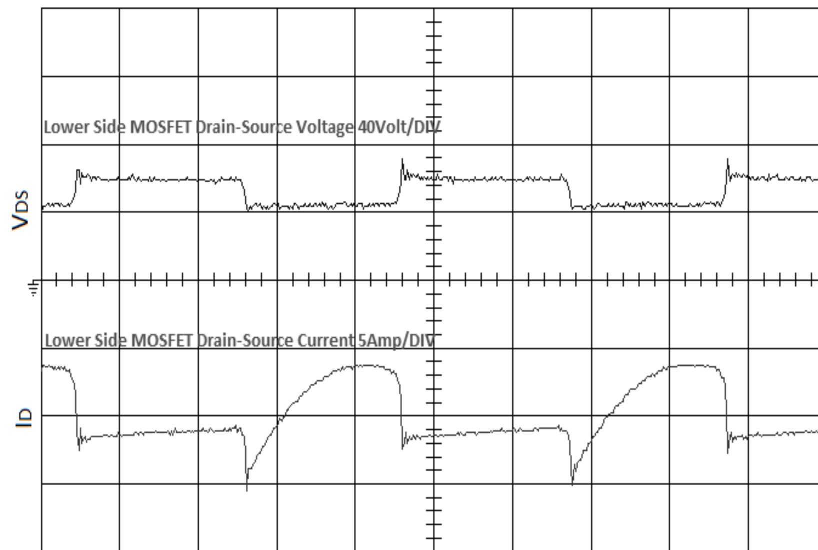
operating frequency is above resonant frequency, since zero transition of the voltage waveform occurs before the current waveform.

4.1.3 Simulation and Experimental Results of Lower Side MOSFET Drain-Source Voltage and Current Above and Below Resonant Frequencies

Lower side MOSFET drain-source voltage and current for above and below resonant frequencies are observed to see the reverse recovery effects of the body diodes. Switching frequency is chosen as 124 kHz for above resonant frequency analyses and 70 kHz for below resonant frequency analyses. When the switching frequency is lower than the resonant frequency, a high overshoots are observed on the lower side MOSFET drain-source current due to the both upper and lower side MOSFET's body diodes.



(a)

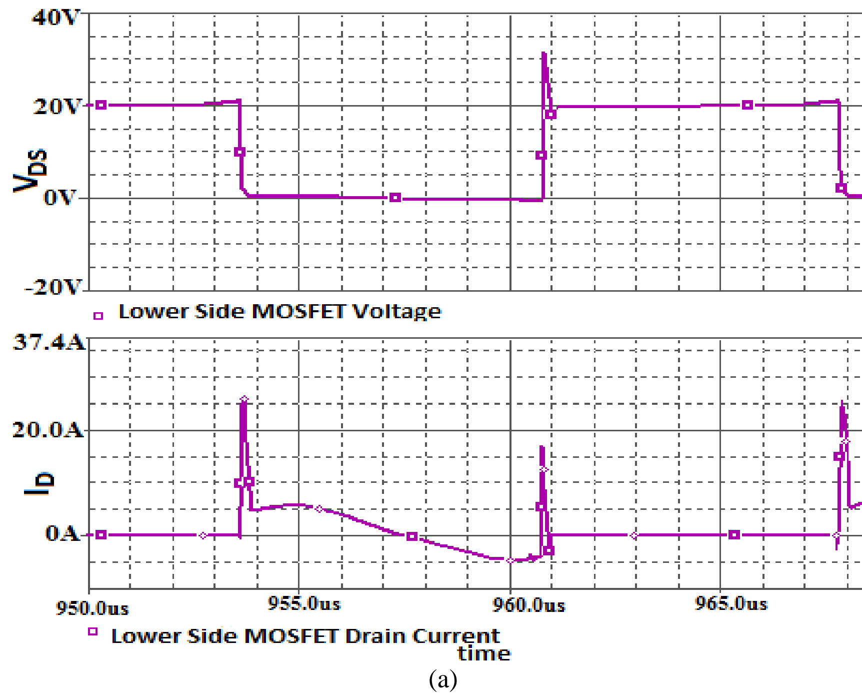


(b)

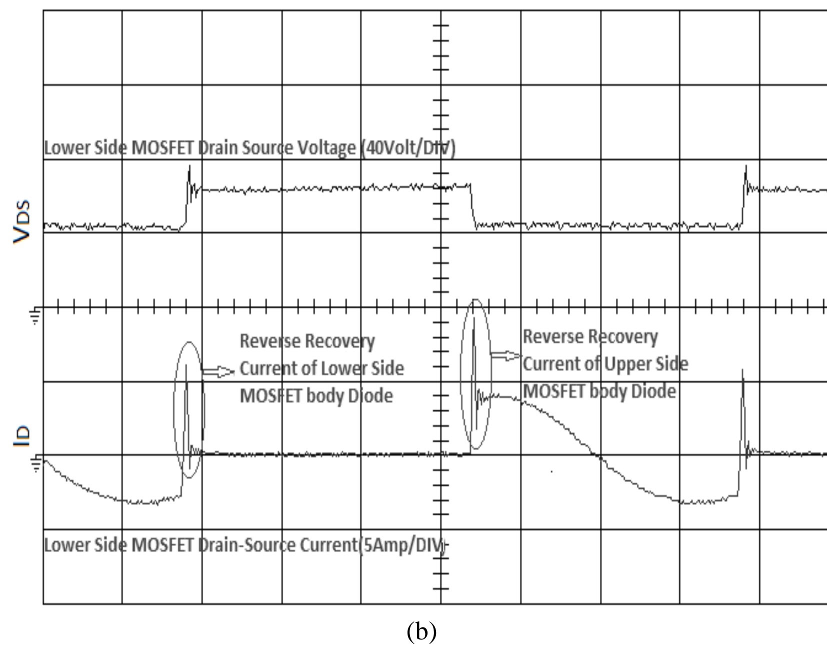
Figure 4.7 a) Simulation results of lower side MOSFET drain-source voltage and drain current b) Experimental results of lower side MOSFET drain-source voltage and current, $f_{switching}$ =124 kHz, and $f_{resonant}$ =106.7 kHz, 2 μs time/div

In the Figure 4.7, lower side MOSFET drain-source voltage and current are shown. The operating frequency is chosen to be equal to 124 kHz. In the OFF state the drain-source voltage of the lower side MOSFET is almost equal to the DC source voltage. Transition of the upper side MOSFET M1 from ON state to the OFF state a low magnitude current spike is seen in the lower side drain current due to the reverse

recovery of the lower side MOSFET M2 body diode. Average value of the current of the lower side MOSFET is equal to zero Ampere, at this time current is flowing through the resonant circuit. On the other hand, when the lower side MOSFET is ON, current is flowing through the drain of lower side MOSFET.



(a)



(b)

Fig 4.8 a) Simulation waveforms of lower side MOSFET drain-source voltage and drain current b) Experimental waveforms of lower side MOSFET drain-source voltage and drain current $f_{switching}$ =70 kHz, and $f_{resonant}$ =106.7 kHz , 2 µs time/div

Simulation and experimental results of lower side MOSFET drain-source voltage and current waveforms below resonant frequency is shown in Figure 4.8. The operating frequency is chosen to be around 70 kHz. When the circuit is in steady state operation and in the time interval that upper side MOSFET is in the OFF state, the current is flowing through the resonant circuit and lower side MOSFET. By the change of the direction of the resonant inductor current due to resonant effect, current begins to flow through the lower side MOSFET body diode and the lower side MOSFET turns off inherently. After a little time upper side MOSFET is triggered and turns on. The inductor current transfers to upper side MOSFET since it provides a higher voltage to feed to the resonant leg. Again the inductor current direction is changed and the current begins to flow through the body diode of the upper side MOSFET (Note that the switching frequency is lower than the resonant frequency in that case). After turning on the lower side MOSFET, the current switches to the lower side MOSFET and reverse recovery current of the upper side MOSFET body diode occurs due to instant reversal of the conducting upper side MOSFET body diode voltage. In fact this reverse recovery current is a short- circuit current (does not pass through the resonant load) with a low duration of time interval.

CHAPTER FIVE
INVESTIGATION OF PARASITIC EFFECTS OF A BOOST CONVERTER

Switched mode power supplies have generally both severe conducted and radiated EMI problems. Although the switching frequency mostly lies in kilohertz range, non negligible frequency content up to a few MHz occurs due to fast transitions of the pulse shaped waveforms.

Practical system characterization should be done by using scattering parameters rather than [Z], [Y], [H], [ABCD] parameters in high frequency. Main reason is that the open circuit or short circuit at one port is needed to determine [Z], [Y], [H], [ABCD] parameters. Making short circuit with a wire adds the inductive effect of the wire itself and open circuit lead to capacitive loading at the terminal, and both of them have nonignorable effect to the circuit (Ludwig & Bretchko, 2000). Considering this situation, layout of the circuit component and wiring parasitic effects are taken into account with full wave electromagnetic modeling techniques in simulation work through the simulated S-parameters. Full wave analysis consists of all electric and magnetic field components and indicates the field effect of distributed elements. For these reasons, full wave electromagnetic modeling techniques play an increasingly significant role to observe the Electromagnetic Interference (EMI) in switched mode power supplies due to the higher operating frequencies and increased circuit density (Lim, Williams & Finney, 2011; He, Fu, Gao, Zhang & Zhou, 2012). EMI appears in case of radiation and conduction. Radiated EMI occurs from the circuit and its interface leads when the energy flows through the circuit (Arnautovski-Toševa, Rousset, Drissi & Grčev, 2005). Conducted EMI depends on the physical condition of the circuit that is the switching action of the circuit. Differential-mode and common-mode interferences are the types of the conducted EMI. In common-mode interference, current flows in the same phase and direction on both power and ground conductors. In differential-mode, current flows in opposite direction through one AC conductor and returns along another. In this analysis travelling time of the signal from one point to any other point in the circuit have to be considered.

As known, in an alternating circuit, when the operating frequency increases the wavelength decreases. If the discrete circuit components average size is more than a tenth of the wavelength. Kirchoff's current and voltage law can not be applied directly instead of this; transmission theory should be applied to the circuit (Ludwig, 2009). Under these circumstances, circuit parameters are given in terms of unit length and called as distributed parameters. In this analysis, length of the transmission line and high frequency behavior of the circuit becomes more important. Full-wave modeling is an analysis technique that uses Maxwell Equations having regard to the transmission theory. CST MW STUDIO is one of the electromagnetic simulators using full wave modeling technique. This simulator was based on the Finite Integration Technique (FIT) including Maxwell's Equations in integral form and was first proposed by Weiland (1977). In this program, meshing is made for solving the geometrical structure and frequency is swept in a wideband to achieve accurate S-parameters. These S-parameters give the behavior of the high frequency characteristics of the circuit. Most researches use this program for microwave designs and antennas, only few of the researches use this program for power electronics designs (Cui, Zhang & Kam, 2008; Pommerenke, Centola, Lam & Steinfeld, 2009; Bhargava, Pommerenke, Kam, Centola & Lam, 2011; Bhargava, Pommerenke, Kam, Chang, Centola, Lam& Steinfeld, 2005, He et al., 2012). Through time, it has been seen that directly observing the parasitic effects which could come up in applications by using 3D programs becomes an important issue. CST MW STUDIO used for listing the EMC Design Guideline to minimize the ringing on the phase voltage waveform and the radiated noise typically in 50-300 MHz range of the synchronous buck converter. This list is obtained by adding a RL snubber circuit, moving the resonant frequency up and adding an input filtering as studied in (Kam et al., 2009). The study referenced in (Bhargava et al., 2011) also focuses on the optimization methods of the layout of a buck converter. In this reference paper, different layout configurations are analyzed and a flat horizontal loop over a ground plane is seen the lowest radiated emission by using this program. Furthermore, the Partial Element Equivalent Circuit and Finite Integration Techniques can be applied in transient analysis of MOSFET on the PCB that makes current noise to observe the EMI (Cui, 2008).

Comparison of SPICE and full-wave simulations of a boost converter was presented by Azizoglu & Karaca (2012). In this chapter, Boost Converter circuit is simulated with SPICE and CST MW STUDIO and implemented. Results are investigated and compared with each other. Furthermore, failures caused by the conducted EMI are especially investigated. For this aim, CST MW STUDIO simulation program is used in the design stage. In the program, meshing is made for solving the geometrical structure and frequency is swept in a wideband to achieve accurate S-parameters. These S-parameters give the behavior of the high frequency characteristics of the circuit.

5.1 A Practical Study on a Boost Converter Circuit and Layout Model

A boost converter circuit is simulated at 101.5 kHz switching frequency. Circuit schematic of this Boost Converter is given in Figure 5.1. IRF540ZS Power MOSFET is used as switching element. Output capacitor (C_O) value of the converter is chosen as 47μF. MBR1045 schottky rectifier is utilized as freewheeling diode to transfer the energy to the output during the OFF period. Load resistor is selected as 20 Ω. Operation mode can be determined by the value of the inductor as driven in section 5.2. Due to the calculations given in the next section, inductor value is chosen approximately 12.52 μH to observe the current and voltage waveforms in critical conduction mode.

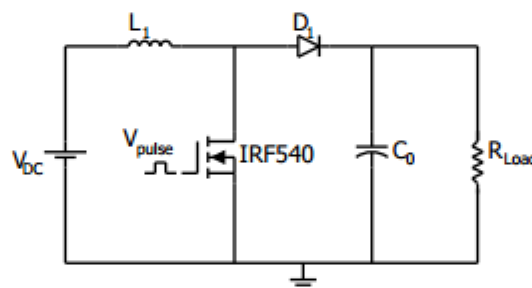


Figure 5.1 Circuit schematic of the implemented Boost converter

The computer simulations have been performed in PSPICE and CST MW STUDIO. Boost converter layout is represented in CST MW STUDIO as seen in

Figure 5.2. Some features of the simulation of the circuit for this program are as follows;

- Dimensions and distances between component nodes are determined by taking the actual components sizes into account.
- Wires are defined as copper which is not a perfect conductor.
- All nodes of the components are defined as ports to obtain S-parameters of those nodes. Since MOSFET has three nodes, ports are defined between the source and the drain and gate and source contacts as explained in (Bhargava, Pommerenke, Kam, Chang, Centola, Lam & Steinfeld, 2009).

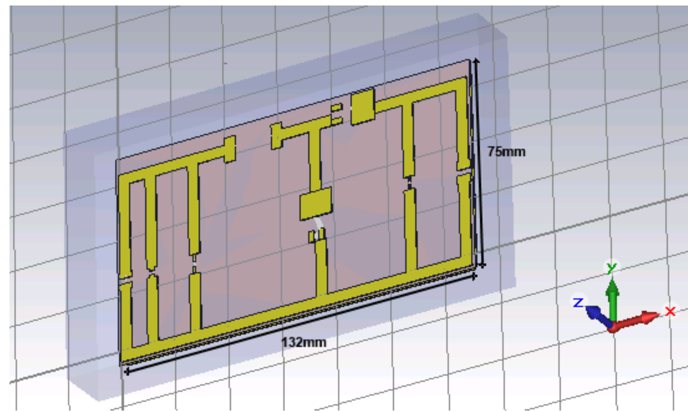


Figure 5.2 Layout designed in CST MW STUDIO

Layout of the components on PCB is crucial to mitigate the possible overshoots and losses of the switching circuit. To represent the DC connection paths with a good accuracy, the simulations are performed between the ranges of 1 Hz and 120 MHz in frequency domain.

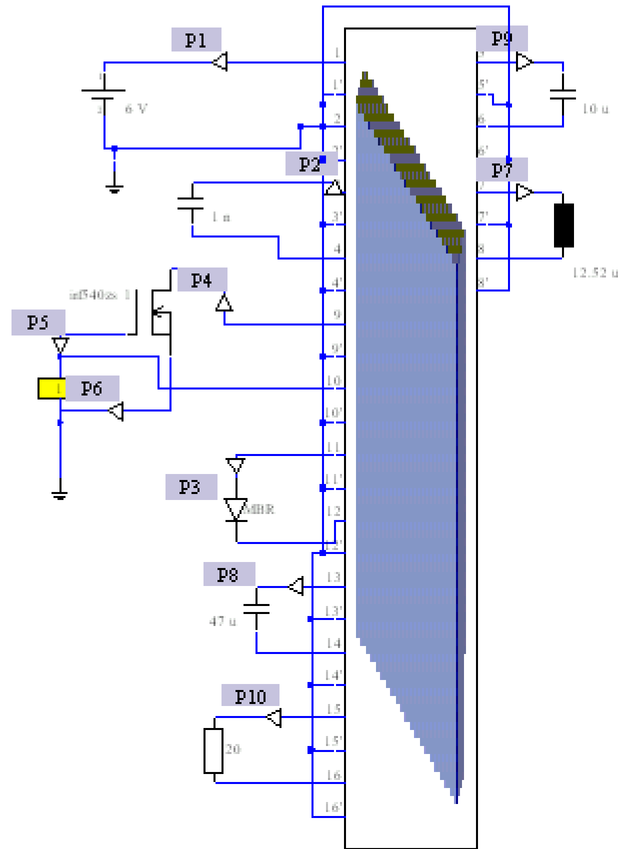


Figure 5.3 CST DESIGN STUDIO Schematic

CST DESIGN STUDIO is an advanced spice software. The S-parameter and impedance results obtained by using the electromagnetic solver (MWS) are transferred to this software automatically in the complete software environment. Layout of the circuit is seen as a block with pins. These pins are indicated the terminals of the components and all circuit elements are connected to the transferred block schematic as shown in Figure 5.3. Semiconductors (MOSFET and diode) are identified to the library by using the model library given in their websites.

5.2 Mathematical Calculations of Ideal case of Boost Converter

Mathematical calculations of the Boost converter for ideal case, by means of neglecting the wiring parasitics are done. Inductor value is chosen as 20 Ω and converter operates in critical conduction mode in this value. Minimum current value of the inductor is observed approximately zero level. This mode is also called transition mode. The expected high reverse recovery current seen in continuous

mode, and expected distortion in input current in discontinuous mode is not seen in case of critical conduction mode. Furthermore, heating caused by switching losses and EMI are generated only when the MOSFET turns off in critical conduction mode.

When MOSFET turns on and diode turns off, input supply draws current from inductance and MOSFET. Then, inductance stores energy due to the current flow. When MOSFET turns off, inductance current can not decreases to zero instantly and it provides diode transition. In this case both input supply and inductance transfer energy to the load through the diode.

Duty cycle is chosen as 0.5, hence output voltage is;

$$V_O = \frac{V_{input}}{1-D} = \frac{6}{1-0.5} = 12 \text{ Volt} \tag{5.1}$$

Switching frequency is adjusted to 101.5 kHz. In this frequency range; minimum inductance value for continuous conduction mode is;

$$L_{\min} = \frac{D \times (1-D)^2 \times R_O}{2 \times f_s} = \frac{0.5 \times (1-0.5)^2 \times 20}{2 \times 101.5kHz} = 12.31\mu H \tag{5.2}$$

Inductance value is chosen approximately 12.52 μH and works in critical conduction mode. Due to the critical conduction mode, inductor current value goes to zero before the MOSFET switch on. Limitation for the continuous conduction mode of the minimum inductance current value is zero. Above this value current becomes continuous, otherwise current becomes discontinuous. In continuous mode rate of the change of current is softer than discontinuous mode.

When the losses are neglected, input power is equal to the output power;

$$V_{in} \times i_{L(average)} = \frac{{V_0}^2}{R} \tag{5.3}$$

Average value of the current drawn from power supply;

$$V_{in} i_L = \frac{\left(\frac{V_{in}}{(1-D)}\right)^2}{R_0} = \frac{V_{in}^{\ 2}}{(1-D)^2 \times R_0} \tag{5.4}$$

$$i_L = \frac{V_{in}}{(1-D)^2 \times R_0} = \frac{6V}{(1-0.5)^2 \times 20} = 1.2 \text{ Amperes} \tag{5.5}$$

Minimum value of the inductor current;

$$i_{\min} = i_{L_1} - \frac{\Delta i_{L_1}}{2} = \frac{V_{in}}{(1-D)^2 \times R_0} - \frac{V_{in} \times D \times T_s}{2 \times L_1} = 1.2 - 1.133 = 0.067 \text{ Amperes} \tag{5.6}$$

Minimum current value of the inductor L_1 is almost zero as it is seen in Equation (5.6) hence it works in critical conduction mode.

Peak value of the inductor current is equal to;

$$i_{\max} = i_{L_1} + \frac{\Delta i_{L_1}}{2} = \frac{V_{in}}{(1-D)^2 \times R_0} + \frac{V_{in} \times D \times T_s}{2 \times L_1} = 1.2 + 1.13 = 2.33 \text{ Amperes} \tag{5.7}$$

It is easily concluded that in a boost converter circuit, average value of the diode current is equal to the load current, since average value of the output capacitor current is zero in a steady state case. And then in ideal case, output current is;

$$I_{diode_avg} = I_{output} = I_L \times (1-D) = 1.2 \times (1-0.5) = 0.6 \text{ Amperes} \tag{5.8}$$

When the output current increases by keeping the duty cycle constant, the inductor current also increases. The switching frequency and the amplitude of the inductor ripple current remain unchanged.

5.3 Analysis of the MOSFET Turn-on Switching Behaviour With Parasitics

Generally, losses caused by the component and wiring parasitics are neglected in the analysis of the converter. Eventhough, ideal calculation is necessary for estimating general working principle, it can not give exact results during transitions. Circuit model of the Boost Converter with component and inductive wiring parasitics that is effective in high-frequency characteristics is seen in Figure 5.4 and must have been taken into account for analaysing the circuit transition behaviour (Severns, 2008).

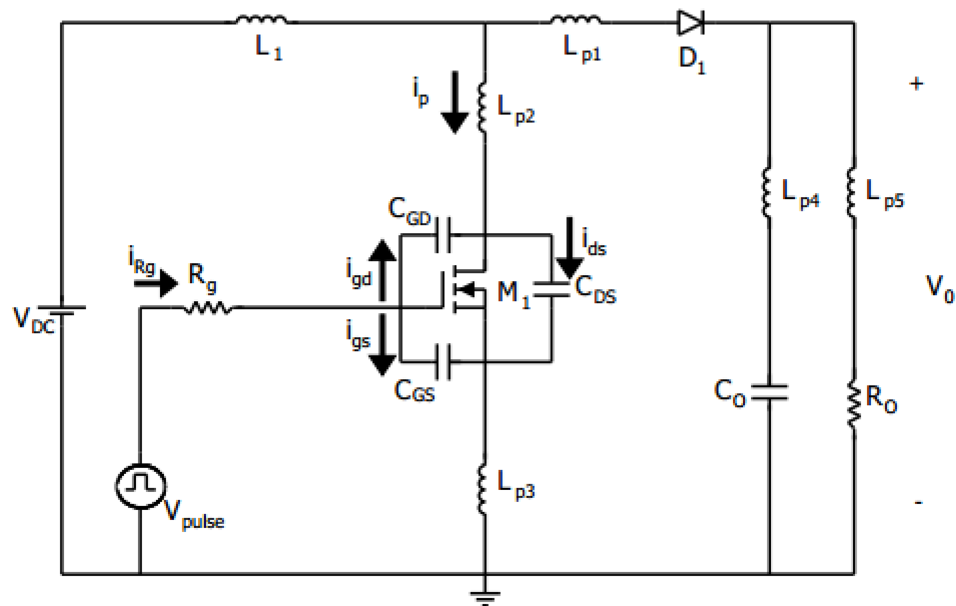


Figure 5.4 Circuit model with inductive wiring parasitic and MOSFET intrinsic capacitances. Here, passive component parasitics and layout stray capacitance are neglected.

Component parasitics are neglected in the analysis and inductive wiring parasitics are indicated with $L_{p1}, L_{p2}, L_{p3}, L_{p4}, L_{p5}$ in the Figure 5.4. The wires are modeled by using S-parameters in the simulation. Thus, wiring parasitics are taken into account in the analysis. The S-parameters are transferred to the MW DESIGN STUDIO (somehow advanced spice software) automatically in the complete software environment. Hence, the non-linear characteristics of the component models are also considered.

MOSFET model parameters that represent its dynamic behaviour have much importance on determining switching behaviour. MOSFET switching is the key point of the analysis. Overshoots and oscillations occur in the turn-on and turn-off transition intervals and observing these undesirable occurrence in the design stage can overcome failures.

Turn-on switching transition;

Stage 1: MOSFET is in cut-off region. Current flows from input through the diode to the output. Inductor current (i_L) decreases in this stage.

Stage 2: Eventhough gate signal is applied to the MOSFET, MOSFET is in cut-off region till the gate-source voltage value passes the treshold voltage level. Drain current is equal to zero volt, and diode continues to conduct. Input capacitance of the gate terminal when drain and source terminals are shorted is equal to the gate-source capacitance and gate drain capacitance, and charged up in this period as well. The gate-source voltage (V_{gs}) is equal to;

$$v_{GS} = V_{pulse}[1 - e^{-(t_1 - t_0)/\tau}] \quad (5.10)$$

$$\tau = R_g (C_{GS} + C_{GD}) \quad (5.11)$$

R_g is the sum of the gate pulse source resistance and internal resistance from gate pin to active gate region of the MOSFET.

The resistance of wires that wiring parasitics of diode and diode parasitic elements are effective in this stage and losses are caused by these parasitics like in the first stage.

Stage 3: When V_{GS} reaches the threshold level, MOSFET begins to work, drain current (i_d) starts to increase and drain- source voltage starts to decrease. Diode current continuous to conduct decreasingly until drain current reaches the load

current value. If the value of the i_d reaches the load current value before the drain-source voltage (V_{DS}) decreases to the ($V_{GS} - V_{treshold}$) level, MOSFET works in ohmic region. On the contrary, MOSFET works in saturation region.

Calculations for both saturation and ohmic regions:

(KCL at node G) => $$i_g(t) = C_{GS}\frac{v_{GS}}{dt} + C_{GD}\frac{v_{GD}}{dt} \tag{5.12}$$

(KCL at node S) => $$i_{DS}(t) + i_d(t) + i_{GS}(t) + i_s(t) = 0 \tag{5.13}$$

(KCL at node D) => $$i_p(t) = i_d(t) - i_{GD}(t) + i_{DS}(t) \tag{5.14}$$

Kirchoff's voltage law is applied to the circuit and equations are obtained as follow;

$$v_{GD} = v_{GS} - v_{DS} \tag{5.15}$$

$$-V_{pulse} + R_g i_g(t) + V_{GS}(t) + L_{p3}\frac{di_s(t)}{dt} = 0 \tag{5.16}$$

$$L_{p3}\frac{di_s}{dt} = V_{pulse} - R_g(C_{GS} + C_{GD})\frac{v_{GS}}{dt} + R_g C_{GD}\frac{v_{DS}}{dt} - v_{GS} \tag{5.17}$$

$$v_{DS} - L_{p1}\frac{di_D(t)}{dt} - V_0 + L_{p2}\frac{di_P(t)}{dt} + L_{p3}\frac{di_s(t)}{dt} = 0 \tag{5.18}$$

If the current of the inductor is assumed as constant, then;

$$v_{DS} - L_{p1}\frac{di_D(t)}{dt} - V_0 - L_{p2}\frac{di_D(t)}{dt} + L_{p3}\frac{di_s(t)}{dt} = 0 \tag{5.19}$$

$$(L_{p1} + L_{p2})\frac{di_D(t)}{dt} = v_{DS} - V_0 + L_{P3}\frac{di_s(t)}{dt} \tag{5.20}$$

Equations for drain current are different for the MOSFET whether it is in ohmic (linear) or saturation (active) region. When MOSFET is in active region, drain current is equal to;

$$i_d(t) = g_{fs}[v_{GS} - V_{th}] \tag{5.21}$$

g_{fs} : transconductance of the MOSFET

$$g_{fs} = \left.\frac{di_d(t)}{dv_{GS}}\right|_{V_{DS}=\text{constant}} \tag{5.22}$$

Although transconductance is a variable parameter, it is taken constant in the calculations.

$$C_{ds}\frac{dV_{ds}}{dt} = i_s - g_{fs}(V_{gs}(t) - V_{th}) - C_{gs}\frac{dV_{gs}(t)}{dt} \tag{5.23}$$

$$C_{gd}\frac{dV_{gs}(t)}{dt} = (C_{ds} + C_{gd})\frac{dV_{ds}(t)}{dt} + g_{fs}(V_{gs}(t) - V_{th}) - i_{in} + i_D(t) \tag{5.24}$$

When MOSFET is in ohmic region, it act as a voltage-dependent resistance (R_{ds_on});

$$R_{ds_on} = \frac{v_{DS}}{i_d(t)} \tag{5.25}$$

$$C_{DS}\frac{v_{DS}(t)}{dt} = i_s - \frac{v_{DS}}{R_{ds_on}} - C_{GS}\frac{v_{GS}}{dt} \tag{5.26}$$

$$C_{GD}\frac{v_{GS}}{dt} = (C_{DS} + C_{GD})\frac{v_{DS}}{dt} + \frac{v_{DS}}{R_{ds_on}} - i_{in} + i_D(t) \tag{5.27}$$

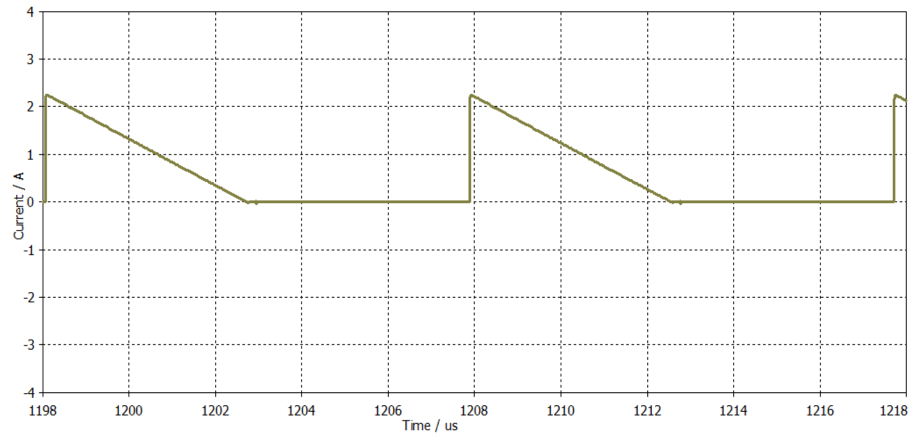
Stage 4: In the fourth stage, drain current is equal to the load current, and Drain-source voltage is equal to the approximately zero volt.

These analyses show that the parasitic capacitances of the MOSFET and parasitic inductances of the circuit effect the voltage and current values of the circuit components and turn-on delay time of the MOSFET.

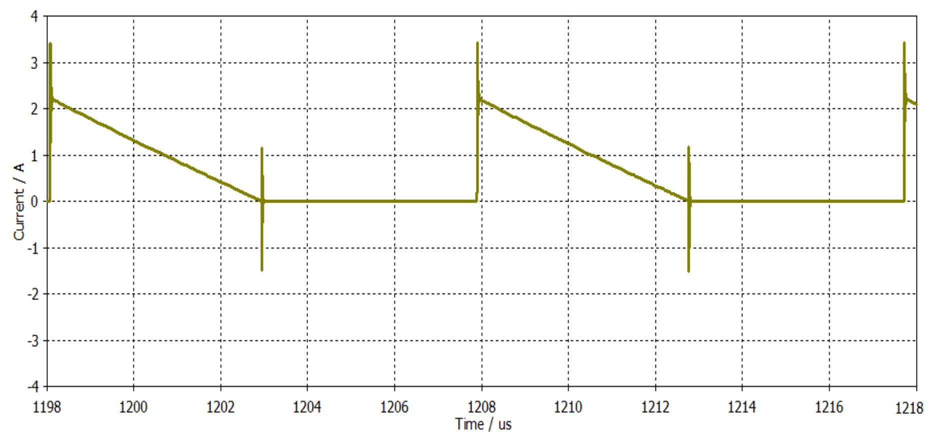
5.4 Comparison of Simulation and Experimental Results

5.4.1 Diode Current Waveform

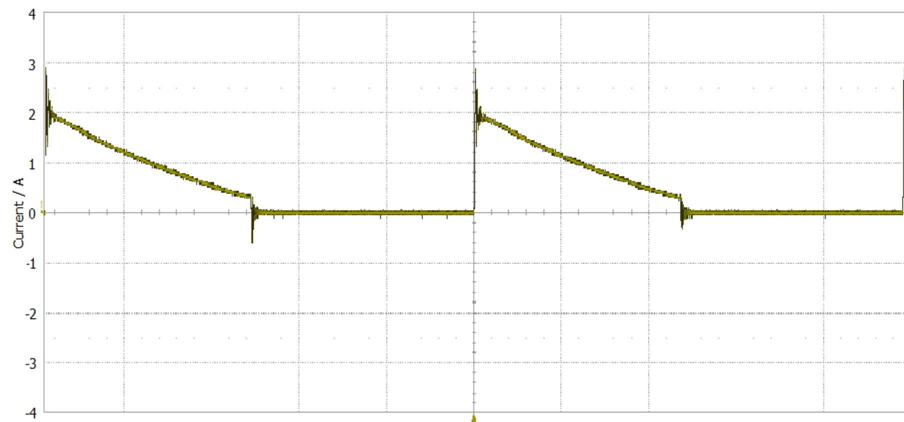
The peak value of the reverse recovery current depends on the operation mode of the converter due to forward current which flows across the diode right before the beginning of the reverse recovery. In the continuous mode, MOSFET turns on and then diode turns off and current of the diode forced to reach zero level. In that case; current can not be zero instantly because of the stored charge carriers in the p-n junction and stored in the bulk semiconductor material (Ma et al., 1993; Dhariwal, et al., 1992). On the other hand, in discontinuous mode, diode turns off and current of the diode is already in zero level when MOSFET turns on and consequently reverse recovery current does not occur. In the critical conduction mode, inductor current reaches almost zero level before MOSFET turns on. When MOSFET turns on and reverse voltage occurs across the terminals of the diode, diode current seen in Figure 5.5 begins to drop and becomes negative due to the excess charge carriers accumulated previously in the diode. The diode current continues to drop its peak negative value until the excess charge carrier concentration is equal to zero. This value is called reverse recovery current (Dhariwal, et al, 1992; Lauritzen, 1993). After reaching negative peak value, the slope of the current becomes positive. The diode voltage continues to increase to its maximum value and voltage is induced across the circuit inductance (Lutz et al, 2011). Finally, diode current drops to its leakage value, while diode voltage drops its steady state value. Reverse recovery current will not be zero but will not be greater than safe working level as well in critical conduction mode as seen in Figure 5.5.



(a)



(b)



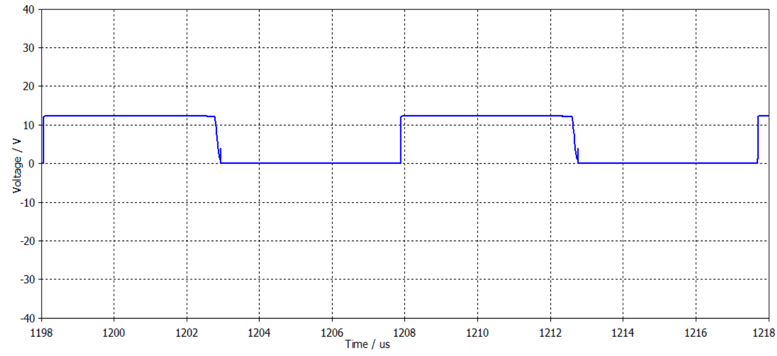
(c)

Figure 5.5 Diode current waveforms a) Simulation with SPICE (without taking into account physical connections parasitics) b) Co-simulation with CST MW STUDIO and DESIGN STUDIO c) Practical result, frequency is 101.5 KHz, 1 amp/div, 2 μs time/div

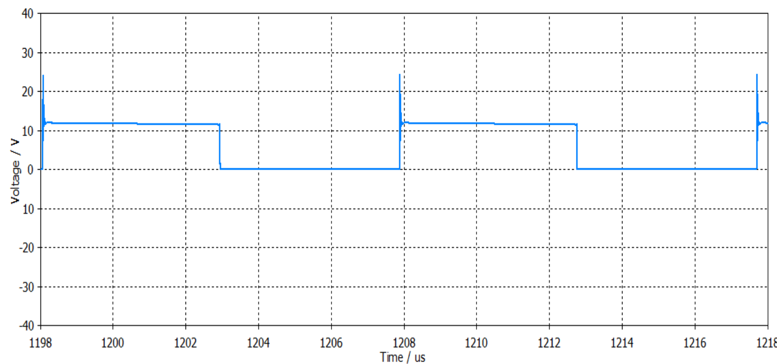
The disperancy of the reverse peak current values (in Figure 5.5) is possibly caused by the less accurate model parameters of the diode and the parasitic inductance of the drain of the MOSFET. Additionally, the series inductor of the copper path of the circuit reduces the slope of the current (di/dt), that is why the reverse recovery current value of the implemented circuit is lower than the reverse recovery current value of the simulation.

5.4.2 MOSFET Voltage Waveform

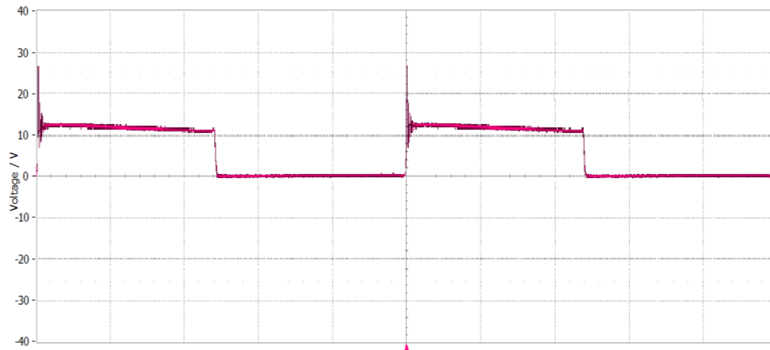
Switching performance of the MOSFET is important since voltage overshoot is occurred during turn-off. Ideally both MOSFET and diode transitions are occurred simultaneously, but in practice there is a little time delay due to the diode forward recovery time and this causes voltage spikes in the switching waveform. When MOSFET turns off, the voltage of the drain is expected to be equal to the output voltage. Although schottky diode is used, it is not fast enough to react to the voltage change instantly. MOSFET has intrinsic capacitances and these capacitances affect the oscillation during transitions in high frequency. And also, oscillations occur during transitions because of the loop inductance (He, Fu, Gao, Zhang & Zhou, 2012; Felic & Evans, 2003).



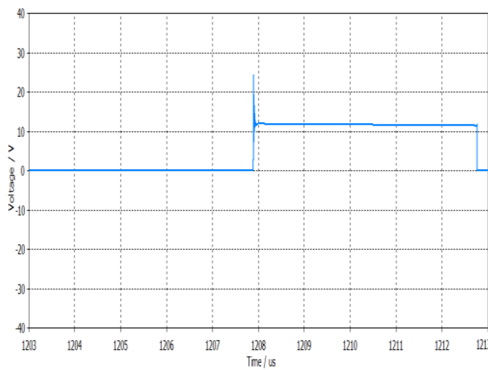
(a)

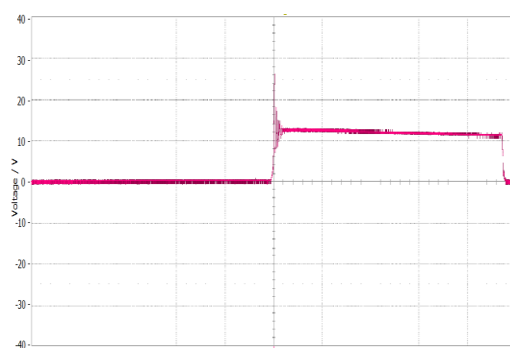


(b)



(c)





(d) (e)

Figure 5.6 MOSFET drain voltage waveforms a) Simulation with SPICE (without taking into account physical connection parasitics) b) Co-simulation with CST MW STUDIO and DESIGN STUDIO

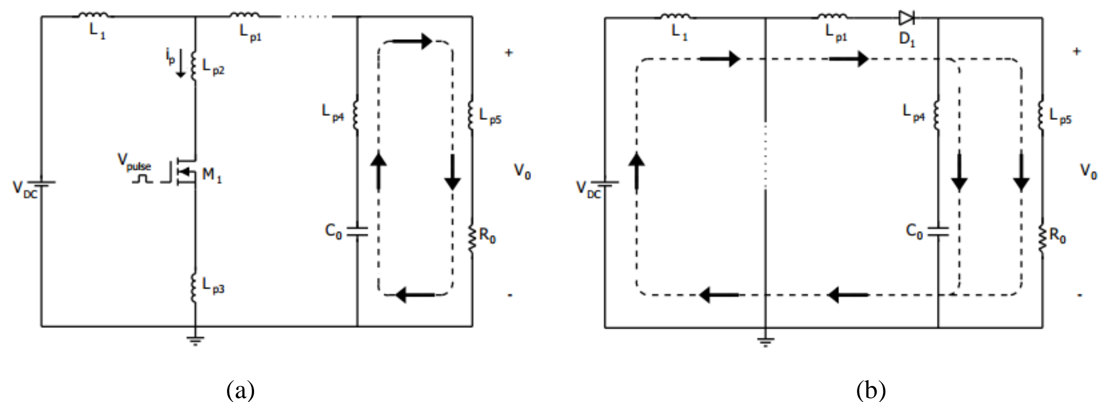
(wiring inductance taken into account by the software) c) Implementation result, 10 volt/div, 2 μs time/div d) Simulation with CST MW STUDIO for one period e) Implementation result for one period

Both simulation and implementation results of the drain voltage of the MOSFET are seen in Figure 5.6. Loop current rapidly increases during transitions and this causes an increment in the strength of the magnetic field since loop inductance stores energy in the form of a magnetic field. When the diode current decreases to zero then high frequency coupling effects disappear gradually.

5.4.3 Load Current Waveform

The complete path of the current flowing through the load changes according to be the ON or OFF case of the MOSFET switch. If MOSFET in the circuit is its ON state, current completes path through the output capacitor and load, otherwise, current completes path through the source, inductance, diode and load. Complete current paths of the load are given in Figure 5.7. Since the magnetic field passing through the area is proportional to the magnetic flux, current will affect the flux variation, too. To reduce the magnetic flux, internal current rises in the opposite direction in the circuit. This causes spikes in the output load during the transitions according to the Faraday's Law, additive inverse of the time rate of change of the magnetic flux linking a closed loop is equal to the induced voltage around that loop:

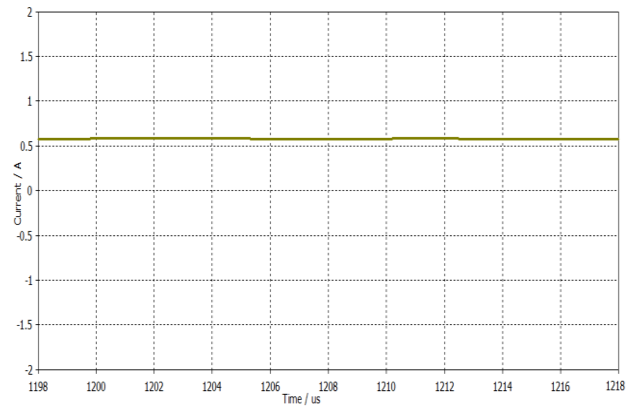
$$V_{induced} = -\frac{d\Phi}{dt} \tag{5.29}$$



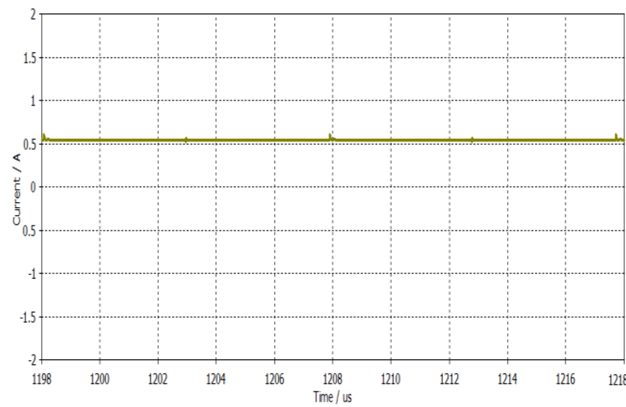
(a) (b)

Figure 5.7 Complete current path of the load when MOSFET switch is a) ON b) OFF

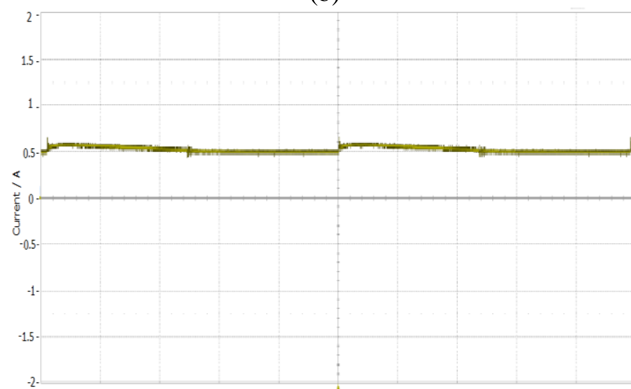
In that case, changing the physical paths of current in Figure 5.7 obviously should cause a change in magnetic flux and due to Faraday's Law this cause a voltage induction in the loops and superimposed current spikes as seen in Figure 5.8.b and Figure 5.8.c.



(a)



(b)



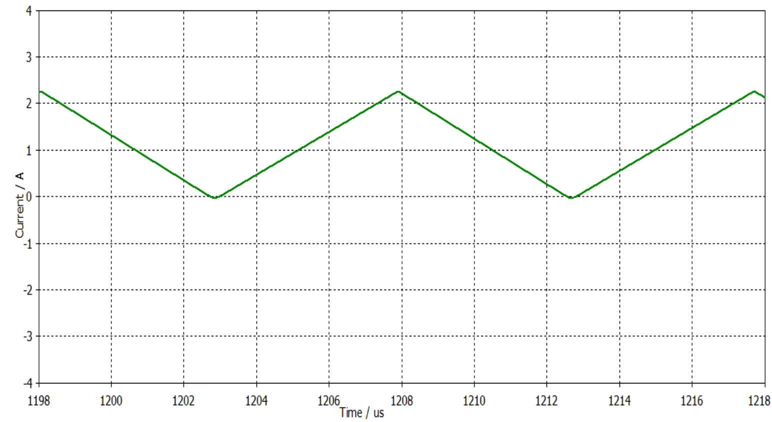
(c)

Figure 5.8 The load current waveforms a) SPICE simulation result (without considering physical connection parasitics) b) Co-simulation with CST MW STUDIO and DESIGN STUDIO (taking into account stray components) c) Measurement result , 1 amp/div (due to current probe scaling settings) , 2 μs time/div

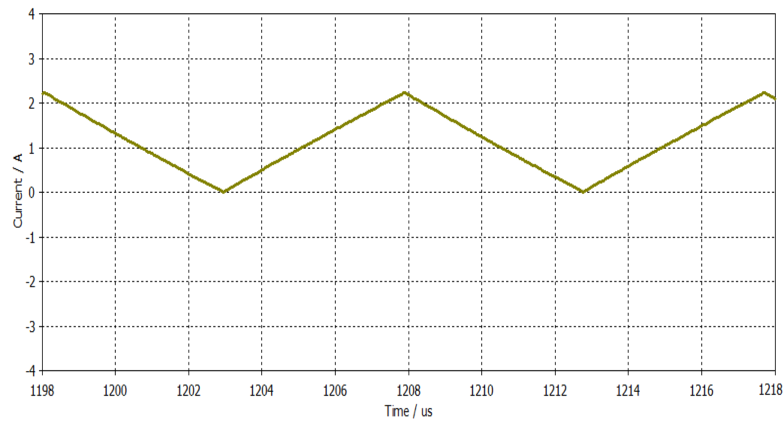
If the SPICE and co-simulation results of Figure 5.8.a and Figure 5.8.b are compared, it is seen that SPICE simulation result does not reflect the load current spikes as seen in Figure 5.8.b due to physical current path changes naturally is ignored in SPICE simulation. Apart from the spikes of the load current, the approximate load current is calculated as 0.6 Ampere for ideal case in Equation 5.8.

5.4.4 Inductor Current Waveform

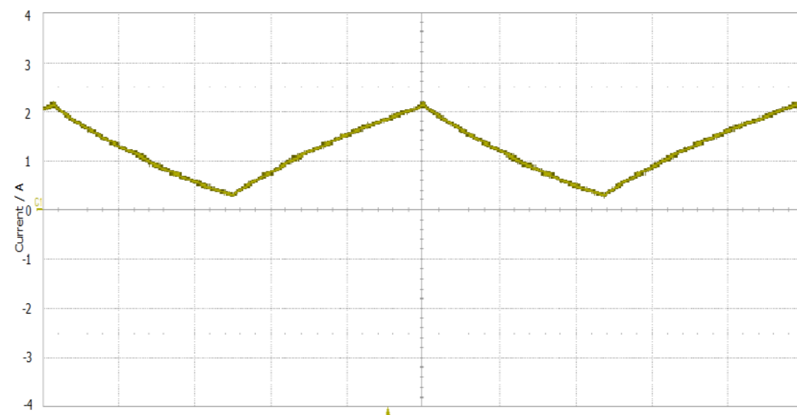
In the boost converter, the average inductor current flows into the load, while the ripple current flows into the output capacitor. If the inductor current is high, ripple component of the current is low and this causes an increase in the peak value of the output current. The inductor current waveform is seen in Figure 5.9. When practical and simulation inductor current results of Figure 5.9.b and 5.9.c are compared, it is seen that practical result of current waveform is not in the shape of straight lines since simulation waveform is in that shape. The reason is possibly that intrinsic resistance of wires, MOSFET on resistance are caused voltage drops and these drops lower the increase rate of inductor current. Ideally the minimum value of the inductor current is equal to 0.067 Ampere as calculated in Equation 5.6. Minimum value of the inductor current is observed 0.06 Ampere in simulation and 0.26 Ampere in implementation. Peak inductor current value is calculated 2.33 Amperes in ideal calculation without losses as in Equation 5.7, in CST MW STUDIO program co-simulation result is equal to 2.127 Amperes and in implementation peak inductor current is equal to 2.14 Amperes.



(a)



(b)



(c)

Figure 5.9 Inductor current waveforms a) Simulation with SPICE (without taking into account physical connections parasitics) b) Co-simulation with CST MW STUDIO and DESIGN STUDIO c) Implementation result, 1 amp/div, 2 µs time/div

Simulation process assumes inductor core material has linear B-H characteristics; however in physical world Ferro-magnetic materials have non-linear B-H

characteristics. Non-linear core material characteristics are not included yet into modern simulation packages for example used in this study.

CHAPTER SIX
SNUBBER CIRCUIT DESIGN FOR MITIGATION OF MOSFET TURN-OFF OVERSHOOT VOLTAGE IN A BOOST CONVERTER

Snubber circuits are generally used in a switch mode power conversion system to make the system to be more reliable. The basic purpose of a snubber circuit is to absorb energy from the stray reactive elements (for example circuit interconnect stray inductors) in the circuit during switching so as to obtain circuit damping, controlling the rate of change of voltage or current or suppressing voltage overshoot (Severns, 2008). In the absence of snubber circuits, the switching elements may be burn, and the circuit can be damaged. Different snubber circuits consisting of passive components have been recommended to mitigate the spikes in literature (Peng, Su & Tolbert, 2004; He, Chen, Wu, Deng & Zhao, 2006; Li, Chung & Sung, 2010; Yun, Choe, Hwang, Park & Kang, 2012). Some active clamp snubber circuits are also recommended in literature (Elasser & Torrey, 1996; Lim, Williams & Finney, 2011). Both active and passive snubber structures have advantages and disadvantage according to the usage purposes. However, using active snubber structure in design increases the complexity of the circuit further. A passive snubber structure is used to mitigate the turn-off overshoot voltage of the MOSFET switch in this chapter of the thesis. Actually, when a snubber circuit is inserted, there will be some losses during the charging or discharging of the snubber capacity. Instead of RC circuit, RCD Snubber circuit is preferred. If diode is not connected parallel to the resistor, time delay can occur and efficiency of the snubber is reduced.

The Boost converter circuit's simulation and implementation results in critical conduction mode were given in the fifth chapter. The same converter circuit is analyzed with 6.8 Ω load resistance in continuous conduction mode in this chapter. Overshoot and oscillation waveforms of the MOSFET during turn-off transitions are observed and a solution is suggested for mitigating these overshoot voltages. The suggested solution includes RCD snubber circuit and tested in both simulation and experimental works as well. The performance of the snubber circuit is scrutinized.

Beside the Power MOSFET and diode forward recovery characteristics, stray inductances and parasitic capacitances have effective roles in turn-off transition of the MOSFET as told in the fifth chapter. For this aim, full-wave modeling technique is again used in this chapter. Thus, whole parasitic effects of the wirings are taken into account during simulation.

6.1 RCD Snubber Circuit and Application for the Purpose of Snubbing Overvoltage

The stored energy in the parasitic circuit elements during transition is dissipated via the path of the snubber circuit. A basic RC snubber circuit is necessary but may not be sufficient in some cases, since a diode should be connected parallel to the snubber resistor as seen in the circuit of Figure 6.1. When MOSFET turns-off, snubber diode will be forward biased, due to current carrying MOSFET drain wiring stray inductance at that instance. Drain current chooses the non-resistance path so it flows across the diode and charged the snubber capacitor. If there were no diode parallel to the snubber resistor in use, capacitor is charged over the resistor and time delay would occur. By the usage of the RCD snubber circuit seen in Figure 6.1, capacitor will be charged without any delay and this provide to the MOSFET voltage to reach the steady state value with decreasing overshoot. Eventually, switching losses are decreased during the switching too. When MOSFET turns-off huge power dissipation occurs due to the multiplication of high voltage and current of the MOSFET without snubber. For this reason, snubber circuit is connected for reducing the rise time of the drain voltage, by a compatible charging time with the decreasing time of the drain current to reach the zero value. When MOSFET turns on, the snubber capacitor discharges through the snubber resistor.

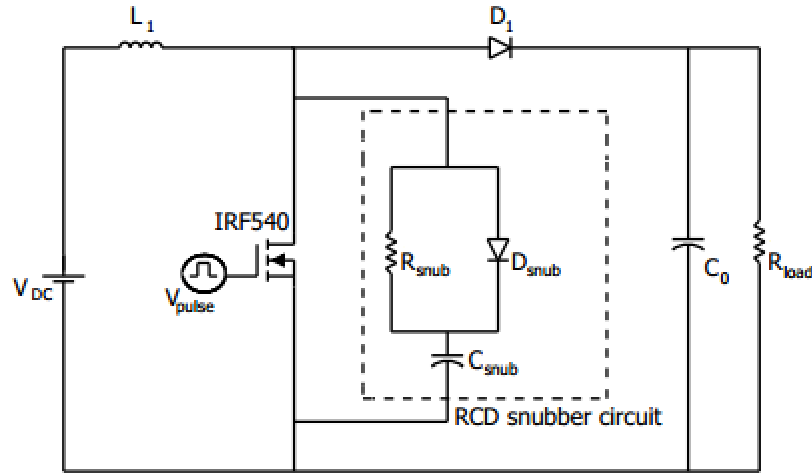


Figure 6.1. Boost converter with turn-off snubber circuit

A RCD Snubber Circuit added to the boost converter is seen in Figure 6.1. The stray inductance of the path that connects the diode D_1 to the MOSFET may cause voltage spikes at turn-off the MOSFET. In addition to this, forward recovery voltage parameter of the fast power diodes may get values of around 60 Volts due to data sheets, somehow this phenomenon may also have an effect to increase turn-off voltage spike magnitudes accross the MOSFET switch.

The snubber capacitor voltage should be increased to the two times of the DC voltage level and drain current decreases to the zero value at the same time. Hence, the capacitor is chosen as follow (Pressman, Billings & Morey, 2009);

$$C_{snub} = \frac{I_p}{2}\frac{t_f}{2V_{DC}} \tag{6.1}$$

I_p = peak current of the MOSFET

t_f =fall time of the MOSFET to its steady state value

From Equation 6.1, capacitor value is calculated as:

$$C_{snub} = \frac{0.48*10^{-6}}{2}\frac{4.42}{2*6} = 88.4nF \tag{6.2}$$

C_{snub} is chosen as 100nF, which is a standard resistor value and approximate value to the calculation.

Snubber resistor is effective during turn on interval, since the snubber capacitor is discharged through this resistor. If there is not any snubber resistor or low valued one is used, the energy stored in the snubber capacitor can be dissipated through the MOSFET during turn-on. And this can cause extra losses and failures. The discharging time of the snubber capacitor should be very low compared to the switching time. And, snubber resistor can be calculated as follow (Pressman, et al, 2009);

$$t_{on(\min)} = 3R_{snub}C_{snub} \tag{6.3}$$

$t_{on(\min)}$ = minimum transition time of MOSFET

Snubber resistor is obtained from Equation 6.3 as;

$$R_{snub} = \frac{t_{on(\min)}}{3C_{snub}} = \frac{3\times10^{-6}}{3\times100\times10^{-9}} = 10\Omega \tag{6.4}$$

These values may not be optimum values in terms of power loss but their performance on mitigation of spike and safety working is appropriate for the realized circuit. A schottky diode (MBR1045) is used as a snubber diode in the experimental set-up. The switching frequency of a Boost converter is selected as 100 kHz, but the frequency content during transition is very high (almost in MHz range) compared to the switching frequency. This high frequency is required to observe all layout effect along with the component's characteristics in analysis. For this purpose, simulation of the circuit is performed with CST MW STUDIO full wave simulation program like in the fifth chapter.

The layout scheme of the Boost converter drawn in CST MW STUDIO is same as seen in Figure 5.2. Snubber circuit is not needed to define in the layout since the snubber elements are connected as close as possible to the MOSFET. Beside the

effect of the paths, behavior of the components should have to include to the circuit design as well and they are connected to the transferred layout block schematic in CST DESIGN STUIO. MOSFET and diode model parameters given in their manufacturer web sites are used. Apart from these, inductive effect of the load resistor should be considered. The high frequency behaviour of the resistor is measured via the implemented resonant structure seen in Figure 6.2.

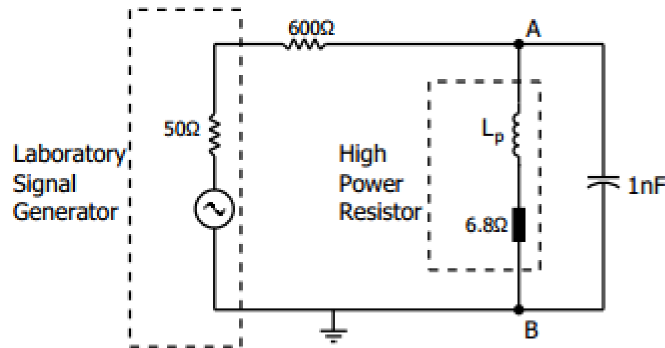


Figure 6.2 Test circuit designed for determining experimentally the load parasitic inductance value

The technique used here is known as a hands-on experiment and given in reference Rudy Severnes (2008). The idea is that beneath the experiment is to construct a resonant circuit by connecting a capacitor in parallel to the load resistor. The unknown stray inductance (L_p) seen in Figure 6.2 along with the capacitor connected constructs a parallel resonant circuit. Adding a high valued resistor in series to laboratory signal generator converts it a sinusoidal current source. As known, when a parallel resonant circuit is driven with a sinusoidal current source, the sinusoidal voltage magnitude across the parallel resonant circuit between A and B nodes gets its maximum value. In the experiment signal source frequency is gradually increased or decreased to seek maximum voltage and then determined resonant frequency (f_{res}). Once this f_{res} determined, the stray inductance value could be determined by using the formula;

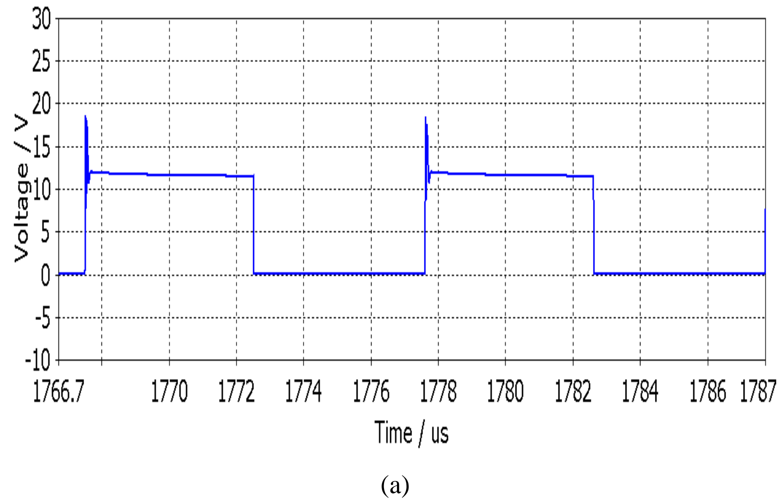
$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \Rightarrow L_{stray} = \left(\frac{1}{2\pi f_{res}}\right)^2 C = 0.42\mu H \tag{6.4}$$

During the experiments it is noticed that this procedure may fail when constructed series resonant circuits rather than constructing parallel resonant circuit using L_{stray} (to be determined) and externally connected capacitor C. The reason eventually concluded is that the inherent output resistance of the signal source. As known generally laboratory signal sources have a 50 Ω output resistance value and this resistance (50Ω) inevitably introduced into series resonant circuit and lowers the quality factor of the circuit and sometimes resonant peaks disappeared. For this reason a parallel resonant phenomenon is used in the experiments towards determining L_{stray} value.

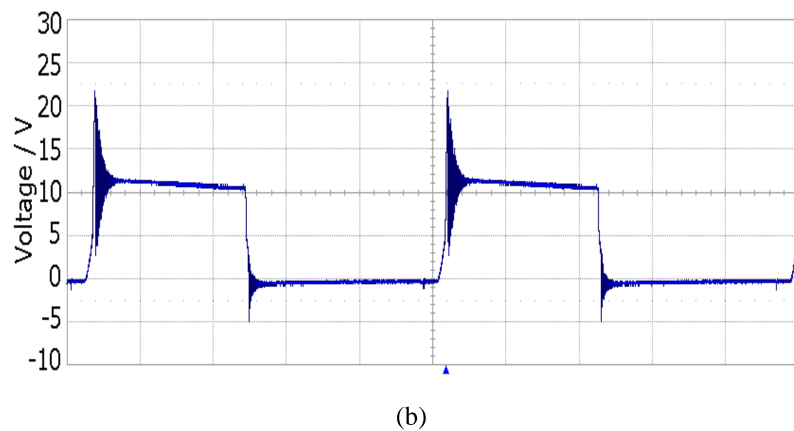
Since the resistor used in CST DESIGN STUDIO is an ideal resistor, a $0.42\mu H$ valued inductor is added to the load resistor in series to represent the actual inductive effect.

6.2 Simulation and Experimental Results Revealing Snubber Circuit Effectiveness

Simulation and experimental results of the MOSFET Voltage waveforms of the Boost converter with and without snubber circuits are compared. Despite the duty cycle is equal to the 0.5 and the theoretical output voltage is expected to be 12 Volt, it is equal to approximately 11.5Volt in both simulation and experimental circuits. The difference is possibly caused by voltage drops across the MOSFET and diode elements in addition to parasitic resistances associated to other circuit elements.



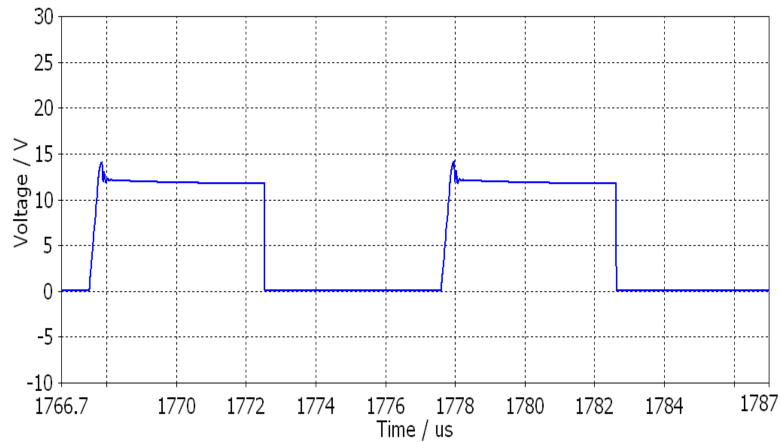
(a)



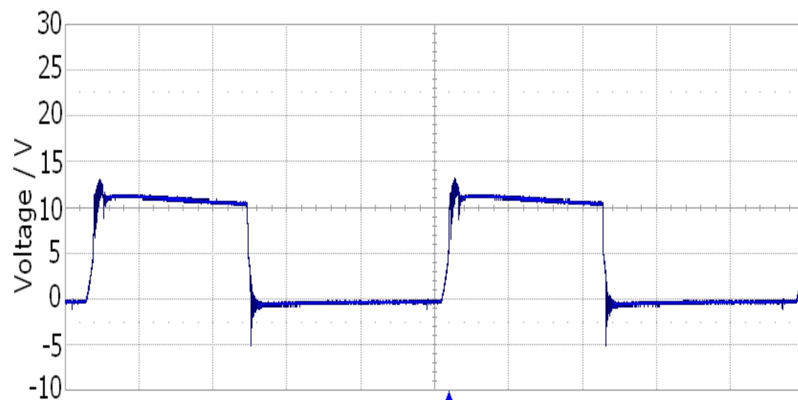
(b)

Figure 6.3 MOSFET drain-source voltage waveforms without snubber circuit a) simulation result b) experimental result 5volt/div, 2µsec/div

Simulation and experimental MOSFET Voltage waveforms without snubber are seen in Figure 6.3. It is measured that the rapid voltage increasing between drain-source terminals is up to 22 Volts, approximately twice of the MOSFET voltage in the circuit without snubber during turn-off transition. Oscillations of the implementation waveform are higher than the simulation results, since the component parasitic are not taken into account in the simulation results. Also the drain and source lead inductances are not considered in the simulation model of the MOSFET.



(a)



(b)

Figure 6.4 MOSFET drain-source voltage waveforms with snubber circuit a) simulation result b) experimental result 5volt/div, 2µsec/div

Voltage waveforms of the MOSFET drain- source terminals with snubber circuit are seen in Figure 6.4. After the snubber circuit is connected, the voltage spike between drain source terminals of the MOSFET decreased to one or two volts (Figure 6.4.b) from approximately 6 Volts and this shows us the instant value of the overshoot voltage decreased from approximately 22 Volt levels.

When figures without snubber circuit (Figure 6.4) and with snubber circuit (Figure 6.5) are compared, it is seen that the designed snubber circuit is sufficient and the semiconductor switching elements could be operated safely. In conclusion, the results show that RCD snubber circuit seen in Figure 6.1 is the key parameter for obtaining low overshoot voltage of the MOSFET during turn-off.

CHAPTER SEVEN
EXPERIMENTAL WORKS ON MOSFET DRIVER (BUFFER) CIRCUIT

There are several methods for amplifying the output current and obtaining enough driving current for power switching elements. Totem pole circuits, Common Emitter Amplifiers, BJT Emitter follower and CMOS Buffer Circuits are widely used. All buffer circuits have advantages and disadvantages. CMOS Buffer circuits have better performance regarding to mitigate shoot through currents and obtain non-inverting outputs. Performance of the driver circuit design is not only depends on the appropriate elements, but also depends on the gate drive resistance, wiring parasitic of the PCB layout and the characteristic properties of the MOSFET. It is ensured to observe and overcome probable problems if all these are considered in circuit analysis at design stage. Although the precise waveforms can not obtained in the switching circuits, obtaining accurate analytical results give an insight into the circuit working principle. These accurate results can only be obtained by considering the effect of both element characteristics and parasitics caused by the connecting wires for analysing the circuit behaviour and losses, especially during switchings (Xiao, Shah, Chow, Gutmann, 2004; Ren, Xu, Zhou & Lee, 2006; Eberle, Zhang, Liu & Sen, 2009; M. Rodriguez, A. Rodriguez,Miaja, Lamar & Zuniga, 2010; Wang, Chung& Li, 2013). The effect of the parasitic elements on the switching performance are investigated with analytical model for buck converter (Chen, Boroyevich, Burgos, 2010; Eberle, Zhang, Liu & Sen 2008). The effects of the parasitic elements and gate drive resistance were also investigated with analytical model (Wang et al., 2013; Zang, Eberle, Yang, Liu & Sen, 2008).

In this chapter, a detailed new analytical model extracting from datasheet of the MOSFET for the CMOS buffer circuit is proposed to observe the ringing of the capacitive input of the MOSFET during the transition of the output of the driver stage from positive voltage level to the zero voltage level. This buffer circuit is suggested in the literature by Xue, Wang, Tolbert & Blalock (2013). Along with the analytical model analysis, simulation method is performed by using CST Design Studio software, and finally implementation methods are applied to the proposed

circuit and results of the circuit are compared. Additionally, the same implementation circuit is set up with different gate drive resistances and checked against the performance of the circuit. Analytical model is solved with MATLAB by using a type of iterative method called Runga Kutta Method for developing a different point of view. Also, the analysis is fulfilled by using first order differential equations, since discontinuties for the currents occurs while mading analysis with second order differential equations in MATLAB.

7.1 Topology of the CMOS Buffer Circuit

7.1.1 Equivalent Circuit Model of the CMOS Buffer Circuit

CMOS buffer structure proposed in (Xue et al., 2013) is demonstrated in the laboratory and gives excellent switching times. The ringings however was high and by analyzing and simulating this circuit topology it is aimed to understand the circuits' operation better and possibly mitigate the transition ringings. Although the switching times are very low, the transitions are still can not be simultaneously and turn on delay time occurs during switching in implementation. The effects of the turn-on delay time of the switches depends on the gate drive resistance, input capacitance of the MOSFETs and wiring inductance of the circuit. In this chapter, all these effects are investigated with a proposed analytical model, simulation and experimental results. In fact, gate drive resistance is especially emphasized during the transition of the input from low to high case. Gate resistance allied with gate-source capacitance affects the charge and discharge times of the MOSFETs. This effect plays an important role in determining the delay time of the MOSFET to become on.

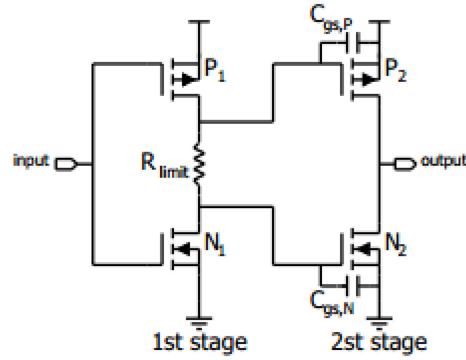


Figure 7.1 The partially analyzed CMOS buffer circuit, the transistor N_2 behavior is analyzed for output transition high to low, and load is assumed a simple capacitor element with an initial charge of Q (Xue et al.,2013)

In Figure 7.1, P_1 and P_2 are P-channel MOSFETs and N_1 and N_2 are N-channel MOSFETs, where $C_{gs,N}$ and $C_{gs,P}$ are the internal gate source capacitance of the MOSFETs. R_{lim} is limiting resistor. The circuit is divided into two stages for obtaining non-inverting amplified output. When input voltage of the circuit seen in Figure 7.1 becomes high, P_1 goes to turn-off state and N_1 becomes on. Therefore N_2 becomes off and P_2 becomes on. On the other hand, when low voltage (below threshold voltage level) is applied to the input of the circuit, N_1 becomes off and P_1 becomes on with a delay time determined by the time constant $\tau_1 = R_{\lim} C_{GS,P}$. Consequently, P_2 becomes off and N_2 becomes on after a delay time determined by time constant $\tau_1 = R_{\lim} C_{GS,N}$. These time delays are provided by the resistor R_{lim} together with the equivalent gate capacitances of the MOSFETs starting to conduct. In this paper, the reasons of the turn on delay and especially the effect of the gate drive resistance are investigated when output stage becomes zero.

The output load is assumed to be a constant capacitance of the driven MOSFET by this buffer circuit. Although this capacitance value changes with the time during transition, it is here assumed to be constant as 10 nF for simplification purpose. Also, the output capacitor keeps the DC voltage constant at the transition moment of the P_2 from on to off, and N_2 from off to on.

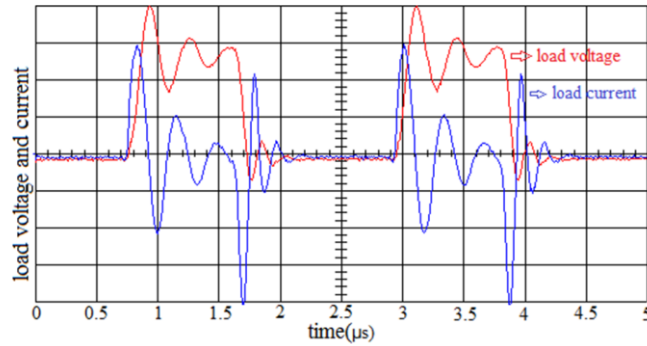


Figure 7.2 Practical waveforms of MOSFET driver (buffer) circuit, output voltage waveform 5 volt/div (red one), load current waveform measured with P6022 current probe 1A/ div (blue one)

This circuit is demonstrated in the laboratory and gives excellent switching times as seen in Figure 7.2 even though the switching frequency is about 450 kHz. In Figure 7.2, the circuit is capable of obtaining acceptable driving waveforms up to 800 MHz with a load consisting of a 10nF ceramic capacitor again. The ringings however were high and by analyzing and simulating this circuit topology we aimed to understand the circuits' operation better and possibly mitigate the ringings.

7.1.2 Equivalent Circuit Model of the Buffer Circuit for the High to Low Input Transition

When upper side MOSFET of the second stage (P_2) is turned off, which is expected to be very fast since no or very low gate driving resistance of $P_{2,}$ lower side MOSFET (N_2) is expected to turn on later and somehow slowly since R_{lim} is the resistor used for limiting the shoot-through current and acts as a gate driving resistance for P_2 as well.

A simplified equivalent circuit for the buffer output considering only high to low transition with parasitic elements could be constructed as seen in the Figure 7.3. In this figure, the transistor shown in Figure is N_2 MOSFET of the previous circuit of Figure 7.1. Clock pulse with 100 kHz frequency is applied to the input of the MOSFET driver of the circuit. This circuit was implemented with IRF540Z power MOSFET. A driver IC is used to drive the circuit of Figure 7.1. The input signal of this pre-driver is provided by a laboratory signal source via a twin cable whose

characteristic impedance (Z_0) is around $220\,\Omega$. To suppress the ringing of the cable it is loaded with a resistor (R_p) at far end as seen in Figure 7.3 and value of this resistor is selected as $220\,\Omega$. Stray inductance can be calculated as given in literature (Ardizzoni, 2005) and are chosen 8nH per cm for the analyzed circuit layout. The detailed parameters of the MOSFET related to turn-on and turn-off behavior have been obtained from the datasheet.

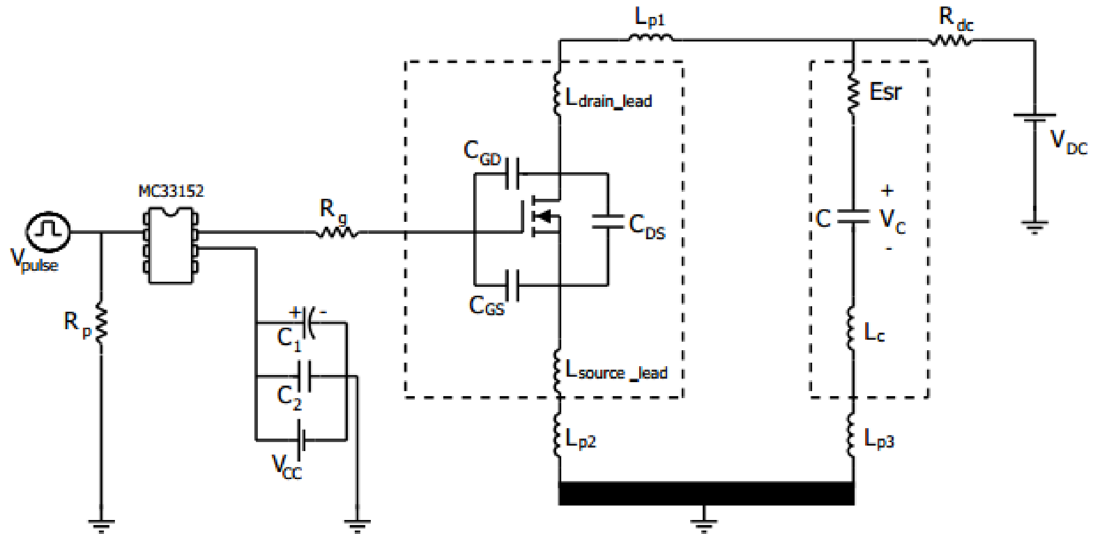


Figure 7.3 Output of the driver stage's equivalent circuit model, Buffer circuit 2nd stage's model for its output transition 1 to 0

L_{source_lead} : internal source inductance;

L_{drain_lead} : internal drain inductance;

R_g : driver external resistance + driver internal resistance;

L_{p1} : parasitic inductance of the wire from drain lead to the capacitor positive lead;

L_{p2} : parasitic inductance of the wire from source lead to the ground;

L_{p3} : parasitic inductance of the wire from capacitor negative lead to the ground;

E_{sr} : equivalent series resistance;

L_c : equivalent series inductance.

V_{CC} : DC supply voltage

C_1, C_2 : DC supply capacitors

The circuit shown in Figure 7.3 is implemented by using surface mount components in order to reduce the layout parasitics and thus electromagnetic interference and losses. Output capacitor's frequency characteristic is considered while performing the analysis. DC voltage source is connected via a resistor (R_{dc}) so as to generate initial dc voltage value for the output capacitor. The value of this resistor is chosen to be $250\,\Omega$.

7.2 Proposed Analytical Model of the CMOS Buffer Circuit

7.2.1 Parameters Used in the Proposed Analytical Model

In conventional circuit analysis, the circuit parasitics and component characteristics especially MOSFET characteristics are not taken into account. However, they are the main causes of the overshoots and oscillations during transitions. The circuit should be analyzed with these parameters and effect of the parameters give a point of view to mitigate the oscillations and failures.

Some assumptions are made for the proposed analytical model. These assumptions are as follows;

- Forward transconductance and drain source resistance of the MOSFET are taken constant (Chung& Li, 2013). In fact, drain source resistance is varied with gate-source voltage of the MOSFET as shown in the manufacturer's data sheet (International Rectifier, n.d.).
- Actually, it is seen that reverse recovery effect is a negligible parameter in this circuit. In fact, the cause of the oscillations is the leakage result of the inductance in the circuit. This situation limits the reverse recovery current. Additionally, the current which flows over parasitic diode is again limited because MOSFET's channel region is in its conduction mode. Because of

these two reasons, reverse recovery current is not taken into account. Also the simulation and experimental results prove that this assumption is correct.

- Layout stray capacitances and stray resistances are neglected.
- Parasitic inductance for the MOSFET gate path is neglected. Since driver integrated circuit is placed to the gate resistance as close as possible to minimize the oscillations caused by this parasitic inductance.

Characteristic properties of the components are given in the data books of the manufacturers (Appendix C). Analytical model is derived in consideration of these characteristic properties.

Forward transconductance is the variation of the drain current with variation of a gate-source voltage while keeping the drain-source voltage constant and given in Equation (5.2).

And, obtained from V_{GS} and I_d graph. For cut off region, g_{fs} is taken zero value since no current is flowing through the drain of the MOSFET.

Drain-source resistance (R_d) of the MOSFET is obtained from drain to source current graph.

In the model circuit (Figure 7.3), the capacitor C is represented with its parasitic resistance and inductance.

Table 7.1 Parameters and abbreviations used in analysis

Parameters	**Abbreviations of the Parameters**	**Value**
Switching frequency	f_{sw}	100kHz
Pulse Voltage	V_{pulse}	20Volt
Electrostatic Resistance of Capacitive load	E_{sr}	0.18Ω
Electrostatic Inductance of Capacitive load	L_C	1nF
Capacitive Load	C	10nF
Gate-Drain Capacitance of MOSFET($V_{DS} = 23Volt$)	C_{GD}	111pF
Gate-Drain Capacitance of MOSFET($V_{DS} = 23Volt$)	C_{GS}	1770pF
Gate-Drain Capacitance of MOSFET($V_{DS} = 23Volt$)	C_{DS}	166pF
Gate-Drain Capacitance of MOSFET($V_{DS} = 1Volt$)	C_{GD2}	330pF
Gate-Drain Capacitance of MOSFET($V_{DS} = 1Volt$)	C_{GS2}	1770pF
Gate-Drain Capacitance of MOSFET($V_{DS} = 1Volt$)	C_{DS2}	400pF
Forward transconductance (cut-off region)	g_{fs}	0
Forward transconductance (saturation region)	g_{fs1}	1S
Internal Gate Resistance	R_{g_int}	6Ω
Internal Drain Inductance	L_d	7.5nH
Internal Source Inductance	L_s	4.5nH
Threshold Voltage of MOSFET	V_{th}	3.2Volt
MOSFET Drain-Source on Resistance	R_{ds_on}	0.15Ω

7.2.2 Proposed Analytical Model for the Switching Behaviour of the MOSFET with capacitive load

The switching behavior of the circuit seen in Figure 7.3 is solved by using analytical model when the lower side MOSFET (N_2) turns on. Analytical approach is solved by using MATLAB/Simulink program (Appendix D). All equations are defined and the graphics of figures are plotted by this program. High order equations are reduced and obtained in first order to overcome the discontinuities seen in the current waveforms.

In the analytical model the turn-on switching transition is determined in three intervals:

Interval 1: Eventhough gate signal is applied to the MOSFET, it is in the cut-off region until the gate-source voltage value passes the treshold voltage level. Drain voltage is equal to capacitor’s initial voltage, and no current flows. Input capacitance of the gate terminal begins to charge up in this period. When drain and source terminals are shorted, input capacitance is equal to the gate-source capacitance and gate drain capacitance. In conventional models, if the internal source and drain inductances and parasitic inductances are neglected, the gate-source voltage (V_{GS}) is equal to the;

$$V_{GS} = V_{pulse}\left[1 - e^{-(t_1 - t_0)/\tau}\right] \qquad \tau = R_g(C_{GS} + C_{GD}) \tag{7.1}$$

where; $R_g = R_{gate_resistance} + R_{g_int}$ and R_{g_int} is the internal resistance of the MOSFET.

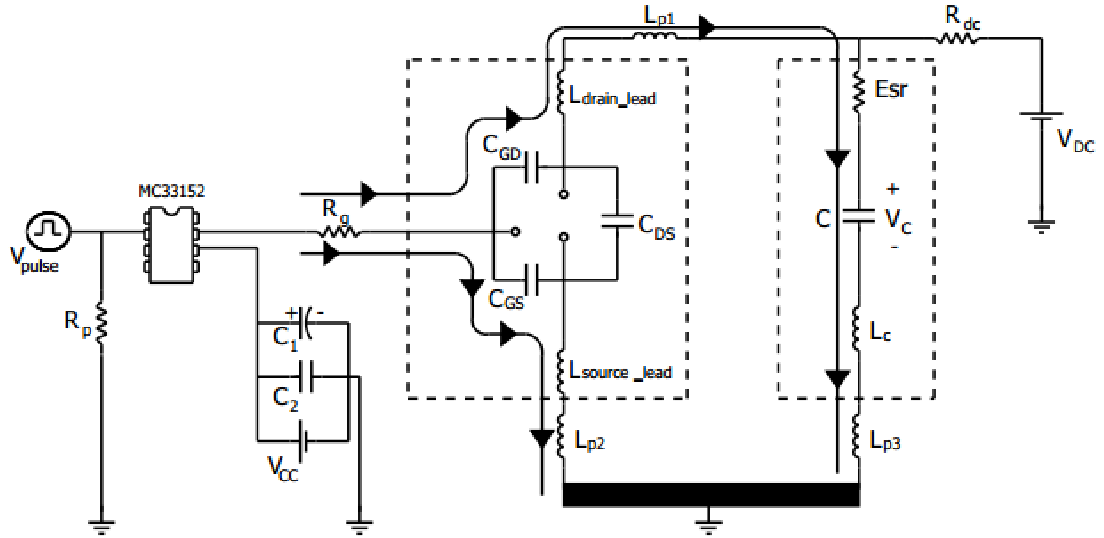


Figure 7.4 Current flowing paths when MOSFET is in cut-off region.

Equation 7.1 is taken for calculating the turn-on delay time in conventional models, but inductances should be taken into account even if the circuit is in cut-off region. The reason for this is the necessity of the closed loop path of the current during charging of the gate-source capacitances. Current flowing paths are seen in Figure 7.4. If these inductances are not considered, turn-on time of the MOSFET will be smaller than the exact value. Transconductance for cut-off region is taken zero and the equations given in the second interval is applied to the MOSFET to obtain accurate results for cut-off region.

Interval 2 and Interval 3: When V_{GS} reaches the threshold level, MOSFET begins to work, drain current (i_d) starts to increase and drain-source voltage starts to decrease. Capacitor voltage starts to decrease from its initial voltage value as well.

When Kirchoff's Current Law is applied to the gate, drain and source of the MOSFET, current equations can be written as follow;

$$i_g(t) = C_{GD}\frac{dv_{GD}}{dt} + C_{GS}\frac{dv_{GS}}{dt} \tag{7.2}$$

$$i_C(t) = (i_{GD}(t) - i_d(t) - i_{DS}(t)) \tag{7.3}$$

$$i_{DS}(t) + i_{GS}(t) + i_d(t) - i_L(t) = 0 \tag{7.4}$$

where, $i_L(t) = i_g(t) - i_C(t)$

When Kirchoff's voltage law is applied to the circuit, voltage equations are obtained as;

$$v_{GD} = v_{GS} - v_{DS} \tag{7.5}$$

$$-V_{pulse} + R_g i_g(t) + v_{GS} + L_S \frac{d(i_L(t))}{dt} = 0 \tag{7.6}$$

$$-V_c - R_c i_c(t) + L_d \frac{di_c(t)}{dt} + v_{DS} + L_S \frac{d(i_L(t))}{dt} = 0 \tag{7.7}$$

where,

$$L_s = L_{source_lead} + L_{p2}$$

$$L_d = L_{drain_lead} + L_{p3} + L_c$$

By differentiating the Equation 7.5 and putting into Equation 7.2, gate current is obtained as;

$$i_g(t) = (C_{GD} + C_{GS})\frac{dv_{GS}}{dt} - C_{GD}\frac{dv_{DS}}{dt} \tag{7.8}$$

Voltage across L_d and L_s are written by using Equations 7.5, 7.6 and 7.7 as follows;

$$L_S \frac{d(i_l(t))}{dt} = V_{pulse} - \left[R_g(C_{GD} + C_{GS})\right]\frac{dv_{GS}}{dt} - \left[R_g C_{GD}\right]\frac{dv_{DS}}{dt} - v_{GS} \tag{7.9}$$

$$-L_S \frac{d(i_L(t))}{dt} = -V_c - R_c i_c(t) + v_{DS} + L_d \frac{di_c(t)}{dt} \tag{7.10}$$

Equations given above are valid for both saturation region and ohmic region. The behaviour of the drain current is a distinctive parameter.

7.2.2.1 Distinctive Features for Interval Two:

When $V_{GS} \geq V_{th}$ and $V_{DS} \geq V_{GS} - V_{th}$, MOSFET is in saturation region and acts as a current source. Drain current of the MOSFET can be written as;

$$i_d(t) = g_{fs}[v_{GS} - V_{th}] \tag{7.11}$$

Figure 7.5 Closed loops of the circuit when MOSFET is in saturation region

Equation 7.6 is obtained by applying Kirchoff voltage law to 1st loop, and Equation 7.7 is obtained by using 2nd loop as seen in Figure 7.5. If the drain current ($i_d(t)$) is integrated into the Equations 7.3 and 7.4, current flowing through the drain source capacitance and capacitive load are obtained by using following equations;

$$C\frac{dv_c}{dt} = C_{GD}\frac{dv_{GS}}{dt} - [C_{GD} + C_{DS}]\frac{dv_{DS}}{dt} - [g_{fs}(v_{GS} - V_{th})] \tag{7.12}$$

$$C_{DS}\frac{dv_{DS}}{dt} = C_{GS}\frac{dv_{GS}}{dt} - [g_{fs}(v_{GS} - V_{th})] + i_L \tag{7.13}$$

7.2.2.2 Distinctive Features for Interval Three:

When $V_{GS} \rangle V_{th}$ and $V_{DS} \langle V_{GS} - V_{th}$, MOSFET is in linear (ohmic) region and acts as a voltage-dependent resistor (R_{ds_on}). In ohmic region, drain current depends on the drain- source voltage and the curve of the drain current and drain- source voltage is approximately linear. Drain current of the MOSFET in this interval is;

$$R_{ds_on} = \frac{v_{DS}}{i_d(t)} \tag{7.14}$$

When drain current equation is put into the capacitor and drain-source current equations in 7.3 and 7.4, the drain source capacitance and capacitive load currents are obtained as;

$$C\frac{dv_c}{dt} = C_{GD}\frac{dv_{GS}}{dt} - [C_{GD} + C_{DS}]\frac{dv_{DS}}{dt} - \frac{v_{DS}}{R_{ds_on}} \tag{7.15}$$

$$C_{DS}\frac{dv_{DS}}{dt} = C_{Gs}\frac{dv_{GS}}{dt} - \frac{v_{DS}}{R_{ds_on}} + i_L \tag{7.16}$$

Figure 7.6 Closed loops of the circuit when MOSFET is in ohmic region

Due to the Kirchoff voltage law Equation 7.6 is obtained from 1st loop, and Equation 7.7 is obtained from 2nd loop as seen in Figure 7.6 .

The difference between the Figure 7.5 and Figure 7.6 is the behavior of the MOSFET. If the drain-source voltage is equal to or higher than the difference between gate-source voltage and threshold voltage, MOSFET acts as a constant current source. Otherwise, it acts as a variable resistance.

7.2.3 Analytical, Simulation and Experimental Model Results

The variations of the gate-source voltage of the MOSFET, load capacitor voltage and drain–source voltage of the MOSFET with different gate resistances are observed by the analytical, simulation and experimental waveforms. All results are performed and compared by using 2.2Ω, 47 Ω and 220Ω gate resistances at every turn.

Some assumptions are made while modeling the circuit analytically and given in part 7.4.1. Also, parasitic resistances occuring due to the soldering are neglected in both simulation and analytical model. These assumptions and neglected parameters cause differences between the waveforms of the results. The differences between the proposed analytical model and the experimental model for the ringing frequencies and the magnitudes of the waveforms are within reasonable bounds. But when simulation results with circuit elements of block models are observed, it is seen that some parameters such as drain lead inductance and drain source inductance were not taken into account though manufacturer model was used. Due to this, explicit differences occur in simulation results. The spice file of the Power MOSFET model used in simulation is given in the Appendix B.

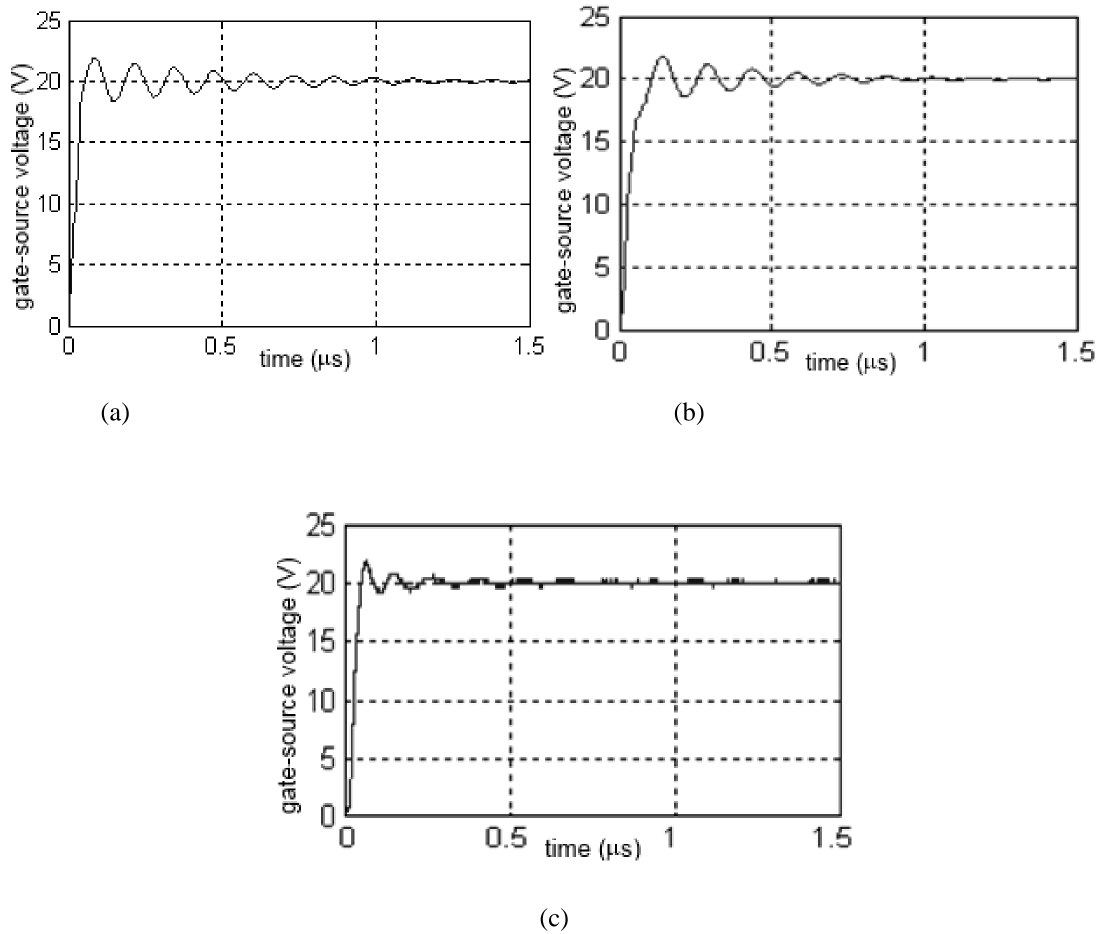


Figure 7.7 MOSFET gate –source voltage waveforms with 2.2Ω gate resistance a) CST Design STUDIO b) Proposed model c) Experimental result (500ns/div, 5volt/div)

Gate Voltage increases from threshold value to higher levels value in the time which required charging the input capacity combined with gate-source and gate-drain capacitances of the MOSFET. Gate-source capacitor is charged very quickly, when gate-source voltage of the MOSFET is very small (2.2Ω), as shown in Figure 7.7.

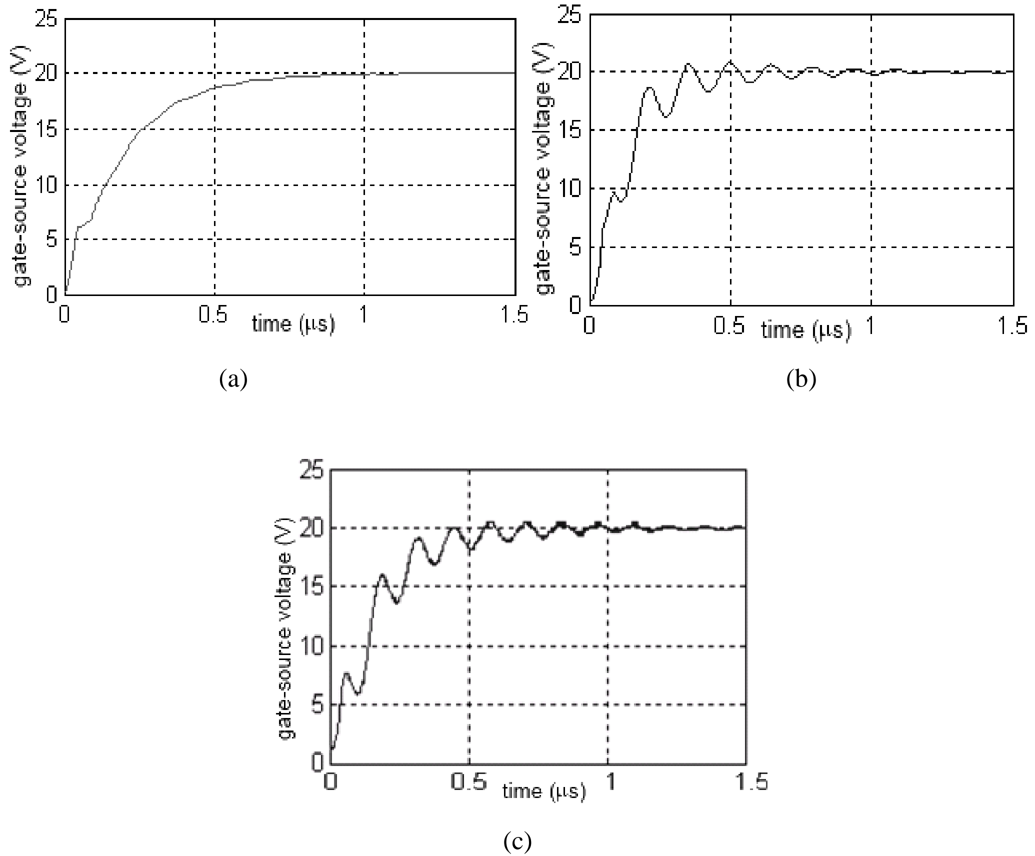


Figure 7.8 MOSFET gate –source voltage waveforms with 47 Ω gate resistance; a) CST Design STUDIO b) Proposed model c) Practically obtained results (500 ns/div, 5 volt/div)

MOSFET Voltage waveforms between gate-source terminals with 47 Ω gate resistance are shown in Figure 7.8. While obtaining this voltage source lead inductance and internal gate resistance are included in Analytical model. But it is seen that these values are not specified in the MOSFET model used in simulation. Application result shows that inductance and resistance in the inner structure of MOSFET also have important effect to observe the oscillations in the terminals of the MOSFET.

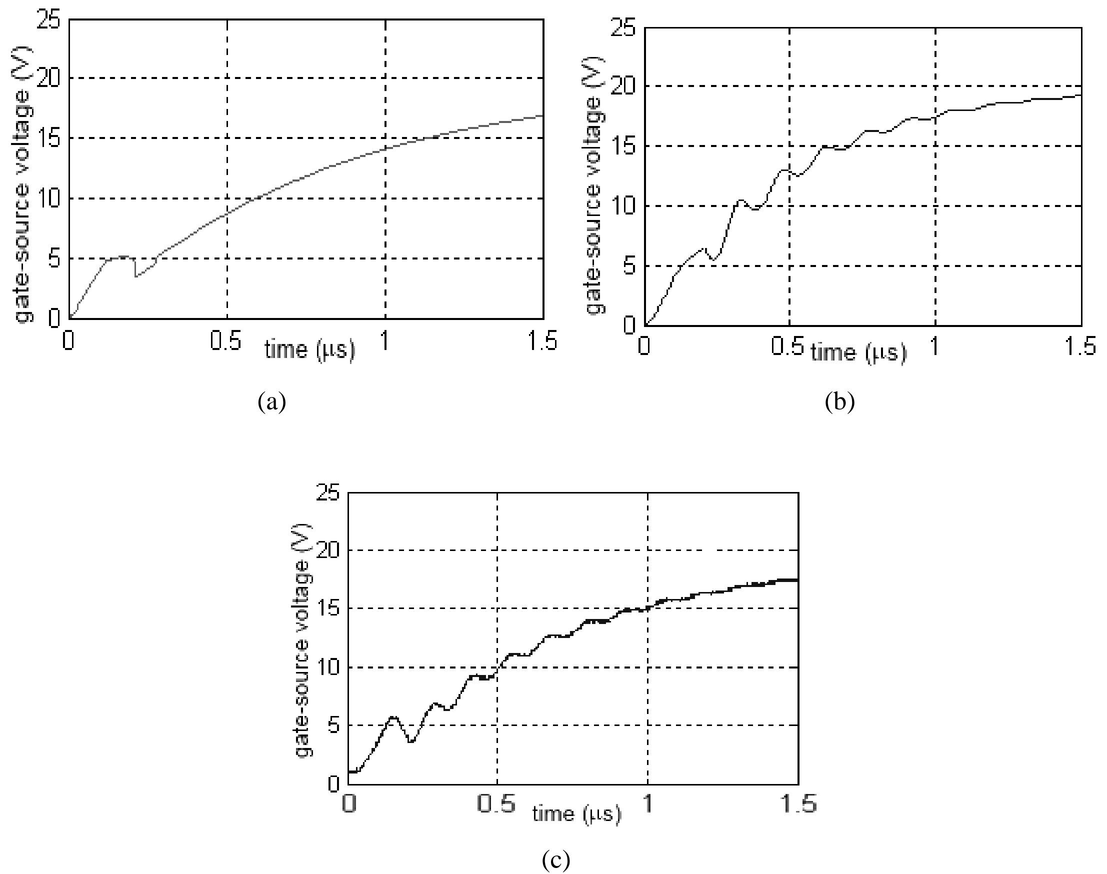


Figure 7.9 MOSFET gate-source voltage waveforms with 220 Ω gate resistance; a) CST Design STUDIO b) MATLAB c) Implemented result (500 ns/div, 5 volt/div)

When gate resistance increases to 220 **Ω**, the gate-source voltage waveforms are shown in Figure 7.9. Again, the ringing frequencies of the signals can not be observed in simulation results. Charging times for gate-source and gate-drain capacitances, increase based on the gate resistance increment. Variation of the gate resistance becomes crucial at this point. As mentioned before, gate source voltage must be higher than threshold value to become on, but by the increment in gate resistance turn-on delay takes longer. Gate-source voltage is also expected to reach pulse voltage value, 20 Volts, in a short time. It reaches this value very quickly for 2.2 Ω gate resistance, beside this it takes longer time when the gate resistance increased. This is because of the time constant which is determined by the gate resistance.

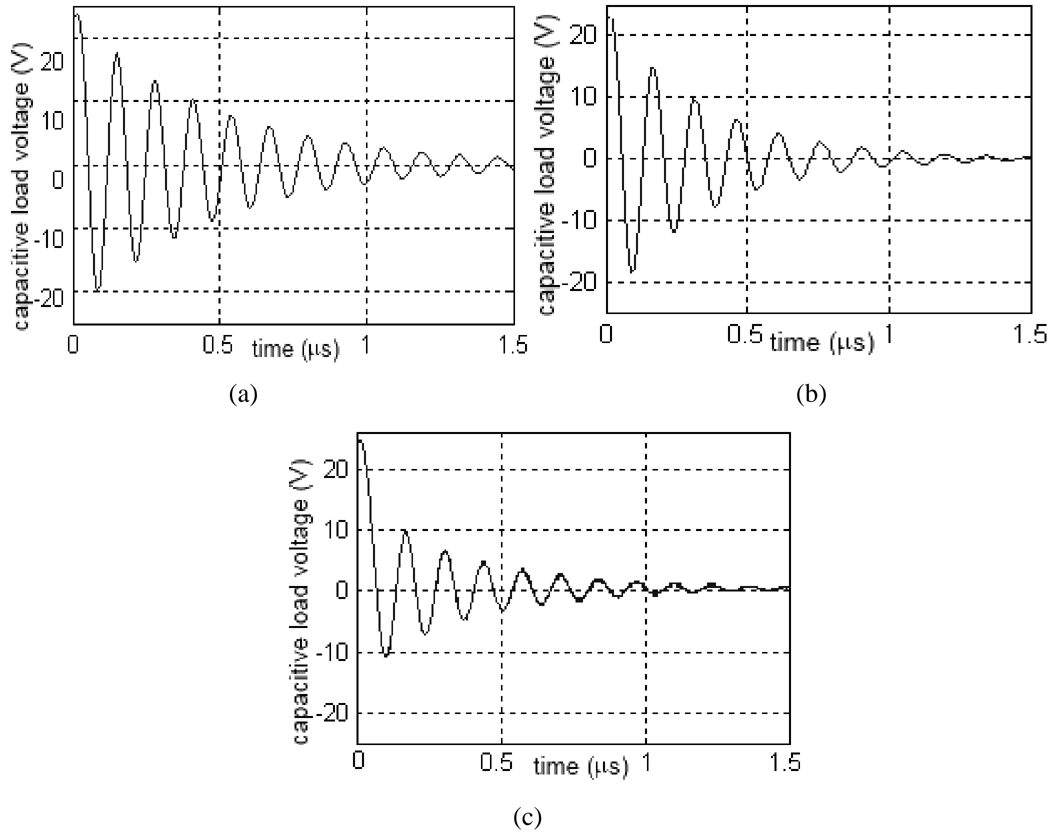


Figure 7.10 Capacitive load voltage waveforms with 2.2Ω gate resistance a) CST Design STUDIO b) MATLAB c) Practically obtained result (500 ns/div, 10 volt/div)

Load capacitor voltage value for 2.2Ω gate resistance is seen in Figure 7.10. Magnitudes of the undesirable oscillations are very high. These high oscillations may cause failures of the components of the circuit. Typically, high-frequency gain of the MOSFET is high; this is why the parasitic oscillation occurs commonly in switching circuits.

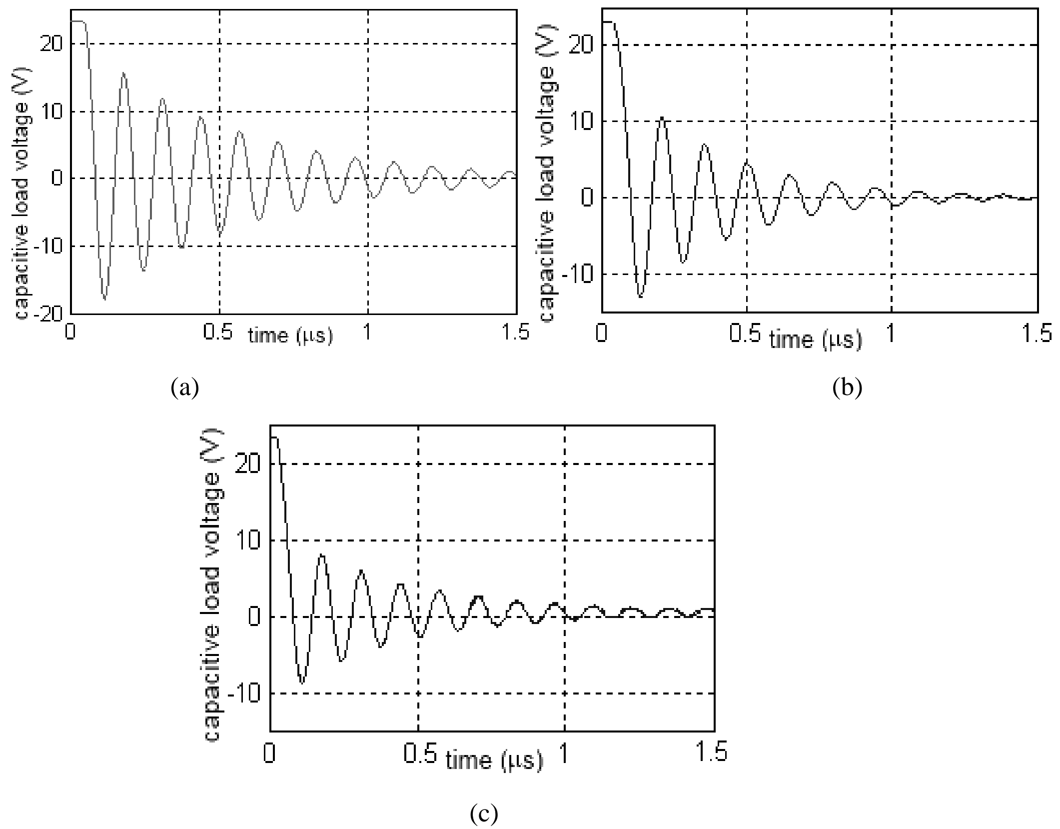


Figure 7.11 Capacitive load voltage waveforms with 47 Ω gate resistance a) CST Design STUDIO b) MATLAB c) Practically obtained result (500 ns/div, 10 volt/div)

In Figure 7.11, load capacitor voltage waveforms for 47 Ω gate resistance are given. Since the input impedance of the MOSFET in the next step is seen capacitive, the output of the buffer is designed as capacitive load. When higher side MOSFET P_2 of Figure 7.1 becomes on and N_2 becomes off a transient, current flows through the output capacitor, and thus capacitor voltage reaches to the 23 Volts and keeps this level. After P_2 turns off, the capacitor maintains its charge. The capacitor begins to discharge the voltage on itself, after the MOSFET N_2 becomes on. But N_2 MOSFET can not become on at the same time, so a delay occurs in order to be on state.

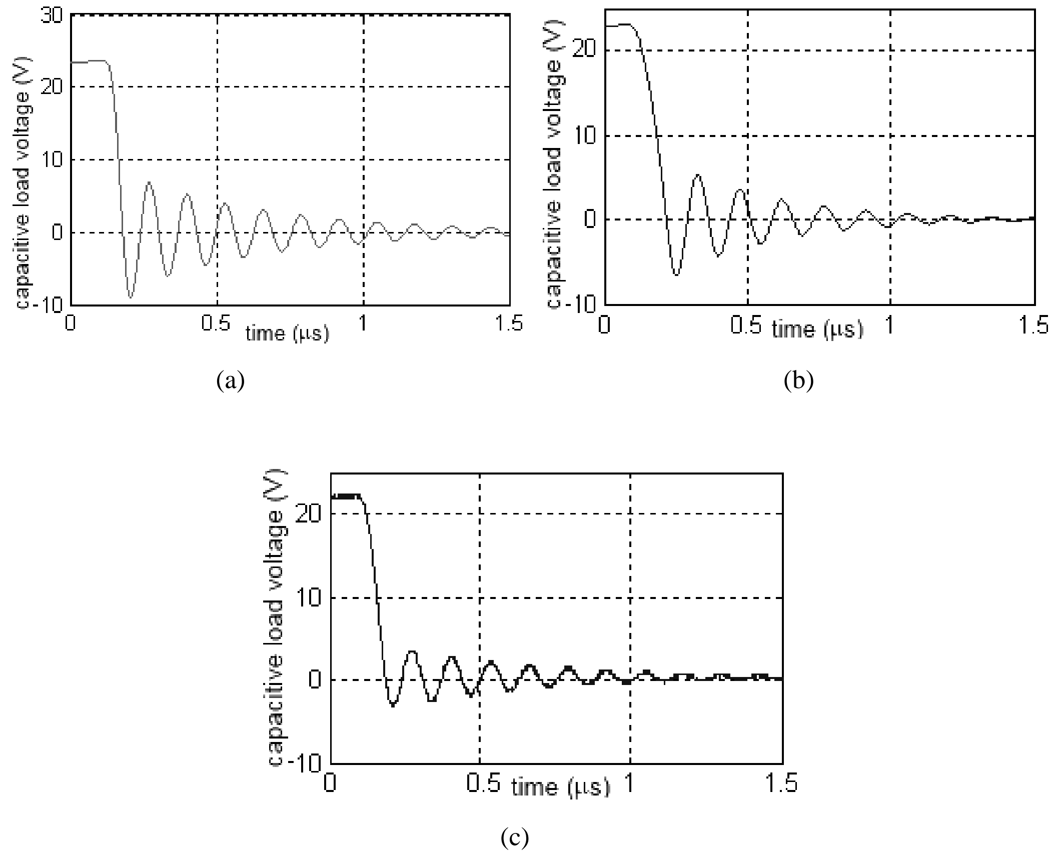


Figure 7.12 Capacitive load voltage waveforms with 220 Ω gate resistance a) CST Design STUDIO b) MATLAB C) Practically obtained result (500 ns/div, 10 volt/div)

When gate resistance is increased to 220 Ω, ringing of the output signal (seen on capacitive load) is decreased as shown in Figure 7.12. Actually, this damping is required to decrease the dv/dt ratio.

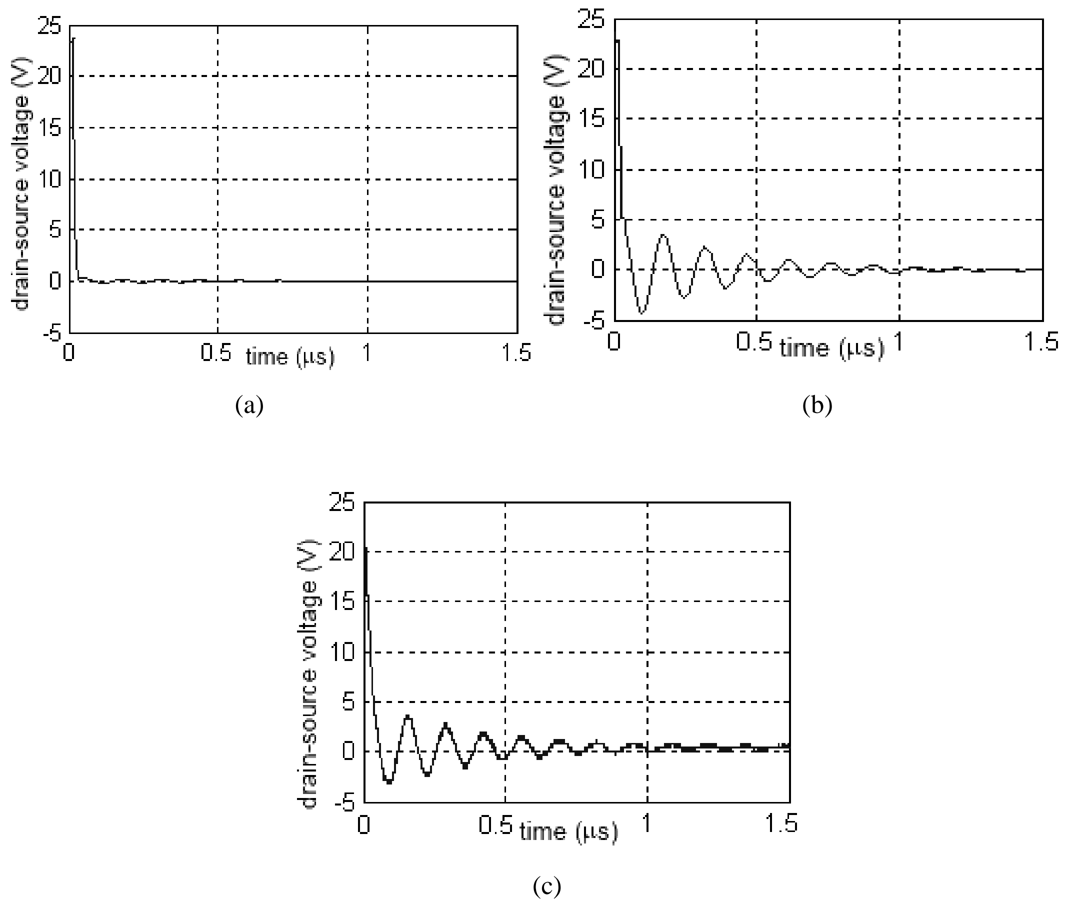


Figure 7.13 MOSFET drain-source Voltage waveforms with 2.2 Ω gate resistance a) CST Design STUDIO b) MATLAB/Simulink C) Practically obtained result (500 ns/div, 5 volt/div)

In Figure 7.13, Drain-Source voltage for 2.2 Ω gate resistance is seen. Analytical model and experimental model results are compatible as shown in figures. Magnitude of the simulation result is very low compared to other results.

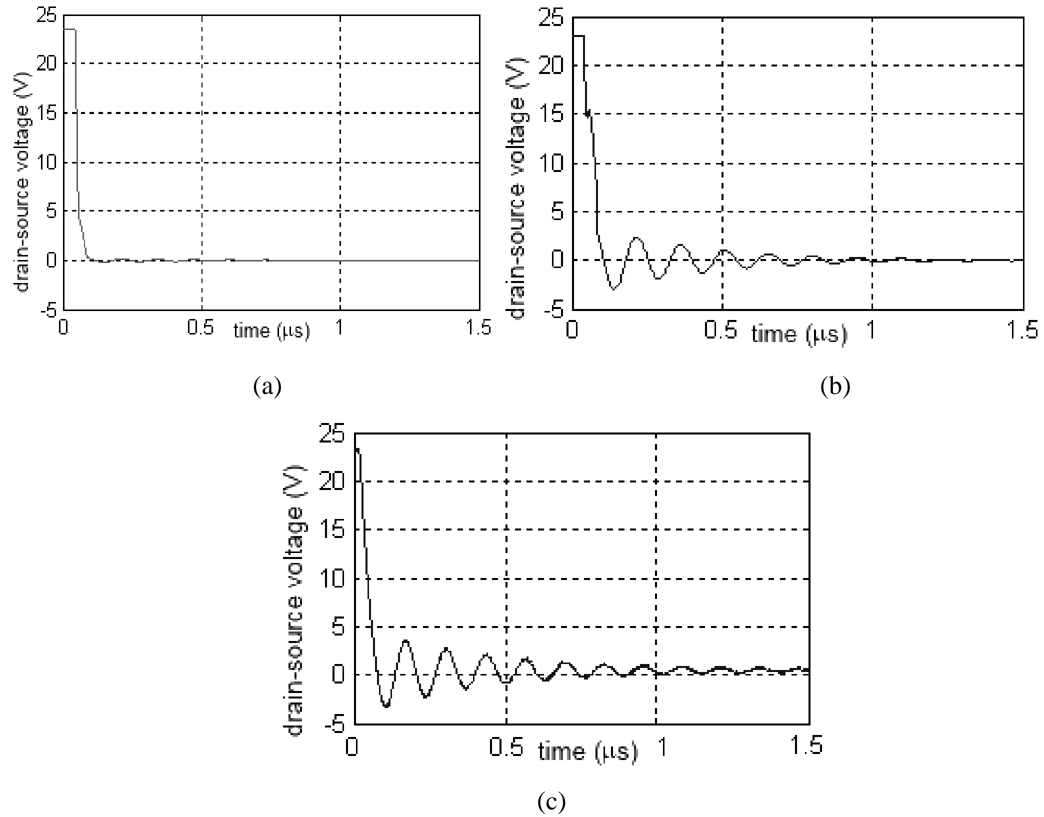


Figure 7.14 MOSFET drain-source voltage waveforms with 47 Ω gate resistance a) CST Design STUDIO b) MATLAB/Simulink C) Practically obtained result (500ns/div, 5volt/div)

Drain-Source voltage of the MOSFET N_2 is seen in Figure 7.14. For 47 Ω gate resistance, the ringing frequencies of the signals are observed approximately 6 MHz analytical model and 6.66 MHz in experimental results. While investigating the drain-source voltage of the MOSFET, both drain and source internal lead inductances should be considered. Despite the most prominent properties are considered in MOSFET model, the internal inductances are not mentioned and this prevents to observe the voltage oscillation seen in the experimental and analytical results.

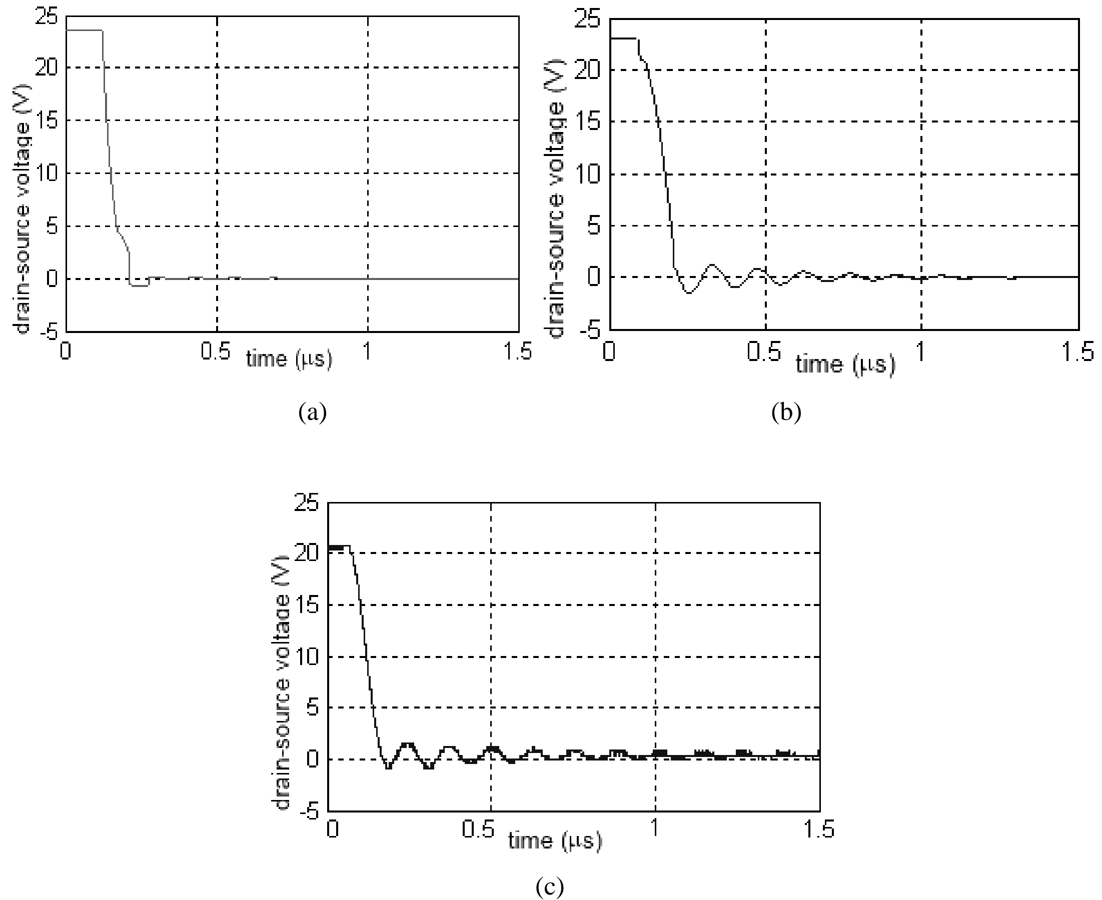


Figure 7.15 MOSFET drain-source voltage waveforms with 220 Ω gate resistance a) CST Design STUDIO b) MATLAB C) Practically obtained result (500 ns/div, 5 volt/div)

As shown in Figure 7.15, when gate resistance is increased to the 220 Ω, the magnitude of the oscillation decreases. The reason for the low magnitude simulation results that is obtained by using CST DESIGN STUIDO is the model of the MOSFET that is used in simulation.

The simulation, analytical and implementation results show that the effect of the gate driver and PCB layout is crucial during the transition of the power switching circuit. Turn-on delay takes longer time and magnitude of the oscillations during transitions decreases when the gate resistance is increased, as it should be expected.

CHAPTER EIGHT
CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

8.1 Conclusion

In this study, switch mode power converter circuits and their loss mechanisms are investigated in order to determine reasons of the failures, the effects on the efficiency and the methods for preventing and /or decreasing failure conditions.

For that purpose, several switch circuits are investigated deeply as evaluation of mathematical models, simulating the circuit by using several simulation techniques and designing experimental circuits for obtaining practical results.

When a switching circuit is established, during the commutation interval, large voltage (current) changing rates may occur across (through) some of the circuit elements. These circuit elements may be semiconductor devices, passive elements or even inevitable parasitic elements of the circuit. The transient driving current flow and the value of the shoot through current at start up may damage just after the driver circuit is just energized. This means by the leakage current of the one of the transistor in the driving circuit while the other one is conducting and named as current hogging.

As known, the semiconductor devices dynamic characteristics differ from their static characteristics and these differences mostly come from non-linear parasitic capacitances of the semiconductor bulk region. All these parasitics are not impactful factors when a circuit is operating with low frequency continuous signals. On the other hand, higher switching frequency of the power processing circuits (converters, inverters) is more preferable because of the smaller circuit size, lower cost and higher power density. In other respects, high switching losses, current/voltage stresses, possible oscillations during the transitions and high Electromagnetic Interference (EMI) caused by high current and voltage peaks during switching actions cause inevitable failures in consequence of the switching frequency

increment. Additionally, operation of a circuit that is based on switching technique, parasitic elements effects on circuit behavior may tremendously change switching waveforms of the circuit. For example, the Miller Theorem provides an insight on the exaggeration of a parasitic capacitance effect on the circuit behavior. In Miller plateau, increment in the capacitor effective value increases the switching losses of the MOSFET.

Determining the losses and parasitic of the circuits in the design stage of ideal passive elements may not be a correct assumption in high frequency switching circuits. For this purpose full wave electromagnetic simulation is used to investigate these probable effects in a studied boost converter circuit. In this manner, CST MW STUDIO software is preferred and results are compared with realized circuit practical results. On account of this program, layout of the Printed Circuit Board (PCB) and characteristic properties of the power semiconductor devices are considered in the design stage.

Simulation with full-wave electromagnetic modeling technique gives an important point of view to observe the whole effects of the circuit and PCB probable effects. Advantage of this program is observing the overshoots of the Boost Converter circuit during switching in the design stage. Overshoots of the investigated boost converter circuit is approximately twice of the MOSFET voltage (22Volt) without snubber circuit during turn-off transition. This overshoot can damage the MOSFET. At this point, a snubber circuit is suggested to mitigate these overshoots. But for the same network after snubber circuit connected, the overshoot voltage decrease to the 13 Volt level. This shows that it is a successful rate for the circuit for operating in the safe area.

In this work, it is also investigated how a driver circuit behaves when all parasitic elements and switching element's non-ideal properties (MOSFET's parasitic capacitances, internal resistances, lead inductances) effects are considered. As a novelty, a new analytical model is proposed by extracting values of aforementioned parasitic elements from datasheet of the MOSFET used in a CMOS buffer circuit

given in the literature. Beside the conventional models, this proposed model takes into account the gate drive resistance, input capacitance of the MOSFETs and wiring inductances of the circuit.

Furthermore, this proposed model is considered the parasitic wiring in the cut-off region of the MOSFET. Thus, effects of the delay time of the MOSFET to become on and possible failures that may be occurs during transitions can be observed. This proposed model results are also examined by comparing the simulation and implementation outputs.

The experimental results show that parasitics caused by the layout of the components on PCB and component's non ideal characteristics change the current and voltage waveforms too much and should be taken into account in simulations.

In power electronic circuits, especially due to the high frequency switching SPICE and so forth conventional simulation programs can not give exact parasitic effects results such as oscillations and overshoots. Simulation with physical based models gives more realistic results in comparison with experimental results and can be seen both in the present thesis studies and also in literature. Even though, this modeling is important in some cases; it is time consuming in some applications. In such cases, analytical model that is proposed can give alternative simulation results to observe the overall effects of the power electronic switching circuits.

8.2 Suggestions for Future Work

The switching behavior of the semiconductor elements are important factors for analyzing the reason of the possible failures of a power electronic circuits. Proposed model is applied for the N- Channel MOSFET of the buffer circuit. A new analytical model for the P-Channel MOSFET needs to be proposed to clarify the whole circuit transitions.

More accurate models of the complex switching circuits can be evaluated in simulation efforts in order to consider all failure mechanisms investigated in this work especially transistor parasitics and EMC/EMI Phenomenon. All failure reasons or resulted unwanted conditions can be explained by this way.

REFERENCES

Arnautovski-Toševa, V., Rousset, Y., Drissi, K. E. K., & Grčev, L. (2005). Radiated EMI from power converters, *Serbian Journal of Electrical Engineering, 2* (2). 117 – 124.

Azizoglu, B. T., & Karaca, H. (2012). Comparison of full-wave and SPICE simulations of a boost converter. *12th Mediterranean Microwave Symposium*, Istanbul, Turkey.

Baker, R. J. (2005). *CMOS circuit design, layout and simulation* (3rd ed.). Piscataway: John Wiley & Sons, Inc.

Baliga, B. J. (2008). *Fundamentals of power semiconductor devices,* USA: Springer Science + Business Media, LLC.

Baliga, B.J., Adler, M. S., Gray, P.V., & Love R.P. (1982). The Insulated Gate Rectifier (I G R): A new power switching device. *IEEE International Electron Device Meeting, 28*, 264 – 267.

Bhargava, A., Pommerenke, D., Kam K., Chang, X., Centola, F., Lam C., et al. (2009). EMI prediction in switched power supplies by full-wave and non-linear circuit co-simulation. *IEEE International Symposium on Electromagnetic Compatibility,* Austin, Texas, USA, 41–46.

Bogdan, M., Wilamowski, J. & Irwin, D. (2011). *Power electronics and motor drives* (2nd ed.). Taylor and Francis Group, LLC.

Bonkowski, R. (2007). Replacing selenium rectifiers. *Antique Wireless Association Journal*, *48*, 26-29.

Bell Tellephone Laboratories (1948), Retrieved February 8, 2013, from http://www.beatriceco.com/bti/porticus/bell/pdf/bell-labs%20transistor%20announcement.pdf

Cova, P., Menozz,i R., Pasqualett,i M., Portesine, M., Scicolone, R., & Zerbinati, B. (1999). Anomalous overvoltage oscillations in the reverse recovery of power p-i-n diodes: experiments and simulations, *Conference on Power Electronics and Applications (EPE'99)*, Lausanne (Switzerland).

David, C. J., & Robert, W. E. (2013). Analysis of switching circuits through incorporation of a generalized diode reverse recovery Model Into State Plane Analysis, *IEEE Transactions on Circuits and Systems—I: Regular Papers, 60* (2), 479-490.

Dhariwal, S. R., & Sharma R. C. (1992). Determination of carrier lifetime in p-i-n diodes by ramp recovery, *IEEE Electron Device Letters*, *13* (2), 98-101.

Dorf, R.C. (Ed.). (1997). *The electrical engineering handbook* (2nd ed.). Boca Raton: CRC Press LLC.

Duarte, C. M. C., & Barbi, I. (2002). An improved family of ZVS-PWM active-clamping DC-to-DC converters. *IEEE Transaction on Power Electronics*, *17* (1), 1-7.

Elasser, A., Torrey, D. A. (1996) Soft switching active snubbers for DC/DC converters. *IEEE Transactions on Power Electronics*, *11* (5), 710-722.

Erickson, R. W. (2000). *Fundamentals of power electronics* (2nd ed.) USA: Kluwer Academic.

Felic, G., & Evans, R. (2003). Modelling and simulation of power converters using the FDTD-SPICE approach, *IEEE International Symposium on Electromagnetic Compatibility (EMC '03), 1* , 277 – 279.

Fiel, A., & Wu, T. (2001) MOSFET failure modes in the Zero-Voltage-Switched Full-Bridge switching mode power supply applications. *Applied Power Electronics Conference and Exposition (APEC 2001), 2* , 1247-1252.

Grand, D. A., & Gowar, J. (1989). *Power mosfets: Theory and Applications* (1st ed.). Canada: John Willey & Sons Inc.

He, J., Fu, Q., Gao, Y., Zhang, C., & Zhou, J. (2012). Radiated emission prediction of a SMPS based on time domain EMF-Circuit co-simulation. *IEEE 7th International Power Electronics and Motion Control Conference – ECCE,* China, 1082-1086.

He, X., Chen, A., Wu, H., Deng, Y., & Zhao, R. (2006). Simple passive lossless snubber for high-power multilevel inverters. *IEEE Transactions Industrial Electronics, 53* (3), 727–735.

Howe, R. T., & Sodini, C. G. (1996). *Microelectronics an integrated approach* (International ed.) London: Prentice-Hall International Inc.

Hummel, R. E. (2004). *Understanding materials science: history, properties, applications* (2nd ed.). New York: Springer-Verlag.

Jitaru, I.D. (1992). A new high frequency, zero-voltage switched, PWM converter. *IEEE Applied Power Electronics Conference and Exposition,* (7) *,* 657 – 664.

Jovanovic, M. M., Wojciech, A. T., & Fred C. L. (1988). Zero-voltage-switching technique in high-frequency off-line converters. *IEEE Proceedings of Applied Power Electronics Conference*, New Orleans, 23-32.

Kazimierczuk, M. K. (2008). Pulse-width modulated DC–DC power converters (1st ed.). United Kingdom: John Wiley & Sons, Ltd.

Kazimierczuk, M.K. (1988). High-speed driver for switching power MOSFETs. *IEEE Transactions on Circuit and Systems , 35* (2), 254-256.

Korec, J. (2011). *Low voltage power MOSFETs design, performance and applications*, New York: Springer.

Laker, K. R., & Sansen W. M. C. (1994). *Design of analog integrated circuits and systems (*International ed.) New York: McGraw-Hill Companies.

Laszlo, B. (2001). *Design and application guide for high speed MOSFET gate drive circuits.* TI-Unitrode Power Supply Design Seminar, United States, 1–37.

Li, R. T. H., Chung, H. S.-H., & Sung, A. K. T. (2010). Passive lossless snubber for boost PFC with minimum voltage and current stress. *IEEE Transactions on Power Electronics*, *25* (3), 602-613.

Lim, T. C., Williams, B.W., & Finney, S.J. (2011). Active snubber energy recovery circuit for series-connected IGBTs. *IEEE Transactions on Power Electronics*, *26* (7), 1879 – 1889.

Ludwig, R., Bretchko, P. (2000). *RF circuit design, theory and applications,* New Jersey: Prentice Hall.

Lutz, J., Schlangenotto, H., Scheuermann, U., & Doncker, R. D. (2011). *Semiconductor power devices physics, characteristics, reliability*, New York: Springer-Verlag.

Miller, J. M.(1919.). Dependence of input impedance of a three-electrode vacuum tube upon the load in the plate circuit. *Journal of the Franklin Institute-engineering and Applied Mathematics,* (351), 367–385.

Mohan, N., Undeland, T. M., & Robbins, W.P. (1989). *Power electronics: converters, application, and design*, United Kingdom: John Willey & Sons.

Ma, C. L., & Lauritzen, P. O. (1991) A simple diode model with reverse recovery. IEEE *Transactions on Power Electronics, 6* (2), 188-191.

Ma, C. L., & Lauritzen, P.O. (1993). A simple diode model with forward and reverse recovery. *IEEE Transactions on power electronics*, *8* (4), 342-346.

Ng, K. K. (2006). *Complete guide to semiconductor devices* (International ed.).New Jersey: Murray Hill.

Ohl, R. S. (1946). *Light-sensitive electric device*. U.S. Patent. 2, 402, 662.

Peng, F. Z., Su, G.-J., & Tolbert, L. M. (2004). A passive soft-switching snubber for PWM inverters. *IEEE Transactions on Power Electronics, 9* (2), 363–370.

Perret, R. (2009). *Power electronics semiconductor devices*. Great Britain & United States: ISTE Ltd & John Wiley & Sons, Inc.

Pressman A. I., Billings K., Morey T. (2009). *Switching power supply design* (3rd ed.). United States: McGraw-Hill Companies.

Puri, V. K. (2000). *Digital electronics: circuits and systems.* New Delhi: Tata McGraw-Hill Companies.

Rashid, M. H., & Rashid H. M. (2006). *SPICE for power electronics and electric power* (2nd ed.). Boca Raton: Taylor & Francis Group.

Rashid, M. H. (2011). *Power electronics handbook; devices, circuits, and applications* (3rd ed.), USA: Elsevier Inc.

Saro, L., Redl R., & Dierberger, K. (1998). High-voltage MOSFET behavior in soft-switching converter: Analysis and reliability improvements. *IEEE Telecommunication Energy Conference*, 30-40.

Severns, R. (2008) *Snubber circuits for power electronics*. SMPS Technology, [E-book] Available: http://www.snubberdesign.com/snubberbook.html.

Shockley, W. (1949). The theory of p-n junctions in semiconductors and p-n junction transistors. *Bell System Technical Journal* , *28*, 435-489

Takahashi, K., Yoshikawa, A., & Sandhu, A. (2007). *Wide bandgap semiconductors fundamental properties and modern photonic and electronic devices*, (Eds.), New York: Springer-Verlag

Tan, C. M., & Tseng, K. (1999). Using power diode models for circuit simulations—a comprehensive review. IEEE *Transactions on Industrial Electronics*, *46* (3), 637-645.

Todd, P. C. (1993). *Snubber circuits: Theory, design and application*. 1 September 2014, http://www.ti.com/lit/an/slup100/slup100.pdf

Vithayathil, J. (1995). *Power electronics: Principles and application* (International ed.). United States of America: McGraw- Hill, Inc..

Fairchild Semiconductor Corporation (2008). *Application note AN-6076 design and application guide of bootstrap circuit for high-voltage gate drive IC*. 5 March 2011, https://www.fairchildsemi.com/application-notes/AN/AN-6076.pdf

Tektronix (2004). *P6022 current probe instruction manual.*12 April 2011, http://www.produktinfo.conrad.com/datenblaetter/1100000-1199999/001171295-an-01-en-TEKTRONIX_P6022_AC _STROMTASTKOPF.pdf.

Weiland, T. (1977). A discretization method for the solution of Maxwell's equations for six-component fields. *Electronics and Communications AEU, 31*, (3), 116–120.

Wolley, E. D., & Van Dell, W. R. (1988). Fast recovery epitaxial diodes (FRED's). *IEEE Conference Record of the Industry Applications Society Annual Meeting*, 1, 655-663.

Yazdani, M.R., & Farzanehfard H. (2012). Conducted electromagnetic interference analysis and mitigation using zero-current transition soft switching and spread spectrum techniques. *IET Power Electronics, 5* (7). 1034-1041

Yun, J-J., Choe, H-J., Hwang, Y-H., Park, Y-K., & Kang, B. (2012), Improvement of power-conversion efficiency of a DC-DC boost converter using a passive snubber circuit. *IEEE Transactions on Industrial Electronics, 59* (4). 1808-1814

Zhang, H., & Pappas, J. A. (2001). A moving boundary diffusion model for PIN diodes. *IEEE Transactions on Magnetics, 37* (1), 406-410.

Zhang, Y., & Sen, P. C. (2003). A new soft-switching technique for Buck, Boost, and Buck–Boost Converters. *IEEE Transaction on Industry Applications, 39* (6), 1775-1882.

APPENDICES

APPENDIX A

Summary of the Diode Models and their characteristics (Tan & Tseng, 1999);

Model	Year	Applicabilities										
		Type of diode			Rating of power diode			DC	Simulator type		# of input	Parameter[c]
		p-i-n	p-v-n[a]	p+n/n+	low PIV[b]	high PIV	high current		PSPICE	Saber	parameters	extraction
Analytical model												
Liang	1990			x	x				x		7	yes
Lauritzen	1991	x			x					x	5	yes
Jin	1991	x	x							x	4	yes
Kraus	1992	x	x		x	x	x	x		x	17	no
Ma I	1993	x			x			x		x	9	yes
Ma II	1993	x	x		x			x		x	6	yes
Yang	1994			x						x	7	no
Tseng I	1994	x	x		x			x	x	x	6	no
Analogy	1995	x	x		x	x	x	x		x	59	no
Strollo	1996	x	x		x	x	x	x	x		20	no
Ma III	1997	x	x		x	x	x	x		x	8	yes
Tseng II	1997	x	x		x	x			x	x	8	no
Numerical and hybrid model												
Vogler	1992	x	x		x	x	x	x		x	26	yes
Winterheimer	1992			x	x	x					6	no
Goebel	1992	x	x		x	x	x	x		x	11	no
Empirical model												
Bertha	1993	x	x	x	x	x	x	x	x		18	yes

APPENDIX B

Spice model file code of the IRF540Z Power MOSFET;

```
* External Node Designations
* Node 1 -> Drain
* Node 2 -> Gate
* Node 3 -> Source
M1 9 7 8 8 MM L=100u W=100u
.MODEL MM NMOS LEVEL=1 IS=1e-32 VTO=4.39635
+LAMBDA=1.10457 KP = 164.601 CGSO=1.70751e-05 CGDO=2.65646e-07
RS 8 3 0.0255521
D1 3 1 MD
.MODEL MD D IS=5.73648e-10 RS=0.00262348 N=1.28253
+BV=100 IBV=0.00025 EG=1.2 XTI=1.38006 TT=1e-07
+CJO=6.17499e-10 VJ=0.5 M=0.528625 FC=0.1
RDS 3 1 1e+07
RD 9 1 0.0001
RG 2 7 6
D2 4 5 MD1
* Default values used in MD1:
*   RS=0 EG=1.11 XTI=3.0 TT=0
*   BV=infinite IBV=1mA
.MODEL MD1 D IS=1e-32 N=50 CJO=5.19046e-10 VJ=0.5 M=0.509408 FC=1e-08
D3 0 5 MD2
* Default values used in MD2:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   BV=infinite IBV=1mA
.MODEL MD2 D IS=1e-10 N=0.4 RS=3e-06
RL 5 10 1
FI2 7 9 VFI2 -1
VFI2 4 0 0
EV16 10 0 9 7 1
CAP 11 10 1.63525e-09
FI1 7 9 VFI1 -1
VFI1 11 6 0
RCAP 6 10 1
D4 0 6 MD3
* Default values used in MD3:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   RS=0 BV=infinite IBV=1mA
.MODEL MD3 D IS=1e-10 N=0.4
.ENDS irf540zs_l
```

APPENDIX C

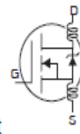
IRF540Z Technical Specifications from datasheet (International Rectifier);

Absolute maximum ratings, electrical characteristics, source-drain ratings and characteristics of IRF540Z;

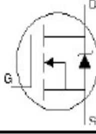
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	36	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	25	
I_{DM}	Pulsed Drain Current ①	140	
P_D @T_C = 25°C	Power Dissipation	92	W
	Linear Derating Factor	0.61	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy②	83	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⑥	120	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw ⑦	10 lbf•in (1.1N•m)	

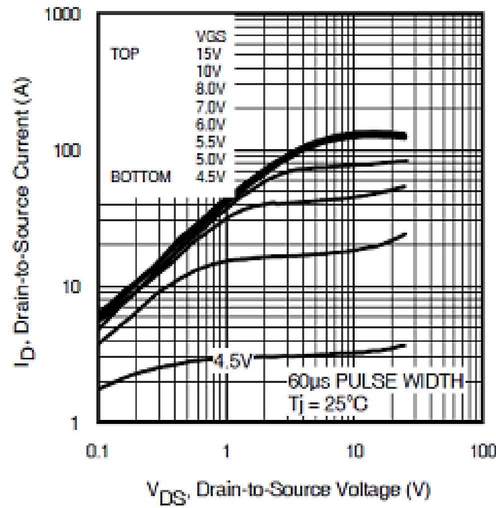
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.093	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	21	26.5	mΩ	V_{GS} = 10V, I_D = 22A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
gfs	Forward Transconductance	36	—	—	V	V_{DS} = 25V, I_D = 22A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 100V, V_{GS} = 0V
		—	—	250		V_{DS} = 100V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
Q_g	Total Gate Charge	—	42	63	nC	I_D = 22A
Q_{gs}	Gate-to-Source Charge	—	9.7	—		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	15	—		V_{GS} = 10V ③
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	V_{DD} = 50V
t_r	Rise Time	—	51	—		I_D = 22A
$t_{d(off)}$	Turn-Off Delay Time	—	43	—		R_G = 12 Ω
t_f	Fall Time	—	39	—		V_{GS} = 10V ③
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) 
L_S	Internal Source Inductance	—	7.5	—		from package and center of die contact
C_{iss}	Input Capacitance	—	1770	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	180	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	100	—		f = 1.0MHz
C_{oss}	Output Capacitance	—	730	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	110	—		V_{GS} = 0V, V_{DS} = 80V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	170	—		V_{GS} = 0V, V_{DS} = 0V to 80V ④

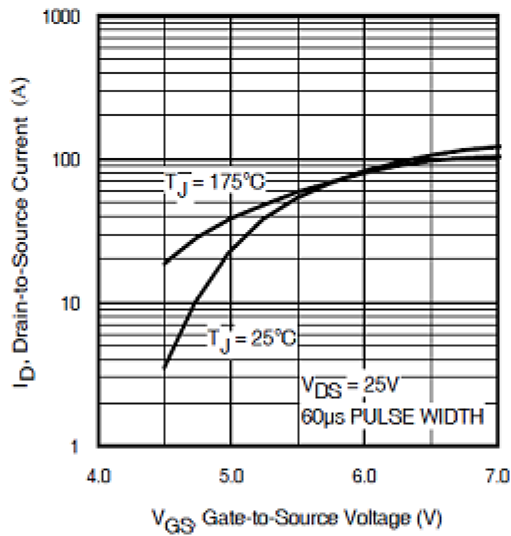
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	36	A	MOSFET symbol showing the 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	140		integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 22A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	33	50	ns	T_J = 25°C, I_F = 22A, V_{DD} = 50V
Q_{rr}	Reverse Recovery Charge	—	41	62	nC	di/dt = 100A/µs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

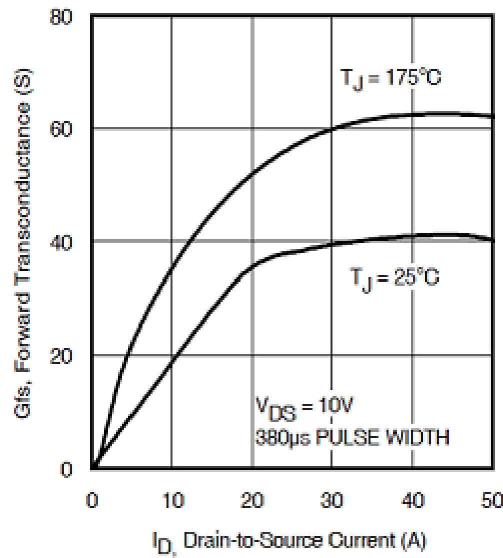
Change of the drain-source current vs. drain source voltage of the IRF540Z at $25^{\circ} C$;



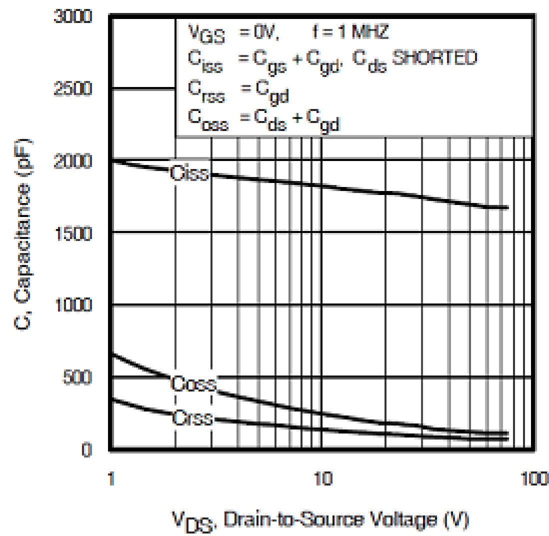
Change of the drain-source current lead to gate source voltage of the IRF540Z when drain-source voltage is equal to the 25 V;



Change of the forward transconductance vs. drain source current of the IRF540Z when drain-source voltage is equal to the 10 V;

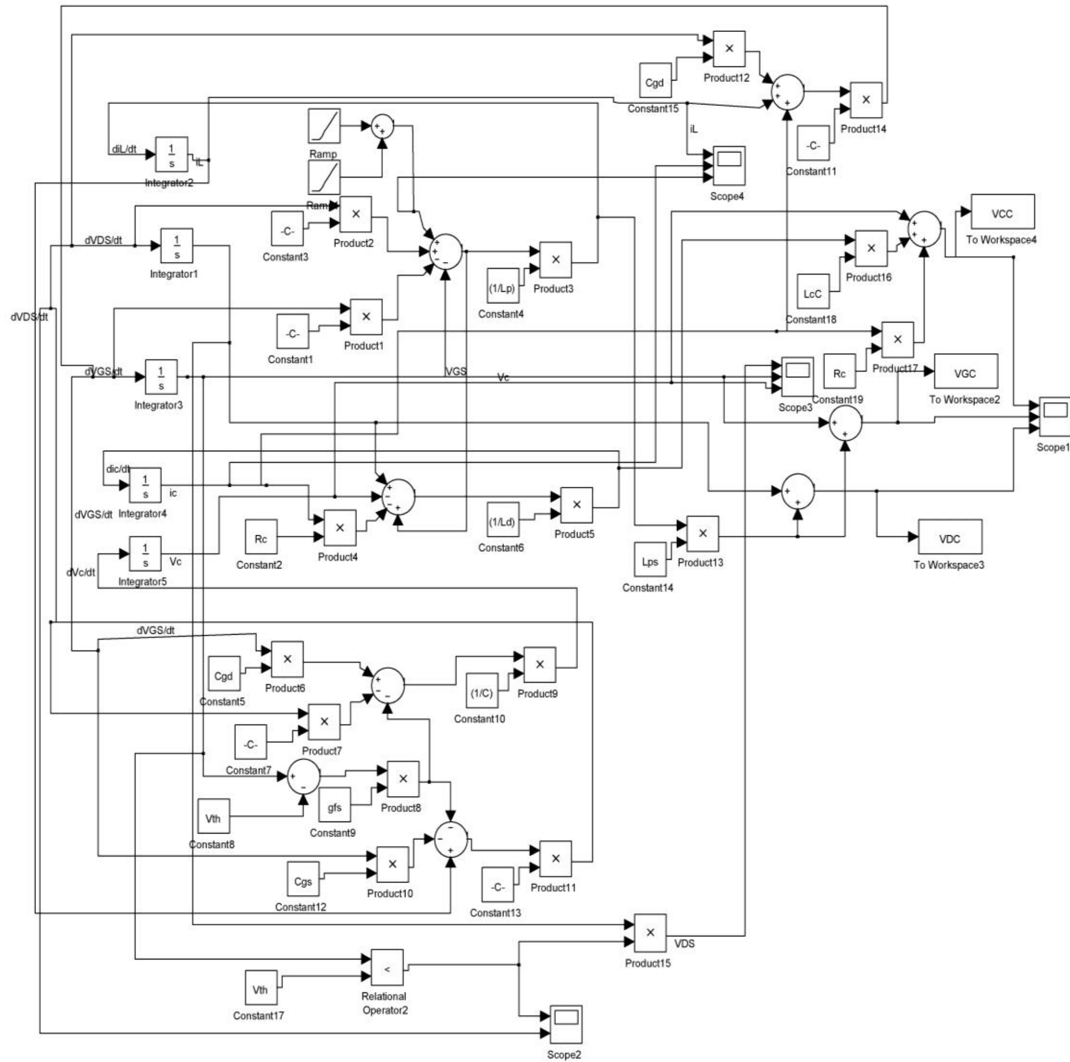


Typical capacitance vs. drain to source voltage;

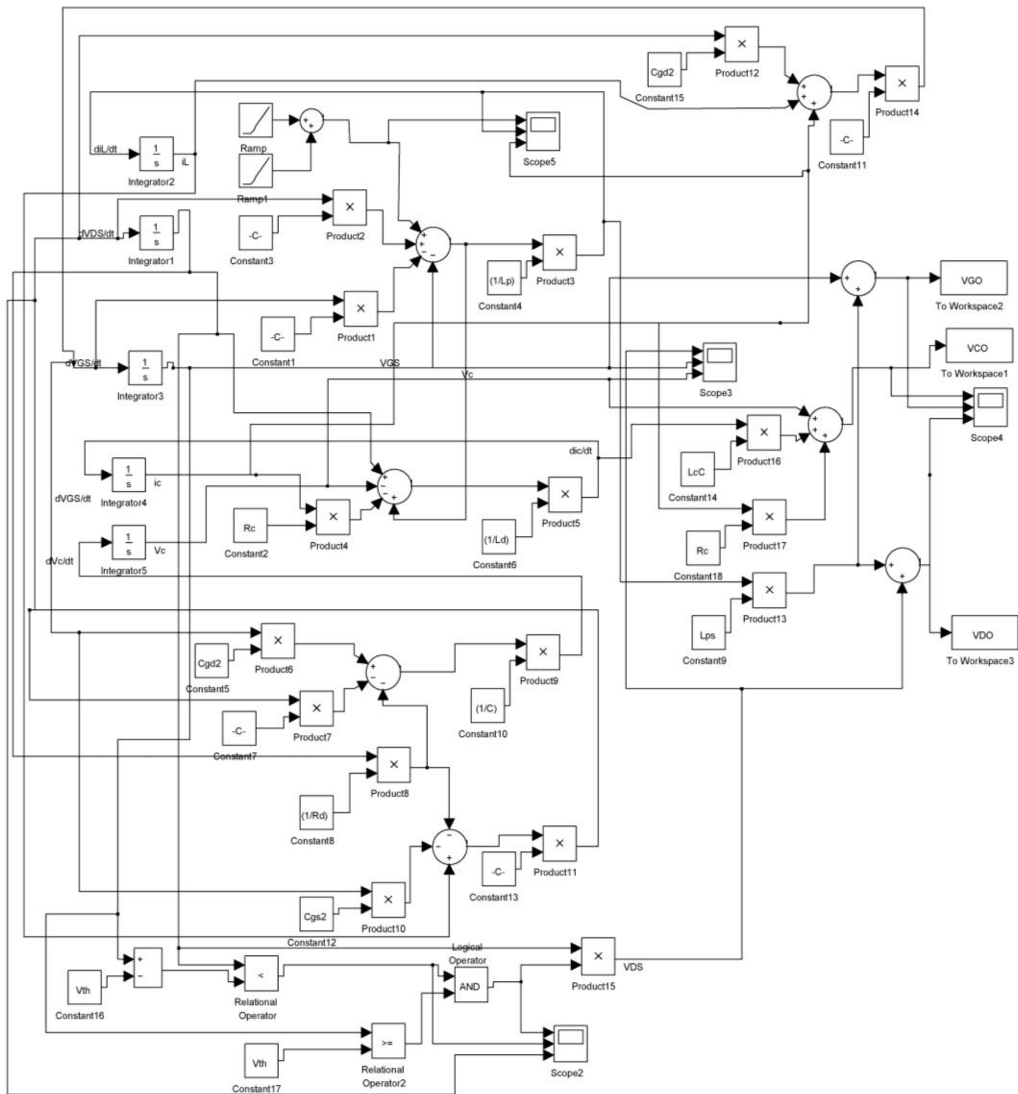


APENDIX D

Analytical Approach Scheme When MOSFET is in Cut-off Region in MATLAB;



Analytical Approach Scheme When MOSFET is in Ohmic Region in MATLAB;



Analytical Approach Scheme When MOSFET is in Saturation Region in MATLAB;