ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

DESIGN OF A CONTROL HARDWARE FOR AN AUXILIARY RESONANT COMMUTATED POLE DUAL ACTIVE BRIDGE CONVERTER

M.Sc. THESIS

Abdulkerim UĞUR

Department of Electrical Engineering

Electrical Engineering Programme

Thesis Advisor: Asst. Prof. Deniz YILDIRIM

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

YARDIMCI REZONANS KUTUP KOMUTASYONLU BİR DUAL AKTİF KÖPRÜ ÇEVİRİCİ İÇİN BİR KONTROL DONANIMI TASARIMI

YÜKSEK LİSANS TEZİ

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OCAK 2012

Abdulkerim UĞUR, a **M.Sc.** student of ITU **Institute of Science and Technology** student ID **504091036**, successfully defended the **thesis** entitled "**DESIGN OF A CONTROL HARDWARE FOR AN AUXILIARY RESONANT COMMUTATED POLE DUAL ACTIVE BRIDGE CONVERTER**", which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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To my family,

FOREWORD

First of all, I would like to express my sincerely thanks to my supervisor Asst. Prof. Deniz Yıldırım at Istanbul Technical University for his support and encouragements during my master studies. Moreover, I would like to show my deepest gratitude to Dipl. Ing. Nils Soltau for his excellent guidance and tutoring during my exchange studies at RWTH Aachen University. It was a pleasure for me to work with him.
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January 2012

Abdulkerim UĞUR
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TABLE OF CONTENTS

Page

ABBREVIATIONS

ARCP	**:** Auxiliary Resonant Commutated Pole
CPLD	**:** Complex Programmable Logic Device
DAB	**:** Dual Active Bridge
DAK	**:** Dual Aktif Köprü
DPS	**:** Dual Phase Shift
E.ON ERC	**:** E.ON Energy Research Center
HVDC	**:** High Voltage Direct Current
PWM	**:** Pulse Width Modulation
SPS	**:** Single Phase Shift
SCU	**:** Stack Control Unit
TRM	**:** Triangular Modulation
TZM	**:** Trapezoidal Modulation
SCU	**:** Stack Control Unit
YRKK	**:** Yardımcı Rezonans Kutup Komutasyonu
ZVD	**:** Zero Voltage Detection
LDO	**:** Low-dropout

LIST OF TABLES

Page

LIST OF FIGURES

Page

DESIGN OF A CONTROL HARDWARE FOR A AUXILIARY RESONANT COMMUTATED POLE DUAL ACTIVE BRIDGE CONVERTER

SUMMARY

Increasing energy demand and the advancement in the renewable energy technologies such as wind and solar power have resulted in development of new research topics. Among these topics, high voltage direct current power transfer from the offshore windfarms makes the design of a megawatt range high power DC/DC converter as one of the important subjects. For this type of an application, design of a durable, reliable and efficient system is absolutely necessary. Therefore to increase the efficiency and to supress the stresses on the semiconductor devices, application of an appropriate soft switching technique is very important.

The dual active bridge (DAB) converter is one of the important candidate topologies for high power DC/DC converters. On the other hand, the soft switching capability of the dual active bridge converter is limited. The solution of this problem could be the adaptation of a well known soft switching method, namely auxiliary resonant commutated pole (ARCP). In this thesis, a flexible control hardware has been developed which will be utilized to combine DAB and ARCP and to manage the switching signals synchronously according to the commands received from the main controller.

The scope of this thesis is the design and implementation of a control hardware for an auxiliary resonant commutated pole multimegawatt dual active bridge converter. The control system has been applied with CPLDs because of its ruggedness and flexibility for different approaches. At the beginning of this thesis, a short introduction to multimegawatt converters and the dual active bridge converter is made, and the analysis of the ARCP is covered. Later, the control mechanism which is applied in VHDL language is presented and the state machine applied in the device to generate and control the switching signals according to the input commands are described in detail. Also, as a part of this thesis, zero voltage detection circuits are examined and a proper solution compatible with the ARCP control unit has been implemented in hardware.

At the end of the thesis, the design of the hardware is explained and the test results of the circuit are given. The software has been verified on a test device and implemented to the prepared control hardware. The control hardware is tested and the response of the device to the input commands has been verified. Moreover, the zero voltage detection circuit is tested with an alternating voltage input and the response has been checked. Similiarly, the thesis includes the result of this circuit as well.

The control hardwares are expected to be used in the 5MW converter which has being developed in E.ON energy research center in Germany.

YARDIMCI REZONANS KUTUP KOMUTASYONLU BİR DUAL AKTİF KÖPRÜ ÇEVİRİCİ İÇİN KONTROL DONANIMI TASARIMI

ÖZET

Artan enerji ihtiyacı ve fosil yakıtlara bağlı klasik enerji santrallerinin çevreye olan olumsuz etkileri, yenilenebilir enerji kaynaklarının önemini iyice artırmıştır. Özellikle rüzgar ve güneş enerjisinin kullanımı üzerine meydana gelen gelişmeler bu kaynaklarının kullanımını yaygınlaştırmakla beraber, getirdikleri sorunlar ve ihtiyaçlara bağlı olarak mühendislere yeni araştırma konuları açmıştır.

Yapılan araştırmalara göre deniz kıyısı rüzgar türbinlerinin ve rüzgar tarlalarının karada olanlardan daha verimli olduğu bilinmektedir. Ancak bu tip santrallerden enerji iletimi beraberinde bazı sorunlar getirmektedir. Bu sorunlardan biri de enerjinin alternatif akımla taşıması sırasında reaktif güç alışverişinden kaynaklanan enerji kaybıdır. Son yıllarda bu tip santrallerden direkt akımla enerji taşıma üzerinde çalışmalar ve uygulamalar yapılmaktadır. Bu tip sistemler için yüksek güçte DA/DA çeviricilerin tasarlanması ve uygulanması gerekmektedir. Bu çalışmada bu amaçla tasarlanan bir çevirici için kontrol donanımı dizayn edilmiş ve test sonuçları verilmiştir.

Tezin başında tezin çıkış noktası anlatılmıştır ve tezin içeriğine ve konunun işlenişine dair genel bilgiler verilmiştir.

Tezin ikinci kısmında, yüksek güçteki çeviriciler üzerinde yapılmakta olan araştırmalar verilmiş ve tartışılmıştır. Bu tip uygulamalar için en uygun topolojilerden biri de dual aktif köprü (DAK) topolojisidir. Çalışmada bu topolojinin genel olarak çalışma prensibi anlatılmıştır. Bu tip bir çeviricide yumuşak anahtarlama hem verimi artırmak hem de yarı iletken elemanlar üzerinde stresleri azaltmak açısından önemli bir ihtiyaçtır. DAK topolojisinin yapısında yumuşak anahtarlama varolsa da, bunun standart kontrol metoduyla sistemin tüm çalışma değerlerinde sağlanması mümkün değildir. Tezin bu kısmında DAK topolojisine ek olarak, bu sorunu aşmak amacıyla literatürde geliştirilen çeşitli kontrol metodlarına değinilmiştir. İkinci kısmın sonunda bu kontrol metodlarının problemleri kısaca anlatılmıştır ve tartışılmıştır.

Bu kontrol metodlarının uygulanmasında varolan zorluklar nedeniyle, bu çeviriciye iyi bilinen yumuşak anahtarlama yöntemlerinden biri, yardımcı rezonant kutup komutasyonu, (YRKK) uygulanması amaçlanmıştır. Tezin üçüncü kısmında YRKK detaylı olarak incelenmiş, çalışma prensibi ve sistem dinamiğine bağlı denklemler çözülmüş ve tartışılmıştır. YRKK için temel olarak bulunan üç farklı komutasyon modu, diyot komutasyonu, anahtar komutasyonu ve yüksek yük akımında komutasyon ayrı ayrı incelenmiştir. Yine YRKK için varolan iki ayrı kontrol metodu sabit zaman kontrolu ve değişimli zaman kontrolu bu bölümde anlatılmış, varolan zorluklara ve problemlere değinilmiştir. Kısmın sonunda gerekli değerlendirme yapılarak sabit zaman kontrol metodunun seçilme nedenleri verilmiştir.

Yine üçüncü bölümde, yapılan analizlere bağlı olarak bir benzetim çalışması ve sonuçları anlatılmıştır. Bu benzetimde YRKK tipi çeviricinin bir faz ayağı için benzetim koşulmuş, çıkan dalga formları ve akım-gerilim değerlerinin teorik çalışmada elde edilen sonuçlar ile benzeştiği doğrulanmıştır.

Tezin dördüncü kısmı, yapılan tasarım ve uygulama çalışmasına bağlı detayları içermektedir. Bu bölümde ilk olarak sistemin genel şeması ve kontrol kısımları anlatılmıştır. Sistem temel olarak üç ayrı kontrol katmanından oluşmaktadır. Sistem için tasarlanan kontrol unitesi en alt katman olup, yarı iletken anahtarlar için gerekli kontrol sinyallerinin bir üst katman olan ana kontrol ünitesinden gelen emirlere göre, üretilmesinden sorumludur. Tasarlanan kontrol unitesi CPLD tabanlı olup, programlanması VHDL dili ile yapılmıştır. Bu sayede sistemin güvenli ve uzun ömürlü olması amaçlanmış; ve aynı zamanda sistem yazılım yoluyla, ileride yapılabilecek değişikliklere açık hale getirilmiştir. Kontrol ünitesinin, çeviricinin sadece bir ayağını kontrol edecek şekilde tasarlanmış olması sayesinde, çeviricideki doğrultucu ve eviricinin her bir ayağı istenilen şekilde ve farklı kontrol algoritmaları ve zamanlamalarıyla kontrol edilebilecektir. Kontrol unitesi için hazırlanan yazılım, uygun bir test devresi ile test edilmiş ve eksiklikleri giderilmiştir. CPLD'nin seçimi ve kodlanmasının ardından, donanım unitesinin tasarımına geçilmiştir. Donanım unitesinin mümkün olduğunca sağlam, güvenilir ve uzun ömürlü olması istendiği için, fiberoptik kablolarla haberleşebilecek şekilde tasarlanmış ve tasarımı sırasında baskı devre EMI/EMC kurallarına özellikle dikkat edilmiştir. Tasarım tamamlandıktan sonra donanım genel olarak test edilmiş, henüz çevirici inşa edilmemiş olması sebebiyle uygulaması yapılamamıştır. Tezin bu kısmına test devresinden elde edilen sonuçlar eklenmiştir.

Tasarlanan kontrol unitesine ek olarak, sistemin daha güvenilir olması için, yarı iletken anahtarlar üzerinde sıfır gerilimini tesbit eden bir donanım hazırlanmıştır. Bu donanım tasarlanan kontrol unitesi ile haberleşerek, yarı iletken anahtarlar üzerindeki gerilim sıfır olmadan uygunsuz bir anahtarlama işleminin yapılmasını engellemek amacıyla tasarlanmıştır. Bu sebeple yine tezin dördüncü kısmında literatürde varolan bu tip uygulamalara göz atılmış ve uygun bir çözüm önerilmiştir. Önerilen çözüm için gerekli donanım tasarlanıp, test edilmiş ve elde edilen sonuçlar bu bölümün sonuna eklemiştir.

Tezin beşinci kısmında yapılan çalışma özetlenerek ileriye dönük yapılabilecek çalışmalara dair bilgiler verilmiştir.

Yapılan çalışmaya dair genel olarak değerlendirme yapılacak olursa, öncelikle bu çalışma halihazırda E.ON enerji araştırmaları merkezinde (E.ON ERC, Germany) yürütülmekte 5MW'lık çeviricide alt katman kontrol unitesi olarak olarak kullanılacaktır. Böyle bir güç düzeyinde sistemin sağlıklı çalışması ve uzun ömürlü olması, ayrıca kontrol ünitesinin anahtarların kontrolü ile direk sorumlu olması sebebiyle hatasız çalışması çok önemlidir. Dolayısıyla tasarlanan kontrol devresinde hem donanım olarak baskı devre kurallarına ekstra özen gösterilmiş, hem de yazılımda ana kontrol unitesiyle haberleşmenin ve senkronizasyonun sağlıklı bir şekilde işlemesi için gerekli teknikler ve filtreler uygulanmıştır. Çeviricinin henüz inşa edilmemiş olması sebebiyle donanımın sağlayacağı faydalar test edilmemiştir ancak teze eklenmemiş olmakla birlikte çeviricinin tamamı için bir benzetim çalışması yapılarak sağlayabileceği katkı genel gözlenmiştir. Bu benzetim çalışması ve sonuçları başka bir teze konu olacak kadar detay içermesi, ana kontrol unitesi için

henüz uygun konrol metodunun belirlenmemiş olması, ve özellikle sabit zaman kontrolü için yapılan hesaplamalara uygun olarak anahtarlama zamanlamalarının henüz tesbit edilmemiş olması sebepleriyle teze eklenmesi uygun görülmemiştir. Ancak bu benzetim çalışması ve tasarlanan kontrol unitesinin gerçek sistemde uygulanması ileriye dönük yapılabilecek iki temel çalışma konusudur.

Yapılan bu çalışma, yüksek güçte çeviriciler için dual aktif köprü çeviricinin ilk defa yardımcı rezonans kutup komutasyonu ile uygulanması, hem de varolan projeye alt katman kontrol unitesinin tasarlanmış olması sebebiyle faydalı bir çalışma olmuştur.

1. INTRODUCTION

Today, the world is mostly rely on the coal, oil and natural gas to generate the required energy. However, these sources are limited and harmful for the stability of the nature. Due to limited sources and increasing demand for energy, the prices on the market increases and countries are having troubles to supply the needs. Oil, the basic fuel for automotives, produces CO_2 as a result of the combustion process which create environmental pollution. As The Kyoto Protocol has entered into force in 2005, it has been aimed to reduce the greenhouse gases like CO_2, which are the product of fossil fuels. Therefore, because of the increasing prices of non-renewable energy sources, the pollution problem and developments in battery technologies, the use of electricity in automotives have become attractive. The research in this area increases the importance of the power electronics, which is one of the key factor of the technological development to control the power flow and to achieve efficient power conversion.

Another research area for the power electronics engineering is the renewable energy sources. Since it became profitable, the number of the applications of wind and solar energy are increasing rapidly. The installed capacity of the wind energy has already reached 196.630 MW, and in Denmark 21% of the generated energy is provided from the wind turbines [1]. However the applications of wind farms bring new difficulties and challanges to the engineers on the grid side. The wind turbines are mostly equipped with an induction generator, which causes difficulties in the grid management because of the reactive power generated. Besides, the transfer of the power is also another issue which has been to considered. The trend in wind energy technology is focused on building bigger offshore wind farms, where better wind speeds are available. Due to the reactive power demand of AC lines, in these type of application High Voltage Direct Current (HVDC) electric power transmission is a better solution to have more efficient system and to connect two different AC networks which are not synchronized.

In both automotive and wind farm applications, the converter design is one of the critical subjects. In automotive such as electric cars or hybrid vehicles applications, a bidirectional current flow and interface between high voltage and grid might be a good feature to support the grid when it is needed. The desire to recharge the energy storage elements, in a short time means to provide power transfer in several kilowatts. These obviously generate new challanges for both power electronic device producers and design engineers. On the other hand, in wind power, the efforts to design a multi-megawatt range converter for HVDC power transmission from the offshore wind farms is an important research area. In these type of applications, a reliable, sustainable and a flexible system is necessary. The input and output voltage levels are at kV levels, therefore to have high voltage transmission, a converter equipped with a high voltage medium frequency transformer is necessary to decline the weight and volume which leads reducement in construction and installation costs. But the key feature of the transformer is the galvanic isolation. Basically, this kind of a transformer allows efficient, high conversion ratios; enables series/parallel connection of inputs and outputs and is a safety feature as inputs and outputs are not connected electrically. In these applications, the Dual Active Bridge (DAB) is considered as a proper solution to fulfill the needs.

Since the time that it has been invented [2, 3], the dual active bridge converter offers a good solution for high power converter applications with its fexibility in conversion of different voltages in an efficient manner. Besides, the basic control mechanism is easy to implement. However, the soft switching area is limited and the reactive power flow inside of the converter brings extra stresses. To avoid these type problems several control methods has been proposed in literature. In high voltage/high power applications, soft switching on the semiconductor devices is extremely important to protect the converter and to have a longlife system. Therefore, a convenient method is necessary.

On the other hand, during the past years, several soft switching methods has been developed. Basically, the soft switching techniques can be classifed as resonant converters, quasi-resonant converters, soft switching pwm converters and soft transition pwm converters. Auxiliary Resonant Commutated Pole (ARCP) converters as one of the soft transition PWM methods which can achieve zero voltage without making any significant change in the hard switching modulation scheme, is one of

the best methods because of its feasibility to many applications [4]. The ARCP converter is basically composed of a converter with an additional switch set, which assists to the commutation of the switches at the main converter by constituting a resonance on the switch voltage. Therefore, it can be applied to a wide range topology. This thesis aims to design a controller hardware which will combine ARCP with dual active bridge converter to achive soft switched, efficient multi-megawatt converter. The hardware designed is expected to be a part of the control system for the ongoing project, namely 5 MW DC/DC converter for offshore wind farms, at E.ON Energy Research Center, RWTH Aachen.

In chapter 2, the concepts of multi-megawatt converters and dual active bridge converters are introduced. In this part, the research efforts for multi-megawatt converter are shown, the dual active bridge converter is described and the control methods of the dual active bridge converter proposed in literature are mentioned. As it is related with the high power converters, a brief information about IGCT technology is given, which is one of key elements for high power converter design, as being one of the candidate semiconductors with IGBTs for high power application.

At the beginning of the chapter 3, the auxiliary resonant commutated pole is analyzed. Later, the dynamics during the operation of the auxiliary switches are attempted to be investigated and control methods proposed in the literature are studied. The advantages and disadvantages of the ARCP, and the problems which might occur in the converter related with the ARCP are examined. At the end of the chapter, the simulation results are given.

Chapter 4 is dedicated to the design and implementation of the control. First, the control hardware is presented. The complete system scheme is introduced and the task definition of the control unit is made. The design of the control hardware which is a CPLD based controller, is basically composed of two steps: software and hardware design. Both parts are explained seperately in detail and the test results are given. As a part of this thesis and the project, a zero voltage detection (ZVD) circuit is designed. The details of this ZVD circuit and the test results are also presented in this chapter.

The thesis is concluded with the general evaluation of the study and the suggestions related with the future work in the conclusion part.

2. MULTIMEGAWATT CONVERTER

In this chapter the multi-megawatt converter technologies will be investigated. In the introduction part, the motivation for these converters and technology trend will be presented. In the second part, the dual active bridge topology proposed for the multi-megawatt converter will be introduced. Since the converter design is out of scope of this thesis, the converter and the control methods proposed in the literature will be analyzed at a basic level. In the last part, related with the converter technologies, semiconductors for high power high voltage applications will be overviewed. The main focus in this part will be the integrated gate commutated thyristors (IGCTs) and their drivers.

2.1 Introduction

Due to increasing energy demand, and problems related with the limited classical energy sources, the renewable energy sources have become important. However, installation of renewable energy sources creates new challanges to engineers. The transmission of power is one of the important issues to be considered. Especially in long distance power tranmission, it has been shown that the High Voltage Direct Transmission (HVDC) is the more suitable method to be applied since it eliminates the problems related with the AC transmission such as reactive power production which leads losses. In wind power generation which leads the current trend in the renewable energy sources, this issue is highly important because of the application of offshore windparks. Therefore medium voltage DC grids using DC/DC converter have become one of the important research areas. On the other hand, high power DC/DC converters are also used in railway applications. Today's railway systems are generally equipped with heavy, expensive and low efficient on board transformers. Related with the advancements in semiconductor technologies and developments of the medium frequency transformers, these high power DC/DC converters are considered to replace these bulky transformers [5]. In Figure 2.1 several high power DC/DC converter research efforts made by energy institutes and railway companies

for different power and frequency levels has been shown. According to that researches a power level up to 5 MW and a switching frequency up to 20 kHz [6] is now possible for a high power/voltage converter. In these converters, IGBT's or GCT based devices are selected for the main semiconductors to achieve high voltage blocking and a high frequency performance. The converter losses are critical at these level of power, therefore using semiconductors efficiently becomes another important issue. Especially to avoid high switching losses and stresses during the commutation, application of an appropriate soft switching technique is inevitable. The semiconductor drivers especially for GCT's is also very critical in terms of performance. Although the current capability of the high voltage Silicon Carbide (SiC) switches on the market are not sufficient currently, they could also provide some promising results in the near future.

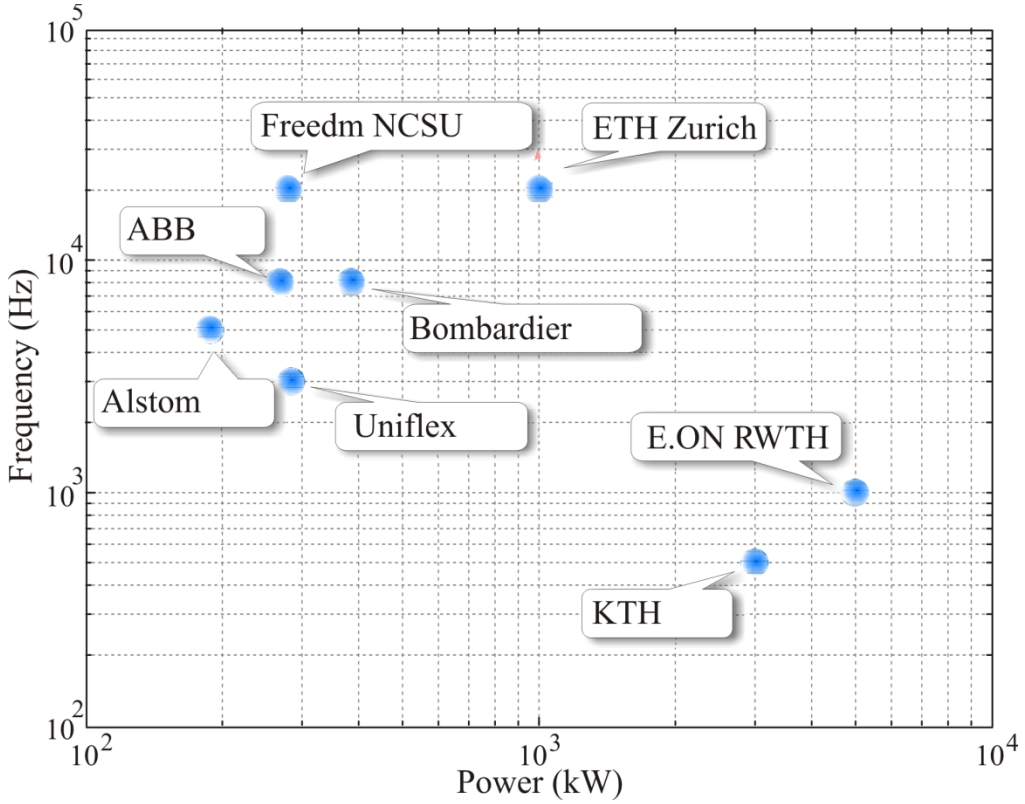


Figure 2.1 : High power DC/DC converter research efforts [6].

Among the high power DC/DC converter applications, the Dual Active Bridge (DAB) and the Series Resonant Converter (SRC) with active output bridge are the two main candidate topologies to achieve high voltage power conversion, soft switching, birectional current flow and isolation between the HV and LV sides [6]. High switching frequencies play a significant role to decrease the size of the

converter elements, especially the transformers. For both topologies the design of the medium frequency transformers is very critical issue since the power density and the isolation between the HV and LV sides is directly related with the efficiency of the converter. Besides, the thermal management of these transformers are more complex when they are compared to the conventional ones. Several studies related with the design considerations of the medium frequency transformers can be found in literature [6, 7]. At E.ON Energy Research Center, RWTH Aachen there has been a small scale prototype based on amorphous core distribution transformer technology developed for medium frequency transformers [8]. Along with this research effort, a 5 MW dual active bridge DC/DC converter is being designed for offshore wind farms. The soft switching area of the dual active bridge is limited within a certain power and voltage conversion ratio, therefore a method to extend this area is necessary. The focus in this thesis on the adaptation of auxiliary resonant pole to dual active bridge converter to extend the area of soft switching for full operation. In the next section the details of dual active bridge converters will be given. The literature research and investigations about the dual active bridge will be used to combine dual active bridge with ARCP, to specify the controller hardware requirements and offer the appropriate switching mechanism.

2.2 Dual Active Bridge Converter

2.2.1 Topology

The dual active bridge topologies was first proposed in [2, 3] (Figure 2.2). Basically the topology is the combination of two active bridges which are connected with a high frequency transformer. The advantages of DAB converter are soft switching, high efficiency, isolation between the input and output voltages and bidirectional current flow. Therefore it could be appropriate especially in the applications for high voltage/power converters and electric vehicles, where a bidirectional DC/DC interface between the battery and the grid is desired. As it is proposed in [2, 3], the active bridges operate in the basic control method with a constant 50% duty cycle, so the output of the each bridge is a square wave. In this topology, the leakage inductance of the transformer is utilized for energy transfer. Therefore a carefully designed transformer with certain stray inductances is required. Between the active bridges a phase shift is provided and the power flow on the leakage inductance of the

transformer is controlled. The soft switching is obtained by ensuring that each switch turns on when its antiparallel diode is conducting which means zero voltage switching. Although there exists the three phase dual active bridge converter, since the operation is similiar with the single phase converter, the analysis will be made for only the single phase one. The operating waveforms of the converter can be seen in Figure 2.4. The transformer can be simplified and modelled with its leakage inductance, since it has been verified that this does not cause any significant discrepancy for the analysis in [2]. The fundamental model of the converter is shown in Figure 2.3. The operation states are described below. Please note that the switching signals of the converters are same for S_1 and S_4 which are complementary to S_2 and S_3. Also at the beginning, the primary current of the transformer is assumed to be negative.

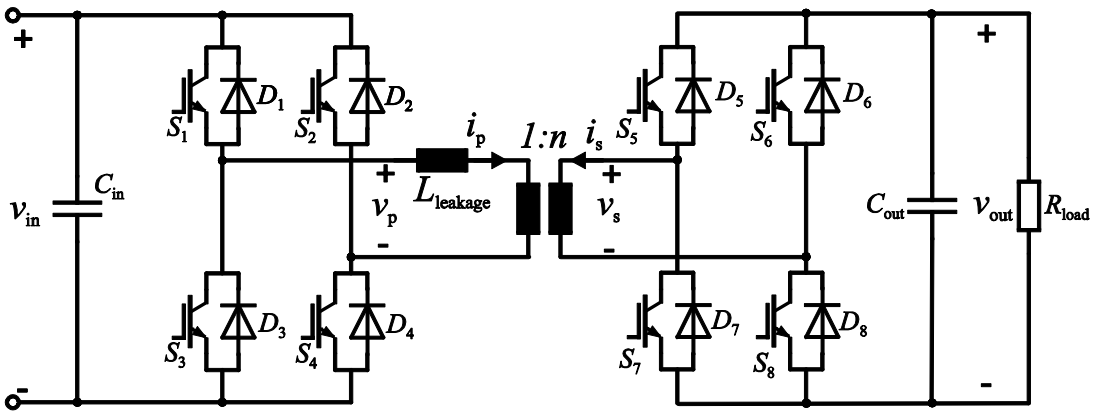


Figure 2.2 : Single phase dual active bridge (DAB) converter.

(a) In the first interval (t_1 - t_0) the voltage on the leakage inductance of the transformer (this could be an additional inductor series to the transformer as well) is $V_{out}/n + V_{in}$, therefore the primary current increases linearly. Since the current on the leakage inductor is negative, the diodes D_1 and D_4 on the input side and the diodes D_6 and D_7 on the output side is conducting. When the current becomes positive, it commutates to the transistors of the switch S_1 and S_4 in the input bridge, S_6 and S_7 in the output bridge.

(b) In the second interval (t_2 - t_1) the voltage on the leakage inductance of the transformer is V_{in} - V_{out}/n therefore in the buck mode operation the current continue to increase with a smaller slope. In this interval the diodes D_7 and D_6 carry the output current.

(c) In the third interval (t_3 - t_2) the operation is essentially the same with the first interval with opposite direction current flow. The diodes D_2 and D_4 on the input side are active and the transition to the transistors T_1 and T_3 occur when the current on the inductance becomes negative. On the output bridge, the switches S_5 and S_8 are actived in this region.

(d) In the last interval (t_4 - t_3) the inductor current decreases linearly with a smaller slope than the previous interval in the buck mode operation since its voltage is V_{out} -V_{in}'. In this interval the diodes D_5 and D_8 carry the output current.

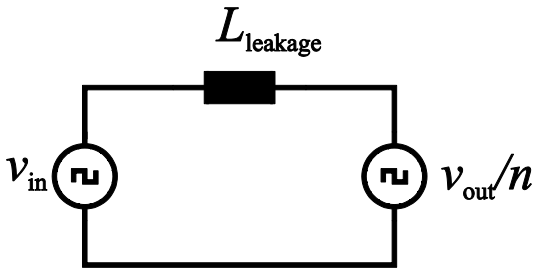


Figure 2.3 : Fundamental model of dual active bridge converter .

Please note that in Figure 2.4 the converter is assumed to be operated in the buck mode operation where $V_{in} > V_{out}/n$. The difference of the boost type operation is that in the second time interval, instead of a slight increase, there occur a slight decrease in the leakage inductor current of the transformer.

From the operation steps it is easy to see that the boundary for the soft switching conditions are $i(0) \leq 0$ for the input bridge and $i(\phi) \geq 0$ for the output bridge. Obviously if these constraints are exceeded, natural commutation will occur in the switching devices. As it is derived in [2] the output power will be:

$$P_0 = \frac{V_{in}^2}{\omega L} D\phi(1 - \frac{\phi}{\pi}) \qquad \textbf{(2.1)}$$

where $D = V_{in} / (V_{out} / n)$. According to the Equation 2.1 the maximum power transfer occur when $\phi = \pi / 2$. This modulation scheme is known as single phase shift (SPS) scheme. Its most important feature is simplicity, and the only control parameter is the phase shift between the input and output voltages of the transformer. On the other hand the problems with this technique are that the soft switching can not be assured for a full operation area [2] and the uncontrolled high reactive power circulating on the transformer. In Figure 2.5 the boundary of soft-hard switching for

different power/phase shift angles in per units ($P_0(pu) = P_0 / (V_{in}^2 / \omega L)$) is given. According to the Figure 2.5, the soft switching can be achieved only for $D=1$, for buck or boost type of operation the operating region is reduced. Especially for the switches with snubbers where the snubber capacitors are employed to have a smaller dv/dt on the transistors during the turn off, operating in the hard switching region could result in device failure during the turn on stage. Therefore to eliminate the problems and extend the area of soft switcing operation, there has been proposed different control methods. In the next subsection these methods will be introduced shortly and their basic advantages and disadvantages will be examined.

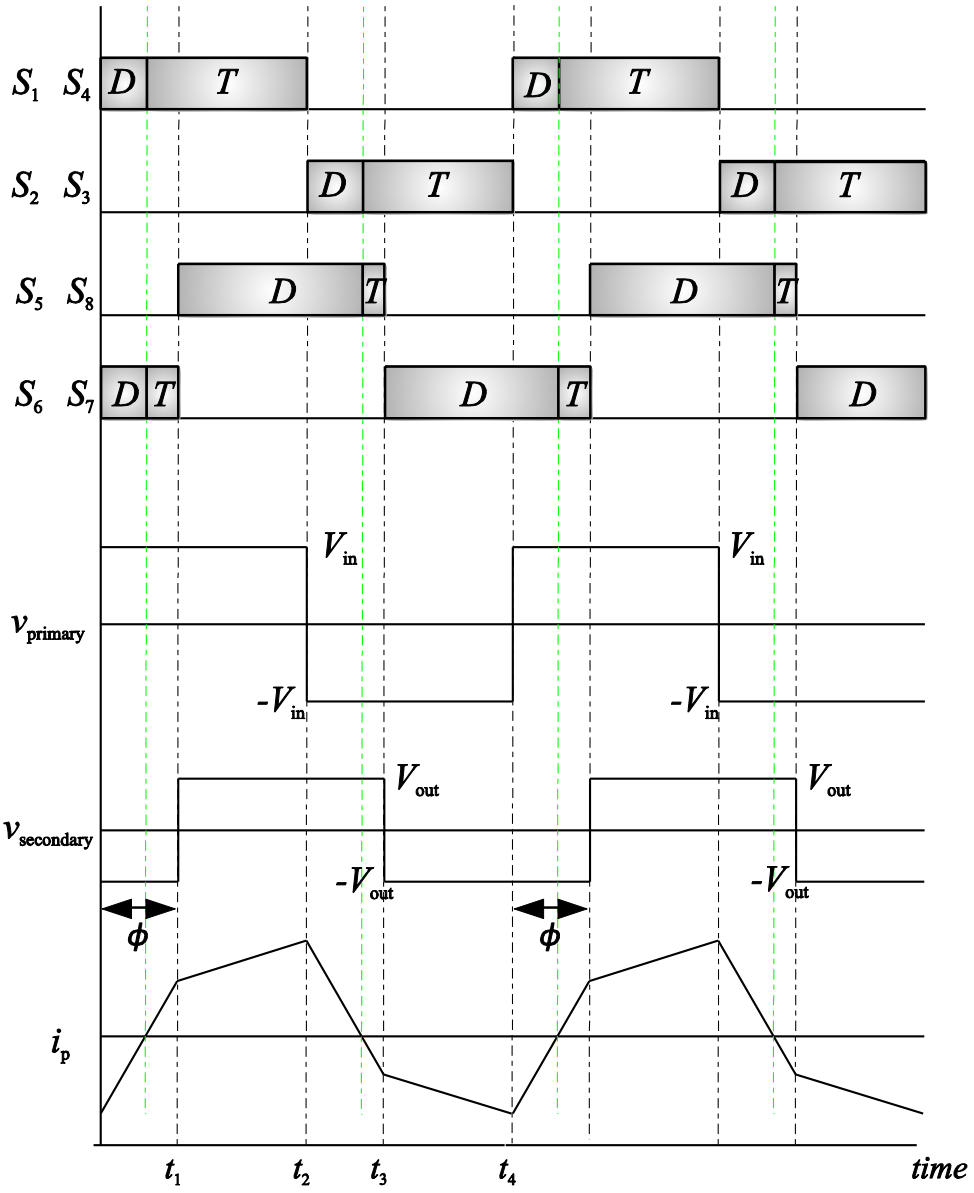


Figure 2.4 : Single phase dual active bridge converter operating waveforms and switching scheme with single phase shift control.

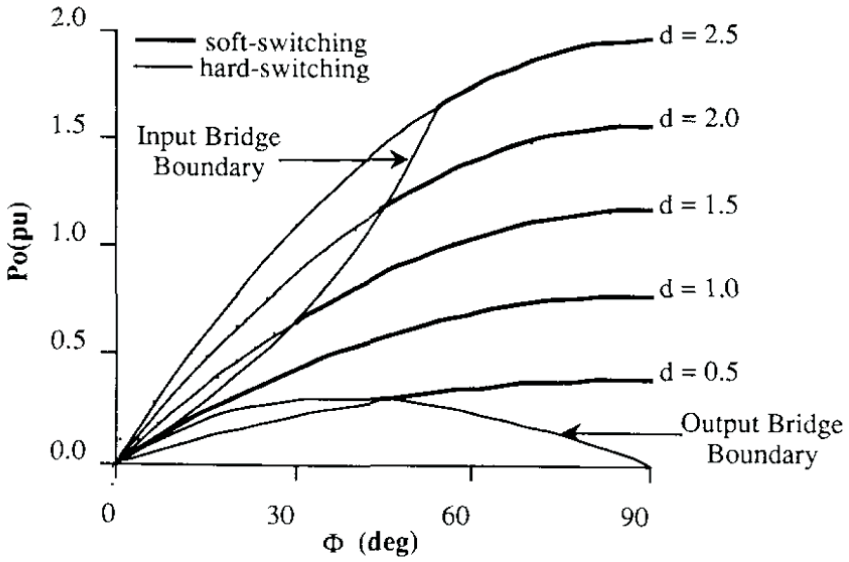


Figure 2.5 : Single phase dual active bridge converter output power vs phase shift (ϕ) [2, 3].

2.2.2 Modulation techniques for dual active bridge converters

2.2.2.1 Triangular modulation

The modulation technique has been introduced in [9]. It basically adjust the duty ratio and phase shift so that the switching occur only when the transformer leakage inductance current is zero or close to zero (ZCS). An example of waveforms for this modulation technique is shown in 2.6.

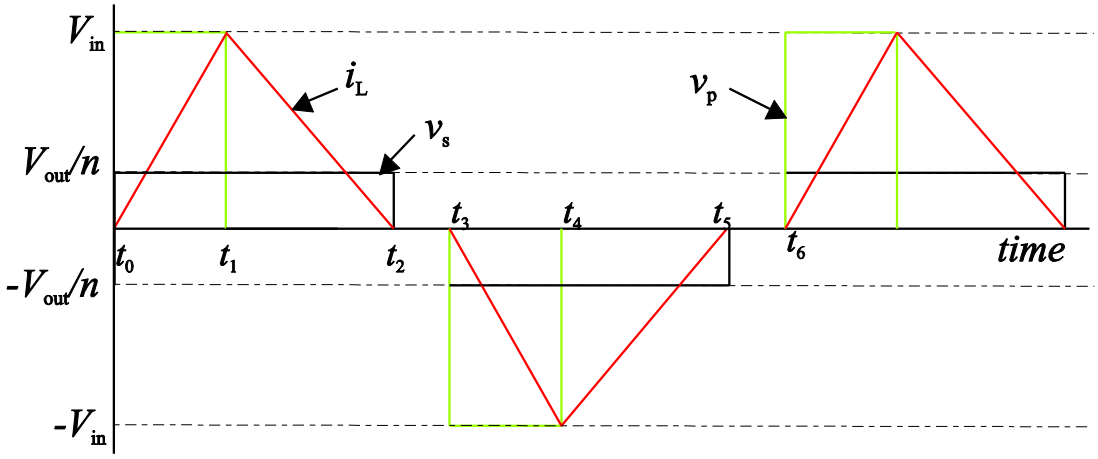


Figure 2.6 : Transformer voltage and current waveforms for TRM technique in DAB converter.

There are three modes of operations in triangular modulation (TRM). In the first interval ($t_0 < t < t_1$) the transformer current rises linearly with a slope $(V_{in}-V_{out}/n)/L$.

In the second interval ($t_1 < t < t_2$) the current decreases linearly with a slope V_{out} / L to zero. The third interval ($t_2 < t < t_3$) is actually employed to adjust the frequency. Please note that in here $V_{in} > V_{out}/n$ is assumed, for the opposite case the current will increase in the opposite direction. The output power is [10]:

$$P_O = \frac{\phi^2 V_{in}(V_{out}/n)^2}{\pi^2 f_s L(V_{in} - V_{out}/n)} \quad \textbf{(2.2)}$$

As it is stated in [9] the maximum power transfer occur for $t_3 - t_2 = 0$. Therefore the operation limit can be found by 2.3, 2.4.

$$P_{TRM,\max} = \frac{V_{out}{}^2(V_{in} - V_{out}/n)}{4 f_s n^2 L V_{in}} \; for \; V_{in} > V_{out}/n \quad \textbf{(2.3)}$$

$$P_{TRM,\max} = \frac{n^2 V_{in}{}^2(V_{out}/n - V_{in})}{4 f_s L V_{out}} \; for \; V_{in} < V_{out}/n \quad \textbf{(2.4)}$$

The important feature of this control method is that the four switches on the output side and the two switches on the input side can operate with ZCS. Obviously to apply this method $V_{in} << V_{out} = n$ or $V_{in} >> V_{out} = n$ must hold, otherwise the transfer power will be small.

2.2.2.2 Trapezoidal modulation

Since in some cases where $V_{in} \approx V_{out} = n$, the maximum power transfer is low in TRM, Trapezoidal Modulation (TZM) is applicable for these cases to have a transfer power $P > P_{TRM,max}$. The inductor current is not zero during the switchings at output side. As it can be seen in Figure 2.7 there are four modes of operation. In the first interval, ($t_0 < t < t_1$) the current rises linearly with a slope V_{in} / L. In the second interval, ($t_1 < t < t_2$) since the secondary side voltage is now equal to the output voltage the current of the transformer increases with a smaller slope $(V_{in} - V_{out}/n) / L$. In the third interval ($t_2 < t < t_3$) the transformer current decreases to zero with a slope $(V_{out}/n) / L$. The last interval is required to adjust the switching frequency as in TRM.

The maximum power transfer for TZM is [10]:

$$P_{TZM,\,max} = \frac{(V_{in}V_{out}/n)^2}{4 f_s L(V_{in}^{\ 2} + V_{in}V_{out}/n + (V_{out}/n)^2} \qquad \textbf{(2.5)}$$

In this method, two of the input and two of the output switches will be operating with ZCS.

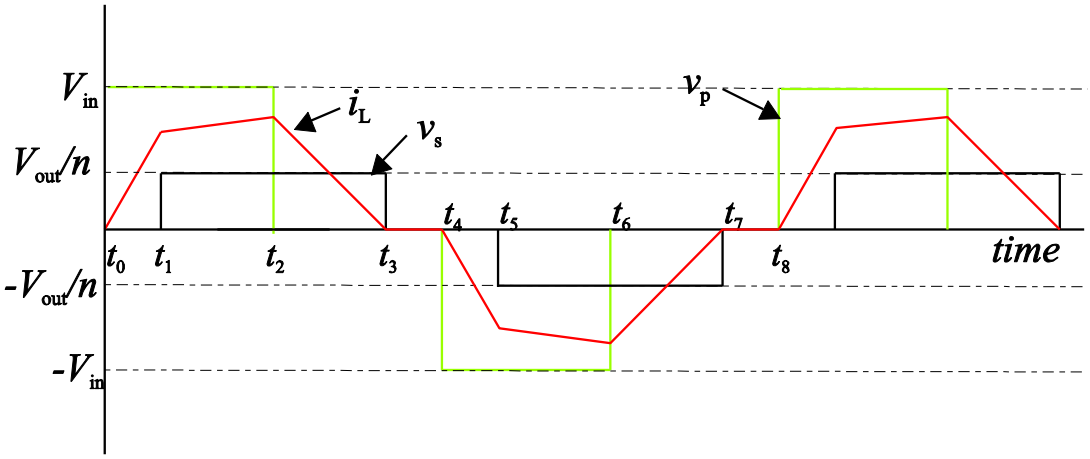


Figure 2.7 : Transformer voltage and current waveforms for TZM technique in DAB converter.

2.2.2.3 Triangular / Trapezoidal modulation

The maximum power transfer of TRM is the minimum power transfer as it is stated before, therefore using both methods alternatively could provide a wide range of operation. For low power transfer TRM and for high power transfer TZM can be used. Since the transformer losses, input bridge losses and output bridge losses are all needed to be considered; an optimization algorithm is necessary.

2.2.2.4 Dual phase shift modulation

Although the combination of TRM/TZM can be operate in wide range power transfer with better efficiency than SPS, the method is difficult to apply in control. Especially the rms current in transformer, transformer losses and the optimization of the leakage inductance requires great attention. Also it has been noted that the rms transformer current is close to SPS in TRM/TZM method [11] therefore, this method does not offer a significant advantage. Therefore in [12] the dual phase shift method modulation (DPS) has been proposed by focusing on the reduction of transformer current. An example of switching scheme and transformer voltages and current waveforms are shown in Figure 2.8.

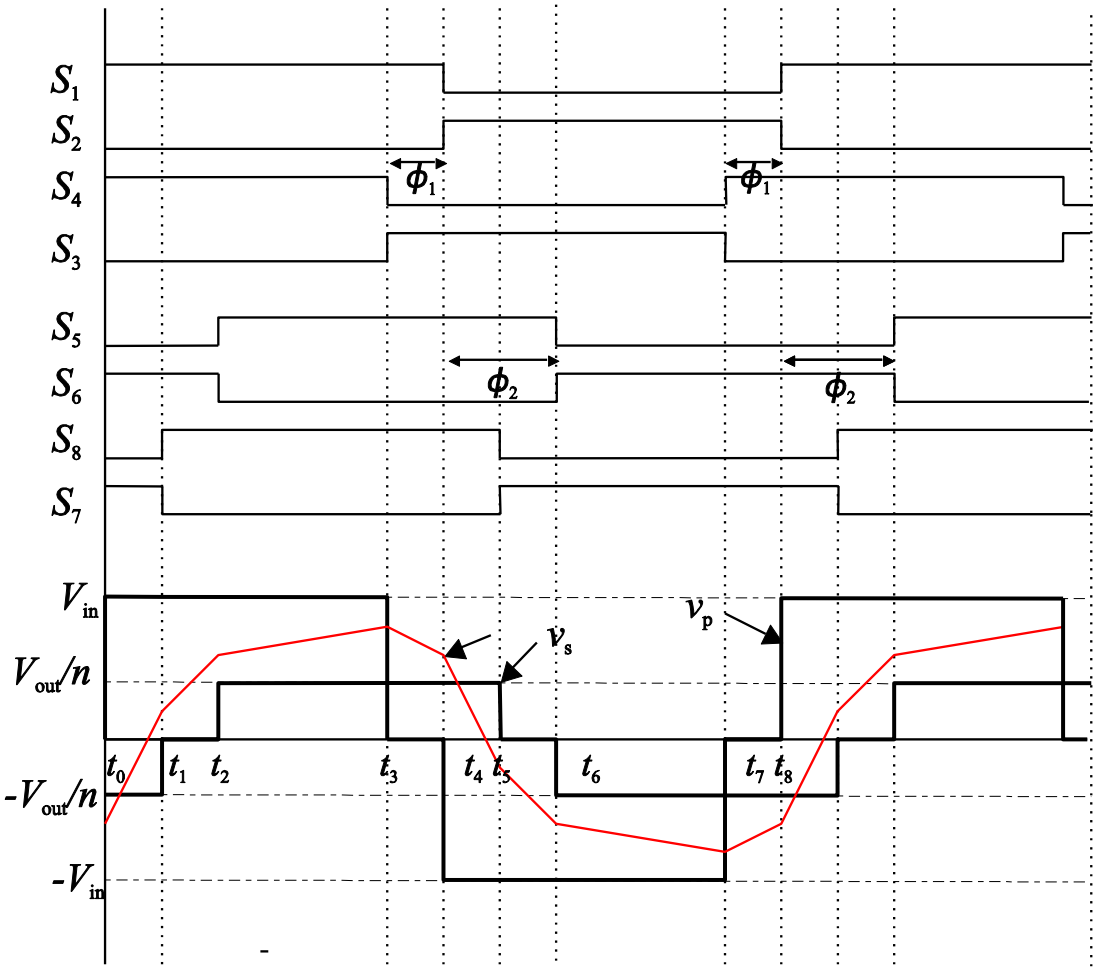


Figure 2.8 : Transformer voltage and current waveforms for DPS technique in DAB converter.

In DPS control, there are two different phase shift parameters one for the phase shift between the two bridges and one for the phase shift between the legs. The total power transfer is expressed with the following [12]:

$$P = \frac{nV_{in}V_{out}}{2f_sL}\begin{cases} \phi_2(2-2\phi_1-\phi_2) & 0 \le \phi_2 \le \phi_1 \\ \phi_2(1-\phi_1\phi_2)-\phi_1-\phi_1^{\,2} & \phi_1 \le \phi_2 \le 1-\phi_1 \\ (1-\phi_1)(1-\phi_2) & 1-\phi_1 \le \phi_2 \le 1 \end{cases} \quad \textbf{(2.6)}$$

Please note that here $\phi_1 \le 1/2$, for $\phi_1 \ge 1/2$ the equation can be found in [12]. The advantages of this method is that in this method more power can be transferred than the standard SPS method. It is also claimed in [12] the reactive power which is inherent in SPS method can be eliminated with dual phase shift.

All the control methods introduced here are generally accompanied with a PI controller to arrange the phase shift and switching timings. The TRM/TZM methods

which are verified experimentally in [9], [11] are basically focused on getting zero current switching to eliminate the losses and increasing operation range. However the method has still problems with the maximum obtainable power transfer and it can be implemented within a limited input/output voltage ratio. The DPS method is focused on the elimination of reactive power and decreasing the rms current on the transformer by introducing a new phase shift parameter between the legs of the full bridges. In [13] which has been published while the studies are running in this thesis, a DPS method has been experimentally veried by also considering the losses which has not been investigated in [12]. However the method still can not achieve ZVS for each switch in some conditions. Moreover, all of these control methods are not very feasible to apply in three phase dual active bridge converter since it is difficult to control the phase shift between the three different phase legs. Therefore, especially for the three level dual active bridge converter, application of an alternative method becomes necessary to widen the soft switching operation range.

The work conducted in this thesis aims to combine a well known topology Auxiliary Resonant Commutated Pole (ARCP) with dual active bridge to achieve soft switching for each switch and to eliminate the losses. The method can be combined with any kind of control method in dual active bridge. In chapter 3 the ARCP converter will be analized in detail.

2.3 Integrated Gate Commutated Thyristors (IGCTs)

The performance of the semiconductor devices in the converter is one of the important design considerations in the project. In this voltage/power range, IGBTs and IGCTs are the most appropriate semiconductor devices where fully controlled switches are required. IGBTs were invented nearly three decades ago and has been widely used in low and medium power applications. These devices compose MOS transistor and bipolar transistor characteristics, therefore they have high power handling capability in medium frequency range. IGBTs are used in a wide range of applications including electric machine drives, UPS and SMPS applications. With the latest developments in the IGBT technology, the devices are now avaliable up to 6.5 kV/900 A [14] ratings in the module packages, therefore they have become also suitable for traction and medim voltage drive purposes.

On the other hand, IGCTs which are thyristor type devices with active turn off capability, are relatively new devices when compared with IGBTs. The term for IGCT is actually used for the combination of the gate driver and the GCT. GCTs are invented as hard driven gate turn off GTOs [15]. Basically the substantional improvements in the GTO such as turn off process, packaging, the inverse diode and the integrated gate driver constitutes IGCT. Because of these improvements, IGCTs can operate at higher frequencies in the snubberless operations with better performances. IGCTs are build in a press pack with their heatsinks and they are the first devices which are integrated with their driver circuitry. Therefore unlike the IGBT, it is not possible to intervene the switching speed with the gate drive circuitry unless a special purpose IGCT has not been intended to be designed.

The IGCT devices are available in the market up to 6.5kV/4000A [16] and they are specifically convenient for high power applications and medium voltage drives. Because of the thyristor type characteristics, IGCTs have better conduction performances than the IGBTs. According the comparison made in [15] the main advantages of the IGBT over IGCT are active control of dv/dt and di/dt, better switching performance especially during turn on because of the transistor type structure, low gate drive power consumption and short circuit protection [17]. On the other hand, IGCT requires less silicon area for the same power level which makes it cheaper, reliable and it has high current handling capability and easier control due to compact design. The multimegawatt converter is expected to operate around 1kHz, with zero voltage turn on at switches for a wide range operation area. The current handling capability and voltage ratings are expected to be around several kA and kV respectively. Besides, the reliability of the converter is very important. Because of these reasons, IGCT type semiconductors are selected as the main switches of the converter in the main converter. Since the control unit will be responsible with the generation of the gate signals to IGCTs, these devices will be investigated in the following sections.

2.3.1 IGCT structure

In Figure 2.9 the internal block diagram of an IGCT has been shown. The gate drive unit is composed of communication elements, turn on and turn off circuitries and a logic unit which monitors and controls the turn off and turn on process according to

the input commands and feedback from the semiconductor device. An internal power supply provides required power to the logic monitoring unit and turn on/off circuitries. The communication with IGCT is provided via optical interface.

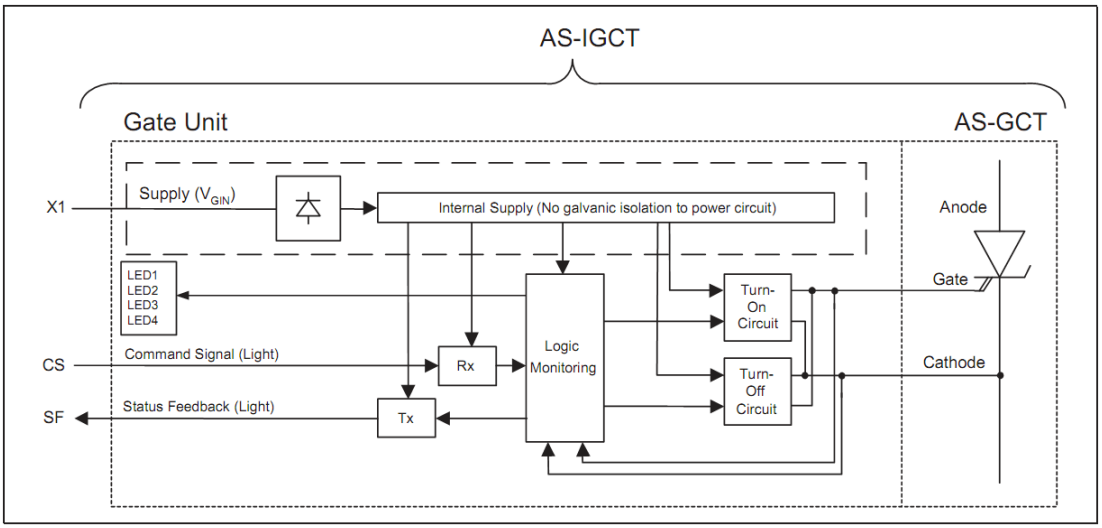


Figure 2.9 : The internal block diagram of an IGCT [18].

As it has been stated IGCTs are thyristor type devices which are composed four layers (Figure 2.10). The turn on and turn off process of the device can be explained simply as follows:

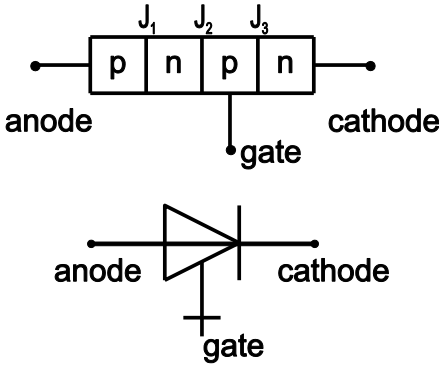


Figure 2.10 : IGCT structure.

2.3.1.1 Off state

During the blocking stage the V_{GC} is kept below a threshold voltage, typically around 1V (Figure 2.11).

2.3.1.2 Turn on

To turn on the device, a pulse gate current applied to the gate and the electron injection across the J_3 junction has been started.

2.3.1.3 On State

During the on state a small gate current is applied to the device to provide uniform current flow through the device (Figure 2.11). The losses during the conduction is relatively small when compared with IGBT, bacause of the thyristor characteristics. The on-state voltage drop can be calculated with the following relation:

$$V_T = V_{T0} + r_D \times I_A \tag{2.1}$$

where V_{TH} is the threshold voltage, r_D is the on-state resistance.

2.3.1.4 Turn off

The device is turned off by applying a negative gate current and commutating the anode current to the gate.

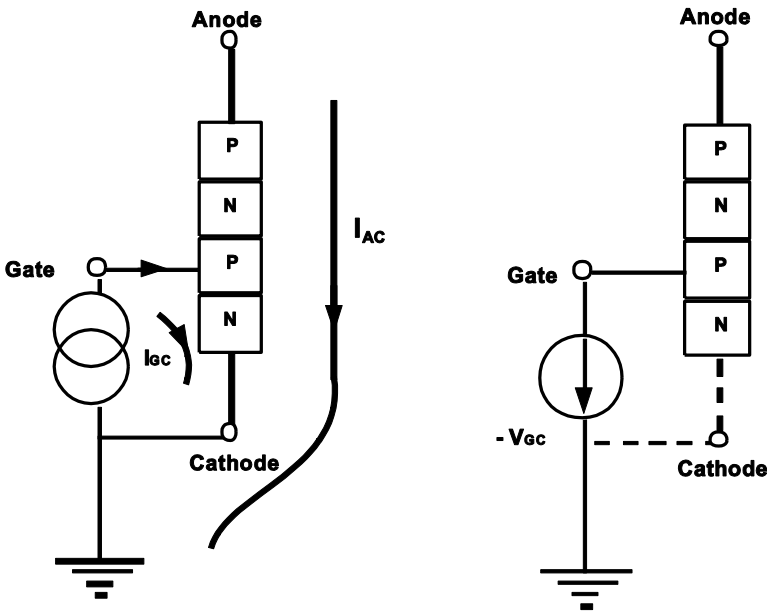


Figure 2.11 : IGCT during conducting (left) and blocking states (right) [19].

Please note that the main difference of the IGCT from a GTO is that during the turn off process the anode current is commutated to the gate before the anode voltage is built up by applying a high negative gate current. A significant advantage of IGCTs is that the device acts like a thyristor during conduction and like a transistor during the turn off. Figure 2.12 shows a typical IGCT gate voltage, anode current and anode to cathode voltage characteristics during the turn off process.

At this point, it is also worthwhile to mention the turn on and turn off circuitries. Typical turn on & turn off circuits are shown in Figure 2.13(a) and 2.13(b)

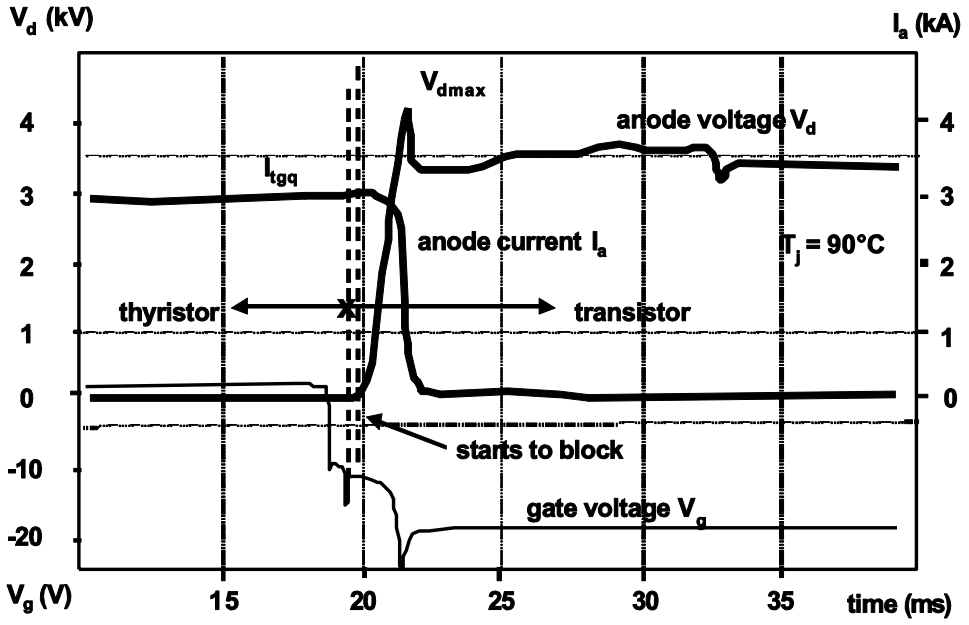


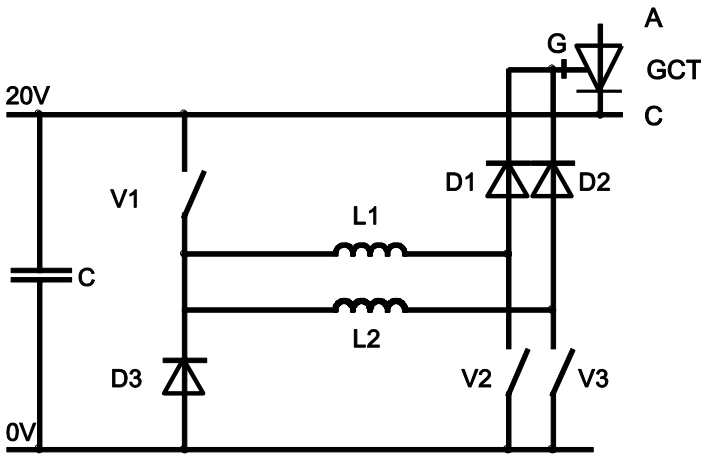
Figure 2.12 : A typical IGCT turn off current and voltage waveforms [19].

respectively [18]. During the turn on process a high *di/dt* transient is required. When switches V_1,V_2 and V_3 are turned on, a pulse current rises on the chokes L_1 and L_2. The current is commutated to gate terminal, by closing first V_2 and then V_3. As the inductance on the gate path is minimized, the fast rise of the gate current leads to a more homogenous transient. The turn off process is provided by closing the switch V_4 in Figure 2.10(b), applying a negative V_{GC}, and commutating the anode current to the gate, before the anode voltage changes. Therefore the turn off circuit must be sufficient to endure the high anode current peak. The required capacitances is provided with paralelled excessive number of capacitors in the gate drive. To minimize the impedance on the gate path the turn off driver is placed as close as possible to the semiconductor.

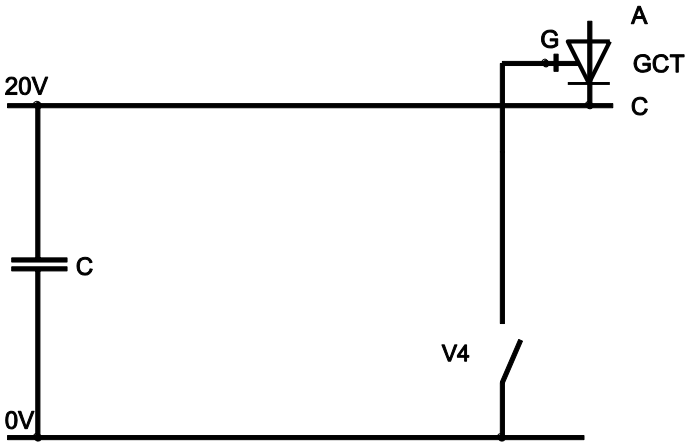
In Figure 2.14 several IGCTs which are products of ABB are shown. IGCTs are produced only in a press pack housing which provides mechanical heatsink and electrical connections. The gate drive circuit is placed with a small gap to avoid the thermal effects.

2.3.2 IGCT application and trends

Generally, the IGCTs were first introduced as a hard driven GTO with several advantages such as snubberless switching capacity ,better switching performance and



a) Typical IGCT turn on circuitry



b) Typical IGCT turn off circuitry

Figure 2.13 : IGCT turn on/off circuitries [18].

more reliability; therefore they quickly replaced the GTO in applications. Currently IGCT is used in STATCOMS, medium voltage drives, interties, and choppers. The device is especially suitable for the applications in the megawatt range. based power modulator and interties up to 100 MW [19]. The research efforts to design PEBBs (power electronic building blocks), which are standardized, compact units that the engineers can apply to a wide range of applications easily, is a part of future trends of IGCTs. In Figure 2.15 an IGCT based water cooled 6 MVA H-bridge or 2-phase converter block MV PEBB power stack has been shown which constitutes one leg of the converter. These block combines semiconductors, cooling units, gate drives communication and protection in a single unit. The designers are only reponsible to provide power and control signals, which decreases the efforts in building complex,

high power applications significantly. IGCTs are especially suitable for these blocks because of the its compact structure.

On the other hand, the current trend on the development of the IGCTs are focused on extending the safe operating area, in other words better power handling capability. Higher voltage ratings is another development issue because of the needs. Currently the ratings are around 6kV, but with the new developments in the structure and doping design of the conventional GCT cell, namely HPT (High Power Technology), it is expected to reach 10kV ratings, which will lead to design of a 3-level 20MW medium voltage drives for 6kA AC machine without any series or parallel connection [21].

Figure 2.14 : Several commercial IGCTs available on the market [18].

The analysis and review made in this chapter about the multimegawatt converter, and high power semiconductors shows that IGCTs are quite suitable for the applications high power/voltage applications if the switching frequency is selected properly. The advantage of IGCT over IGBT during the conduction will lead a better performance. Although the dual active bridge converter promises soft switching up to some level, to have a better performance and a very wide soft switching operation area, development of a new method is necessary. This is also important in the IGCT side because of the its thyristor type structure. Therefore, in this thesis auxiliary resonant commutated pole and dual active bridge converter is aimed to be combined. Actually

in the past a high power ARCP voltage source inverter is developed with IGCT [17], where the inverter shows very promising results around 750Hz switching frequency and 3MVA drive application. Therefore the combination of these two topologies in an IGCT based converter is expected to have high performance. In the next chapter, the auxiliary resonant commutated pole converter will be investigated, and the control methods will be analyzed. According to the analysis, project specifications and project requirements, a stack controller will be designed to control the switches according to the input commands.

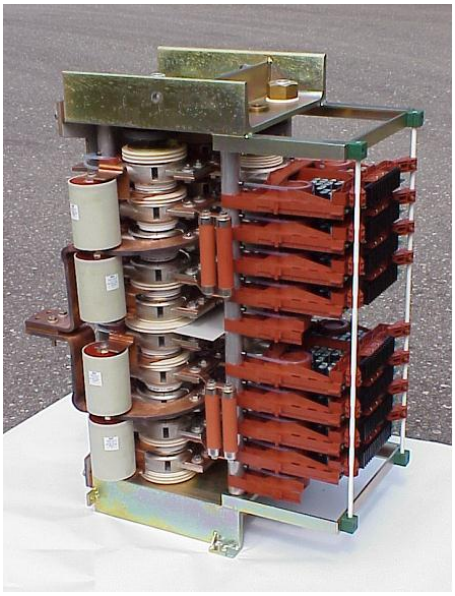


Figure 2.15 : IGCT Power Stack [20].

3. ANALYSIS OF AUXILIARY RESONANT COMMUTATED POLE CONVERTER

In this chapter the ARCP will be introduced and the advantages and the disadvantages of the topology will be investigated. The chapter basically constitutes four parts which are: Introduction, Operation, Control and Simulation. The analysis of the ARCP Inverter has been made for a single phase leg. In the first section, ARCP inverter leg will be introduced. In the second section, basic three operation mode will be analyzed and related calculation will be examined. The thesis mostly focuses on the ARCP control, therefore the analysis will be made deeply. In the third section control methods and their effects will be discussed. The chapter will be completed with the simulation results of the ARCP inverter leg.

3.1 Introduction

The ARCP topology for a phase leg is shown in Figure 3.1. It was first introduced by GE Research and Development in [22, 23]. During the last two decades ARCP has been widely studied and implemented with different topologies and control methods. The main circuit is almost the same for application to different topologies in this method, except the parallel snubber capacitors $C_r/2$ with the main switching devices is a necessity. The auxiliary switching devices are series with a resonant inductor L_r which operate under zero current switching conditions. For positive output current during the turn on process of the upper switch the auxiliary circuit initiates a resonant cycle and the switch can be turned on when the pole current hits the zero voltage. In the same manner, the auxiliary circuit can be used to assist the turn off process. The auxiliary switches are activated only during the commutation process, therefore the dynamics of the converter is mostly protected. Now the detailed analysis of the operation will be given. The operation analysis has been made for a single phase leg, since the switching scheme will be exactly the same for the other legs in both single and three phase converters.

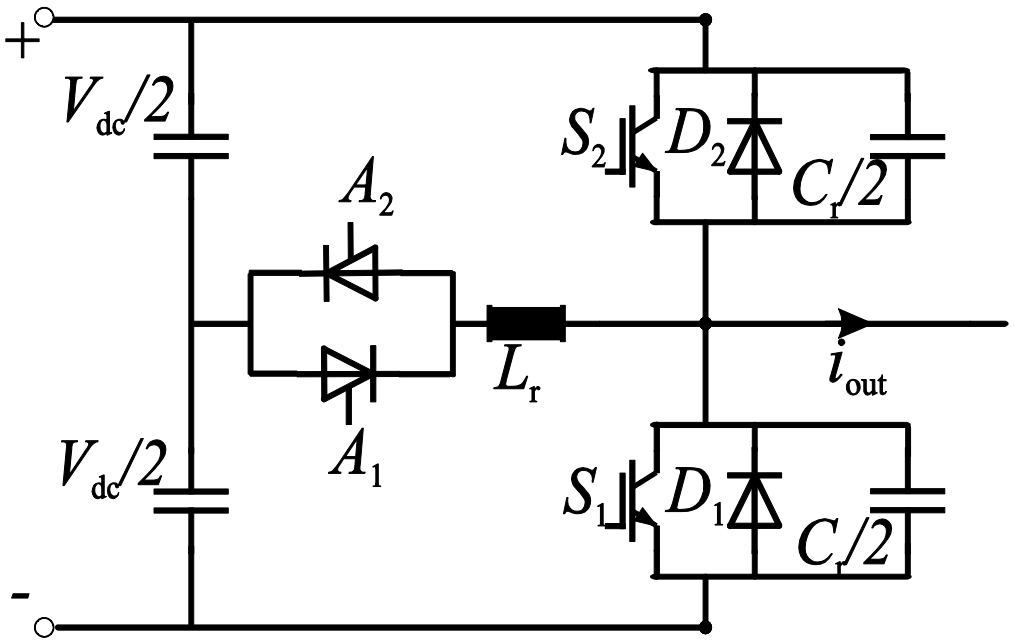


Figure 3.1 : ARCP one phase leg .

3.2 Operation of an ARCP Leg

As it is mentioned, operation principle of the ARCP is simple. Basically, during the commutation, the auxiliary switches help to the discharge of the snubber capacitors. When the voltage of the related capacitor becomes zero, the switches can be turned on safely with zero voltage. Although the principle is essentially simple, the method still requires careful analysis and calculations to prevent problems and to assure safely working conditions. In this part of the thesis, the commutation characteristics for diode and switch will be investigated in detail seperately. For heavy load conditions, the auxiliary switches are not necessarily be employed which will be studied also in this part.

3.2.1 Commutation from diode

To examine the transition where the load is switched from the lower rail to the upper rail, the output has been assumed as positive constant current. For this analysis, all the devices are assumed to be ideal. In Figure 3.2 the voltage and current variations during the transition are shown. Here V_1 represents the voltage across the switch S_1 and I_r represent the current on the resonant inductor. The process is shown in Figure

3.3. Also note that during the analysis for all of the equations, the currents and voltages are defined as in Figure 3.3(a).

a) At first the lower diode is conducting (Figure 3.3(a)) and the voltage on the upper capacitor is V_{dc}.

b) The auxiliary thyristor A_1 is turned on. The voltage on the inductor becomes $V_{DC}/2$. The current on the auxiliary inductor starts to increase linearly with the constant voltage on it. When the diode D_1 current becomes zero it reverse biased, and the switch S_1 becomes conducting. The duration of this period is in Equation 3.1.

$$t_1 - t_0 = \frac{2L_r I_{load}}{V_{DC}} \qquad \textbf{(3.1)}$$

c) With the turn on of the lower switch the boost phase begins. This period is required because of the nonideal behavior of the components and energy losses caused by auxiliary switching period. If this period is missed the zero voltage switching can not be ensured. During this phase the additional energy stored in the inductor is $L_r(I_{boost} - I_{load})^2/2$. The duration of this phase is simply a delay time which should be defined by the requirements of the application. Further information about the delay time control methods will be given in section 3.3.

$$t_2 - t_1 = \Delta t \qquad \textbf{(3.2)}$$

d) When the switch S_1 is turned off the resonant cycle starts. The current present on the switch S_1 diverts to the snubber capacitors. The snubber capacitors and resonant inductor L_r together creates a sinusoidal voltage and current. This phase continues until the voltage on lower switch becomes equal to dc rail voltage. Please note that at the beginning of this phase, the voltage of the S_1 can not increase abruptly because of the snubber capacitors, therefore switching losses are mostly prevented. There will be a small amount of loss related with the current tail in the semiconductor and increase rate of the capacitor voltage. The differential equations for this phase are:

$$i_r - \frac{C_1 dv_{C1}}{dt} + \frac{C_2 dv_{C2}}{dt} = I_{load} \qquad \textbf{(3.3)}$$

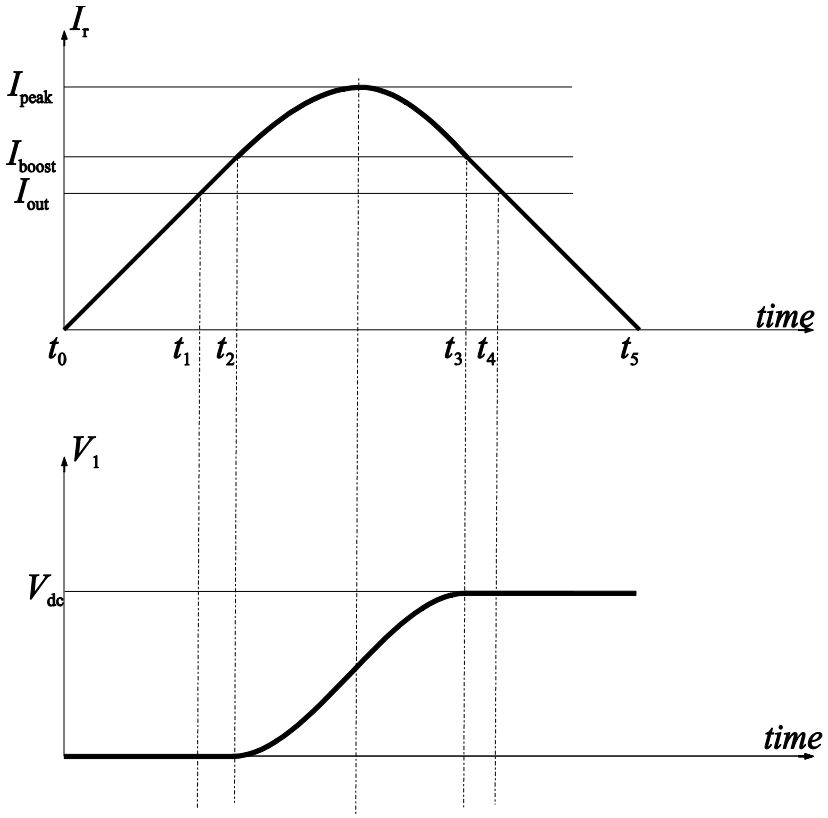


Figure 3.2 : Voltage and current variations during the commutation of diode .

$$\frac{L_r di_r}{dt} + v_{C1} = \frac{V_{DC}}{2} \tag{3.4}$$

where $C_1 = C_2 = C_r / 2$, $i_r(0) = I_{boost}$ and $v_{C1}(0) = 0$. Since $v_{C1} + v_{C2} = V_{DC}$ Equation 3.3 can be simplified as:

$$i_r - \frac{C_r dv_{C1}}{dt} = I_{load} \tag{3.5}$$

If we combine Equations 3.4 and 3.5 with the boundary conditions then the solution for inductor current and capacitor voltage becomes:

$$i_r(t) = I_{load} + (I_{boost} - I_{load})\cos(\omega t) + \left(\frac{V_{DC}}{2\sqrt{L_r/C_r}}\right)\sin(\omega t) \tag{3.6}$$

$$v_{C1}(t) = \frac{V_{DC}}{2} + \left(\sqrt{L_r / C_r}\,(I_{boost} - I_{load})\right)\sin(\omega t) + \frac{V_{DC}}{2}\cos(\omega t) \tag{3.7}$$

where ω is $1/\sqrt{L_r C_r}$. Expression 3.6 and 3.7 can be simplified by using trigonometric manipulations as follows:

$$i_r(t) = I_{load} + \sqrt{(I_{boost} - I_{load})^2 + (\frac{V_{DC}}{2\sqrt{L_r/C_r}})^2}\sin(\omega t + \phi) \quad \textbf{(3.8)}$$

$$v_{C1}(t) = \frac{V_{DC}}{2} + \sqrt{L_r/C_r}\sqrt{(I_{boost} - I_{load})^2 + (\frac{V_{DC}}{2\sqrt{L_r/C_r}})^2}\cos(\omega t + \phi) \quad \textbf{(3.9)}$$

where $\phi = \tan^{-1}((I_{boost} - I_{load})/(\frac{V_{DC}}{2\sqrt{L_r/C_r}}))$. In the latest form of the inductor current, it is easy to see that the peak current value on the auxiliary switch is:

$$i_{peak} = I_{load} + \sqrt{(I_{boost} - I_{load})^2 + (\frac{V_{DC}}{2\sqrt{L_r/C_r}})^2} \quad \textbf{(3.10)}$$

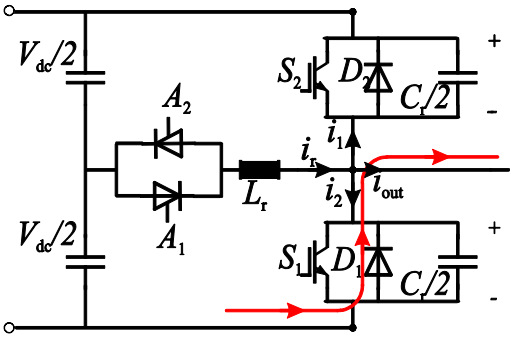
The duration of this phase can be found in Equation 3.12 via Equation 3.11.

$$V_{DC}/2 = \sqrt{L_r/C_r}\sqrt{(I_{boost} - I_{load})^2 + (\frac{V_{DC}}{2\sqrt{L_r/C_r}})^2}\cos(w(t_3 - t_2) + \phi) \quad \textbf{(3.11)}$$

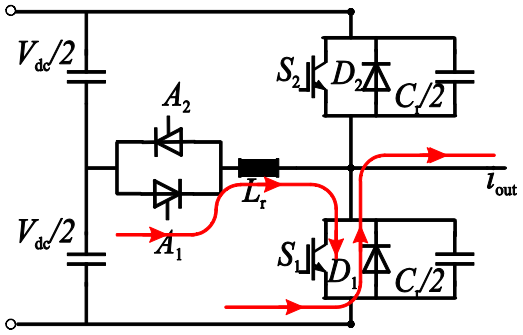
$$t_3 - t_2 = (\cos^{-1}(\frac{V_{DC}/2}{\sqrt{L_r/C_r}\sqrt{(I_{boost} - I_{load})^2 + (\frac{V_{DC}}{2\sqrt{L_r/C_r}})^2}}) - \phi)/\omega \quad \textbf{(3.12)}$$

e) When the voltage on the capacitor C_1 attempts to overshoot the positive dc rail, the diode of the upper side becomes conducting. In this phase switch S_2 can be turned on with zero voltage. This phase continues until the inductor current falls below the load current i.e. the leftover boost energy on the inductor turns back to capacitors. Please note that the voltage of the inductor in this phase is constant, therefore inductor current decreases linearly. The duration of this phase can be calculated as:

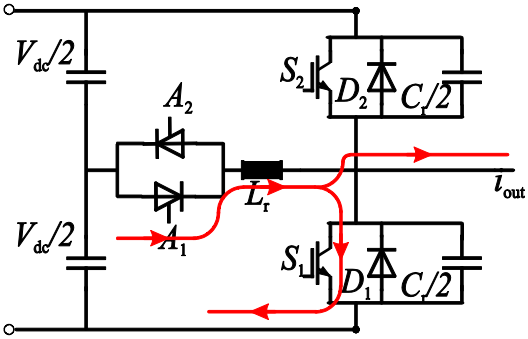
$$t_4 - t_3 = \frac{2L_r(I_{boost} - I_{load})}{V_{DC}} \quad \textbf{(3.13)}$$



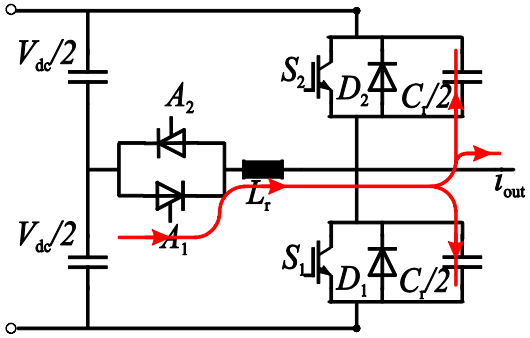
(a) Diode is D_1 conducting



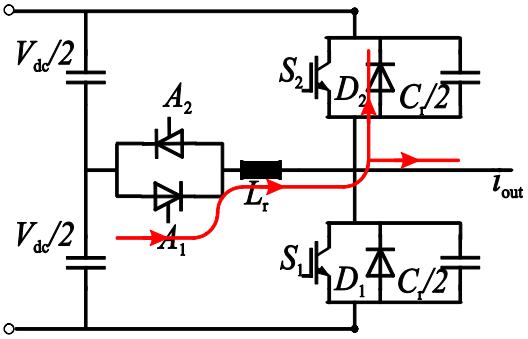
(b) Auxiliary switch A_1 has turned on



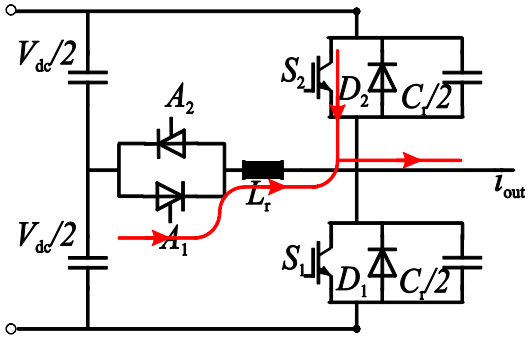
(c) Switch S_1 is turned on diode D_1 is reverse biased



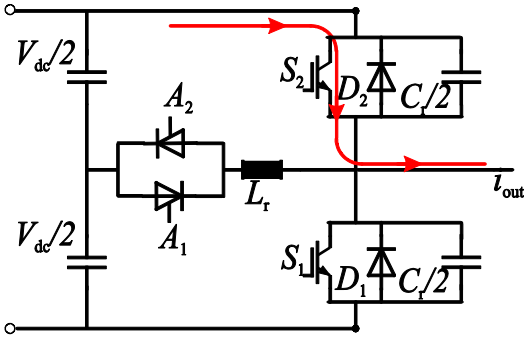
(d) Switch S_1 is turned off



(e) Diode D_2 becomes conducting



(f) Switch S_2 is turned on



(g) Auxiliary switch A_1 is turned off

Figure 3.3 : Commutation of a diode .

f) When I_r decreases below the load current, the switch S_2 becomes conducting and load current is transfered to the switch. I_r decreases linearly until it hits zero. At this point, auxiliary thyristor has turned off naturally. In the applications with IGBTs or GCTs...etc. this semiconductor should be gated off intentionally. The duration of this phase can be calculated as:

$$t_5 - t_4 = \frac{2L_r I_{load}}{V_{DC}} \tag{3.14}$$

g) After the turn off of the auxiliary switch, the converter becomes ready for the next commutation. For a properly functioning commutation with zero voltage switching, it is important to calculate the total duration of the commutation and to arrange the switching signals conveniently. The equation of the complete duration of the commutation is given in Equation 3.15.

$$T_{commutation} = \frac{2L_r I_{load}}{V_{DC}} + \Delta t + t_{resonance} + \frac{2L_r(I_{boost} - I_{load})}{V_{DC}} + \frac{2L_r I_{load}}{V_{DC}} \tag{3.15}$$

$$T_{commutation} = \frac{2L_r(I_{boost} + I_{load})}{V_{DC}} + \Delta t + t_{resonance} \tag{3.16}$$

Please note that Δt, the duration of boost phase, is actually equal to $2L_r(I_{load} - I_{boost})/V_{DC}$. Also in this equation $t_{resonance}$ denotes t_3 - t_2 i.e. the duration of resonance state.

3.2.2 Commutation from switch

The commutation sequence for switch is similiar with the diode case. Here, also it is assumed that the load current is constant and low. For high load current, the auxiliary switch is not necessarily be utilized which will be described in Section 3.2.3. Voltage and current variation during the process is in Figure 3.4 and the process is shown in Figure 3.5.

a) At first, switch S_2 is conducting. When the auxiliary switch A_2 is gated on the boost phase begins.

b) During the boost phase the voltage on the inductor is constant and equal to $V_{DC}/2$. Thus, as in the commutation of diode, the inductor current increases linearly. When it reaches to boost current, the switch S_2 is turned off and the resonance cycle begins. Also as in the previous case, the voltage across the switch can not increase abruptly because of the snubber capacitors, so the losses are prevented. The duration of this phase is:

$$t_2 - t_1 = \frac{2L_r I_{boost}}{V_{DC}} \qquad \textbf{(3.17)}$$

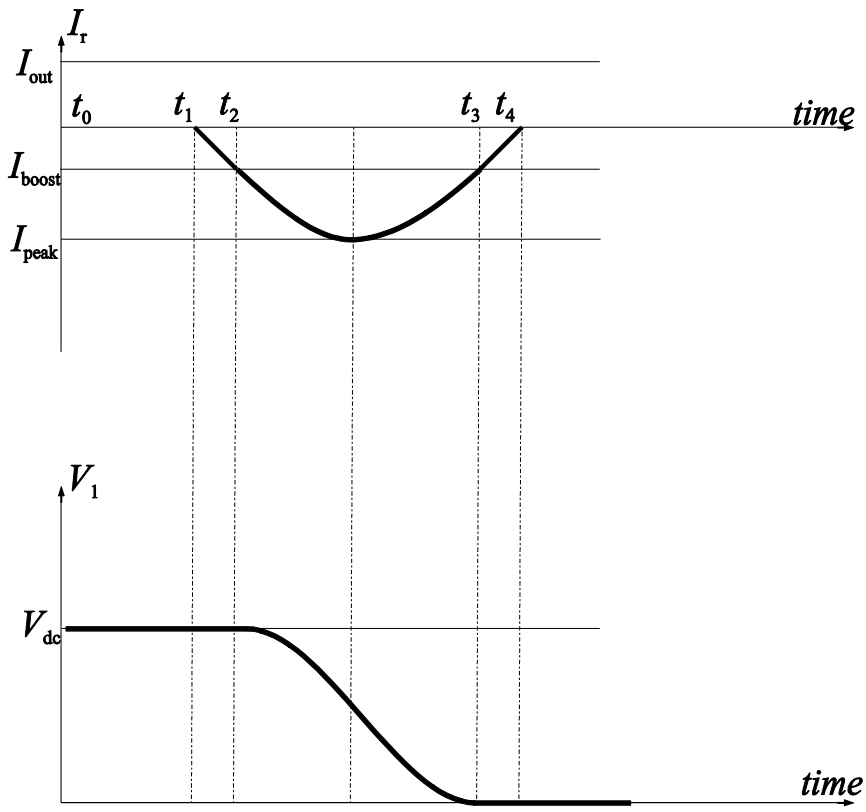


Figure 3.4 : Voltage and current variations during the commutation of switch.

c) With the beginning of the resonant cycle, the current present on the switch S_2 diverts to the snubber capacitors. The snubber capacitors and resonant inductor L_r together creates a sinusoidal voltage and current. This phase continues until the voltage on the lower switch becomes equal to zero. At this point diode D_1 becomes forward biased and the next phase begins. If we define the voltages and currents of the circuit as in the commutation of the diode, the differential equations will be the

same. At the beginning, $i_r(0) = I_{boost}$ and $v_{C1}(0) = V_{DC}$. If we combine them the solution of the equations becomes:

$$i_r(t) = I_{load} + (I_{boost} + I_{load})\cos(\omega t) - \left(\frac{V_{DC}}{2\sqrt{L_r/C_r}}\right)\sin(\omega t) \quad \textbf{(3.18)}$$

$$v_{C1}(t) = \frac{V_{DC}}{2} - \left(\sqrt{L_r/C_r}\,(I_{boost} - I_{load})\right)\sin(\omega t) + \frac{V_{DC}}{2}\cos(\omega t) \quad \textbf{(3.19)}$$

where ω is $1/\sqrt{L_r C_r}$. Expression 3.18 and 3.19 can be simplified by using trigonometric manipulations as follows:

$$i_r(t) = I_{load} - \sqrt{(I_{boost} + I_{load})^2 + \left(\frac{V_{DC}}{2\sqrt{L_r/C_r}}\right)^2}\,\sin(\omega t + \phi) \quad \textbf{(3.20)}$$

$$v_{C1}(t) = \frac{V_{DC}}{2} + \sqrt{L_r/C_r}\sqrt{(I_{boost} + I_{load})^2 + \left(\frac{V_{DC}}{2\sqrt{L_r/C_r}}\right)^2}\,\cos(\omega t + \phi) \quad \textbf{(3.21)}$$

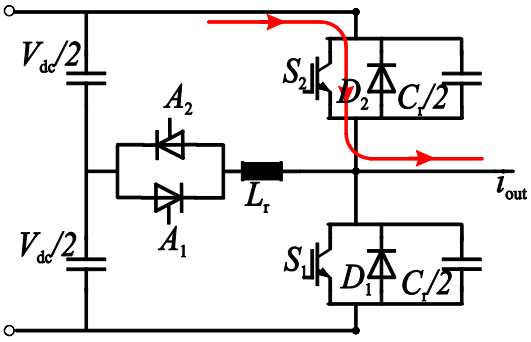
where $\phi = \tan^{-1}\left((I_{boost} + I_{load})/\left(\frac{V_{DC}}{2\sqrt{L_r/C_r}}\right)\right)$. The negative peak inductor current is:

$$i_{peak} = I_{load} - \sqrt{(I_{boost} + I_{load})^2 + \left(\frac{V_{DC}}{2\sqrt{L_r/C_r}}\right)^2} \quad \textbf{(3.22)}$$

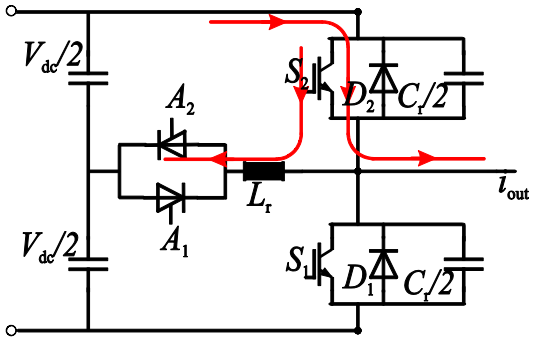
The duration of this phase is:

$$t_3 - t_2 = \left(\cos^{-1}\left(-\frac{V_{DC}/2}{\sqrt{L_r/C_r}\sqrt{(I_{boost} + I_{load})^2 + \left(\frac{V_{DC}}{2\sqrt{L_r/C_r}}\right)^2}}\right) - \phi\right)/\omega \quad \textbf{(3.23)}$$

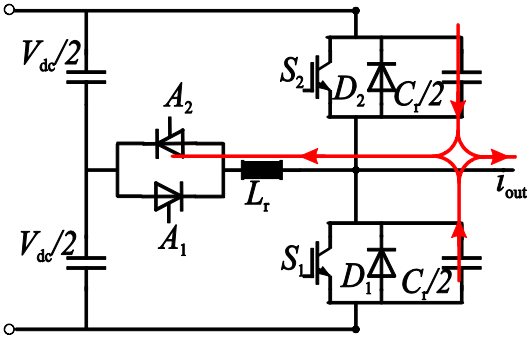
d) In this phase, the remaining boost energy on the inductor turns back to the capacitor. When the current on the inductor becomes equal to zero the auxiliary switch can be gated off. The duration of this phase is:



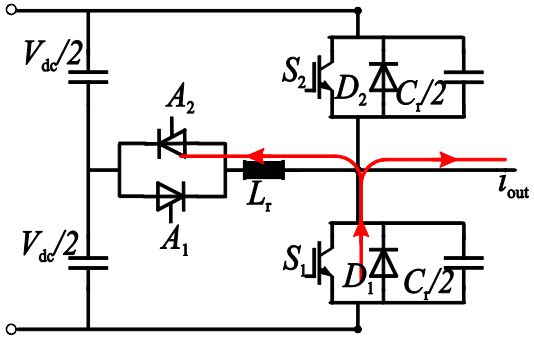
(a) Switch is S_2 conducting



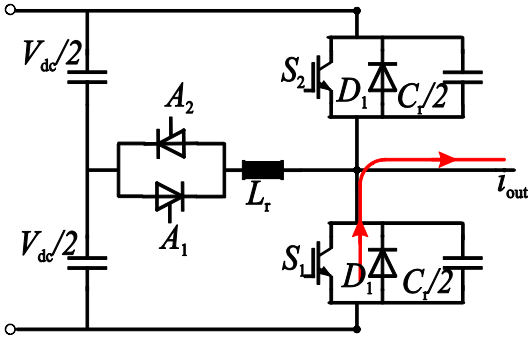
(b) Auxiliary switch A_2 is turned on



(c) Switch S_1 is turned on diode D_1 is reverse biased



(d) Diode D_1 is forward biased



(e) Auxiliary switch A_2 is turned off

Figure 3.5 : Commutation of a switch.

$$t_4 - t_3 = \frac{2L_r I_{boost}}{V_{DC}} \qquad \textbf{(3.24)}$$

When the the auxiliary switch is turned off, the commutation process ends and the circuit becomes available for the next commutation. Total duration of the commutation is in Equation 3.25.

$$T_{commutation} = \frac{4L_r I_{boost}}{V_{DC}} + t_{resonance} \quad \textbf{(3.25)}$$

In both commutation of diode and switch the total duration can be deviated a bit because of the losses during the process. Although zero voltage switching has been ensured in this method, the losses are not disappeared completely since the conduction losses of the auxiliary switches should also be considered. So the designer should be careful and include these losses in his/her calculations. Actually in this topologies, the auxiliary switches are not needed to operate for high load current cases. In the following subsection the operation for high load current will be examined.

3.2.3 Commutation at high load

In this mode of operation, the load current is assumed to be larger than a specific threshold value. The auxiliary switching circuitry is not included to the switching process. The circuit operates similiar to the snubber circuit. The load current is sufficient enough to drive the load voltage to the positive rail.

At first, switch S_2 is conducting and carries the load current. Then instead of turning on the auxiliary switches, the switch S_2 is directly switched off. At this point, the load current starts to drive load voltage to the opposite rail. Load voltage decreases linearly during this phase. When the load voltage becomes equal to zero, diode D_2 becomes forward biased and starts to carry the load current which concludes the switching process. The duration of the switching is:

$$T_{commutation} = \frac{CV_{DC}}{I_{load}} \quad \textbf{(3.26)}$$

The plot of load voltage is in Figure 3.6 and the process is shown in 3.7.

When the strategy is analyzed, the basic advantages of auxiliary resonant commutated pole converter are:

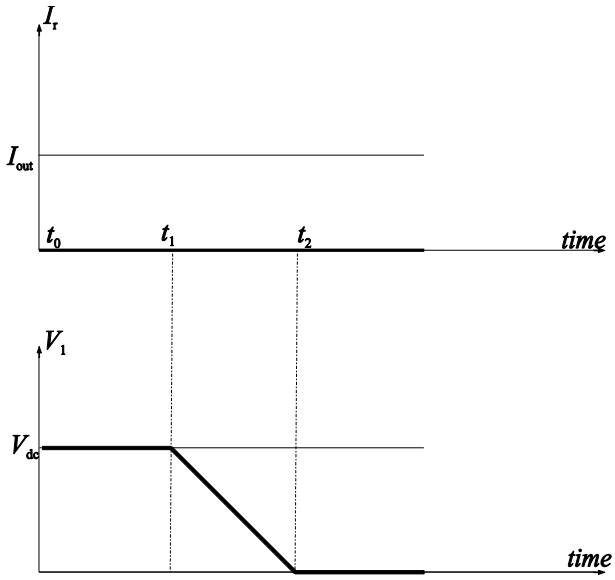
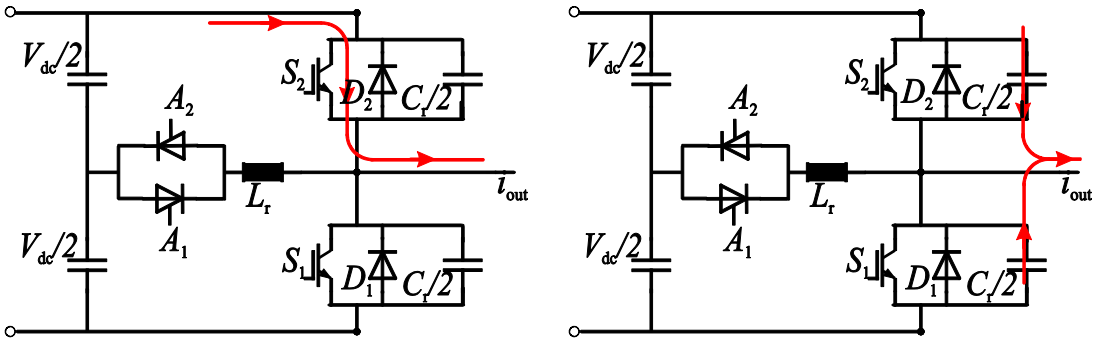
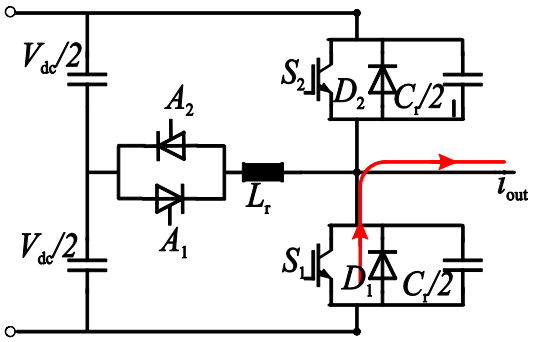


Figure 3.6 : Voltage and current variations during the commutation of a switch at high load current.



(a) Switch is S_2 conducting

(b) Switch S_2 is turned off



(c) Diode D_1 is forward biased

Figure 3.7 : Commutation of a switch at high load current.

- The main PWM scheme is not necessarily be modified.
- Zero voltage turn-on and turn-off can be ensured for both bottom and top main switches.
- There are not any additional stresses on the main switches.
- The method can be applied to different circuit topologies.

On the other hand ARCP has also some disadvantages. Fundamentally, the auxiliary circuitry means some additional costs. However especially for high scaled projects these costs becomes less important when it is compared with the advantages of soft switching. Another disadvantage of the ARCP is the additional complexity. The main switches of the inverter and the auxiliary switches should be synchronized with each other. The boost time of the ARCP and the dead time of the main PWM scheme should be arranged carefully to avoid short circuits in the inverter and unintended stresses on the semiconductors. Before switching off the auxiliary semiconductors, it is necessary to discharge the snubber capacitors which are parallel to the main switches. Otherwise there will occur semiconductor device failures. To avoid these problems the control strategies also needed to be studied. In the next section the basic control methods and strategies will be examined. The problems of ARCP and their solution methods are also be discussed in this section.

3.3 Control Methods

During the commutation process, as it is defined in the expression 3.16 and 3.25, the boost and load currents are effective parameters to determine the duration of the commutation which obviously affects the performance of the inverter. Since the boost current is a function of the boost time, the duration of the boost phase is the critical control parameter. In theory the boost time or the boost current itself can be both be a control parameter. One of the studies on boost time control has been made in [24], in which the output current is measured to extract a value for I_{boost} - I_{load}. The value is used to determine a proper boost time and suitable gate signals for thyristors. Obviously, the method requires accurate current sense and calculation power. Although the method is a good solution to take precautions of switching faults which will be explained later in this section, as it is stated in [24] the implementation of that

kind of a system is difficult and requires too much effort as well as being an expensive solution. And also, it basically controls the boost time. Because of these reasons, in this thesis only the boost time control methods are examined. The boost time control methods can be divided into two main categories which are fixed time control and variable time control [25]. In fixed time control method the turn on time of the auxiliary switches is fixed as it is assumed in the operational analysis of ARCP leg, and it is easy to implement. However, since the load current is not adapted according to the load current, larger current stresses and more power losses are unavodiable. On the other hand in the variable time control method, these disadvantages can be eliminated by setting the duration of the commutation depending on the output current. However, this obviosly increases the complexity of the control and requires a good sensor capability which can be difficult to achieve especially in high power levels. Both methods now will be investigated. Please note that as in the section 3.2 the analysis made for a single ARCP leg.

3.3.1 Fixed time control

In fixed time control method, the switching time is independent of the load current. Therefore the I_{boost} is same for different current levels. In Figure 3.8 and Figure 3.9 the switching scheme for positive current and fixed time control methods are given for low load and high load current cases respectively. If the load current varies in a cycle, the boost current should be fixed, so that the maximum load current becomes smaller than the boost current with a margin. This will lead to more energy storage requirements since $E_{stored} = L_r(I_{boost} - I_{load})^2 /2$. Obviously since the switching pattern will be the same for different current levels, the switching signals can be fixed according to the needs of the circuit which makes the implementation of this method considerably easy. The designer is responsible to determine the needs of the circuit and arranging the deadtime of the main switching signals pattern and triggering the auxiliary switches by considering that needs. For the diode commutation, triggering time of auxiliary switch A_1 (t_1) can be determined by considering the turn off time of the main switch S_2 (t_3) as:

$$t_3 - t_1 = \frac{2L_r I_{max}}{V_{DC}} + \Delta t \qquad \textbf{(3.27)}$$

and for commutation of switch triggering time of auxiliary switch A_2 (t_8) is:

$$t_8 - t_7 = \Delta t \tag{3.28}$$

In light load case, the excessive energy stored in the inductor and extra turn on time of the auxiliary switches causes more losses.

As it was stated before, the auxiliary switches are not necessarily be employed for high output current. This case is shown in Figure 3.10. This will eliminate the conduction losses in the auxiliary switches. However in this case the load current should be enough to discharge the capacitors and drive the V_{S1} to the opposite rail. If the switch S_2 is gated on before V_{S1} reaches to the opposite rail, the power which exists on the snubber capacitor will be dissipated on the switch and possibly destroy the device. Therefore the method can be dangerous for low load current cases if the switching pattern is not carefully designed (Figure 3.11). The threshold current value for the high load current case is given in Equation 3.29 where $t_8 - t_7$ is actually the minimum deadtime between the main switching signals.

$$I_{threshold} = \frac{C_r V_{DC}}{t_8 - t_7} \tag{3.29}$$

Basic solution to avoid this problem is to trigger the auxiliary switch when the load current is below the threshold value and not to use the auxiliary switch when the load is enough to drive the voltage from rail to rail. Another solution is using the auxiliary circuitry in all cases even the load is sufficient to discharge the snubber capacitors. This will decrease the complexity, but will lead more losses. Also using different techniques for the snubber circuitry could be an interesting solution. However these techniques generally cause losses and increase the complexity. Also they can affect the dynamics of the whole system. Therefore, using either first or second solution is more practical.

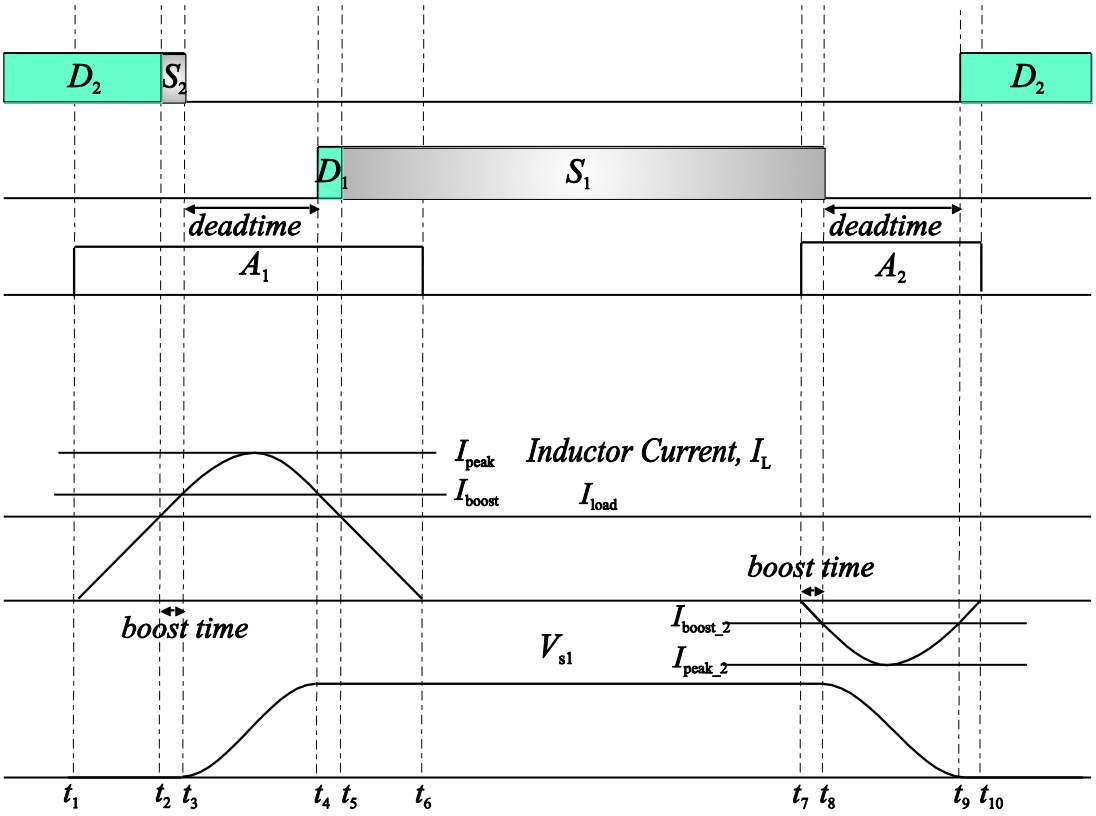


Figure 3.8 : Switching diagram for low load current.

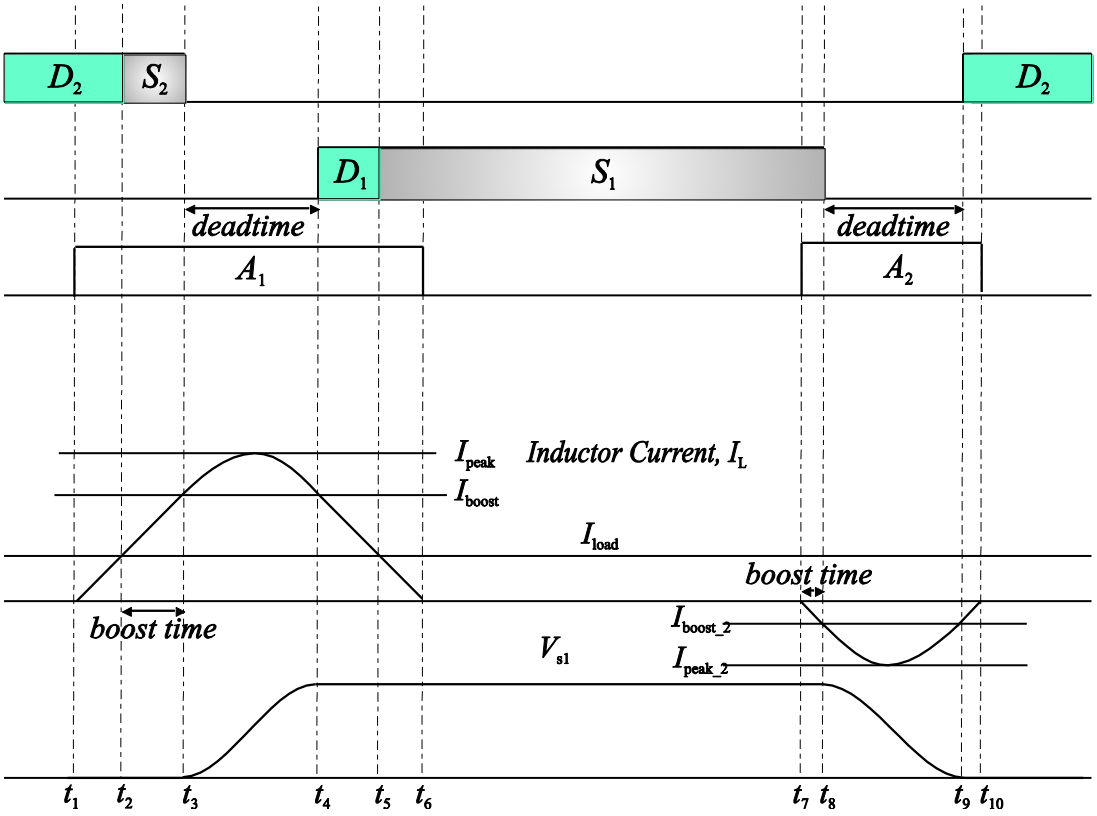


Figure 3.9 : Switching diagram for high load current (aux. switch is effective).

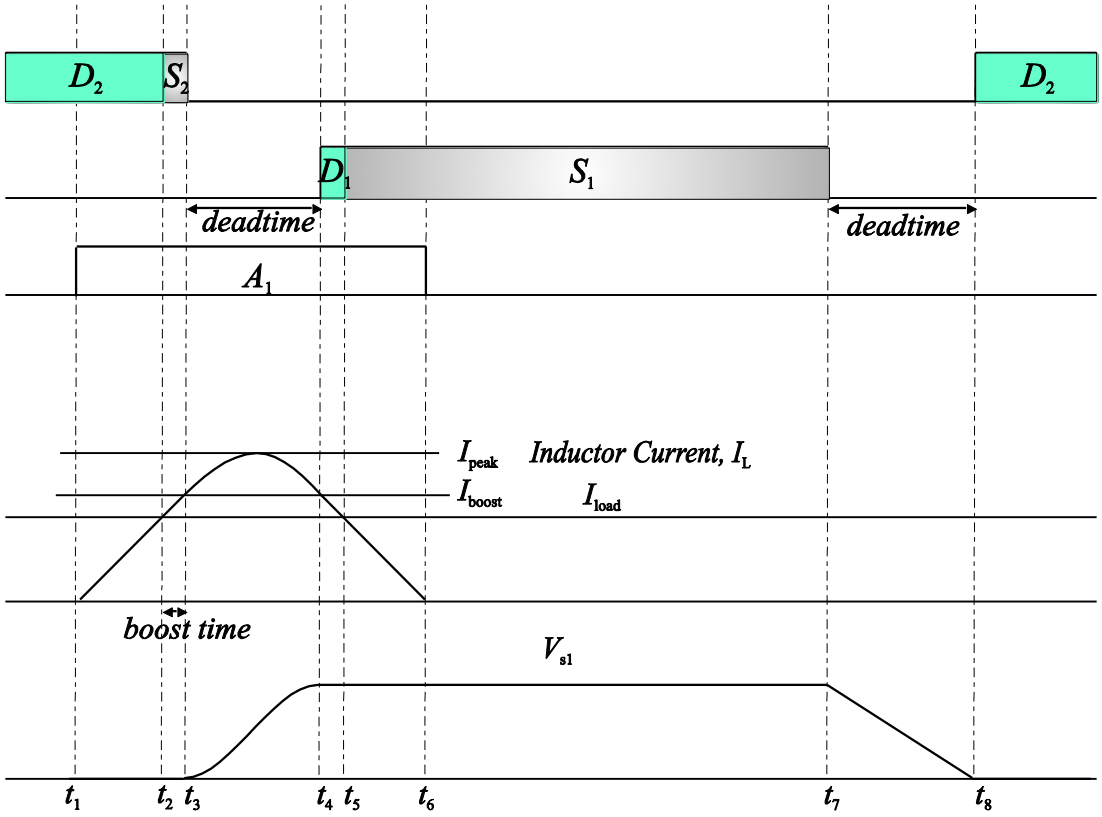


Figure 3.10 : Switching diagram for high load current (aux. switch is ineffective).

3.3.2 Variable time control

In this control scheme, I_{boost} is arranged according to the output load current. Unlike the fixed time control method, here the boost time is fixed so that the auxiliary switches can be triggered for a shorter period in the low load current conditions. The auxiliary switch turn on timing should be determined according to the load current. A sample switching pattern is shown in Figure 3.12. Here all the red dotted lines denote the values and timings associated with the variable time control method. It is obvious that the main switching pattern is still the same. The auxiliary switch is triggered $t_3 - t_1'$ before the turn off of the main switch S_1. This duration can be calculated by combining Equation 3.1 and 3.2 as:

$$t_3 - t_1' = \frac{2L_r I_{max}}{V_{DC}} + \Delta t \qquad \textbf{(3.27)}$$

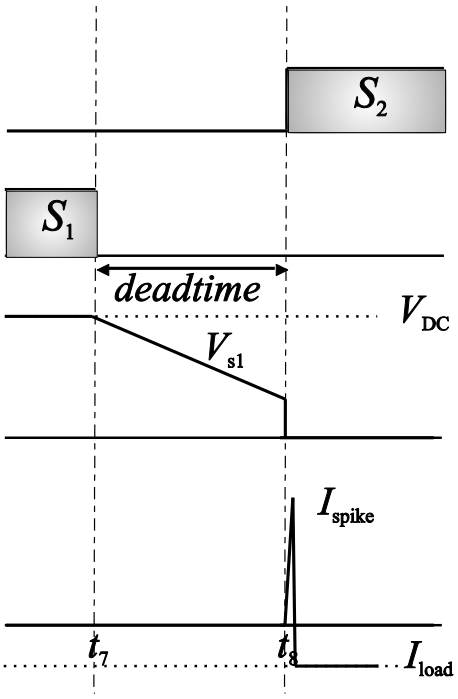


Figure 3.11 : Problem in low load case (aux. switch is ineffective).

As it can be seen in Figure 3.12 with this method, peak of the inductor current will be lower in light load conditions. In both control methods the resonance phase duration is fixed and only dependent on the resonance capacitor and inductor as in Equation 3.12, therefore the deadtime of the main control and the resonance elements can be calculated without much effort. Also similiary in fixed time control method, the auxiliary swithes is not needed to be used during the commutation of switch as in fixed time control method for the heavy load case.

Although this method can reduce the losses and stresses on the semiconductors, it has a significant disadvantage which is that the load current should be sensed and the auxiliary switch trigger signals should be arranged. Therefore it increases sensor cost and control complexity. The analysis made in [25] claims that the variable control method does not provide significant improvement in efficiency, but could be useful to reduce the stresses on the devices i.e. maximum current. In control hardware design, the fixed time control method has been chosen because of the useful nature of the dual active bridge topology in which the switching signals can be fixed to a certain frequency with 50% percent duty cycle as it was described in chapter 2 for SPS control method.

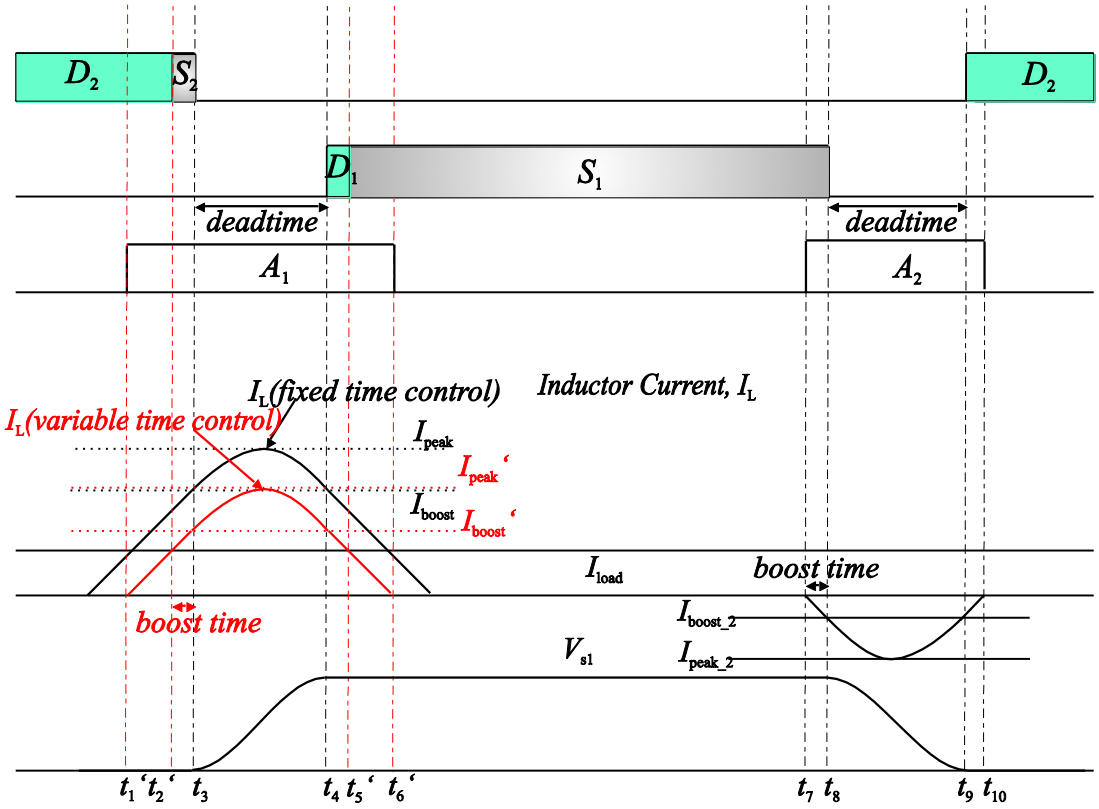


Figure 3.12 : Switching diagram for variable time control method.

3.4 Simulation of an ARCP Leg

In order to verify the analysis the ARCP converter has been simulated for one leg by using Ansoft Simplorer 7.0. The simulation schematic is shown in Figure 3.13. The characteristics of the switching elements are modelled by using exponential function, and the circuit elements are lossless. The output is modelled as a current source for simplicity. The parallel diodes to the auxiliary thyristors are included to allow reverse direction current flow and GTOs are used for the main switches as it is done in the main reference of ARCP [22]. The simulation parameters are in table 3.1.

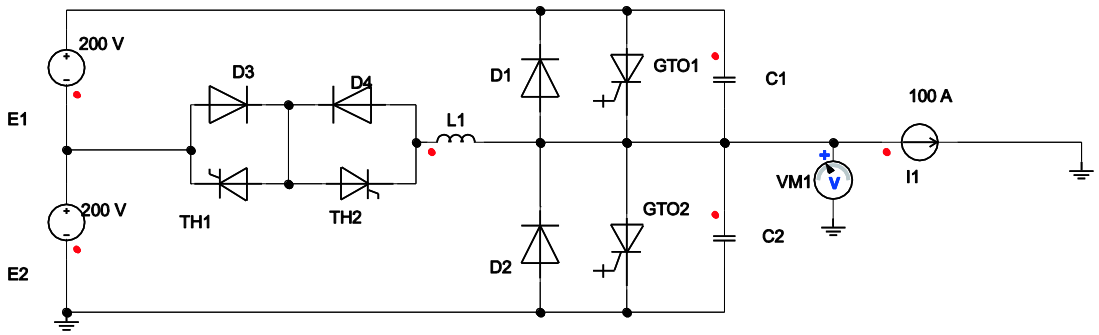


Figure 3.13 : Simulation schematic for an ARCP Leg.

Table 3.1 : Simulation parameters.

V_{DC}	400 V
I_{out} (for heavy load conditions)	100 Ampers
I_{out} (for light load conditions)	10 Ampers
L_r (resonant inductor)	50µH
$C_r/2$ (snubber capacitor)	3µF
f (switching frequency)	1kHz
deadtime	100µsec
boost-time	35µsec

For heavy and light load conditions the output current is selected as 100A and 10A respectively. In the simulation fixed time control method is applied, in other words the boost-time is fixed as 35µsec. The deadtime between the high and low switching signals is 50µsec. The snubber capacitors are 3µF for each GTO, therefore the effective resonance capacitance is 6µF. The switching frequency is selected as 1kHz. For heavy load condition the voltage transition and resonant current waveform is given in Figure 3.14. As it can be calculated by 3.10 the maximum current is around 170A in commutation of diode. Since the load current is high, the difference between the load current and boost current is reasonable (22 A). The The resonance duration, i.e the voltage transition time is consistent with the calculations which is around 43µsec. Similiarly, the waveforms of commutation of the switch are proper, as they are expected and they match up with the calculations. In Figure 3.15 the implemented control signals for this simuation is given.

In Figure 3.16 the circuit simulated without triggering the the ARCP thyristor TH_2 during the switch commutation. Since the load is high enough the commutation occurred naturally and zero voltage switching is ensured. However when the load is decreased, the situation is different. As it is stated earlier, this time the load is not capable of discharging or charging the capacitors, therefore the voltage transition can not be completed before the upper GTO is turned. Obviously, this will cause losses and the sudden voltage change on the snubber capacitor will result in high current spikes on the transistor which can destroy the device as it is stated earlier and shown in Figure 3.11. To prevent this, either the ARCP switches should be utilized always, or the output current is monitored and the commutation duration is calculated to determine where the ARCP assistance needed to be applied. The results of the triggering the ARCP thyristor during the commutation is shown in Figure 3.18. As it is expected the commutation occur in a safely manner.

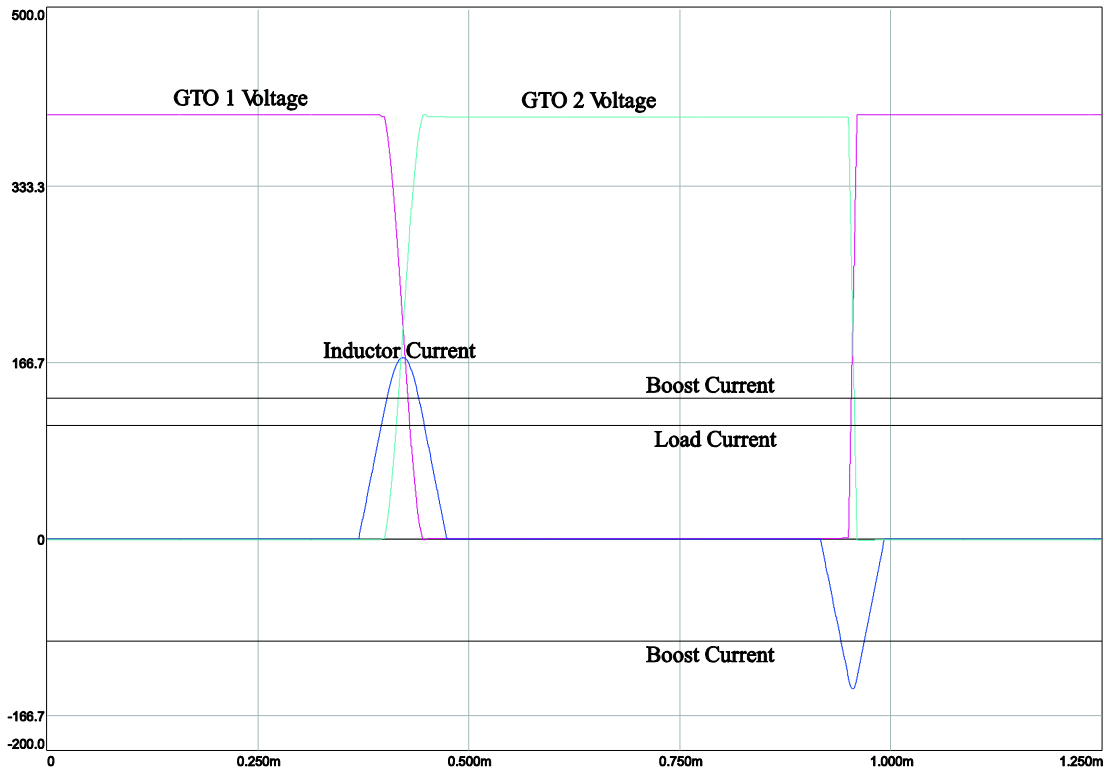


Figure 3.14 : Voltage transitions and Resonant inductor current with ARCP.

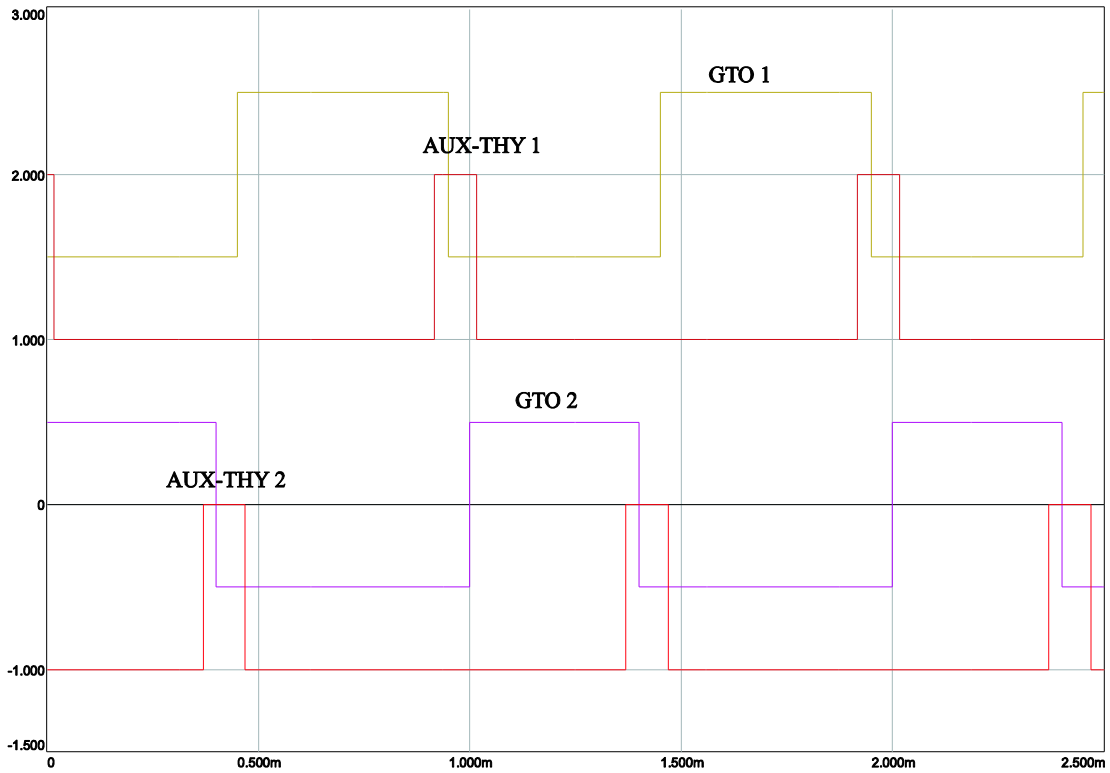


Figure 3.15 : Switching signals for Figure 3.14.

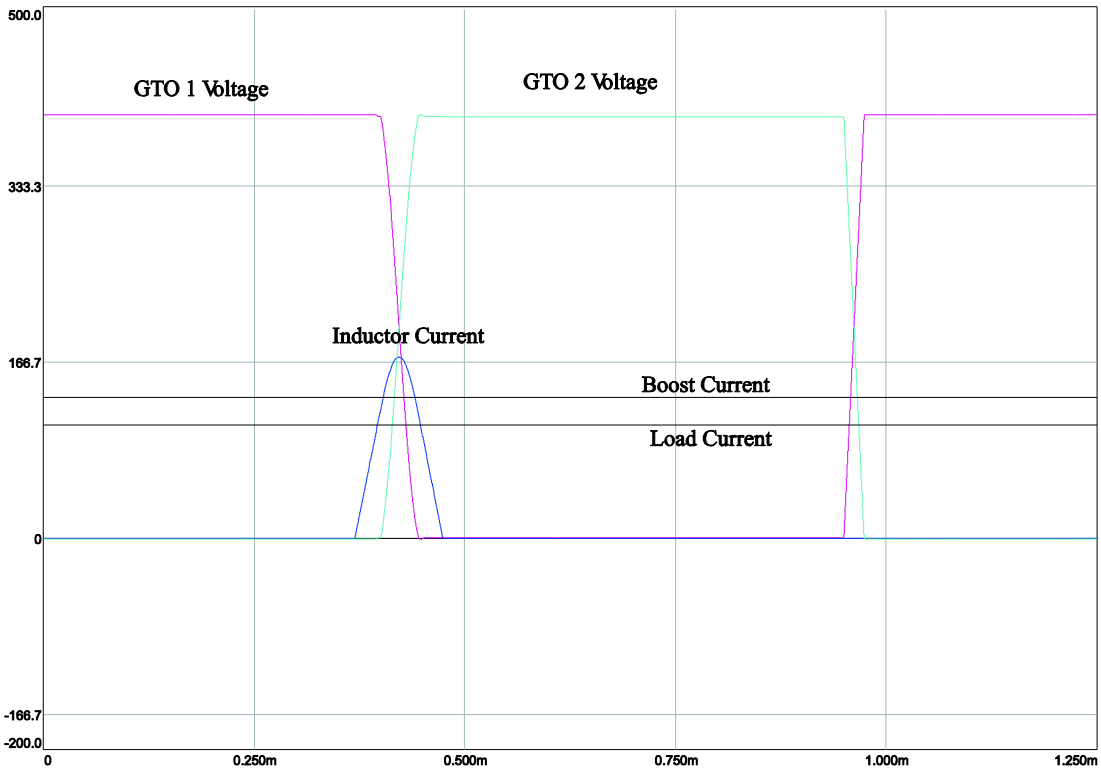


Figure 3.16 : Voltage transitions and resonant inductor current without switching on ARCP switches during the switch commutation (Heavy load).

Figure 3.17 : Voltage transitions and resonant inductor current without switching on ARCP switches during the switch commutation (Light load).

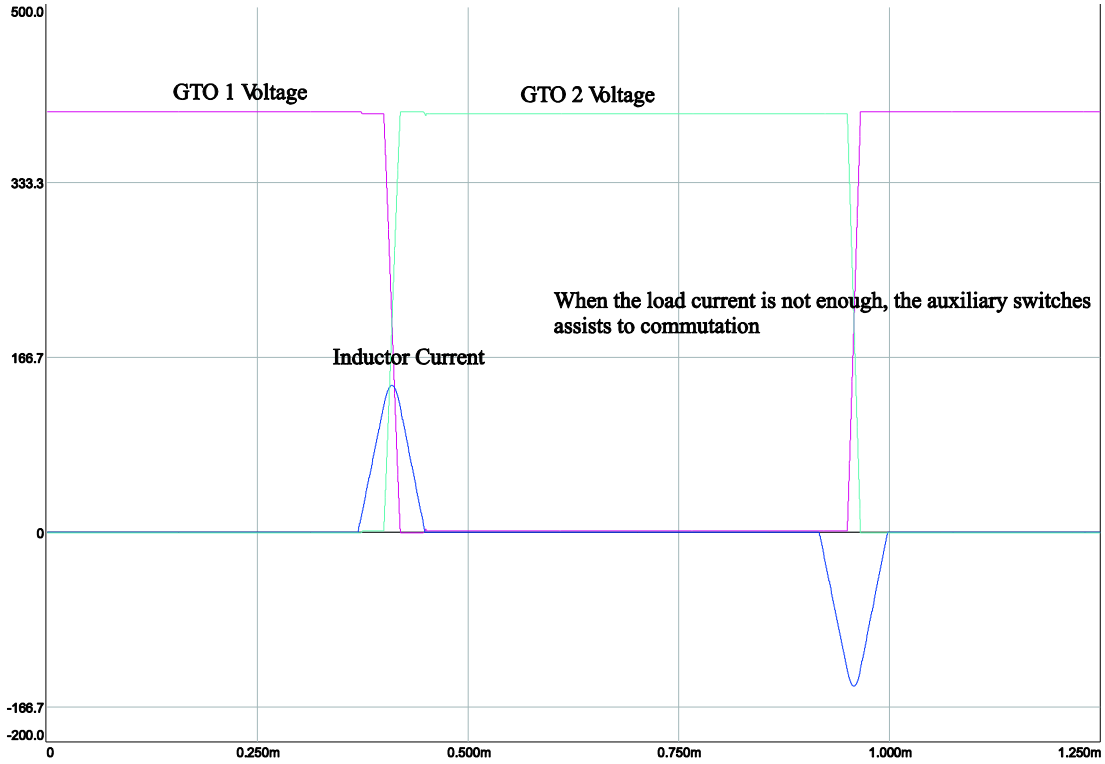


Figure 3.18 : Voltage transitions and resonant inductor current with switching on ARCP switches during the switch commutation (Light load).

In the low load case (Figure 3.18) although the load current is 10A, the current on the inductor is around 170A. This obviously result in excessive losses and additional stresses on the auxiliary switches. Therefore in some cases, where the losses are significant and important, it can be a good idea to apply variable control method.

4. CONTROL HARDWARE DESIGN

In this chapter of the thesis, the design of the control hardware will be introduced. In the first section, the requirements of the control hardware will be determined and the whole control scheme of the converter will be presented. The second section explains the implemented control software and control signals scheme. In the last part, realized control hardware, namely stack control unit which generates the control signals of the power stacks according to the input of the main controller will be presented and the test results will be given. The control hardware is accompanied with a zero voltage detection circuit (ZVD) to ensure safe operation. The design procedure of the ZVD circuit and the realized circuit is included also in this section.

4.1 Introduction

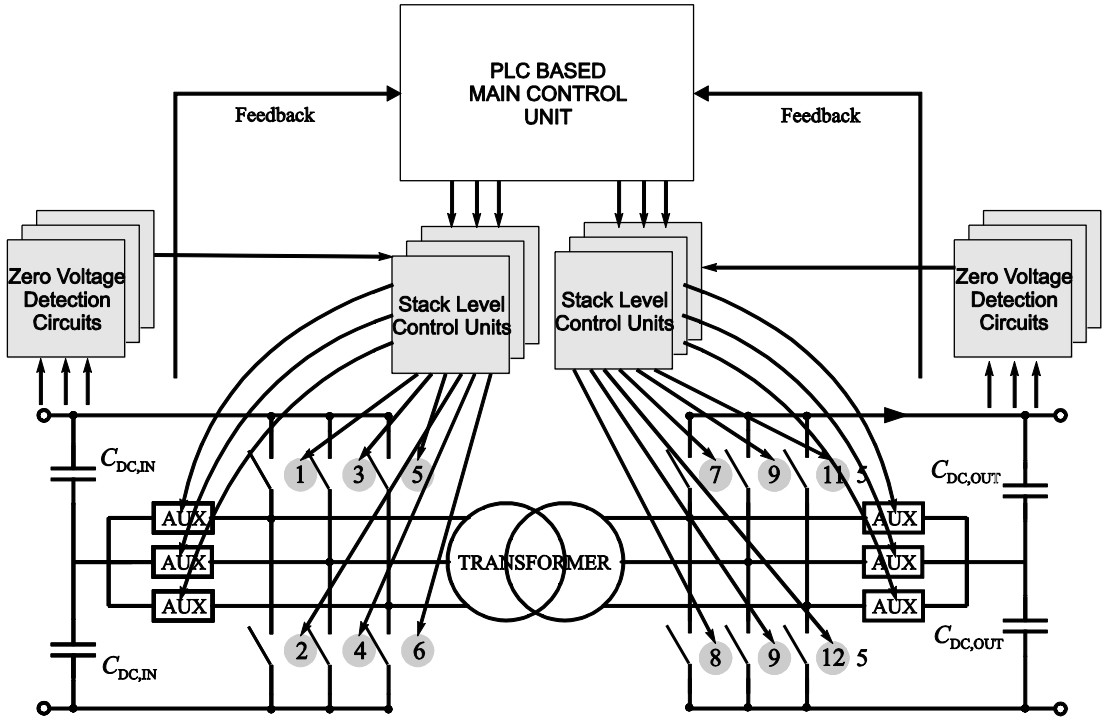


Figure 4.1 : Complete converter scheme.

Complete converter system is shown in Figure 4.1. Since the converter has not been completely built up yet, the converter will be explained according to the first projections of the project. The converter part is a three level dual active bridge converter. For each leg of the converter there is a seperate auxiliary switching set with a resonant inductor. The auxiliary switches are thyristor type, which are triggered by the stack control units (SCU). The main switches are IGCT type switches with antiparallel diodes and they are paralleled with a snubber capacitor to provide resonance during commutation. In each leg there are four IGCT devices, two in the upper side and two in the lower side. The IGCT devices offer the best performances with soft switching and they are integrated with their driver circuitry, therefore they are quite appropriate and useful for this type of an application. The ratings for each of the IGCT's will be around 4500V/4000A therefore the inverter side is capable of blocking 9000V total and standing 4000A input current. The switching frequency for the converter is planned to be 1 kHz which can be modified by the main controller and the SCU. The ratings of the auxiliary switch thyristors will be the same ratings with the IGCT's. However, the ratings of the thyristors can be altered after the analysis of the complete converter according to the peak current and stresses in the auxiliary switches which is actually out of scope of this thesis. A detailed control system diagram of the converter for a single phase leg is given in Figure 4.2.

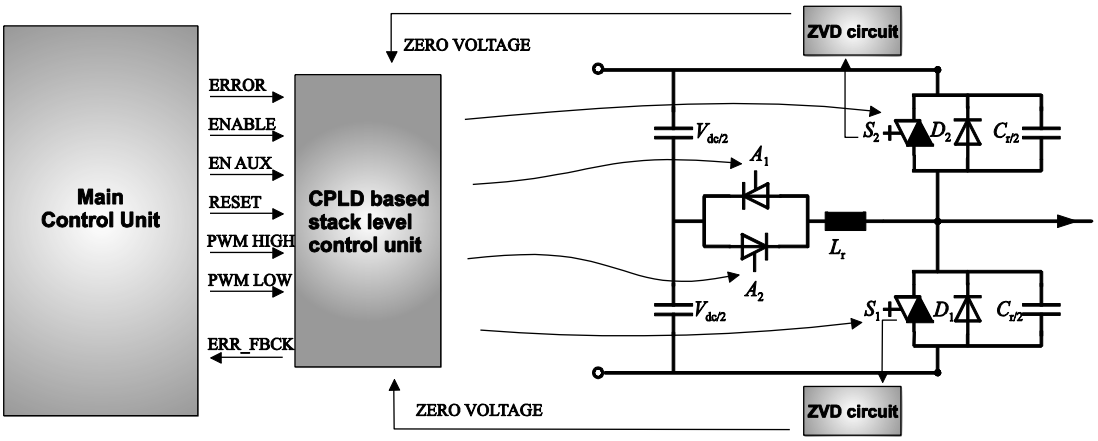


Figure 4.2 : Detailed control system diagram for one leg of the converter.

The control system is supervised by the main control unit. This supervisor unit is responsible for generating pwm signals, enable signals and reset-error handling. Thus, the appropriate PWM tecnique is applied in this unit. The PWM signals is

given to stack control unit in which the control signals of the IGCTs and the auxiliary thyristors are generated. There are eight communication signals between the main unit and the stack control unit to handle the switching signals. SCU evaluates the input commands coming from the main unit and generates gate drive signals for the switches and thyristors. The stack control unit is designed to control one leg of each bridges instead of controlling all three phase converter which will lead to have more flexible system. Therefore in a complete converter there are three SCU for each inverter and rectifier part of the dual active bridge converter. There are also two zero voltage detection circuits which communicates with SCU. When one of the switch voltage becomes zero, these circuits send signals to SCU. Now the software of the SCU and control mechanism will be explained in detail.

4.2 Control Software Design

The communication with the main unit and the generation of the control signals require fast and reliable solutions. Although the main control algorithm will be determined and the start-reset-error functions are controlled by the main controller; the stack controller is directly responsible with the control of the switching signals, therefore it should be design on a reliable and safe manner with compatible and fast operation features. To provide these properties the Complex programmable logic devices (CPLDs) are selected as the control chip. The implementation of CPLDs are ratherly complex when they are compared to microcontrollers or microprocessors, but they offer fast operation with the capability of handling high number of I/O communications and calculations at the same time. The XC95** and XC95**XL series of the Xilinx CPLDs are quite convenient for this type of an application, since they are cheap, reliable and widely used. The software of the CPLD has been prepared by using Xilinx ISE 13.1 design tool in VHDL language.

The state machine designed for the main module is shown in Figure 4.3. In the idle-state the circuit is prepared to generate the output signals. When the enable signal is received, the new state of the module becomes state-operation. When the state-operation begins, the pwm signals for upper and lower switches are automatically started to be generated. In this state, simply a submodule is enabled; namely delaycounter module which runs a delay mechanism to generate the predetermined deadtime. A similiar mechanism is also used for the auxiliary switch signals. If

enable-aux signal which is generated by the main controller is received, SCU starts to output the auxiliary switch signals. The deadtime and boost time of ARCP which is critical for zero switching and safe operation, can be controlled and altered in the main module during the programming stage. During the operation if the enable signal is terminated, the system turns back to idle state. If error signals is received in any state of the module, the system enters to the state-shutdown in which the outputs are cut down immediately. When the system is in the shutdown state the module waits for the error to be cleared and to receive a reset signal to change the state to idle state. The reset signal is asynchronous with the clock therefore the system turns back to idle state as soon as it is received. Please note that, the error signal is defined for the opposite logic (i.e negative logic) to prevent problems in case of a power cut.

As it is stated earlier, the auxiliary signals and pwm signals are generated with similiar modules. The state machine diagrams of this modules are shown in Figures 4.4, 4.5. For the main switch signals the procedure is as follows.

The operation is composed of 5 different state. In the idle-state the module is ready to receive enable. Also in this state a counter has been initialized to count the deadtime. When the enable = 1 is recognized, the module starts to wait for the pwmhigh which denotes the input pwm signal for the upper switch of a phase leg coming from the main controller to become 1, to change the state to off-rise-state. In the off-rise-state the outputs for the switch signals are 0. When the endofdelay signal which is generated by the delaycounter is received, i.e. the deadtime has been passed, the new state becomes high-on-state. The signal for upper switch (pwmouthigh) becomes 1 in this state and the delaycounter reinitilized. With the falling edge recognition, this state ends and off-fall-state begins. The operation of off-fall-state is similiar with the off-rise-state and the end of delay signal starts low-on-state in which the signal for lower switch (pwmoutlow) becomes 1. When the rising edge of the input pwmhigh is recognized, the module turns back to the off-rise-state and the procedure restarts. During the operation if enable = 0 is received, the state of the submodule changes to idle-state. Here, ZV detection signal is optional. This signal can be used instead of endofdelay signal or it can be employed as an auxiliary safety function along with the endofdelay signal.

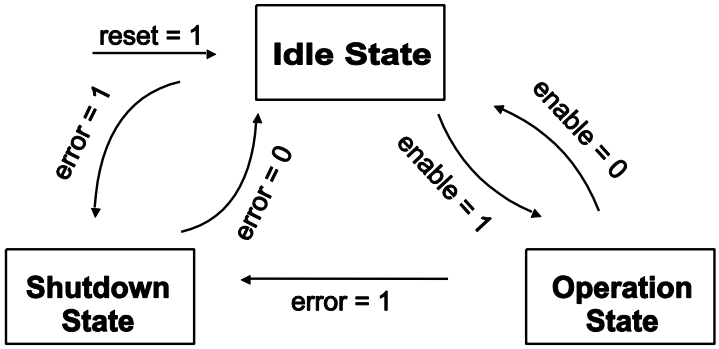


Figure 4.3 : Main module state machine.

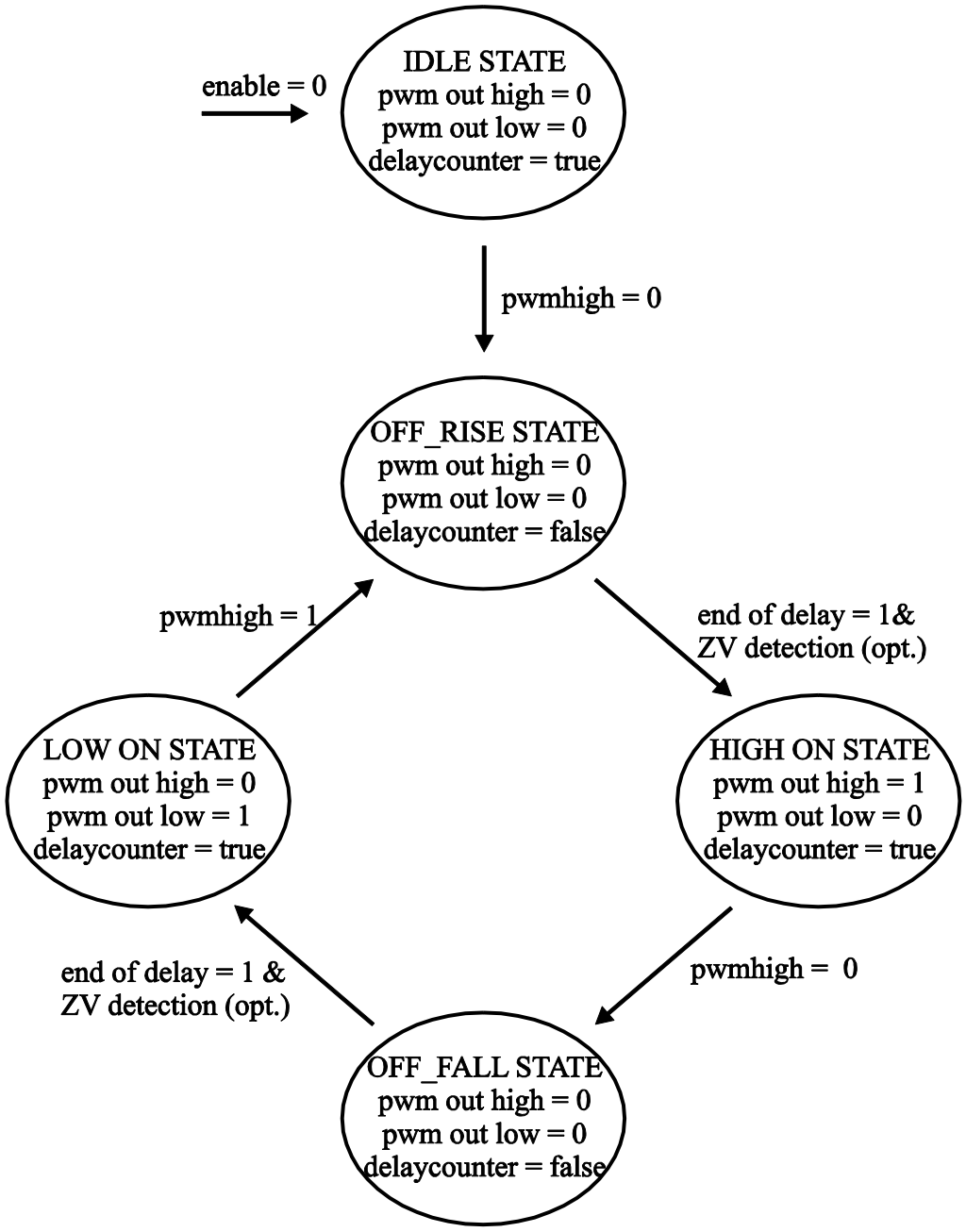


Figure 4.4 : Main switch module state machine.

The state machine of the auxiliary switch module is similiar to the main switch module, but in this module the input pwm signals do not come from the main module, instead the output of the main switch module is the input of the auxiliary switch module to ensure a synchronous operation. Also in here an input flag (y) is defined to prevent generation of an unintended delay-time for auxiliary switch signals at the beginning of the enabling of the module. y signal which is defined as 0 in the idle state becomes 1, after a complete period of the switching.

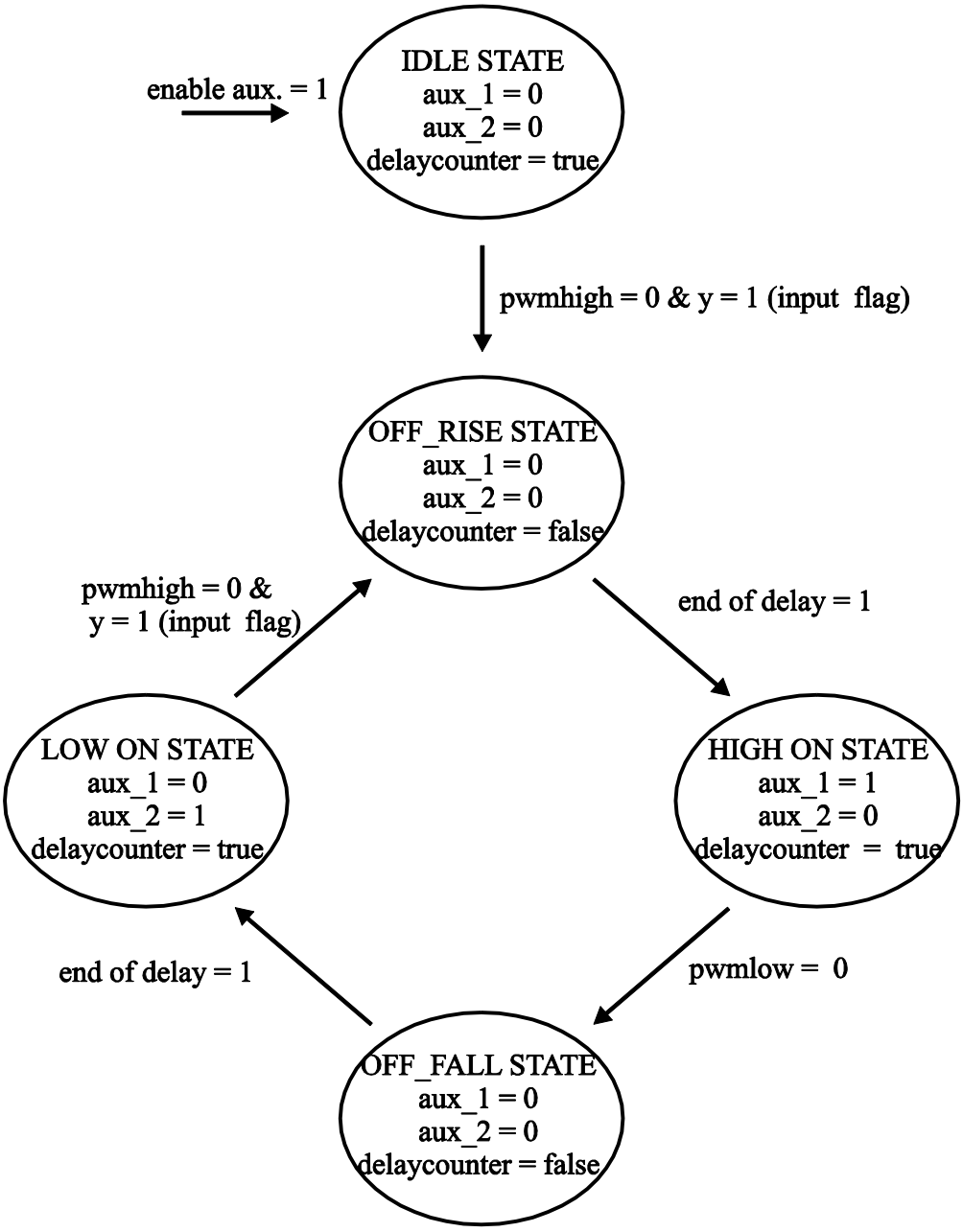


Figure 4.5 : Aux. switch module state machine.

There is also one more important issue worthwhile to explain. In the auxiliary state machine, the turn off of the switching signals are connected to pwmhigh signal, although it can be extended to complete running duration of the auxiliary thyristors to prevent malfunctions during the utilization of the thyristors. With this method the auxiliary switches will never be triggered if the main switches are off.

An example of switching signals are given in Figure 4.6. For this figure, the states of each submodule are denoted with as in table 4.1. The Off-Rise and Off-Fall states correspond to deadtime/boost-time states and the switches are off. In the High-On state the upper switch of the converter leg receives high, and in the Low-On state the bottom switch of the converter leg receives high. The software has been tested and verified in behavioral simulation of Xilinx with a test bench code. The results of the behavioral simulation of the Xilinx ISE 13.1 is given in Figure 4.7. In this figure, it is possible to verify the state transitions which are denoted with the term pr_state according to the input signals. As it is intended, the auxiliary switch signals are not directly employed with the reset command. The signals are activated after one cycle and when *y=1* the auxiliary switches are activated. The results are matched with the purpose.

As it can be concluded from the Figure 4.6 and state machine diagrams, the fixed time control method is chosen as the control method for ARCP. The switch on duration of the auxiliary switches and the deadtime which determined according to the ARCP requirements can be implemented during the programming stage of the devices. Since the board has programming connectors (see Section 4.3), it can be manipulated according to the needs easily. The switching frequency should also be predetermined and implemented in the software during the programming stage. On the other hand, the realized board is flexible and the CPLD XC95144XL is capable of implementing more complex systems. Therefore the software can be altered later on if it is needed. Since the zero voltage switching is critical, to prevent malfunctions in the system a zero voltage detection functionality has been added to the software (Figure 4.4) which can be used along with a zero voltage detection circuit. With this functionality, the switches will not be turned on until the SCU receives a zero voltage recognition signal. This is basically a precaution to protect the switches for the extreme cases which are not predicted earlier. Therefore a zero voltage detection

circuit together with SCU has been designed as a secondary supporting circuit for this thesis. The details about this circuit, its design and test results will be given in section 4.3.

Table 4.1 : States in Figure 4.6.

Name	Mod.	State
A1	Main SW Mod.	Off-Rise
A2	Main SW Mod.	High on
A3	Main SW Mod.	Off-Fall
A4	Main SW Mod.	Low On
B1	Aux. SW Mod.	Off-Rise
B2	Aux. SW Mod.	High on
B3	Aux. SW Mod.	Off-Fall
B4	Aux. SW Mod.	Low On

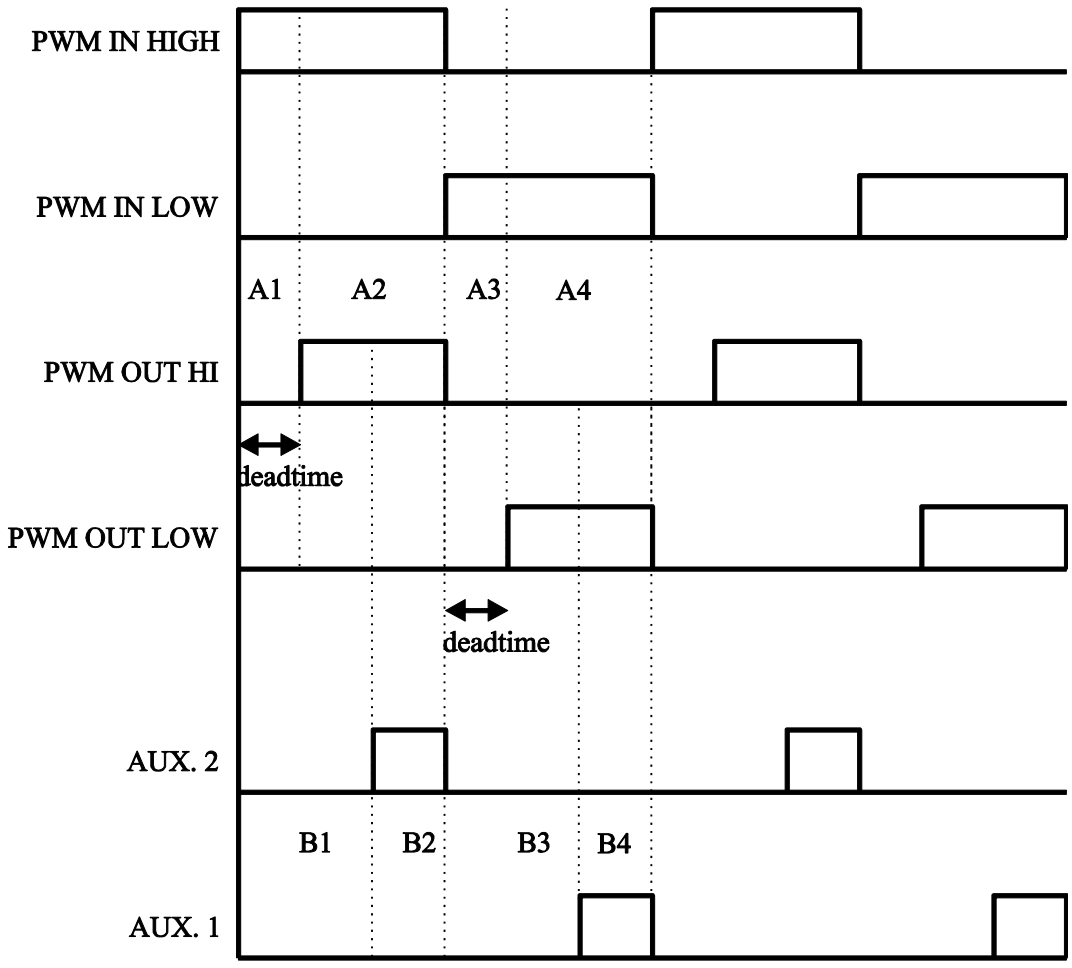


Figure 4.6 : Switching Scheme Proposed in the software.

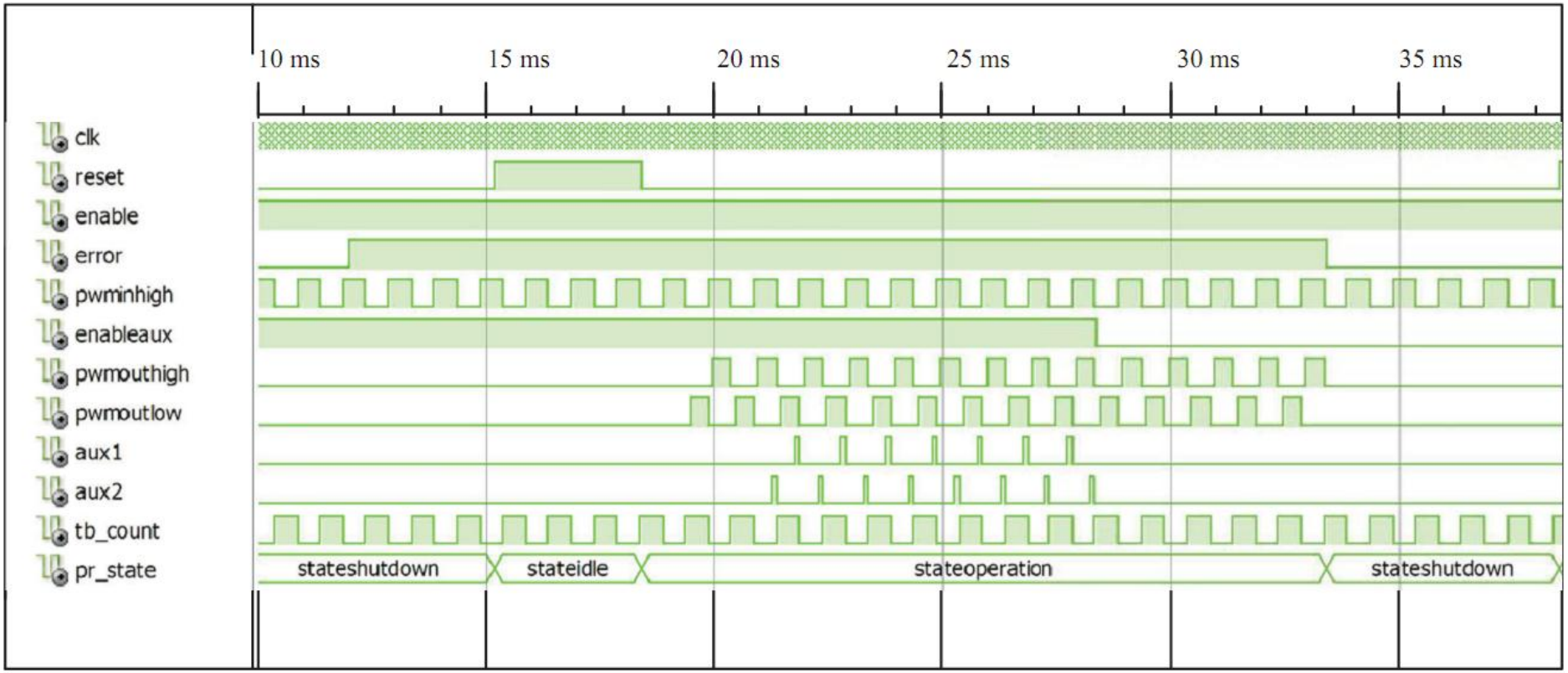


Figure 4.7 : State machine and switching scheme in behavioral simulation.

4.3 Stack Control Unit and Zero Voltage Detection Circuit Realization

4.3.1 Stack control unit

The realized control unit for single phase leg has shown in Figure 4.8. The circuit is designed on a 89.5 mm x 96.5 mm PCB. At the middle of the PCB, the control chip Xilinx XC95144XL-10TQ100 CPLD has been placed which is accompanied by a 10 MHz oscillator nearby. The CPLD has 144 macrocells and 100 I/O pins which are proper for our application. In this converter a realiable communication is very important. Therefore to ensure a secure communication on the left and right side of the PCB the fiberoptic communication elements are lined up. ABB 5SHY 35L4510 [26] is the expected to be used as the main switch semiconductors in the dual active bridge converter, therefore Avago Technologies HFBR-1521Z transmitters and HFBR-2528 receivers are selected as the fiberoptic link components which are compatible with the target IGCT device communication for full performance. The functionality of the communication elements on the board is tabulated in table 4.2.

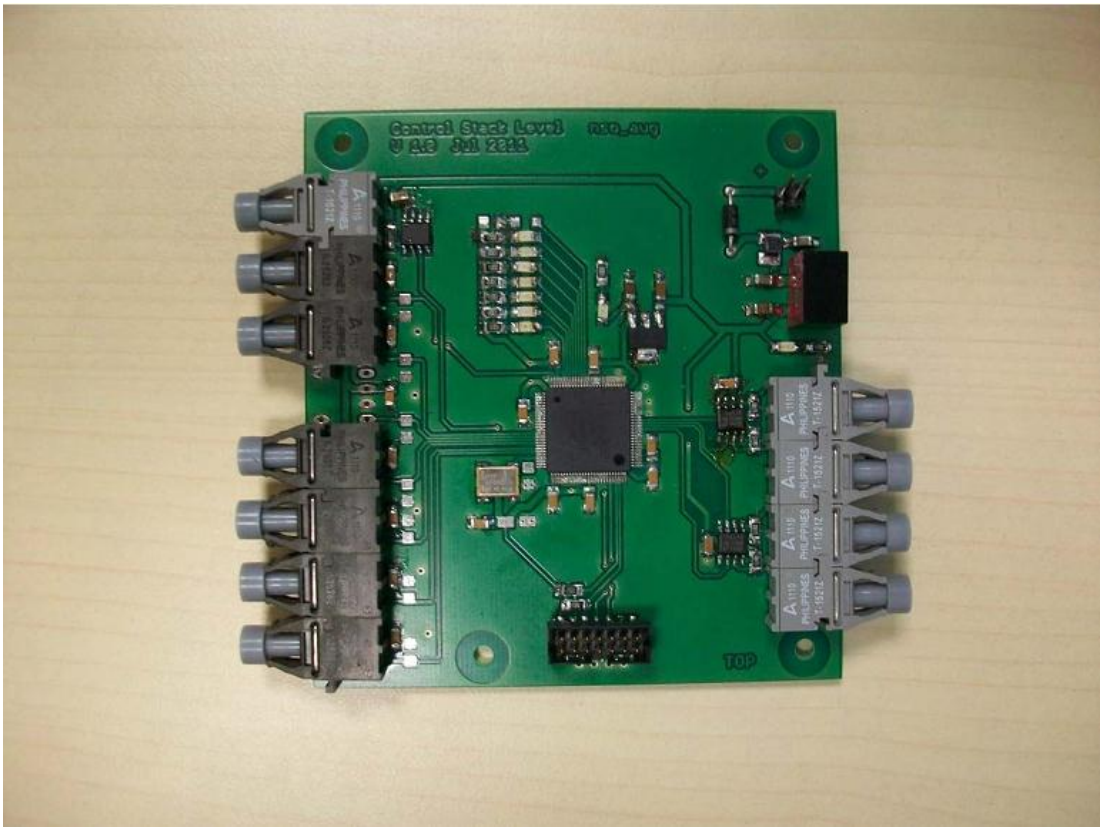


Figure 4.8 : Stack control unit.

Table 4.2 : Communication Elements.

Name	Communication Partner	Function
ERR-R	Main Unit	Error input
Res	Main Unit	Reset input
ZVS	ZVD Circuit	zero voltage recognition input
HI	Main Unit	input PWM for upper switch
LOW	Main Unit	input PWM for lower switch
AUX	Main Unit	auxiliary switches enable input
ENA	Main Unit	operation enable input
ERR-T	Main Unit	error received signal
ALO	Aux Thyristor 1	auxiliary switch control signal
AHI	Aux Thyristor 2	auxiliary switch control signal
LOW	Lower IGCT	IGCT control signal
HIGH	Upper IGCT	IGCT control signal

To protect the CPLD and to provide the necessary power to the transmitters, SN75451B peripheral drivers are added to the board which are placed next to the transmitters. The power input of the SCU is 24V, therefore a tracopower TSR-1 2450 converter is used to provide 24V/5V DC-DC conversion. The communication elements are powered up with this 5V. The XC95144XL is a 3.3V CPLD, therefore a LM3940 3.3V LDO regulator is placed to the board. The CPLD is programmed with JTAG programmer Platform Cable USB II of the Xilinx, thus a compatible connector molex 87832-1421 is attached on the bottom of the board.

Since the converter and the main unit has not been prepared yet, and it is not possible to provide external signals from a signal generator to the fiberoptic communication receivers, the board has not been tested when it is fully functioning. However, it has been observed with the help of the leds placed on the PCB that the board reacts well to the input commands and main state machine works well when inputs are provided. The software has been tested in Xilinx ISE 13.1 behavioral simulation. Besides to verify the software in a real system, another board with a same series CPLD (XC9572) as in the SCU and with standard connectors is used. To provide pwm input TTI TG2000 function generator is employed. The test conditions are tabulated in table 4.3. Please note that although it is not needed, an input port has been spaced for pwm signal of the lower switch. This can be utilized for the different type control methods such as dual phase shift control if it is needed, or it can be used for a different purpose.

Table 4.3 : Test Conditions for ARCP-DAB Stack Control Unit.

frequency	1kHz
duty cycle	50%
deadtime	100µsec.
boost-time	100µsec.

The resulting switching scheme is given in Figures 4.9, 4.10, 4.11. The test results shows that the switching signals are generated as it is determined when enable signal is received. Here the deadtime and boost-time are both chosen as 0.1 ms. The switch on time for each switch is 0.4 ms. In Figure 4.12, 4.13 the respond to the error input is shown. When the error signal is received, the state becomes error state and all the signals are shutdown immediately. The respond time to the error input is around 400 ns which is much better than it is needed for this application.

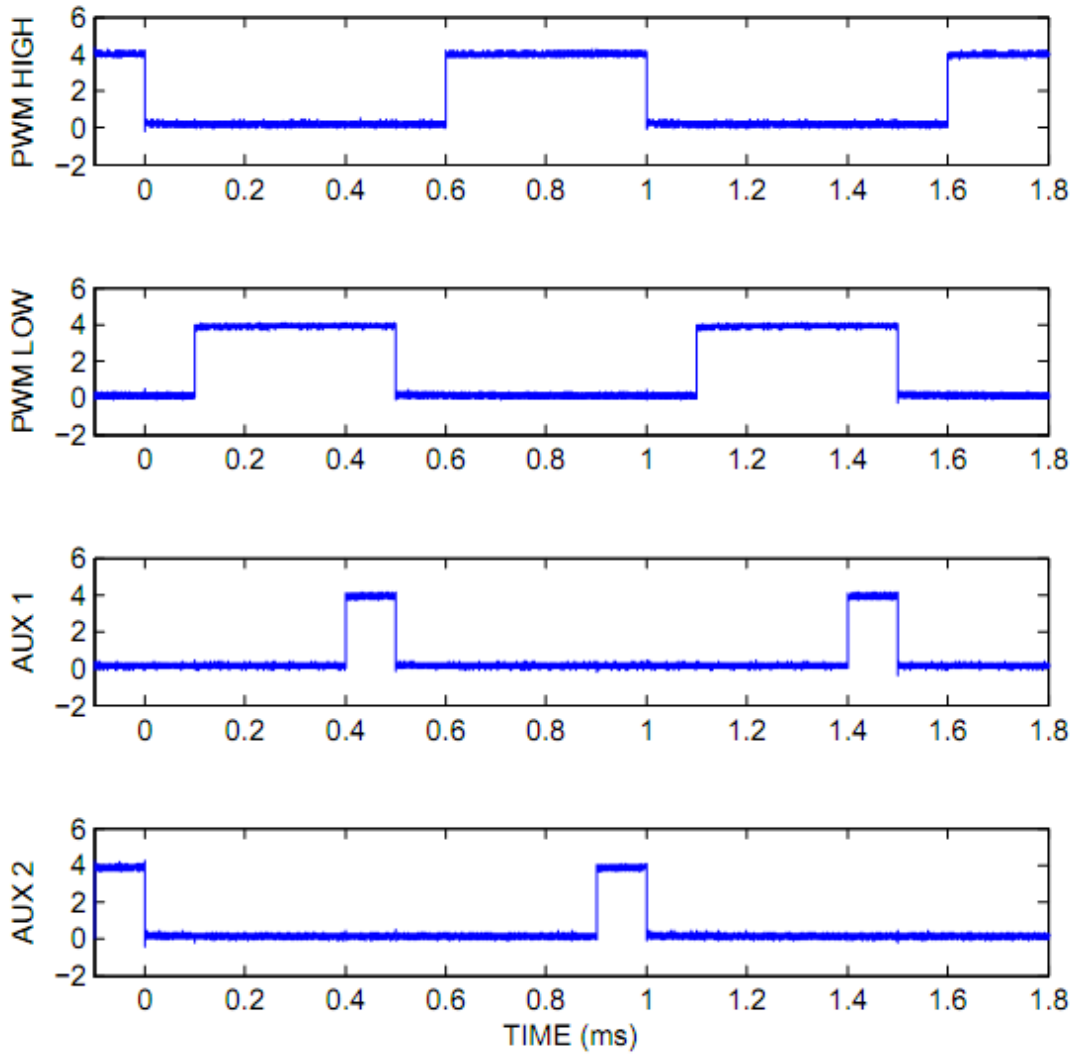


Figure 4.9 : Test results of the software (waveforms).

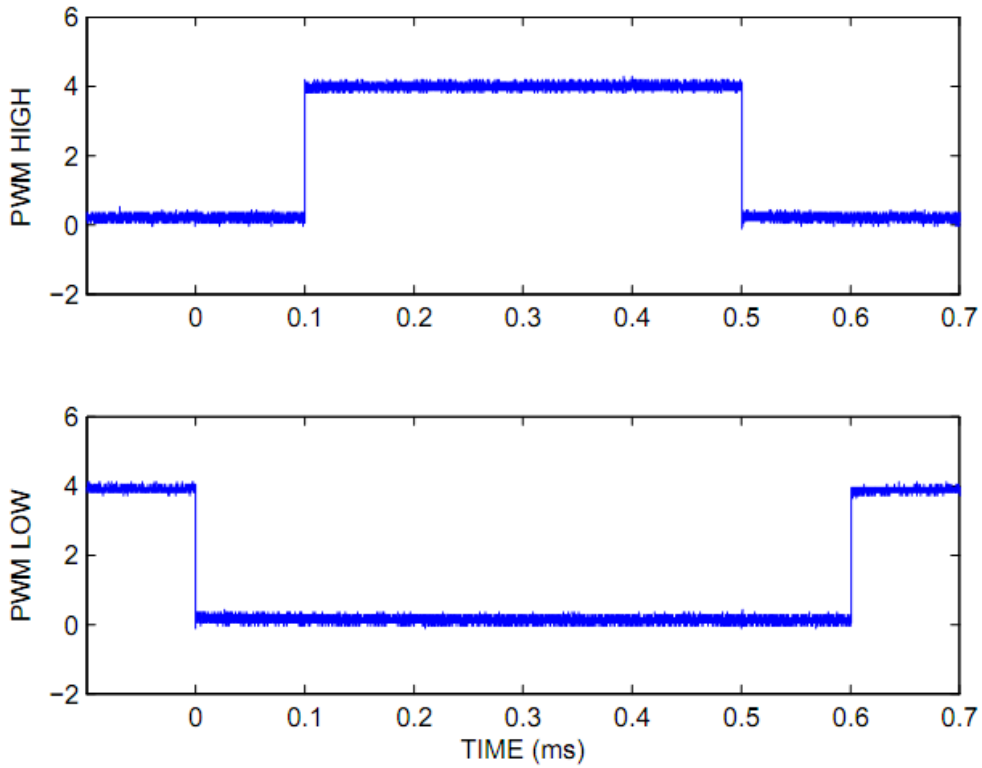


Figure 4.10 : Test results of the software (main switch signals).

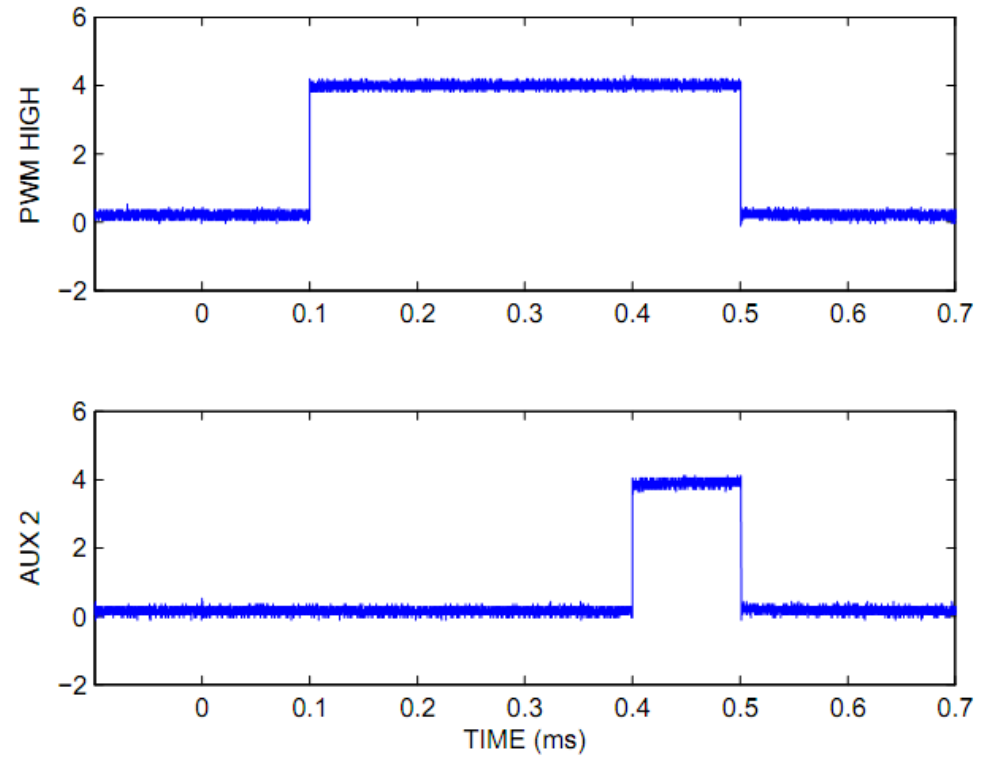


Figure 4.11 : Test results of the software (auxiliary switch signal for lower switch).

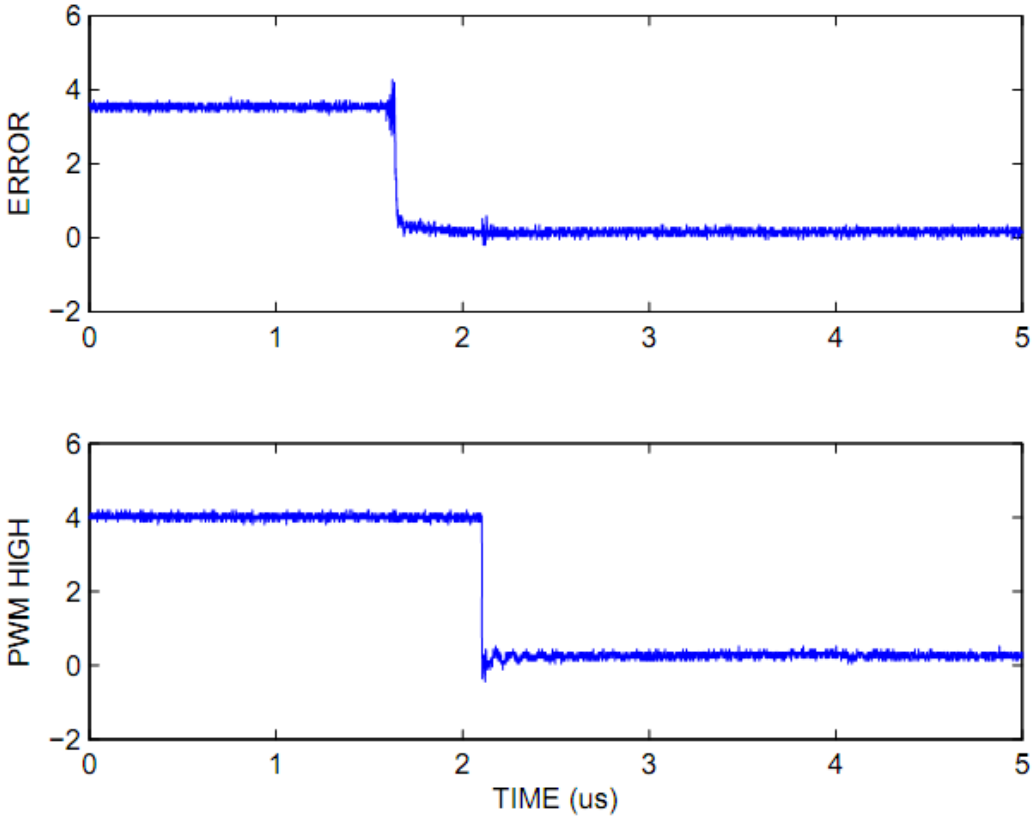


Figure 4.12 : Test results of the software (error recognition a) .

According to the first projection of the thesis; the input pwm is a square wave in 1kHz, in other words single phase shift is selected as the control method of the DAB. However the SCU is available for the implementation of different control methods, which brings flexibility to the system. The phase shift between the full bridges can be controlled without any restriction. The board controls only one phase leg, therefore it is also possible to implement a phase shift between the legs, which makes also possible to use dual phase shift control in the DAB. The inputs of the board offers a very reliable communication and they can drive the related IGCT directly. Another important feature of the prepared board is that the state machines and software can be altered easily. Also the use of CPLD makes it possible to protect the system in a fast manner in case of a failure of the system. In the device, the %60 of the macrocells has been used, however optimization of the counter algorithm could provide a better cell usage. Similiarly, optimization of the input-output ports can lead a better reaction performance. But these issues are not considered during the design since the performance of the device is already good enough for this type of a system.

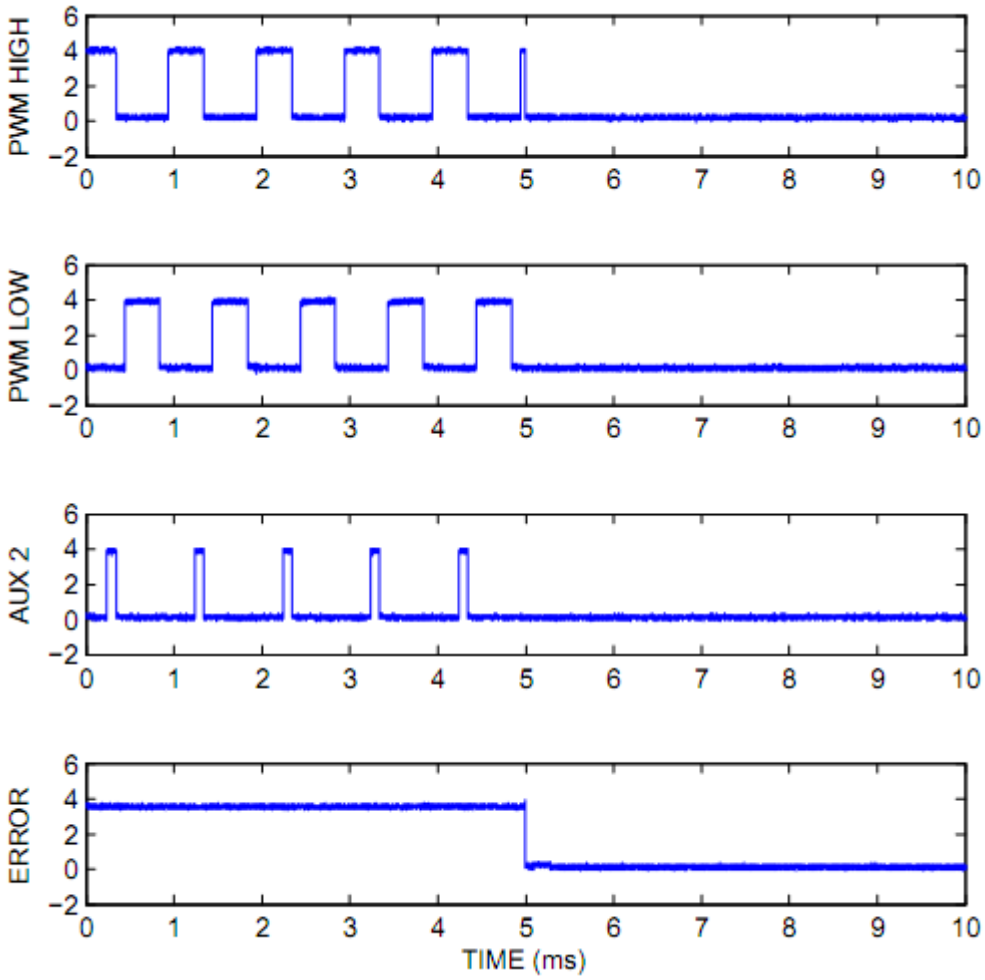


Figure 4.13 : Test results of the software (error recognition b) .

Please note that, the figures are drawn with *Matlab 2010b,* according to the data captured from the oscilloscope *Tektronix, TDS3000C.*

4.3.2 Zero voltage detection circuit

In normal conditions, with the related calculations of the operating conditions, the deadtime should be long enough to transfer the voltage on the semiconductors to transfer rail to rail. However to increase the reliability of the system a zero detection circuit is proposed which will cooperate with SCU and prevent the switching before the voltage on the corresponding switch reaches to zero.

Since the voltage will be high on the switches, monitoring and handling the noisy input and providing high resolution are difficult by applying standard voltage dividers with operating amplifiers. For a similiar application in [27, 28] a zero voltage detection has been proposed and applied by using a diode with a high voltage

blocking capability. In these circuitries a 300V power supply has been used to make sure that the diode becomes conducting before the switching level reached. In [29] a similiar method has been used to monitor the voltage on the semiconductor to provide short circuit protection with an additional diode which eliminates the effect of the high voltage blocking diode voltage drop which is highly depended on the environmental conditions.

In this thesis, since an accurate monitoring is not necessary, the circuit proposed in [27, 28] is adopted. Since the monitored voltage on the semiconductor will be very noisy, a typical schmitt trigger circuit is applied with a fast operating amplifier. This method also reduces the need for a high voltage power supply. The complete proposed circuit is in Figure 4.14.

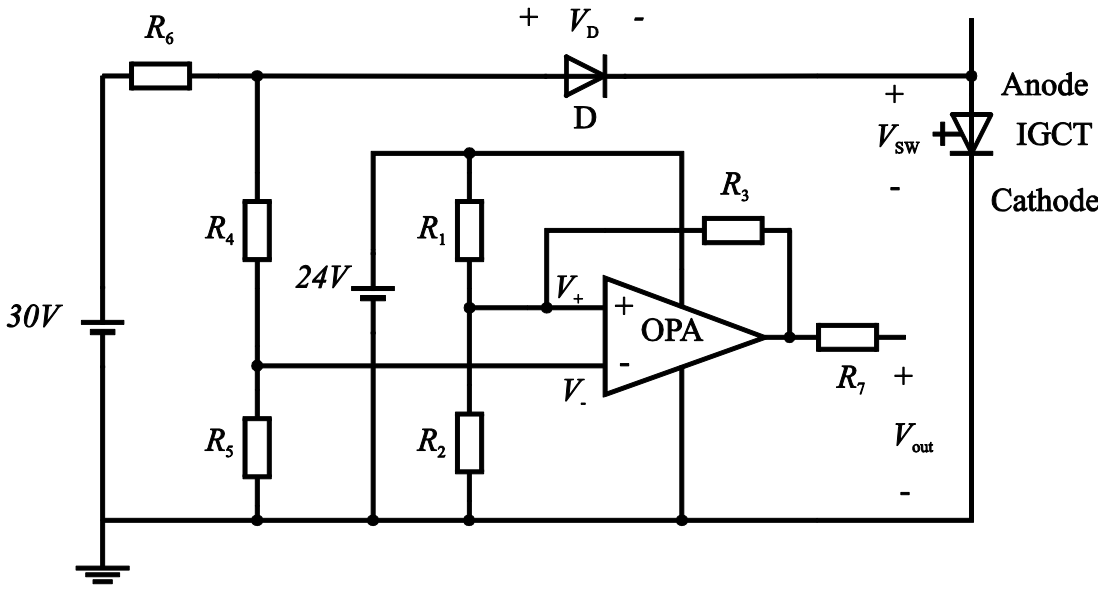
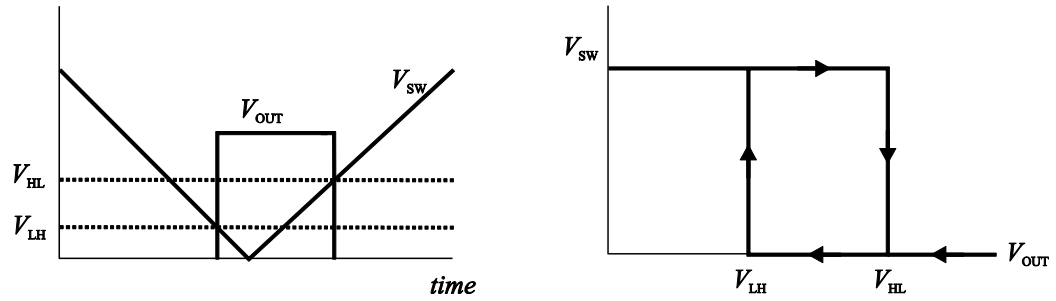


Figure 4.14 : Zero voltage detection with hysteresis.



a) V_{OUT} and V_{SW} b) V_{OUT} vs V_{SW}

Figure 4.15 : Zero voltage detection circuit input output relation.

The idea in the method is simple. Unless the diode is not forward biased, the voltage of the switch is blocked and not monitored. V_- is determined by the voltage division of 30V supply therefore the op amp is protected from high voltages. When the switch voltage decreases below $30V - V_D$, where V_D denotes the voltage drop on diode when it is forward biased, the diode becomes conducting and the voltage $V_{R5} + V_{R4}$ becomes equal to $V_{SW} + V_D$. The peripheral of the op-amp is arranged for non-symmetrical schmitt trigger with single power supply. This will remove the need for negative power supply and the output voltage will either zero or 24V.

$$V_- = \frac{(V_D + V_{SW})R_5}{R_4 + R_5} \tag{4.1}$$

$$\frac{V_+ - 24}{R_1} + \frac{V_+}{R_2} + \frac{V_+ - V_{OUT}}{R_3} = 0 \tag{4.2}$$

for $V_+ > V_- \rightarrow V_{OUT} = 24V$ then

$$V_{LH} = \frac{(R_2R_3(R_4 + R_5)) \times 24V + (R_1R_2(R_4 + R_5)) \times 24V}{R_5(R_1R_2 + R_2R_3 + R_1R_3)} - V_D \tag{4.3}$$

and for $V_- > V_+ \rightarrow V_{OUT} = 0V$ then

$$V_{HL} = \frac{(R_2R_3(R_4 + R_5)) \times 24V}{R_5(R_1R_2 + R_2R_3 + R_1R_3)} - V_D \tag{4.3}$$

where V_{LH} and V_{HL} are low to high and high to low voltage thresholds for the output of the op amp respectively. The margin between V_{LH} and V_{HL} can be arranged with the resistances R_1, R_2, R_3, R_4 and R_5. Please note that in the equations the op-amp is assumed to be ideal. In Figure 4.15 an example of waveforms for V_{OUT} and V_{SW} are shown.

The realized circuit is given in Figure 4.16. The input of the PCB is 30V and a 78M24 LDO has been used to provide 24V for opamp. The op-amp is selected as TI THS-3092-D, high voltage low distortion amplifier with high slew rate. The high voltage blocking diode is chosen as NTE517, 15kV/500 mA diode. The voltage drop of the diode is 14V when it carries the maximum current, which is enough to provide

a satisfactory voltage margin in the schmitt trigger. The peripheral resistances can be arranged according to the needs which brings flexibility for monitoring. For output a HFBR-1521Z transmitter is put as in the SCU. The current of the transmitter is arranged to 60 mA with R_7 resistor. The dimension of the PCB is 3,5cm x 7cm, which is quite small. The distance between input of the PCB and ground layer is 25mm, which provides a safely operating condition up to 4.5kV according to the IPC standards for coated boards. The vias which are placed for screw connections provides electrical and mechanical connections. In this manner, it has been aimed to provide connection to the metalic shield and the zero voltage input provided via a coaxial cable from the IGCT.

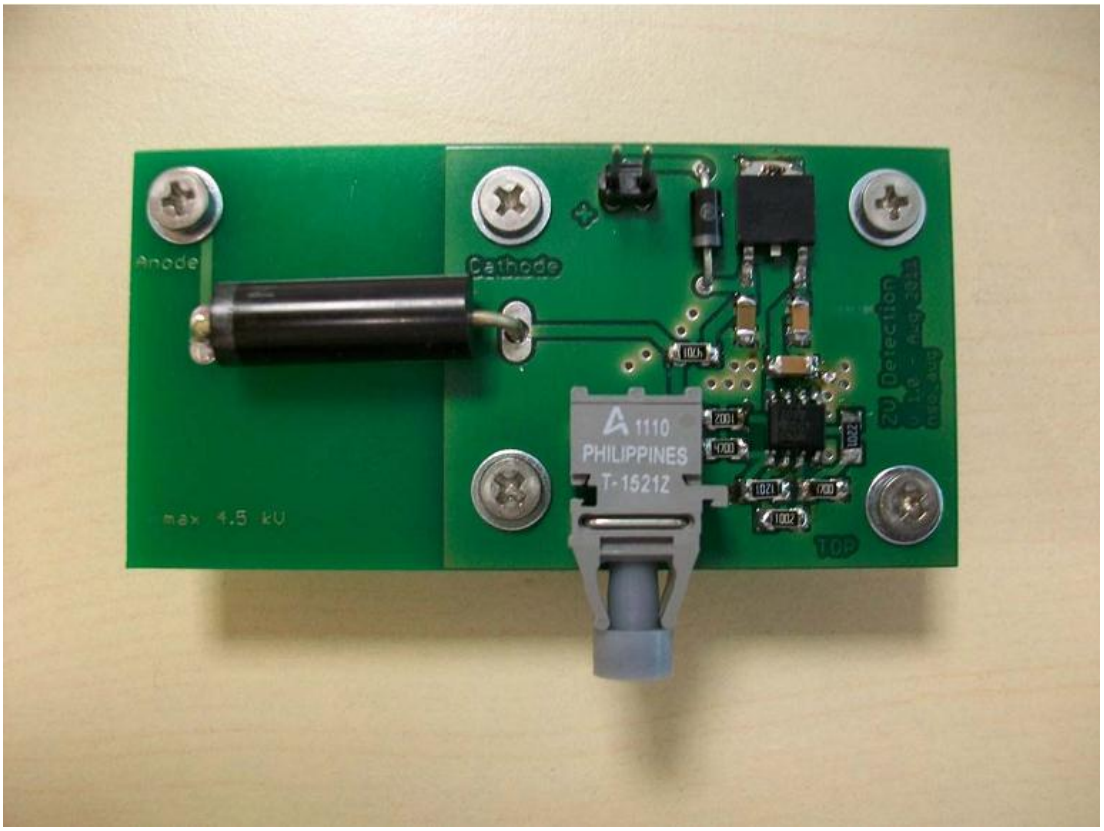


Figure 4.16 : Realized ZVD circuit.

The ZVD circuit has been tested with the conditions given in table 4.4. The test results are given in Figure 4.17 and 4.18. As an input a 40V AC voltage has been applied. The detection limits are defined as 7 volts for low to high transition and 12 volts for the high to low transition. In other words, the input noise up to 12 volts is permittable in this arrangement. Of course it is possible to change this lower or

higher thresholds with different resistances. The test results are consistent with the calculation. During the application, the circuit is expected to work up to 4kV safely.

Table 4.4 : Test Conditions for zero voltage detection circuit.

Input voltage	40 V_{AC}
R1	2.2kΩ
R2	470Ω
R3	1kΩ
R4	10kΩ
R5	10kΩ
R6	4.7kΩ

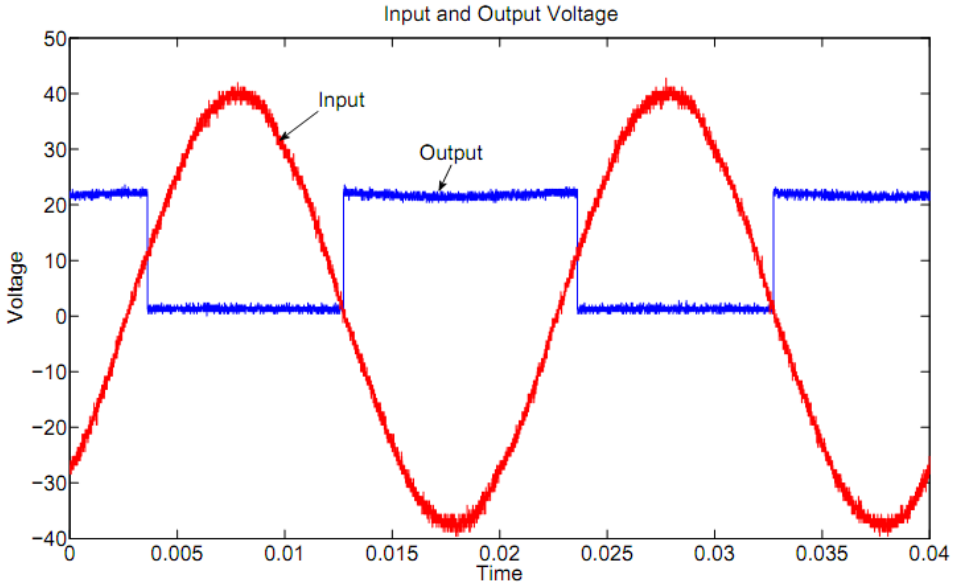


Figure 4.17 : Test results of the ZVD circuit, input-output waveforms.

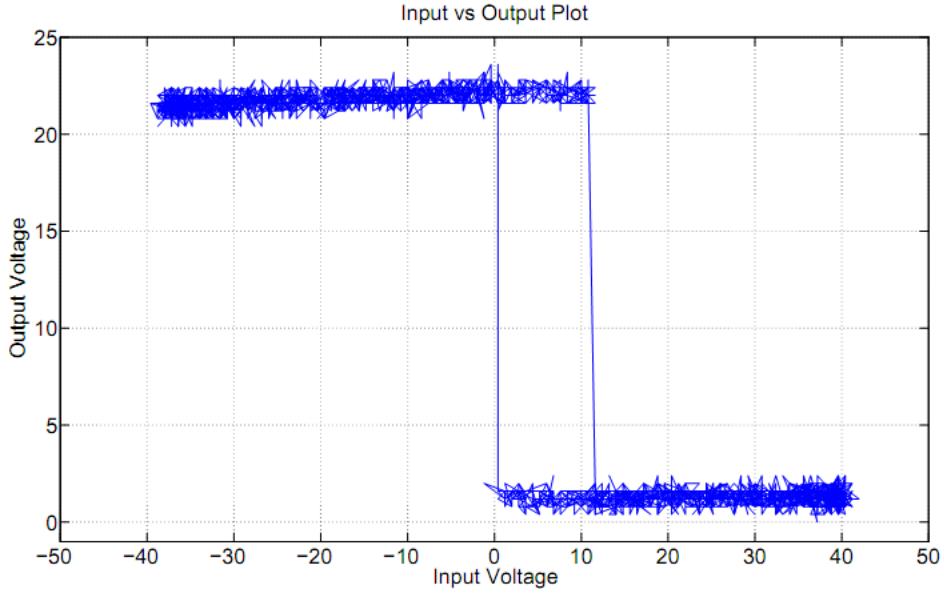


Figure 4.18 : Test results of the ZVD circuit, input vs output.

5. CONCLUSION AND FUTURE WORK

In this thesis, it has been aimed to design a sublevel controller which combines the dual active bridge, the candidate topology for the multimegawatt converter with auxiliary resonant commutated pole, the candidate soft switching technique. With this controller, it has been expected to extend the soft switching operation area to a full operation range by the help of auxiliary switch circuitries. Therefore in the first chapter of this thesis, the motivation of the thesis is explained in detail.

The thesis begins with the details of the motivation and continues with the muti-megawatt converter concept in the second chapter. In this chapter, the dual active bridge topology and control methods are examined. The integrated gate commutated thyristors which are the candidate semiconductor switches of the converter are presented and the reasons of the selection are given. The knowledge gained in this chapter is used to determine the controller specification during the design process.

In chapter 3, the auxiliary resonant commutated pole converter has been examined for a single leg in details. First the topology and the operation is explained. Then the control methods and issues concerning the control methods are pointed out. At the end of this chapter, the simulation of the converter has been made and analyzed. The theoretical analysis of ARCP leg will be useful during the experimental converter design to decide the circuit parameters.

The design procedure is presented in the fourth chapter. At the beginning of this chapter, the determined specifications of the controller are given and the software is explained. Then, the details of the board and test results of the controller are given. At the end of the chapter, the zero voltage detection circuit is introduced, details of the design and test results are given.

During the studies in this thesis, the most challenging part was the examination of the ARCP converter and DAB topology, and preparing a concept to combine them together. The software programming required a deeper knowledge up to some level,

therefore the VHDL language and programming tricks were examined. Besides, to prepare the real circuit the PCB design software Cadsoft Eagle 5.9 were studied and the issues related with the high frequency signal level design were covered. Moreover, the IGCTs and the prospected IGCT device were examined. To complete the controller, the zero voltage detection methods were studied, several methods were discussed and and a proper solution has been offered and designed. In this perspective, the total workdone is way way beyond the ones described this thesis.

The control unit is prepared by considering the simplicity and exibility principles. Since the main switches and auxiliary switches are controlled by different state modules in the software, the hardware can also be utilized without ARCP only as an interface between the power stack and the main controller.

Actually, related with this thesis study, a DAB converter with auxiliary swithes in the inverter side has been simulated by using Ansoft Simplorer 7.0. The results showed that the auxiliary switches can provide soft switching in light load case where the soft switching is not ensured in the standard control method. However, the analysis has not been completed yet and further investigations is required for both theoretical and practical issues. Besides, the exact project parameters are needed to make a proper simulation. Therefore, although the results are promising, the simulation is left outside of this thesis as a further work subject along with the complete analysis of the ARCP DAB converter.

On the other hand, definitely the application of the controller board to the realized converter or a prototype converter and a comparison of performances with and without ARCP is the most important future work subject. This rearch effort will provide information about the pros and cons of the method in practice. Moreover, further improvements can be performed to the controller hardware. By doing this, different control methods can be implemented for ARCP and DAB converter and their effects can be examined experimentally.

In conclusion, with the addition of the experimental research, this study is expected to be a good contribution to the research studies in the high power/high voltage converter design for the offshore windparks field.

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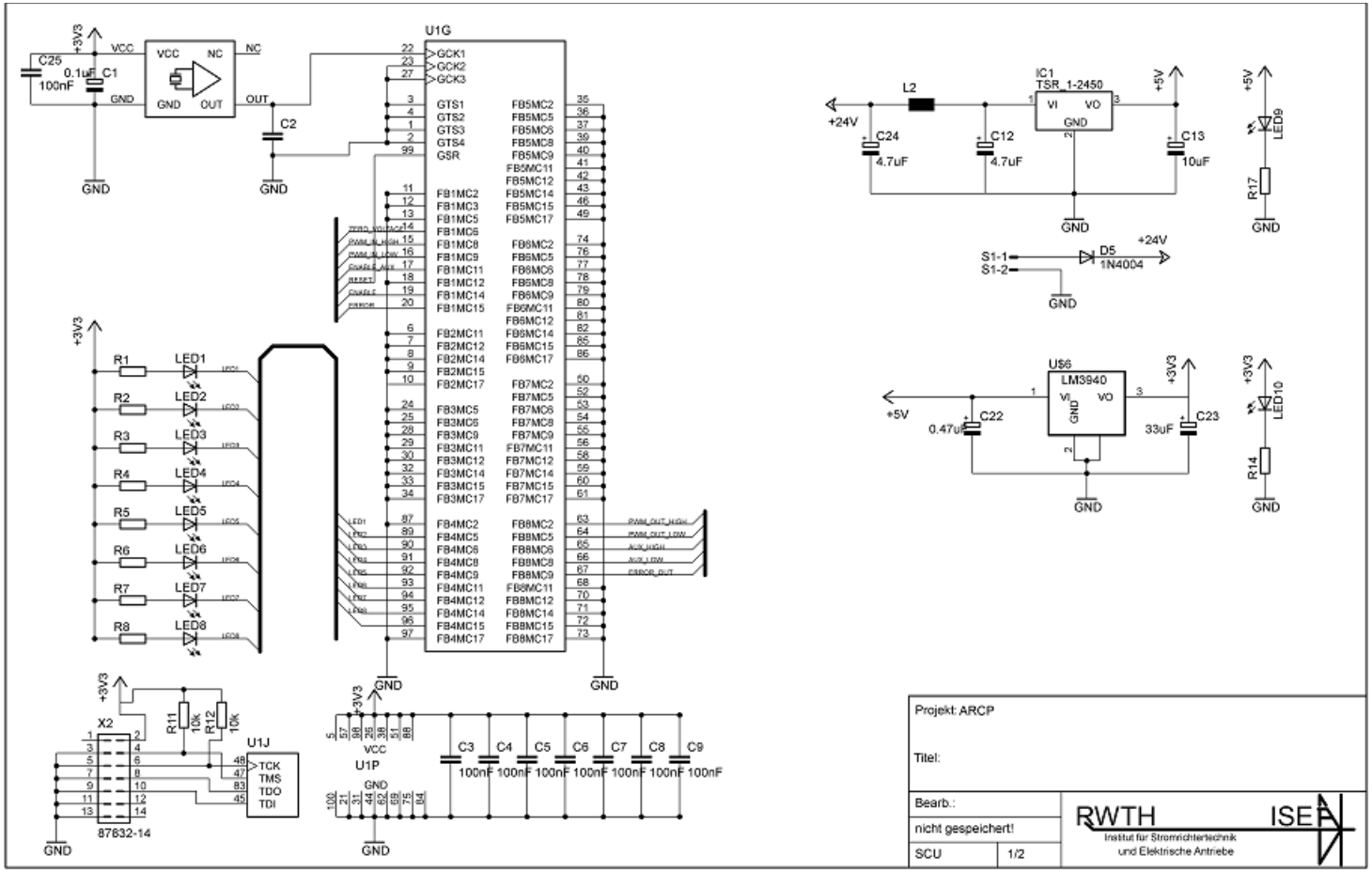
APPENDICES

APPENDIX A.1 : Stack Control Unit Circuit Diagram

Table A.1 : Circuit elements of stack control unit.

Component name	Description
744045008	Wurth Elektronik SMD HF-CHOKE WE-LQ
TSR 1-2450	Tracopower DC/DC Converter,24V/5V,1A
LM-3940	National Semiconductor LDO 3.3V Regulator
XC95144XL-10TQG100C.	Xilinx 9500XL Series CPLD
LF SPXO018036 CFPS-73	IQD Frequency Products Oscillator
87832-1421	Molex Header 2mm Milli-Grid Shrouded Vertical
HFBR-2528Z	Avago Techonologies Fiber Optic Receiver
SN75451BD	TI Peripheral Driver
HFBR-1521Z	Avago Techonologies Fiber Optic Transmitter
HSME-C150	Avago Technologies Led Green
1N4004	Fairchild Diode 1A

APPENDIX A.1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C25
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100nF
C1
VCC
NC
GND
OUT
C2
GCK1
GCK2
GCK3
GTS1
GTS2
GTS3
GTS4
GSR
L2
+24V
IC1
TSR_1-2450
VI
VO
C24
4.7uF
C12
4.7uF
C13
10uF
+5V
LED9
R17
S1-1
S1-2
D5
1N4004
U$6
LM3940
C22
0.47uF
C23
33uF
LED10
R14
R1
R2
R3
R4
R5
R6
R7
R8
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
X2
87832-14
R11
R12
10k
U1J
TCK
TMS
TDO
TDI
U1P
C3
C4
C5
C6
C7
C8
C9
100nF
Projekt: ARCP
Titel:
Bearb.:
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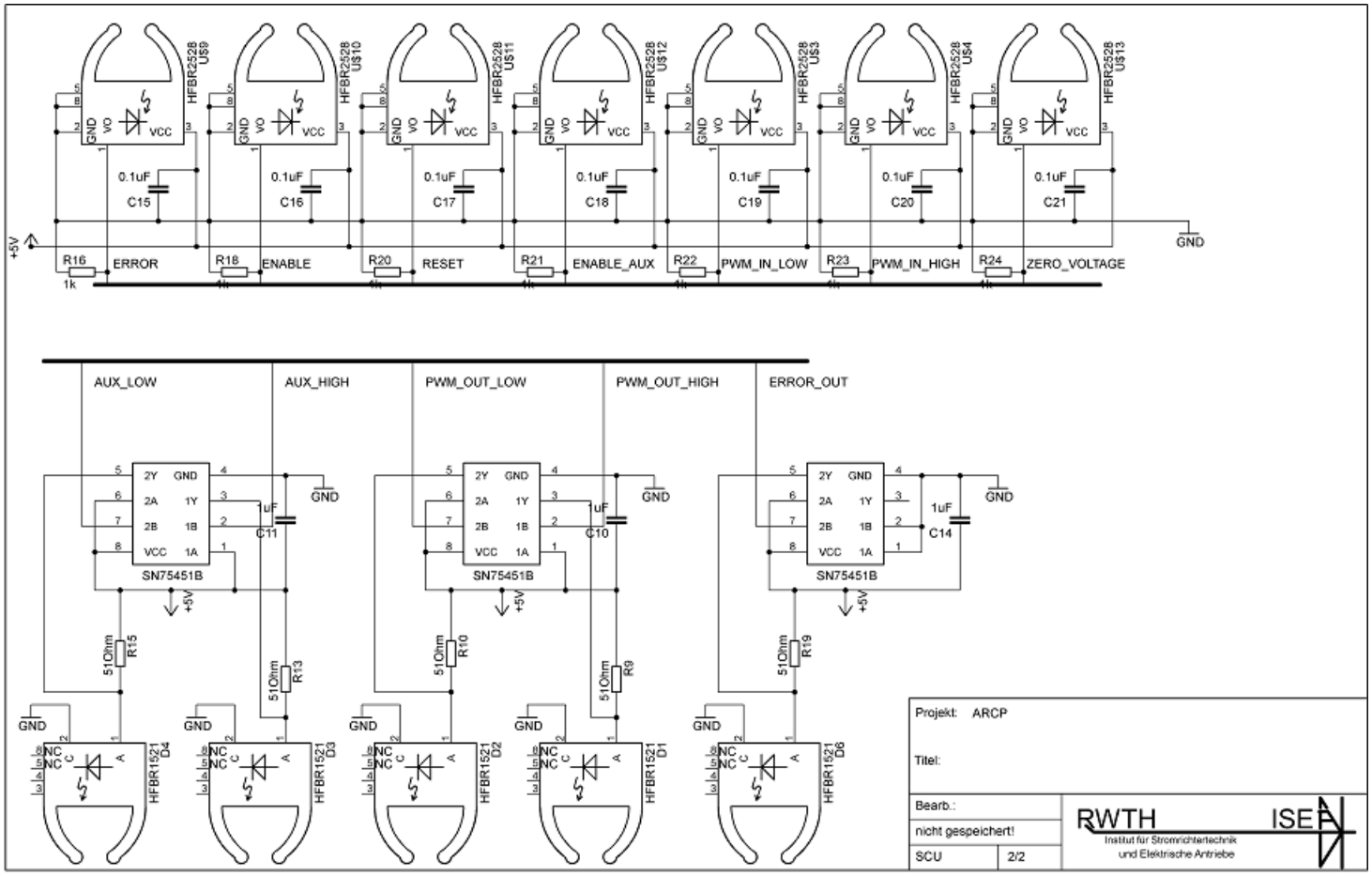
SCU
1/2
RWTH
ISEA
Institut für Stromrichtertechnik
und Elektrische Antriebe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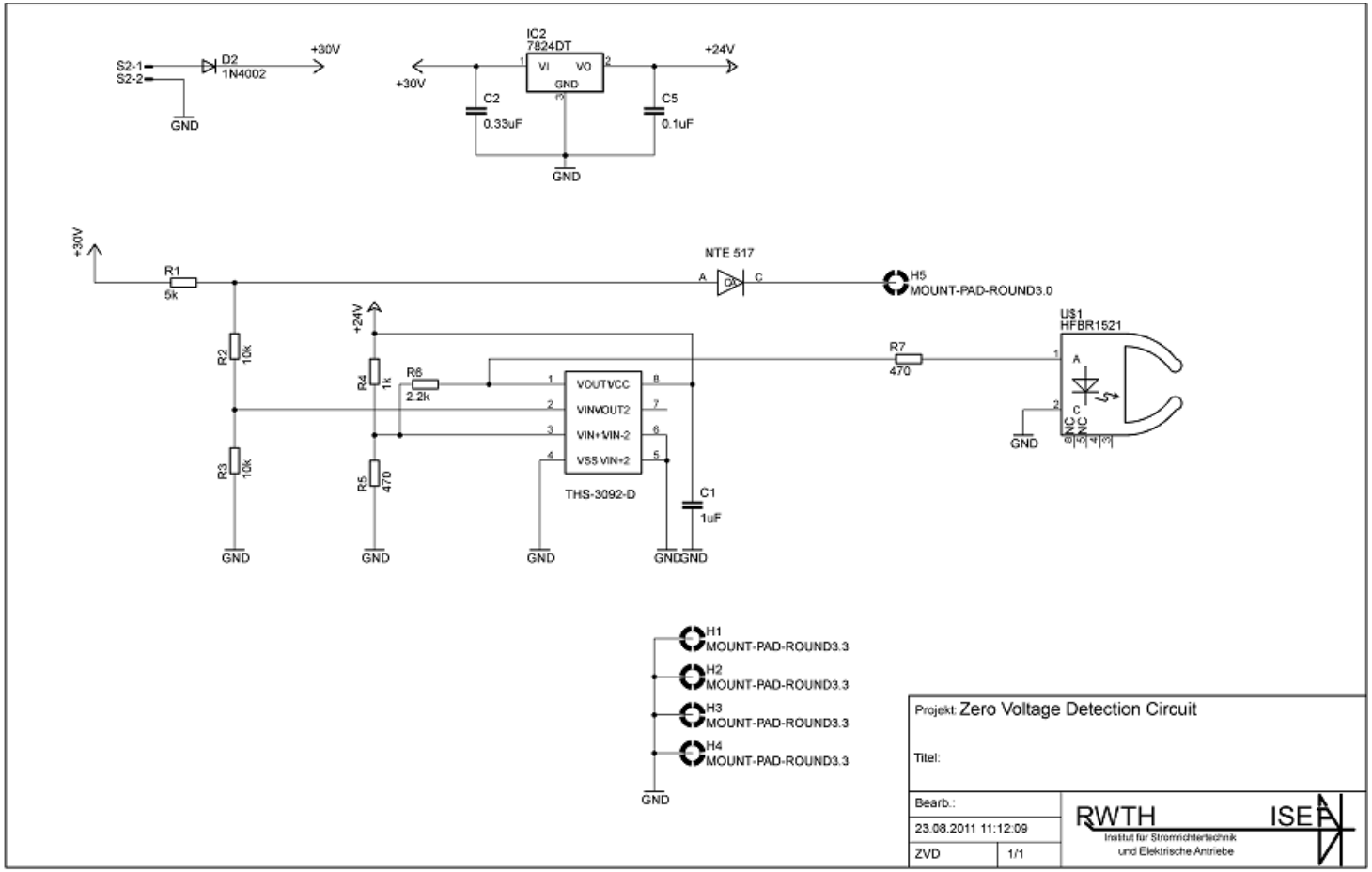
HFBR2528 U$10
HFBR2528 U$11
HFBR2528 U$12
HFBR2528 U$3
HFBR2528 U$4
HFBR2528 U$13
GND VO VCC
0.1uF C15
0.1uF C16
0.1uF C17
0.1uF C18
0.1uF C19
0.1uF C20
0.1uF C21
+5V
GND
R16 1k ERROR
R18 ENABLE
R20 RESET
R21 ENABLE_AUX
R22 PWM_IN_LOW
R23 PWM_IN_HIGH
R24 ZERO_VOLTAGE
AUX_LOW
AUX_HIGH
PWM_OUT_LOW
PWM_OUT_HIGH
ERROR_OUT
2Y GND 1Y 2A 1B 2B VCC 1A
SN75451B
1uF C11
1uF C10
1uF C14
51Ohm R15
51Ohm R13
51Ohm R10
51Ohm R9
51Ohm R19
NC A C NC
HFBR1521 D4
HFBR1521 D3
HFBR1521 D2
HFBR1521 D1
HFBR1521 D6
Projekt: ARCP
Titel:
Bearb.:
nicht gespeichert!
SCU 2/2
RWTH ISEA
Institut für Stromrichtertechnik und Elektrische Antriebe

APPENDIX A.2 : Zero Voltage Detection Circuit Diagram

Table A.2 : Circuit elements of zero voltage detection circuit.

Component name	Description
1N4002	ON Semi Diode 100V/1A
HFBR-1521Z	Avago Techonologies Fiber Optic Transmitter
NTE-517	NTE Electronics 15kV/550mA Diode
THS-3092-D	TI Dual Op Amp 5700V/s
TS78M24CP	TAIWAN SEMICONDUCTOR 24V LDO Regulator 0.5 A

APPENDIX A.2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C5
0.1uF
R1
5k
NTE 517
H5
MOUNT-PAD-ROUND3.0
U$1
HFBR1521
R2
10k
R3
10k
R4
1k
R5
470
R6
2.2k
R7
470
VOUTVCC
VINVOUT2
VIN+VIN-2
VSS VIN+2
THS-3092-D
C1
1uF
H1
MOUNT-PAD-ROUND3.3
H2
MOUNT-PAD-ROUND3.3
H3
MOUNT-PAD-ROUND3.3
H4
MOUNT-PAD-ROUND3.3
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Titel:
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23.08.2011 11:12:09
ZVD
1/1
RWTH ISEA
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und Elektrische Antriebe

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