ISTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY

ANALYSIS OF THE LOG-DOMAIN FILTERS DESIGNED WITH E-CELLS

M.Sc. Thesis by
Burcu YALDIZ

Department : Electronics and Communication Engineering

Programme : Electronics Engineering

Thesis Supervisor: Prof. Dr. Ali Toker

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Burcu YALDIZ
(504071207)

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Supervisor (Chairman) : Prof. Dr. Ali TOKER (ITU)
Members of the Examining Committee : Prof. Dr. Serdar ÖZOĞUZ (ITU)
Prof. Dr. Özcan KALENDERLİ (ITU)

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

E-CELL DEVRELERLE TASARLANAN LOG-DOMEN SÜZGEÇLERİN ANALİZİ

YÜKSEK LİSANS TEZİ
Burcu YALDIZ
(504071207)

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Tez Danışmanı : Prof. Dr. Ali TOKER (İTÜ)
Diğer Jüri Üyeleri : Prof. Dr. Serdar ÖZOĞUZ (İTÜ)
Prof. Dr. Özcan KALENDERLİ (İTÜ)

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FOREWORD

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Burcu Yaldız

Electronics & Communication Engineer

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ABBREVIATIONS

KCL	**:** Kirchhoff`s Current Law
KVL	**:** Kirchhoff`s Voltage Law
TL	**:** Translinear
ESS	**:** Exponential state – space synthesis
$\boldsymbol{R_B}$	**:** Base resistor of BJT
$\boldsymbol{R_E}$	**:** Emitter resistor of BJT
$\boldsymbol{V_A}$	**:** Early voltage
$\boldsymbol{\beta_F}$	**:** Beta current gain
$\boldsymbol{f_c}$	**:** Cut-off frequency
Log-domain	**:** Logarithmic domain
LP	**:** Low-pass
R	**:** Resistor
C	**:** Capacitor
L	**:** Inductor
$\boldsymbol{R_S}$	**:** Source resistor
$\boldsymbol{R_L}$	**:** Load resistor
SFG	**:** Signal flow graph
NPN	**:** N-Type BJT transistor
PNP	**:** P-Type BJT transistor
RHS	**:** Right-hand side

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ANALYSIS OF THE LOG-DOMAIN FILTERS DESIGNED WITH E-CELLS

SUMMARY

The aim of this thesis is to analyze the effects of the transistor current gain, β_F, on the performance of E-cells. The effects of input and output impedance values were investigated and studied for the low-pass filters. Moreover, the sensitivity analysis for the filters were performed. While using E-cells, all the transistors are chosen as BJT transistors and for the analysis, four class of E-cell couples were considered.

Log-domain filters have received significant attention in the literature because they can work with low supply-voltage and low current at high frequencies easily. Furthermore, they offer tolerances to distortions and noise. The input and output of the log-domain filters are current but during the processes inside the filter are performed by using voltages. The logarithm of the input current is taken and a voltage is produced inside the filter. The processes inside the filter will continue and at the output, the voltage is exponentiated to produce a current at the output of the filter.

First of all, the BJT`s current gain was analyzed for the E-cells. For this purpose, model parameters were used for the BJTs of the E-cells. Then, for the same model parameters are used for the same E-cells except beta. Beta was set to big enough to act as infinite. After that, DC analysis were performed for the E-cells and the outputs of the E-cells were drawn and compared in logarithmic axis. As a result of these analysis, it was seen that, the output currents were close to each other and had a linear increase in a defined voltages. But out of these voltages, the output currents were getting far away from each other, which E-cells are simulated when beta is infinite and finite. In another words, for definite voltages, there is no difference on the output current when beta value was set to infinite or finite. But out of these ranges, when beta was set to infinite, the output current was getting away from the output current when beta is finite.

After Beta analysis was finished, the input - output impedance values were calculated per E-cell. These calculated values were used in the filter design steps. By using E-cell circuits, third order Chebychev low-pass LC ladder filter was designed. The capacitance and inductance values of this filter was calculated for the cut-off frequency. Then, low-pass log-domain filter was designed by using E-cells which is transformed from LC ladder filter by using some design steps. The transistors in the E-cells used model parameters. The capacitors placed in the log-domain filter were also calculated from the LC ladder prototype. On the other side, the input – output capacitance values were subtracted from the capacitors in the another log-domain filter designed with E-cells. The AC analysis were performed for these three log-domain filters. First filter was the LC ladder prototype, second one was the log-domain filter designed with E-cells and the third one was the filter designed with E-cells but capacitance values were subtracted from the existing values. As a result of the AC analysis, it was seen that, the cut-off frequency for the third filter had a better

output than the second filter. After this analysis, the effect of the emitter resistors were added to the third filter, which had also capacitance values effect. For this purpose, by using emitter resistors, a constant was calculated and bias currents in the filter was multiplied with this constant. AC analysis was run again to see the effects of emitter resistors and capacitors. As the result of this analysis, the emitter resistances made a fall on the cut-off frequency of the filter. Also, the cut-off frequencies of these filters were lower than the filters designed with E-cells by using model parameters and ideal capacitor values.

When this AC analysis was finished, the sensitivities of the filters were analyzed. The values of capacitors and resistors are stated with 15% tolerance and the analysis was made step by step by changing the tolerance values of the circuit elements. The simulations showed that, cut-off frequency of the filters had low sensitivity to the tolerances of capacitors and resistors. The sensitivity of the filters were seen clearly before and after the cut-off frequency. This result was same for all the designed filters.

Later works will be performed for improving the output current and cut-off frequency when adding capacitors and resistors to the filters.

E-CELL DEVRELERLE TASARLANAN LOG-DOMEN SÜZGEÇLERİN İNCELENMESİ

ÖZET

Bu tezin amacı, E-cell devrelerdeki sonsuz Beta etkisinin incelenmesi ve bu devreler kullanılarak tasarlanan alçak geçiren süzgeçlerde giriş – çıkış empedans değerlerinin etkilerinin analizi ve yorumlanmasıdır. Ayrıca süzgeçlerin duyarlılık analizleri de yapılmıştır. Buradan yola çıkarak sadece BJT tranzistörlerden oluşan dört tane E-cell devre çifti seçilmiştir.

Log-domen süzgeçlerin seçilmesindeki amaç; bu devrelerin düşük gerilim ve akım kullanarak yüksek frekanslarda kolaylıkla çalışabilmeleridir. Ayrıca bu devreler, bozulmalara ve gürültüye karşı da sahip olduğu yapı dolayısıyla diğer devre bloklarına göre daha toleranslıdır. Log-domen süzgeçler, girişinde ve çıkışında akım olan, ancak süzgeç içerisindeki işlemler sürecinde gerilimle çalışan yapılardır. Girişteki akımın logaritması alınır, gerekli işlemlerden geçer, çıkışta tekrar akım elde etmek için gerilimin üsteli alınır ve akım elde edilir.

Log-domen süzgeçlerle ilgili ilk çalışmalar Adams tarafından yapılmıştır. Ancak Adams`dan sonra uzunca bir süre kimse bu konuyla ilgili bir çalışma yapmamıştır. Aradan geçen uzun yıllar sonrasında tekrardan log-domen süzgeçlerle ilgili ilk çalışma Frey tarafından yapılmıştır. Kendisi Adams ve Seevinck'in çalışmalarından yola çıkarak, log-domen süzgeçlerin durum uzayı denklemi aracılığı ile tasarlanabileceğini belirtilmiştir. Ayrıca yine Frey'in öne sürdüğü başka bir tasarım yöntemi kullanılarak yüksek dereceden süzgeç tasarlamanın biraz karmaşık olduğu gözlenmiştir. Bu konuda Perry ve Robets'ın öne sürdüğü tasarım yöntemi ile yüksek dereceden süzgeç tasarlanması kolaylaşmıştır.

Frey, daha sonraki yıllarda log-domen süzgeç tasarımlarında kullanılmak amacıyla bir devre tasarlamıştır ve bu hücreye "E-cell" adını vermiştir. Bu hücreler aldıkları işaretin durumuna göre E+ cell ya da E- cell adını almıştır. Böylece log-domen süzgeçlerde E-cell kullanılmasına başlanmıştır. Frey'den sonra Punzenberger ve Enz de yeni bir E-cell devresi tasarlamıştır. Callegari ve Setti ise MOSFET ve BJT'lerden oluşan E-cell devreleri tasarlamışlardır.

Yapılan E-cell devre tasarımlarından sonra, Leung, E-cell devrelerde bazı idealsizlik parametrelerinin devreler ve süzgeçler üzerindeki etkilerini incelemiştir.

Yapılan bu çalışmada ise öncelikle her E-cell devresi için Beta'nın etkisi incelenmiştir. Bu nedenle, her devrede yer alan tranzistörler için ilgili model parametreleri kullanılmıştır. Daha sonra aynı hücrenin yine model parametreleri aynı fakat sadece beta değeri yeteri kadar büyük (sonsuz) seçilerek DC analizi PSPICE kullanılarak gerçekleştirilmiştir. Bu hücrelerin çıkış akımları logaritmik eksende çizdirilip karşılaştırılmıştır. Bunun sonucunda görülmüştür ki, belli gerilim aralıklarında beta sonsuzken ve normal değerdeyken, her iki E-cell devresinin de çıkış akımları birbirlerine yakın ve paralel bir şekilde doğrusal olarak artmaktadır.

Ancak bu değerler dışındaki gerilimlerde, iki çıkış akımı da birbirinden uzaklaşmaktadır. Yani diğer bir deyişle, belli gerilim değerleri için betanın sonsuz ya da sonlu olması çıkış akımı üzerinde pek fazla bir etkiye sahip değilken, bu gerilimler dışında betanın sonsuz olduğunda sahip olduğu çıkış akımı betanın sonlu olduğu değerden gittikçe uzaklaşmaktadır.

Daha sonra her bir E-cell devresi için giriş-çıkış empedans değerleri yine PSPICE kullanılarak hesaplanmıştır. Hesaplanan bu değerler daha sonraki süzgeç tasarım aşamasında kullanılmıştır.

Var olan E-cell devrelerle üçüncü dereceden Chebychev alçak geçiren LC basamak türünden bir süzgeç tasarlanmıştır. Bu süzgecin kondansatör ve bobin değerleri kesim frekansına uygun olarak hesaplanmıştır. Daha sonra LC basamak türünden devre üzerinden log-domen süzgeç yapısına geçmek için kullanılan tasarım aşamalarından geçilerek E-cell devrelerle üçüncü dereceden alçak geçiren bir süzgeç tasarlanmıştır.

Bunun için öncelikle tasarlanacak devreye uygun LC basamak türünden bir süzgeç bulunur. Bu süzgeçten yola çıkarak, bu devrenin uygun işaret akış diyagramı çıkartılır. Daha sonra bulunan işaret akış diyagramından yola çıkarak çeşitli eklemeler yapılır. Mesela, her integral alıcı devresinden sonra LOG bloğunun konması veya her süzgecin çıkışına EXP bloğunun yerleştirilmesi gibi.

LC basamak türünden E-cell devrelerle tasarlanan süzgece geçişte, kondansatör değerlerinde de gerekli değişiklikler çeşitli hesaplamalar sonucunda elde edilmiştir. Bir diğer tarafta da yine E-cell devrelerle tasarlanan log-domen süzgeç yapısında önceden hesaplanan kondansatör değerleri süzgeçteki kondansatör değerlerinden çıkarılmıştır. Burada bahsedilen üç süzgeç şunlardır: RLC türünden 3. dereceden Chebychev alcak geçiren süzgeç (ideal süzgeç), E-cell devreleri kullanılarak LC basamak türünden elde edilen süzgeç ve yine E-cell devreleriyle tasarlanan LC basamak türünden süzgeç. Ancak belirtilen son süzgecin, ikinci süzgeçten farkı, kondansatör ve direnç değerlerinin bu üçüncü süzgeç üzerinde gösterilmesidir. Bu üç süzgeç kullanılarak devrelerin AC analizleri gerçekteştirilmiştir. Bu analizler sonucunda giriş-çıkış kondansatör değerleri belirtilen son süzgeçte yer alan kondansatör değerlerinden çıkarıldığında kesim frekansında idealdeki süzgecin kesim frekansına doğru bir kayma, ya da diğer bir deyişle iyileşme görülmektedir. Daha sonra, kondansatör değerlerinin eklenmiş olduğu süzgece emetör direncinin etkisi de eklenmiştir. Bunun için emetör dirençleri kullanılarak bir sabit hesaplanmıştır ve bu sabit ile süzgeçte yer alan akımlar çarpılmıştır. Elde edilen akım değeri ile süzgeçlerin AC analizleri tekrar yapılmıştır. Bu analizler sonucunda da kesim frekansında, yani emetör direnci etkisinin süzgecin kesim frekansında bir düşmeye neden olduğu gözlenmiştir. Bu süzgeçlerin kesim frekansları, ideal durumdaki E-cell devrelerle tasarlanan süzgeçlerin kesim frekanslarından daha düşüktür.

Bu analizlerden sonra, süzgeçler için duyarlılık analizleri de gerçekleştirilmiştir. Bu analiz için de süzgeçlerde yer alan kondansatör ve direnç değerleri %15 değerinde toleransla, birer birer değiştirilmiştir ve bu yapılan değişikliklerin çıkış akımı üzerindeki duyarlılıkları incelenmiştir. Yapılan değişiklikler sonucunda, kesim frekansının, kondansatör ve dirençlerde yapılan bu değişimlere karşı fazla duyarlı olmadığı, kesim frekansı öncesi ve sonrasında ise duyarlılığın daha fazla olduğu görülmüştür. E-cell devrelerle tasarlanan tüm süzgeçlerde de yine aynı sonuçlar elde edilmiştir.

Bundan sonra yapılacak çalışmalar, E-cell devreler kullanılarak tasarlanan süzgeçlere kondansatör değerleri ve emetör dirençlerinin etkileri eklendiğinde, bu çalışmada elde edilen çıkışlardan daha iyi ve ideale yakın çıkış akımları ve kesim frekansları elde edilmesi şeklinde olabilir.

1. INTRODUCTION

Log-domain signal processing concept was known for over thirty years and for the last fifteen years, a lot Log-domain signal processing concept was known for over thirty years and for the last fifteen years, a lot of researches have been performed about this subject. The general idea of log-domain filter is to take an input signal and compress it at the input stage. Then the signal is processed in a compressed way and after all, at the output, the signal is expanded again to preserve the linearity. This is also known as companding and was introduced by Tsividis *et al.* [1]. A basic representation for log-domain filter is shown in Figure 1.1.

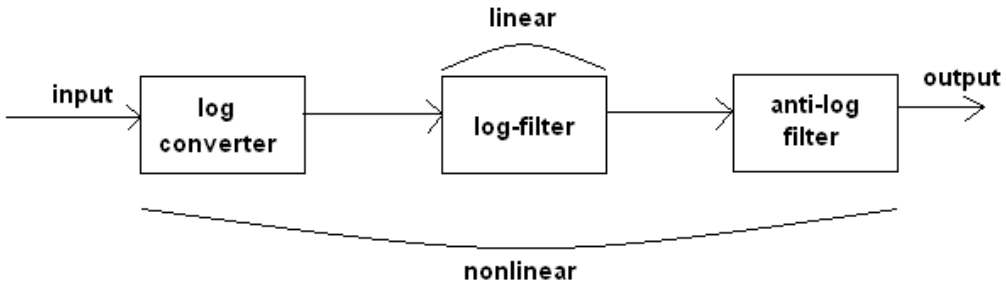


Figure 1.1 : The concept of log-domain filtering [2].

It was firstly mentioned by Adams in 1979 ([2]) and after that, it was emerged as candidate in low-power high-speed continuous time filtering concept [3]. The attraction of log-domain filters was started when Frey proposed a general state-space synthesis method [4], [5] based on the works of Adams and Seevinck [6].

Frey also proposed a new synthesis method for log-domain filters [5]. But this method is not easy to apply for higher order filters. The equations for the filter become more complex. Then Perry and Roberts proposed a new synthesis method for the design of higher order filters [7]. This method is based on the operational simulation of LC ladder networks. By using this method, a high order signal-flow graph (SFG) can be transformed with log-domain operation, by preserving the input-output relationship in linear.

Later then, a new synthesis method was proposed, Bernoulli cell. The name of this method comes from the mathematical expression of the Bernoulli equation. The translinear equation of the circuit is similar to Bernoulli equation.

When new synthesis methods were developed for making the equations calculated easily, another unknown parts of the log-domain filter was investigated. For example, Frey proposed a new circuit to design the log-domain filters by using modular circuits blocks. Frey named these cells as *E-cell*, which is similar with transconductors [5]. Also, Bernoulli cells are used again, while designing the log-domain filters.

Ungoing research on the topic leads to be new open problems. Nonidealities of E-cells are just one of them. These nonidealities of E-cells were investigated in [8] – [10]. The researchers used different E-cell blocks for studying the effects of these nonidealities.

1.1 The Purpose of the Thesis

The motivation of this work is to analyze the effects of the main transistor parameters (just for infinite Beta) and the impedances of different E-cell blocks in the log-domain filter designs. This thesis is organized as follows. In chapter two, the history of log-domain filters and E-cells is summarized. In chapter three, the E-cells blocks are simulated with BJT model parameters, with finite Beta and infinite Beta, and DC analysis are made. Also, in chapter three, the input and output impedances are calculated per E-cell block. These effects are added to the filter designs and AC analysis is performed for the third-order Chebychev low-pass log-domain filters. At last, the sensitivities of the filters are analyzed.

2. HISTORY OF LOG-DOMAIN FILTERS AND E-CELLS

Log domain filtering concept was first announced by Adams in 1979 [11]. Adams explained the log filter as: *"a circuit, composed of both linear and non-linear elements, which, when placed between a log converter and an anti-log converter* (*in the "log domain"*), *will cause the system to act as a linear filter"* [2]. Adams designed this filter shown as in Figure 2.1 by using only diodes, capacitors, current sources and op-amps.

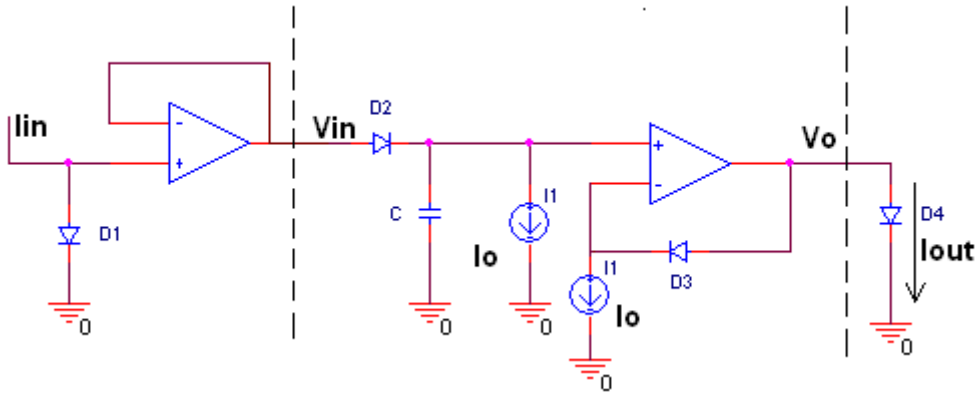


Figure 2.1 : Adam's basic log-domain filter [11].

Adams` filter can be divided in three parts by the dashed lines. The block on the left hand side performs as a log converter and the block on the right hand side performs as an anti-log converter. An input current is forced through a diode to produce a voltage. This voltage becomes the logarithm of the input current. Then, this voltage is applied to *diode-capacitor-current source* which is called as log filter. After these processes, the output is recovered by a level-shifter which is followed by an exponentiator [4].

The cut-off frequency of the filter is calculated with

$$f_{cutoff} = \frac{1}{2\pi} \cdot \left(\frac{I_o}{V_T C}\right) \qquad \textbf{(2.1)}$$

In the equation (2.1), the I_o means bias current, V_T means Threshold voltage which is nearly 26 mV and C means the capacitor value. But this proposed filter has

disadvantages as a result of using op-amps such as implementation of logging, level-shifting and the exponentiating functions. Also using opamps degrade performance, owing to noise DC offset and frequency limitations [4].

After Adams` works about log-domain filter, many people wasn't interested about this topic until 1990s. In this year, Frey proposed a general log-domain filter design approach known as "*exponential state-space synthesis (ESS)*" [5]. Moreover, Frey proposed an idea that log-domain filters can be realised by using only capacitors, transistors and current sources. Frey also used mapping technique so that state variables are related to current, not voltage.

After a couple of years, when Frey named a kind of transconductor as "*E-cell*" in 1996 [5] (also the first E-cell block was proposed in this year), the log-domain filter designs with E-cells began. An E-cell circuit was formed by the emitter-follower plus offset. E-cell circuits require little loop gain so that very high frequency operations will be possible.

The general state space representation of a linear filter from [5] is shown as follows:

$$\dot{x}(t) = A(t) + Bu(t) \quad \textbf{(2.2)}$$

$$y(t) = Cx(t) + Du(t) \quad \textbf{(2.3)}$$

In the equations (2.2) and (2.3), $x(t) = (x_1(t), x_2(t), ..., x_N(t))^T$ is vector of state variables, dot over x means differentiation, $u(t)$ and $y(t)$ are scalar input and output signals, A is an $n \times n$ matrix, B and C are $n \times 1$ matrices and D is a scaled feed through from the filter input to the output.

If the Laplace transform of the equations (2.2) and (2.3) is taken, it can be

$$sX(s) = AX(s) + BU(s) \quad \textbf{(2.4)}$$

$$Y(s) = CX(s) + DU(s) \quad \textbf{(2.5)}$$

Then $X(s)$ in equation (2.4) can be eliminated and replaced it in equation (2.5), so it can be

$$(sI - A)Y(s) = U(s)(CB + D) \quad \textbf{(2.6)}$$

After all, rearranging equation (2.6), the transfer function of $H(s)$ will be,

$$H(s) = \frac{Y(s)}{U(s)} = C(sI - A)^{-1}B + D \quad \textbf{(2.7)}$$

Then the mapping on the state variables are defined by

$$f(V_i) = x_i \quad \textbf{(2.8)}$$

(2.8) is substituted into (2.7) and the result is

$$F`(V)\dot{V} = AF(V) + BU \quad \textbf{(2.9)}$$

$$Y = CF(V) + DU \quad \textbf{(2.10)}$$

where $F(V) = X = (f(V_1), f(V_2), ..., f(V_N))^T$ and $F^{'}(V)$ is a Jacobian matrix.

There are N state equations. If both sides of (2.9) and (2.10) are multiplied by $C_i / f^{'}(V_i)$, the x state equation will be as follows:

$$C_i\dot{V}_i = \frac{C_i}{f`(V_i)}AF(V_i) + \frac{C_iB_i}{f`(V_i)}U \quad \textbf{(2.11)}$$

for i = 0, 1, 2, …, N.

Equation (2.11) will be defined as a node equation. Left-hand side of the equation defines a current which is flowing into a grounded capacitor connected to the i-th node and V_i is thought as the i-th node voltage. In conclusion, the right-hand side (RHS) of the equation will be the sum of currents flowing into this capacitor.

The RHS of the equations are expanded into a sum of terms and $f^{-1}(\cdot)$ is applied to the input that is assumed to be a current and the predistorted voltage V_O is produced. The RHS of the equation can be written as a sum of N terms and

$$C_i\dot{V}_i = \sum_{j=1}^{N} C_iA_{ij}\frac{f(V_j)}{f`(V_i)} + C_iB_i\frac{f(V_o)}{f`(V_i)} \quad \textbf{(2.12)}$$

In this equation, A_{ij} is the *ij*-th element of state matrix A.

Each term on the RHS takes the form of a controlled nonlinear transconductance.
The output equation is written same as follows: creating a node voltage V_{N+1} with a grounded constant voltage source. Y is defined as current, flowing into this new source.

$$Y = \sum_{j=1}^{N} C_{oj}\frac{f(V_j)}{f`(V_{N+1})} + D_o\frac{f(V_o)}{f`(V_{N+1})} \quad \textbf{(2.13)}$$

$$C_{oj} = C_o f^{'}(V_{N+1}) \tag{2.14}$$

$$D_{oj} = D_o f^{'}(V_{N+1}) \tag{2.15}$$

(2.13), (2.14) and (2.15) can be realized with an output current i_{out} responds to a pair of voltages V_i and V_j and written as in equation (2.16)

$$i_{out} = K_{ij} \frac{f(V_j)}{f^{'}(V_i)} \tag{2.16}$$

Voltage N + 1 will be chosen zero for convenience. K_{ij} is some constant which is named as conductance later. If $i = j$ then the trasconductor can be replaced by a simpler circuit. After all these equations, Figure 2.2 represents the filter structure.

Figure 2.2 : Basic ESS (exponential state space) filter structure [5].

Basically, this filter structure can be explained just like that:

$f^{-1}(.)$ applies the inverse of f(.) to u (the current) and produce V_O (the voltage). Then this signal is processed by the core nonlinear filter circuitry. Finally, the output current is obtained by mapping one or more of the core filter voltages with the function f(.). Another word, to get mathematical equations, the following steps should be done which are listed below:

- Represent filter in state space formulation.
- Transform dynamical equations into nodal equations using (2.8).

All these equations made by Frey was to define a log filter such as

$$x_i = f(V_i) = I_{st} e^{\alpha V_i} \tag{2.17}$$

where I_{st} and α are real constants and their units are A and V^{-1}.

Substituting (2.17) in (2.16) and rearranging it again, a new equation will be as

$$i_{out} = K_{ij} \frac{I_{st} e^{\alpha V_j}}{\alpha I_{st} e^{\alpha V_i}} = \frac{K_{ij}}{\alpha} e^{\alpha (V_j - V_i)} \tag{2.18}$$

The complementary bipolar transistor is easily designed if $\alpha = 1/2V_T$ where $V_T = kT/q$ is the thermal voltage. K_{ij} will be positive or negative. The circuit implementation for each case is shown in Figure 2.3a and Figure 2.3b where $I_{ij} = |K_{ij}|/\alpha$. Frey named these transconductors as "E+ cell" or "E- cell", corresponding to the signs of K_{ij}.

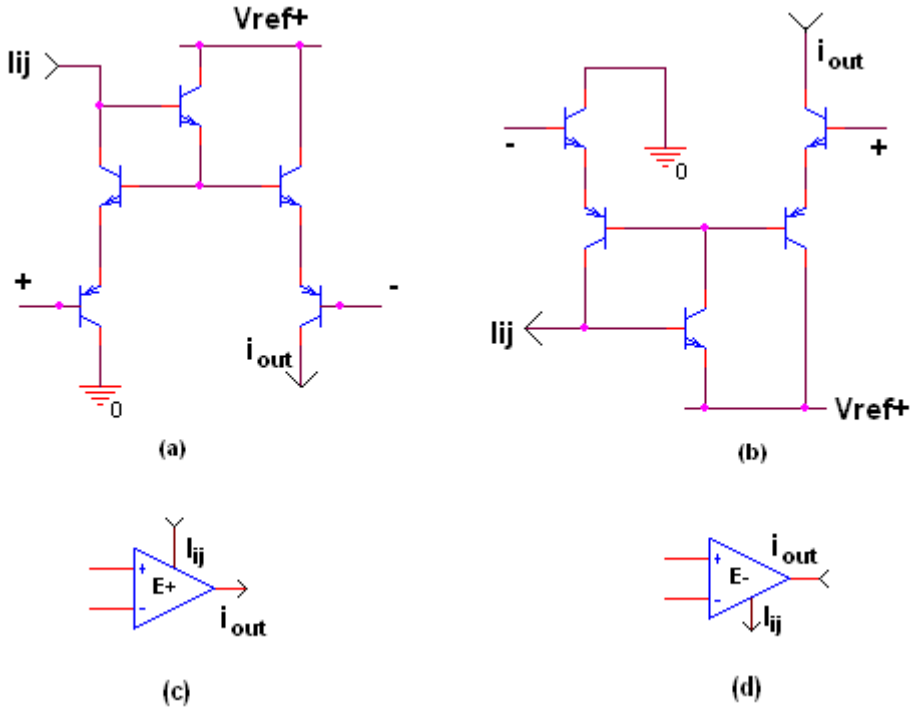


Figure 2.3 : a) Positive and b) Negative E-cell transconductors for log filters and their respective circuit symbols c) and d) [5].

By using E-cells in Figure 2.3, Frey designed a bandpass filter and analyzed it. The simulated filter is shown in Figure 2.4.

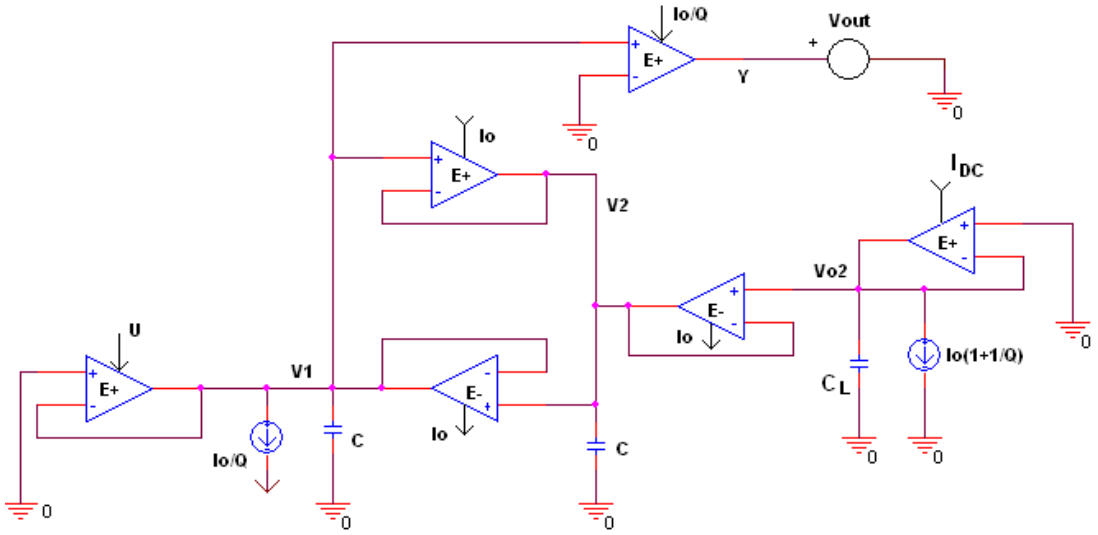


Figure 2.4 : Log filter implementation of a bandpass filter [5].

In 1996, another E-cell was proposed by Punzenberger and Enz [12]. Enz *et al.* designed a new single-ended log-domain integrator and then, they improved this circuit by adding BJTs, current sources, etc. Companding technique and current-mode approach are used for increasing the dynamic range.

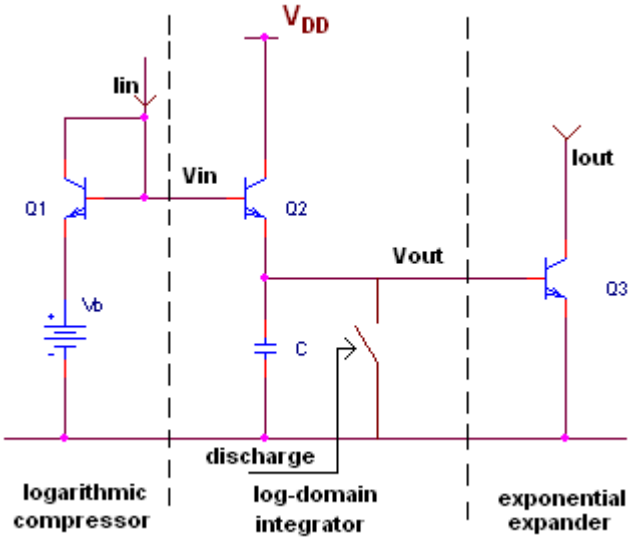


Figure 2.5 : Principles of current-mode filtering [12].

In Figure 2.5, the transistor Q1 and voltage source Vb form logarithmic compressor, Q_2 and C form a log-domain integrator and finally Q3 is used for exponential expander. Also, assuming all transistors is ideal and base currents are neglected.

The circuit in Figure 2.5 is not useful because C has to be charged and discharged periodically. This makes the input current restricted to positive values. Also, base current (I_B) limits the gain and introduces distortion.

Thus, to minimize the effects of base currents:

- BJT transistors are replaced by MOSFET operating in weak inversion region,
- Follower circuits are inserted,
- Some base current cancellation circuitry is added.
- A circuit principle which is rather insensitive to base currents is used.

The E-cell used in proposed filter is shown in Figure 2.6 [12].

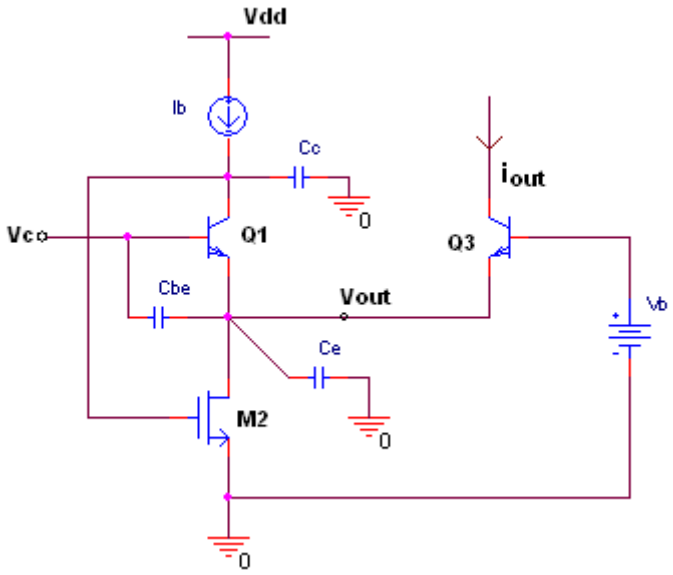


Figure 2.6 : The E- cell used in [12], [13].

According to the last two combinations of methods explained above, a new circuit was proposed. It is shown in Figure 2.7 [12].

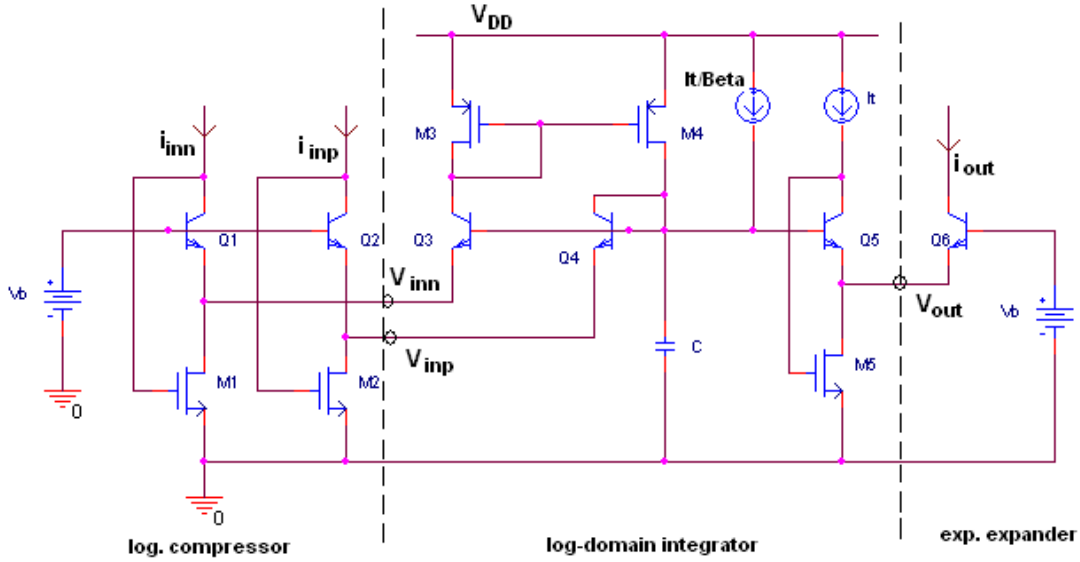


Figure 2.7 : Proposed single-ended integrator [12].

Fox *et al.* increased the number of E-cells that they used in their paper [14]. A translinear loop will be applied to the E+ cells (including V+, Q1, Q2 and V-) and E-cells (including V+, Q3, Q4, V- for the Figure 2.8 and 2.9 and V+, Q4, Q3, Q5,Q6, V- for the Figure 2.10) in Figure 2.8 – 2.10. So the output current for E+ cell or noninverting cell is

$$I_{outP} = I_O exp\left[\frac{V_+ - V_-}{V_t}\right] \quad \textbf{(2.19)}$$

E- cell or inverting cell provides an inverted current.

$$I_{outN} = I_O exp\left[\frac{V_- - V_+}{V_t}\right] \quad \textbf{(2.20)}$$

The E-cells analyzed in [14] are shown in Figures 2.8 - 2.10.

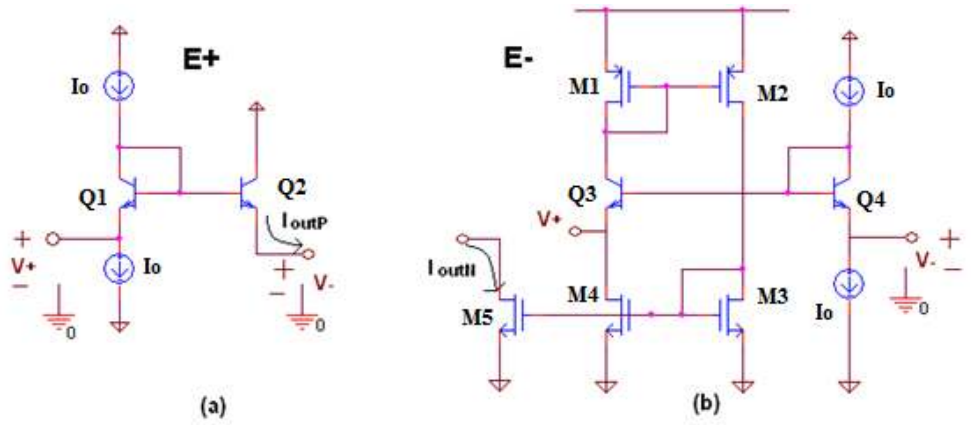


Figure 2.8 : a) E+ (noninverting) and b) E- (inverting) log-domain cells [14].

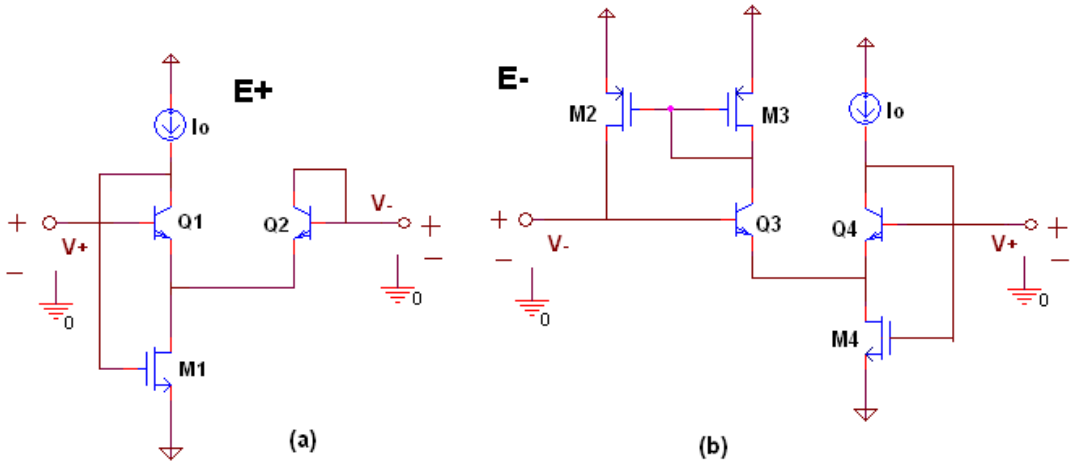


Figure 2.9 : a) E+ and b) E- log-domain cell topologies [14].

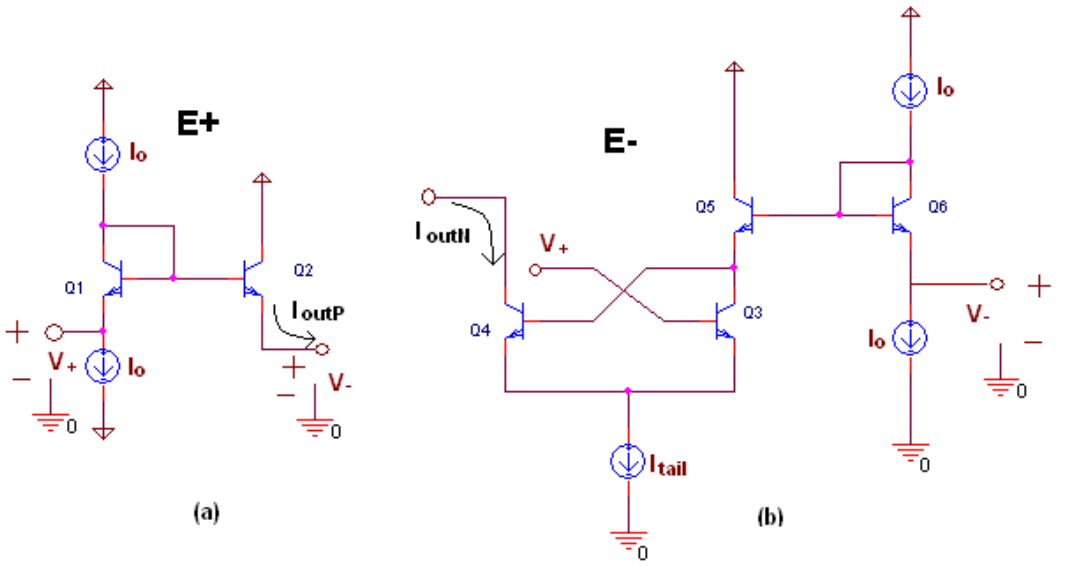


Figure 2.10 : a) E+ and b) E- log-domain cell topologies [14].

Fox *et al* [14] used these three E-cell couples. They designed a single-ended log-domain second order lowpass/ bandpass filter and analyzed the output current in different situations to determine which E-cell couple provides better output.

Callegari and Setti also investigated E-cell based design strategies. By using these, Setti *et al.* introduced a duality principle which can allow finite β_F compensation [8]. The E-cell couples used in [5] and [8] are shown in Figure 2.3, 2.11 and 2.12.

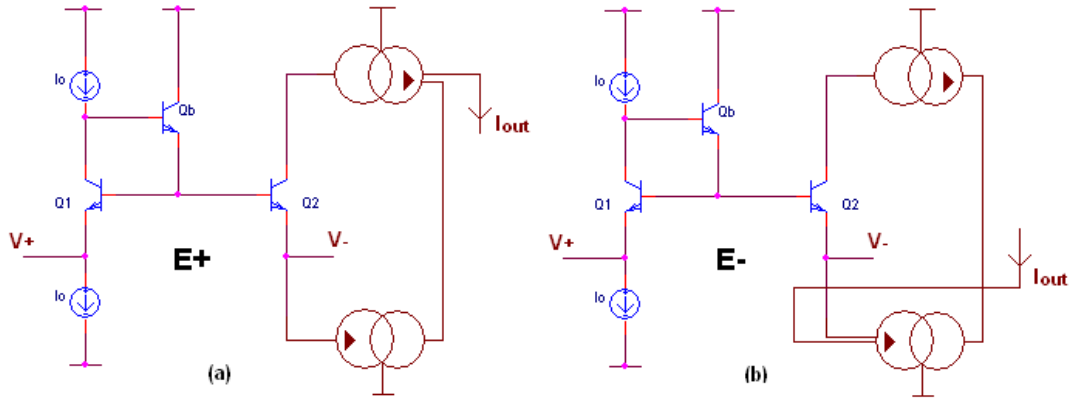


Figure 2.11 : a) E+ and b) E- log-domain cells with base coupled transistors [8].

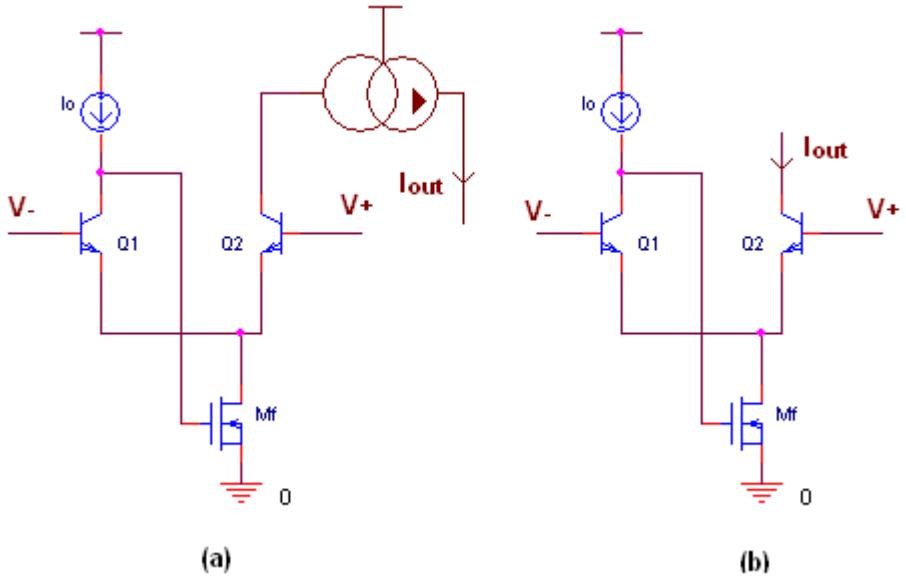


Figure 2.12 : a) E+ and b) E- log-domain cell with emitter coupled transistors [8].

The E-cells that Callegari and Setti analyzed are composed of both MOSFET and BJT transistors.

Finally, during the analysis about E-cells, Leung made a research about the transistor nonidealities in log-domain filter [9]. These nonidealities are

- parasitic emitter resistance,
- parasitic base resistance,
- finite Beta effect and
- Early voltage.

Leung designed a biquad log-domain filter by using the E- cell and the E+ cell shown in Figure 2.13.

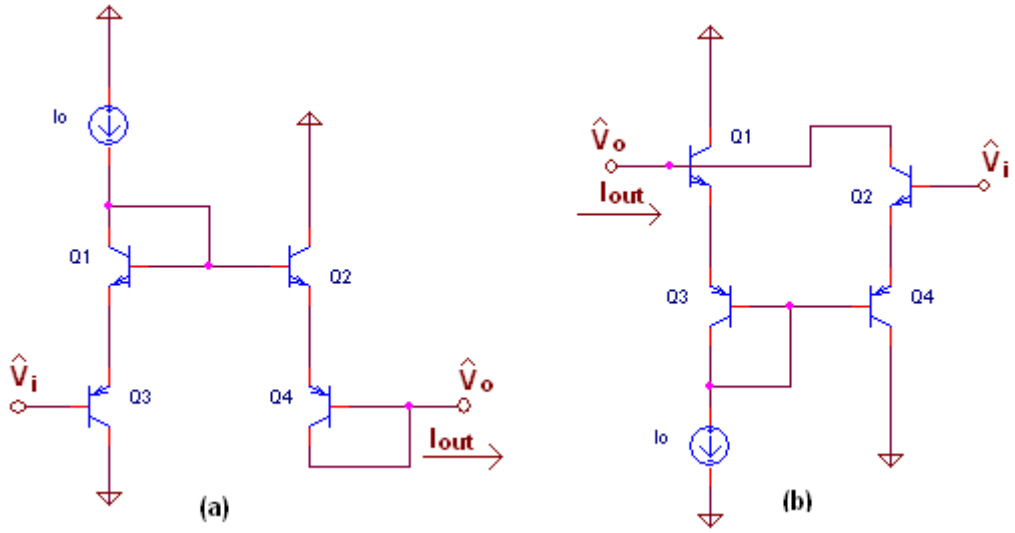


Figure 2.13 : a) E+ cell and b) E- cell circuits [9].

In the beginning of the analysis, Leung used translinear analysis to calculate the output current.

$$I_{out} = I_O e^{(\hat{V}_i - \hat{V}_o)/(2V_T)} \quad \textbf{(2.21)}$$

Leung combined the two E-cells (E- cell and E+ cell) with a capacitor to form the log-domain integrator shown in Figure 2.14.

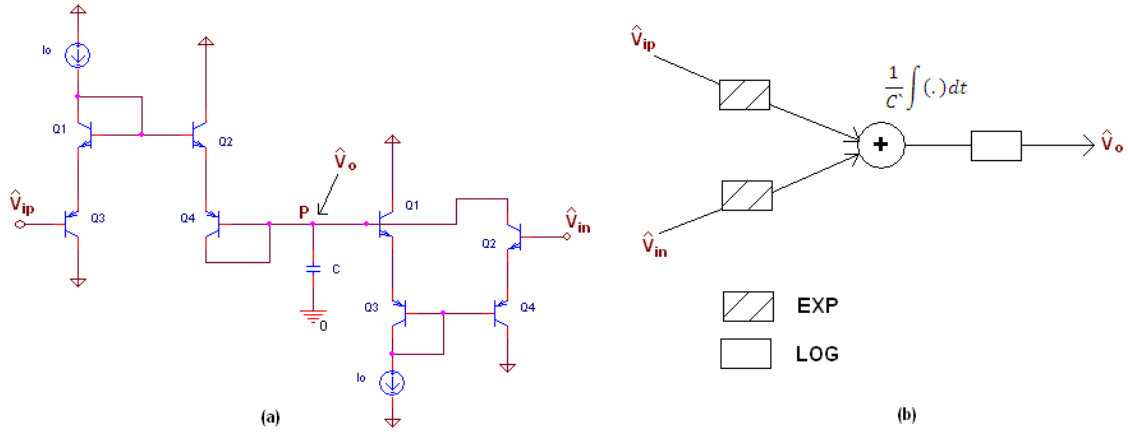


Figure 2.14 : a) The log-domain positive and negative integrator pair; and b) the corresponding log-domain integrator SFG [9].

KCL is applied at node P and

$$C\frac{d\hat{V}_o}{dt} = I_o e^{(\hat{V}_{ip} - \hat{V}_o)/(2V_T)} - I_o e^{(\hat{V}_{in} - \hat{V}_o)/(2V_T)} \quad \textbf{(2.22)}$$

is calculated. Both sides of the equation is multiplied by $e^{\hat{V}_o/2V_T}$ and the chain rule is applied,

$$\frac{2V_T}{I_o} C \frac{d}{dt}\left(I_o e^{\hat{V}_o/2V_T} - I_o\right) = \left(I_o e^{\hat{V}_{ip}/2V_T} - I_o\right) - \left(I_o e^{\hat{V}_{in}/2V_T} - I_o\right) \quad \textbf{(2.23)}$$

By using equation (2.22), EXP and LOG functions will be defined as follows:

$$LOG(x) = 2V_T ln\left(\frac{I_o + x}{I_o}\right) \quad \textbf{(2.24)}$$

$$EXP(x) = I_o e^{x/2V_T} - I_o \quad \textbf{(2.25)}$$

and the log-domain integration

$$EXP\left(\hat{V}_o\right) = \frac{1}{C`} \int \left\{EXP\left(\hat{V}_{ip}\right) - EXP\left(\hat{V}_{in}\right)\right\} dt \quad \textbf{(2.26)}$$

will be written, where $C` = (2V_T/I_o)C$.

Leung calculated a transfer function for the filter and he calculated the output current for every nonideality parameter.

Employing these blocks, an ideal low-pass log-domain biquad realizing the transfer function (2.27) is built using the operational simulation of LC ladders as shown in Figure 2.15 [9]

The filter equation is

$$H_{ideal}(s) = \frac{1}{s^2 + (\omega/Q)s + \omega^2} \quad \textbf{(2.27)}$$

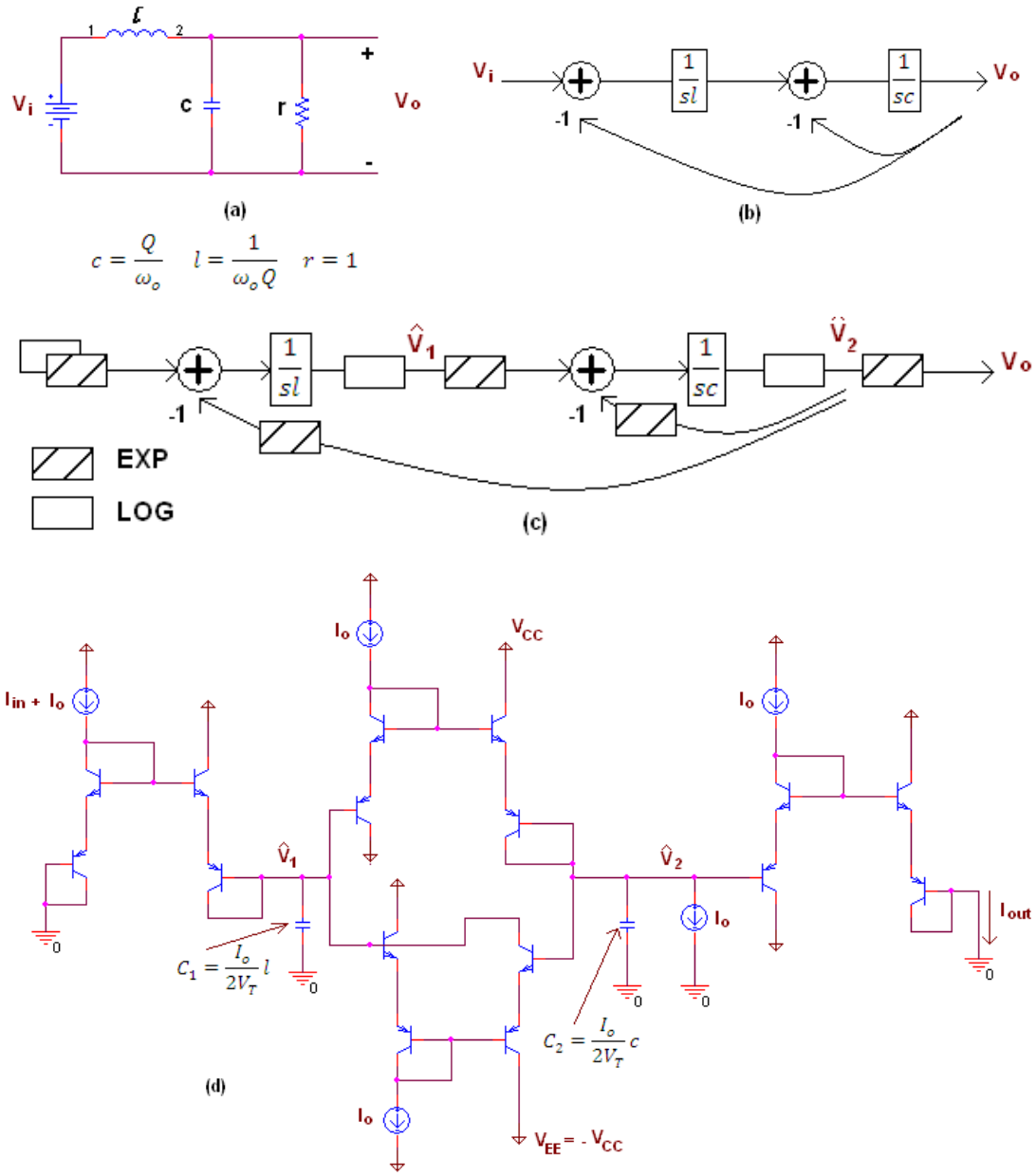


Figure 2.15 : a) LP LC biquad prototype, b) the corresponding SFG, c) log-domain SFG, d) log-domain biquad filter [9].

Effects of Parasitic Emitter Resistance

By applying KVL in E+ cell and E- cell in Figure 2.13a and 2.13b after adding the emitter resistors is given in equation (2.28), one obtained,

$$\hat{V}_i + (R_{EN} + R_{EP})(I_o - I_{out}) - 2V_T ln\left(\frac{I_{out}}{Io}\right) - \hat{V}_o = 0 \qquad \textbf{(2.28)}$$

where R_{EN} and R_{EP} are respectively the emitter resistances for NPN and PNP BJT transistors. By rearranging equation (2.27), one obtained,

$$I_{out} \cong I_o e^{\frac{\hat{V}_i - \hat{V}_o}{(R_{EN}+R_{EP})I_o + 2V_T}} \quad \textbf{(2.29)}$$

is. Assuming $R_{EN} = R_{EP} = R_E$ and $2R_E = R_{EN} + R_{EP}$ yields

$$C\frac{d\hat{V}_o}{dt} = I_o e^{\frac{\hat{V}_{ip} - \hat{V}_o}{2R_E I_o + 2V_T}} - I_o e^{\frac{\hat{V}_{in} - \hat{V}_o}{2R_E I_o + 2V_T}} \quad \textbf{(2.30)}$$

Both sides of the equation is multiplied by $e^{\frac{\hat{V}_o}{(2R_E I_o + 2V_T)}}$ and newly defined LOG and EXP functions appear as [9].

$$LOG(x) = (2R_E + 2V_T)\ln\left[(I_o + x)/I_o\right] \quad \textbf{(2.31)}$$

$$EXP(x) = I_o e^{x/(2R_E + 2V_T)} - I_o \quad \textbf{(2.32)}$$

The result of log-domain integration with the effect of R_E is taken account

$$EXP(\hat{V}_o) = \left(\frac{V_T}{R_E I_o + V_T}\right) \cdot \frac{1}{C} \cdot \int \{EXP(\hat{V}_{ip}) - EXP(\hat{V}_{in})\} dt \quad \textbf{(2.33)}$$

Equation (2.33) is compared with equation (2.26) and it shows that there is a scalar error k which is due to by the parasitic emitter resistance in the log-domain integrator.

Effects of Current Gain of the BJT, Beta

To analyze the effect of finite Beta, KVL is used in Figure 2.13 that leads to

$$I_{out} = \frac{I_o e^{\left(\hat{V}_i - \hat{V}_o\right)/(2V_T)}}{1 + \frac{1}{\beta + 1} e^{\left(\hat{V}_i - \hat{V}_o\right)/(2V_T)}} \quad \textbf{(2.34)}$$

The equation (2.34) shows us an undesirable negative feedback under the presence of finite beta that is shown in Figure 2.16a.

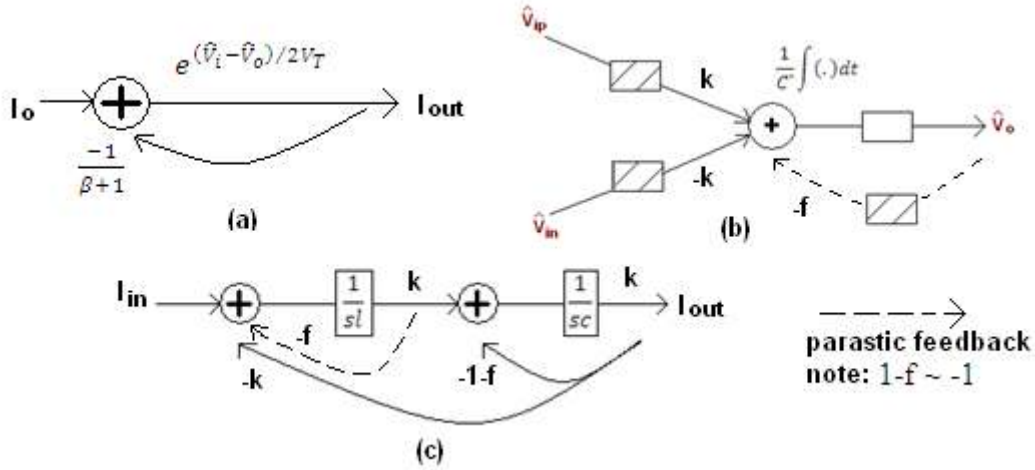


Figure 2.16 : a) Feedback mechanism of log-domain cells, b) log-domain integrator SFG, c) biquad SFG [10].

Equation (2.34) is rewritten as

$$C\frac{d\hat{V}_o}{dt} = k \cdot I_o e^{(\hat{V}_{ip}-\hat{V}_o)/2V_T} - k \cdot I_o e^{(\hat{V}_{in}-\hat{V}_o)/2V_T} - f \cdot I_o \quad \textbf{(2.35)}$$

In the equation written above, *f* represents negative feedback and *k* represents scalar error. These two terms are the key effects of β [9]. Finally, the log-domain integrator equation becomes

$$EXP(\hat{V}_o) = \frac{1}{C}\int \left\{k \cdot \left(EXP(\hat{V}_{ip}) - EXP(\hat{V}_{in})\right) - f \cdot EXP(\hat{V}_o)\right\} dt \quad \textbf{(2.36)}$$

Effects of Parasitic Base Resistance

The effect of parasitic base resistance is not seen unless Beta is finite. Also, R_B adds an additional voltage, $R_B I_C/\beta$ across each device in translinear loop.

Nonzero R_B only lowers ω_o. Its effect is enlarged with higher bias current and lower Beta [10].

Effects of Early Effect

Early voltage modulates the current I_S [9] as

$$I_{S,eff} = I_S \cdot \left(1 + \frac{V_{CE}}{V_A}\right) \quad \textbf{(2.37)}$$

The KVL is applied to Figure 2.16 and the output current with the effect of Early voltage is

$$I_{out} = \sqrt{\lambda} I_o e^{(\hat{V}_i-\hat{V}_o)/2V_T} \quad \textbf{(2.38)}$$

where

$$\lambda = \frac{\left(\frac{1+V_{CE2}}{V_{AN}}\right)\left(\frac{1+V_{CE4}}{V_{AP}}\right)}{\left(\frac{1+V_{CE1}}{V_{AN}}\right)\left(\frac{1+V_{CE3}}{V_{AP}}\right)} \qquad \textbf{(2.39)}$$

In equation (2.38), V_{AN} voltage means Early voltage for NPN BJT transistor, V_{AP} means Early voltage for PNP BJT transistor and V_{CE} means the collector-emitter voltage.

I_{out} is equivalent to bias current and I_o is replaced by $\sqrt{\lambda} I_o$.

V_A slightly drops the actual f_{cutoff}, raise filter gain and lower Q [9].

After 4 years, in 2004, Oiza and Psychalinos analyzed the nonidealities effect of E-cells in [10] same as Leung *et al.* did in [9] but using different E-cell couples. This E-cell couple is shown in Figure 2.17.

The E-cells that Oiza and Psychalinos used composed of only NPN BJT transistors. Oiza *et al.* investigated the nonideal effects such as base resistance, finite β and emitter resistance. At last, Oiza and Psychalinos designed a third order Chebychev low-pass log-domain filter. The aim of [10] is how to compensate these nonideal effects.

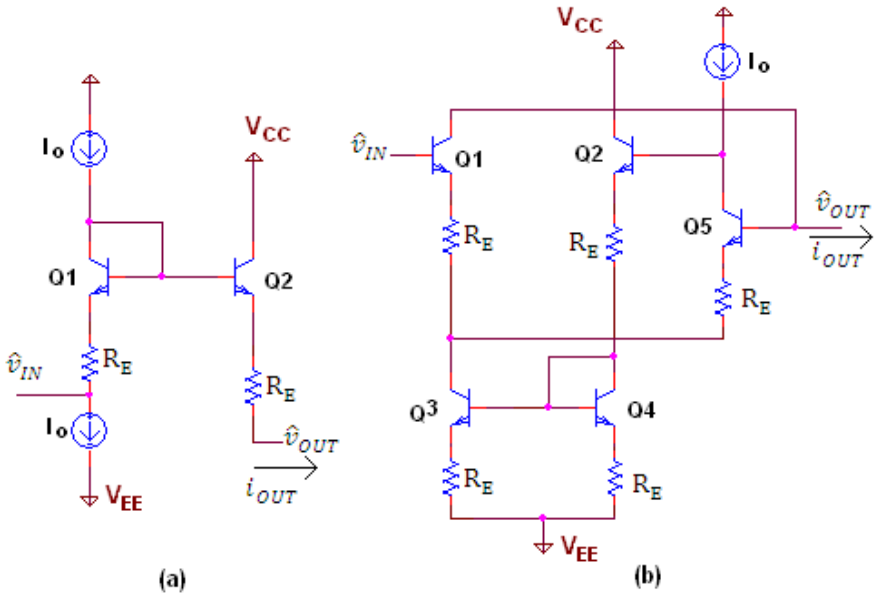


Figure 2.17 : a) E+ cell and b) E- cell with the effect of parasitic emitter resistance [10].

The first nonideality is the effect of emitter resistance. Figure 2.17 shows the emitter resistor added circuit.

As Leung did before, the analysis should begin with the KVL to E+ cell around Q1 and Q2.

$$\hat{v}_{IN} + R_E(I_o + i_{out}) - V_T \cdot ln\left(\frac{i_{out}}{I_o}\right) - \hat{v}_{OUT} = 0 \quad \textbf{(2.40)}$$

The circumflexes mean log-domain signal is followed, I_O is the DC current and V_T is the thermal voltage which is also expressed as kT/q [10].

Equation (2.40) can be simplified by using first-order Taylor series approximation and

$$i_{OUT} \cong I_o \cdot \left[1 + \frac{\hat{v}_{IN} - \hat{v}_{OUT}}{V_T + I_o R_E}\right] \quad \textbf{(2.41)}$$

The internal voltages $\hat{v}_{IN}$ and $\hat{v}_{OUT}$ are limited to a range of few of V_T's and the equation $\hat{v}_{IN} - \hat{v}_{OUT} \ll V_T + I_o R_E$ could be considered [10]. So, the equation (2.41) is rewritten again and the output current becomes

$$i_{OUT} \cong I_o e^{\frac{\hat{v}_{IN} - \hat{v}_{OUT}}{V_T + I_o R_E}} \quad \textbf{(2.42)}$$

Same calculations are done for E- cell and the output current for E- cell is same in equation (2.42). Using the equation (2.42), LOG, EXP and the output voltages for the E-cells are

$$LOG(x) = (V_T + I_o R_E) \cdot ln\left(\frac{I_o + x}{I_o}\right) \quad \textbf{(2.43)}$$

$$EXP(x) = I_o e^{\frac{x}{V_T + I_o R_E}} - I_o \quad \textbf{(2.44)}$$

$$EXP(\hat{v}_{OUT}) = \frac{V_T}{(V_T + I_o R_E)} \cdot \frac{I_o}{C V_T} \int \{EXP(\hat{v}_{IN1}) - EXP(\hat{v}_{IN2})\} dt \quad \textbf{(2.45)}$$

The emitter resistance R_E introduces a scalar error to the output of integrator and it affects only the cut-off frequency of the derived log-domain filter [10]. The cut-off frequency is lower than the ideal log-domain filter.

To compensate the introduced error, Oiza and Psychalinos proposed that the DC current sources should be adjusted by the nominal value of I_o by the factor

$$k_{RE} = \frac{V_T + I_o R_E}{V_T} \quad \textbf{(2.46)}$$

For analyzing the effect of finite Beta, KVL is applied to E+ cell.

$$\hat{v}_{IN} - \hat{v}_{OUT} = -V_T \cdot ln\left(\frac{i_{c1}}{I_S}\right) + V_T \cdot ln\left(\frac{i_{c2}}{I_S}\right) \quad \textbf{(2.47)}$$

In the above equation, i_{C1} and i_{C2} are the collector currents of the transistors Q1 and Q2. I_S is the saturation current of the base-emitter junction.

By rearranging equation (2.47), the output current for E+ cell becomes

$$i_{OUT} = \frac{I_o \cdot e^{\frac{\hat{v}_{IN}-\hat{v}_{OUT}}{V_T}}}{1+\frac{1}{\beta+1} \cdot e^{\frac{\hat{v}_{IN}-\hat{v}_{OUT}}{V_T}}} \quad \textbf{(2.48)}$$

and the output current for E- cell is

$$i_{OUT} = \frac{I_o \cdot e^{\frac{\hat{v}_{IN}-\hat{v}_{OUT}}{V_T}} + \frac{1}{\beta} I_o}{1+\frac{\beta+2}{\beta} \cdot \left[1+e^{\frac{\hat{v}_{IN}-\hat{v}_{OUT}}{V_T}}\right]} \quad \textbf{(2.49)}$$

The Beta introduces a scalar error and an extra feedback in the configuration of integrator. This scalar error can be compensated by adjusting the nominal value of DC current sources, I_o. As a result, by injecting this extra DC current at the capacitor node, the feedback is canceled.

For the compensation of the effect of finite Beta, it will be shown with the effect of parasitic base resistance. Because parasitic base resistance effects only when the finite Beta effect is considered.

By applying KVL on E+ cell, the output current is

$$\hat{v}_{IN} - \hat{v}_{OUT} = -V_T \cdot ln\left(\frac{i_{c1}}{I_S}\right) + V_T \cdot ln\left(\frac{i_{c2}}{I_S}\right) + i_{B1}R_B + i_{B2}R_B \quad \textbf{(2.50)}$$

If equation (2.50) is rearranged, the output current for E+ cell becomes

$$i_{OUT} \cong I_o e^{\frac{\hat{v}_{IN}-\hat{v}_{OUT}}{V_T + I_o \frac{R_B}{\beta}}} \quad \textbf{(2.51)}$$

The output current for E- cell is same as in equation (2.51).

Parasitic base resistance also introduces a scalar error and this affects only the cut-off frequency of the derived filter just like the emitter- resistance did. To prevent it, the nominal value of DC current source, I_o should be multiplied by the factor

$$k_{RB} = \frac{V_T + I_o \frac{R_B}{\beta}}{V_T} \quad \textbf{(2.52)}$$

Up to this point, the history of the log-domain filters and E-cells were specified. The researches made about these filters and designs were presented. The nonidealities of the E-cells with their mathematical expressions were analyzed. At last, compensation methods of these nonidealities were specified. Finally, the analysis part of this thesis is going to be started. DC analysis of the specified E-cells were investigated.

3. ANALYSIS OF E-CELLS

3.1 DC Analysis of E-cells

In section 2, a literature survey on log-domain filters and E-cells are presented. Then, in this section, the DC analysis of different E-cell blocks is going to be presented. For this purpose, four different E-cell couples are used. All the analyzed E-cells that contain BJTs. The E-cells considered are shown in Figure 3.1.

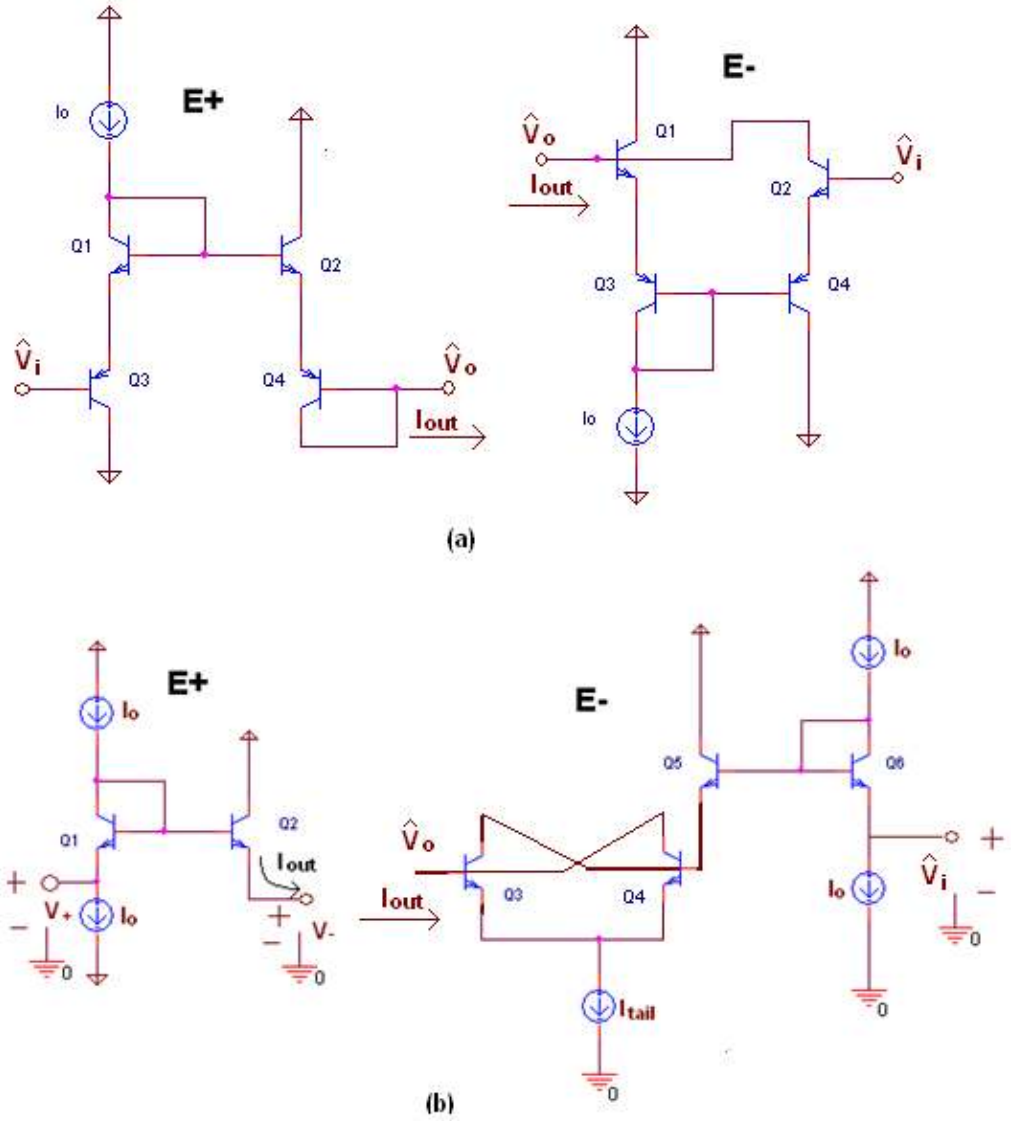


Figure 3.1 : The first group of analysed E-cell blocks, a and b [9], [14], [17].

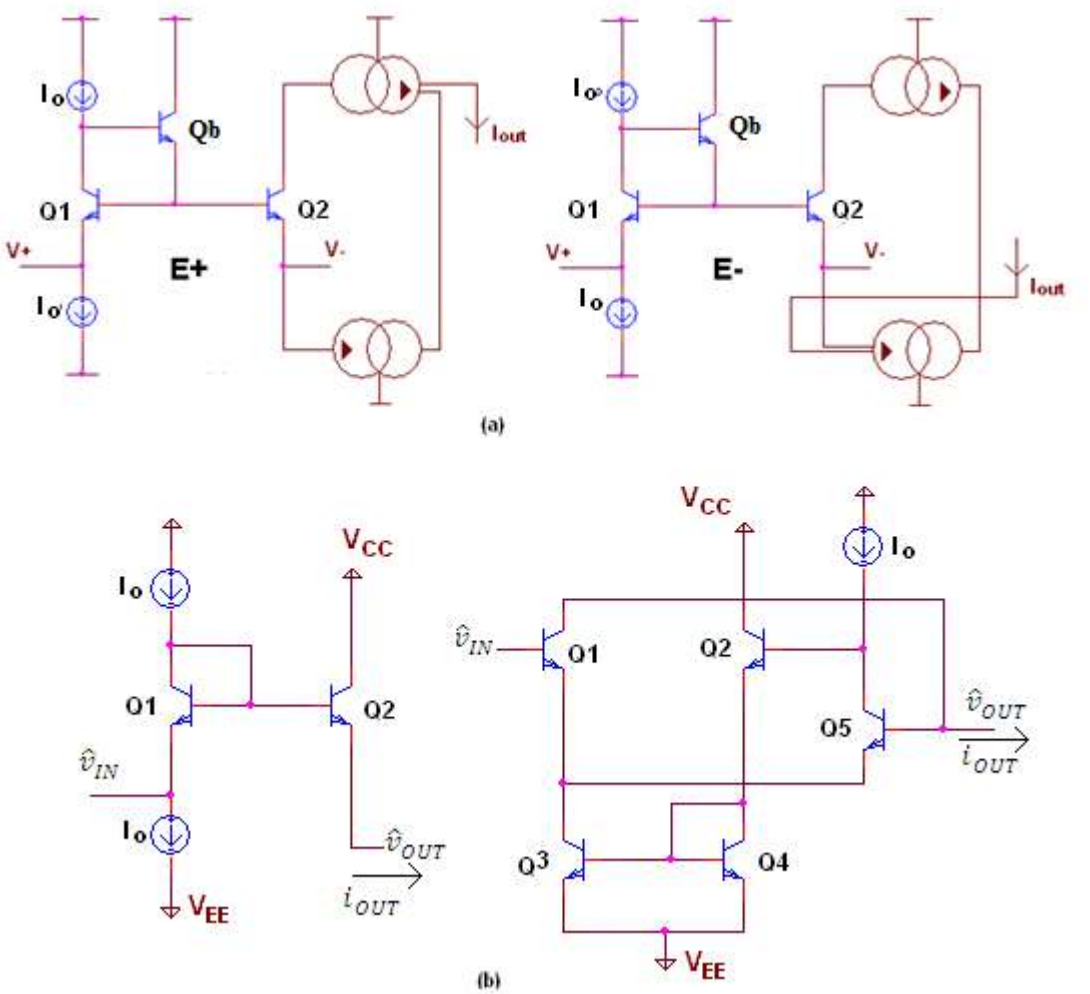


Figure 3.2 - The second group of E-cell blocks, a and b [8], [10].

The output current equation for the E-cells in Figure 3.1a is

$$I_{out} = I_o e^{(V_i - V_o)/2V_T} \quad \textbf{(3.1)}$$

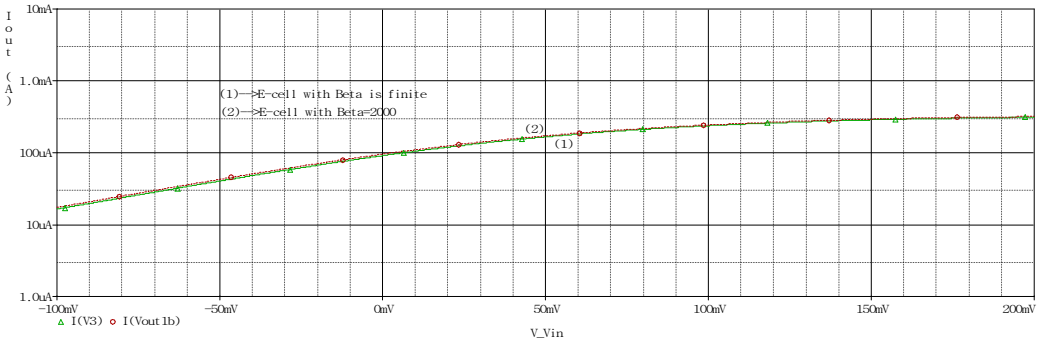
The output current equation for the E-cells in Figure 3.1a, 3.2a, and 3.2b is

$$I_{out} = I_o e^{(V_i - V_o)/V_T} \quad \textbf{(3.2)}$$

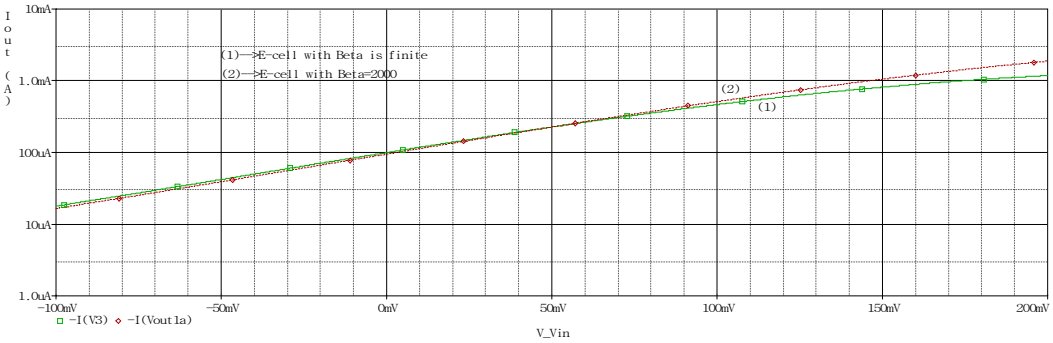
During the analysis, the bias current, I_o, was set to $100\mu A$ and the supply voltage was $\pm$1.65V.

For the DC analysis, BJT transistors use NPN1X and PNP1X model parameters, presented in [23]. During the analysis, two model parameters are used for each E-cell. One E-cell is simulated by using model parameters shown in [23]. Then, the same E-cell is simulated with parameters in [23] but this time, only BF value is set big enough (β_F = 2000) to act as infinite.

The results of the DC analysis are shown in Figure 3.3 - 3.6. For all the figures, the characteristic labeled as (1) shows the output current for E-cell with finite Beta. The characteristic labeled as (2) shows the output current for E-cell with infinite Beta. The y – axis show the output current and x – axis shows the positive bias voltage of the E-cell.

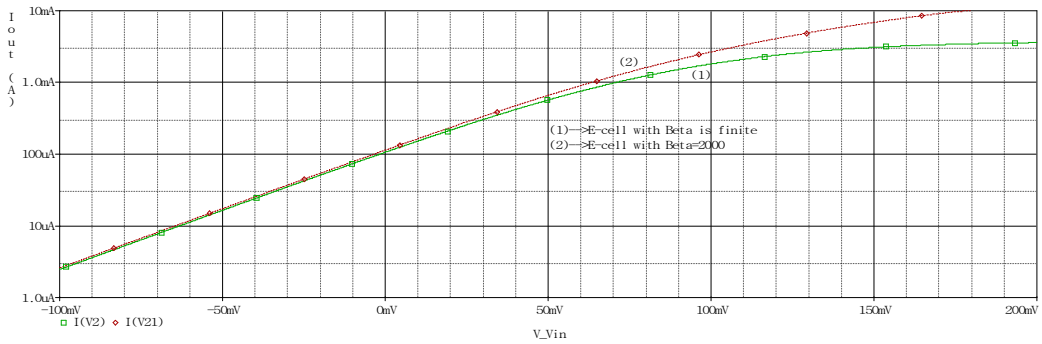


(a)

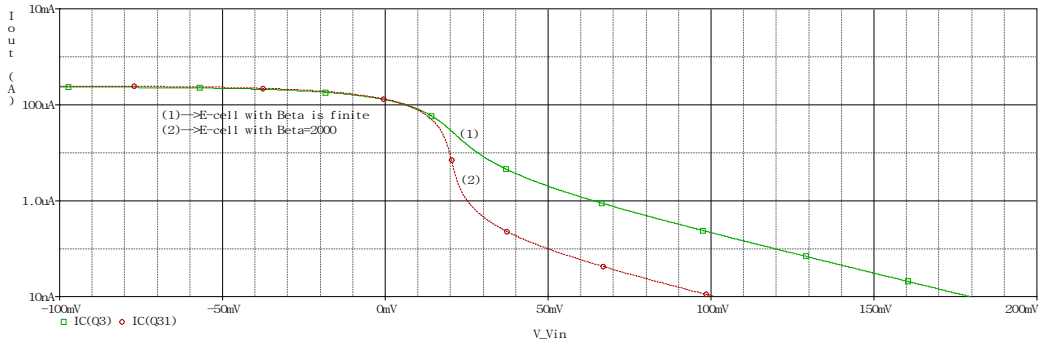


(b)

Figure 3.3 : The output currents for the a) E+ cell and b) E- cell in Figure 3.1a.

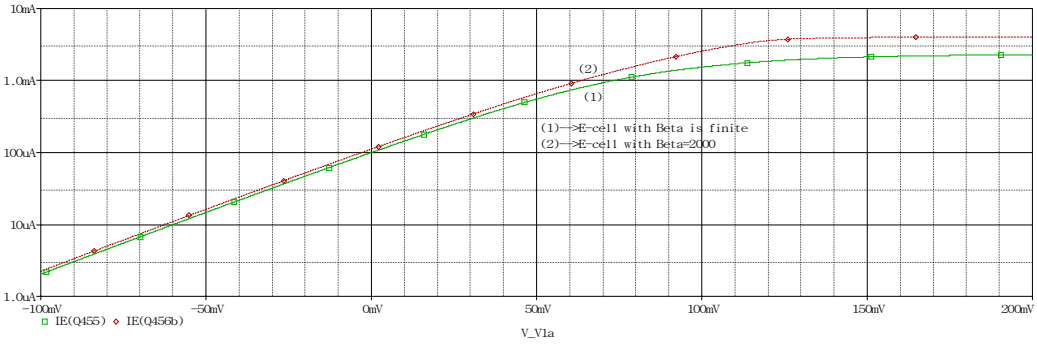


(a)

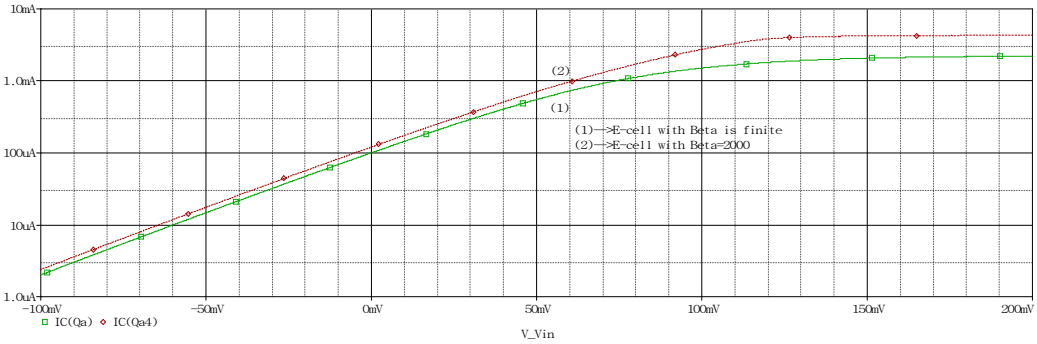


(b)

Figure 3.4 : The output currents for the a) E+ cell and b) E- cell in Figure 3.1b.

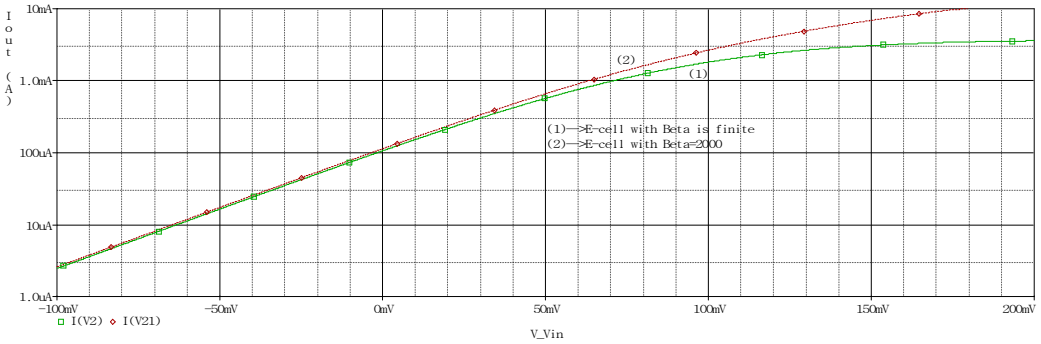


(a)

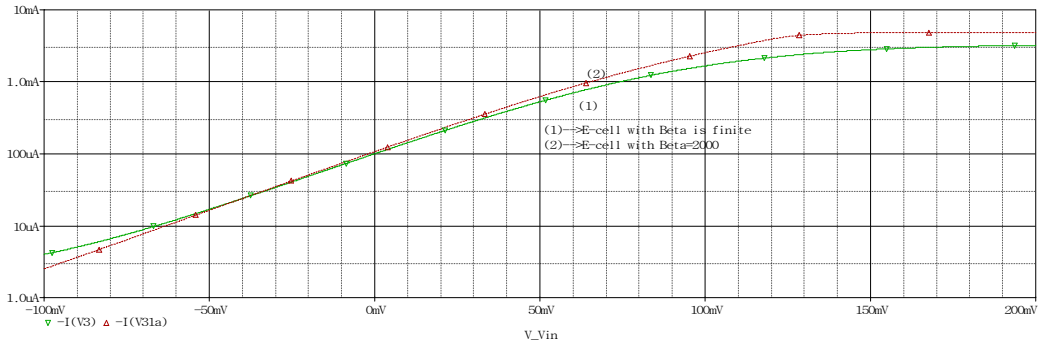


(b)

Figure 3.5 : The output currents for the a) E+ cell and b) E- cell in Figure 3.2a.



(a)



(b)

Figure 3.6 : The output currents for the a) E+ cell and b) E- cell in Figure 3.2b.

When the output currents are increasing in logarithmic axis, the two output currents for different Beta values are nearly close to each other for defined voltages ranges. But if the output current is still increasing while the bias voltage is increasing (except for the Figure 3.4b), the effect of finite Beta will be seen clearly. The output current gets far away from the output current of E-cell designed with BJT model parameters than the E-cell designed with infinite Beta. For the Figure 3.4b, the output current decreases while the positive bias voltage increases. And the output current which has infinite Beta, has smaller output current than the output current with finite Beta.

To simulate the circuits with infinite Beta value, Beta is set to 2000, much larger than its nominal value.

3.2 AC Analysis of E-cells

3.2.1 Specifying the values of parasitic capacitors and resistors

Following the results, illustrating DC behaviour of the values of the E-cells in the previous section, the values of the parasitic capacitors and resistors are calculated in this section.

First, considered E+ cell is shown in Figure 3.1a.

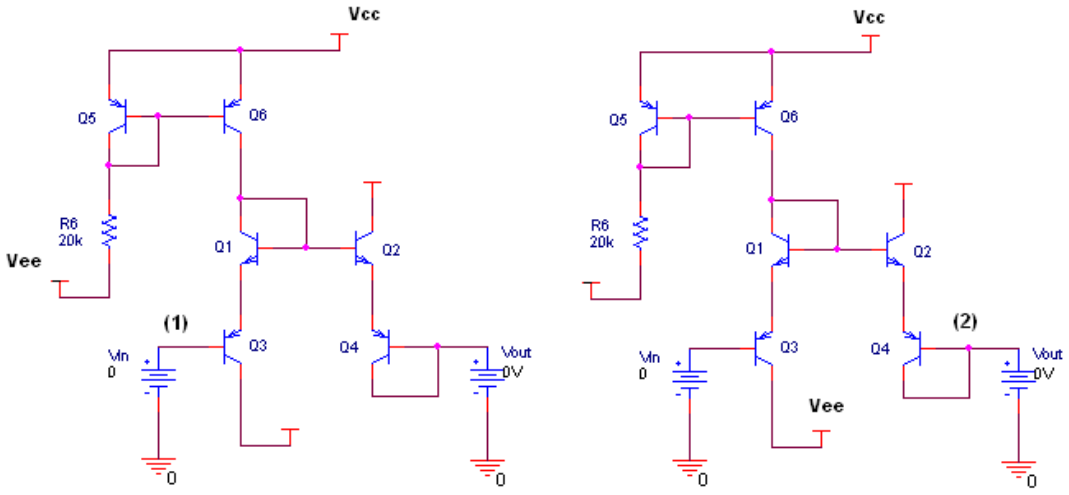


Figure 3.7 : Calculating parasitic capacitances by using E-cells.

For example, an AC voltage source is connected in series with the input of the E+ cell, labeled as (1). The current of AC voltage source is measured. Calculating the imaginary part of the current gives the input capacitance value and the real part gives the input parasitic resistance. The capacitance and resistance values are constant at a definite frequency. But after that frequency, the output decreases as the frequency increases. Then, the AC voltage source is connected to the output of the E+ cell (in series with the DC voltage source), point (2) in Figure 3.7 and current of this point will be measured. Again, calculation of the imaginary and real parts gives the parasitic capacitance and resistance. When the analysis is finished for the first E+ cell, similar steps are performed for the rest of the E-cells in Figure 3.1 and as a result, parasitic capacitance and resistance values ($C_{in}, C_{out}, R_{in}, R_{out}$) are derived.

By using simple equations, imaginary and real parts of the impedance will be calculated. For this purpose it can be written as $V = Z_{EQ}.I$ and it becomes as $\frac{V}{I} =$

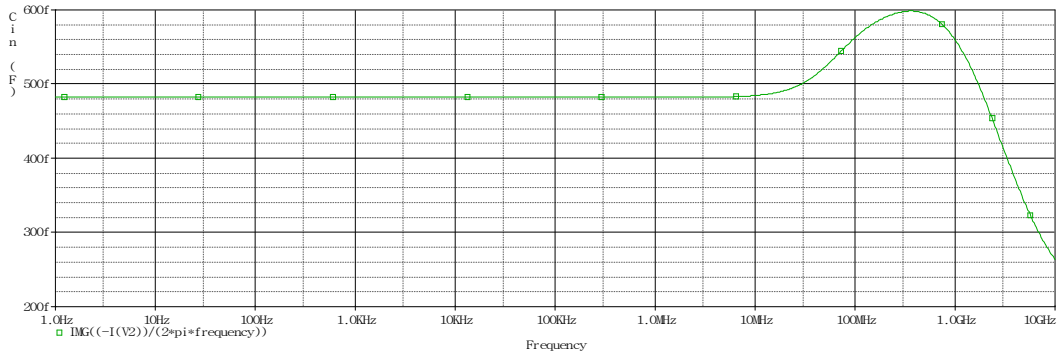
Z_{EQ}. If V equals to 1 (1V AC), then $1/I = Z_{EQ}$ and by rewriting it, the current will be equal to I = Y_{EQ}= sC + G

In the above equations, Z_{EQ} means equivalent impedance value, Y_{EQ} means equal admittance and G means conductance. The values of capacitances and resistances will be calculated in PSPICE by

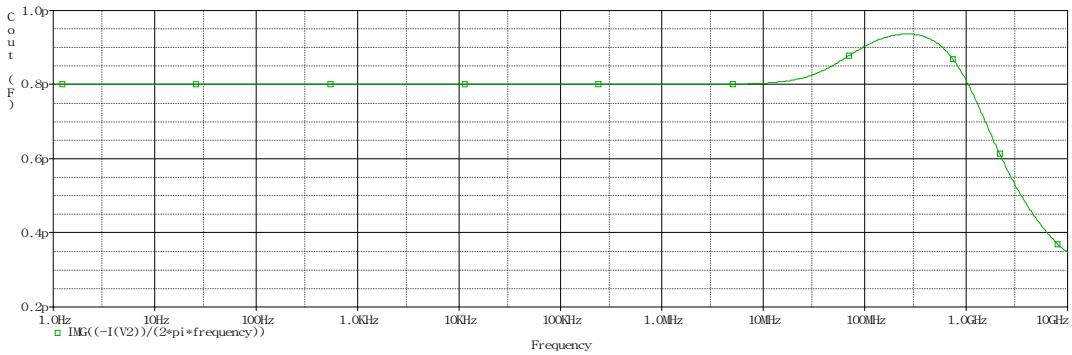
Capacitance = $IMG((I)/2\pi f)$

Resistance = 1/G = 1/ R(I)

Where f means frequency, IMG(I) means imaginary part of the admittance, and R(I) means the real part of the current at the AC voltage source applied to the E-cell.



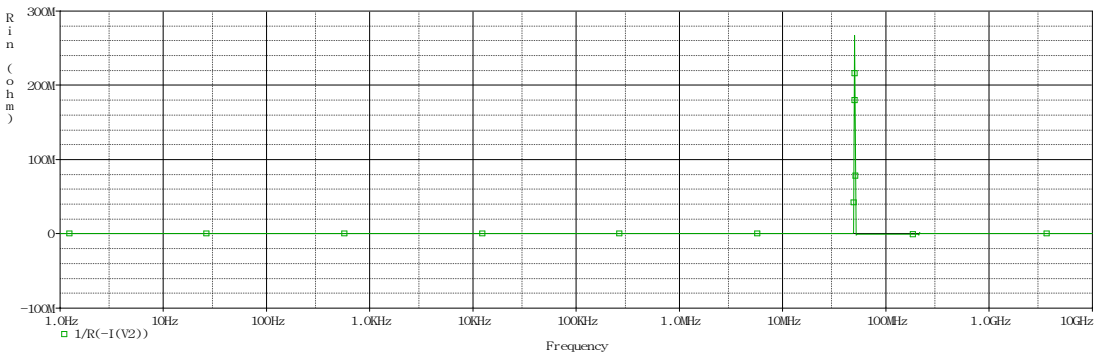
(a)



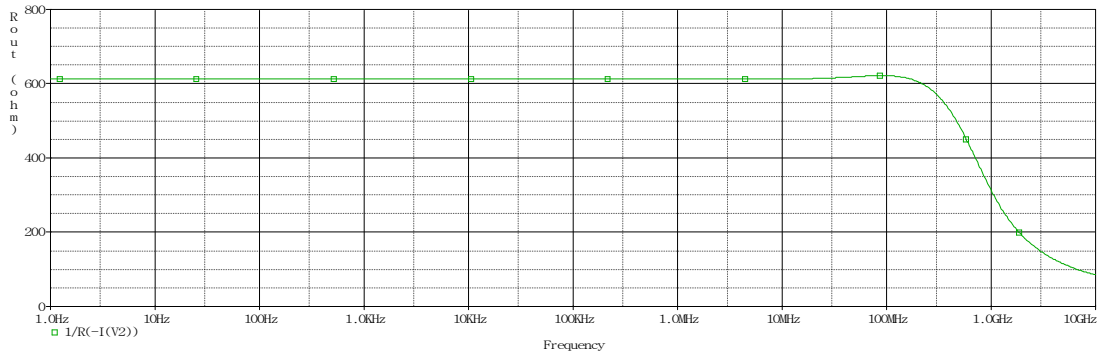
(b)

Figure 3.8 : Capacitance values for E+ cell a) C_{in} and b) C_{out} for the Figure 3.1a.

The current value for the AC voltage source is measured. Then the real part of the current is calculated. As a result, the resistance values are calculated for each E-cell where the frequency is stable until a definite frequency.



(a)



(b)

Figure 3.9 : Resistance values for E+ cell a) R_{in} and b) R_{out} for the Figure 3.1a.

The simulated values for the capacitance and resistances are listed in Table 3.1.

Table 3.1 : The resistance and capacitance values for the E-cells in Figure 3.1.

	Cin (F)	**Cout (F)**	**Rin (Ω)**	**Rout (Ω)**
Figure 3.1a – E+ cell	0.4p	0.8p	62.4k	611
Figure 3.1a – E- cell	68p	2.56p	65	-757
Figure 3.1b – E+ cell	3.72p	-0.1p	13.5k	258
Figure 3.1b – E- cell	2.74p	4.12p	-16.5k	-254
Figure 3.2a – E+ cell	-1.73n	3.53p	1	290
Figure 3.2a – E- cell	-1.53n	2.31n	1	4.7
Figure 3.2b – E+ cell	3.72p	-0.1p	13.5k	258
Figure 3.2b – E- cell	1.76p	4.41p	14.5k	-297

In the Table 3.1, some values are negative or much larger than the expected values. For example, the output resistance for the E- cell in Figure 3.1a is negative. Because there is a positive feedback in the circuit and when the input voltage is increased, the current at the output decreases. And these effects make the output resistance value negative.

Until now, DC analysis was performed for all the E-cell couples to determine the effect of Beta. For this purpose, two model parameters were used. First E-cell was designed with model parameters shown in [23]. Second model parameters were just same as in [23] but in this model, Beta was set to big enough to act as infinite. The output currents were compared in section 3.1.

When the DC and AC analysis were finished, analyzing the effects of capacitors and resistors were started. The aim of the this analysis was to simulate the filters designed with E-cells shown in Figure 3.1 and 3.2 and including the impedance values which were calculated in section 3.2.1.

3.2.2 Analyzing the third order low-pass Chebychev log-domain filter

After all the DC and AC analysis are finished for E-cells, the next step is to simulate a filter to see the effects of capacitances and resistances. Therefore, a third-order Chebychev low-pass filter is used. The steps that are used for designing filter are:

- Find an LC ladder that meets the design specifications,
- Derive the corresponding SFG from LC ladder prototype,
- Modify the SFG to obtain the log-domain equivalence,
    - Placing a LOG block after each integrator,
    - Placing an EXP block at the input to each summer, before the multiplicative factor)
    - Placing an EXP block at the output of the system,
    - Placing a LOG block at the input to the system,
- Replace the integrator branches of the log-domain SFG with log-domain integrator circuit [2].

This filter can be modeled by using only R, L, C and voltage source as shown in Figure 3.10.

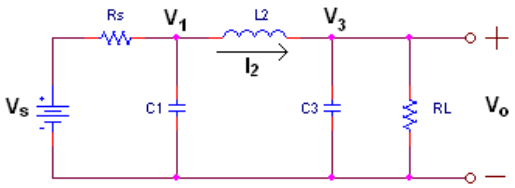


Figure 3.10 : 3rd order Chebychev low-pass LC ladder prototype [2].

To obtain the signal flow graph (SFG) of the filter, the modified nodal analysis is applied to the points of V_1, V_3 and I_2. The results are

$$I_2 = \frac{1}{L_2} \cdot \int (V_1 - V_3) dt \quad \textbf{(3.3)}$$

$$V_1 = \frac{1}{C_1} \cdot \int \left(\frac{V_S}{R_S} - I_2 - \frac{V_1}{R_S} \right) dt \quad \textbf{(3.4)}$$

$$V_3 = \frac{1}{C_3} \cdot \int \left(I_2 - \frac{V_3}{R_L} \right) dt \quad \textbf{(3.5)}$$

The DC gain of the circuit shown in Figure 3.10 is 0.5 so to compensate for this loss, the voltage across the load resistor is scaled by a factor of 2 and it becomes

$$V_{out} = 2 \cdot V_3 \quad \textbf{(3.6)}$$

By using the equations from (3.3) to (3.5), the SFG of the LC ladder prototype will be drawn and it is shown in Figure 3.11.

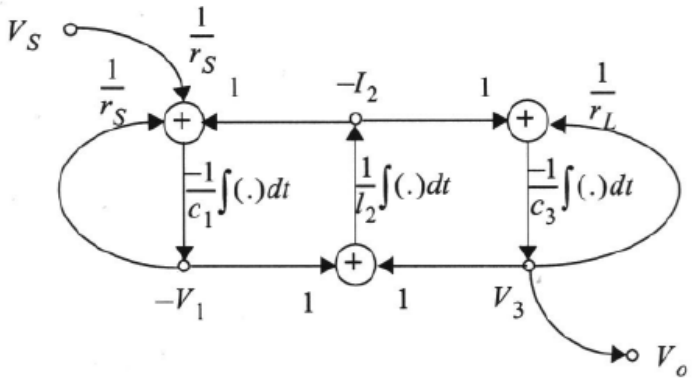


Figure 3.11 : Corresponding linear SFG of Figure 3.10 [2].

After that, the mappings shown below should be done.

$$V_s \Leftrightarrow I_{in} \qquad V_1 \Leftrightarrow \hat{V}_1 \qquad V_3 \Leftrightarrow \hat{V}_3$$

$$I_2 \Leftrightarrow \hat{V}_2 \qquad V_o \Leftrightarrow I_{out}$$

By using the Figure 3.12, the filter will be drawn with the LOG and EXP blocks.

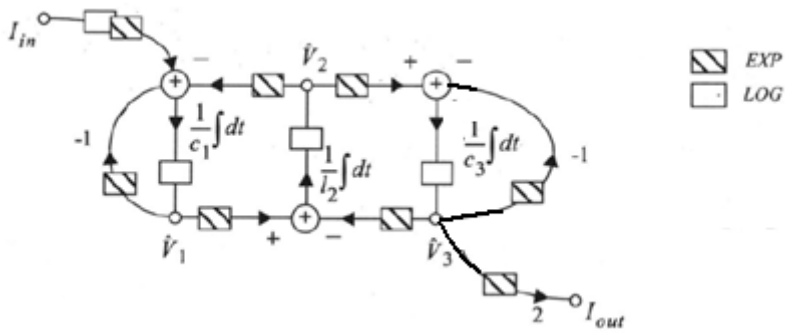


Figure 3.12 : The SFG of the 3rd order Chebychev low-pass log-domain filter [2].

The values of capacitances and inductance will be transformed into capacitors to place in the filter designed with E-cells. This transformation will be done as follows:

$$(c_1, l_2, c_3) = \frac{I_o}{2V_T}(C_1, C_2, C_3) \qquad \textbf{(3.7)}$$

$I_o/2V_T$ comes from the output current equation of the E-cell. I_o means the bias current and V_T is the threshold voltage. At last, the EXP block at the output is biased with $2I_o$ to account for the DC gain of the LC ladder [2].

By using the E-cells shown in Figure 3.1a, the log-domain filter is designed as shown in Figure 3.13

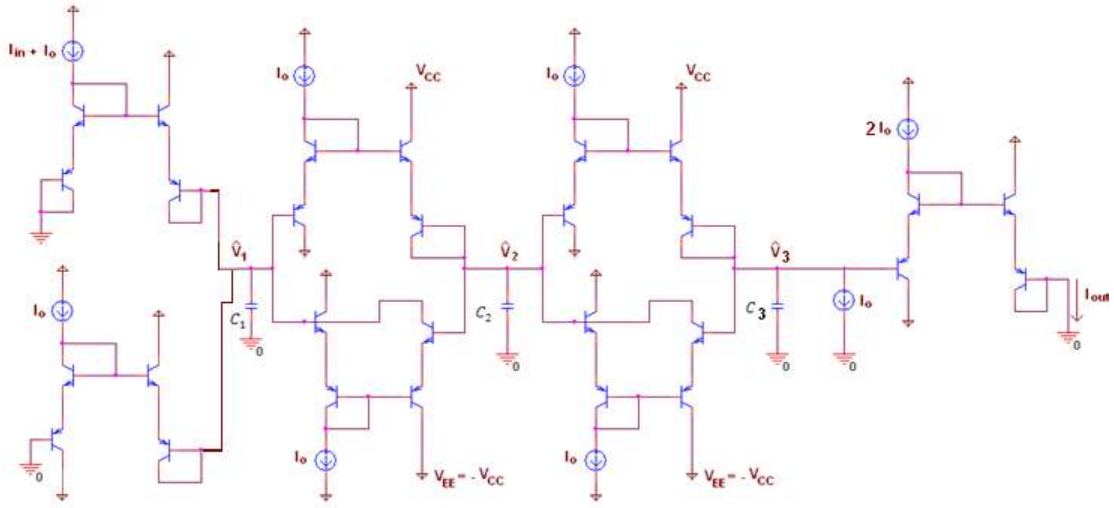


Figure 3.13 : The 3rd order Chebychev low-pass log-domain filter [2].

In this figure, I_{in} is the AC current source and the voltages with the circumflexes are the currents which transformed into voltages.

By using the analysis method and steps mentioned here, analyzing the filters with different E-cell couples will be done. First of all, the calculations of the capacitors and inductor values for the lowpass LC ladder prototype are done. From [15], the normalized values of capacitors and inductor are selected for the third order Chebychev filter design having 0.5 dB ripple with 1 rad/s bandwith. The R_s and R_L values are stabilized to 1Ω. The capacitance values are C1 = C3 = 2.0236 F and inductance value is L2 = 0.9941 H for 0.5db ripple with 1 rad/s bandwith.

The cut-off frequency is selected as 10 MHz for filters. So the capacitance and inductance values should be calculated by using this cut-off frequency.

$$\hat{C} = \frac{C}{2\pi f R} \tag{3.8}$$

$$\hat{L} = \frac{LR}{2\pi f} \tag{3.9}$$

New values for the capacitors are $\hat{C}$ = C1 = C3 = 32.222 nF and $\hat{L}$= L2 = 15.829 nH. These values are going to be replaced in Figure 3.14. By using Thevenin`s theorem in Figure 3.10; voltage source – source resistor combination is transformed into current source – source resistor combination.

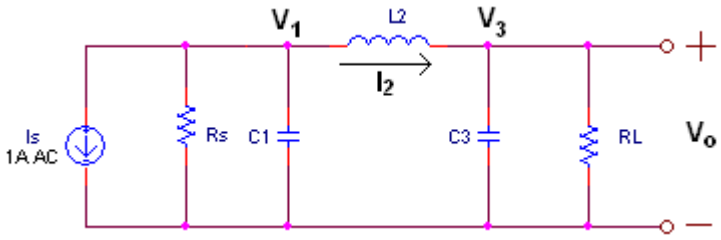


Figure 3.14 : 3rd order Chebychev low-pass LC ladder prototype drawn in Pspice.

The next step is to calculate the values of capacitances in the filter which is designed with E-cells. For the circuits, shown in Figure 3.1a, capacitance values are

$$\text{C1} = \text{C3} = \hat{C}\frac{I_o}{2V_T} \tag{3.10}$$

$$\text{C2} = \hat{L}\frac{I_o}{2V_T} \tag{3.11}$$

and for the rest of the E-cells (shown in Figure 3.1b, 3.2a and 3.2b) the capacitor values will be calculated by using below equations.

$$\text{C1} = \text{C3} = \hat{C}\frac{I_o}{V_T} \tag{3.12}$$

$$C2 = \hat{L}\frac{I_o}{V_T} \quad \textbf{(3.13)}$$

In above equations, from (3.10) to (3.13), I_o is taken as 100μA. When the LOG and EXP equations are calculating, differentiating the output current gives us I_o/V_T or $I_o/2V_T$ as a multiplying factor. This is also defined in equation (2.25).

All these values are going to be placed in the filters designed with E-cells. These E-cells form a third order Chebychev low-pass log-domain filter. This filter can be drawn by using sample blocks shown in Figure 3.1 and 3.2.

By using E-cells couples, four filters are simulated. First filter is designed with E-cells shown in Figure 3.1a and the capacitance values are C1 = C3 = 61.965 pF and C2 = 30.441 pF. For the other filter designs, by using another E-cell couples show in Figure 3.1b, 3.2a and 3.2b, the capacitance values are C1 = C3 = 123.93 pF and C2 = 60.882 pF. $I_{in} = I_1 = I_2 = I_O$ are selected as 100 μA.

When all the designs are finished, the next step is to compare the filters. During the comparison, three different shapes of the same filter are used. The first one is the third order low-pass LC ladder filter. The second one is the third order Chebychev low-pass log-domain filter designed with E-cells. The BJTs in E-cells use model parameters shown in Appendix (NPN1X and PNP1X). And the last one is again a third order Chebychev low-pass log-domain filter designed with same E-cells as in Appendix. But in this design, parasitic capacitances and later parasitic resistors are added.

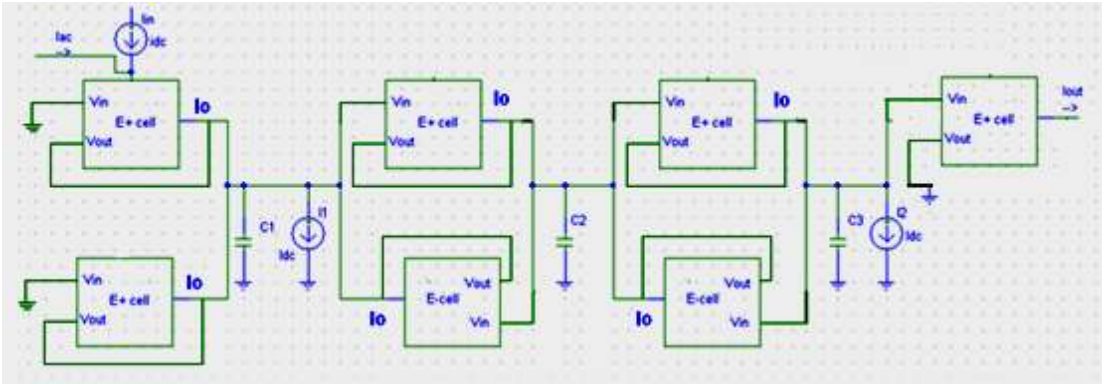


Figure 3.15 : Design of 3rd order Chebychev low-pass log-domain filter.

When designing filters by using E-cells, the prototype in Figure 3.15 is used. From the Figure 3.16 to 3.19, characteristic (1) shows the output current produced by third order Chebychev low-pass LC ladder circuit. Characteristic (2) shows the output

current designed with E-cells using model parameters shown in Appendix. Characteristic (3) shows the output current designed with E-cells using model parameters shown in Appendix and including parasitic capacitances. Parasitic capacitance values were subtracted from the values of capacitors placed in the filter.

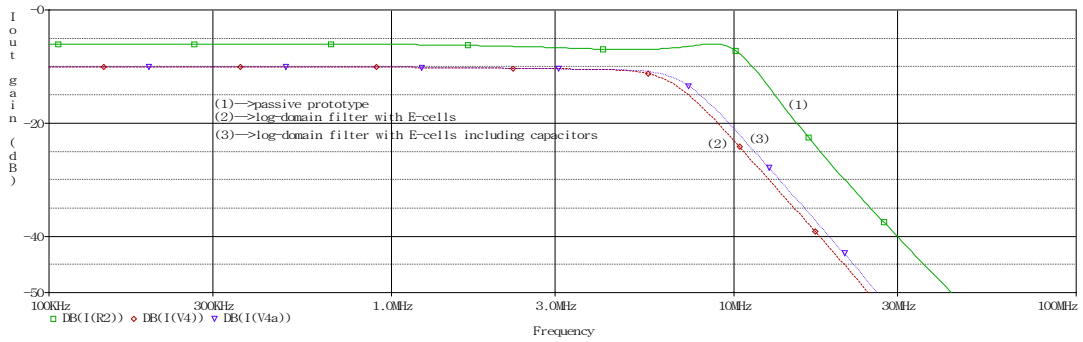


Figure 3.16 : Output currents using with E-cells in Figure 3.1a.

For the Figure 3.16, cut-off frequency of (1) is 10 MHz. Cut-off frequency for (2) is 6.69 MHz and for (3), it is 7.25 MHz. The capacitance values are set to 57.05 pF, 26.7 pF and 60 pF when including parasitic input and output capacitance values calculated before.

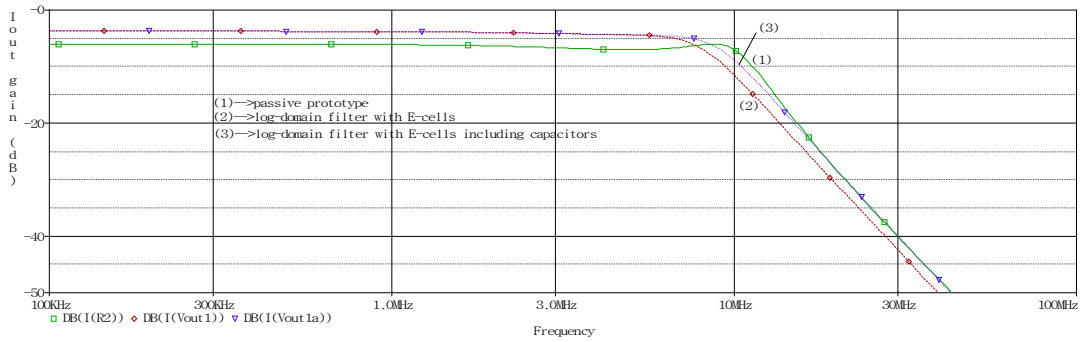


Figure 3.17 : Output currents using with E-cells in Figure 3.1b.

For the Figure 3.17, cut-off frequency of (1) is 10 MHz. Cut-off frequency for (2) is 7.97 MHz and for (3), it is 8.93 MHz. The capacitance values are set to 117 pF, 50 pF and 117 pF.

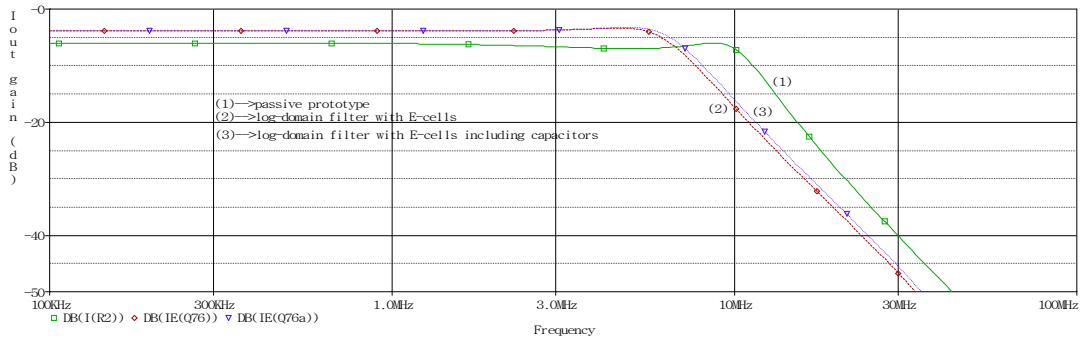


Figure 3.18 : Output currents using with E-cells in Figure 3.2a.

The capacitance values for the Figure 3.2a are 116 pF, 57 pF and 118 pF. The cut-off frequencies for the Figure 3.18 are 10 MHz for (1), 6.7 MHz for (2) and 7.2 MHz for (3).

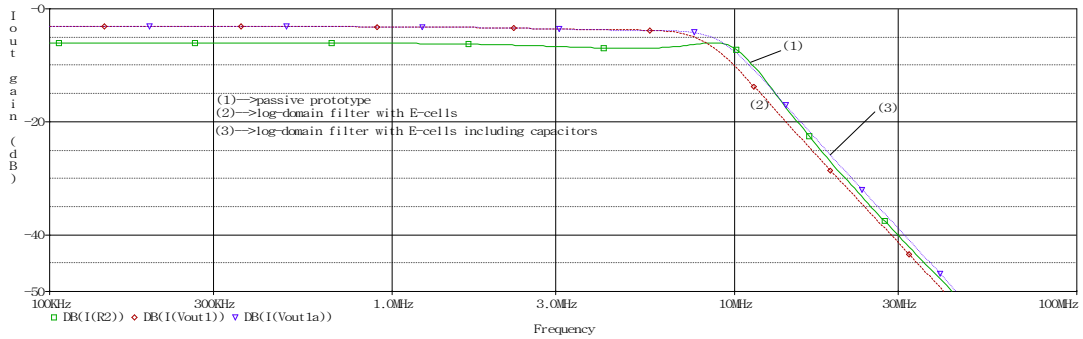


Figure 3.19 : Output currents using with E-cells in Figure 3.2c.

The capacitance values for the Figure 3.19 are 115.6 pF, 51.1 pF and 115.4 pF. The cut-off frequencies are 10 MHz for (1), 8.34 MHz for (2) and 9.3 MHz for (3).

The next step is to take account the effect of parasitic resistances to the filters. For this purpose, current sources in the filter should be multiplied with a constant value.

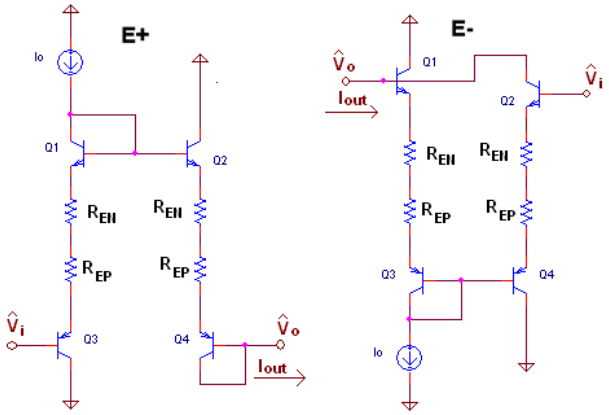


Figure 3.20 : E-cells with parasitic emitter resistors shown in Figure 3.1a.

For the E-cells in Figure 3.20,

$$V_i + (R_{EN} + R_{EP})(I_o - I_{out}) - 2V_T ln\left(\frac{I_{out}}{I_o}\right) - V_o = 0 \quad \textbf{(3.14)}$$

where R_{EN} is the emitter resistance for the NPN transistor and R_{EP} is the emitter resistance for the PNP transistor. By using Taylor series expansion, equation (3.14) can be rearranged by

$$V_i + (R_{EN} + R_{EP})(I_o - I_{out}) - 2V_T\left(\frac{I_{out}}{I_o} - 1\right) - V_o = 0 \quad \textbf{(3.15)}$$

and output current becomes

$$I_{out} = I_o\left[1 + \frac{V_i - V_o}{2V_T + (R_{EN} + R_{EP})I_o}\right] \quad \textbf{(3.16)}$$

Due to the companding nature of the log-domain circuits, the internal voltages are limited to a range of few V_T`s and thus the following approximation $V_i - V_o \ll 2V_T + (R_{EN} + R_{EP})I_o$ could be considered. Thus, equation (3.16) could be rewritten as follows [10]

$$I_{out} \approx I_o e^{\frac{V_i - V_o}{2V_T + (R_{EN} + R_{EP})I_o}} \quad \textbf{(3.17)}$$

By using LOG and EXP functions, exponential voltage at the output will be written as

$$EXP(V_o) = \left(\frac{2V_T}{2V_T + (R_{EN} + R_{EP})I_o}\right)\frac{I_o}{2V_T}\frac{1}{C}\int\{EXP(V_{ip}) - EXP(V_{in})\}dt \quad \textbf{(3.18)}$$

So, as a result, nonzero emitter resistance will introduce a scalar error and it will be defined as

$$k_{RE} = \frac{2V_T}{2V_T + I_o(R_{EN} + R_{EP})} \quad \textbf{(3.19)}$$

This value is used by multiplying the bias the current placed in the E-cells in Figure 3.1a. For the E-cells in Figure 3.1b, 3.2a and 3.2b, the multiplying factor of the bias current is

$$k_{RE} = \frac{V_T}{V_T + I_o(R_{EN} + R_{EP})} \quad \textbf{(3.20)}$$

k_{RE} parameter changes the time constant of the circuit and make cut-off frequency slide. The parasitic resistances were added after adding the parasitic capacitances to the filters. The value of R_E is assumed as $R_E = R_{EN} = R_{EP}$. And the value of R_E is

taken as 20 ohm which is defined in [2] and it is used for calculating the k_{RE} parameter . The output currents were simulated and outputs are shown in Figure 3.21 – 3.24. From these figures, characteristic (1) shows the output current produced by third order Chebychev low-pass LC ladder circuit. Characteristic (2) shows the output current designed with E-cells using model parameters shown in Appendix. Characteristic (3) shows the output current designed with E-cells using model parameters shown in Appendix and including parasitic capacitances and resistances.

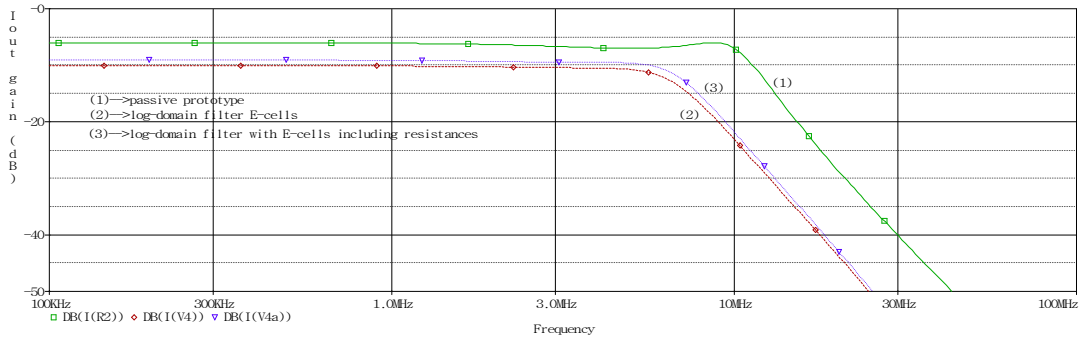


Figure 3.21 : Output currents using E-cells in Figure 3.1a including resistances.

All the bias currents in the filter designed with E-cells in Figure 3.1a were set to 92 µA. This value was calculated by using the equation in (4.17) and the values from Table 3.1. The new cut-off frequency for the characteristic (3) in Figure 3.21 is 6.89 MHz.

Another analysis is performed for the E-cell couple in Figure 3.1b, shown in Figure 3.22.

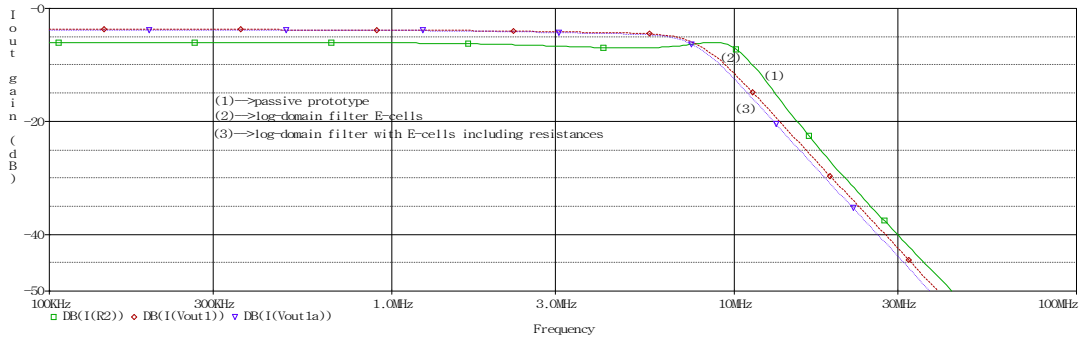


Figure 3.22 : Output currents using E-cells in Figure 3.1b including resistances.

The new cut-off frequency for the characteristic (3) in Figure 3.22 is 7.8 MHz. The bias currents for the filter are 86.6 µA. This filter is designed with E-cell in Figure 3.1b.

The cut-off frequency of Figure 3.23, including parasitic capacitances and resistances for the characteristic (3) is 6.22 MHz. The bias currents are 86.6 µA and 173.2 µA. This filter is designed with E-cell in Figure 3.2a.

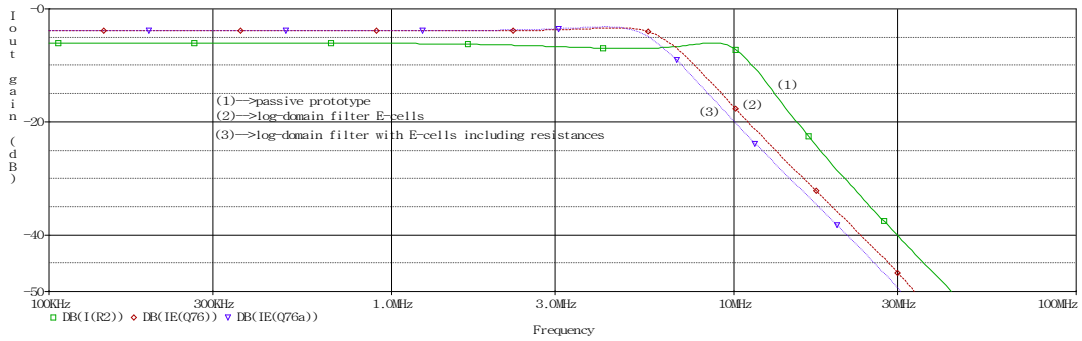


Figure 3.23 : Output currents using E-cells in Figure 3.2a including resistances.

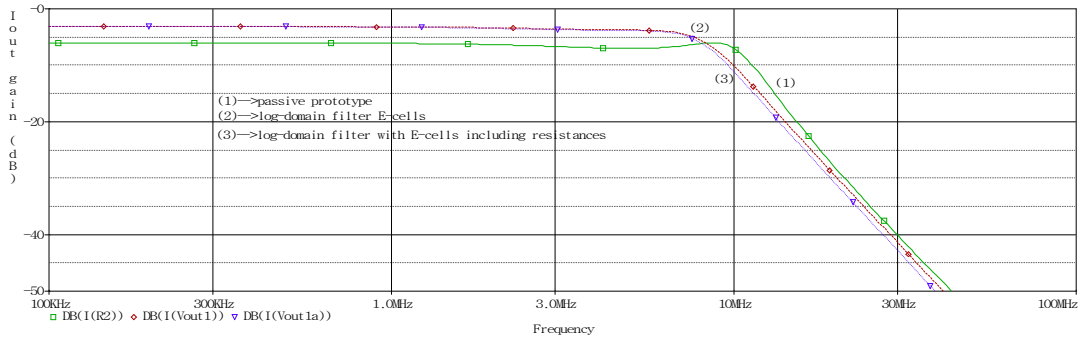


Figure 3.24 : Output currents using E-cells in Figure 3.2b including resistances.

For the characteristic (3) in Figure 3.24, the new cut-off frequency when all the parasitic effects are added is 8.06 MHz. The new bias current for the filters is taken as 86.6 µA. This filter is designed with the E-cell in Figure 3.2b.

As can be seen from the analysis, when effect of capacitors is added to the filters, a slight difference is seen at the cut-off frequencies when compared to the ideal case. The cut-off frequency of the filter, including capacitance values has better output characteristic than the filter designed with the E-cells with the default capacitance values. However, when adding the effects of resistances to the filters, by multiplying the bias current with a constant calculated before, the output currents differ from the ideal case and case where only capacitor effects are considered. The effect of resistances reduces the cut-off frequency. When the bias current is decreased, the cut-off frequencies of the filters decrease as well.

3.2.3 Sensitivity analysis of log-domain filters

In this section, sensitivity analysis of the log-domain filters are presented. For this purpose, first of all, capacitance and resistor values are varied with 15% tolerance in the filter simulated in Figure 3.14. The output current are shown in Figure 3.25.

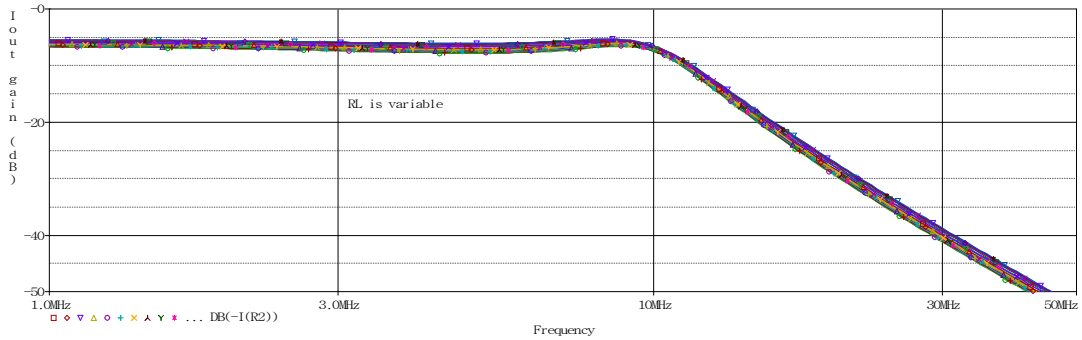


Figure 3.25 : The output current of filter with tolerance of R_L shown in Figure 3.14

For changing the capacitance value, C3, with a tolerance of 15%, the output current will be as shown in Figure 3.26.

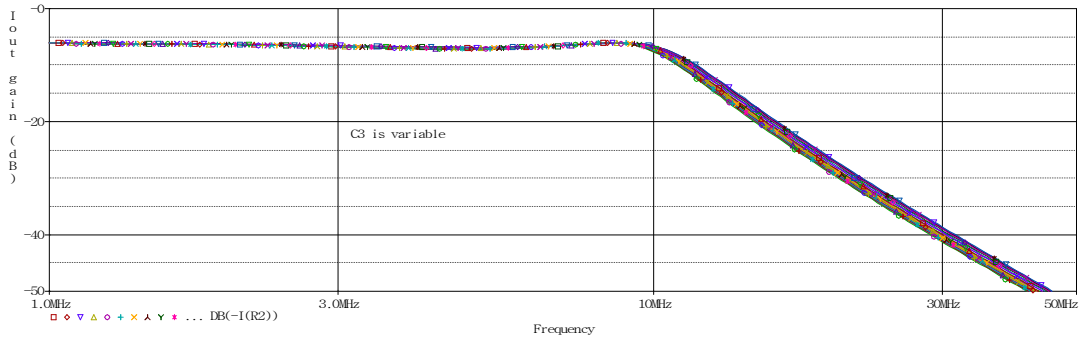


Figure 3.26 : The output current of filter with tolerance of C3 shown in Figure 3.14

Finally, changing the capacitance value, C1, with a tolerance of 15%, the output current will be as drawn in Figure 3.27.

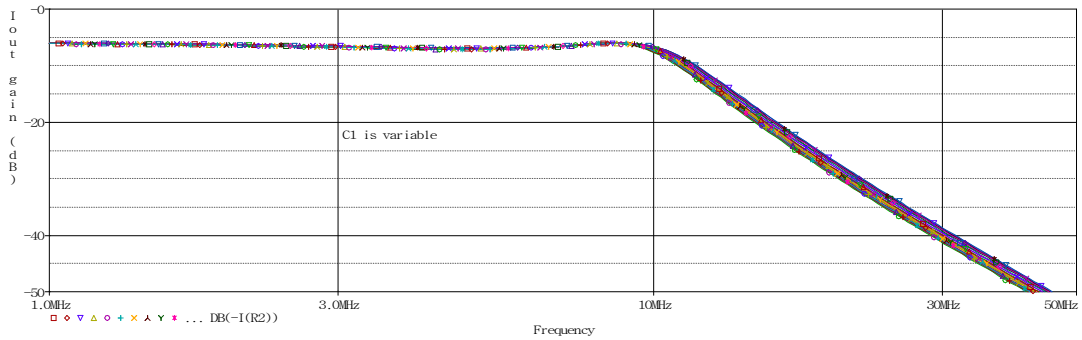


Figure 3.27 : The output current of filter with tolerance of C1 shown in Figure 3.14

As can be seen from the Figures 3.25 – 3.27, the cut-off frequency of LC ladder prototype is not sensible to the changes in the value of capacitors and resistors, employed in the filter. The changes of the sensitivity to C1 is clearly seen in the output of filter after and before the cut-off frequency.

The parameters are used again with 15% tolerance for the rest of the filters designed with E-cells which are shown in Figure 3.1 and 3.2. In here, the sensitivity analysis for the filter designed with E-cells shown in Figure 3.2a will be shown and compared. The capacitor value, C3 in Figure 3.15 is simulated with 15% tolerance and the output current will be as in the Figure 3.28.

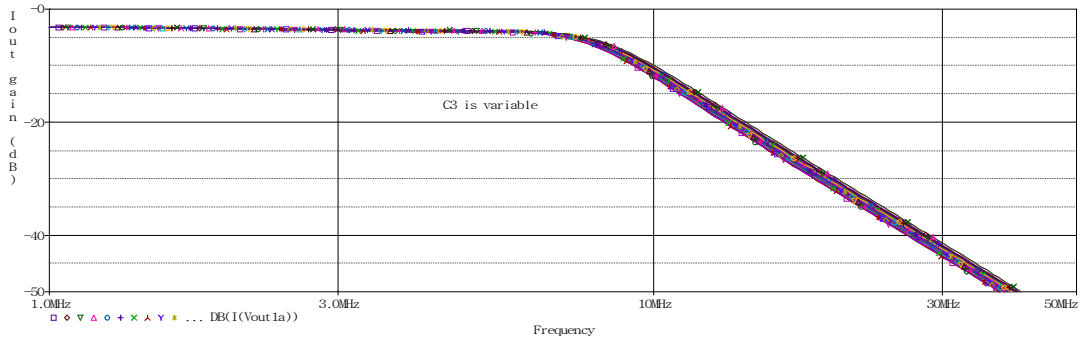


Figure 3.28 : The output current of filter with tolerance of C3 shown in Figure 3.15

The capacitor value, C2 in Figure 3.15 is simulated with 15% tolerance and the output current will be as in the Figure 3.29.

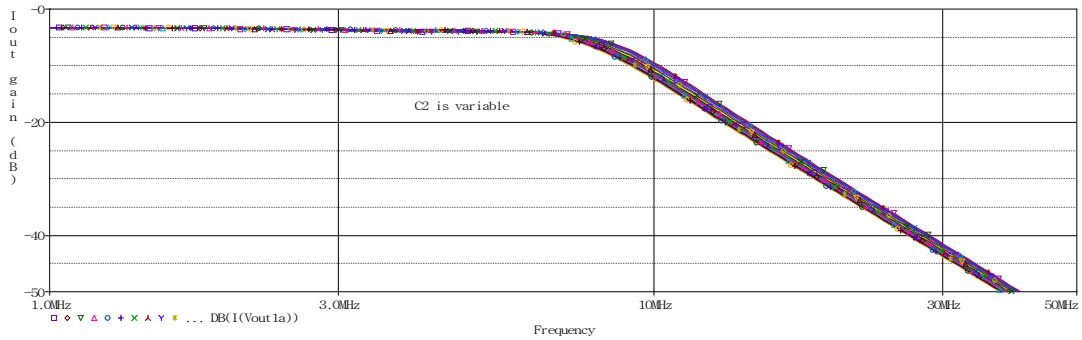


Figure 3.29 : The output current of filter with tolerance of C2 shown in Figure 3.15

Last sensitivity analysis was performed for the capacitor, C1 in Figure 3.15 and the result is shown in Figure 3.30.

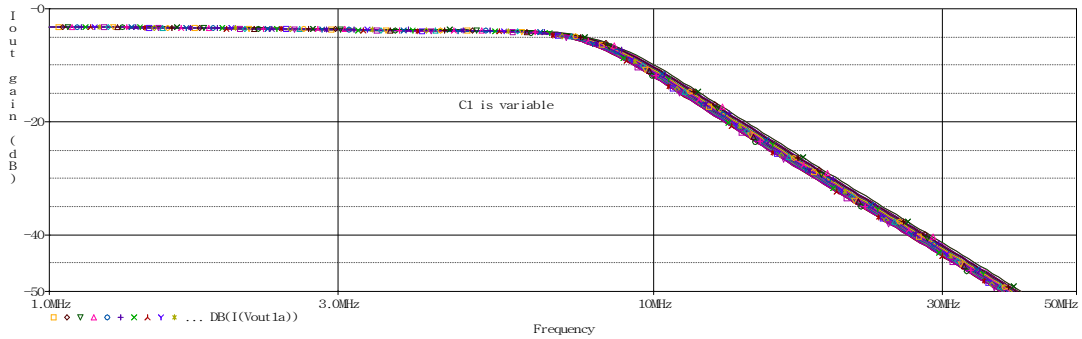


Figure 3.30 : The output current of filter with tolerance of C1 shown in Figure 3.15

As can be seen from the sensitivity analysis, the filters with LC ladder prototype and designed with E-cells which are including parasitic resistors and capacitors, the sensitivity to the resistors and capacitors are lower at the cut-off frequency ranges. But outside this area, the sensitivity to these parameters has larger effect on the filters. There are many changes on the output current when there is 15% tolerance. The sensitivity analysis are performed for the filters designed with another E-cell couples. Same results were extracted for these filters again.

4. CONCLUSION

Log-domain filters designed with E-cell blocks are analyzed for compensating the effects of beta and impedances and presented in this thesis. When the value of beta is set to infinite, the output current is close to the output current of E-cell designed with a finite beta value for a definite range. The output currents increases/ decreases linearly. But the output currents for the different Beta values differ and move away from each other outside these definite range. The two output currents still follow each other linearly but also diverge from each other.

The capacitance and resistance values have different effects on the cut-off frequency of the log-domain filters designed with E-cells. When, only capacitance values are added to the filters, or another word, capacitance values are subtracted from the capacitors placed in the filters, cut-off frequency of the filter is increased. But this change is very small. But if the effect of resistances is added to the filter by multiplying the bias currents with a constant, including the subtracted capacitance values, the cut-off frequencies are lower than the cut-off frequency including just subtracted capacitance values.

Also, the sensitivity analysis shows that, the filter designed with E-cells or LC ladder prototype, has low sensitivity during the cut-off frequency area. The tolerances of the elements with 15% make small oscillation at the cut-off frequency. But these oscillations are higher outside of the cut-off frequency range. So it can be said that these filters have low sensitivity to the tolerances of elements in the filter.

The new researches will be performed on the impedance values to get better output current and cut-off frequencies. E-cell couple shown in Figure 3.2b will be used for better outputs.

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APPENDIX

BJT Model Parameters Used in The Pspice Simulation Circuits

.MODEL NPN1X NPN RB=64 IRB=0 RBM=32 RC=144 RE=2.5 IS=1.523E-17 EG=1.206 XTI=2 XTB=2.363 +BF=80 IKF=7.540E-3 NF=1 VAF=90 ISE=5.976E-15 NE=1.999 BR=4 IKR=10E6 NR=1 VAR=3 ISC=2.336E-20 NC=1.653 TF=40P TR=381P CJE=2.601E-13 VJE=1.104 MJE=0.495 CJC=2.108E-13 +VJC=0.615 MJC=0.335 XCJC=0.1597 CJS=4.101E-13 VJS=0.500 MJS=0.318 FC=0.5

.MODEL PNP1X PNP RB=23 IRB=0 RBM=14 RC=93 RE=2.5 IS=1.034E-17 EG=1.206 XTI=1.5 XTB=2.053 +BF=80.6 IKF=6.602E-3 NF=1 VAF=43.0 ISE=8.009E-15 NE=1.557 BR=4 IKR=10E6 NR=1 VAR=1.4 +ISC=4.009E-16 NC=1.634 TF=65P TR=850P CJE=2.326E-13 VJE=0.8918 MJE=0.493 CJC=3.814E-13 VJC=0.530 MJC=0.190 XCJC=0.1597 CJS=8.672E-13 VJS=0.600 MJS=0.348 FC=0.5

CURRICULUM VITAE

Candidate's full name:	Burcu Yaldız
Place and date of birth:	Karşıyaka/ İzmir – 12/ 04/ 1985
Permanent Address:	Sahrayıcedit Mah. Atatürk Cad. Hafız İmam Sok. Akyüz Apt. No: 1 D: 14 34734 Kadıköy/ İstanbul
Universities and Colleges attended:	Istanbul Technical University
	Kadir Has University