ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

DESIGN OF AN INVERTER-BASED VARIABLE GAIN AMPLIFIER FOR PAM-4 OPTICAL RECEIVERS

M.Sc. THESIS

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Department of Electronics and Communication Engineering

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PAM-4 OPTİK ALICILAR İÇİN EVİRİCİ TABANLI KAZANCI AYARLANABİLEN KUVVETLENDİRİCİ TASARIMI

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To all children,

FOREWORD

All praise is due to Allah, the Most Merciful and Compassionate, who created us, made us aware of His existence, and endowed us with countless blessings and knowledge. My success is solely with Allah's permission.

I would like to sincerely thank my advisor, Assoc. Prof. Dr. Mustafa Berke Yelten, for the guidance, support, and unique perspectives he provided me throughout my courses and thesis.

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TABLE OF CONTENTS **Page**

FOREWORD ..... **ix**
TABLE OF CONTENTS ..... **xi**
ABBREVIATIONS ..... **xiii**
SYMBOLS ..... **xv**
LIST OF TABLES ..... **xvii**
LIST OF FIGURES ..... **xx**
SUMMARY ..... **xxi**
ÖZET ..... **xxv**
1. INTRODUCTION **1**
1.1 Purpose of Thesis 3
1.2 Literature Review 4
1.3 Thesis Organisation 7
2. LINEARITY **9**
2.1 Definition of Linearity 11
2.2 Linearity Improvement Methods 12
2.2.1 Degeneration 13
2.2.2 Feedback 13
2.2.3 Predistortion 15
2.2.4 Triode devices 15
2.2.5 g_m / g_m method 15
2.3 Linearity Simulation Methods 17
3. INVERTER-BASED VGA **23**
3.1 Unit Cell 23
3.2 Proposed VGA 25
3.3 PVT Insensitive Biasing of VGA 27
4. SIMULATION RESULTS **31**
4.1 Layout 31
4.2 Testbench 32
4.3 DC Results 33
4.4 Frequency Response Results 37
4.5 Transient Results 39
4.6 Distortion and Eye Diagram Results 40
4.7 Noise Results 43
4.8 Worst-Case Corner Performance Summary 43
5. CONCLUSIONS **45**
REFERENCES **47**
CURRICULUM VITAE **53**

ABBREVIATIONS

AC : Alternating Current
AGC : Automatic Gain Control
B2T : Binary-to-Thermometer
BER : Bit Error Rate
CMOS : Complementary Metal Oxide Semiconductor
CTLE : Continuous-Time Linear Equalizer
DC : Direct Current
FF : Fast-Fast
FS : Fast-Slow
Gbps : Gigabit per second
HD : Harmonic Distortion
IIP3 : Input Third-Order Intercept
IP3 : Third-Order Intercept
IRN : Input-Referred Noise
ISI : Intersymbol Interference
LDO : Low-Dropout Regulator
MOSFET : Metal Oxide Semiconductor Field-Effect Transistor
NF : Noise Figure
NMOS : N-type Metal Oxide Semiconductor
NRZ : Non-Return-to-Zero
OIP3 : Output Third-Order Intercept
OPAMP : Operational Amplifier
OTA : Operational Transconductance Amplifier
PAM : Pulse Amplitude Modulation
PGA : Programmable Gain Amplifier
PMOS : P-type Metal Oxide Semiconductor
PVT : Process, Voltage, and Temperature
RFIC : Radio Frequency Integrated Circuit
RLM : Transmitter Linearity
SF : Slow-Fast
SNR : Signal-to-Noise Ratio
SS : Slow-Slow
THD : Total Harmonic Distortion
TIA : Transimpedance Amplifier
VGA : Variable Gain Amplifier
VTC : Voltage Transfer Characteristic

SYMBOLS

C	**:** Capacitance
C_{ox}	**:** Oxide Capacitance
g_m	**:** Transconductance
g_{ds}	**:** MOSFET Output Conductance
I_D	**:** Drain Current
L	**:** Channel Length
R_{off}	**:** MOSFET Switch OFF Resistance
R_{on}	**:** MOSFET Switch ON Resistance
r_{ds}	**:** MOSFET Output Resistance
V_T	**:** Threshold Voltage
W	**:** Channel Width
μ_n	**:** Electron Mobility
λ	**:** Channel Length Modulation

LIST OF TABLES

Page

Table 4.1 : Power consumption across various PVT conditions..... **34**
Table 4.2 : Performance summary at the worst corners..... **44**
Table 5.1 : Comparison of the proposed VGA with existing literature **46**

LIST OF FIGURES

Page

Figure 1.1 : Example of the symbols for NRZ and PAM-4 using the same data pattern [1]. **2**
Figure 1.2 : Optical receiver front end and the scope of this thesis. **3**
Figure 1.3 : Example characteristics of an analog-controlled VGA vs. a digitally-controlled VGA [2]. **5**
Figure 2.1 : Simple small signal model of n-channel MOSFET. **10**
Figure 2.2 : (a) MOSFET as a switch, (b) its ON model, and (c) its OFF model. **11**
Figure 2.3 : (a) block diagram of the ideal voltage amplifier and (b) its input-output characteristic. **12**
Figure 2.4 : Resistive-loaded common source amplifier with source degeneration. **13**
Figure 2.5 : Block diagram of an amplifier with feedback. **14**
Figure 2.6 : Transfer characteristics of an amplifier with and without feedback. . **14**
Figure 2.7 : Conceptual representation of the predistortion technique. **15**
Figure 2.8 : Inverter transconductor schematic. **16**
Figure 2.9 : Block diagram of simple g_m/g_m amplifier **16**
Figure 2.10 : Deviation from ideal characteristic. **17**
Figure 2.11 : Gain versus input voltage. **18**
Figure 2.12 : Frequency spectrum of an amplifier output including third order products [3]. **19**
Figure 2.13 : IIP_3 and OIP_3 on *Pout* vs. *Pin* plot [4]. **20**
Figure 2.14 : Formation of NRZ eye diagram [5]. **20**
Figure 2.15 : (a) Example of ideal and (b) non-ideal PAM-4 eye diagrams [6]. ... **21**
Figure 3.1 : (a) Inverter g_m unit cell and (b) g_m cell as load. **24**
Figure 3.2 : Simple voltage amplifier using unit cells. **24**
Figure 3.3 : Conceptual schematic representation of the proposed VGA. **26**
Figure 3.4 : Schematic diagram of the proposed VGA. **26**
Figure 3.5 : Block level schematic of the replica biasing circuit. **28**
Figure 3.6 : Transistor-level schematic of the replica biasing. **29**
Figure 4.1 : Layout of (a) $1X$, (b) $1.5X$, and (c) $2X$ cells. **32**
Figure 4.2 : Layout of the proposed VGA. **32**
Figure 4.3 : Testbench for simulations. **33**
Figure 4.4 : Normalized gain vs. the input voltage under worst PVT conditions with/without replica bias. **34**
Figure 4.5 : Gain vs. gain code with best-fit curve and gain error. **35**
Figure 4.6 : Gain vs. gain code over corners. **35**
Figure 4.7 : DC voltage transfer characteristics for different gain codes. **36**
Figure 4.8 : DC voltage transfer characteristics for different gain codes across corners. **36**

Figure 4.9 : Frequency response as a function of gain code. **37**
Figure 4.10 : Frequency response as a function of gain code over corners. **37**
Figure 4.11 : Bandwidth as a function of gain code over corners. **38**
Figure 4.12 : Stability analysis of LDO loop across corners at maximum and minimum gain settings. **38**
Figure 4.13 : Transient response of 1 GHz sinusoidal input at minimum VGA gain for various amplitudes. **39**
Figure 4.14 : Transient response of 1 GHz sinusoidal input at maximum VGA gain for various amplitudes. **39**
Figure 4.15 : Peak-to-peak output voltage vs. peak-to-peak input voltage for 1 GHz sinusoidal input. **40**
Figure 4.16 : HD3 and THD over input amplitudes. **40**
Figure 4.17 : NRZ eye diagram for 1 Gbps input at maximum gain setting. **41**
Figure 4.18 : NRZ eye diagram for 5 Gbps input at maximum gain setting. **41**
Figure 4.19 : NRZ eye diagram for 10 Gbps input at maximum gain setting. **42**
Figure 4.20 : PAM-4 eye diagram for 1 Gbps input at maximum gain setting. **42**
Figure 4.21 : PAM-4 eye diagram for 5 Gbps input at maximum gain setting. **42**
Figure 4.22 : PAM-4 eye diagram for 10 Gbps input at maximum gain setting. . . . **43**
Figure 4.23 : Input-referred noise at maximum and minimum gain settings over corners. **43**
Figure 4.24 : Noise figure at maximum and minimum gain settings over corners. . **44**

DESIGN OF AN INVERTER-BASED VARIABLE GAIN AMPLIFIER FOR PAM-4 OPTICAL RECEIVERS

SUMMARY

Optical communication is a widely adopted and highly efficient technology that plays a crucial role in various fields and industries, encompassing a broad range of applications, from telecommunications to data centers, and its usage continues to grow rapidly as demand for faster and more reliable communication increases. Although two-level Pulse Amplitude Modulation (PAM-2), also known as Non-Return-to-Zero (NRZ), is the traditional and most widely used PAM technique in optical systems, there has been a growing trend toward adopting higher-level PAM modulations, such as PAM-4. This shift is driven by higher-level PAM's ability to transmit more bits per symbol, allowing for significantly higher data rates. This increased efficiency facilitates faster data transmission without requiring additional bandwidth, making it a more efficient approach for modern communication systems that demand higher performance. One of the most widely used higher-level PAM modulation techniques is PAM-4, which utilizes four distinct levels, with 2 bits being represented per level. Thus, PAM-4 significantly enhances the efficiency of data transmission by encoding more information in each symbol. This allows the effective data rate to become twice that of NRZ for the same bandwidth, providing a substantial improvement.

Besides the advantages of multi-level PAM over NRZ, it also has some challenges, such as stricter linearity requirements and reduced noise immunity. As the amplitude levels increase in higher-order PAM modulations compared to NRZ, the linearity requirements for the circuits and systems become more stringent. These challenges must be carefully considered to ensure optimal performance and reliability when designing circuits and systems that implement multi-level PAM modulation.

To meet these requirements, it is essential to design circuits with high linearity to prevent signal distortion and ensure accurate data transmission. Achieving this level of linearity is a challenging task that requires careful consideration of various design techniques, as well as an evaluation of the trade-offs between performance, complexity, and cost.

This thesis presents the design of a high-linearity, digitally controlled Variable Gain Amplifier (VGA) for PAM-4 optical receivers, realized using a 65 nm CMOS process and operating with a supply voltage of 1.8 V. The study investigates a variety of linearity improvement methods, such as degeneration, feedback, predistortion, the use of triode devices, and the inverter-based g_m/g_m method. The inverter-based g_m/g_m technique is selected for its outstanding performance in terms of linearity and other key parameters, such as bandwidth, noise, and compactness. This technique effectively handles the stringent linearity requirements imposed by PAM-4 modulation, thereby ensuring efficient and reliable signal transmission in high-speed optical systems.

The inverter-based g_m/g_m technique is examined in detail, where the unit cell structure is created by incorporating switches into the inverter, allowing the cells to be enabled or disabled. Analyses of the pole, zero, and gain of the simplest g_m/g_m amplifier are conducted. Following these analyses, the concept of the VGA is developed through several iterations of simulations. The VGA concept consists of three main components, each containing parallel cells: First, the controlled input cells, which adjust the gain using gain control bits. The second part includes the always-on g_m cells, which set the minimum gain, with more cells providing higher initial gain. The third part consists of load cells, which are always active and adjust the gain step. The number of load cells determines the step size, fewer load cells lead to larger gain steps, while more load cells result in smaller steps. The VGA uses a 15-bit thermometric code to provide precise, fine-grained control over the gain settings. The proposed VGA is implemented in a pseudo-differential structure to take advantage of improved noise immunity and a higher signal swing. To reduce gain compression caused by the output resistances of the cells as the gain code increases, and to maintain minimal gain error across all codes, larger unit cells are employed as the gain code rises. For this, the first 6 bits control 1X unit cells, the next 4 bits control 1.5X unit cells, and the final 5 bits control 2X unit cells. This adaptive cell size approach helps to preserve the overall performance of the amplifier, even as the gain settings are adjusted. Additionally, the number of load cells remains constant regardless of the gain code, ensuring that the load capacitance stays consistent. This consistency is vital for maintaining uniform bandwidth across different gain codes, as the dominant pole that determines the bandwidth originates from the output node where the load cells are connected.

Inverter-based circuits are highly sensitive to variations in process, voltage, and temperature (PVT). To mitigate this sensitivity, the replica biasing method can be employed. There are various ways to implement the replica biasing method. The approach used in this study involves a reference diode-connected 1X cell, known as the replica. This replica remains continuously on. A constant reference current, I_{ref} of 30 μA, flows through the replica cell, generating a reference voltage, V_{ref}, that is proportional to I_{ref}. The resulting V_{ref} voltage is the sum of the V_{GS} and V_{SG} voltage drops across the NMOS and PMOS devices within the reference cell. This V_{ref} is then used as the reference input for a low-dropout regulator (LDO), which copies the reference voltage to its output. This output voltage also serves as the supply for the VGA. The reference voltage tracks PVT variations, allowing the VGA supply to adapt automatically and maintain a stable bias current under changing conditions. For example, if the threshold voltages of devices decrease in a particular PVT case, the gate-source voltages, V_{GS}, also decrease to maintain the same I_{ref} current, causing V_{ref} to decrease and, consequently, reducing the VGA supply. For the LDO, the indirect Miller-compensation technique is employed, utilizing a compensation capacitor of 500 fF. A critical consideration is that LDO pass devices must be appropriately sized to supply the maximum current required by the VGA core. If the pass devices are not properly sized, the replica biasing circuit may not function as intended. This replica biasing technique ensures robust performance for the VGA under varying PVT conditions, facilitating reliable operation. The usage of replica biasing provides a PVT-robust operation of the VGA across various conditions, as evidenced by the simulation results.

After the schematic-level design of the VGA is completed, the layout is developed by first creating the individual layouts of the unit cells, then combining them and performing the necessary routing to form the overall VGA layout. The layouts of the 1X, 1.5X, and 2X cells share the same structure, with the only difference being their horizontal sizes. The overall layout of the VGA is highly compact, with dimensions of only 66 μm $\times$ 25 μm.

Post-layout simulations have been carried out under various PVT conditions, taking into account the effects of process variations, supply voltage fluctuations, and temperature changes. These simulations demonstrate the design's high performance across various aspects, including DC characteristics, frequency response, transient behavior, and linearity. Under typical operating conditions, the simulations show that the VGA provides a 7.5 dB gain range with 0.5 dB increments, minimal gain error within $\pm$ 0.15 dB, and a consistent 5.2 GHz bandwidth across all gain settings. For linearity evaluation, a sinusoidal signal at 1 GHz with varying input amplitudes was applied. At a 100 mV input amplitude, the third-order harmonic distortion (HD3) remained below -50 dB, while the total harmonic distortion (THD) stayed under 0.3% across all gain settings. When the input amplitude was increased to 200 mV, HD3 was under -44 dB, and THD remained below 2% for all gain settings. The eye diagrams displayed a wide and high shape, confirming strong performance in terms of intersymbol interference (ISI) and linearity. Additionally, the VGA demonstrated low noise levels, with an input-referred noise (IRN) of 1.26 nV at maximum gain and 2.3 nV at minimum gain at 1 GHz. The average noise figure (NF) was found to be 4.75 dB at maximum gain and 8.83 dB at minimum gain, further showcasing the low-noise performance across the entire gain range.

In conclusion, an inverter-based VGA has been designed for PAM-4 optical receivers. To enhance PVT robustness, the replica biasing method is employed. The proposed VGA offers precise gain control, constant bandwidth, high linearity, high swing, and low noise performance. Its versatility makes it suitable not only for optical communication systems but also for a wide range of other applications.

PAM-4 OPTİK ALICILAR İÇİN EVİRİCİ TABANLI KAZANCI AYARLANABİLEN KUVVETLENDİRİCİ TASARIMI

ÖZET

Optik haberleşme, çeşitli alanlar ve endüstrilerde kritik bir rol oynayan ve hızlı bir şekilde büyüyen, geniş çapta kabul görmüş ve son derece verimli bir teknolojidir. Optik haberleşme telekomünikasyondan veri merkezlerine kadar geniş bir uygulama yelpazesinde kullanılmakta ve daha hızlı ve güvenilir iletişim talepleri arttıkça kullanım oranı hızla artmaktadır. Sıfıra Dönüşsüz (NRZ) olarak da bilinen iki seviyeli Darbe Genlik Modülasyonu (PAM-2) optik sistemlerde geleneksel ve en yaygın kullanılan PAM tekniği olmasına rağmen, PAM-4 gibi daha yüksek seviyeli modülasyonlara doğru eğilim artmaktadır. Bu değişim, daha yüksek seviyeli PAM modülasyonunda sembol başına daha fazla bit iletme kapasitesine sahip olmasından kaynaklanmaktadır, bu da önemli ölçüde daha yüksek veri hızlarına olanak tanır. Bu artan verimlilik, ek bant genişliği gereksinimi olmadan daha hızlı veri iletimini mümkün kılarak, daha yüksek performans gerektiren modern iletişim sistemleri için daha verimli bir yaklaşım sunar. En yaygın kullanılan yüksek seviyeli PAM modülasyon tekniklerinden biri olan PAM-4, dört farklı seviye kullanır ve seviye başına 2 bit iletme kapasitesine sahiptir. Sonuç olarak, PAM-4 her sembolde daha fazla bilgi kodlayarak veri iletim verimliliğini önemli ölçüde artırır. PAM-4 aynı bant genişliği için NRZ'nin iki katı kadar yüksek bir etkin veri hızı sağlar ve büyük bir iyileşme sağlar.

Ancak, NRZ ile karşılaştırıldığında daha yüksek seviyeli PAM modülasyonlarında genlik seviyeleri arttıkça, devreler ve sistemler için doğrusallık gereksinimlerinin daha sıkı hale gelmesi ve gürültü bağışıklığının azalması gibi bazı zorluklar vardır. Çok seviyeli PAM modülasyonunu uygulayan devreler ve sistemler tasarlanırken, optimal performans ve güvenilirliği sağlamak için bu zorluklar dikkatlice değerlendirilmelidir.

Bu zorlu gereksinimleri karşılamak için, işaret bozulmalarını önlemek ve doğru veri iletimini sağlamak adına yüksek doğrusallık sağlayan devreler tasarlamak önemlidir. Bu doğrusallık seviyesini elde etmek, çeşitli tasarım tekniklerini dikkatle düşünmeyi ve performans, karmaşıklık ve maliyet arasındaki dengeyi değerlendirmeyi gerektirir.

Bu tezde, PAM-4 optik alıcıları için yüksek doğrusallıklı, dijital kontrollü bir Değişken Kazançlı Kuvvetlendirici (VGA) tasarımı sunulmaktadır. Tasarım, 65 nm CMOS teknolojisi kullanılarak yapılmış ve 1.8 V besleme gerilimi ile çalışmaktadır. Çalışmada, bazı temel doğrusallık iyileştirme yöntemleri incelenmiştir. Bu yöntemler arasında dejenerasyon, geri besleme, predistorsiyon, triyot cihazlarının kullanımı ve evirici tabanlı g_m/g_m tekniği yer almaktadır. Evirici tabanlı g_m/g_m tekniği, doğrusallığın yanısıra, bant genişliği, gürültü ve kompaktlık gibi diğer önemli parametreler açısından üstün performans sağladığından dolayı seçilmiştir. Bu teknik,

PAM-4 modülasyonu için lazım olan yüksek doğrusallık gereksinimlerini etkili bir şekilde karşılamakta olup, yüksek hızlı optik sistemlerde verimli ve güvenilir işaret iletimi sağlamaktadır.

Evirici tabanlı g_m/g_m tekniği, eviriciye anahtarlar eklenerek hücrelerin açılıp kapanması sağlanmış ve ayrıntılı olarak incelenmiştir. En basit g_m/g_m kuvvetlendiricisinin kutup, sıfır ve kazanç analizleri yapılmıştır. Yapılan bu analizler ve simülasyon iterasyonları sonucu bir VGA konsepti geliştirilmiştir. Oluşturulan VGA konsepti, her biri paralel hücreler içeren üç ana bileşenden oluşmaktadır. İlk bileşen, kazancı kontrol bitleriyle ayarlayan kontrollü giriş hücreleridir. İkinci bileşen, minimum kazancı belirleyen ve her zaman açık durumda olan g_m hücreleridir. Daha fazla g_m hücre sayısı yüksek taban kazancı sağlarken, g_m hücrelerinin sayısının azalması minimum kazancı azaltmaktadır. Üçüncü olarak her zaman aktif olan yük hücreleri bulunmaktadır. Bunlar da kazanç adımının boyutunu belirler. Daha az yük hücresi, daha büyük kazanç adımları sağlarken, yük hücresi sayısı artınca daha küçük adımlar elde edilir. VGA, kazanç ayarlarını hassas ve ince bir şekilde kontrol etmek için 15 bitlik termometrik kod kullanmaktadır. Önerilen VGA, daha yüksek işaret salınımı ve gelişmiş gürültü bağışıklığı sağlamak için sözde-farksal bir yapıda gerçekleştirilmiştir. Kazanç kodu arttıkça hücrelerin çıkış dirençlerinden kaynaklanan kazanç sıkışmasını azaltmak ve tüm kodlar boyunca minimal kazanç hatası sağlamak için daha büyük birim hücreler kullanılmıştır. Bunun için, ilk 6 bit 1X birim hücrelerini kontrol etmek için kullanılmakta, sonraki 4 bit 1.5X birim hücrelerini kontrol etmekte ve son 5 bit ise 2X birim hücrelerini kontrol etmektedir. Bu adaptif hücre boyutu yaklaşımı, kazanç kodunun değişmesiyle kuvvetlendiricinin genel performansını korumaya yardımcı olmaktadır. Ayrıca, yük hücrelerinin sayısı, kazanç koduna bağlı olmaksızın sabit tutulmuştur, bu da çıkış düğümündeki kapasitörün farklı kazanç kodlarında yaklaşık sabit kalmasını sağlamaktadır. Bu durum, bant genişliğinin sabit kalması için önemlidir, çünkü bant genişliğini belirleyen baskın kutup, yük hücrelerinin bağlandığı çıkış düğümünden gelmektedir.

Evirici tabanlı devreler, süreç, voltaj ve sıcaklık (PVT) varyasyonlarına karşı oldukça hassastır. Bu hassasiyeti azaltmak için replika kutuplama yöntemi kullanılabilir. Replika kutuplama yönteminin çeşitli uygulama şekilleri mevcuttur. Bu çalışmada kullanılan yaklaşım, şöyle açıklanabilir: Her zaman açık olan ve referans olarak kullanılan diyot bağlı 1X hücre vardır. 30 μA'lik sabit bir referans akımı, I_{ref}, replika hücresinden geçer ve bu, I_{ref}'e orantılı bir referans gerilimi olan V_{ref}'i oluşturur. Oluşan V_{ref} gerilimi, referans hücresindeki NMOS ve PMOS cihazları üzerindeki V_{GS} ve V_{SG} gerilim düşüşlerinin toplamıdır. Bu V_{ref}, düşük-kayıplı düzenleyici (LDO) için referans giriş olarak kullanılır. LDO, referans gerilimini döngüsü sayesinde çıkışına kopyalar. Bu çıkış gerilimi, aynı zamanda VGA için besleme gerilimi olarak kullanılır. Referans gerilimi PVT varyasyonlarını takip eder ve VGA beslemesi, değişen koşullara göre otomatik olarak uyum sağlar ve sabit bir kutuplama akımı sağlar. Örneğin, cihazların eşik gerilimleri belirli bir PVT durumunda azalırsa, aynı I_{ref} akımını korumak için V_{GS}'ler de azalır, bu da V_{ref} geriliminin düşmesine ve dolayısıyla VGA'nın besleme geriliminin azalmasına yol açar. LDO için, dolaylı Miller kompanzasyonu tekniği ve 500 fF'lik bir kompanzasyon kapasitörü kullanılmıştır. LDO geçiş cihazlarının, ana VGA devresi tarafından gereken maksimum akımı sağlamak için uygun şekilde boyutlandırılması gerektiği kritik bir

hususdur. Eğer geçiş cihazları doğru şekilde boyutlandırılmazsa, replika kutuplama devresi beklenen şekilde çalışmayabilir. Bu replika kutuplama tekniği, değişen PVT koşulları altında VGA için sağlam performans sağlar ve güvenilir çalışma sağlar. Simülasyon sonuçlarıyla kanıtlandığı üzere, replika kutuplama tekniğinin kullanılması VGA'nın PVT değişimlerine dirençli olmasını sağlamaktadır.

VGA'nın şematik düzeydeki tasarımı tamamlandıktan sonra, birim hücrelerin ayrı ayrı serimleri oluşturulup, bunlar birleştirilmiş ve üst düzeydeki gerekli bağlantılar da yapılarak VGA serimi tamamlanmıştır. 1X, 1.5X ve 2X hücrelerinin serimleri aynı yapıyı paylaşmakta olup, tek fark yatay boyutlarıdır. VGA'nın genel serimi oldukça kompakt olup, yalnızca 66 μm $\times$ 25 μm boyutlarındadır.

Serim sonrası simülasyonlar, süreç varyasyonları, besleme gerilimi dalgalanmaları ve sıcaklık değişikliklerinin etkileri dikkate alınarak çeşitli PVT koşulları altında gerçekleştirilmiştir. Bu simülasyonlar, tasarımın DC özellikleri, frekans yanıtı, zamana bağlı davranışı ve doğrusallık gibi çeşitli yönlerden yüksek performans sergilediğini göstermektedir. Tipik çalışma koşulları altında, simülasyonlar, VGA'nın 0.5 dB adımlarla 7.5 dB kazanç aralığı sunduğunu, kazanç hatasının çok az ve $\pm$ 0.15 dB içinde olduğunu ve tüm kazanç ayarlarında 5.2 GHz bant genişliği sağladığını göstermektedir. Doğrusallık testi için, girişe 1 GHz frekansında çeşitli genliklere sahip bir sinüzoidal işaret uygulanmıştır. 100 mV'luk giriş genliği için, üçüncü dereceden harmonik bozulma (HD3) değeri tüm kazanç ayarlarında -50 dB'nin altında kalmış, toplam harmonik bozulma (THD) ise %0.3'ün altında kalmıştır. Giriş genliği 200 mV'a çıkarıldığında, HD3 tüm kazanç ayarlarında -44 dB'nin altında kalmış ve THD %2'nin altında kalmıştır. Göz diyagramları geniş ve yüksek olup, semboller arası girişim (ISI) ve doğrusallık açısından yüksek performansı doğrulamaktadır. Ayrıca, VGA tüm kazanç aralığında düşük gürültü performansını sergilemiştir. 1 GHz'de, maksimum kazançta 1.26 nV, minimum kazançta ise 2.3 nV girişe göre hesaplanmış gürültü değeri (IRN) sergilemektedir. Ortalama gürültü katsayısı (NF), maksimum kazançta 4.75 dB ve minimum kazançta 8.83 dB olarak bulunmuş.

Sonuç olarak, PAM-4 optik alıcıları için evirici tabanlı bir VGA tasarlanmıştır. PVT dayanıklılığını artırmak için replika kutuplama yöntemi kullanılmıştır. Önerilen VGA, hassas kazanç kontrolü, sabit bant genişliği, yüksek doğrusallık, yüksek salınım ve düşük gürültü performansı sunmaktadır. Bu performans, VGA'yı yalnızca optik iletişim sistemleri için değil, aynı zamanda çok sayıda diğer uygulama için de uygun hale getirmektedir.

1. INTRODUCTION

Optical communication has become a cornerstone of modern telecommunications, enabling high-speed data transmission over long distances. It has gained increasing attention over the years due to significant advantages such as immunity to electromagnetic interference, long-distance transmission, efficient high-frequency performance, secure communication, and lower attenuation. With the exponential growth of internet traffic and the increasing demand for bandwidth, optical fibers provide an efficient solution, allowing for higher data rates than traditional electrical transmission methods. The ability to transmit vast amounts of information quickly and reliably makes optical communication essential for telecommunications and applications in the healthcare, automotive, and space sectors.

Optical communication systems frequently utilize Pulse Amplitude Modulation (PAM) for data transmission. The most recognized and straightforward type of PAM is Non-Return-to-Zero (NRZ), also referred to as PAM-2, which employs only two amplitude levels. With the increasing demand for higher data rates, there is a notable trend toward higher-level PAM modulations, such as PAM-4, which has become one of the most popular choices. This shift is driven by the fact that as the number of levels (X) in the PAM modulation increases, the amount of information transmitted per symbol also increases, thereby enhancing the data rate without requiring additional bandwidth. The number of bits per symbol (b) in a PAM system is determined by the number of amplitude levels (X) and is given by

$$b = \log_2(X) \tag{1.1}$$

Higher-level PAM modulations transmit more information per symbol cycle than lower-level schemes like NRZ. Consequently, when operating at the same bit rate, higher-level PAM systems feature a baud rate (or symbol rate) lower than that of NRZ. Reducing the baud rate helps mitigate signal loss in the transmission channel,

allowing existing channels to support higher bit rates without increasing the baud rate, thereby minimizing channel loss. This is another important reason for the use of higher-order PAM modulation. The relationship between data rate and baud rate in PAM modulation, depending on the modulation level (X), can be generalized as in (1.2).

$$\text{Data Rate} = \text{Baud Rate} \times \log_2(X) \tag{1.2}$$

Although multi-PAM modulation offers the abovementioned advantages, higher modulation levels can reduce immunity to noise and jitter [7]. For example, the eye swing of a PAM-4 signal is reduced to one-third that of an NRZ signal, which leads to a theoretical reduction of 9.5 dB in the signal-to-noise ratio (SNR) compared to NRZ. Furthermore, the linearity requirements for high-order PAM signals are stricter than those for NRZ modulation due to the increased number of amplitude levels that must be accurately distinguished [8]–[11].

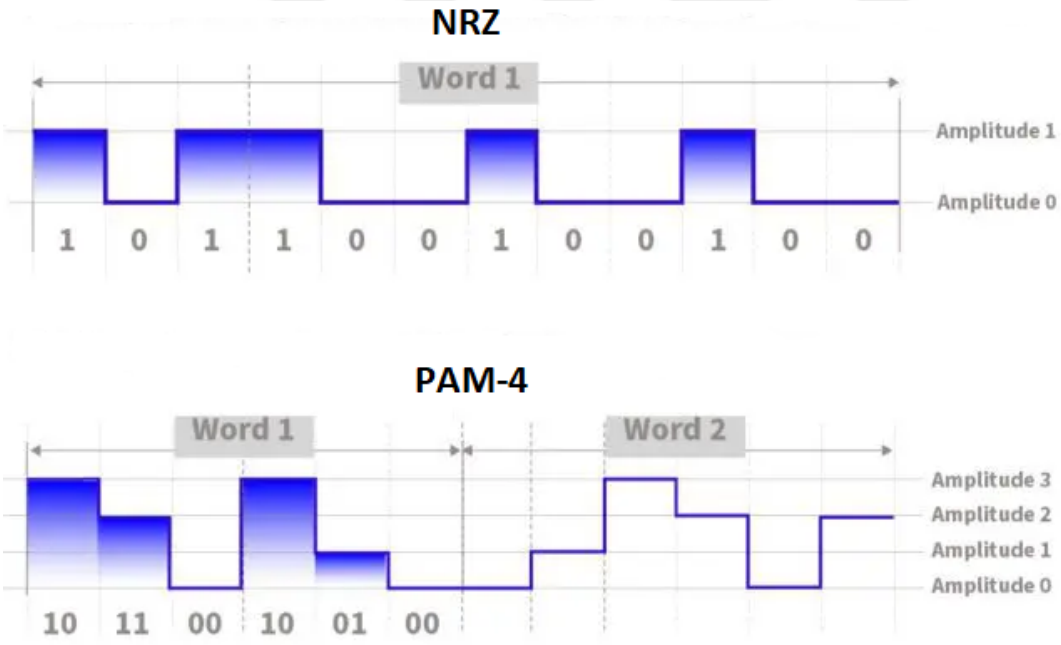

Figure 1.1 : Example of the symbols for NRZ and PAM-4 using the same data pattern [1].

As the modulation levels increase, the amplitude differences between them become smaller, making it more difficult for the receiver to differentiate between them. To

avoid distortion, this requires highly linear performance from the transmitter and receiver, ensuring that each signal level is accurately represented and interpreted.

In multi-PAM applications, each amplitude level must be amplified equally; otherwise, the bit error rate (BER) performance will deteriorate. Uneven amplification can lead to signal distortion, making it difficult for the receiver to accurately distinguish between the different levels. This misalignment increases the likelihood of errors during data transmission and affects the overall reliability of the system. Therefore, maintaining consistent amplification across all PAM levels is crucial to optimize performance and ensure robust communication in higher-order PAM systems. Fig. 1.1 shows an example of the symbols for PAM-4 and NRZ using the same data pattern.

1.1 Purpose of Thesis

This thesis aims to design a digitally controlled variable gain amplifier (VGA) specifically for a PAM-4 optical receiver, achieving high linearity, low noise, and a bandwidth of 5 GHz across all gain settings.

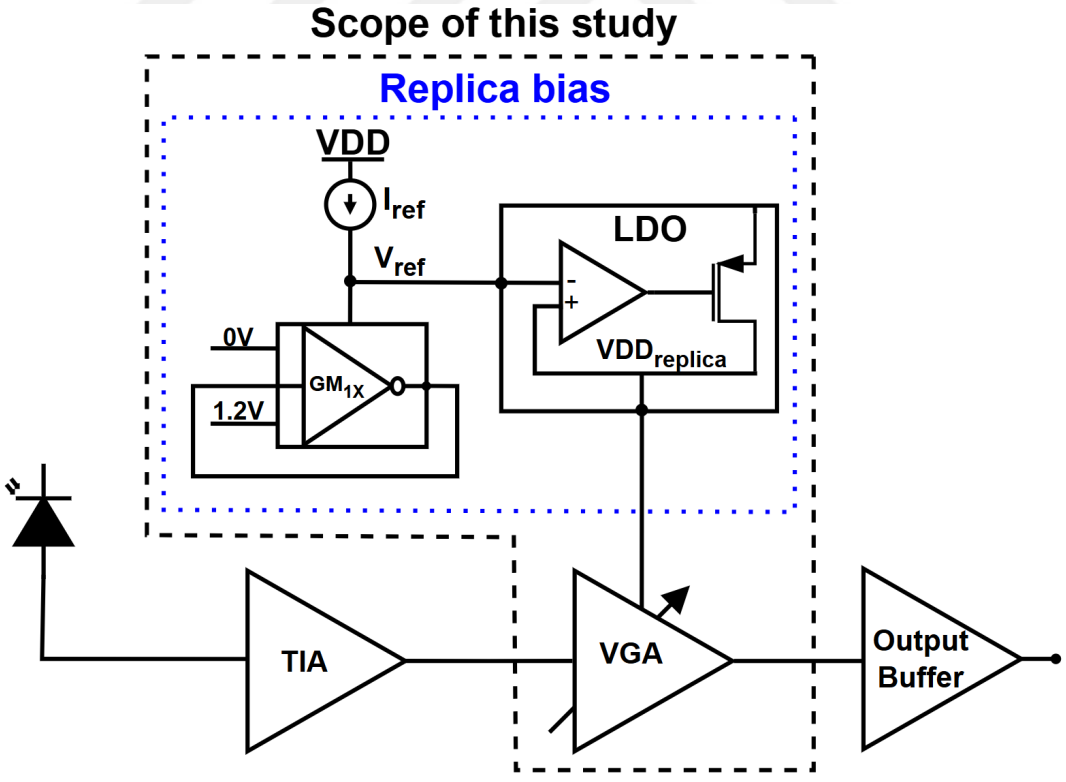

Figure 1.2 : Optical receiver front end and the scope of this thesis.

This design emphasizes high linearity through an inverter-based architecture, recognized for its effective performance in signal amplification, which is crucial for accurately processing PAM-4 signals. To address the challenges posed by process, voltage, and temperature (PVT) variations inherent in inverter-based designs, the thesis incorporates a low-dropout regulator (LDO) based replica biasing method. This technique effectively minimizes the impact of these variations on the performance of the VGA, ensuring consistent operation and reliability across diverse conditions. Fig. 1.2 illustrates the optical receiver front end and outlines the scope of this work, which includes the VGA and the replica biasing method.

1.2 Literature Review

This thesis primarily addresses the design of a VGA with high linearity. An in-depth exploration of linearity was carried out as a starting point, covering both intuitive and mathematical perspectives. Fundamental techniques for improving linearity, including degeneration, feedback, predistortion, the utilization of triode devices, and the inverter-based g_m/g_m method, were thoroughly examined. A detailed discussion of these methods is provided in Chapter 2.

A comprehensive review of numerous papers on linearity-based design was conducted, enabling a thorough understanding and comparison of the advantages and limitations of each approach. Subsequently, the research shifted its focus specifically to VGAs. VGAs are extensively used across various applications, including wireless and wireline communications, optical communication, and hard disk drives. They also find critical applications in hearing aids, biomedical devices, and audio/video signal processing circuits. Additionally, VGAs play a vital role in radar and lidar systems, as well as in various instrumentation applications.

VGAs can be categorized based on their control parameters into two primary types: continuous and digital. In this study, the designed VGA is digitally controlled, also known as a programmable gain amplifier (PGA). The distinction between these two categories is shown in Fig. 1.3.

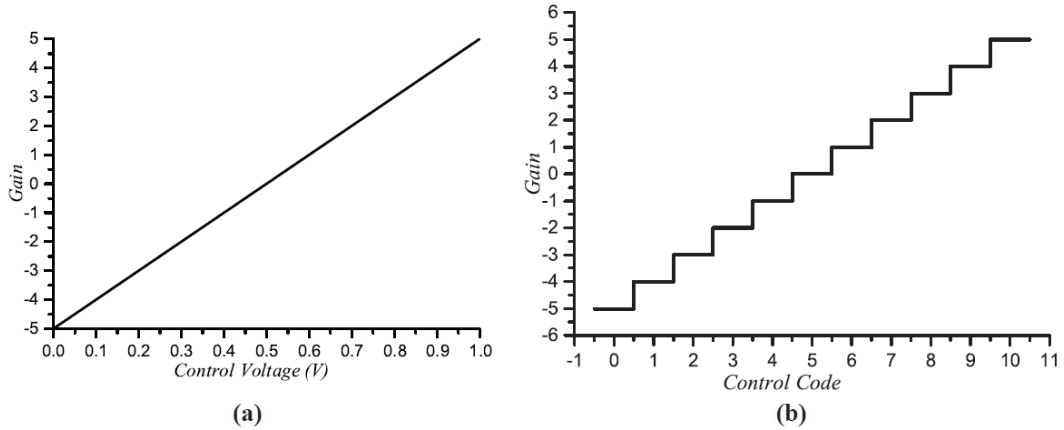

Figure 1.3 : Example characteristics of an analog-controlled VGA vs. a digitally-controlled VGA [2].

There are several fundamental topologies commonly used in VGA design. One widely used topology is the source-degenerated differential amplifier [12]. In this configuration, the gain is controlled by adjusting the source degeneration resistors, which enhance the amplifier linearity and reduce distortion. This topology offers good linearity and wide bandwidth, making it suitable for various applications. However, it has some limitations. The amplifier may exhibit unwanted low-frequency peaking at lower gain levels, distorting the frequency response. Moreover, parasitic capacitances at the degeneration nodes constrain the maximum achievable gain, which can reduce both bandwidth and performance at higher gain settings.

Alternatively, the Gilbert cell topology can be employed for VGA design, offering a different approach to gain control. However, this method presents several challenges. It typically requires higher voltage operation, which results in increased power consumption. Additionally, the Gilbert cell tends to have poorer linearity than other VGA topologies, making it less suitable for applications that demand high precision and low distortion.

Another approach is the g_m-ratioed amplifier, where the gain is determined by the transconductance ratio (g_m) of the input and load transistors. Tuning is achieved by adjusting the current source to modify g_m. g_m-ratioed VGAs are known for their high linearity and stable performance, even in the presence of process variations. However, this method has drawbacks, including reduced output swing, varying common-mode DC output, and inconsistent bandwidth at different gain levels.

A further method involves using variable feedback resistors, such as switched resistive networks or Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) acting as linear resistors. However, this design approach has several limitations. It cannot provide continuous gain and requires additional resistors and chip area as more gain settings are added. Its bandwidth is gain-dependent, meaning that as the gain increases, the bandwidth decreases.

In conclusion, the primary challenges in VGA design include maintaining constant bandwidth and common-mode voltage across varying gain settings, achieving a high output swing with good linearity, and minimizing noise.

CMOS inverters present a promising option for implementing a VGA. While inverters are typically used in digital circuits, their application in analog design has gained popularity in recent years due to several notable advantages [13,14]. One key benefit is that both NMOS and PMOS transistors within an inverter share the same current, which results in a higher effective transconductance (gm_{eff}) for the same power consumption compared to single-transistor configurations, such as common-source amplifiers. The increased gm_{eff} leads to improved gain and better noise performance. Moreover, the simplicity of the inverter circuit, with only two nodes, input, and output, eliminates the risk of introducing additional poles that could degrade the bandwidth [15]. Inverter-based circuits also offer high output swing and rail-to-rail operation, as they do not require current sources. Furthermore, when configured as unit cells, inverters provide a compact and symmetrical layout, reducing systematic mismatches and enhancing overall circuit efficiency.

Many studies have explored the use of inverters in analog circuits, such as inverter-based Operational Amplifiers (OPAMPs) [16], Operational Transconductance Amplifiers (OTAs) [17,18], and filter circuits [19]. Inverter-based Transimpedance Amplifiers (TIAs) [20,21] and output buffers [22] have also been widely recognized for their effectiveness in high-speed applications. In [23], an inverter-based continuous-time linear equalizer (CTLE) with PVT-hardened biasing is presented. The work in [24] describes an inverter-based analog front end, incorporating a programmable gain amplifier (PGA) and CTLE for PAM-4 wireline applications. In

optical communication, inverter-based optical receiver designs have been presented in [25]–[28]. Beyond these examples, there is a wealth of other studies on inverter-based circuits in the literature.

One limitation of inverter-based analog circuits is their sensitivity to PVT variations, especially when the supply voltages are not adaptive. DC currents vary significantly across different PVT corners, deteriorating linearity and other performance characteristics, such as bandwidth and noise. This issue can be mitigated by employing the replica biasing method, which was also utilized in this study. This method ensures more stable operation across varying environmental conditions.

Overall, inverter-based VGAs offer substantial potential for high-performance applications. Their compact design, ease of integration, and favorable power-to-performance ratio make them particularly attractive for modern communication systems, sensor interfaces, and signal processing circuits.

1.3 Thesis Organisation

This thesis begins by introducing the significance of optical communication, the role of multi-level PAM, and the motivation behind the study. This chapter also presents a comprehensive literature review covering the fundamentals and various topologies of VGAs, particularly emphasizing the significance of inverter-based designs.

Chapter 2 delves into the fundamentals of linearity in amplifier design, exploring various techniques for improving linearity and methods for simulating linearity.

Chapter 3 introduces the proposed inverter-based VGA design in detail, including an in-depth explanation of the circuit architecture and the replica biasing method used to enhance over-corner performance.

Chapter 4 presents the layout of the proposed VGA, along with the results from post-layout simulations that validate its functionality and performance.

Finally, Chapter 5 summarizes the key findings and suggests potential future research and development directions.

2. LINEARITY

This chapter discusses the fundamentals of linearity, methods for improving linearity, and techniques for simulating linearity. First, it is essential to examine the operating regions of the MOSFET. The MOSFET has three distinct operating regions, cut-off, linear, and saturation, determined by the DC voltages at its terminals. For an n-channel MOSFET, if $V_{GS} < V_{TH}$, the current is 0, and the operation region is the cut-off region. If $V_{GS} \geq V_{TH}$ and $V_{DS} \leq V_{GS} - V_{TH}$, the MOSFET operates in triode region, while if $V_{GS} \geq V_{TH}$ and $V_{DS} \geq V_{GS} - V_{TH}$, it operates in the saturation region. The current equations for the triode and saturation regions are given in (2.1) and (2.2), respectively.

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] (1 + \lambda V_{DS}) \tag{2.1}$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \tag{2.2}$$

In the current equations, μ_n denotes the electron mobility, C_{ox} represents the oxide capacitance per area, V_{TH} is the threshold voltage, and λ is the channel length modulation parameter.

MOSFETs are mainly used for switching operations and signal amplification. The MOSFET typically operates in the saturation region, which acts as a voltage-controlled current source for amplification. In this mode, a small signal current is generated in response to variations in V_{GS}. The small-signal model of the MOSFET can be utilized for amplification applications. Fig. 2.1 shows the simple small-signal model of an n-channel MOSFET.

Several important parameters need to be discussed. First is the transconductance g_m, which measures the ability to convert voltage changes at V_{GS} into a small signal current in the drain. Mathematically, it is defined as the derivative of the I_D equation with

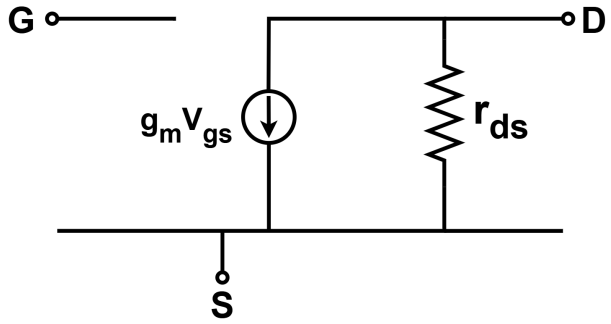

Figure 2.1 : Simple small signal model of n-channel MOSFET.

respect to the V_{GS} voltage. In the saturation region, g_m can be expressed in three different forms, as shown in equations (2.3), (2.4) and (2.5).

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \tag{2.3}$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \tag{2.4}$$

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}} \tag{2.5}$$

Another important parameter is the output resistance r_{ds}, which is typically desired to be high for effective amplification and current source applications. The output resistance is defined as the derivative of the V_{DS} voltage with respect to I_D and is given by equation (2.6).

$$r_{ds} = \frac{1}{\frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \lambda} \tag{2.6}$$

Assuming $\lambda V_{DS} \ll 1$, the output resistance can be approximated by (2.8).

$$r_{ds} \approx \frac{1}{\lambda I_D} \tag{2.7}$$

The output conductance g_{ds} of a MOSFET can also be defined as the inverse of the output resistance r_{ds}.

$$g_{ds} = \frac{1}{r_{ds}} \approx \lambda I_D \tag{2.8}$$

Another key parameter is the intrinsic gain, defined as the product of g_m and r_{ds}. It represents the maximum voltage gain achieved using a single device.

In switching applications, one terminal of the MOSFET is used to control the signal passage between the other two terminals. When used as a switch, the MOSFET operates in the linear region, functioning as a voltage-controlled resistor. The on-resistance R_{on} of the MOSFET is given by (2.9), assuming $V_{DS} \ll 2(V_{GS} - V_{TH})$.

$$R_{on} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \tag{2.9}$$

For effective switching, the R_{on} resistance, which represents the resistance when the switch is closed, should be minimized. In contrast, the R_{off} resistance, which represents the resistance when the switch is open, should be maximized. Fig. 2.2 illustrates the MOSFET used as a switch, along with its open and closed models.

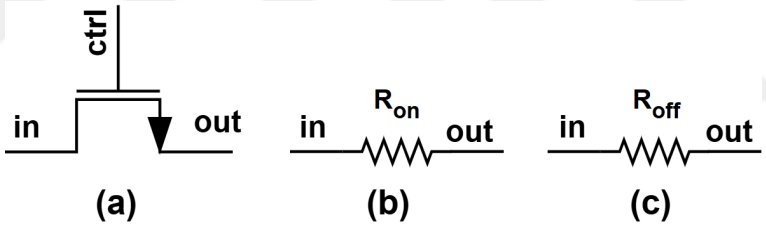

Figure 2.2 : (a) MOSFET as a switch, (b) its ON model, and (c) its OFF model.

The g_m in the linear region varies linearly with V_{DS} and is given by equation (2.10).

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{DS} \tag{2.10}$$

2.1 Definition of Linearity

Linearity is the ability of an amplifier to produce an output signal where the amplitude changes proportionally with the input signal amplitude. An ideal amplifier exhibits constant gain throughout the entire input range, resulting in a perfectly linear input-output characteristic.

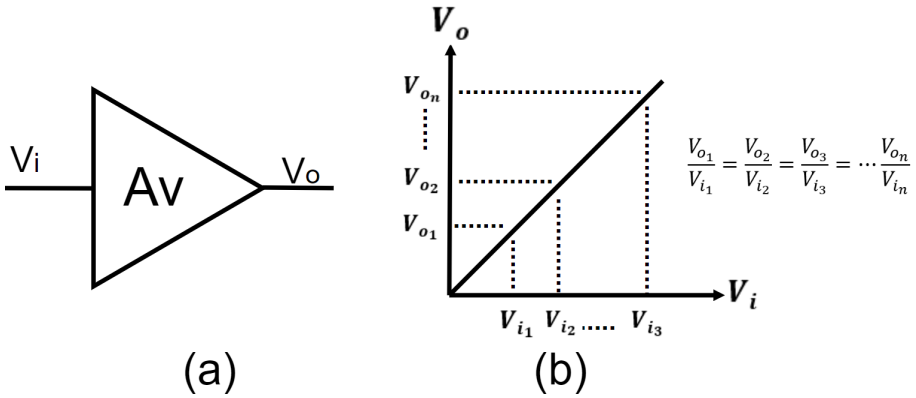

Figure 2.3 : (a) block diagram of the ideal voltage amplifier and (b) its input-output characteristic.

Fig. 2.3 illustrates an ideal voltage amplifier along with its voltage transfer characteristics (VTC). However, in practice, no amplifier achieves perfect linearity; all amplifiers exhibit some nonlinear behavior. The input-output relationship of a nonlinear amplifier can be described using a power series expansion.

In this approach, the output $y(t)$ of a nonlinear amplifier, in response to the input $x(t)$, can be expressed as shown in (2.11).

$$y(t) = \alpha_1 x(t) + \alpha_2 x(t)^2 + \alpha_3 x(t)^3 + \alpha_4 x(t)^4 + \alpha_5 x(t)^5 + \cdots \tag{2.11}$$

For small values of x, which corresponds to the linear region of the amplifier, the output y(t) can be approximated by (2.12), where α_1 represents the small signal gain of the amplifier.

$$y(t) \approx \alpha_1 x(t) \tag{2.12}$$

2.2 Linearity Improvement Methods

The purpose of linearization is to make the amplifier's gain less sensitive to variations in device parameters such as g_m and r_o. There are various techniques for linearization of amplifiers in the literature. This section discusses the main linearization methods. There are also other methods that are modified or combined versions of these main techniques.

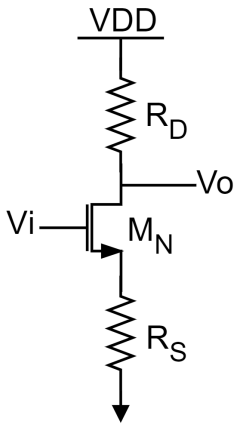

Figure 2.4 : Resistive-loaded common source amplifier with source degeneration.

2.2.1 Degeneration

One of the most commonly used methods for linearizing amplifiers is degeneration. This technique involves placing a resistor at the source of the transistor, which significantly reduces the amplifier's dependence on device parameters and thus improves linearity. For instance, the simple resistive-loaded common-source amplifier, as shown in Fig. 2.4, incorporates degeneration.

The gain of this amplifier is given by (2.13), assuming the body effect is neglected:

$$A_V = -\frac{g_m R_D}{1 + g_m R_S} \tag{2.13}$$

When $g_m R_S \gg 1$, the gain simplifies to (2.14), becoming independent of the device parameters.

$$A_V \approx -\frac{R_D}{R_S} \tag{2.14}$$

2.2.2 Feedback

Feedback is another technique used to linearize amplifiers. In addition to properties like gain insensitivity and bandwidth extension, feedback offers a significant advantage in reducing nonlinearity in amplifiers [29]–[31]. This concept can be better understood through the general block diagram of a feedback amplifier shown in Fig. 2.5. The gain expression for this general feedback amplifier is given by (2.15).

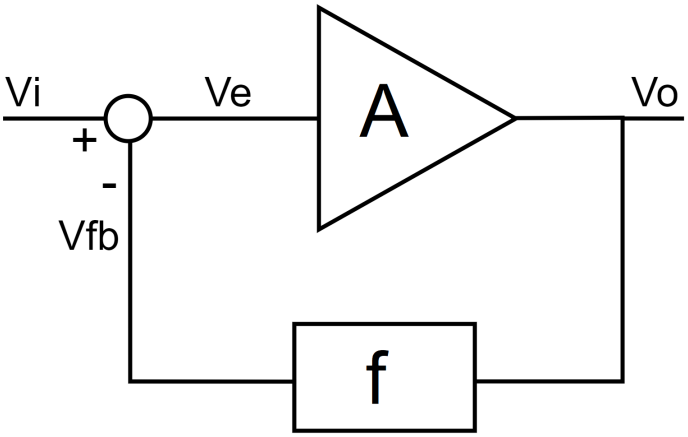

Figure 2.5 : Block diagram of an amplifier with feedback.

$$A_V = \frac{V_o}{V_i} = \frac{A}{1+Af} \tag{2.15}$$

In this expression, Af denotes the feedback amount known as the loop gain. When Af is much larger than 1, the gain expression can be simplified to (2.16). This simplification linearizes the amplifier's behavior by minimizing the influence of the main amplifier, making its performance primarily dependent on the feedback parameters. Fig. 2.6 presents an example of the input-output characteristic of an amplifier, both with and without feedback. As observed, the feedback application results in a linearization of the characteristic.

$$A_V \approx \frac{1}{f} \tag{2.16}$$

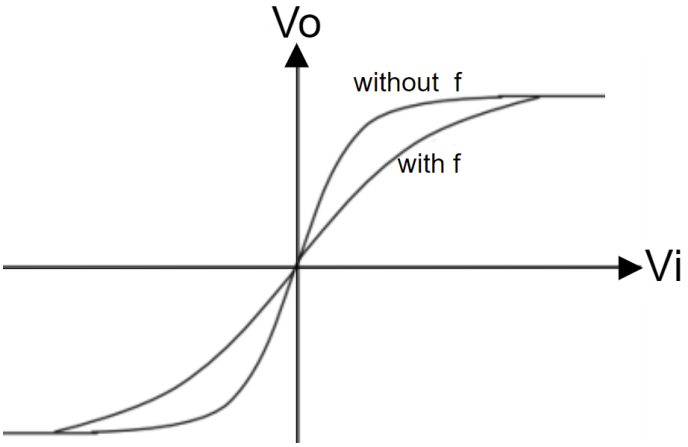

Figure 2.6 : Transfer characteristics of an amplifier with and without feedback.

2.2.3 Predistortion

Most amplifiers exhibit compressive behavior, meaning that the output increases linearly with the input up to a certain point, after which it begins to saturate. In contrast, expansion refers to a scenario where the output initially increases linearly with the input but then rises rapidly and non-linearly.

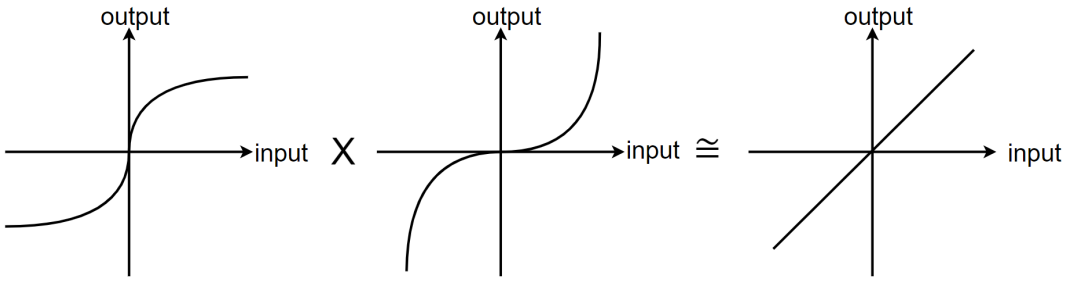

Figure 2.7 : Conceptual representation of the predistortion technique.

The predistortion technique improves overall linearity by combining two stages: one with expansion characteristics and the other with compression characteristics [32,33]. This concept is illustrated in Fig. 2.7.

2.2.4 Triode devices

Another method for linearizing amplifiers involves using input devices that operate in the triode region [34]–[36]. As demonstrated in (2.1) and (2.10), the drain current I_D in the triode region varies linearly with the gate-source voltage V_{GS}, while the g_m varies linearly with the drain-source voltage V_{DS}. This characteristic reduces nonlinearity compared to devices operating in the saturation region. However, a challenge with this approach is that the g_m of devices in the triode region is lower than that of devices in the saturation region, making it more difficult to achieve high gain. Cascode devices can address this issue and maintain the available gain, which isolates the load resistance from the low output resistance of the input device, thereby enhancing overall performance.

2.2.5 g_m / g_m method

The g_m/g_m method is an appealing alternative for designing highly linear amplifiers [15,37]–[39]. This approach utilizes an inverter transconductor followed by a

diode-connected inverter load, effectively canceling the nonlinear characteristics of the transconductor. The output current for the transconductor shown in Fig. 2.8 is expressed in (2.17).

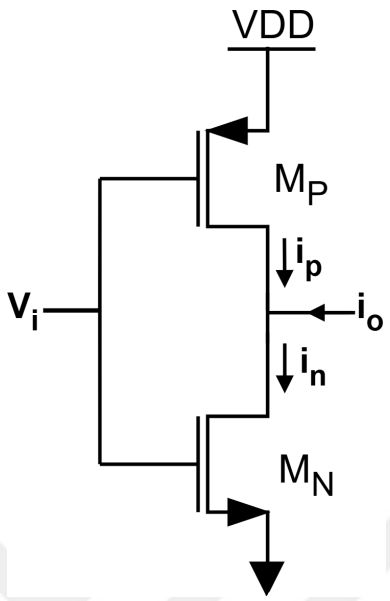

Figure 2.8 : Inverter transconductor schematic.

$$i_o = i_n - i_p \approx (k_n V_{ov,n} + k_p V_{ov,p}) V_i + \left(\frac{k_n}{2} - \frac{k_p}{2}\right) V_i^2 \tag{2.17}$$

where $k = \mu_n C_{ox}\left(\frac{W}{L}\right)$ and $V_{ov} = V_{GS} - V_{TH}$. If $k_n = k_p$, the second-order nonlinearity can be effectively canceled.

The block diagram of a simple g_m/g_m amplifier is illustrated in Fig. 2.9, and the gain of this amplifier is given by (2.18), assuming channel length modulation is neglected.

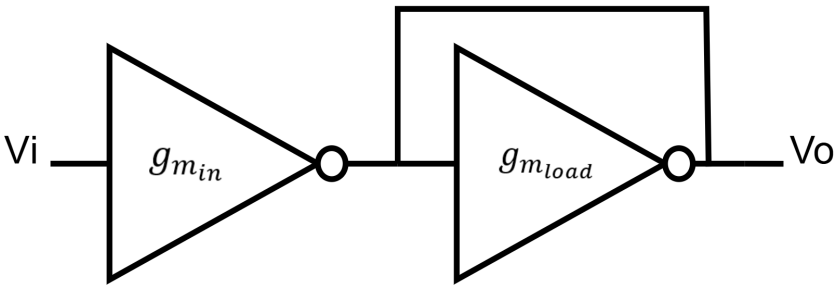

Figure 2.9 : Block diagram of simple g_m/g_m amplifier .

$$A_V \approx \frac{g_{m_{in}}}{g_{m_{load}}} = \frac{g_{m,N_{in}} + g_{m,P_{in}}}{g_{m,N_{load}} + g_{m,P_{load}}} \tag{2.18}$$

2.3 Linearity Simulation Methods

An important consideration is the approaches employed to simulate linearity. Several methods are available for this purpose, which are discussed below. Firstly, the flatness of g_m over the varying input voltage can be used as a linearity metric [40]–[44]. While this method provides a useful assessment, it primarily accounts for nonlinearity from g_m. However, the output resistance of the devices, r_o, is also a significant source of nonlinearity. Therefore, it is more effective to evaluate the flatness of the overall gain, which incorporates the effects of both g_m and r_o, by sweeping the input voltage. Any deviation from the ideal curve, as shown in Fig. 2.10, can be characterized as nonlinearity. In particular, the voltage transfer characteristic (VTC) slope varies at different input levels for a nonlinear amplifier. This definition provides a useful metric for evaluating nonlinearity in sweeping methods [30].

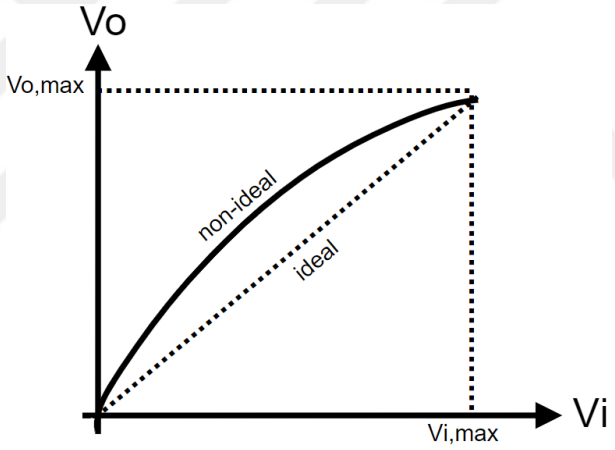

Figure 2.10 : Deviation from ideal characteristic.

Nonlinearity can also be assessed by examining the gain versus input voltage plot, as shown in Fig. 2.11. The input range in which the gain decreases by 1 dB from the mid-gain level can serve as a useful measure of nonlinearity, especially when comparing different topologies.

A further method to characterize the amplifier nonlinearity is harmonic distortion, which accounts for the influence of frequency components on this nonlinearity. When a pure sinusoidal signal is applied at the input, the frequency components and their respective coefficients can be determined using (2.11). Assuming the input signal is

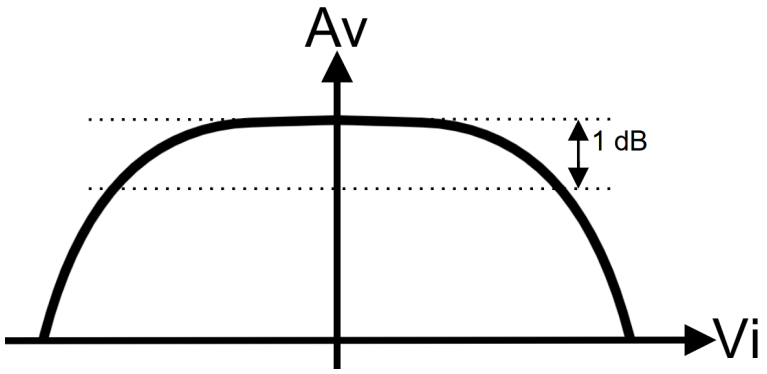

Figure 2.11 : Gain versus input voltage.

given by $x(t) = A\cos(\omega t)$, the output $y(t)$ can be expressed as in (2.19), revealing the presence of multiple frequency components in addition to the fundamental frequency.

$$y(t) = \alpha_1 A\cos(\omega t) + \alpha_2 A^2\cos^2(\omega t) + \alpha_3 A^3\cos^3(\omega t) + \cdots \tag{2.19}$$

$$\cos^2(x) = \frac{1+\cos(2x)}{2} \tag{2.20}$$

$$\cos^3(x) = \frac{3\cos(x)+\cos(3x)}{4} \tag{2.21}$$

$$\cos^4(x) = \frac{3+4\cos(2x)+\cos(4x)}{8} \tag{2.22}$$

Using trigonometric equations such as (2.20), (2.21) and (2.22), equation (2.19) can be written as in (2.23).

$$y(t) = \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos(\omega t) + \frac{\alpha_2 A^2}{2}\cos(2\omega t) + \frac{\alpha_3 A^3}{4}\cos(3\omega t) + \cdots \tag{2.23}$$

Now, another measure of nonlinearity, harmonic distortion (HD), can be defined using (2.23) [29].

$$HD_n = \frac{\text{Magnitude of } n^{\text{th}} \text{ harmonic}}{\text{Magnitude of fundamental component}}, \quad \text{for } n > 1 \tag{2.24}$$

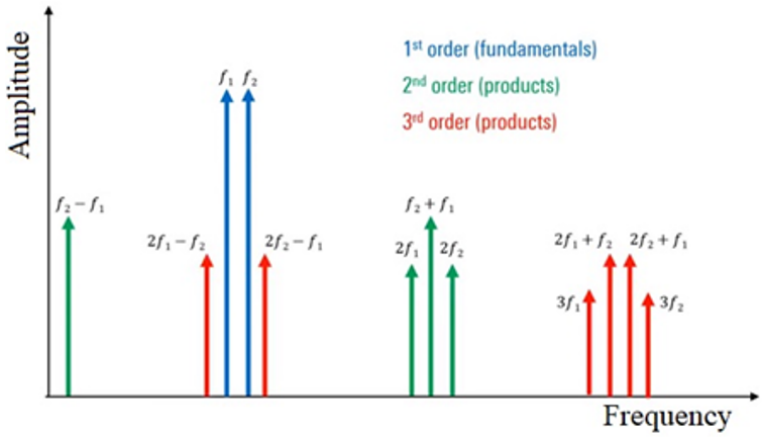

Figure 2.12 : Frequency spectrum of an amplifier output including third order products [3].

In addition to HD_n, total harmonic distortion (THD) is defined as the ratio of the sum of the powers of all harmonics with $n > 1$ to the power of the fundamental harmonic, as shown in (2.25). THD is commonly used as a measure of nonlinearity.

$$THD = \frac{\sqrt{\frac{\alpha_2^2 A^4}{8} + \frac{\alpha_3^2 A^6}{32} + \cdots}}{\frac{\left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)^2}{2}} \tag{2.25}$$

Third-order intercept (IP3) is another method for measuring nonlinearity. In this approach, two signals with frequencies close to each other, f_1 and f_2, are typically applied to the input, and the output frequency components are analyzed. As shown in Fig. 2.12, the components with frequencies $2f_1 - f_2$ and $2f_2 - f_1$, which are closest to the main signal components, are the most problematic.

In the output power versus input power graph shown in Fig. 2.13, the fundamental and third-order components intersect at a specific point. The fundamental component increases with a slope of 1, while the third-order component increases with a slope of 3. The input level at this intersection is referred to as the input third-order intercept (IIP3), and the output level at this intersection is known as the output third-order intercept (OIP3).

IP3 is generally a power-based measurement rather than one based on voltage or current. It is primarily used for Radio Frequency Integrated Circuits (RFIC) and systems.

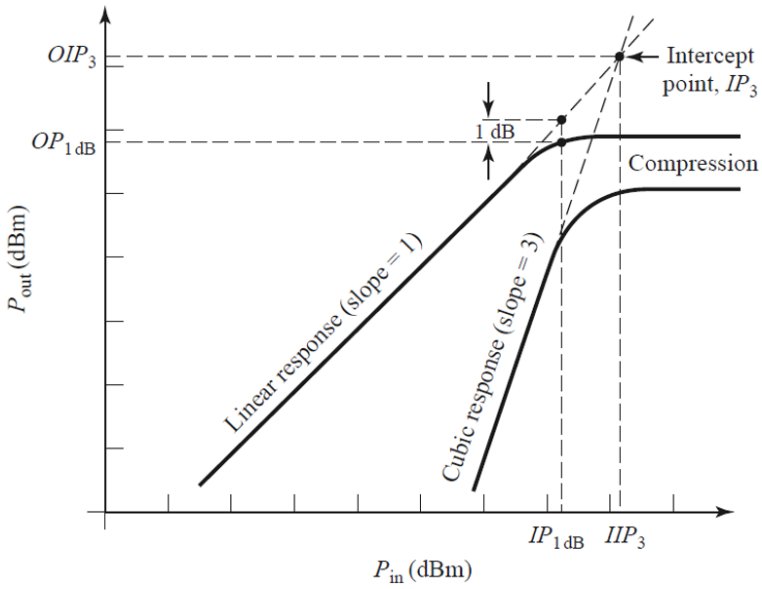

Figure 2.13 : IIP_3 and OIP_3 on *Pout* vs. *Pin* plot [4].

Another method to characterize linearity is through the use of the eye diagram. An eye diagram is created by superimposing consecutive waveforms, as illustrated in Fig. 2.14, which presents an example of an NRZ eye diagram.

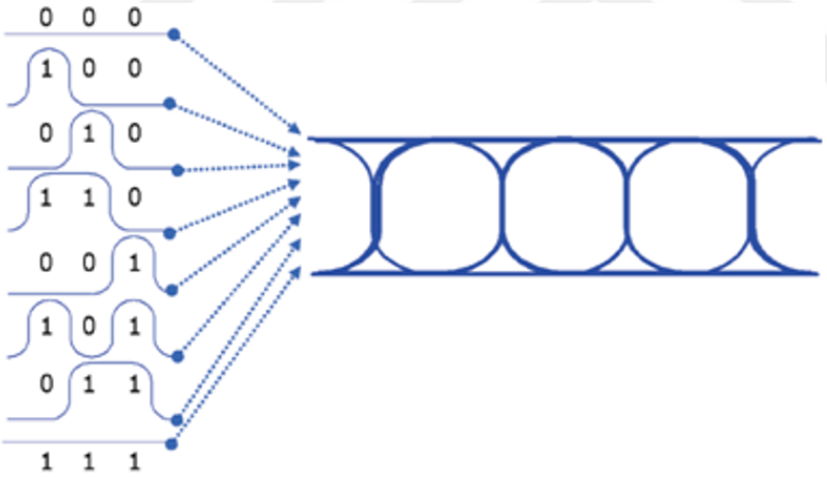

Figure 2.14 : Formation of NRZ eye diagram [5].

A careful look at the eye diagram can also provide information about signal-to-noise ratio, clock jitter, and skew [45]. The eye diagram of multiple PAM applications provides information about the linearity of the circuit or system. For an ideal $PAM-X$ application, there are $X-1$ eyes in the eye diagram, and the eye heights are the same. Namely, eyes are symmetrical. A numerical measurement, transmitter linearity (R_{LM}), can be used to determine nonlinearity from the eye diagram. Fig. 2.15 shows examples

of the ideal eye diagram and non-ideal eye diagram of PAM-4 modulation and the parameters used in the R_{LM} calculation.

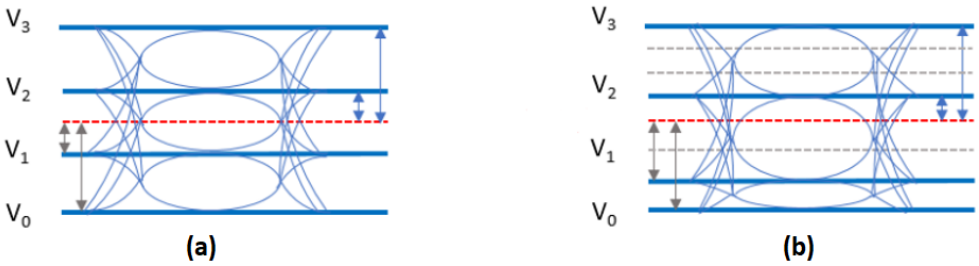

Figure 2.15 : (a) Example of ideal and (b) non-ideal PAM-4 eye diagrams [6].

$$V_{\min} = \frac{V_0 + V_3}{2} \tag{2.26}$$

$$E_{S1} = \frac{V_1 + V_{\min}}{V_0 - V_{\min}} \tag{2.27}$$

$$E_{S2} = \frac{V_2 - V_{\min}}{V_3 - V_{\min}} \tag{2.28}$$

$$R_{LM} = \min(3 \times E_{S1}, 3 \times E_{S2}, 2 - 3 \times E_{S1}, 2 - 3 \times E_{S2}) \tag{2.29}$$

An ideal eye diagram has a R_{LM} of 1, while a non-ideal eye diagram has a R_{LM} of less than 1. For example, a R_{LM} of 0.9 means 10% of nonlinearity.

3. INVERTER-BASED VGA

In this chapter, the proposed inverter-based VGA, which employs the g_m / g_m method, is explained in detail. The concept of the unit cell and the design of a simple unit cell-based amplifier are discussed, along with pole-zero and gain analyses. A conceptual diagram of the proposed VGA is presented to aid in understanding, followed by an explanation of the designed VGA based on this concept. Finally, the replica biasing method, implemented with an LDO, is explained.

3.1 Unit Cell

The proposed inverter-based VGA utilizes unit cells to achieve a compact design while effectively minimizing systematic mismatches. Each unit cell comprises inverters that allow for adjustable g_m by incorporating switches that control the activation and deactivation of the cell. To mitigate nonlinearity arising from the inherent square-law behavior of the transistors, significant efforts have been directed toward matching the g_m of the NMOS and PMOS devices, denoted as M_N and M_P respectively [15]. As illustrated in Fig. 3.1, the load is designed to remain constant, while both NMOS and PMOS switches are configured to remain always ON. Incorporating switches for both the g_m and load cells is crucial to prevent any potential imbalance between the g_m cell and the load cell, ensuring consistent performance.

The straightforward amplifier design utilizing a g_m cell and a load cell is presented in Fig. 3.2, and it incorporates two poles: one at the input and another at the output, along with a zero created by the feedforward capacitor in the input stage. The input pole is given in (3.1), while (3.2) describes the output pole, and the location of the zero is given in (3.3). In these equations, C_{in} represents the total parasitic capacitances at the input node. R_{in} signifies the output resistance of the preceding stage, and C_{load} denotes the load capacitance. Furthermore, C_{out} indicates the parasitic capacitance at the output node.

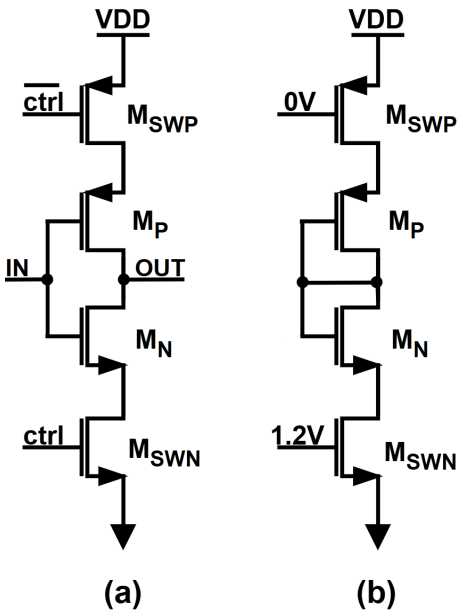

Figure 3.1 : (a) Inverter g_m unit cell and (b) g_m cell as load.

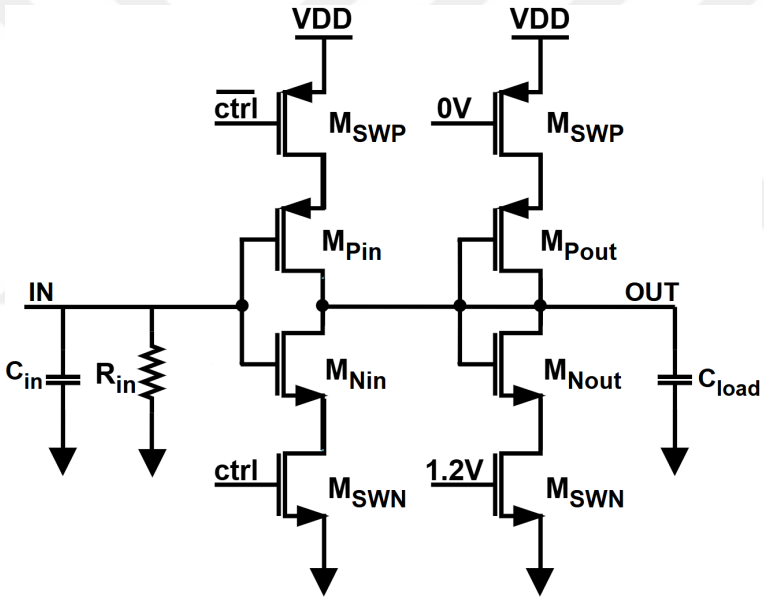

Figure 3.2 : Simple voltage amplifier using unit cells.

$$\omega_{in} \approx \frac{1}{R_{in}.C_{in}} \tag{3.1}$$

$$\omega_{out} \approx \frac{g_{m,MN_{out}} + g_{m,MP_{out}}}{C_{load} + C_{out}} \tag{3.2}$$

$$\omega_z \approx \frac{g_{m,MN_{in}} + g_{m,MP_{in}}}{C_{GD,MP_{in}} + C_{GD,MN_{in}}} \tag{3.3}$$

Along with the poles and zeros, the gain of this configuration can be described as shown in (3.4).

$$A_v = \frac{V_{out}}{V_{in}} = -\frac{g_{m,MNin} + g_{m,MPin}}{g_{m,MNout} + g_{m,MPout} + g_{ds,MNin} + g_{ds,MPin} + g_{ds,MNout} + g_{ds,MPout}} \quad (3.4)$$

As seen, the gain depends not only on the g_m values but is also influenced by the output conductances g_{ds}, which negatively affect the gain, causing it to decrease. The gain equation can be simplified to (3.5) by neglecting the channel length modulation.

$$A_v = \frac{V_{out}}{V_{in}} \approx -\frac{g_{m,MNin} + g_{m,MPin}}{g_{m,MNout} + g_{m,MPout}} \quad (3.5)$$

3.2 Proposed VGA

The conceptual diagram of the proposed VGA is shown in Fig. 3.3. The g_m cells consist of two components: a permanent, always-on section that sets the base gain and adjustable g_m cells that alter the overall gain. The gain of the VGA is theoretically defined as the ratio of the total g_m to the load. By modifying the adjustable g_m cells, the gain can be controlled through control bits. As illustrated in the figure, fixed load cells maintain a consistent bandwidth across different gain settings by remaining continuously active. There are several key aspects essential for understanding the working principle. The idea of the proposed VGA can be explained as follows, assuming 5 continuously active g_m cells and 3 load cells as an example. As the control code varies from 0 to 15, the theoretical gain for each control code can be computed as $\frac{5+0}{3}$, $\frac{5+1}{3}$, $\frac{5+2}{3}$, and so on up to $\frac{5+15}{3}$. The number of always-on load cells influences the magnitude of the gain increments: having more load cells leads to a smaller step in gain for each increase in the control code, while fewer load cells result in larger increments. Conversely, the number of always-on g_m cells sets the baseline gain: fewer g_m cells yield a lower base gain, while more cells provide a higher initial gain. For example, with a control code of 0 and 6 load cells, if there are 9 always-on input cells, the minimum achievable gain is $\frac{9}{6}$. On the other hand, if only 4 input cells are always on, the minimum gain would be $\frac{4}{6}$. Although the VGA concept is based on this idea, in practice it is affected by transistor and cell nonidealities, meaning the actual gain

values may not exactly match the theoretical calculation. Therefore, the desired values can be obtained through iterations during design.

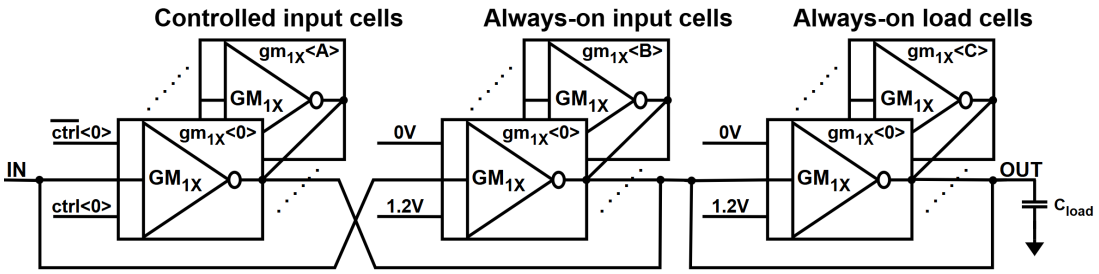

Figure 3.3 : Conceptual schematic representation of the proposed VGA.

The VGA is based on the concept illustrated in Fig. 3.3. However, there are primarily two modifications. First, to harness the benefits of differential structures, such as improved noise immunity, reduced second-order harmonic distortion, and enhanced voltage swing, the VGA is configured pseudo-differential, as shown in Fig. 3.4. While increasing the g_m code increases the VGA's gain, saturation occurs at higher input code values. As more g_m cells are activated, their output conductance g_{ds} significantly affects the overall load, leading to gain saturation as the gain code increases. As the second modification, to alleviate this gain compression issue, as depicted in Fig. 3.4, the proposed VGA uses the first 6 bits to control the $1X$ cells, the next 4 bits for the $1.5X$ cells, and the final 5 bits for the $2X$ cells. This configuration effectively counters gain compression as the g_m code increases, resulting in a more linear relationship between gain and control code. Another critical aspect is the biasing of the VGA. The bias points for the input and output nodes are determined as follows: the diode-connected load cells set the bias at the output node. For the input of the

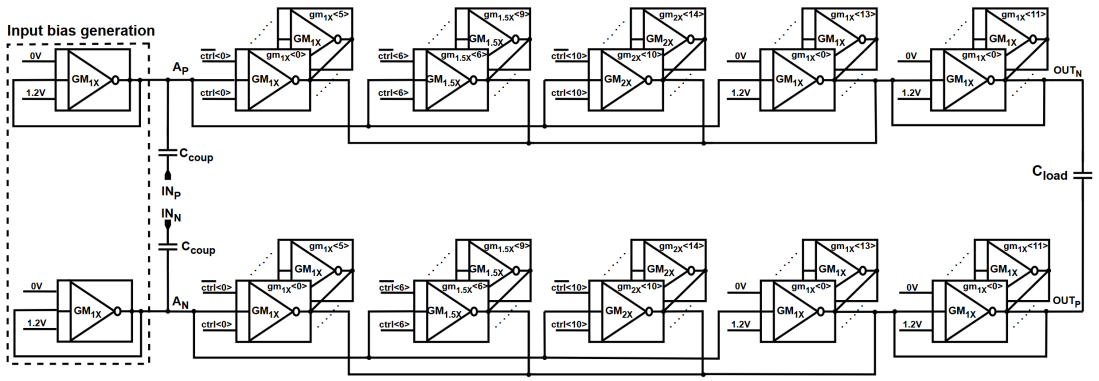

Figure 3.4 : Schematic diagram of the proposed VGA.

g_m cells, the preceding stage in the receiver chain generally supplies the bias voltage. However, since VGA is considered independently in this study, the bias point of the input node must also be established. For this purpose, a diode-connected unit cell is placed at the input, as shown in Fig. 3.4. This structure generates robust and well-defined V_{GS} voltages like current mirrors.

Like the basic circuit depicted in Fig. 3.2, the proposed VGA features two poles, one at the input and another at the output. A zero is introduced due to the drain-gate parasitic capacitances associated with the g_m cells. Given that the effective g_m of cells ($g_{m_{1X}}$, $g_{m_{1.5X}}$, $g_{m_{2X}}$) parasitic capacitances, and output conductances, the equations for the input pole, output pole, zero, and gain can be formulated as shown in (3.6), (3.7), (3.8), and (3.9), depending on the control bits.

$$\omega_{P_{\text{in}}} \approx \frac{g_{m_{1X}}}{C_{A_{P,N}}} \tag{3.6}$$

$$\omega_{P_{\text{out}}} \approx \frac{g_{m_{1X}} \sum_{n=0}^{11} n}{C_{load} + C_{out}} \tag{3.7}$$

$$\omega_z \approx \frac{g_{m_{1X}} \sum_{n=0}^{5} \text{ctrl}[n] + g_{m_{1.5X}} \sum_{n=6}^{9} \text{ctrl}[n] + g_{m_{2X}} \sum_{n=10}^{14} \text{ctrl}[n] + g_{m_{1X}} \sum_{n=0}^{13} n}{C_{GD_{1X}} \sum_{n=0}^{5} \text{ctrl}[n] + C_{GD_{1.5X}} \sum_{n=6}^{9} \text{ctrl}[n] + C_{GD_{2X}} \sum_{n=10}^{14} \text{ctrl}[n] + C_{GD_{1X}} \sum_{n=0}^{13} n} \tag{3.8}$$

$$A_V \approx \frac{g_{m_{1X}} \sum_{n=0}^{5} \text{ctrl}[n] + g_{m_{1.5X}} \sum_{n=6}^{9} \text{ctrl}[n] + g_{m_{2X}} \sum_{n=10}^{14} \text{ctrl}[n] + g_{m_{1X}} \sum_{n=0}^{13} n}{g_{m_{1X}} \sum_{n=0}^{11} n + g_{ds_{1X}} \sum_{n=0}^{11} n + g_{ds_{1X}} \sum_{n=0}^{5} \text{ctrl}[n] + g_{ds_{1.5X}} \sum_{n=6}^{9} \text{ctrl}[n] + g_{ds_{2X}} \sum_{n=10}^{14} \text{ctrl}[n] + g_{ds_{1X}} \sum_{n=0}^{13} n} \tag{3.9}$$

3.3 PVT Insensitive Biasing of VGA

One of the primary drawbacks of inverter-based circuits is their sensitivity to PVT variations. These fluctuations can lead to inconsistent performance, affecting the overall reliability and functionality of the circuit. To address these challenges, techniques such as replica biasing have been implemented [15,46,47]. This method stabilizes the performance of inverter-based circuits by providing a variable supply voltage that compensates for PVT fluctuations, thus enhancing the circuit's robustness. In the replica biasing technique, a reference circuit, known as the replica, plays a

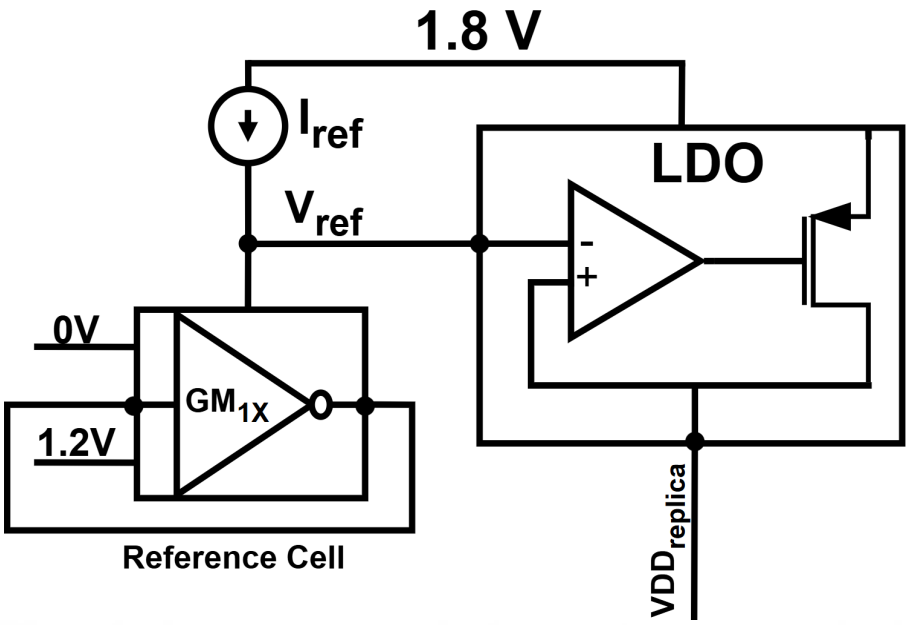

Figure 3.5 : Block level schematic of the replica biasing circuit.

crucial role by continuously monitoring changes in temperature and voltage while measuring essential parameters like bias voltages and currents. This setup allows the replica to capture the operational conditions of the circuit, including variations that might not be immediately evident. The information gathered from this reference circuit enables the main circuit to adjust through a feedback mechanism, effectively correcting for these variations to maintain consistent performance under varying conditions. In this study, an LDO-based replica biasing method is employed. The block-level schematic and transistor-level schematic of the replica biasing technique used in this study are shown in Fig.3.5 and Fig.3.6, respectively. A $1X$ diode-connected unit cell, $g_{m_{1X}}$, serves as the reference for biasing. The nominal bias current for this unit cell is generated by a fixed current source, I_{ref}, with its value chosen to be 30 μA. As shown in Fig.3.6, a differential pair, along with a stacked PMOS load and PMOS pass-gate transistors M_{passa} and M_{passb}, facilitates the implementation of the indirect Miller compensation technique.

The bias current produced by this arrangement generates a reference voltage, V_{ref}, which is then copied by the LDO to supply the VGA. This reference voltage allows the VGA supply to adapt automatically by continuously monitoring PVT variations, ensuring operation at a constant bias current across all conditions. The V_{ref} voltage

can be expressed in terms of V_{GS} values of the devices in the always-on reference cell as shown in (3.10), assuming that the switches, M_{SWP} and M_{SWN}, do not cause any voltage drop.

$$V_{ref} = V_{GS_{MN}} + |V_{GS_{MP}}| \tag{3.10}$$

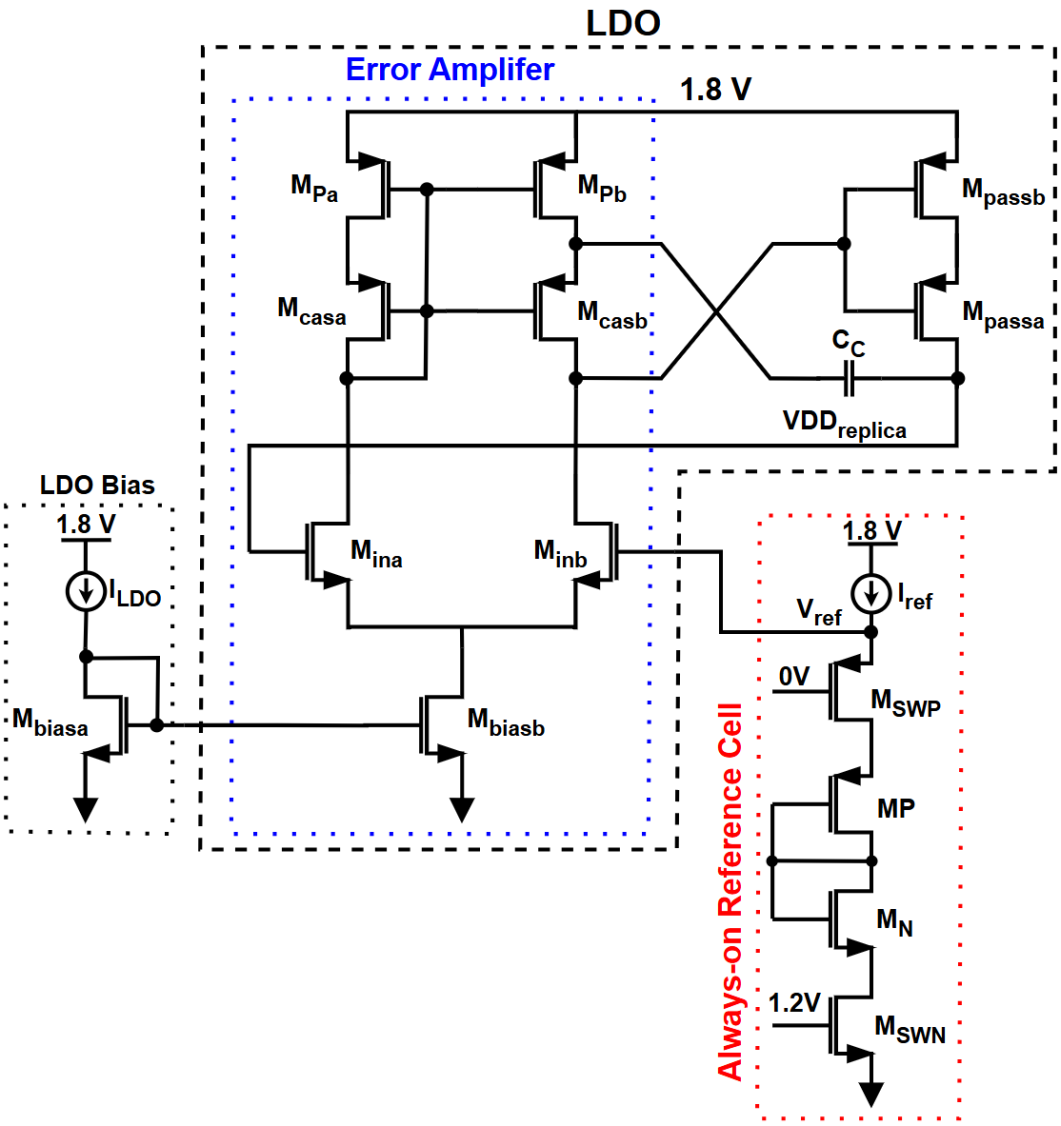

Figure 3.6 : Transistor-level schematic of the replica biasing.

For example, if the threshold voltages decrease in a specific corner, the V_{GS} voltages will also decrease in order to maintain the same fixed reference current, I_{ref}. As the V_{GS} voltages decrease, the V_{ref} voltage also decreases, which in turn causes the supply for the VGA, $VDD_{replica}$, to decrease as well.

The current through the LDO output, specifically through the LDO pass devices M_{passa} and M_{passb}, is also used by the VGA, meaning the current is reused. Due to this current reuse, there is only a small increase in the overall current consumption from the LDO, which is primarily caused by the error amplifier of the LDO. The biasing of the error amplifier is achieved using a simple current mirror consisting of the M_{biasa} and M_{biasb} devices, with a reference current I_{LDO} of 50 µA. The copy ratio between the current source device of the error amplifier, M_{biasb}, and the reference device, M_{biasa}, is 8.

One crucial aspect to consider is carefully selecting the dimensions of the LDO pass devices. These devices must be appropriately sized to ensure they can adequately supply the current required by the VGA across all gain conditions. This meticulous design consideration is essential for the efficient operation of the VGA, allowing it to maintain optimal performance even under various operational circumstances. The replica biasing method employed in this circuit plays a crucial role in achieving a realistic and high-quality design. As demonstrated in Chapter 4, this approach significantly minimizes sensitivity to PVT variations, thereby enhancing the reliability and stability of the circuit.

4. SIMULATION RESULTS

This section presents the layout figures for both the sub-blocks and the overall circuit, the testbench used for simulations, and the post-layout simulation results evaluated under PVT conditions. The simulations provide a comprehensive circuit performance analysis, covering key metrics such as DC behavior, frequency response, transient response, distortion, and noise performance. These analyses are essential to understanding the overall functionality and robustness of the designed system. The post-layout simulations are conducted under specific PVT conditions. For voltage, simulations are performed at supply voltages of 1.7 V and 1.9 V, with the nominal supply voltage set to 1.8 V. Temperature variations are considered by analyzing extreme values of -40 °C and 120 °C. In contrast, the nominal temperature is set at 27 °C. Additionally, the effects of process variations are captured by simulating four different process corners, which represent combinations of fast and slow process parameters: Fast-Fast (FF), Fast-Slow (FS), Slow-Fast (SF), and Slow-Slow (SS). These process corners, combined with the voltage and temperature variations, result in 16 unique corner cases. The comprehensive set of 16 corner cases provides a robust evaluation of the circuit performance under varying conditions. At the end of this section, a table summarizing the worst-case performance across all corner cases. This table highlights the most challenging performance limitations encountered throughout the design space, offering insights into the worst-case behavior of the designed VGA under extreme operating conditions.

4.1 Layout

The layouts of the $1X$, $1.5X$, and $2X$ cells share the same structure, with the sole distinction being their sizes, which are adjusted through multiplier scaling, as shown in Fig. 4.1. Additionally, the VGA core layout is compact and symmetrical, with dimensions of 66 $\mu m \times 25$ μm, as illustrated in Fig. 4.2.

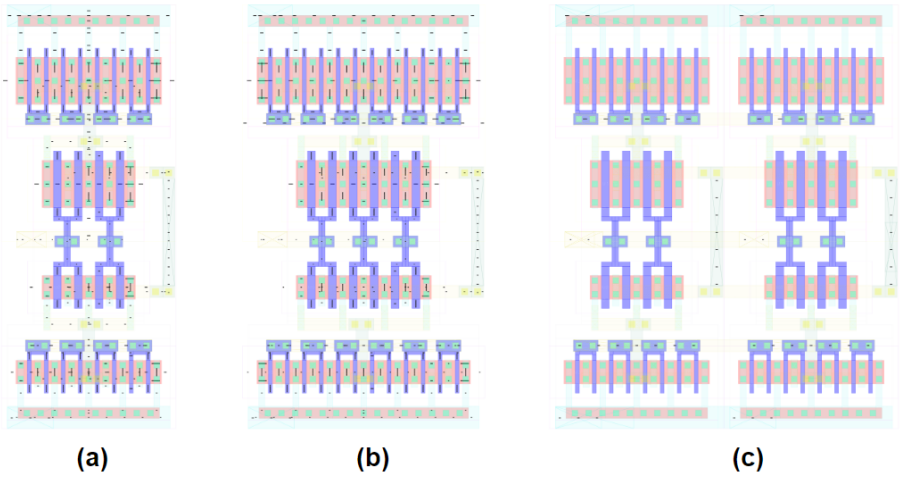

Figure 4.1 : Layout of (a) $1X$, (b) $1.5X$, and (c) $2X$ cells.

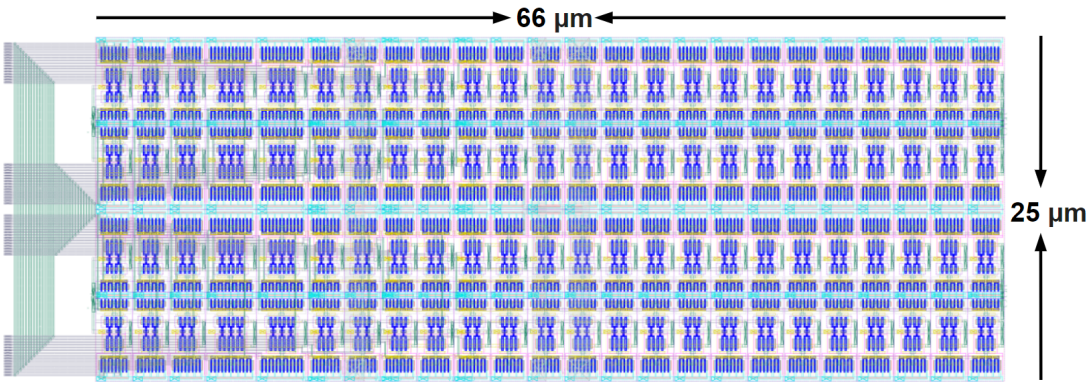

Figure 4.2 : Layout of the proposed VGA.

4.2 Testbench

Fig. 4.3 shows the testbench used for the simulations, which consists of three main parts. The first part is the VGA, which includes both the core of the VGA and the input bias cells. The second part is the replica biasing circuit, consisting of the LDO and the always-on reference cell. The third part handles the inputs and outputs. The signal inputs are applied differentially, with half of the signal applied to one input and the other half, in the opposite phase, applied to the other input. AC coupling capacitors, C_{coup}, are used because the bias for the input nodes does not come from input sources, but rather is generated by 1X diode-connected cells. The gain control code is applied to the Busset block, an ideal block implemented with Verilog-A code in the simulator, to convert the decimal input into binary bits. For example, to observe the gain versus gain code characteristic, the *Gain_code* variable is swept, and the corresponding binary bits are generated by the Busset block. Once the binary bits are created, they are applied to

the Binary-to-Thermometer (B2T) decoder block, which converts the binary bits into thermometric bits, as suggested by its name. This is because the gain control of the VGA is done using thermometric codes. The B2T block is implemented with standard logic gates, although it can also be implemented using Verilog-A, similar to the Busset block. Finally, the VGA outputs are differentially connected to the load capacitor, C_{load}, which has a value of 25 fF.

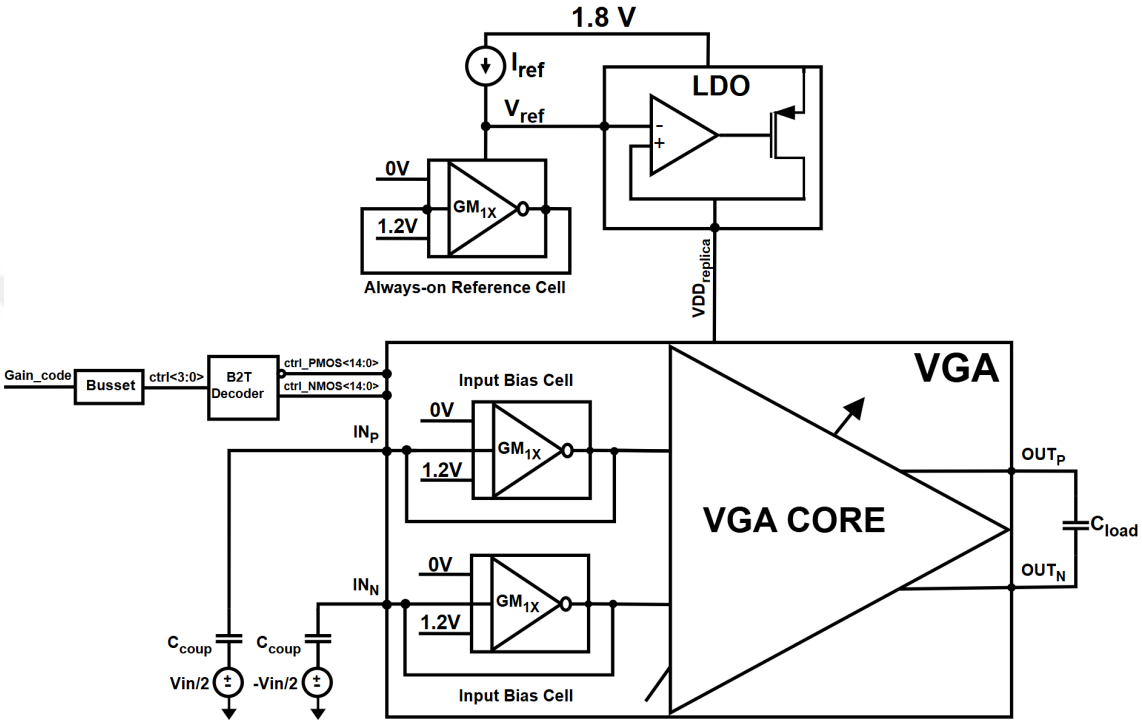

Figure 4.3 : Testbench for simulations.

4.3 DC Results

The primary objective of the results section is to demonstrate that the applied replica biasing method functions correctly and effectively. Table 4.1 serves as key evidence supporting this claim. The table presents the minimum, nominal, and maximum power consumption of the VGA across process corners, with and without the replica biasing circuit, at both minimum and maximum gain settings.

From the data, it is immediately clear that the variation in power consumption is excessive without replica biasing. The power consumption fluctuates dramatically at the maximum gain setting, ranging from 1.461 mW to 11.26 mW. Similarly, the

Table 4.1 : Power consumption across various PVT conditions.

Bias method	VGA Gain setting	Min power	Nominal power	Max power
Without replica bias	Min gain	808 μW	2.896 mW	6.34 mW
	Max gain	1.461 mW	5.18 mW	11.26 mW
With replica bias	Min gain	3.006 mW	3.015 mW	3.025 mW
	Max gain	5.265 mW	5.286 mW	5.297 mW

power consumption ranges from 808 μW to 6.34 mW at the minimum gain setting. These wide variations indicate poor stability in power consumption, which can hurt performance and reliability. However, when the replica biasing circuit is applied as the supply for the VGA, the power consumption variation is significantly reduced. With replica biasing in place, the variation at the minimum gain setting narrows to between 3.006 mW and 3.025 mW. At the maximum gain setting, it remains tightly clustered between 5.265 mW and 5.297 mW. This sharp reduction in variation underscores the effectiveness of the replica biasing method in stabilizing power consumption and, consequently, circuit performance across different process corners. These results strongly demonstrate that the replica biasing method is effective and plays a crucial role in reducing power consumption fluctuations, which directly contributes to improved performance and reliability of the VGA across varying process conditions.

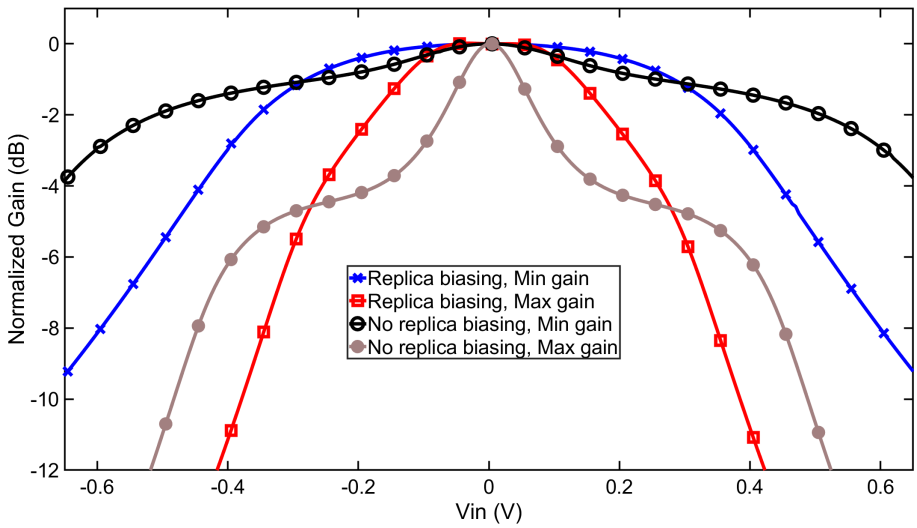

Figure 4.4 : Normalized gain vs. the input voltage under worst PVT conditions with/without replica bias.

Besides the power consumption table, Fig. 4.4 also demonstrates the effectiveness of the replica biasing method. It shows the normalized gain versus input voltage under

the worst-case PVT conditions, both with and without replica biasing, at maximum and minimum gain settings. The figure clearly shows that the input range with replica biasing is much wider than without, indicating better linearity, which also serves as further evidence of the effectiveness of replica biasing, supporting the results in Table 4.1.

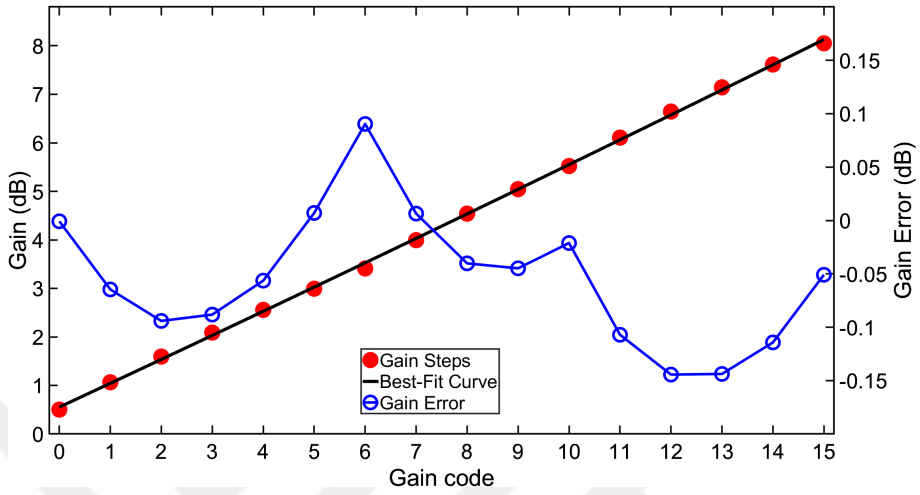

Figure 4.5 : Gain vs. gain code with best-fit curve and gain error.

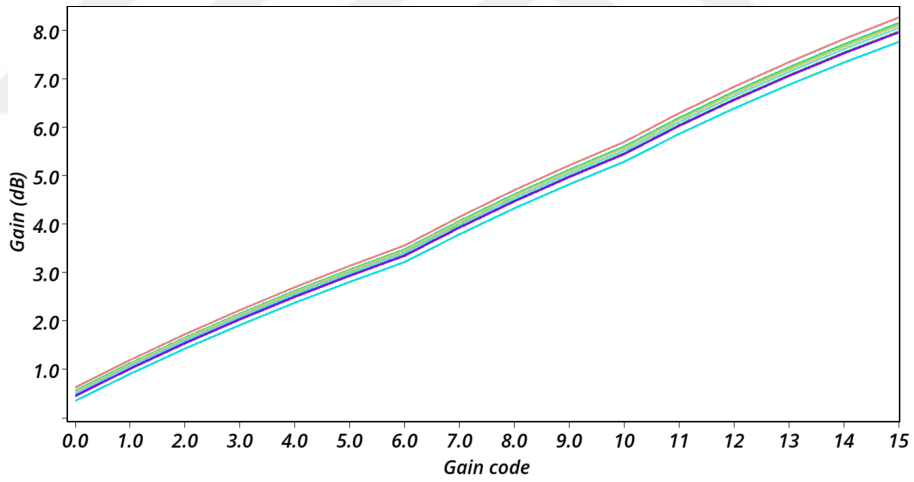

Figure 4.6 : Gain vs. gain code over corners.

Fig. 4.5 shows the gain steps of the VGA versus the gain code, along with the best-fit curve and the associated gain error. The figure illustrates that the VGA demonstrates an exceptionally linear gain characteristic, with the gain error remaining minimal, within ± 0.15 dB. Additionally, Fig. 4.6 presents the gain curve versus gain code across various process corners, highlighting minimal variation in gain with negligible

fluctuations between the corners. The minimum gain range of 7.41 dB occurs at the FF/1.9 V/120 °C process corner.

Figure 4.7 illustrates the DC voltage transfer characteristic as a gain function under nominal conditions, whereas Figure 4.8 presents this characteristic across different process corners. As observed, an increase in the gain code results in a narrowing of the linear range, whereas a decrease in the gain code leads to an expansion of the linear range.

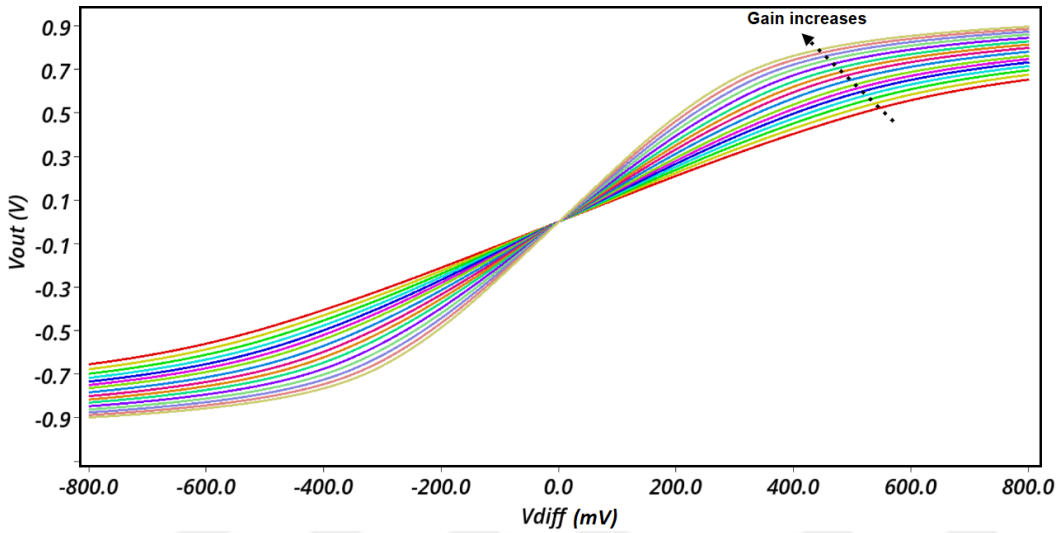

Figure 4.7 : DC voltage transfer characteristics for different gain codes.

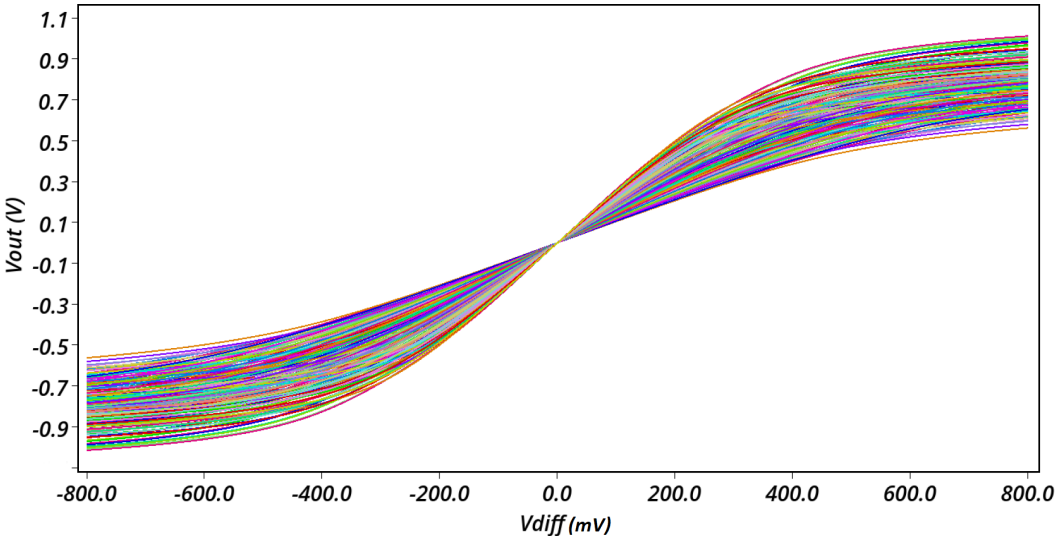

Figure 4.8 : DC voltage transfer characteristics for different gain codes across corners.

4.4 Frequency Response Results

Additionally, Fig. 4.11 shows the bandwidth as a function of gain code across these corners. The bandwidth exhibits minimal variation for the same process corner across different gain codes, ranging from 5.2 GHz to 5.31 GHz under nominal conditions. In the worst-case corner, SS/1.7 V/120 °C, the bandwidth ranges from 4.19 GHz to 4.26 GHz, indicating the impact of environmental and process variations on performance. Apart from the high-frequency poles given in (3.6) and (3.7), there is also a low cut-off frequency pole, as seen in Fig. 4.9 and Fig. 4.10, due to the coupling capacitors at the input. These coupling capacitors were added only for testing the VGA independently.

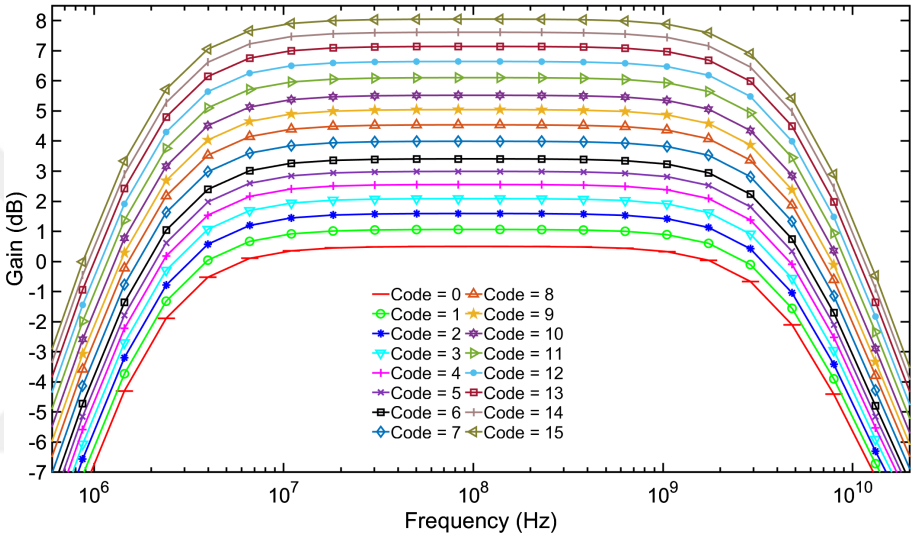

Figure 4.9 : Frequency response as a function of gain code.

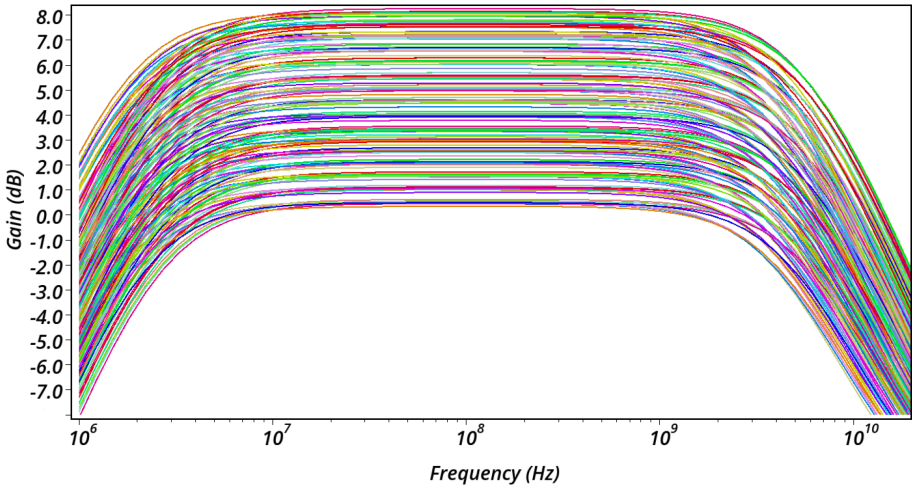

Figure 4.10 : Frequency response as a function of gain code over corners.

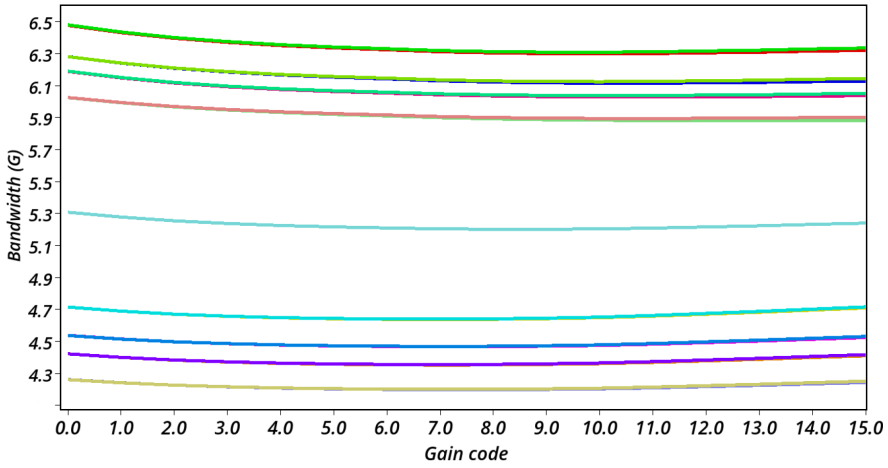

Figure 4.11 : Bandwidth as a function of gain code over corners.

Fig. 4.9 shows the frequency response for different gain codes under nominal conditions. Meanwhile, Fig. 4.10 depicts the frequency response as a function of gain code across various process corners, emphasizing the impact of process variations.

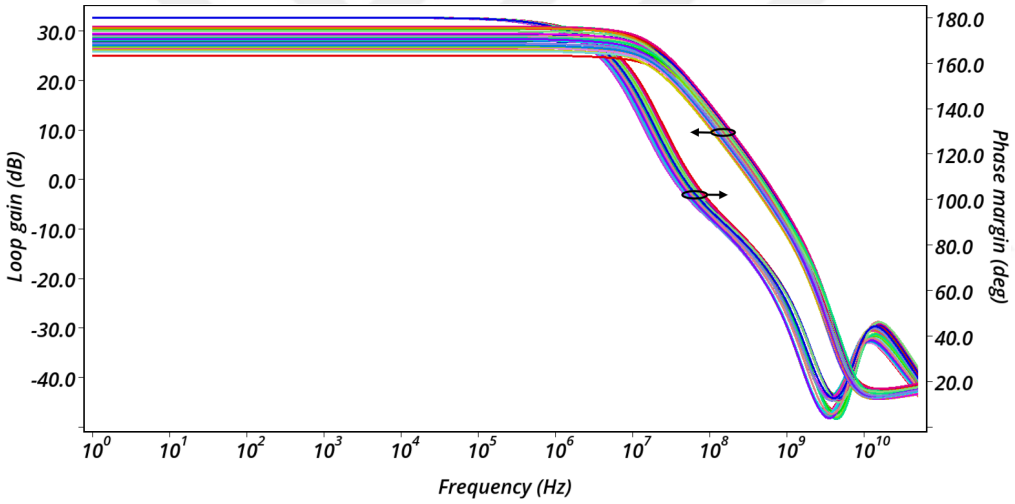

Figure 4.12 : Stability analysis of LDO loop across corners at maximum and minimum gain settings.

Additionally, Fig. 4.11 shows the bandwidth as a function of gain code across these corners. The bandwidth exhibits minimal variation for the same process corner across different gain codes, ranging from 5.2 GHz to 5.31 GHz under nominal conditions. In the worst-case corner, SS/1.7 V/120 °C, the bandwidth ranges from 4.19 GHz to 4.26 GHz, indicating the impact of environmental and process variations on performance. Apart from the high-frequency poles given in (3.6) and (3.7), there is also a low cut-off

frequency pole, as seen in Fig. 4.9 and Fig. 4.10, due to the coupling capacitors at the input. These coupling capacitors were added only for testing the VGA independently.

Fig. 4.12 illustrates the stability analysis of the LDO loop for both maximum and minimum gain settings across corners. Throughout all corners and gain settings, no stability issues are detected. Additionally, the phase margin consistently exceeds 65 ° across all gain settings and process corners.

4.5 Transient Results

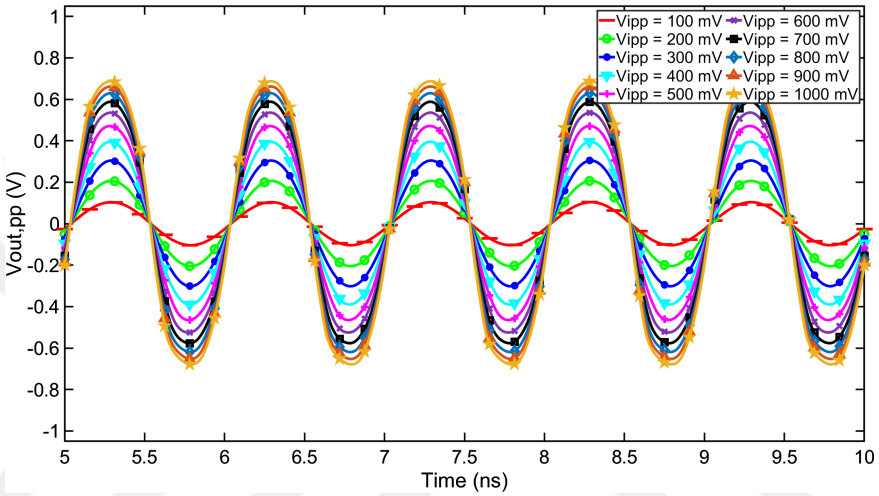

Figure 4.13 : Transient response of 1 GHz sinusoidal input at minimum VGA gain for various amplitudes.

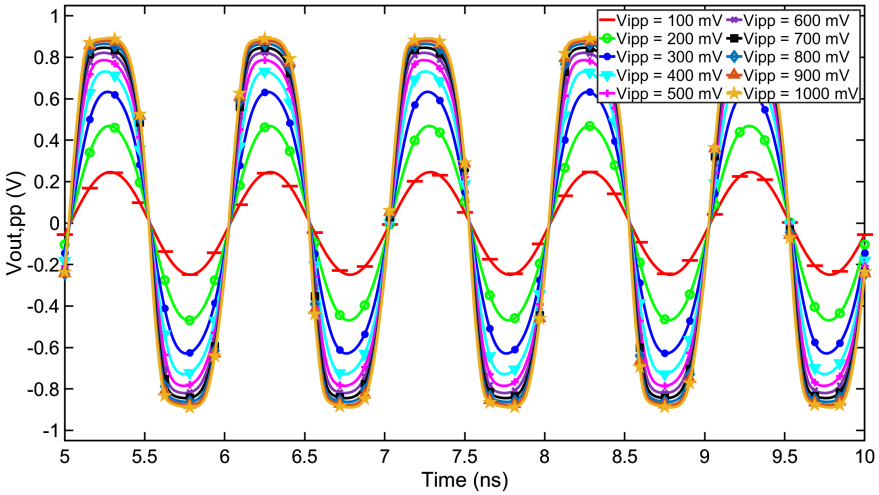

Figure 4.14 : Transient response of 1 GHz sinusoidal input at maximum VGA gain for various amplitudes.

Fig. 4.13 and Fig. 4.14 show the transient response for a 1 GHz sinusoidal input with various amplitudes at the minimum and maximum gain settings, respectively. Fig. 4.15 shows the peak-to-peak output voltage versus the peak-to-peak input voltage for the same sinusoidal signal for both the maximum and minimum gain settings. As can be seen, the VGA linearly amplifies the signal up to output swings of approximately 1.2 V, which is a strong indicator of high linearity.

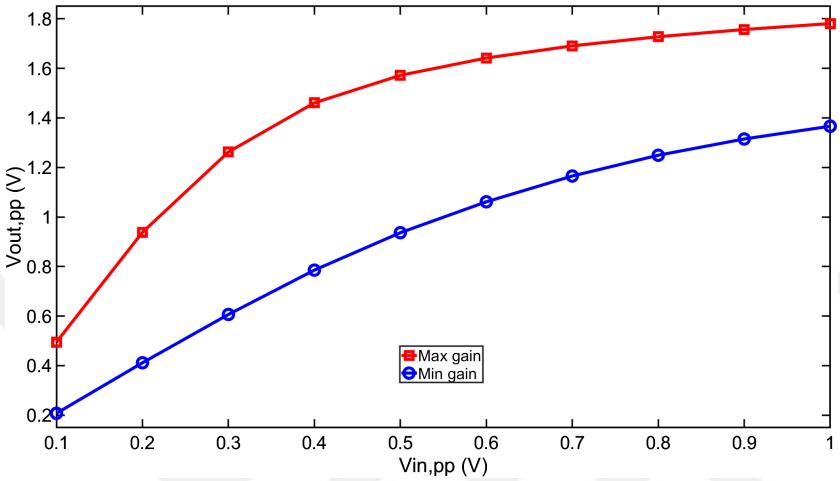

Figure 4.15 : Peak-to-peak output voltage vs. peak-to-peak input voltage for 1 GHz sinusoidal input.

4.6 Distortion and Eye Diagram Results

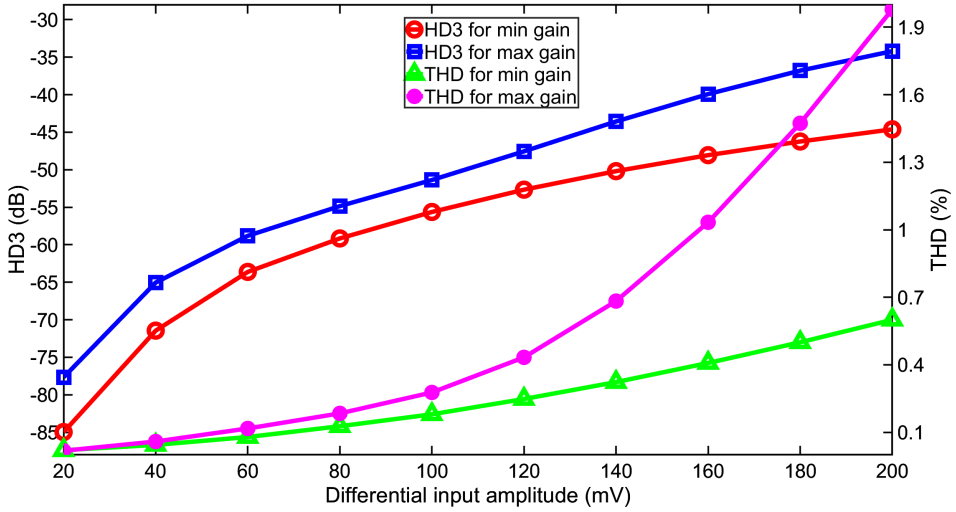

Figure 4.16 : HD3 and THD over input amplitudes.

For linearity analysis, HD3, THD, and eye diagram simulations were conducted. A sinusoidal signal with a frequency of 1 GHz and an amplitude sweep ranging from

20 mV to 200 mV was applied, and the output frequency spectrum was analyzed to calculate the HD3 and THD values for each amplitude. The results of these calculations are shown in Fig. 4.16. The worst HD3 values are -34.2 dB and -44.62 dB for the maximum and minimum gain settings, respectively, occurring at the highest amplitude of 200 mV. Similarly, the worst THD values are 1.97% and 0.6% for the maximum and minimum gain settings, further confirming the VGA's high linearity.

Eye diagrams were also analyzed to assess the signal integrity. Fig.4.17 displays the NRZ eye diagram for a 1 Gbps input, Fig. 4.18 shows the NRZ eye diagram for a 5 Gbps input, and Fig.4.19 illustrates the NRZ eye diagram for a 10 Gbps input, all with a peak-to-peak input amplitude of 400 mV at the maximum gain setting.

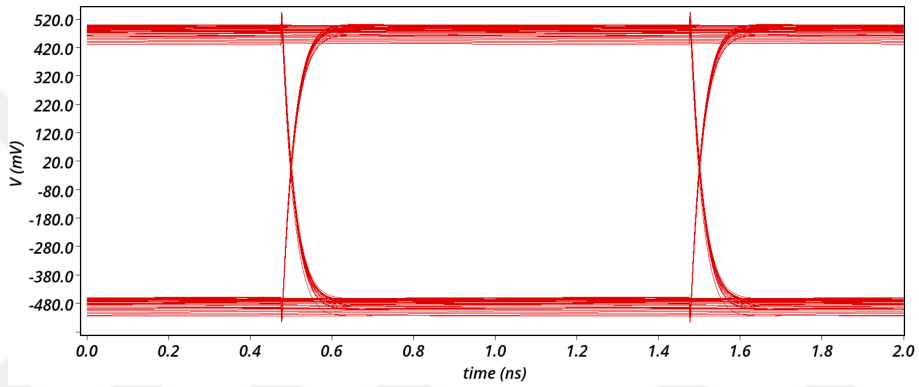

Figure 4.17 : NRZ eye diagram for 1 Gbps input at maximum gain setting.

A similar approach was followed for the PAM-4 eye diagrams, using a 400 mV input amplitude at three different data rates: 1 Gbps, 5 Gbps, and 10 Gbps. The corresponding eye diagrams are shown in Fig. 4.20, Fig. 4.21, and Fig. 4.22.

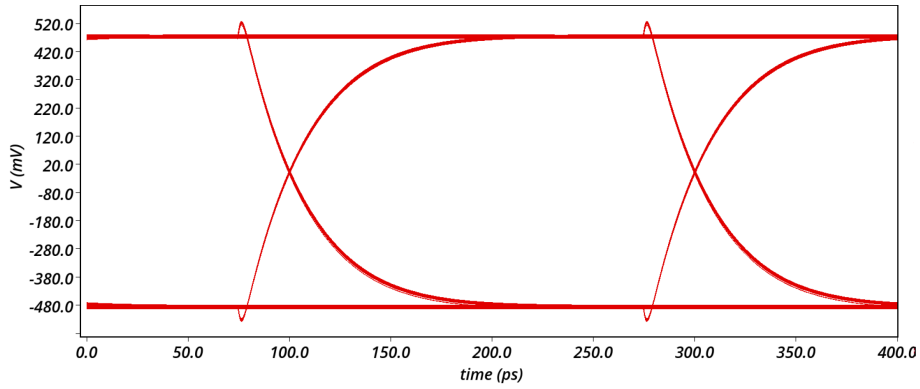

Figure 4.18 : NRZ eye diagram for 5 Gbps input at maximum gain setting.

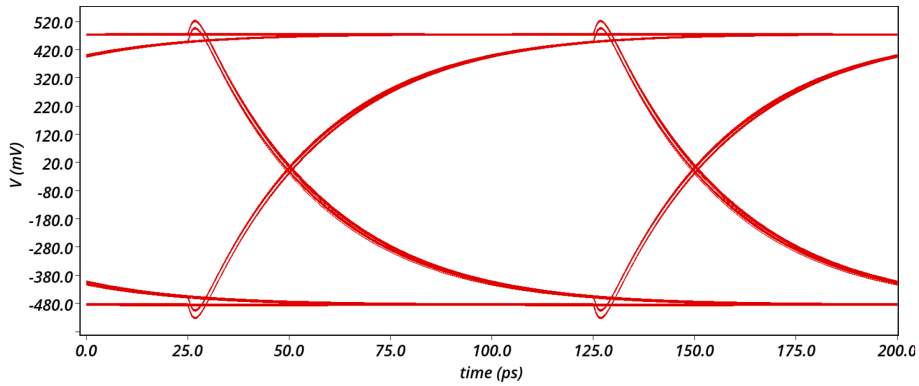

Figure 4.19 : NRZ eye diagram for 10 Gbps input at maximum gain setting.

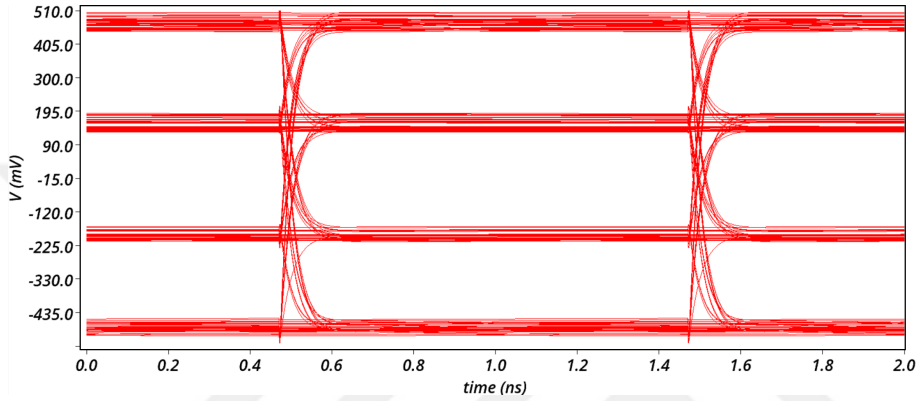

Figure 4.20 : PAM-4 eye diagram for 1 Gbps input at maximum gain setting.

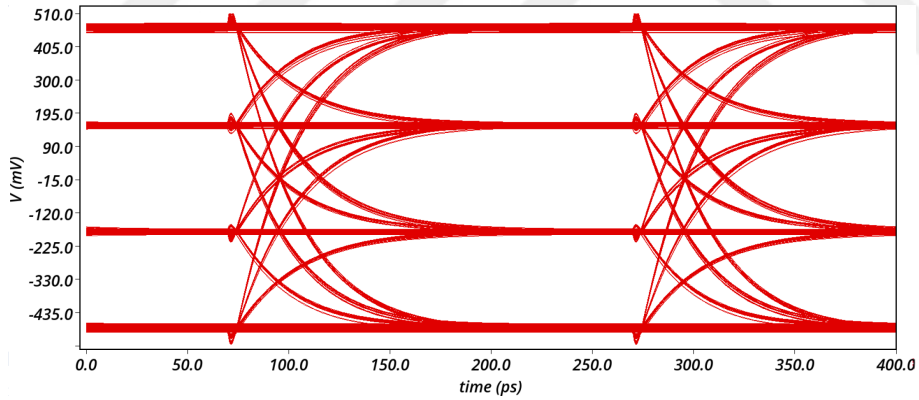

Figure 4.21 : PAM-4 eye diagram for 5 Gbps input at maximum gain setting.

The eye openings in both the NRZ and PAM-4 eye diagrams are wide and high, indicating excellent performance in terms of intersymbol interference (ISI) and minimal signal degradation. Moreover, the similar eye heights across the different PAM-4 levels highlight the VGA's excellent linearity across various modulation schemes. The VGA performs effectively even at a 10 Gbps PAM-4 input, demonstrating its capability for high-speed data transmission.

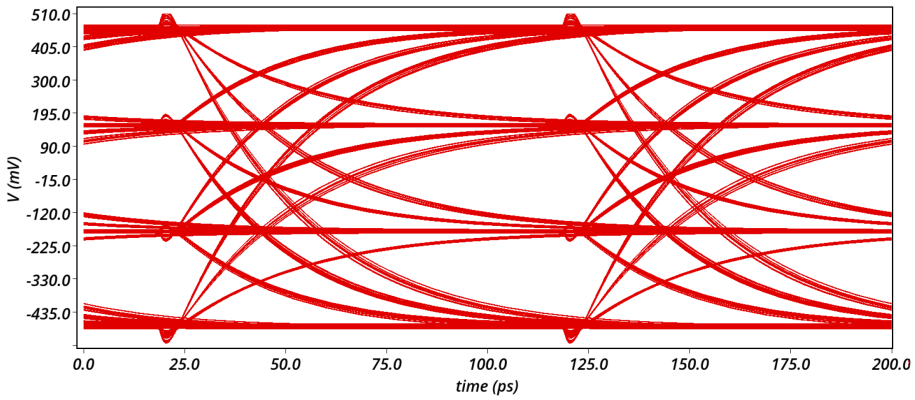

Figure 4.22 : PAM-4 eye diagram for 10 Gbps input at maximum gain setting.

4.7 Noise Results

Fig. 4.23 illustrates the input-referred noise at both maximum and minimum gain settings, while Fig. 4.24 presents the corresponding noise figure (NF) across process corners for these gain settings. In the nominal case, the input-referred noise is 1.26 nV at maximum gain and 2.3 nV at minimum gain at 1 GHz under typical conditions. The RMS input noise integrated from 10 MHz to 5 GHz is 89 μV at maximum gain and 162 μV at minimum gain. The average NF over the same frequency range is 4.76 dB for the maximum gain setting and 8.8 dB for the minimum gain setting. These results indicate that the proposed VGA provides satisfactory noise performance.

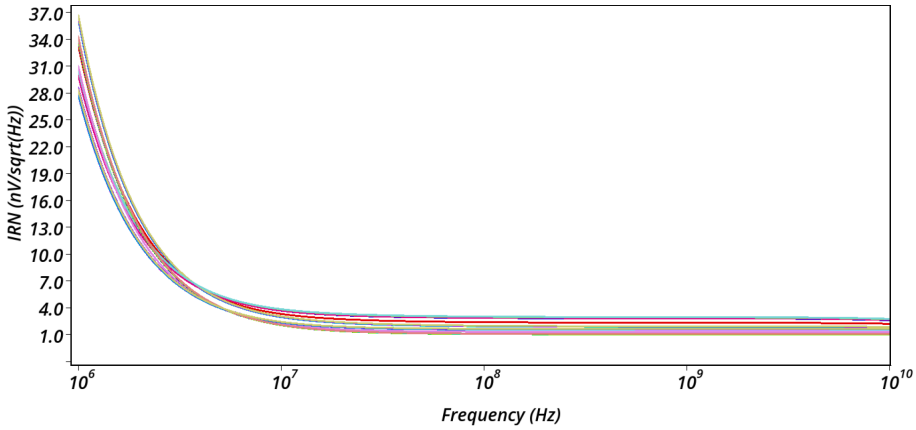

Figure 4.23 : Input-referred noise at maximum and minimum gain settings over corners.

4.8 Worst-Case Corner Performance Summary

Table 4.2 summarizes the performance of the designed VGA under worst-case corner conditions. The table presents the corresponding worst-case corner condition for

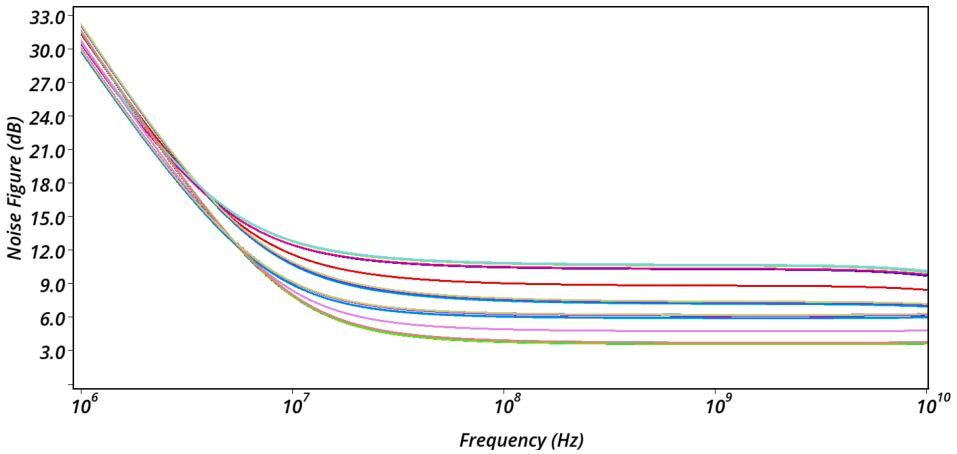

Figure 4.24 : Noise figure at maximum and minimum gain settings over corners.

each design specification and the resulting performance metrics under those specific conditions.

Table 4.2 : Performance summary at the worst corners.

Specification	Worst PVT Case	Value	Unit
Input range for 0.5 dB compression at maximum gain	FF, 1.7 V, 120 °C	432	mV
Input range for 0.5 dB compression at minimum gain	FF, 1.7 V, −40 °C	213	mV
Gain range	FF, 1.9 V, 120 °C	7.41	dB
Bandwidth range	SS, 1.7 V, 120 °C	4.19 - 4.26	GHz
HD3 for 100 mV (pk), 1 GHz input at maximum gain	FS, 1.9 V, −40 °C	−48.17	dB
HD3 for 100 mV (pk), 1 GHz input at minimum gain	FS, 1.9 V, −40 °C	−51.9	dB
THD for 100 mV (pk), 1 GHz input at maximum gain	FS, 1.9 V, −40 °C	0.42	%
THD for 100 mV (pk), 1 GHz input at minimum gain	FS, 1.9 V, −40 °C	0.27	%
Integrated RMS input noise up to 5 GHz, at maximum gain	SS, 1.7 V, 120 °C	113	μV
Integrated RMS input noise up to 5 GHz, at minimum gain	SS, 1.7 V, 120 °C	206	μV

5. CONCLUSIONS

This thesis presents the design and implementation of an inverter-based VGA tailored for PAM-4 optical receivers, with potential applicability to other systems and applications. The primary objective was to achieve high linearity to meet the stringent demands of PAM-4 modulation. The research begins with a comprehensive literature review, emphasizing the advantages of multi-level PAM schemes over NRZ formats and exploring various VGA topologies and linearity-driven design techniques. The insights from prior studies guided the adoption of the inverter-based g_m/g_m architecture for its superior linearity, bandwidth, signal swing capability, low noise, and compact design.

The designed VGA employs 15 thermometric bits to ensure a monotonic characteristic. Through iterative design, the VGA achieved significant advancements, including the incorporation of larger g_m cells to mitigate gain saturation at higher gain codes and the implementation of fixed load cells to ensure consistent bandwidth across all gain settings. A replica biasing scheme utilizing an LDO was employed to address PVT variations, stabilizing the VGA's performance under varying conditions. The final design achieved a compact layout with dimensions of 66 μm $\times$ 25 μm.

Post-layout simulations revealed that the VGA offers a gain range of 7.5 dB with precise linear steps of 0.5 dB, minimal gain error within $\pm$0.15 dB, and a power consumption of 5.29 mW at the maximum gain setting. The design maintained a stable 5.2 GHz bandwidth across all gain settings. A sinusoidal signal at a 1 GHz frequency with various amplitudes was applied for linearity analysis. HD3 values were below -50 dB for a 100 mV input amplitude and below -34 dB for a 200 mV input amplitude for all gain settings. Additionally, the THD remained below 0.3% for a 100 mV input amplitude and below 2% for a 200 mV input amplitude across all gain codes. This demonstrates high linearity and minimal distortion. The VGA demonstrated low noise performance, with an IRN of 1.26 nV at maximum gain, 2.3 nV at minimum gain

at 1 GHz, and an average NF of 4.76 dB at maximum gain and 8.8 dB at minimum gain. Stability analysis of the LDO loops confirmed reliable operation across all gain modes and process corners. Eye diagram simulations conducted at data rates of 1 Gbps, 5 Gbps, and 10 Gbps further validated the high linearity and low ISI of the design, affirming its effectiveness for PAM-4 modulation.

A comparison of the designed VGA with existing solutions in the literature, presented in Table 5.1, illustrates its competitive performance in terms of gain control, linearity, bandwidth, and noise characteristics.

In conclusion, the proposed inverter-based VGA offers a compact and high-performance solution for PAM-4 optical receivers. With precise gain control, consistent bandwidth, high linearity, and low noise characteristics, it proves to be a reliable and efficient choice for optical receivers and a wide range of other applications. As a result, there is significant potential for a substantial increase in the use of inverter-based analog circuits across various fields, including wireless, wireline, and optical communication. As future work, the applicability of the designed VGA to PAM-8 modulation will be examined and evaluated to determine its potential for even higher-order modulation schemes.

Table 5.1 : Comparison of the proposed VGA with existing literature

Design	**[48]**	**[49]**	**[50]**	**Proposed**
CMOS Technology	28 nm FDSOI	28 nm FDSOI	40 nm	65 nm
Gain Range/Error (dB)	14/ -	7.4/ -	51/ $\pm$1	7.5/ $\pm$0.15
Bandwidth (GHz)/ Constant	15/ no	3.6/ no	7/ yes	5.2/ yes
Noise (IRN)/NF	300 μV (rms)	5.9 dB	30.5 dB	88 μV (rms) /4.7 dB
Linearity	–	$-$54 dBm (IM3)	$-$8 dBm (OP1dB)	$-$51 dB (HD3)
Power/Supp. (mW/V)	32/1	22.5/1.5	27.06/1.1	5.28/1.8
Area (mm^2)	0.0975	1 (whole chip)	0.038	0.00165

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