POWER AWARE SWITCHED CAPACITOR INTEGRATOR DESIGN

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ABSTRACT

POWER AWARE SWITCHED CAPACITOR INTEGRATOR DESIGN

Switched Capacitors are used as resistors because they have better accuracy and they consume less die area than other resistor implementations in integrated circuits. In this technique, a capacitor is charged and discharged in order to transfer charge. This charge transfer is related to switching speed and the value of the capacitance. Transferring charge from one node to other the one with switching gives the ability to control the charge transfer rate in a given time which means controlling the current. Changing the current between two nodes means changing resistance between these two nodes. The value of this capacitance determines the total charge transferred in one switching cycle and how frequently repeating this charging and discharging determines total charge transferred from one node to the other node.

Another application of switched capacitor circuits is integrators, transfer ratio between output and input is determined with the ratio of the integrating capacitor over switching capacitor and switching frequency. Switching frequency can be easily controlled and capacitor ratio can also be easily controlled as a multiple of standard capacitors. In this way, switch capacitor integrator can be designed with not too much effort and without trying to adjust input resistor.

Designing from switching part to overall switched capacitor integrator, each part will be analyzed in detail to examine which parameters affect on circuits performance. Initially circuit is realized with ideal elements. Then it is realized with the real IC counterparts. Finally switching is analyzed as charge and discharge events to understand which parameters affect the limits of the switching stage and transferred to the second stage.

At integrator part, Miller OTA configuration is analyzed to find a solution which will be good enough given input signals, gain, bandwidth and power requirements. During this

design phase, power consumption is critical to increase the efficiency of the overall circuit. Because most of the power consumption of the circuit is from opamp or OTA part, thus lowering the power of this part is very important.

ÖZET

GÜÇ TÜKETİMİ ODAKLI ANAHTARLAMALI KONDANSATÖR TÜMLEYİCİ TASARIMI

Anahtarlamalı kondansatörler diğer direnç uygulamalarına göre daha hassas direnç değerleri ve daha az kırmık alanı kullanması nedeniyle kullanılırlar. Bu yöntemde bir kondansatör şarj ve deşarj edilerek yükün bir yerden başka bir yere aktarılması sağlanır. Bu yük transferi anahtarlama hızına ve kondansatör değerine bağlı olarak değişmektedir. Bir düğümden başka bir düğüme belli bir süre içinde yük aktarımını kontrol etmek akımı kontrol etmek anlamına gelir. İki düğüm arasındaki akımı değiştirmek de o iki düğüm arasındaki direnci değiştirmek anlamına gelir. Bu kondansatörün büyüklüğü bir anahtarlama süresi içinde ne kadar yük aktarılacağını belirler ve anahtarlama sıklığı da toplamda ne kadar yük aktarımı yapıldığını belirler.

Anahtarlamalı kondansatörlerin başka bir avantajı da çıkışla giriş arasındaki oran tümleme kapasiteyle anahtarlama kapasitesi ve anahtarlama sıklığıyla orantılıdır. Anahtarlama sıklığı ve kondansatör oranı kolaylıkla kontrol edilebilir. Bu yöntemle anahtarlamalı kondansatör tümleme işlemi giriş direncini ayarlamayla uğraşmadan ve çok fazla çaba gerekmeden yapılır.

Genel olarak anahtarlamalı kondansatörden tümleyiciye kadar bütün devre kısımları incelenerek gerçek devreyle tasarlanan devre arasındaki fark azaltılmış olacaktır. İlk olarak ideal devre kullanılıp ardından gerçek entegre devre eşlenikleriyle gerçeklenmiştir. Ardından anahtarlama işlemi şarj ve deşarj olarak incelenerek hangi değişkenlerin anahtarlamayı etkilediği ve bir sonraki kısıma aktarıldığı incelendi.

Tümleyici kısmında Miller OTA devresi araştıralarak belirli kazanç ve bant genişliği değerleri için istenilen güç için çözüm araştırıldı. Bu dizayn sürecinde güç tüketimi verimliliği kritik olarak devrenin verimliliğini arttırma da önemlidir. Çünkü harcanan

gücün büyük bir kısmı bu tümle bölümündeki opamp ve OTA da harcanmaktadır, bu nedenle bu bölümün güç tüketiminin azaltılması çok önemlidir.

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LIST OF SYMBOLS/ABBREVIATIONS

CMOS	Complementary Metal-Oxide Semiconductor
IC	Integrated Circuit
NMOS	N-Channel Metal-Oxide Semiconductor
PMOS	P-Channel Metal-Oxide Semiconductor
OTA	Operational Transconductance Amplifier
SC	Switched Capacitor

1. INTRODUCTION

Due to the technological improvements in IC technology, channel lengths are very small in CMOS technology. These short channel devices are quite difficult to model because many design parameters show up and hand calculations and actual behavior become inconsistent. Without having accurate hand calculations, the designed circuit and actual circuit behave very differently. In this thesis, the gap between desired and actual design has been tried to be minimized.

In conventional IC design, building a resistor with a given accuracy is difficult. Switched capacitor circuits are used in IC design, because they have accurate equivalent resistor values which can be easily adjusted by capacitor value and switching frequency. Another disadvantage of building a resistor in IC is that it consumes much chip area. Switch capacitor circuits consume less chip area compared to conventional resistor implementations.

Switched capacitors are used in integrator applications which are basic building blocks of active filters. Capacitor ratio in switched capacitor integrators makes switched capacitors the best candidate for having less mismatch errors. Transfer function of a switched capacitor integrator is given by

$$\frac{V_{out}(\mathrm{t})}{V_{in}(t)} = \frac{C_s . f_s}{C_{\mathrm{int}} . 2\pi f} \tag{1.1}$$

2. SWITCHED CAPACITOR

2.1. Basic Principle

Switched capacitor circuits basically consist of a capacitor, switching signals and switches. In this technique, the capacitor is charged and discharged during different clock cycles and charge is transferred from one node to the other. Charge transfer rate in a given time is related with the speed of charging and discharging as well as the capacitor value. During the charging cycle, the switch which connects the capacitor with the source signal is in the on state with its appropriate clock signal. The capacitor is charged to the input source signal. Then, this switch turns off and the other switch which connects capacitor to the output node turns on with the appropriate clock signal. The charge which was stored in the previous cycle discharges from output node path to the ground.

As explained above, switches are assumed to be ideal. With this ideal assumption charging and discharging time will be ideally zero. However, in practice, these switches are formed with transistors which have resistance. Charging and discharging events are affected by this resistance. Increasing the transistor sizes will cause decreasing of the resistance; however, it will cause an increase of the parasitic effects such as charge injection and clock feedthrough. Another important issue is that, charging and discharging time must be ideally infinite; however, in practice charging or discharging to 99.9 % of the desired value is accepted to be enough.

During these charging and discharging cycles, the total charge transferred in a given time will be determined by how fast the charge transfer rate is and how big this capacitor is. Switching speed and capacitor value affect the equivalent resistance because, if the transfer rate becomes faster, the transferred charge increases and if the capacitor gets bigger, then the charge which is transferred within one cycle gets larger. Thus, switching rate and capacitor value determine the amount of charge which is transferred from one node to the other in a given time. Changing charge transfer rate between two nodes in a given time means changing current and also changing resistance. Thus, controlling the charge transfer rate means controlling the resistance.

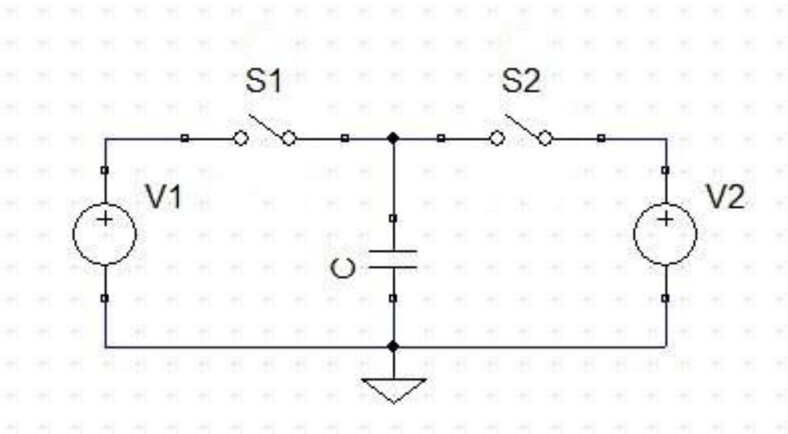

Figure 2.1. Basic Switched Capacitor

2.1.1. Mathematical Expression

Between two nodes which have voltage values V1 and V2 stored charge at capacitance is given by

$$\Delta Q = C_s \Delta V = C_s (V_1 - V_2) \tag{2.1}$$

If this charge transfer is repeated n times, or specifically F_{CLK} times the transferred charge is

$$\Delta Q.F_{CLK} = F_{CLK} C_s (V_1 - V_2) \tag{2.2}$$

$$I = \frac{\Delta Q}{\Delta t} \quad \Rightarrow I = \frac{\Delta Q}{T} = \Delta Q.F_{CLK} \tag{2.3}$$

$$I = F_{CLK} C_s (V_1 - V_2) \tag{2.4}$$

$$\frac{(V_1 - V_2)}{I} = R_{eq} \Rightarrow \frac{(V_1 - V_2)}{I} = \frac{1}{F_{CLK} C_s} = R_{eq} \tag{2.5}$$

3. CHARGING AND DISCHARGING A CAPACITOR

3.1. Charging a Capacitor

Since switched capacitor circuits are based on charging and discharging a capacitor, these events will be analyzed in detail in this section. In charging –with the assumption that there is no charge on the capacitor initially- the capacitor will charge up to the voltage of the input source; however, this charging will not be linear because the rate of charging is proportional to the voltage difference which is changing with time. However, in practice charging will be done after a couple of time constants which is the product of the charging path resistance with the capacitor's value. In general, five time constants (5RC) are accepted enough in mostly settling conditions. However, especially in switched capacitor circuits, eight time constants will be accurate enough to accept that the capacitor is charged and the conditions are stable. Error and time constant relation is given by

$$e^{-\frac{t}{RC}} \Rightarrow e^{-\frac{5RC}{RC}} = 0.006737 \quad \text{results 0.6 \% error}$$

0.1 % error is accepted to be enough accurate in most cases

$$e^{-\frac{t}{RC}} = 0.001 \Rightarrow t = 6.9RC \quad \text{for calculation simplicity t=8RC error=0.000335}$$

A simple circuit for capacitor charging is depicted in Figure 3.1.

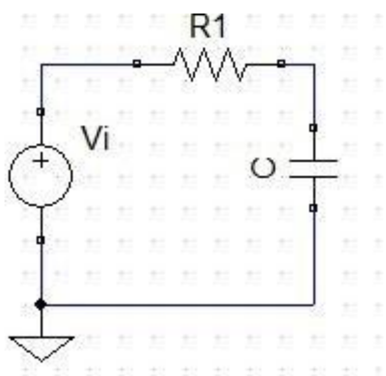

Figure 3.1. Charging a Capacitor

Voltage of the capacitor during charging is

$$V_i = RI + V_c \qquad I = C\frac{dV_c}{dt} \qquad V_i = RC\frac{dV_c}{dt} + V_c \qquad \Rightarrow \qquad V_c = Ae^{-\frac{t}{RC}} + B \tag{3.1}$$

$$V_i = Ae^{-\frac{t}{RC}} + B + ARC(-\frac{1}{RC})e^{-\frac{t}{RC}} \qquad \Rightarrow \qquad \text{B}=V_i \qquad V_c = Ae^{-\frac{t}{RC}} + V_i \tag{3.2}$$

$$\Rightarrow \quad \text{boundary conditions} \quad t = 0 \quad \& \quad V_c = 0$$

$$0 = Ae^0 + V_i \qquad A = V_i \qquad \Rightarrow \qquad V_c = V_i e^{-\frac{t}{RC}} + V_i \qquad \Rightarrow \qquad V_c = V_i(1 - e^{-\frac{t}{RC}}) \tag{3.3}$$

3.2. Discharging a Capacitor

Discharging a capacitor through a resistor starts with the same voltage on the capacitor as initial state. Then, its charge flows through the resistor and decreasing both voltage and charge on the capacitor. Initially, the voltage difference is maximal which causes the maximal charge flowing through resistor. When voltage difference becomes small, the charge flow will be low causing complete discharging to last infinitely long; however, in practice again, eight time constants are enough to be accepted to be completely discharged. A circuit for discharging a capacitor is depicted in Figure 3.2.

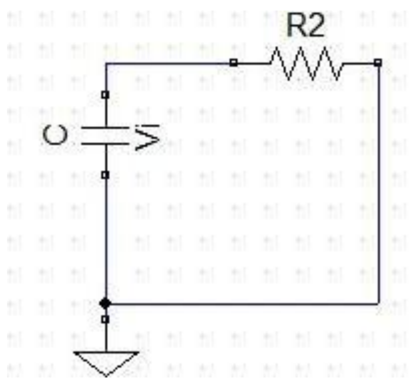

Figure 3.2. Discharging a Capacitor

The voltage of the capacitor during discharging is

$$I = C\frac{dV_c}{dt} \qquad I = \frac{V_c}{R} = C(-\frac{dV_c}{dt}) \qquad V_c + RC\frac{dV_c}{dt} = 0 \qquad V_c = Ae^{-\frac{t}{RC}} \tag{3.4}$$

$\Rightarrow$ boundary conditions $t = 0$ & $V_c = 0$ $\rightarrow$ $V_i = Ae^0$ $A = V_i$

$$V_c = V_i e^{-\frac{t}{RC}} \tag{3.5}$$

4. ENERGY CALCULATIONS FOR SPICE

The main aim of this work is to reduce the power consumption in switched capacitor circuits and therefore power calculations and simulations will be very important. To find the relation of power with the biasing of the circuit will be the key feature of this thesis; however, switching activity causes simulators to miscalculate the actual power. To observe the relation between biasing and power and to compare with the simulator outputs, a simple circuit is built for energy calculation **[**1**]**. Since power is the derivative of the energy with respect to the time, energy calculations will be enough to achieve power measurements. Total energy consumed by the circuit will be used to find average power consumption of the circuit. The circuit which calculates power is depicted in Figure 4.1.

Using a capacitor as current integrator, voltage of the capacitor will be the energy consumed by circuit. For this purpose, the voltage difference of a circuit and its current is multiplied and it is used as dependent current source. Then, this is applied to the capacitor with this current controlled current source. For avoiding a singular matrix error in spice, a very big resistance is connected in parallel to the capacitor.

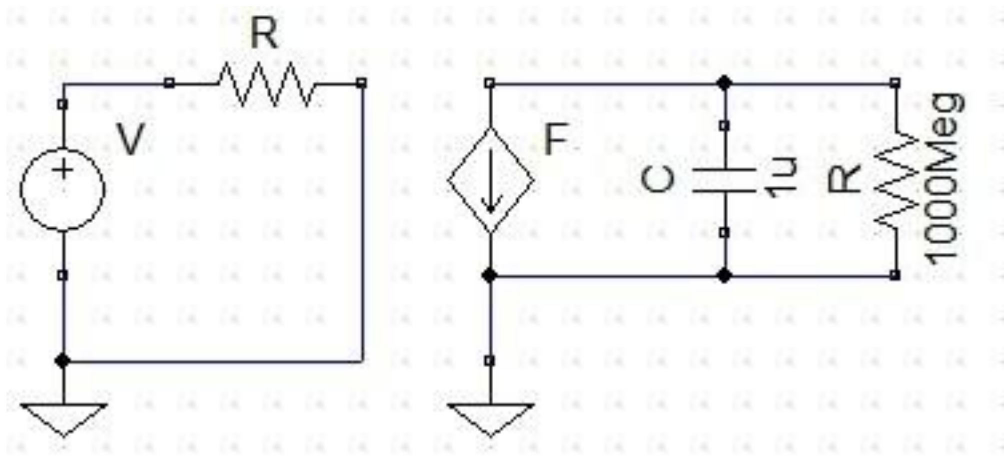

Figure 4.1. Energy Calculation circuit

$$i = C\frac{dV}{dt} \tag{4.1}$$

$$CdV = idt \tag{4.2}$$

$$V = \frac{1}{C}\int k.idt \tag{4.3}$$

$$\frac{k}{C}\int idt = Ve \tag{4.4}$$

$$\Rightarrow k = C \tag{4.5}$$

Energy calculations for spice can be seen in Figure 4.2.

Energy calculation for Hspice:

```
vin 1 0 pulse (0V 1V 10ns 10ns 10ns 999us 1ms)
vs 1 2 0
rl 2 0 1k
fcr pf 0 vs 1
rfc pf 0 1
energy ep 0 vol='(v(2)*v(pf)*1e-6)'
vvtc ep epn 0
rpe epn 0 1
fint intp 0 vvtc 1
vint intp intn 0
cint intn 0 1u
rint intn 0 100000meg
```

Energy calculation for Winspice:

```
b9 98 0 i=0.000001*(v(x)-v(y))*i(vi)
v99 98 99 0
c9 99 0 1u
r9 99 0 1000000meg
```

Figure 4.2. Energy Calculations for Spice

4.1. Energy During Charging and Discharging

During both charging and discharging some part of the energy is dissipated and some is transferred to the output. If the timing conditions are suitable for both charging and discharging, half of the energy is dissipated on the charging path and the other half is transferred to the output.

4.2. Switched Capacitor Circuit's Energy

A simple sinusoidal signal which has maximum value of Vm is applied as seen in Figure 4.3., the energy stored at the capacitance and the energy dissipated at the switches are calculated.

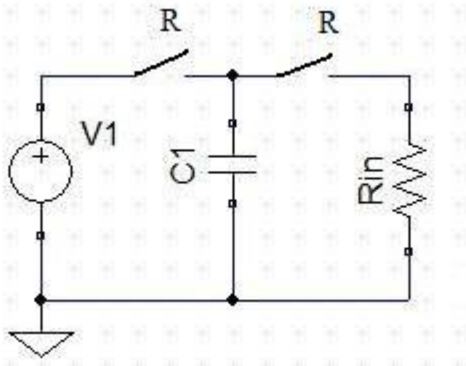

Figure 4.3. Simple Switched Capacitor circuit

In a charging cycle, the energy is dissipated on $R_{\text{charging path}}$ in one cycle is given by

$$\int (\frac{Vm.e^{-\frac{t}{RC_s}}}{\sqrt{2}})^2 \frac{1}{R_{\text{charging path}}} dt = \frac{Vm^2 e^{-\frac{2t}{RC_s}}}{2} \frac{1}{R} \frac{RC_s}{2} \left[0, Tsw\right] = \frac{Vm^2}{2} \frac{1}{R} \frac{RC_s}{2} = \frac{Vm^2.C_s}{4} \qquad (4.6)$$

Energy dissipated during charging = Energy stored on capacitor = Energy dissipated during discharging

$$E_{total} = E_{charging} + E_{discharging} \qquad \Rightarrow \quad 2.\frac{Vm^2}{2} \frac{1}{R} \frac{RC_s}{2} = \frac{Vm^2}{2} \frac{1}{R} RC_s = \frac{Vm^2}{2} C_s \qquad (4.7)$$

Continuous time Equivalent Resistor:

$$\int (\frac{Vm}{\sqrt{2}})^2 \frac{1}{R_{eq}} dt = \frac{Vm^2}{2} \frac{1}{R_{eq}} t\left[0, T_{\text{input signal}}\right] = \frac{Vm^2}{2} \frac{1}{R_{eq}} T_{\text{input signal}} \qquad (4.8)$$

Switched Capacitor and Equivalent Resistor:

$$\frac{Vm^2}{2} \frac{1}{R} RC_s \frac{T_{\text{input signal}}}{T_{\text{switching signal}}} = \frac{Vm^2}{2} \frac{1}{R_{eq}} T_{\text{input signal}} \qquad (4.9)$$

$$\frac{1}{R} RC_s \frac{1}{T_{\text{switching signal}}} = \frac{1}{R_{eq}} \qquad \Rightarrow R_{eq} = \frac{T_{\text{switching signal}}}{C_s} \qquad (4.10)$$

To verify these results, the energy dissipated of a simple Switched Capacitor circuit is calculated and simulated with the spice energy sub circuit. A sine signal applied with a 5V maximum amplitude with 50 μs period, a 1 nF capacitance and 1 MΩ Rin resistance is used.

$$Ec \rightarrow \quad Vc = Vie^{-\frac{t}{RC}} \quad ic = \frac{Vie^{-\frac{t}{RC}}}{Rin + R} \quad Rin \gg R \quad Rin + R \cong Rin \tag{4.11}$$

$$Ec = \int Vie^{-\frac{t}{RC}} . \frac{Vie^{-\frac{t}{RC}}}{R} dt = \int \frac{Vi^2 e^{-\frac{2t}{RC}}}{R} dt = \frac{Vi^2 e^{-\frac{2t}{RC}}}{R} \frac{-RC}{2} \left[0, 50u\right] = \frac{CVi^2 e^{-\frac{2t}{RC}}}{2} \tag{4.12}$$

$$10^{-9} \frac{25}{2} (1 - e^{-\frac{2.50.10^{-6}}{10^6.10^{-9}}}) = 12,510^{-9} (1 - 0,904) = 1,19nJ \quad \text{in simulation} \quad 1,1994\text{nJ} \tag{4.13}$$

5. OPAMP DESIGN

5.1. Ideal Opamp

For simplicity, an ideal opamp is used for simulations and first designs. Then, real opamp design will be examined. Typically, the open loop gain of an opamp is several thousand. As an ideal opamp, voltage controlled voltage source having a gain of 10000 is used. Output voltage will be equal to the input voltage multiplied by the gain factor. For input resistance, ideal opamps have infinite input resistance. In practice, they are in the order of mega ohms and in this work one mega ohm input resistance is used. To model the power consumption, 10k ohm output resistance is used. Other effects such as slew rate, gain bandwidth will not be included in the model for simplicity of ideal model.

5.1.1. Ideal opamp with feedback

In this configuration, a feedback element is connected from input to output. Initially, a resistance is used as a feedback element for simplicity; however, to model the behavior of the integrator, a capacitor will be used as a feedback element. Since output voltage is a multiple of input voltage, most of the current from the source will pass through the feedback loop because voltage difference between the output node and input node of the opamp is much greater than the voltage difference between the input node and ground.

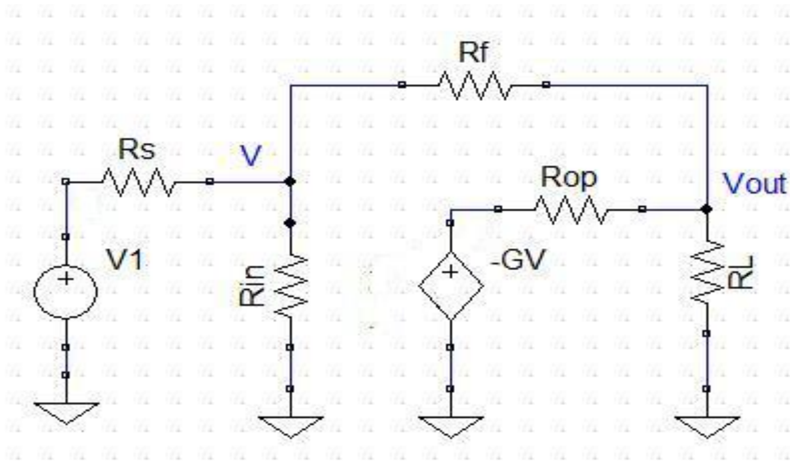

Figure 5.1. Ideal opamp with feedback

If we write the equations for this circuit and try to solve for V_{out}/V_{in}, we can get:

$$\frac{V-V_i}{R}+\frac{V}{R_{in}}+\frac{V-V_{out}}{R}=0 \tag{5.1}$$

$$V(\frac{1}{R_s}+\frac{1}{R_{in}}+\frac{1}{R_f})=\frac{V_{out}}{R_f}+\frac{V_i}{R_s} \tag{5.2}$$

$$\frac{V_{out}-V}{R_f}+\frac{V_{out}+GV}{R_{op}}+\frac{V_{out}}{R_L}=0 \tag{5.3}$$

$$V_{out}(\frac{1}{R_f}+\frac{1}{R_{op}}+\frac{1}{R_L})=V(\frac{1}{R_f}-\frac{G}{R_{op}}) \tag{5.4}$$

$$V_{out}(\frac{1}{R_f}+\frac{1}{R_{op}}+\frac{1}{R_L})(\frac{R_f R_{op}}{R_{op}-GR_f})=V \tag{5.5}$$

$$V_{out}(\frac{1}{R_f}+\frac{1}{R_{op}}+\frac{1}{R_L})(\frac{1}{R_s}+\frac{1}{R_{in}}+\frac{1}{R_f})(\frac{R_f R_{op}}{R_{op}-GR_f})=\frac{V_{out}}{R_f}+\frac{V_i}{R_s} \tag{5.6}$$

$$\left[\left\{(\frac{1}{Rf}+\frac{1}{Rop}+\frac{1}{RL}).(\frac{1}{Rs}+\frac{1}{Rin}+\frac{1}{Rf}).\frac{Rf.Rop}{Rop-G.Rf}\right\}-\frac{1}{Rf}\right]=\frac{Vi}{Rs} \tag{5.7}$$

$$RL >> Rop \quad \& \quad Rin >> Rs \tag{5.8}$$

$$G.Rf >> Rop \ \text{ and if we choose } G.Rs >> Rf \tag{5.9}$$

$$Vout(-\frac{1}{Rf})\cong\frac{Vin}{Rs} \tag{5.10}$$

$$\frac{Vout}{Vin} = -\frac{Rf}{Rs} \tag{5.11}$$

Another way to prove that almost all current flows through the feedback -if opamp's open loop gain is big enough- is:

$$\frac{V}{Rin} = Irs \quad \& \quad -\frac{G.V}{Rf} = Irf \tag{5.12}$$

$$\frac{Irf}{Irin} = \frac{-G.V.Rin}{Rf.V} = -\frac{G.Rin}{Rf} \tag{5.13}$$

$$Rin >> Rf \Rightarrow \quad Irf >> \mathrm{Irin} \tag{5.14}$$

5.2. Miller OTA

For less power, high speed and less die area considerations 0.35μm CMOS process is used. However, the ever decreasing of channel lengths and transistor sizes make analog design a hard task. General expressions become inconsistent with the actual design and the planned one. Thus, making a design with these device sizes needs new techniques. Gm/id based design technique is used to realize a Miller OTA.

5.2.1. Gm/id Based Design

Gm/id is a new design methodology which gives continuous information about device operation region to facilitate analog design. It is based on the relation between transconductance over drain source current with normalized current which is the drain source current divided by W/L of the transistor **[**2**]**. Another advantage of this technique is that it gives information to calculate device sizes and taking all channel lengths equal makes the design easier. To design with the gm/id method, there must be information about device behavior which could be the mathematical model, actual device measurements or simulator output. In the proposed design in [3], the device is measured and simulated with BSIM 3v3 parameters which are shown in Figure 5.2.

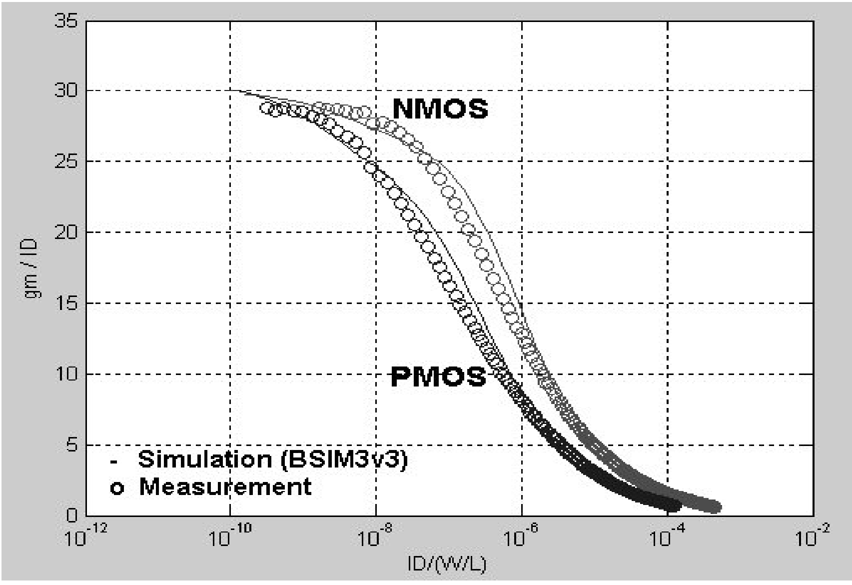

Figure 5.2. gm/id versus normalized id (id/(w/l)) [3]

Differential input single output Miller OTA in Figure 5.3. is used as the topology and transistor sizes are shown in Table 5.1. In Table 5.2. Early voltages of NMOS and PMOS are shown.

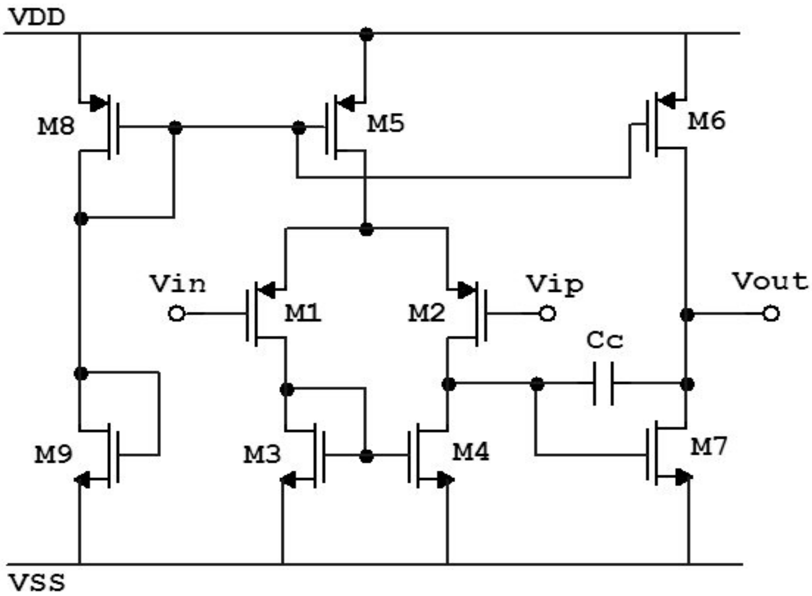

Figure 5.3. Miller OTA from [4]

Table 5.1. Transistor Sizes

Transistor	g_m/I_D	W/L	W (μm)	L (μm)
M1	10.47	36	108	3
M2	10.47	36	108	3
M3	10	10	6	0.6
M4	10	10	6	0.6
M5	7	30	30	1
M6	7	158	158	1
M7	10	103	62	0.6
M8	7	30	30	1.5
M9	1	0.25	1	4

Table 5.2. Early Voltage’s of NMOS and PMOS transistors

L (μm)	VA (V)	
	NMOS	PMOS
1	129.5	27.55
2	178.8	48.06
2.5	204.05	57.99
5	297.3	103.9
7.5	357.8	151.5
10	426.2	198.9

The proposed circuit in [5] is introduced with a few additions to the original gm/id design. It is proposed that adding the channel length as a variable will make the design more flexible. Changing the channel lengths makes the design more flexible; however, it makes the design process more difficult by taking into account some other effects related to channel length such as output resistance. In the proposed design scheme, the authors of [5] focus on getting information about the Early voltage of the NMOS and PMOS transistors which change with channel length. Then, adding this extra information to the original design methodology more design parameters will be obtained which makes the design more flexible. By controlling output resistance with changing the Early voltage, the gain will be more easily adjustable. However, Early voltage dependency with the channel length is not linear. Thus, NMOS and PMOS transistors are simulated to get data about the relation between channel lengths and the Early voltage.

Total gain of the OTA is the product of first stage gain and the second stage gain.

In general, $A_V = gm.ro = \frac{gm}{gds}$ For this OTA:

$$A_{V1} = (\frac{gm}{ID})_2 (\frac{V_{A2}.V_{A4}}{V_{A2}+V_{A4}}) \qquad A_{V2} = (\frac{gm}{ID})_7 (\frac{V_{A6}.V_{A7}}{V_{A6}+V_{A7}}) \quad G = A_{V1}.A_{V2} \tag{5.15}$$

The Miller OTA in Figure 5.3. is simulated; it is observed that 80 dB open loop gain can be achieved with this OTA. However, to make a new design with gm/id method is not easy since the design in [5] is achieved with the help of an optimization software. Without any optimization software, desired specifications could not be obtained. Thus, the Miller OTA was designed manually.

5.3. Miller OTA Manual Design

To build an OTA with TSMC 0.35µm CMOS process by gm/id design methodology using a simulator is the easiest and most accurate one to get a gm/id versus id/(W/L). This simulation was a dc sweep to observe Id for different gate source voltages. 1.65 V is used as supply voltage. The applied gate voltage is changed by a dc sweep. Then, with an Ocean script in Cadence tool, gm, id and some other transistor parameters are extracted in a scientific output form to be processed in Matlab. The graph in Figure 5.5. is plotted with Matlab. Y axis is gm/id and X axis is normalized current meaning id divided by W/L to find unity current expression. In Figure 5.5., the upper curve belongs to NMOS and the lower one belongs to PMOS.

Gm/id method is applied to the circuit with data gathered from simulations with technology TSMC 0.35µm; however, as mentioned without any optimization software, the circuit does not work as expected; some bias points were inappropriate for proper operation. With some manual modifications, Miller OTA functioned as expected. Its gain is 90 dB and total current is 100 µA and half of this current is from biasing and it can be lowered to 5 µA, which means 55 µA total current.

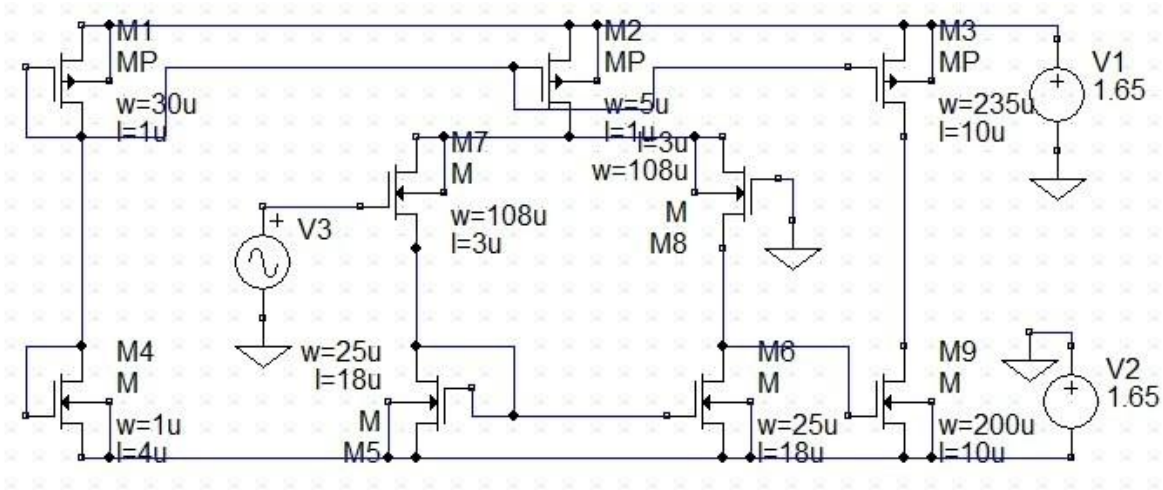

Figure 5.4 Manual OTA design

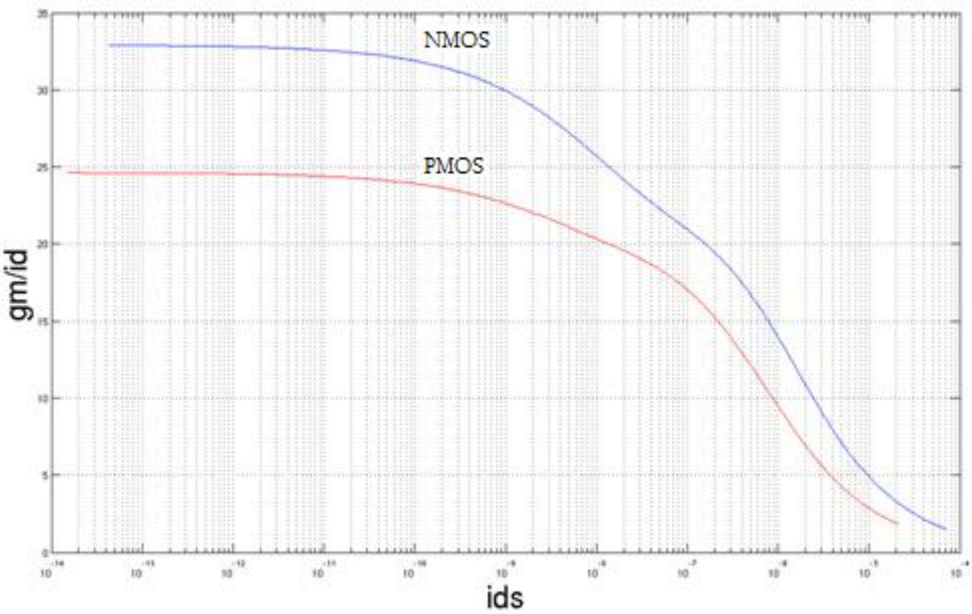

Figure 5.5 gm/id versus id/(W/L) of manual design

5.4. Fully Differential Class AB Opamp Design

5.4.1. Class A and Class AB Design

Differential input stages are used in almost all opamp configurations because of better common mode rejection properties. However, at the output stages there is no obligation to make two outputs if not needed. Having two opposite phases at two output stages will improve the circuit's performance at the expense of doubling power consumption of output stages. Thinking that almost all power is consumed at the output stages which are used for driving relatively big loads compared to internal transistors loadings, doubling the output stage is a very big disadvantage. There is a tradeoff between single ended and fully differential design based on power consumption and common mode rejection properties. For better noise rejection, fully differential design is preferred.

At the output stage, another argument is having Class A or Class AB output stages. Class A is simpler and better for high frequency applications; however, Class AB is better for high slew rate and having less offset errors at the output stage.

In switched capacitor integrators, the integration capacitor is connected between input and output of the opamp. When an opamp is used in closed loop configuration –with the assumption of having big open loop gain- current will pass only through the feedback path. Theoretically, all current from resistance or in switched capacitor designs current from sampling capacitor will pass through the integration capacitance which means that the opamp's input is a virtual ground. Considering that the integration capacitance is connected between output of the integrator and virtual ground makes this integration capacitance as output load which is basically connected between output and ground. This virtual ground property of the opamp makes integration capacitance as a direct load. Another load is the input stages of the other circuits which will be the load of the output stages of the integrator. As a total load at the output, it will be mostly capacitive and slew rate of the opamp will be very important driving this capacitive loads.

From the point of view of circuit design, simply Class A has NMOS and PMOS transistors connected from their drains as output terminal, the sources of the NMOS and PMOS transistors are connected to Gnd and Vdd respectively. To increase the gain of the opamp, there could be cascode stages for output; however, this would decrease maximum output swing and is not preferred especially for low voltage designs. In Class A design, there is only one driving transistor NMOS or PMOS and the other one is used as cascode or simply as a resistor whose current is coming from the driving transistor and its voltage is used as output voltage. Class A and Class AB output stages can be seen in Figure 5.6. In Class AB design NMOS and PMOS are both driving transistors and they are cascode of each other one to form the output voltage. Since there are two driving transistors, it is obvious that current driving capability of this design is better than Class A design. Another main advantage is Slew Rate will be much higher than Class A design. Another disadvantage of Class A design is quiescent working point must be at the middle of the positive and negative rail and this increases the quiescent power consumption. In Class AB design, quiescent current consumption will be very low, Class A design efficiency is at maximum 25 %, however, in Class AB design efficiency can be almost 85 %.

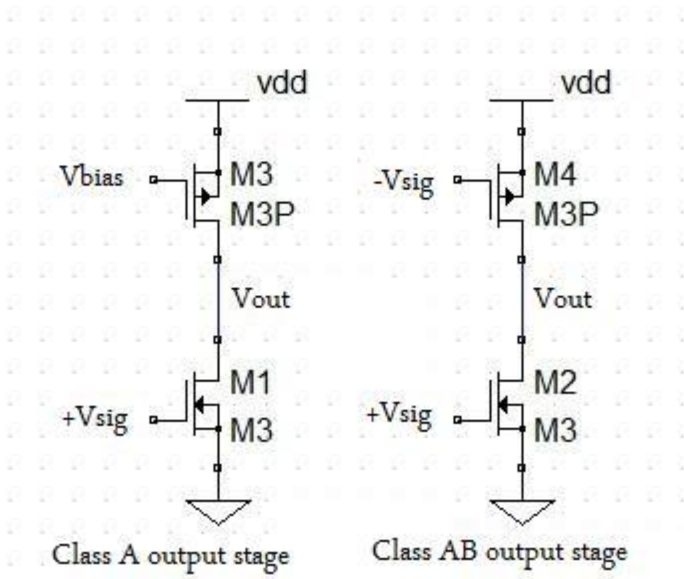

Figure 5.6. Class A and Class AB output stages

Biasing is done with one NMOS and one PMOS transistors. Their drains and gates are connected to ensure that transistors are in saturation region. Biasing circuit can be seen in Figure 5.7.

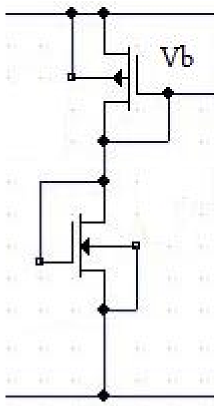

Figure 5.7. Biasing Circuit

5.4.2. Input Stage Design

Input stage is very important because it is the core of the amplifier and its specifications will determine the overall opamp specifications. Transconductance of the differential input stage will determine bandwidth, gain-bandwidth and the gain of the first stage.

Overdrive voltages of transistors must be arranged such that they will ensure that transistors are at saturation. However, overdrive voltages cannot be very high because if the overdrive voltage is high, then drain source voltage must be high to guarantee working at saturation which will in turn cause loosing from output swing. Since recent IC process supply voltages are low, channel lengths must not be too small for gain requirements. However, there is a trade-off between speed and gain to choose the right channel length. In general, working with submicron technologies, couple of minimum channel length is advised for optimum gain and speed [6].

To find the overall gain of an opamp, gain of the first stage must be found; then, second stage gain and the overall gain can be calculated.

Internal gain of a transistor is $A_V = \dfrac{g_m}{g_{ds}}$ and to find this gain, g_m and g_{ds} must be defined

$$g_m = \frac{2I_D}{V_{gs} - V_{th}} = \frac{2I_D}{V_{ov}} \tag{5.16}$$

$$g_{ds} = \frac{I_D}{V_A} \quad \& \quad V_A \sim L \tag{5.17}$$

From simulations, channel length and Early voltage relation is found empirically which is given by

$$V_A = \lambda_L L^{0.63} \tag{5.18}$$

$$g_{ds} = \frac{I_D}{\lambda_L L^{0.63}} \tag{5.19}$$

Gain of the input stage is: $A_V = \dfrac{g_{m9}}{g_{ds9} + g_{ds2}}$ (5.20)

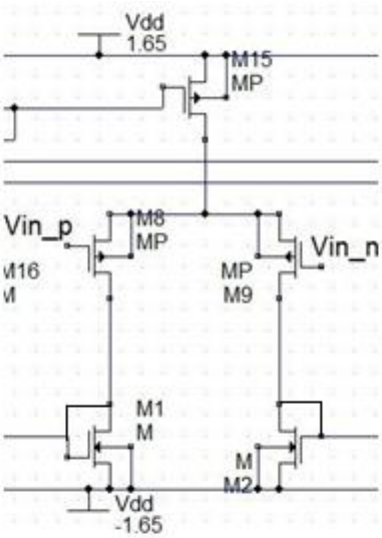

Figure 5.8. Input Stage

5.4.3. Output Stage Design

Output Stage is designed with Class AB architecture which is mentioned previously. One input from the first differential stages output is directly connected to NMOS, for input of PMOS; output of the first stage is mirrored with a current mirror and then, connected to the PMOS. For simulations 10 pF capacitance is used to model the load; however, it must be considered that this integrator can be used as an intermediate state and output load will be possibly less than 10 pF.

Using two transistors at the output stage allows high output swing, because there are only two transistors and voltage drop at the output wil only be two drain-source voltages. Fully differential Class AB opamp can be seen in Figure 5.9.

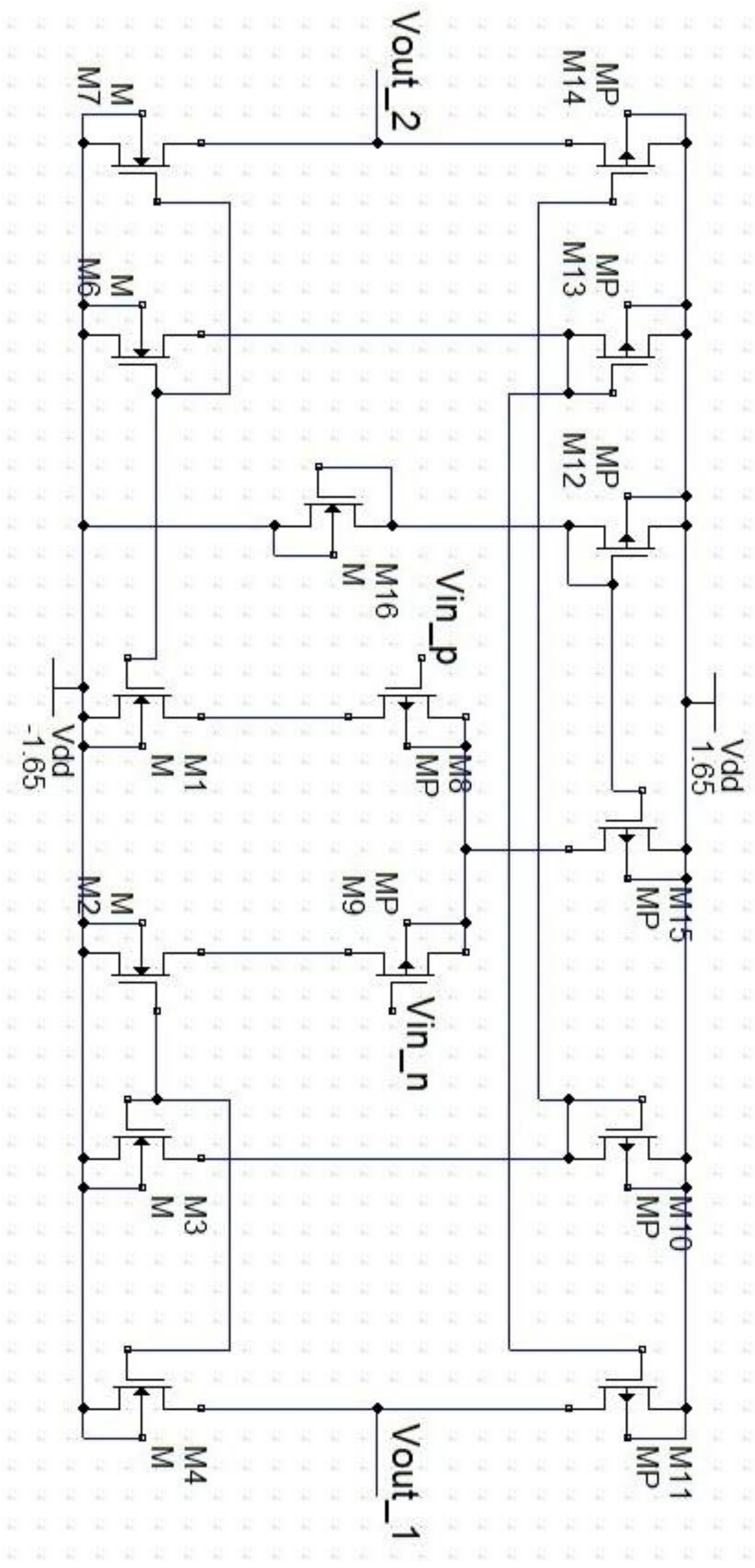

Figure 5.9. Fully Differential Class AB opamp

6. SWITCH DESIGN

In order to implement the switched capacitor integrator in a CMOS IC, all parts must be transistors including the switches. Ideal switches are assumed to have no voltage drop between their terminals; however, transistor switches show voltage drop between their drain-source nodes. Another disadvantage is that their behavior changes with biasing. Thus, biasing must be proper and the actual behavior of the transistors during transition time must be taken into account.

6.1. MOS Transistor as a Switch

MOS transistors have the advantage of having almost perfect isolation when they are at "OFF" state like an ideal switch; however, they have a disadvantage when their "ON" state. Clock signals which applied to gate of MOS transistors can cause errors to switching activity. There are two major error sources related to MOS switch; one is charge injection and the other one is clock feedthrough.

6.2. Charge Injection Error

When the transistor is turned on, some charge is stored under the gate which forms a channel and which is the main working principle of the MOS transistor. However, when the transistor is turned off, the charge which has been stored under the gate goes into two directions; to the source and to the drain terminals. One node is most probably connected to Vdd or ground and charge is absorbed by these supply terminals and has no affect on switching activity. However, charge which is not absorbed by the supply terminals goes to the sampling capacitance and cause an offset error at this capacitor. In Figure 6.1., the charge injection effect can be seen.

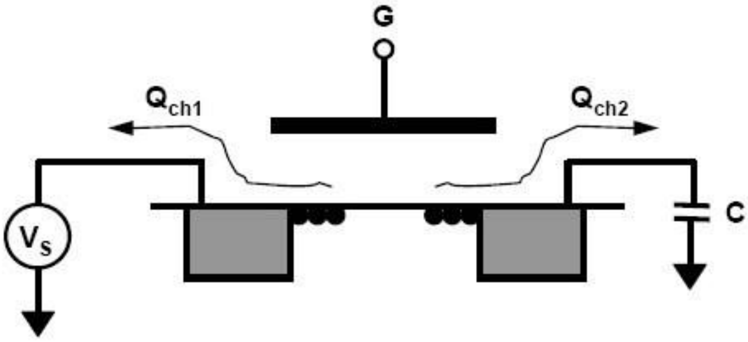

Figure 6.1. Charge injection in a MOS transistor

Charge which formed at the channel is given by

$$Q_{ch} = WLC_{ox}(V_{gs} - V_{th}) \tag{6.1}$$

Error at the capacitance can be explained with

$$Q = CV \quad \Rightarrow \quad Q + \Delta Q = C(V + \Delta V)$$
$$\Delta V \quad = \text{offset error at the capacitance} \tag{6.2}$$

To decrease the charge injection error, storage capacitance must be increased or transistors sizes must be decreased. However, these resizing alternatives of the circuit must be considered carefully, because each will affect the overall performance. From the channel charge and transistor size equation, it can be deduced that, reducing transistor sizes will directly decrease the charge injection. However, reducing transistor sizes must be done carefully because, transistor sizes directly affect the on resistance which will change the settling time.

6.2.1. Decreasing the charge injection with dummy switch

To reduce the charge injection error, dummy switch configuration can be used which is depicted in Figure 6.2. In this configuration, dummy switch will inject opposite charge which will recombine with the charge of the actual switch. The main disadvantage of this configuration is that it will increase clock feedthrough error. Opposite clock signal is applied to the gate of the dummy switch. Another disadvantage of this configuration is that it needs an extra clock. Opposite charges will cancel each other and less injected charge will cause error at the capacitance. For exact cancellation of the charge, the size of the dummy switch must be adjusted correctly.

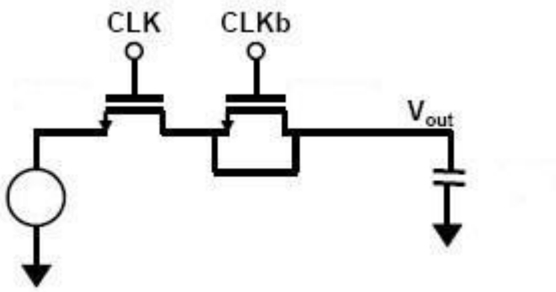

Figure 6.2. Dummy Switch technique

6.2.2. Decreasing the charge injection with complementary switch

In this configuration, one NMOS and one PMOS are connected in parallel and opposite clock signals applied to the gates of the transistors. Injected charges of NMOS and PMOS cancel each other and charge injection effect will be reduced. Another advantage of this configuration is "ON" resistance of the system will be decreased with parallel connected two transistors which will result fast settling response (decreasing T=RC time constant). However, in this technique, like in the dummy switch technique, another transistor and clock signal is needed. Another disadvantage of this configuration is increasing of the parasitic capacitances, which will cause charge sharing and degrading the overall systems response.

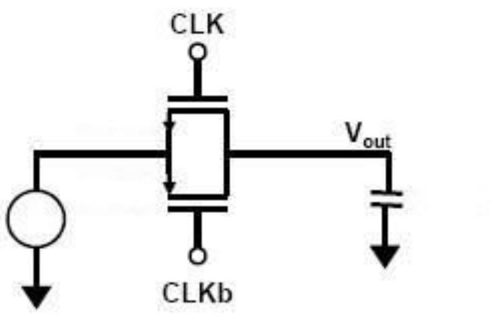

Figure 6.3. Complementary Switch technique

6.3. Clock Feedthrough Error

Through the production process of MOS transistors, drain and source regions can't be manufactured accurately enough to be perfectly aligned beneath the gate plate. During the production, extended drain and source areas will be produced which will be parallel to the gate electrode. Between these overlapped areas and the gate plate, there is a gate oxide layer, which will form parasitic capacitances with these extended drain and the source regions. These parasitic capacitances will not cause much harm in digital circuits with the assumption of working at not very high frequency; however, in analog circuits it can affect the overall system badly. When transistors are at their "ON" state, these parasitic capacitances are charged with applied clock signals and when transistors are at their "OFF" state, the charge which stored on these parasitic C_{gs} and C_{gd} capacitances discharges. Like in charge injection, some of this charge goes to supply terminals and some goes to the sampling capacitance which will cause an offset error at the sampling capacitance. Another error related to these parasitic capacitances is that they cause leakage of digital noise to the main signal as being coupling capacitance to digital noise.

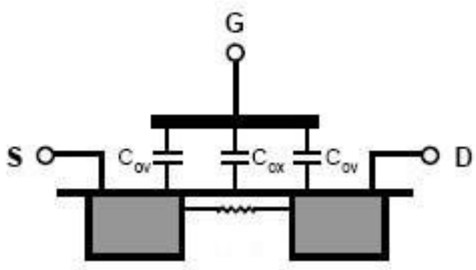

Figure 6.4. Overlapped capacitances of MOS transistor

Several designs have been proposed to reduce or cancel clock feedthrough effect. The most effective techniques are fully differential cancellation [7], quasi differential cancellation [8] and suppression with negative feedback [9] [10].

6.4. Transmission Gate Based Switch

NMOS and PMOS single switches are not used in analog design due to threshold drop between their drain and source terminals; however, NMOS and PMOS transistors are used parallel in analog design as switch, which is called complementary or transmission gate switch. Transmission gate is better than NMOS or PMOS single switches; however, it has disadvantages too. It needs two transistors which mean adding parasitic capacitances to main signal path. Another disadvantage is that it needs two clock signals. Transmission gate, used for switched capacitor integrators in this work, has two clock inputs, one is positive and the other one is negative and their timing conditions are similar. This configuration is used to reduce the charge injection, clock feedthrough and on resistance. In charge injection mentioned earlier, charge goes in two directions, one is the supply rail which can be ground or Vdd and the other one is the capacitor. In this configuration, most of the charge formed during the "ON" state of NMOS transistor will be cancelled at the "OFF" state by opposite charge which is formed at the PMOS transistor. In this way, offset error at the capacitor is reduced greatly. The transmission gate topology can be seen in Figure 6.5.

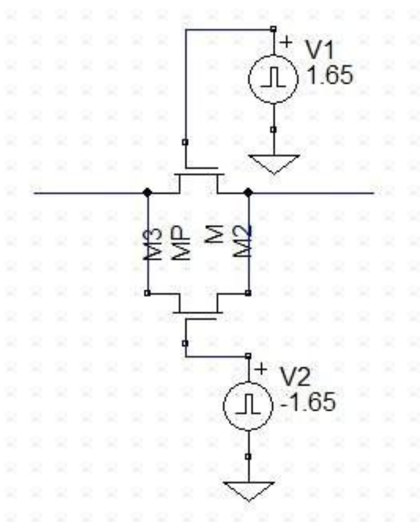

Figure 6.5. Transmission Gate

In this configuration, if NMOS and PMOS transistors have the same sizes their parasitic capacitance will be the same. Clock feedthrough effect is expected to be the same and the charge formed at the "ON" state of the transistors is expected to be same. However, at the output of the transmission gate, charge injection and clock feedthrough effects won't cancel each other exactly, because different thresholds will cause deterioration in this symmetric cancellation.

6.5. Switch Design Considerations

Switch design mainly consists of two major concerns; one is conduction and the other one is parasitic effects. For less settling time, on resistance of the switches must be small which means large transistor sizes. However, for less parasitic effects, transistor sizes must be small. Thus, there is a tradeoff in choosing the size of the transistor.

At low frequencies, there will be enough time for settling even at minimum allowable sizes of transistors; however, at high frequencies settling time must be less compared to the settling time for low frequencies. As mentioned in previous sections seven time constants accepted to be enough accurate for settling.

$$T_{sw} = R_{sw}.C_s \quad \text{and} \quad R_{sw}.C_s.7 \leq T_{ON}(switch) \tag{6.3}$$

$$I_d = \frac{\mu_{n,p}.W.C_{ox}(V_{gs} - V_{th})^2}{2L} \tag{6.4}$$

$$Q_{ch} = WLC_{ox}(V_{gs} - V_{th}) \tag{6.5}$$

Minimum sampling capacitance is used to decrease the settling time, transistor sizes must be large which will in turn result in increasing of the parasitic effects such as charge injection and clock feedthrough. Thus, at high frequencies again there is a tradeoff between speed and error. Choosing minimum allowable channel length is advantageous both in terms of conduction and less parasitic effects. However, choosing transistor width must be considered carefully. Increasing width linearly increases injected charge and almost linearly decreases on resistance. To observe channel on resistance relation with width of transistor, a dc sweep simulation is done. A NMOS transistor's width is increased from the minimum allowable width of 600 nm (in 0.35 µm CMOS process) to 10 µm and on resistance of the transistor is depicted in Figure 6.6.

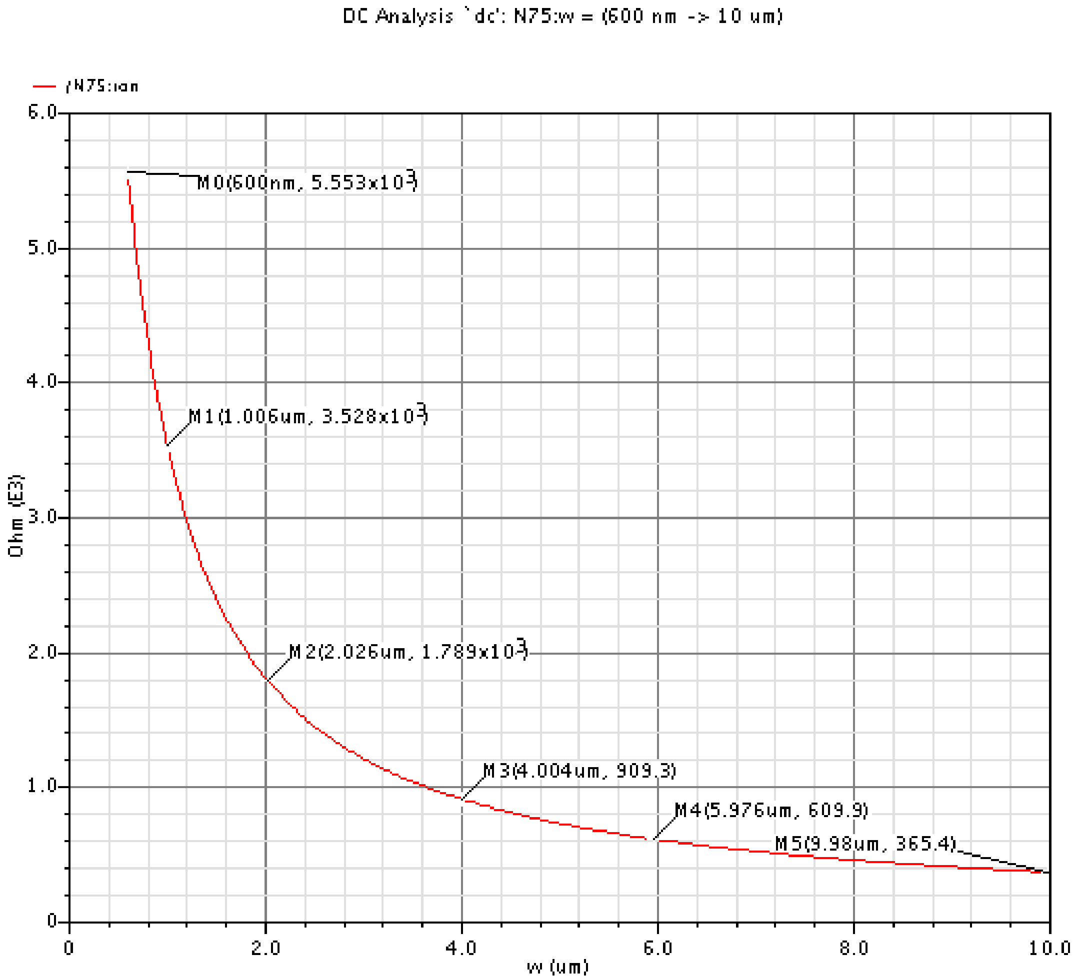

Figure 6.6. On resistance of NMOS changing with width from 600nm to 10µm

To observe the charge injection relation with transistor sizes, two circuits are built. One is built with switches whose transistors width are 0.6 µm and the other one is built with 6 µm width of transistors, both having 400 nm channel length and 100 fF sampling capacitance. The voltage on the sampling capacitances for both circuits can be seen in Figure 6.7. Output voltage of 101.9 mV belongs to switches which have 6 µm width and the output voltage of 100.2 mV belongs to switches which have 0.6 µm width.

Error of $6\mu m$ width transistor is: $101.9 - 99.975 = 1.925 mV$

Error of $0.6\mu m$ width transistor is: 100.2-99.975=0.225mV

Error of 6 μm width transistor is almost ten times of 0.6 μm width transistor.

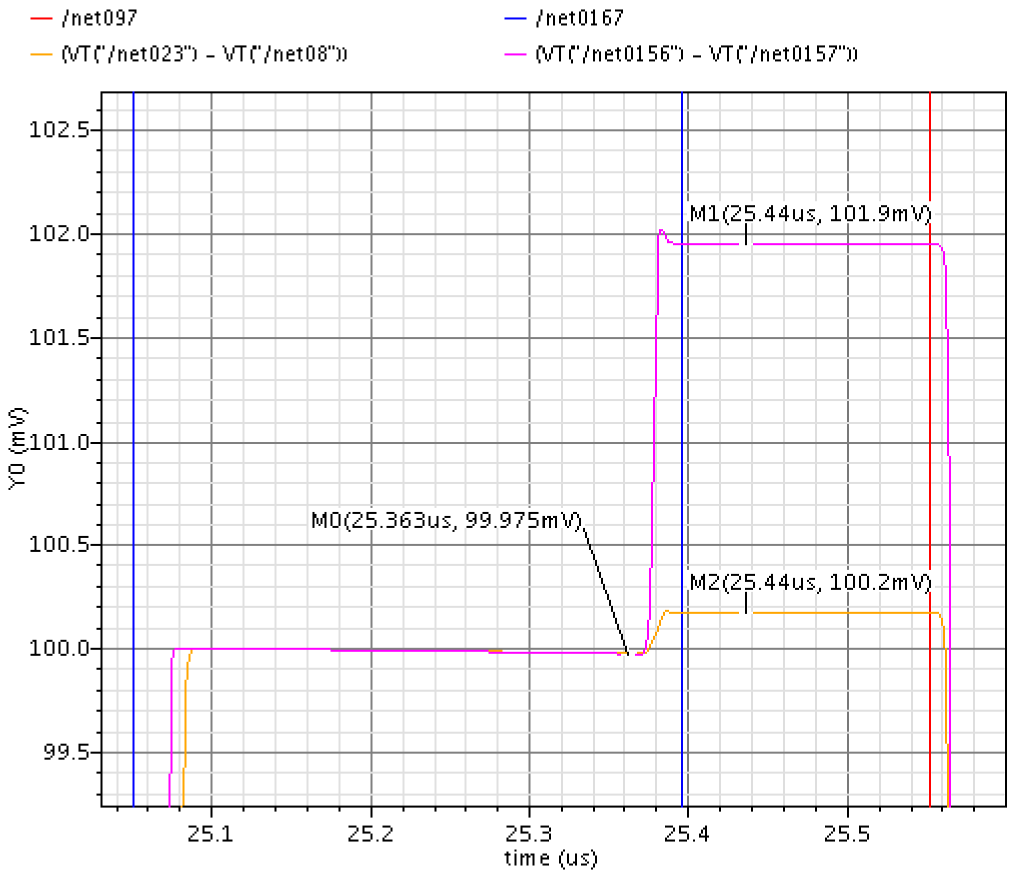

Figure 6.7. Charge injection error of two switches; w = 600 nm and w = 6 μm

Another main design consideration for the switching part is choosing the size of the sampling capacitance. To reduce the charge injection and the other parasitic effects, the sampling capacitance must be as large as possible. Increasing the sampling capacitance leads to store more charge on it and injected charge will be less effective when having more charge on sampling capacitance. However, when sampling capacitance is small, injected charge over stored charge ratio gets bigger which will result increasing the error. However, for less settling time, sampling capacitance must be as small as possible because increasing the sampling capacitance will directly increase the settling time. Thus, again there is a tradeoff between speed and error. To observe the relation between the sampling capacitance size and the charge injection error, two switched capacitors are built; one has 0.1 pF sampling capacitance and the other one has 1pF sampling capacitance and both having 6 μm width and 0.4 μm length of transistors as switches. The voltages of the two circuits sampling capacitances can be seen in Figure 6.8. The output signal which is marked with 100.173 mV belongs to 0.1 pF sampling capacitance circuit and output signal which is marked with 100.003 mV belongs to 1 pF sampling capacitance circuit.

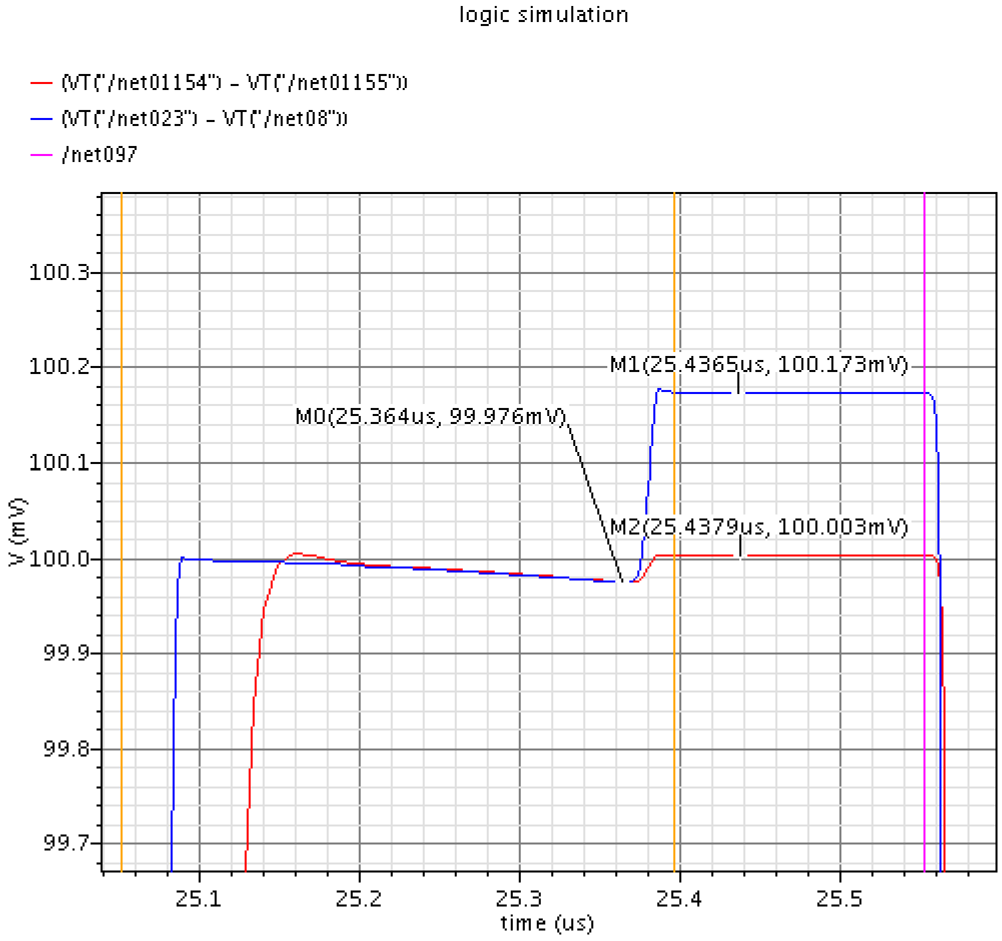

Figure 6.8. Charge injection error of two switches having 0.1 pF and1 pF sampling capacitance

Error at 0.1 pF sampling capacitance is: 100.173-99.976=0.197 mV

Error at 1 pF sampling capacitance is: 100.003-99.976=0.027 mV

Error of 0.1 pF sampling capacitance is almost ten times of 1 pF sampling capacitance ones.

It can be seen from the last two simulation results that both have almost ten times error ratios but not exactly ten times, because of other parasitic effects such as charge sharing between sampling capacitance and parasitic capacitances of transistors such as gate-source, gate-drain and drain-source capacitance. In real IC design; however, there will be extra parasitic capacitances from connection paths and extra errors related to mismatching.

Another main design issue of the switches is the clock feedthrough effect. To decrease the clock feedthrough effect, transistor sizes must be small as possible to decrease the parasitic overlapping capacitances C_{gs} and C_{gd}. These parasitic capacitances linearly increase with the increasing of the transistor sizes. Thus, making transistors small will cause less error. To observe the relation between transistor sizes and parasitic capacitances C_{gs} and C_{gd}, a dc sweep simulation is done. In this simulation, channel length is chosen as 0.4 µm and width of transistor is increased from 0.6 µm to 10 µm and simulation result can be seen in Figure 6.9. It can be seen from figure that parasitic capacitances are increased linearly with increasing of transistor width.

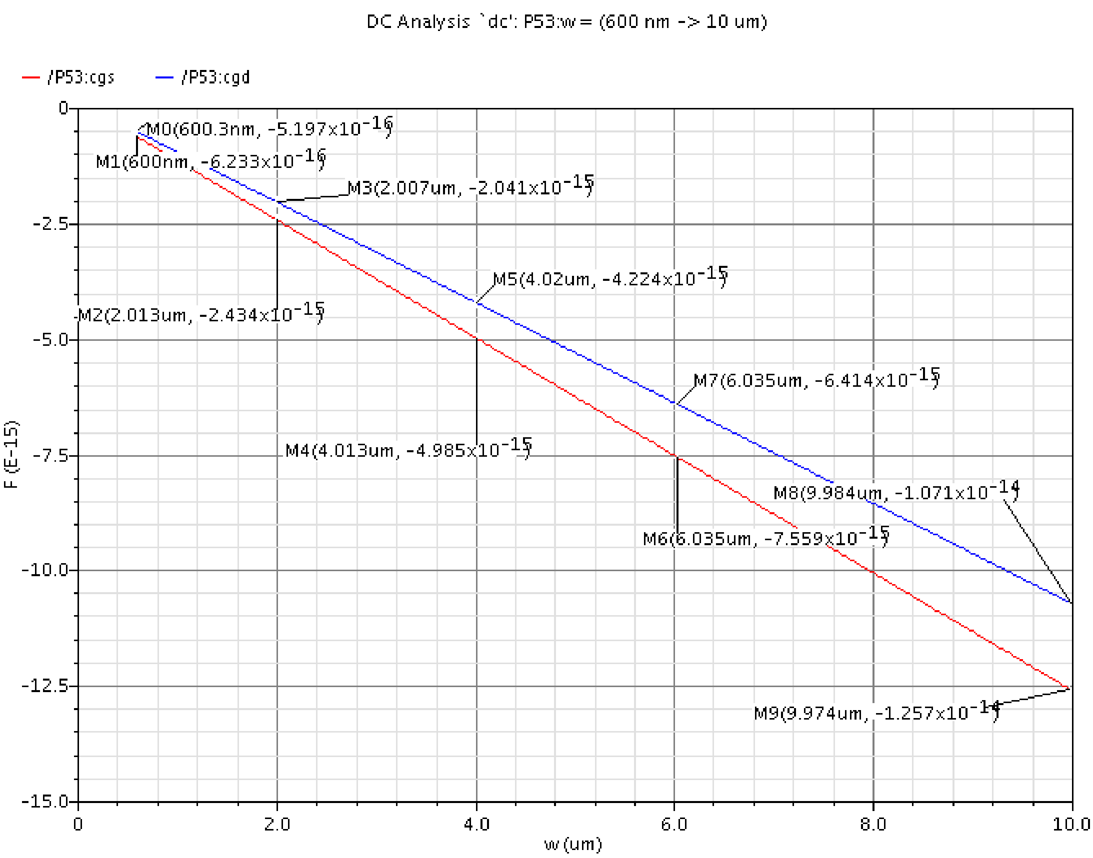

Figure 6.9. C_{gs} and C_{gd} relation with width of transistor

7. SWITCHED CAPACITOR INTEGRATOR DESIGN

7.1. Switched Capacitor Architectures

For different purposes, various switched capacitor architectures are used. Stray insensitive architecture is used commonly because of suppressing the parasitic effects of stray capacitance. Stray capacitance causes crosstalk noise which means signals can affect each other and sometimes leak to other signals which will affect circuit's performance severely.

For preventing short circuit or unwanted signal leakage, applied clock signals must be non-overlapping. In Figure 7.1. non overlapping clock signals are depicted.

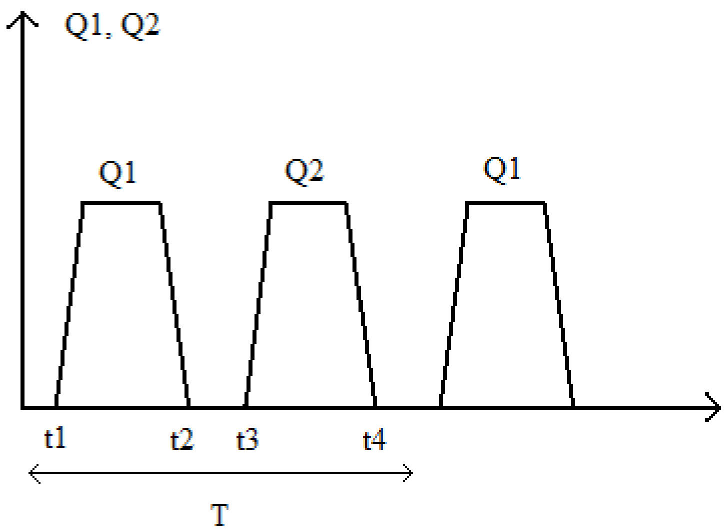

Figure 7.1. Non Overlapping Clock Signals applied to switches

Switched capacitors are used for realization of resistors with capacitors as mentioned earlier. To obtain a desired resistor with switched capacitors, different architectures are used having different properties. In Figure 7.2. switch capacitor simulation techniques [11] is depicted.

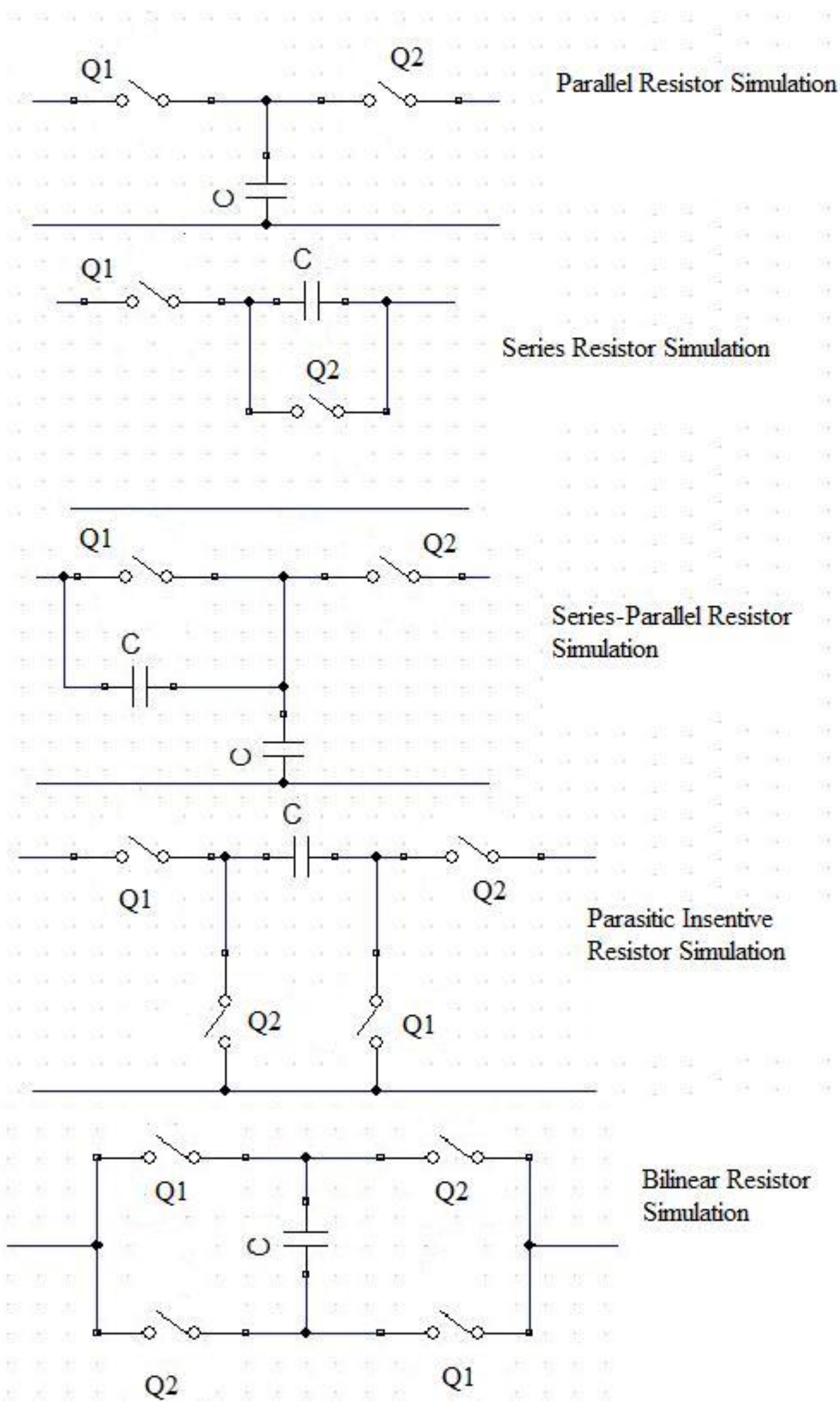

Figure 7.2. Switched Capacitor Resistor simulation

7.2. Switched Capacitor Integrator

Switched capacitor integrators are almost the same as resistor based integrators; only resistor is replaced with the switched capacitor. Resistor based and switched capacitor based integrators can be seen in Figure 7.3. Output signals are similar which can be seen in Figure 7.4.

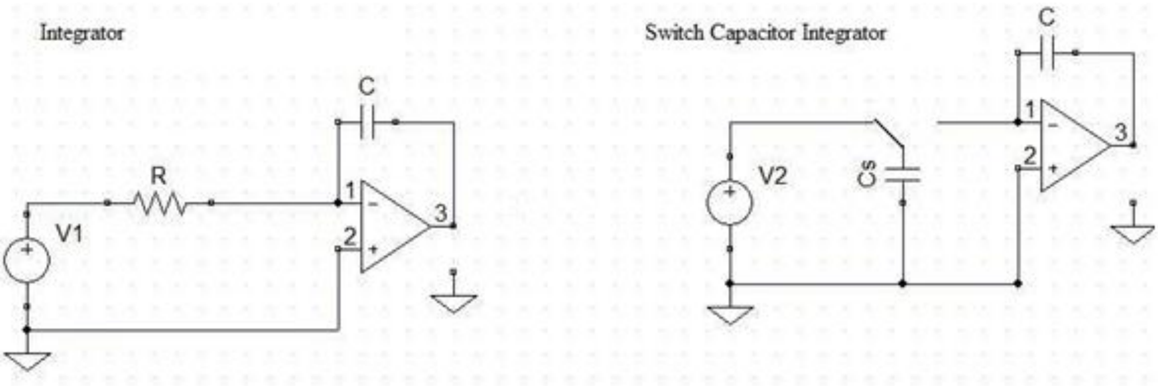

Figure 7.3. Integrator and Switched Capacitor Integrator

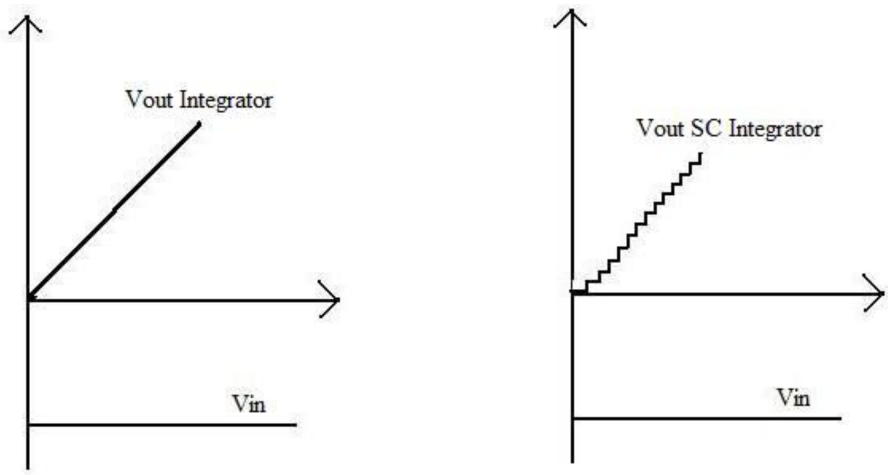

Figure 7.4. Output of Integrator and SC Integrator

Switched capacitor integrators are generally used in the filter applications to obtain a desired filter function. They have basically an opamp, a switched capacitor part and a capacitor to integrate the input signal. Assuming the opamp to be ideal, the entire signal will flow through the integrating capacitor. There will be no current sinking into the opamp; however, works by pulling the current from integration capacitor. Thus means that the main performance of the integrator is directly related to the opamp's performance. Thus, opamp's properties will affect overall performance such as speed, frequency response and slew rate specifications.

7.3. Switched Capacitor Integrator Architectures

For different purposes different switch capacitor architectures are used. The simple architecture is not used because it has parasitic (stray) capacitance. Inverting and non inverting stray insensitive integrators are used to invert the output phase or not. Summing and differential ones are used for processing many signals as input. Switched capacitor integrator architectures are depicted in Figure 7.5.

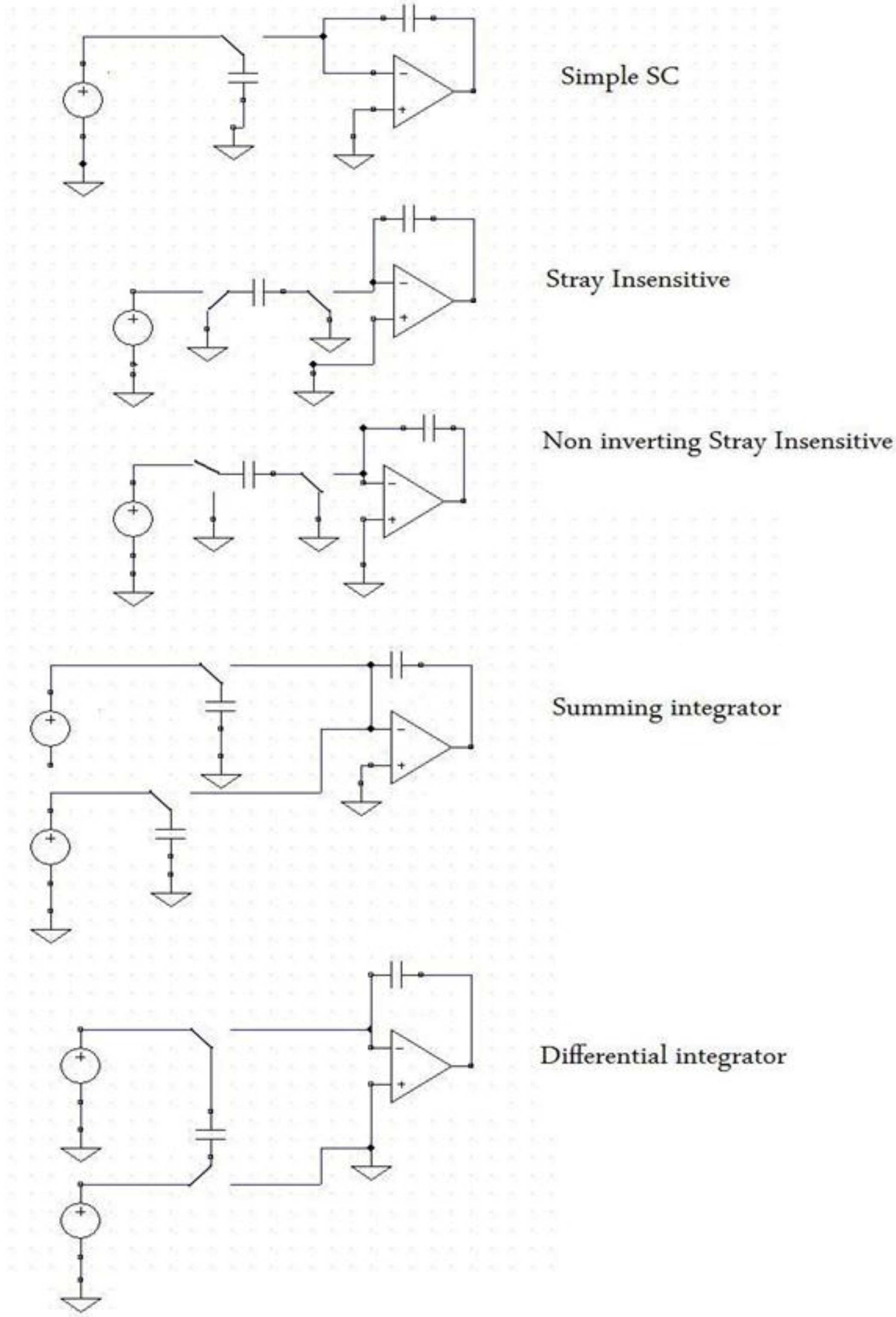

Figure 7.5. Switched Capacitor Integrator Architectures

7.4. Switched Capacitor Integrator with Ideal Opamp

In this section, switched capacitor integrators are realized with ideal switches and an ideal opamp. Stray insensitive architecture is used because in real transistor based switched capacitor integrators, the integrator will suffer from parasitic effects of stray capacitance. To model real transistor based switches with ideal components, switches are modeled as ideal switches having a 1 KΩ resistor at their “ON” state and having 1 TΩ resistance at their “OFF” state. 1 MΩ resistance is parallel connected to the input of the ideal opamp, to model the input resistance of the opamp. All current coming from AC source will pass from the switched capacitor equivalent resistor through integrating capacitor to the output. The circuit with ideal elements is depicted in Figure 7.6. Output is calculated and simulated with ideal components and results are compared. Calculated and simulation results are almost same.

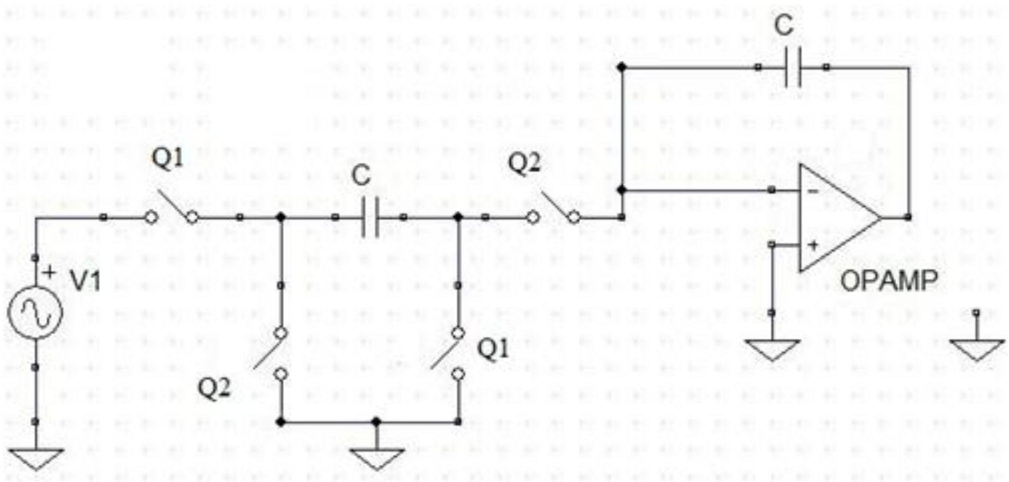

Figure 7.6. Switched Capacitor Integrator with ideal opamp

$$R_{switch} = 1k\Omega \ \ \& \ \ \mathrm{C}_{samp} = 1pF \ \ \& \ \ \mathrm{C}_f = 50\mathrm{pF} \tag{7.1}$$

$$\mathrm{T}_{on}, \mathrm{T}_{off} = 25.10^{-9} \ \ \& \ \ V_{in} = 10^{-2} \sin 2\pi 10^3 t \tag{7.2}$$

$$8.2.R.C \le \mathrm{T}_{on} \quad \Rightarrow \quad 8.2.10^3.10^{-12} \le 25.10^{-9} \tag{7.3}$$

$$20.10^{-9} \le 25.10^{-9} \quad \text{charging and discharging time is enough} \tag{7.4}$$

$$R_{sc} = \frac{T_{samp}}{C_{samp}} = \frac{10^{-7}}{10^{-12}} = 10^5 \Omega \tag{7.5}$$

$$I_{cf} = C_f \frac{dV_C}{dt} \quad \& \quad \mathrm{V}_C = V_{out} \tag{7.6}$$

$$I_{cf} = \frac{V_{in}}{R_{sc}} \tag{7.7}$$

$$\mathrm{V}_C = V_{out} = \int \frac{1}{C_f} I_{cf}\, dt \tag{7.8}$$

$$\mathrm{V}_C = V_{out} = \int \frac{V_{in}}{\frac{T_{samp}}{C_{samp}} C_f}\, dt \tag{7.9}$$

$$\int \frac{10^{-2} \sin 2\pi 10^3 t}{10^{-7}} \frac{C_{samp}}{C_f}\, dt = \frac{10^{-2}(-\cos 2\pi 10^3 t)}{10^{-7} 2\pi 10^3} \frac{10^{-12}}{50 10^{-12}} \Big|_0^T \Rightarrow \tag{7.10}$$

$$\frac{-\cos 2\pi 10^3 t}{\pi} = -0.318 \cos 2\pi 10^3 t \tag{7.11}$$

Output signals amplitude from simulation is 0.317V.

7.5. Switched Capacitor Transistor Implementation

In the previous sections switched capacitor integrator's parts; opamp and switching part are analyzed first with ideal components, then each part is realized with MOS transistors. In this section, the overall system will be analyzed in more detail. To observe the actual circuit's performance, real switched capacitor integrator filter design specifications are used in the design, such as input signal's amplitude and frequency, sampling frequency, sampling and integration capacitor values. A sine wave is applied with 0.1V amplitude and 10 kHz frequency, sampling capacitance is 0.5 pF, integration capacitance is 1 pF and sampling frequency is 1 MHz.

Before going into the details of the actual MOS based realization of switched capacitor integrator, simple resistor based switched capacitor integrator will be examined first. In this configuration, current which comes from the signal source will pass through a resistor and will be integrated on a capacitor and the output signal will be obtained. Basic resistor based integrator configuration can be seen in Figure 7.7.

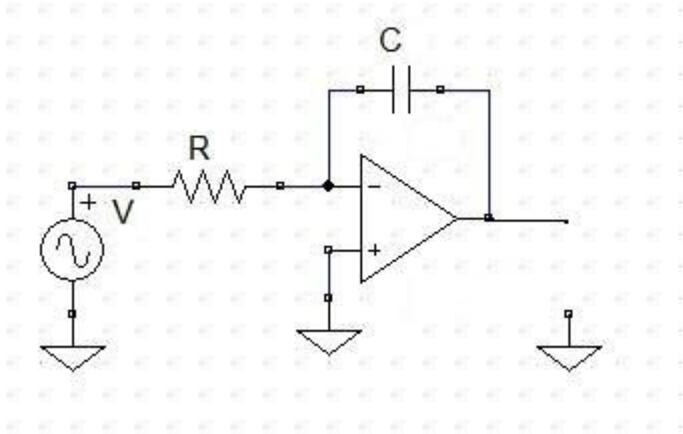

Figure 7.7. Basic Integrator Structure

Assuming the opamp's open loop gain to be quite high and using the opamp in a closed loop, all current will be passing through the feedback path and output signal will be formed on the capacitance.

$$\frac{V_s(t)}{R} = C_{\text{int}} \frac{dV_C}{dt} \tag{7.12}$$

$$\frac{dV_C}{dt} = \frac{V_s(t)}{R.C_{\text{int}}} \tag{7.13}$$

$$\int \frac{V_s(t).dt}{R.C_{\text{int}}} = V_C(\text{t}) \tag{7.14}$$

$$V_C(t) = \frac{1}{R.C_{\text{int}}} \int V_s(t).dt \tag{7.15}$$

Assuming switched capacitor as an equivalent resistor, the equation is mainly same with adding the sampling capacitor and frequency to the original equation. With switched capacitor equivalent resistor, the equation becomes:

$$R_{sw} = \frac{1}{C_s.f_s} \tag{7.16}$$

$$V_s(t).C_s.f_s = C_{\text{int}} \frac{dV_C}{dt} \tag{7.17}$$

$$\frac{dV_C}{dt} = \frac{V_s(t).C_s.f_s}{C_{\text{int}}} \tag{7.18}$$

$$\int \frac{V_s(t).C_s.f_s.dt}{C_{\text{int}}} = V_C(\text{t}) \tag{7.19}$$

$$V_C(\text{t}) = \frac{C_s.f_s}{C_{\text{int}}} \int V_s(t).dt \tag{7.20}$$

Switched capacitor integrator implementation can be seen in Figure 7.8.

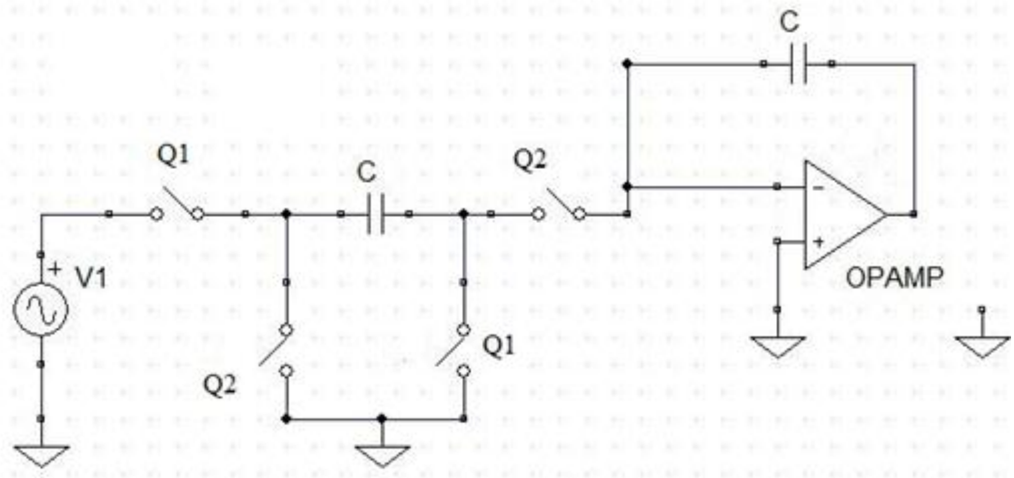

Figure 7.8. Switched Capacitor Integrator

The actual circuit which is formed with TSMC 0.35 μm CMOS process can be seen Figure 7.9.

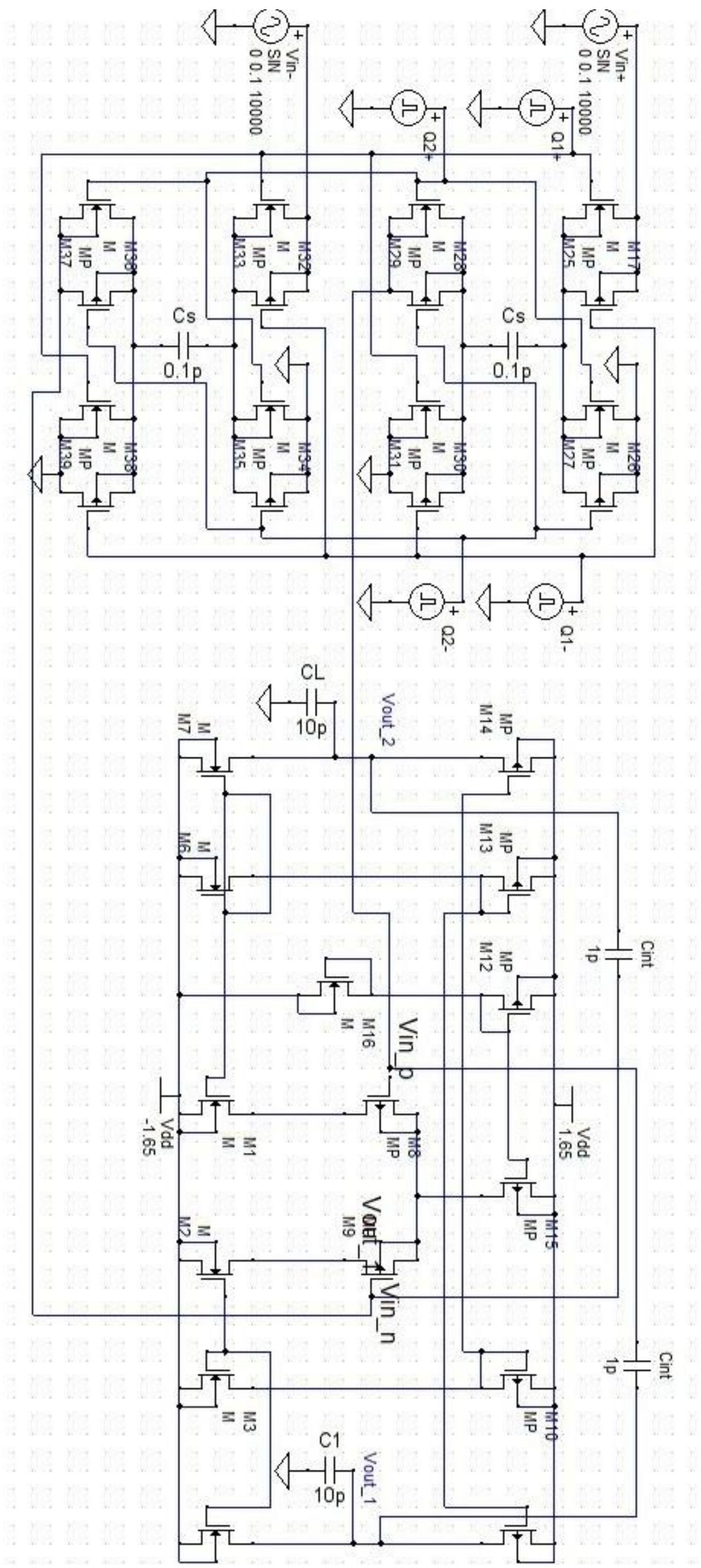

Figure 7.9. Switched Capacitor Integrator Transistor Implementation

Applying a 0.1V and 10kHz sine wave to the integrator;

$$C_s = 0{,}1pF \quad \& \quad C_{\text{int}} = 1{,}59pF \quad \& \quad f_s = 1MHz \tag{7.21}$$

$$V_C(\text{t}) = V_{out}(\text{t}) = \frac{C_s . f_s}{C_{\text{int}}} \int V_s(t).dt \tag{7.22}$$

$$V_s(t) = V_m \sin 2\pi\, ft \tag{7.23}$$

$$V_{out}(\text{t}) = \frac{C_s . f_s}{C_{\text{int}}} \int V_m \sin 2\pi\, ft.dt \tag{7.24}$$

$$V_{out}(\text{t}) = \frac{-V_m . C_s . f_s . \cos 2\pi\, ft}{C_{\text{int}} . 2\pi\, f} \tag{7.25}$$

$$V_{out}(\text{t}) = \frac{-0{,}1.0{,}1.10^{-12}.10^6 \cos 2\pi\, ft}{1.59.10^{-12}.2\pi 10^4} = -0{,}1 \cos 2\pi\, ft \tag{7.26}$$

Amplitude of the output signal is 0,1V

7.6. Integrator offset

In simulations, it has been seen that the output signal is different from expected. It is basically because of taking this integral without the initial conditions. As a simple integration without the initial conditions, cosine starts at 1 does not start at 0. Dividing this integral into four parts and considering with initial conditions:

$$\frac{C_s . f_s}{C_{\text{int}}} \int V_m \sin 2\pi\, ft.dt \tag{7.27}$$

$$\left. \frac{-C_s . f_s . V_m . \cos 2\pi\, ft}{C_{\text{int}} . 2\pi\, f} \right|_0^T = \left. \frac{0{,}1.0{,}1.10^{-12}.10^6 \cos 2\pi\, ft}{1.59.10^{-12}.2\pi 10^4} \right|_0^T = \tag{7.28}$$

$$0{,}1.\cos 2\pi\, ft \Big|_0^T = 0{,}1.\cos 2\pi\, ft \Big|_0^{\frac{T}{4}} + 0{,}1.\cos 2\pi\, ft \Big|_{\frac{T}{4}}^{\frac{T}{2}} + 0{,}1.\cos 2\pi\, ft \Big|_{\frac{T}{2}}^{\frac{3T}{4}} + 0{,}1.\cos 2\pi\, ft \Big|_{\frac{3T}{4}}^{T} \tag{7.29}$$

$$f = 10^4 \quad \text{T} = 10^{-4} \tag{7.30}$$

$$0{,}1.\cos 2\pi\, ft \Big|_0^{\frac{T}{4}} = 0 - (-0{,}1) = 0{,}1 \tag{7.31}$$

$$0,1.\cos 2\pi ft \Big|_{\frac{T}{4}}^{\frac{T}{2}} = 0,1 - 0 = 0,1 \tag{7.32}$$

$$0,1.\cos 2\pi ft \Big|_{\frac{T}{2}}^{\frac{3T}{4}} = 0 - 0,1 = -0,1 \tag{7.33}$$

$$0,1.\cos 2\pi ft \Big|_{\frac{3T}{4}}^{T} = -0,1 - 0 = -0,1 \tag{7.34}$$

Initially output is zero and at the first quarter of integral result is 0.1V

so after the first quarter: $V_{out} = 0 + 0.1V = 0.1V$

after the second quarter: $V_{out} = 0.1V + 0.1V = 0.2V$

after the third quarter: $V_{out} = 0.2V - 0.1V = 0.1V$

after the last quarter: $V_{out} = 0.1V - 0.1V = 0$

Consequently a cosine wave which has an offset value of amplitude of the input signal is obtained. Applied signal, expected output signal discarding the initial conditions and the actual output signal can be found in Figure 7.10., Figure 7.11. and Figure 7.12., respectively.

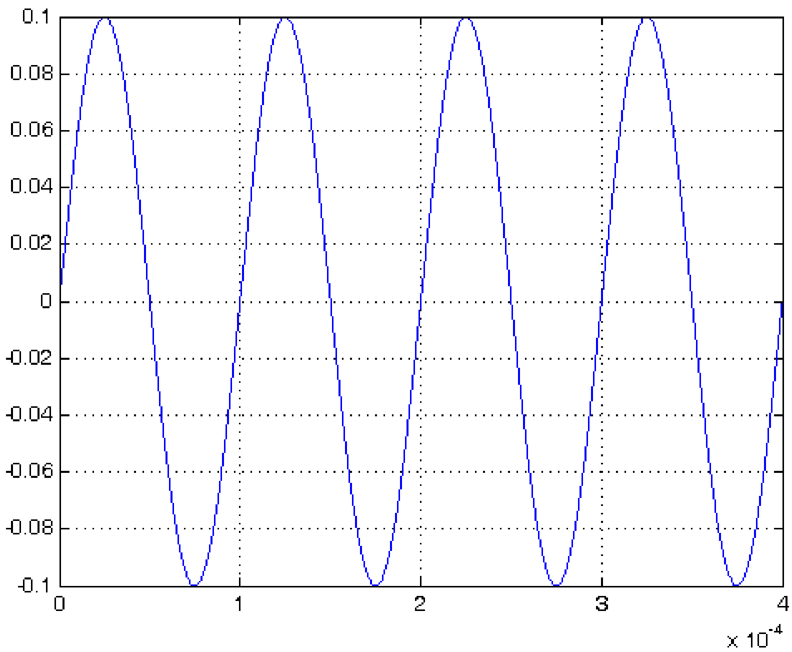

Figure 7.10. Applied input sine signal

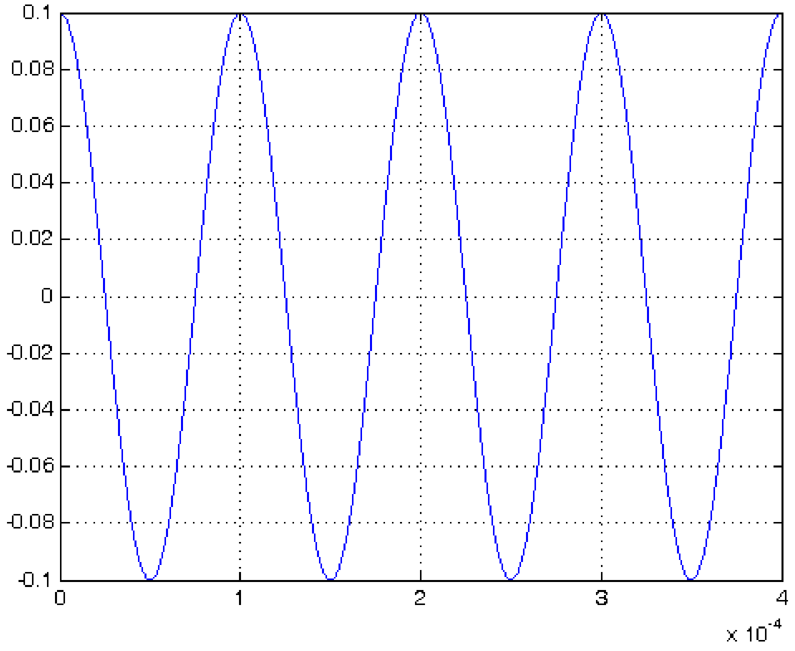

Figure 7.11. Expected cosine output signal discarding the initial conditions

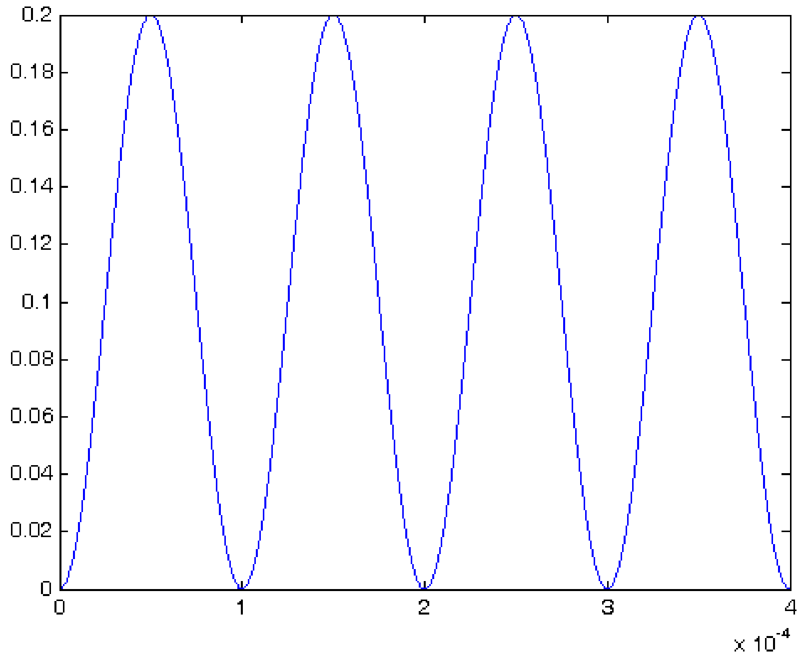

Figure 7.12. Expected ideal integrator output signal with initial conditions

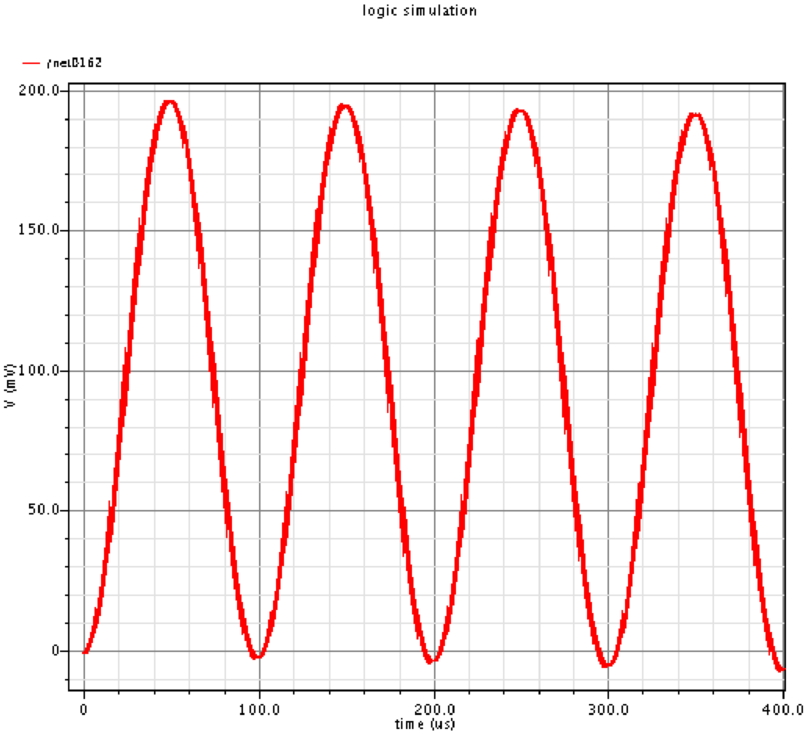

Figure 7.13. Output of the integrator

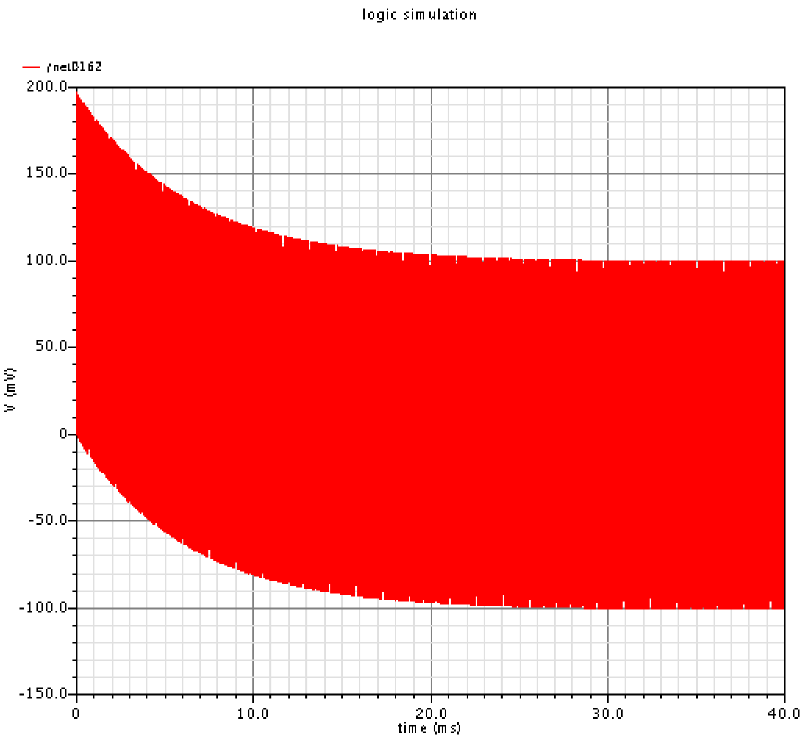

Figure 7.14. Long time simulation of the integrator to observe settling

From Figure 7.12. and Figure 7.13., it can be seen that expected the ideal integrator output signal and the actual circuit signal is different. Actual circuit's output signal has a tendency to settle at zero offset which is very meaningful and consistent with the first driven mathematical expression without taking into account the initial conditions. Settling of the output signal can be seen in Figure 7.14. This settling tendency comes from offset voltage at the capacitor, and this offset voltage is formed once at the beginning of the integration. It can be expressed as:

$$Q = CV \tag{7.35}$$

Q is the stored charge at the C capacitance with the applied V voltage. This Q charge is spent at the output load and output signal settles to zero offset due to this charge consumption at the output load. This settling is an undesirable situation and it causes errors to the overall. Decreasing this settling time will reduce the error caused by this offset. A design, which is called lossy integrator, is used to reduce this error. In this architecture, a parallel resistance is connected to the integration capacitance which is used to spend these extra charges not to cause the offset voltage.

However, there is a trade off in choosing this resistance value because a too large resistance will not help much about this settling and too small resistance will cause the current which is passing on this resistor comparable to the current on the integration capacitor and it will deteriorate the output signals amplitude and phase.

Connecting a 100 MΩ resistor parallel to the integration capacitance makes this settling time 0.6 ms, however, without this resistor settling takes almost 25 ms. Output of the lossy integrator and settling behavior can be seen in Figure 7.15.

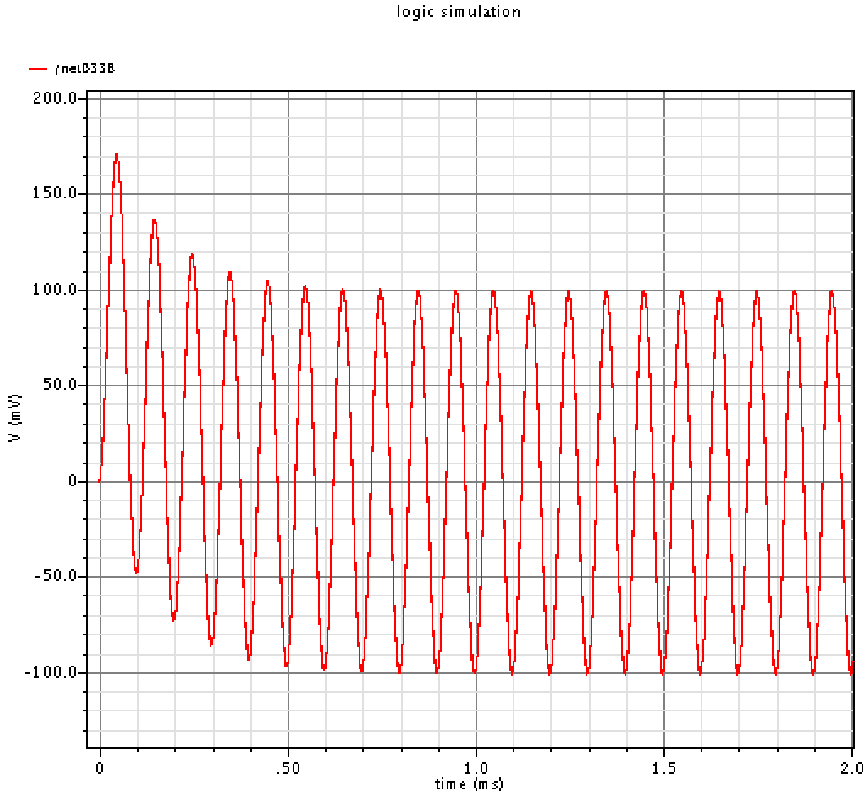

Figure 7.15. Output of the Lossy Integrator

To reduce this settling time, this effect must be considered at the first design phase. Reducing integration capacitance will result in reduction of the charge which will cause this offset voltage at the output of the integrator and reducing this extra charge will result to be spent and finished in a less time at the parallel resistance and consequently, it will shorten the settling time. However, reduction of the integration capacitance must be considered with the overall system design, including sampling capacitance, sampling and input frequency and slew rate requirements.

To model the integrator with changing signals instantaneously –as in actual physical circuits- rather than periodical signals as applied in simulations, another signal with a delay is applied after the main signal. Due to the superposition theory, each signal's effect will be considered by itself and overall result of the circuit will be the sum of each signal's response. For integrator settling with two signals; after settling of the first main signal, the other signal is applied and this result is compared with the lossy integrator's response to these same two mixed signals. A 100 mV main sine signal is applied at the time zero, another 50 mV sine signal is applied with 30 ms delay. With second input signal, total signal’s amplitude becomes 75 mV due to the voltage division of the switches. Actual mixing circuit and its equivalent circuit can be seen in Figure 7.16. and in Figure 7.17. respectively. Results show that lossy integrator configuration is a good and yet simple architecture for reducing the settling time of the integrator. Main disadvantage of the lossy integrator configuration is that it causes phase errors. By paying special attention to this phase error, lossy integrator configuration makes settling time very short compared to its original configuration. Normal integrator response and lossy integrator response can be seen in Figure 7.18. and Figure 7.19. respectively.

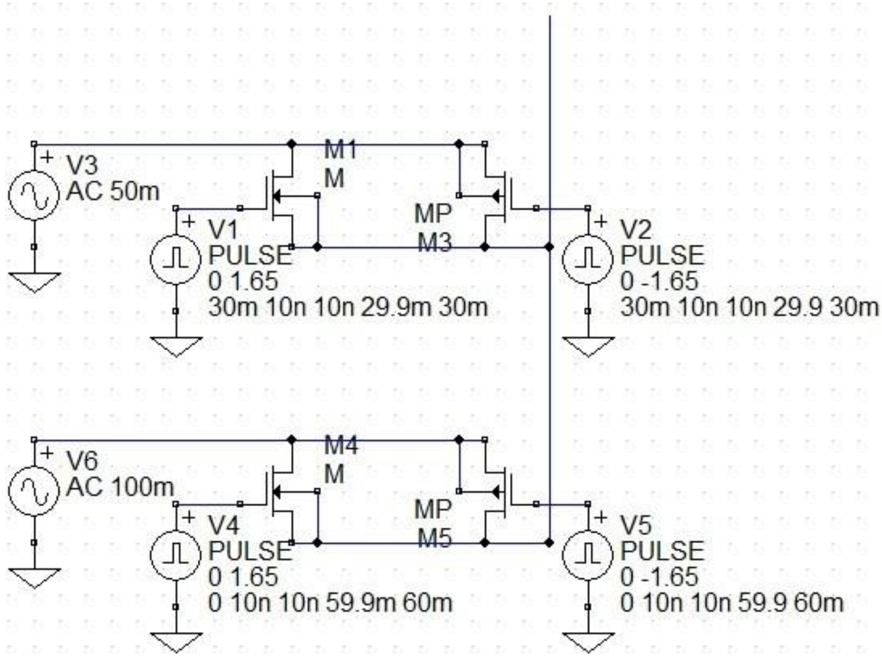

Figure 7.16. Input mixing circuit

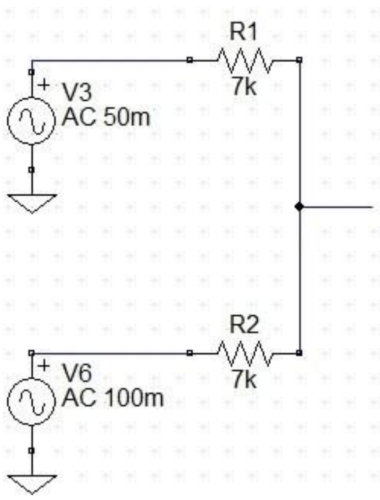

Figure 7.17. Equivalent of the input mixing circuit

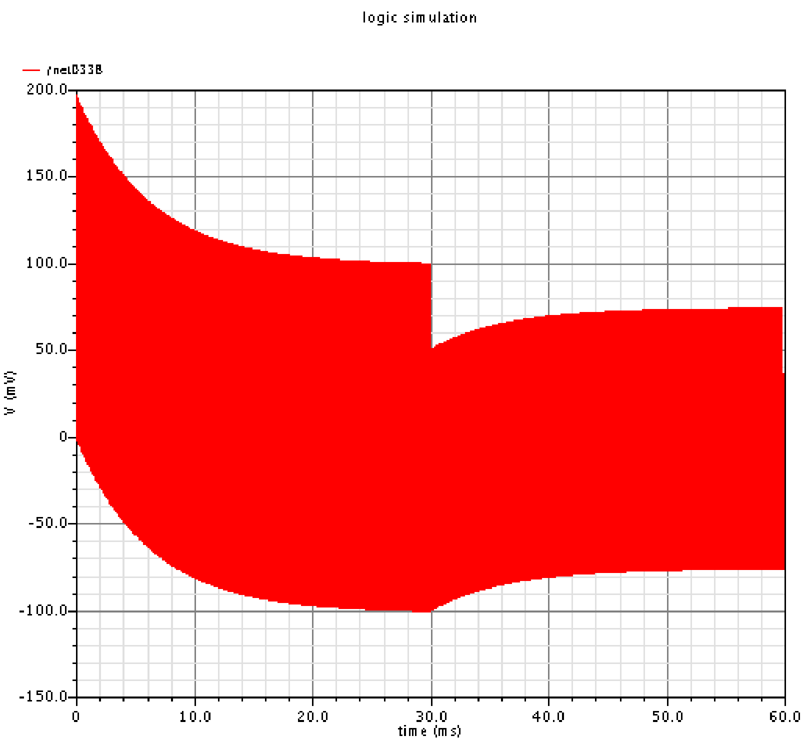

Figure 7.18. Normal integrator response to two mixed signals

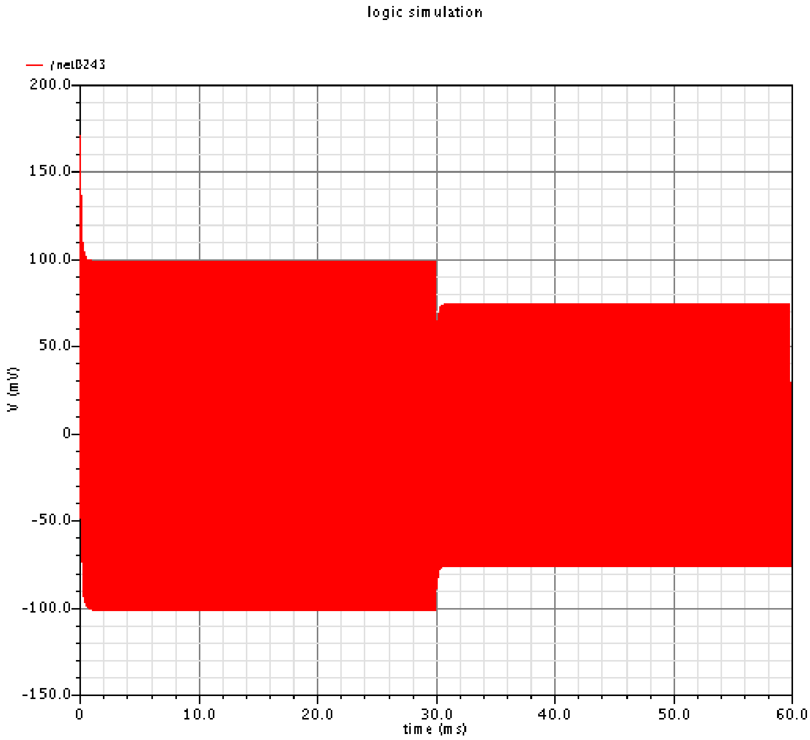

Figure 7.19. Lossy integrator response to two mixed signals

8. LOW POWER SWICTHED CAPACITOR INTEGRATOR DESIGN

Designing a circuit which consumes low power is a real challenge for a designer. For low power consumption consideration, there are many different architectures. Most of these architectures are focused on decreasing the quiescent power consumption. For low power switched capacitor integrator design, there could be several approaches reducing the power consumption without any major performance degradation. These are; low power opamp design, dynamic biasing and decreasing the capacitances at switching part which means power reduction by modification at the switched capacitor part. These three approaches will be examined in much detail in this chapter to investigate possible solutions for power reduction in switched capacitor integrator design.

8.1. Low Power Opamp Design

Low power opamp design has a major importance in low power integrated circuit design for two basic reasons; because, opamps are basic elements of many architectures in different electronic design areas and generally opamps are the most power consuming parts.

Ever decreasing channel lengths with the enhancement in integrated circuit technology adds another challenge in analog design. With short channel length transistors, gain of the transistors is less compared to relatively long channel devices. To obtain the required gain, the gain of the one stage won’t be enough and two or in some extreme cases three stages will be needed to obtain the required gain. However, adding extra gain stages adds a major design criterion to be examined carefully; stability. To design stable opamps, careful design steps are needed, because if the opamp is not stable, there could be savage errors in the overall system.

Another harsh design criterion comes with new technological trends such as low supply voltages. Actually, low supply voltage design idea comes with the same low power design aim. Reducing the power supply voltages pushes designers not to use or limit the usage of cascoding which is a very useful technique to obtain gain. However, adding series transistors adds extra drain-source voltage drop and this is a main limitation of output swing. If cascoding is not really necessary, it has been avoided by designers in low supply voltage designs.

Due to arguments briefly examined in this chapter, stability becomes a major concern. To design a stable opamp needs detailed calculations in every step of design the phase. Generally, to obtain a stable opamp can be summarized that input and output stages' (if three stages; second and third stages also) transconductance, compensation capacitance and load capacitance will be the main design parameters and they will determine the opamp's stability.

In detailed stability analysis of the two stage opamp in [6], to design a stable opamp:

$\frac{g_{m2}}{g_{m1}} = 4\frac{C_L}{C_C}$ g_{m1} is the transconductance of the first stage and g_{m2} is the transconductance of the second stage, C_L is the output capacitance and C_C is the compensation capacitance.

C_c is the compensation capacitance connected in parallel between second stage's input and output. C_c is used to split two poles far enough to not to cause oscillations. However, if the working frequency is relatively low, then it is possible to obtain a stable opamp without using any compensation capacitance.

To design a low power opamp for switched capacitor integrator, integration capacitance must be accepted and added as load capacitance and the design must be done due to the total load. Slew rate must be calculated to meet the required value and quiescent currents must be adjusted to these required specifications.

8.2. Dynamic Biasing

Another low power design technique is dynamic biasing. In this technique, basically bias currents and voltages are increased when needed and decreased when not needed.

Dynamic biasing naturally increases the slew rate and in this way driving capacitive loads will become easy and feasible with less current. Generally in dynamic biasing, applied input signals are measured at the input stage and then if high inputs are detected, transistors which are directly or indirectly controlled by this input voltage increase the biasing currents and with these increased biased currents, capacitive loads or compensation capacitance charging will take less time.

8.2.1. Adaptive biasing topology [12]

Adaptive biasing circuit is basically built by an NPN input differential pair, two transistors which detect the differences between the input voltages and a current mirror which gives the output current to the load resistor R. In this design, the main aim is to add extra tail current which will be activated due to the input signal conditions. Static power consumption is reduced and with this additional tail current, slew rate is enhanced. Adaptive biasing topology can be seen in Figure 8.1. and Figure 8.2. with bipolar and CMOS transistors.

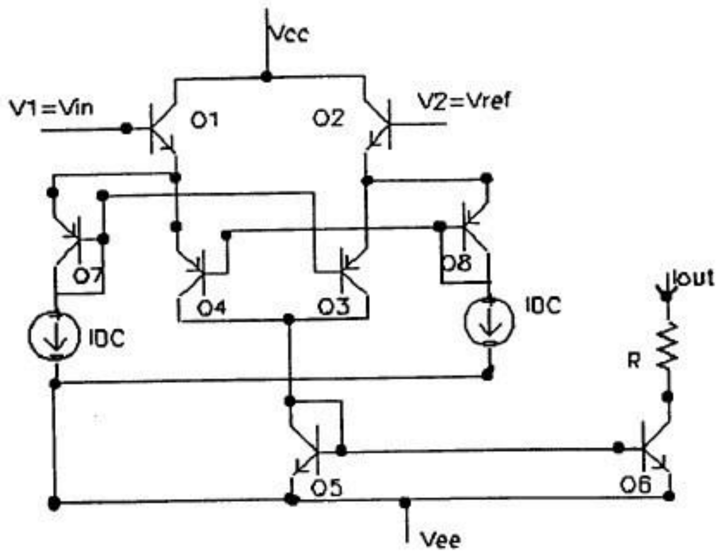

Figure 8.1. Adaptive biasing topology realized with bipolar transistors [13]

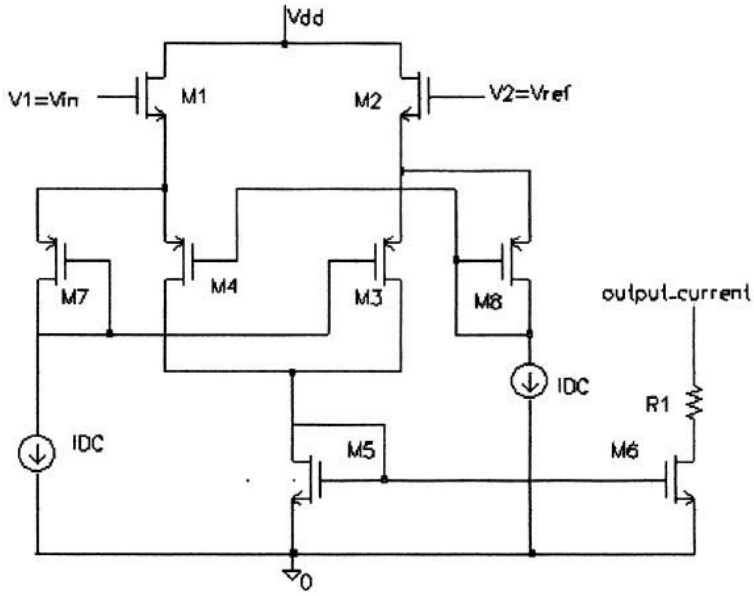

Figure 8.2. Adaptive biasing topology realized with CMOS [12]

8.2.2. Dynamic Biasing topology [14]

In this architecture, a replica of the input stage is used to measure the input and output of this replica is used to add extra current to the original circuit. In this way, slew rate is highly increased.

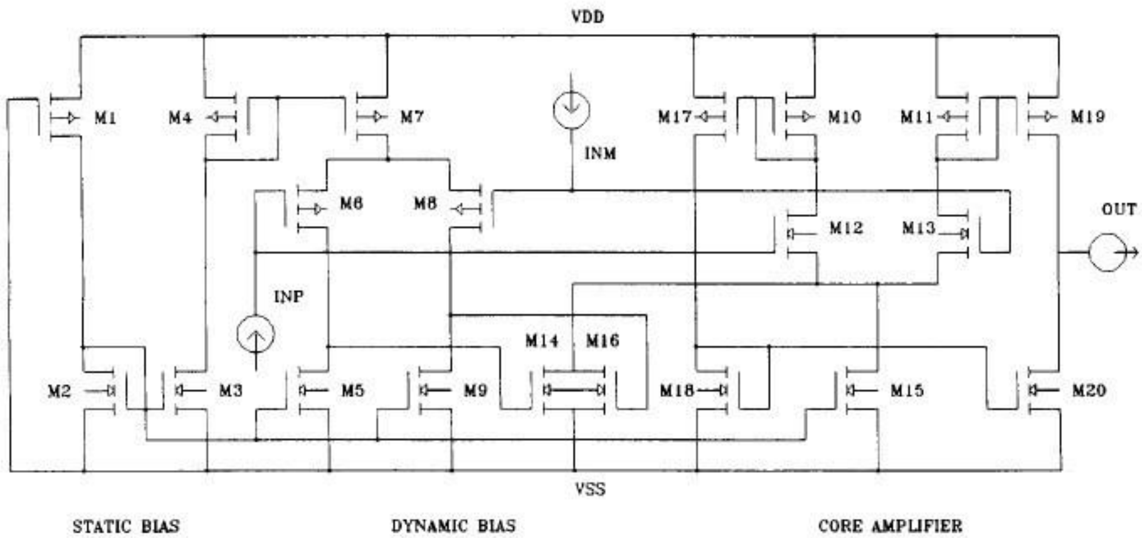

Figure 8.3. Dynamic biasing architecture [14]

8.3. Low Power integrator design with new architectures

To reduce the power consumption of the switched capacitor integrator, another approach is reducing the overall system's power by architectural modifications in switched capacitor part to reduce the capacitive load of the integrator. In this way, there will be less capacitive load and less slew rate requirement which will result reduction of the quiescent current.

Actually reducing the integration capacitance is generally a well known idea at designing of large time constant integrators. In large time constant integrators, integration capacitance must be very big compared to sampling capacitance. In this configuration, sampling frequency and sampling is dictated by the demand of the filter characteristics of the circuit. The only adjustable parameters are sampling and integration capacitances. To obtain a large time constant filter response, there must be large capacitance ratio between sampling and integration capacitance. Sampling capacitance could not be done much smaller than 100 fF (actually general tendency is using 500 fF as minimum) because of the error which is related with charge sharing due to the parasitic capacitances of the switches. Thus, integration capacitance must be done very big to maintain the capacitance ratio. And making this capacitance very big will result increasing of the quiescent current to charge and discharge this integration capacitance. Overall power is increased as a result of driving big capacitances.

Another main disadvantage of the big integration capacitance in IC design is, they consume much chip area which could be crucially important in some of the applications. Thus, reducing the capacitance is very important both power and chip area consumption criteria.

Several architectures are proposed to increase the integration capacitance, without actually increasing it physically. In these techniques generally input or output current is divided by capacitive dividers and small part of this current passes through sampling or integration capacitance. Effective capacitance which has been perceived by the system will be increased without actually increasing it. Generally they work with the same basic capacitive dividing principle, however different architectures show different behaviors which will be examined in detail.

8.3.1. The T-Cell Method [15]

To achieve a large capacitance ratio, first C_{in} must be small as possible and C_f must be as large as possible. To obtain this condition, an attenuator is placed before to the sampling capacitance and an amplifier is placed between the output and the integration capacitance. The conceptual schematic can be seen in Figure 8.4.

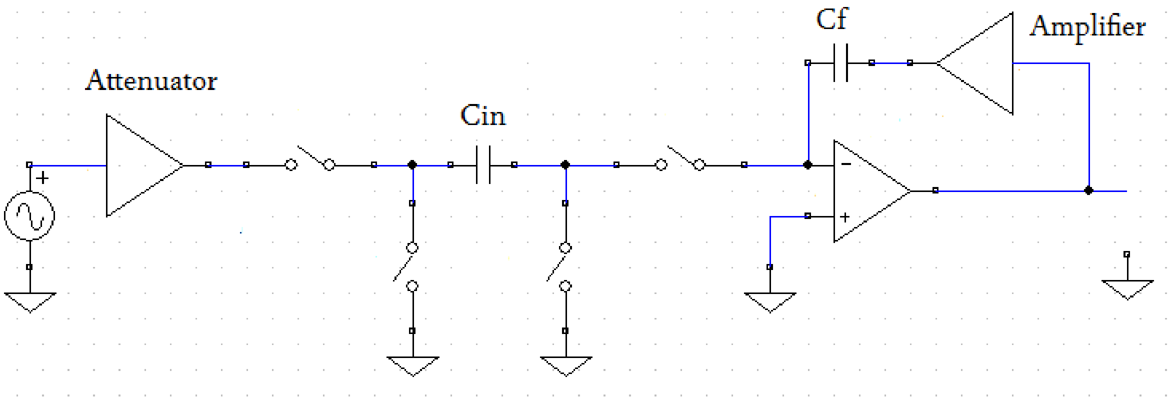

Figure 8.4. Conceptual implementation of large time integrator

The attenuator reduces the input signal by a attenuation factor and the feedback signal is increased by an amplification factor. Thus, overall effective capacitance ratio is increased by the product of these two factors. The main disadvantage of this system is that it needs an extra opamp which will be used between integration capacitance and output. This will cause increasing of power consumption and chip area. Attenuation does not need any active elements so; there will be no extra power consumption for attenuator. Attenuation is implemented with passive voltage division. T-Cell Method implements a small input capacitor by means of capacitive voltage division. Switched capacitive implementation of the system can be seen in Figure 8.5.

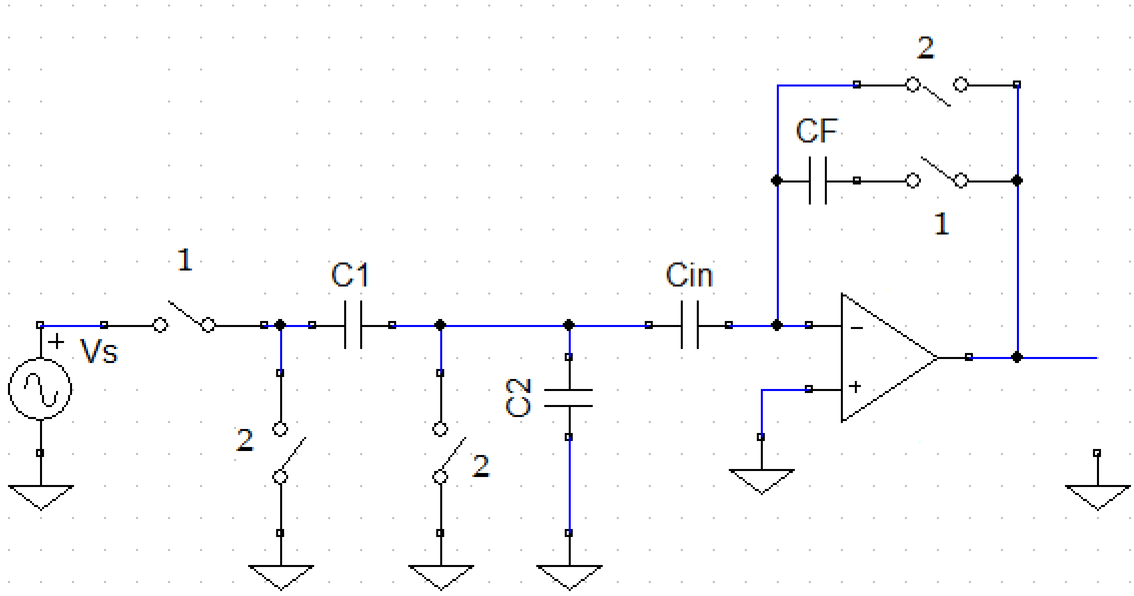

Figure 8.5. Large time constant integrator using T-Cell technique

C1 and C2 ensure that only a small fraction of the input charge is integrated by passing through integration capacitance C_f. The z-domain transfer function, when the output is sampled in phase 1 is given by

$$\frac{V_O(z)}{V_{in}(z)} = -\frac{C_1}{C_1 + C_2 + C_{in}} \frac{C_{in}}{C_F} \frac{1}{1 - z^{-1}} \tag{8.1}$$

8.3.2. The Split-Integrating Capacitor Technique [16]

The split-integrator technique uses same principle as T-Cell Method; however, implementation is parasitic-insensitive. It is done by throwing away a big fraction of the input charge and only passing a small fraction of it through integration capacitor.

In the conventional integrator, current comes from the input source and passes through the integration capacitor and the output voltage is obtained in this way, however, in split-integration capacitor technique, large part of the input current is sucked by the charge pulling network and only small fraction of it passes through the integration capacitor. In this way, integration capacitance looks big or input capacitance looks small, or in general their ratios look big without actually making them too small or too big.

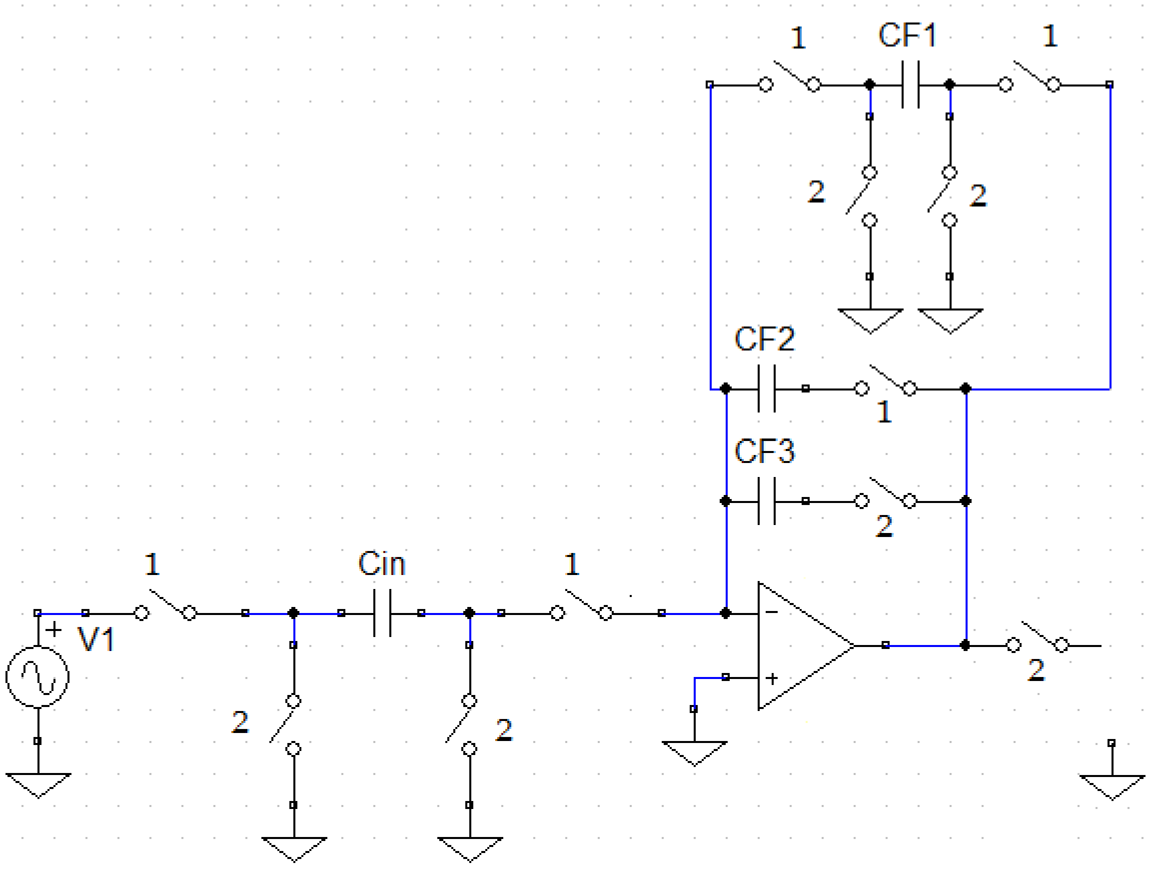

Figure 8.6. The split-integrator implementation

Implementation of the technique can be seen in Figure 8.6. Integration capacitor is split into three pieces as feedback capacitors, C_{F1}, C_{F2} and C_{F3}. In conventional integrator which has two phases, integration and sampling are performed only in phase 1, in phase 2 the integrator is idle. In the split-integrator technique both phases are used. In phase 1, the input charge is divided between C_{F1} and C_{F2}; in phase 2, the bigger capacitor C_{F1} discharges to ground and a large portion of the input charge is lost. The smaller capacitor C_{F2} which holds a small portion of the input charge, discharges through the integration capacitor and forms the actual integration operation. Only small portion of the input charge is integrated which effectively makes integration capacitor bigger than its actual value.

The z-domain transfer function can be written as

$$\frac{V_O(z)}{V_{in}(z)} = -\frac{C_{F2}}{C_{F3}} \frac{C_{in}}{C_{F2}+C_{F1}} \frac{z^{-\frac{1}{2}}}{1-z^{-1}} \qquad (8.2)$$

The relationship between the time constant and the clock frequency is

$$\tau = \frac{C_{F3}}{C_{in}} \frac{C_{F2} + C_{F1}}{C_{F2}} \frac{1}{f_{clk}} \tag{8.3}$$

To obtain a big integrator to sampling capacitor ratio, C_{F3} and C_{F1} must be large while C_{in} and C_{F2} must be small.

8.4. Charge Sharing Switched Capacitor Integrator

A novel charge sharing based switched capacitor integrator is proposed in this thesis. Mainly, it is based on reducing the effective input capacitor, in this way integration capacitor can be chosen much smaller while maintaining the same sampling to integration capacitance ratio. Reducing the integration capacitance will result in less current for the integration process which will be the main goal and purpose of this work, reducing the integrator power consumption. Another main advantage will be less slew rate requirement, which will be needed to obtain the same design specifications with less power consumption.

For biomedical applications large sampling to integration capacitance is needed for low frequency low pass filters. However, obtaining large capacitance ratio is not easy if this capacitor ratio is more than 100. As explained previously, sampling capacitor has a minimum value because of clock feedthrough, charge injection and other parasitic effects. If sampling capacitance is chosen as minimum value then, to obtain a large capacitance ratio, integration capacitance must be enlarged to maintain the same capacitance ratio. However, increasing the integration capacitance has several disadvantages; mainly it consumes more chip area and it needs more power to charge and discharge this big integration capacitance and it needs high slew rate. With this charge sharing architecture large capacitance ratios can be obtained without actually increasing chip area and power consumption.

Charge sharing switched capacitor architecture can be seen in Figure 8.7., to show more details about new architecture only switching and sampling capacitors is depicted, opamp and integration capacitance are not shown in this figure. In this configuration, charge of the main capacitance is shared with another capacitance, and charge which left on the main capacitance is sent to integration capacitance to be used in integration process. In general, switched capacitor integrator designs need two clock phases for proper operation and for this configuration, another clock phase is needed for charge sharing event.

The detailed working principle of this architecture will be examined in each clock phase in this section. In the first clock phase Q_1, main sampling capacitor is charged with the source signal and its output voltage is the same as the input signal at the last moment of the phase Q_1. At the second phase Q_2, C_s which is the main sampling capacitance and C_{shr} which is the charge sharing capacitance are parallel connected and the charge at C_s passes to C_{shr} until their voltages are equal to V_{shr}. Choosing charge sharing capacitance C_{shr} much bigger than the main sampling capacitance C_s, the remaining charge at C_s will be very few compared to its initial charge after Q_1 phase. At the Q_3 phase, charge which is left at C_s from the Q_2 phase will be sent to the integration capacitor for completing the integration process. However, at the Q_2 phase, charge remaining at C_{shr} must be reset to zero initial value for the next charge sharing process. It is done at the Q_1 phase before the charge sharing occurs. This charge cleaning can be done at the Q_3 phase, however if it is done at the Q_3 phase it can be charged by leakage current during the Q_1 phase and stored charge on C_{shr} will cause errors; for this reason, charge cleaning must be done at the Q_1 phase before charge sharing event happened at phase Q_2.

Charge sharing switched capacitor circuit is built by having a sampling capacitance of 0.1 pF as minimum reasonable value which will not cause much noticeable errors. Charge sharing capacitance is chosen as 0.9 pF to obtain a total at 10 times smaller effective capacitance than the original value.

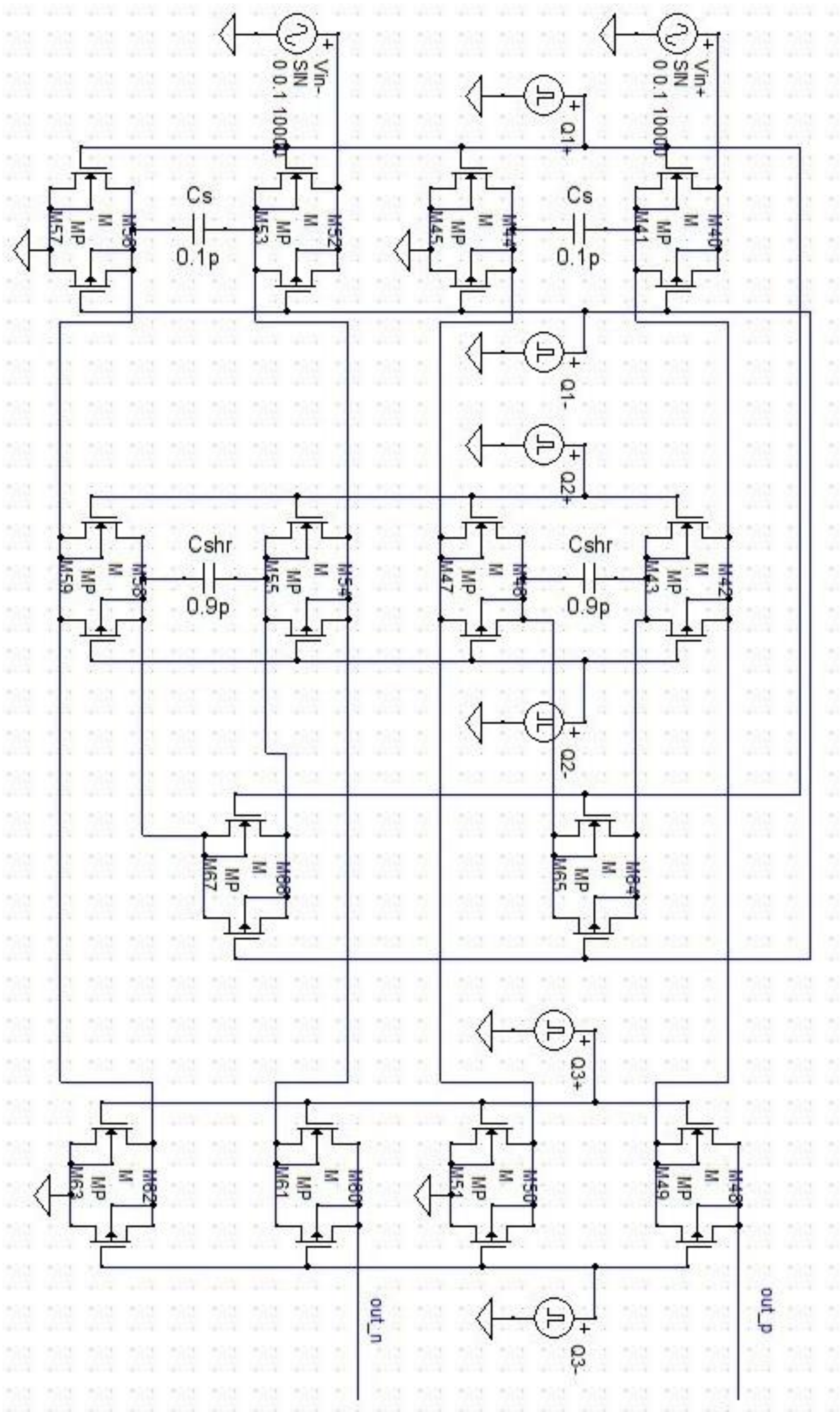

Figure 8.7. Charge Sharing Switched Capacitor Integrator without opamp and Cint

General switched capacitor integrator relationship between capacitors, sampling and input frequencies and input voltage amplitude is

C_s : Sampling Capacitor, C_{int} : Integration Capacitor

f_s : Sampling frequency, f : Input signal's frequency

V_{in} : Applied input signals amplitude

$$V_{out}(\mathrm{t}) = \frac{C_s . f_s}{C_{\text{int}}} \int V_{in}(t).dt \tag{8.4}$$

Considering the input signal as sinusoidal wave and the output is:

$$V_{out}(\mathrm{t}) = \frac{C_s . f_s}{C_{\text{int}}} \int V_{in} \sin 2\pi ft.dt = \frac{-V_{in}.C_s . f_s.\cos 2\pi ft}{C_{\text{int}}.2\pi f} \tag{8.5}$$

the amplitude of the output is: $$V_{out}(\mathrm{t}) = \frac{V_{in}.C_s . f_s}{C_{\text{int}}.2\pi f} \tag{8.6}$$

To find the effective sampling capacitor:

$V_{in}.C_s = Q_s$ when other capacitor C_{shr} parallel connected to C_s, total charge is

$$Q_{shr}(t=0) + Q_s = 0 + Q_s = Q_s \tag{8.7}$$

$$V_{in}.C_s = (C_s + C_{shr})V_{shr} \tag{8.8}$$

the amplitude of the output is: $$V_{out}(\mathrm{t}) = \frac{V_{in}.C_s . f_s}{C_{\text{int}}.2\pi f} \tag{8.9}$$

output voltage of the C_s and C_{shr} after charge sharing is

$$V_{shr} = \frac{V_{in}.C_s}{C_s + C_{shr}} \tag{8.10}$$

or equivalent capacitor value can be found to simlipfy equations

$$C_{s\_equ} = \frac{C_s}{C_s + C_{shr}} \tag{8.11}$$

Integrator output signal can be described with this new capacitance ratio

$$V_{out}(\mathrm{t}) = \frac{-V_{in}.C_s . f_s.\cos 2\pi ft}{C_{\text{int}}.2\pi f} \quad \& \quad C_{s\_equ} = \frac{C_s}{C_s + C_{shr}} \tag{8.12}$$

$$V_{out}(\mathrm{t}) = \frac{-V_{in}.C_s . f_s.\cos 2\pi ft}{(C_s + C_{shr}).C_{\text{int}}.2\pi f} \tag{8.13}$$

amplitude is: $$V_{out}(\mathrm{t}) = \frac{-V_{in}.C_s.f_s}{(C_s + C_{shr}).C_{\mathrm{int}}.2\pi f} \tag{8.14}$$

8.4.1. Sampling Capacitance Signals of Conventional Switched Capacitor Integrator

To observe exactly working principle and charging and discharging of charge sharing switched capacitor integrator, conventional switched capacitor integrator's sampling capacitance signal is examined first. In general, a capacitance's voltage is the same as the applied signal. However, in switched capacitor applications switches are not ideal switches which transfer all the charge and maintain the same voltage between the input and output of the switch. Due to the threshold voltage drop of a single MOS, transmission gate is used. However, there are undesirable parasitic effects such as clock feedthrough and charge injection error which were explained in detail in the previous sections. To minimize these effects, transistors which are used as switches must be as small as possible to reduce the clock feedthrough and charge injection error. However, shrinking the size of the transistors is not always a possible solution because, with small transistor sizes, conduction of the transistors will be less, causing long charging and discharging times. For high frequency applications, fast switches are desirable, resulting in big transistors as switches. Thus, there is a trade-off about the sizing of the switching transistors; small ones will cause less error; however, slow charging and discharging operations, large ones cause more error and fast charging and discharging operations. This common point about sizing of a transistor is that as small as possible channel length is desirable, because small channel length will both reduce parasitic capacitance and the resistance of the transistor.

Conventional switched capacitor integration is achieved with two operations charging the sampling capacitor with the input signal and discharging it to the integration capacitance. However, in these charging and discharging operations, clock feedthrough and charge injection will cause changing the output voltage of the sampling capacitance and the overall transferred charges to the integration capacitance will cause error to the output of the system. To see a clear picture of charging and discharging of a sampling capacitor, conventional switched capacitor integrator is simulated and its sampling capacitances voltage can be seen in Figure 8.8. Clock signals at Q_1 and Q_2 phases are scaled down from the original value to the almost capacitance signal value to be displayed on the same voltage scale with capacitance voltage.

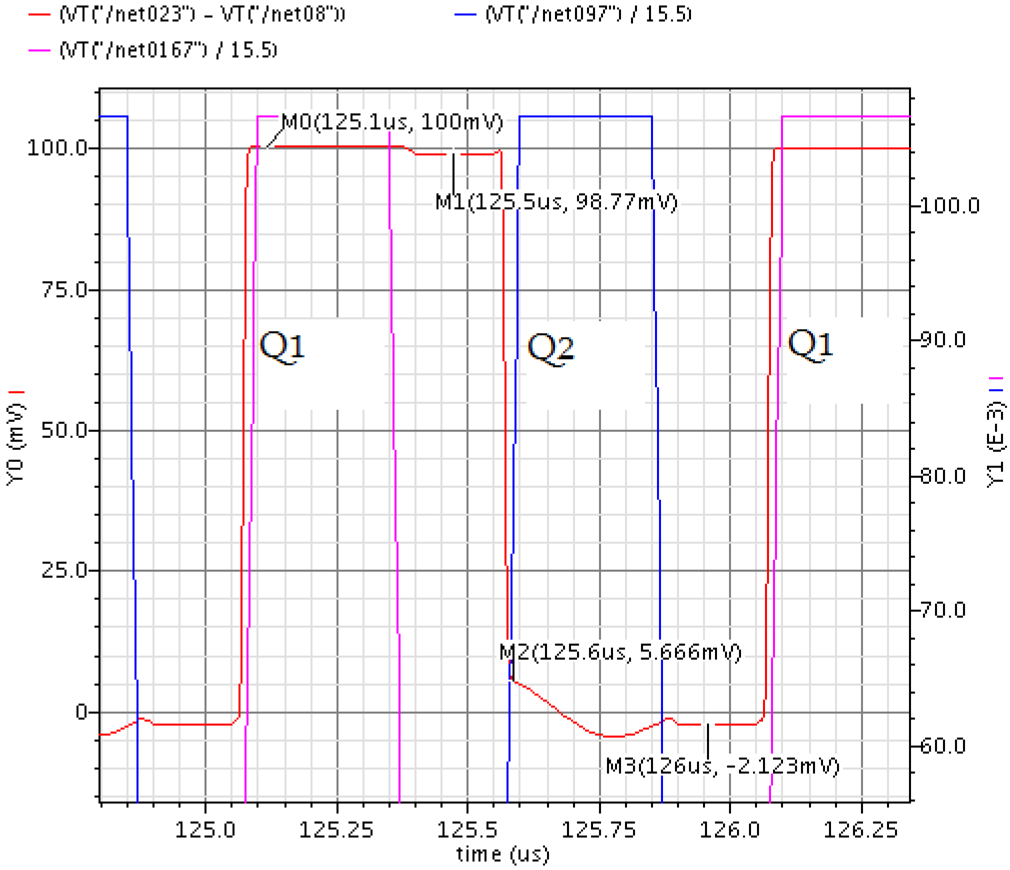

Figure 8.8. Charging and Discharging of Sampling Capacitance of Conventional Switched Capacitor Integrator

At middle of the conduction period of the switch, capacitance voltage is exactly the same as the applied voltage without any loss. However, when applied clock signal is removed due, the voltage on capacitance is decreased due to the charge injection and clock feedthrough effect, because the charge formed during the conduction of the NMOS and PMOS transistors is not equal. Electrons are more than holes at the conduction phase of NMOS and PMOS transistors. Charge formed during "ON" state of the transistors is given by this equation:

$$Q_{chnl} = W.L.C_{ox}(V_{gs} - V_{th}) \tag{8.15}$$

Since having the same gate-source voltage as the clock signal, having less threshold voltage of NMOS transistor, will cause forming more electrons in the NMOS transistor compared to fewer holes in the PMOS transistor. During the off to on state transition of both NMOS and PMOS transistors, electrons which are formed at the channel area of the NMOS transistor will recombine with holes which are formed at the channel area of the PMOS transistor. However, due to more electrons than holes, there will be remaining electrons after recombination which will cause charge injection and voltage drop at the sampling capacitance. This charge injection error can be reduced with symmetric architectures such as stray insensitive fully differential integrator architecture. With this configuration, there will be almost the same voltage drop (not equal voltage drop because of having different input voltages to the switches) at each input of the integrator and they will almost cancel each other with differential input stages common mode rejection property.

8.4.2. Sampling and Charge Sharing Capacitance Signals of Charge Sharing Switched Capacitor Integrator

Charge sharing switched capacitor integrator is the same as conventional integrator at Q_1 phase; sampling capacitance is charged with the input signal. At Q_2 phase, C_s and C_{shr} capacitances are parallel connected to each other which will cause transferring of charge from main the sampling capacitance C_s to the charge sharing capacitance C_{shr}. After charge sharing, each capacitance voltage will be the same as the other one; however, having different charges on each. In this work, to obtain ten times smaller effective capacitance than conventional one, charge sharing capacitance is nine times the main sampling capacitance. Charging and discharging of charge sharing switched capacitor integrator’s main sampling and charge sharing capacitance signals can be seen in Figure 8.9. and Figure 8.10. respectively. Clock signals at Q_1, Q_2 and Q_3 phases are scaled down from the original value to the almost capacitance signal value to be displayed on the same voltage scale with capacitance voltage.

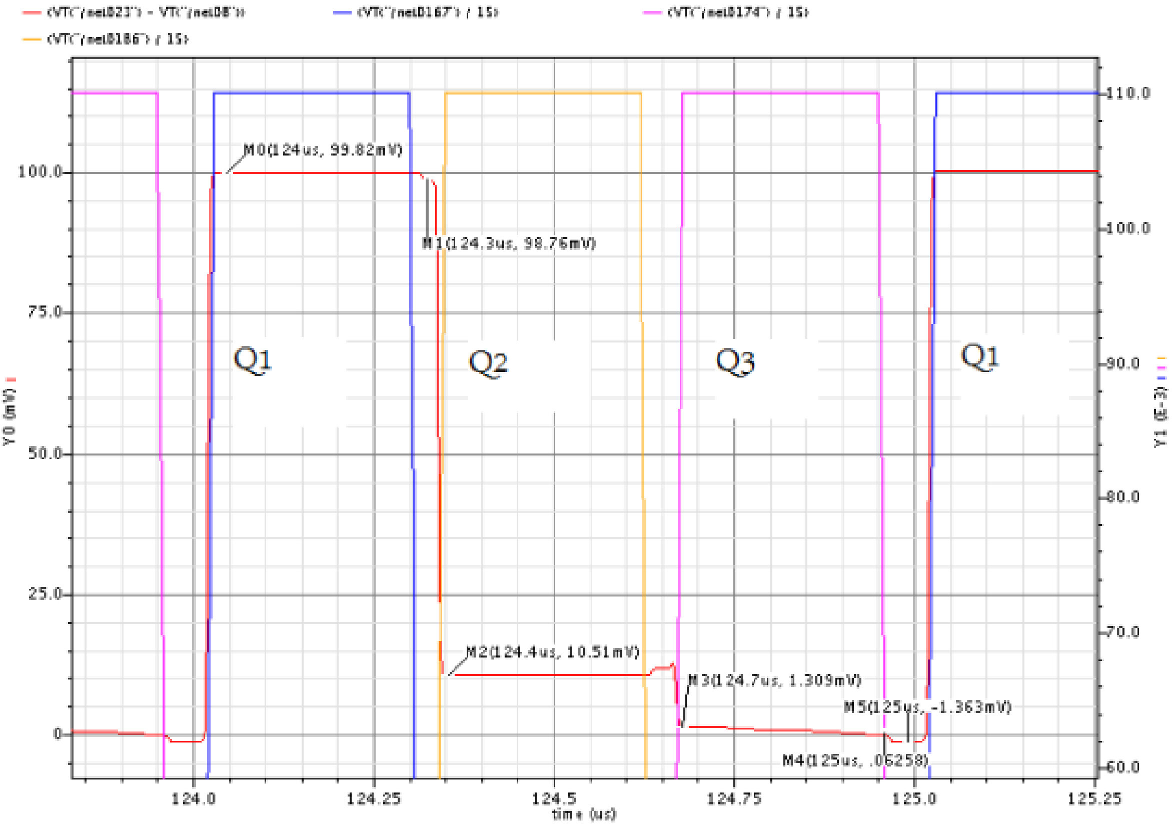

Figure 8.9. Charging and Discharging of Charge Sharing Switched Capacitor Integrator's main sampling capacitance

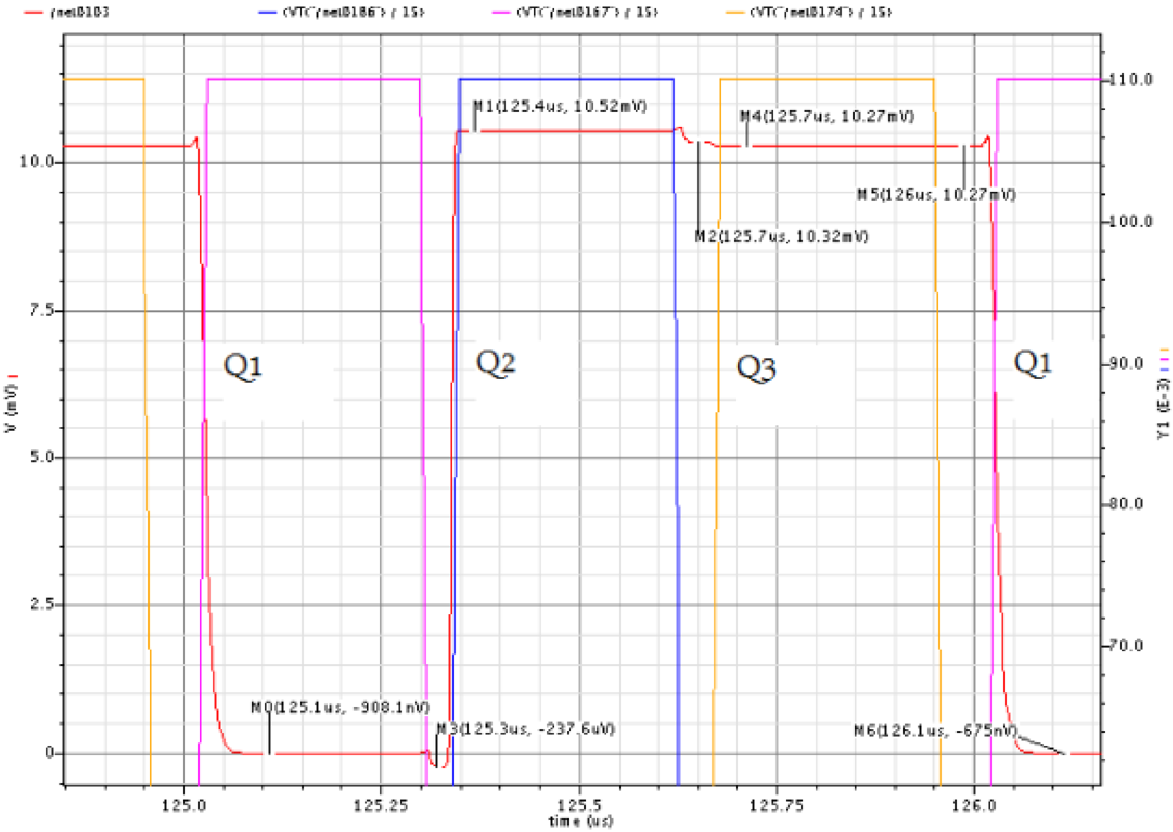

Figure 8.10. Charging and Discharging of Charge Sharing Switched Capacitor Integrator's Charge Sharing Capacitance

To test the charge sharing architecture and to compare with the conventional switched capacitor integrator, two circuits are built and simulated, one is conventional switched capacitor integrator and the other one is charge sharing switched capacitor integrator.

8.4.3. Conventional Switch Capacitor Integrator

A sine wave having 100 mV amplitude and 10 KHz frequency is applied as input signal. As sampling capacitance, 0.1 pF is used and 1.59 pF capacitance is used as integration capacitance. Sampling signals which control the switches are 1 MHz which means taking 100 samples in each applied signal period which is quite enough to reconstruct the integrated signal's shape at the output. The expected amplitude of the output signal is expected amplitude is 100 mV such as the input signals amplitude. The amplitude of the output signals amplitude can be given by:

$$V_{out}(\mathrm{t}) = \frac{V_{in}.C_s.f_s}{C_{\mathrm{int}}.2\pi f} \quad \Rightarrow \tag{8.16}$$

$$V_{in} = 100mV \quad \& \quad f = 10^4 \quad \& \quad f_s = 10^6 \tag{8.17}$$

$$\mathrm{C}_s = 0{,}1pF \quad \& \quad \mathrm{C}_{\mathrm{int}} = 1{,}59\,pF \tag{8.18}$$

$$V_{out}(\mathrm{t}) = \frac{0{,}1.0{,}110^{-12}.10^6}{1{,}5910^{-12}.2\pi 10^4} = 10^{-1} = 100mV \tag{8.19}$$

Simulation result of the conventional switched capacitor integrator can be seen in Figure 8.11.

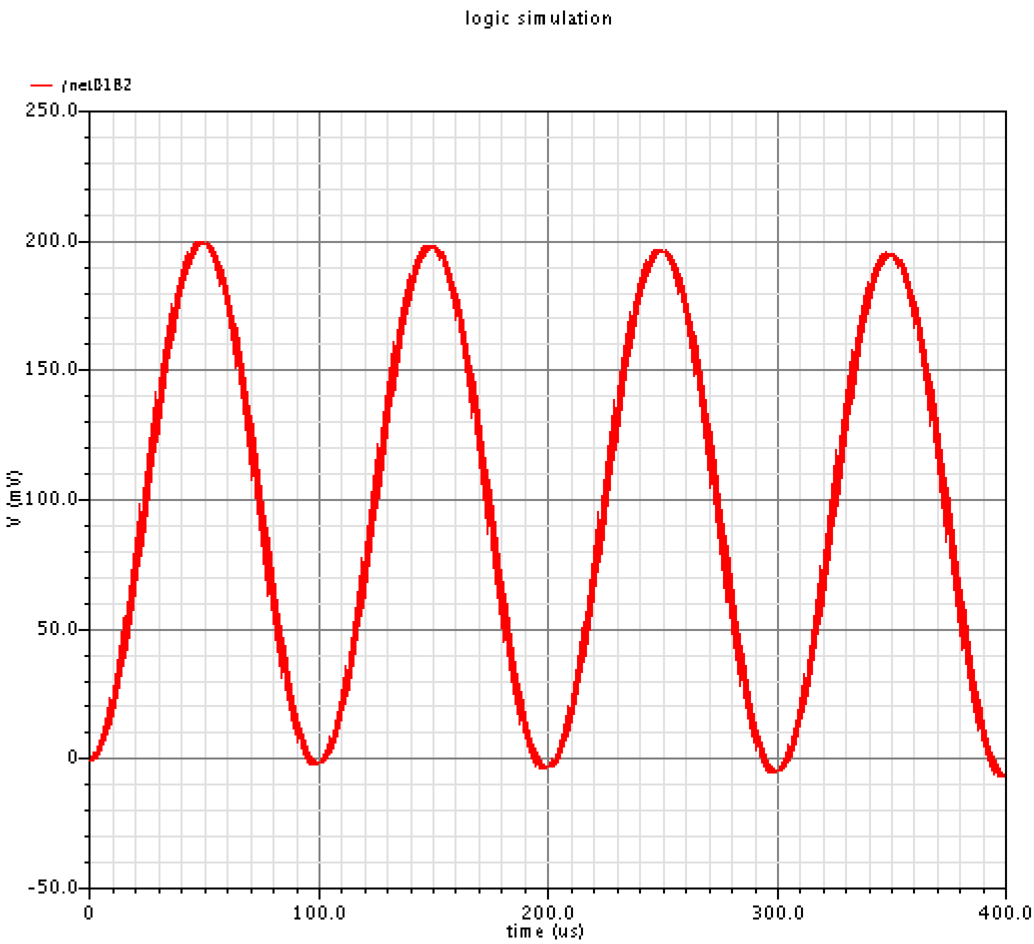

Figure 8.11. Output of the Conventional Switched Capacitor Integrator

No load is used for this simulation; however, to test the circuit when having a capacitive load, a 1 pF capacitance is added to the output of the integrator. Output of the integrator with 1 pF load capacitance can be seen in Figure 8.12.

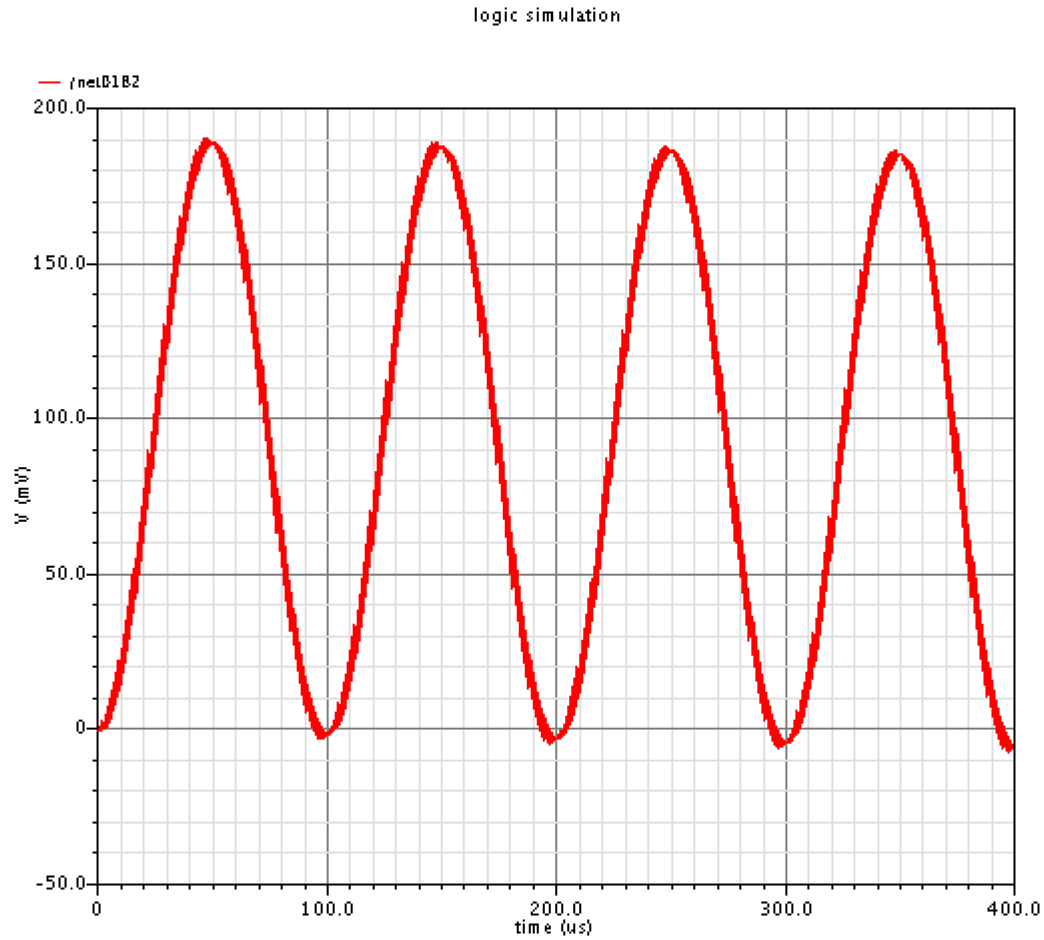

Figure 8.12. Output of the Conventional Switched Capacitor Integrator with 1pF load

Amplitude of the output signal is less than 200 mV as expected, because of the loading effect of 1 pF capacitance. As mentioned earlier, output of the integrator settles to dc zero offset after some time. Settling of the conventional integrator can be seen in Figure 8.13.

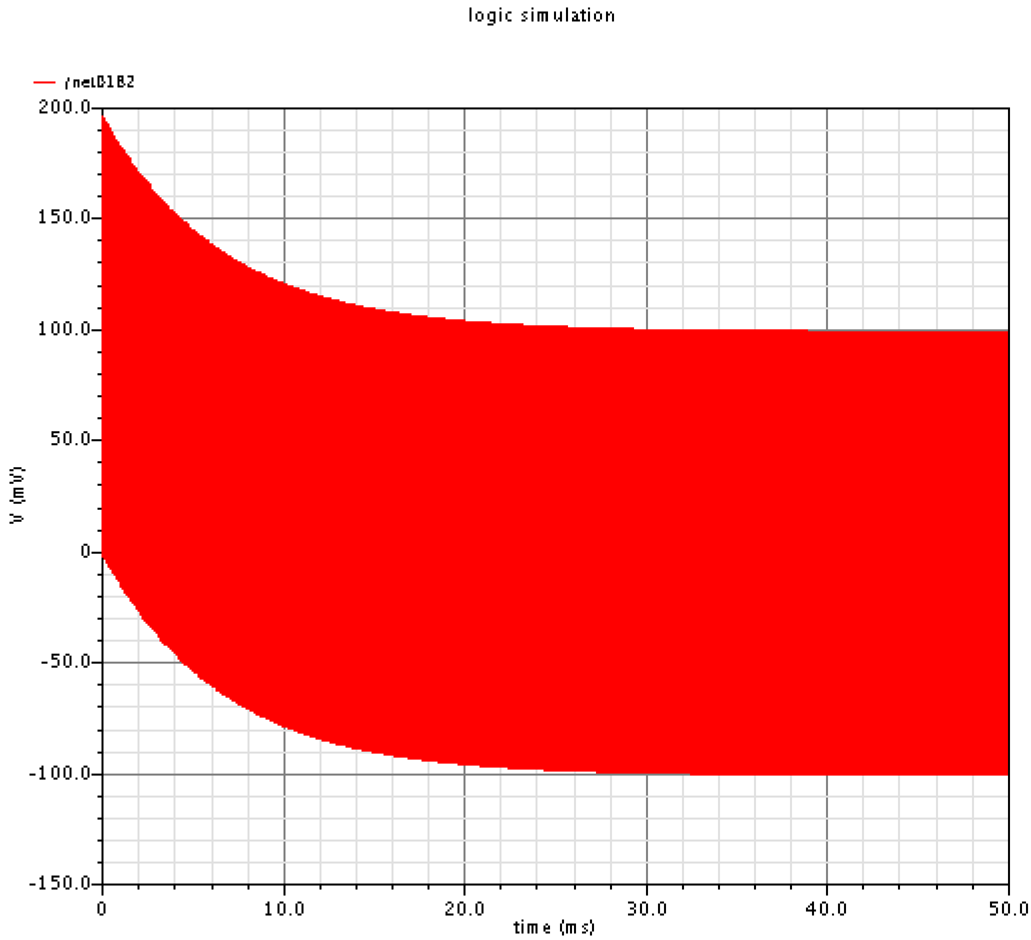

Figure 8.13. Settling of the Conventional Switched Capacitor Integrator

To reduce the settling time, lossy integrator configuration is used. After simulation, the signal settling takes less time compared to its original settling time. As can be seen in Figure 8.13. and Figure 8.14. settling takes approximately 1.5 ms for lossy integrator configuration; however, it takes almost 30 ms for the conventional integrator.

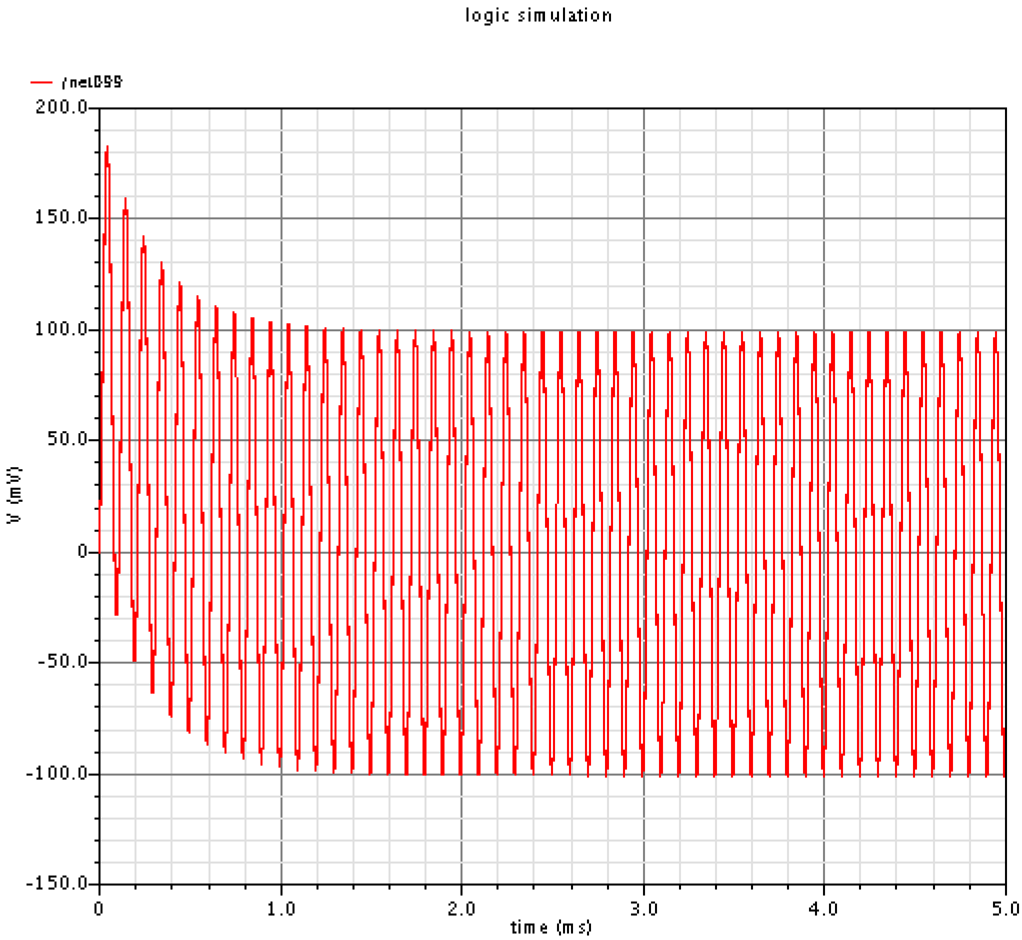

Figure 8.14. Settling of the Conventional Lossy Integrator

8.4.4. Charge Sharing Switched Capacitor Integrator

For charge sharing switched capacitor integrator, the same input signal is used which is used for the conventional switched capacitor integrator. Main sampling capacitance is 0.1 pF and charge sharing capacitance is 0.9 pF. With this configuration, effective sampling capacitance is 0.01 pF and to obtain the same output signal as conventional ones, integration capacitance can be done 10 times smaller than its original value. 1.59pF integration capacitance is used in conventional integrator and in charge sharing based one 0.159 pF integration capacitance is used. 1 pF capacitance is used as load. Output of the charge sharing switched capacitor integrator can be seen in Figure 8.15.

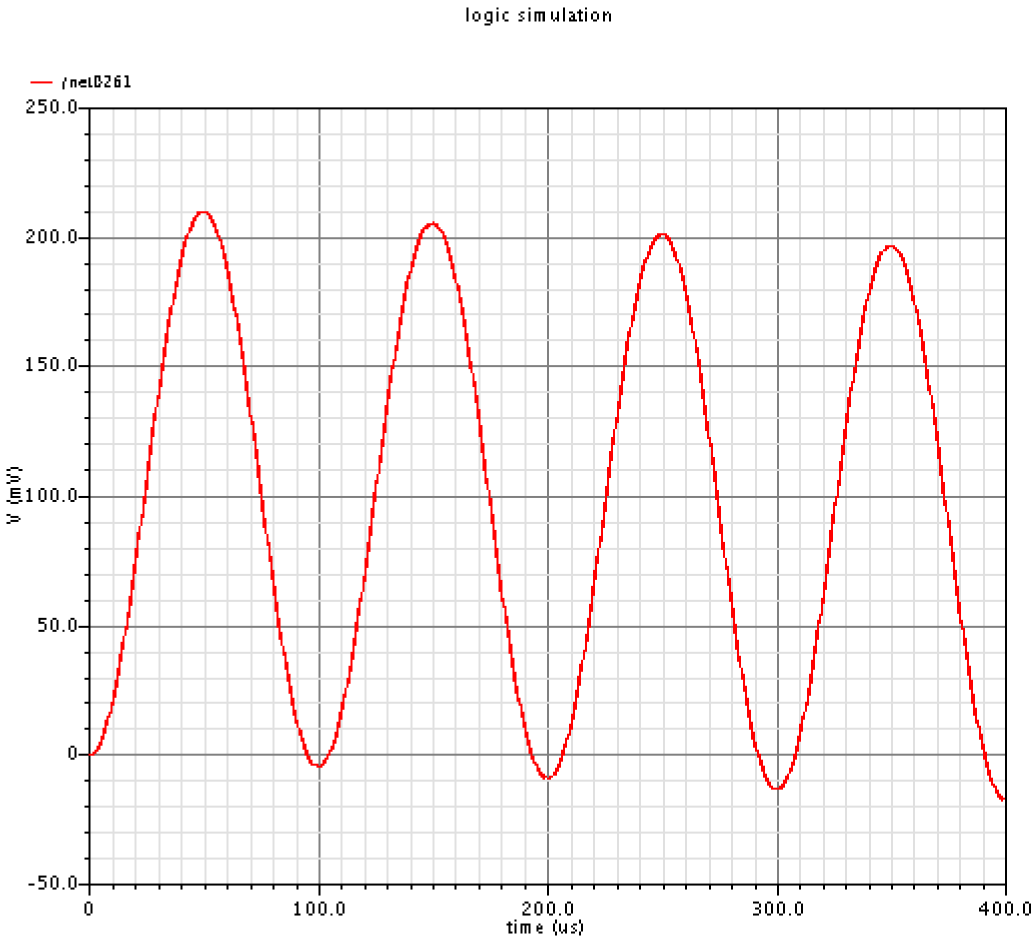

Figure 8.15. Output of the Charge Sharing Switched Capacitor Integrator

Settling of the charge sharing switched capacitor integrator can be seen in Figure 8.16. It takes 30 ms to settle for the conventional switched capacitor integrator, however, it takes 3 ms to settle the charge sharing based ones which is very meaningful considering the reduction of the integration capacitance by ten times. Settled final output signal of the charge sharing switched capacitor integrator can be seen in Figure 8.17.

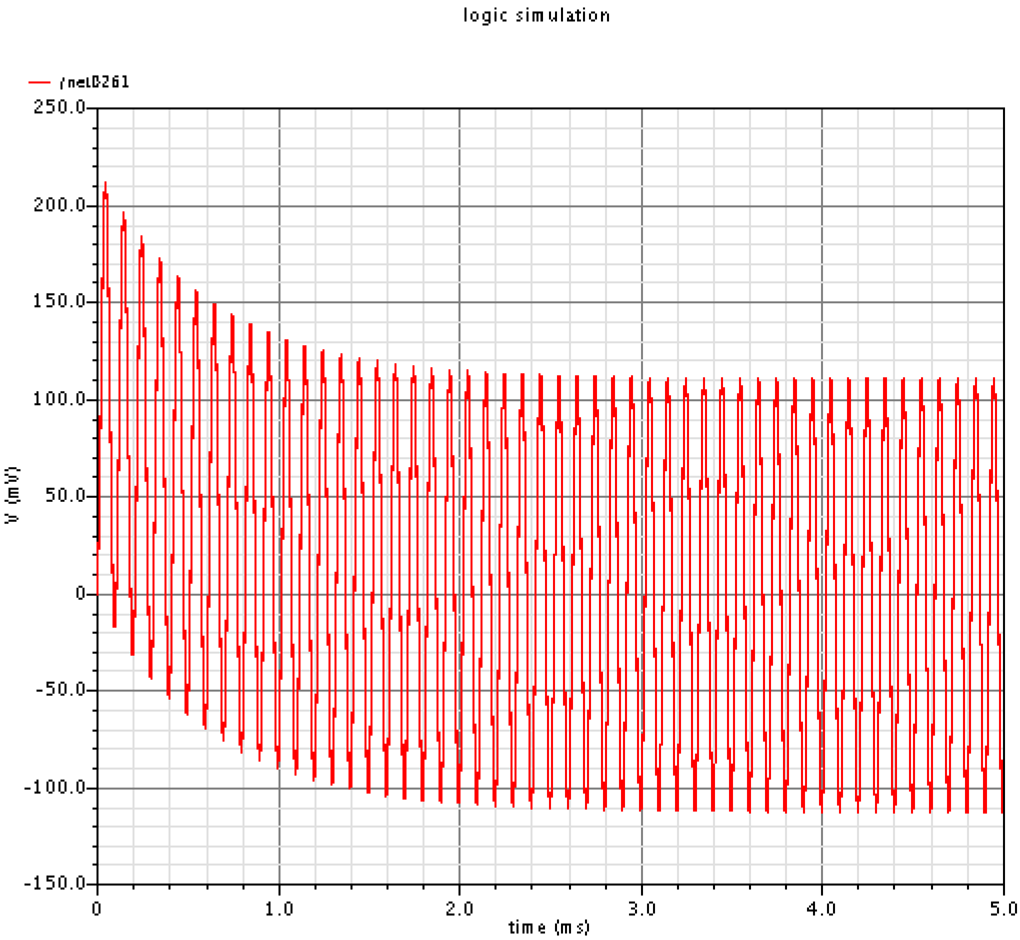

Figure 8.16. Settling of the Charge Sharing Switched Capacitor Integrator

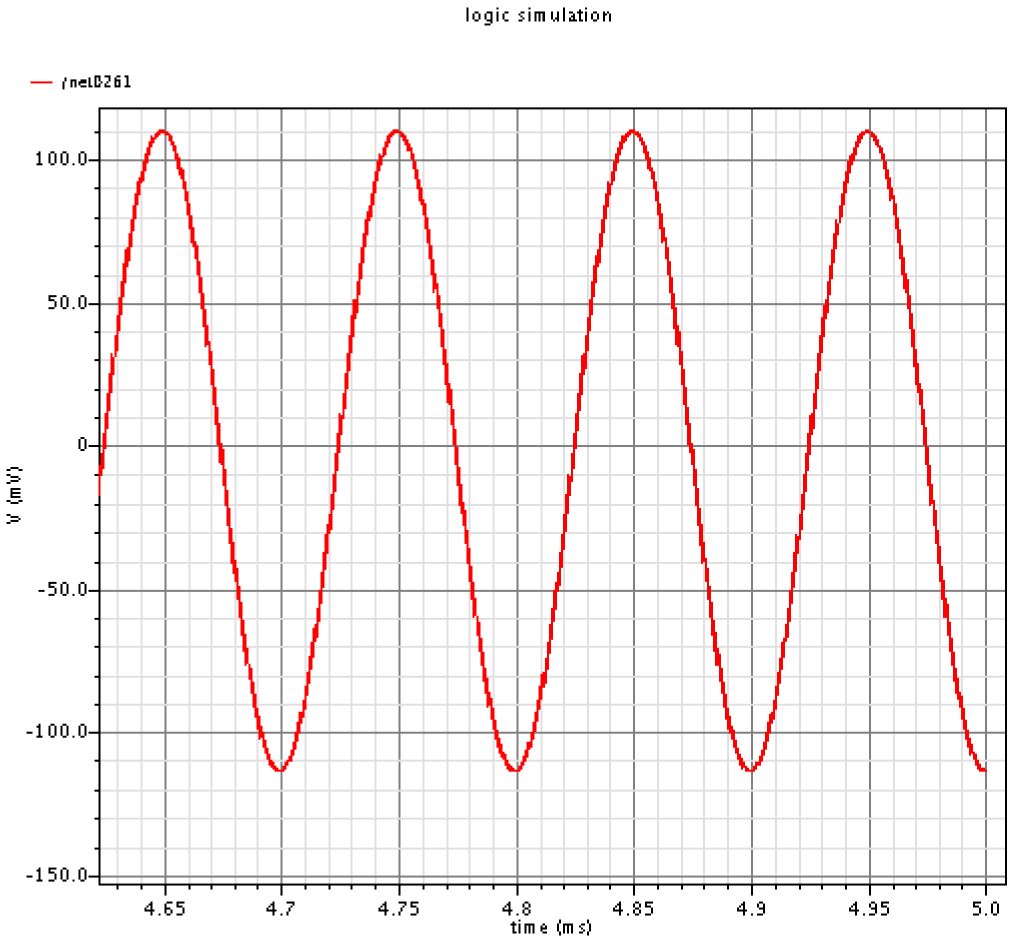

Figure 8.17. Settled output of the Charge Sharing Switched Capacitor Integrator

Lossy integrator configuration is used again for the settling time reduction and the output of the charge sharing switched capacitor lossy integrator can be seen in Figure 8.18. It takes only one signal period to dissipate the charge which causes the integration offset. The error of even the first signal period is quite small compared to almost 80 % error of the conventional switched capacitor lossy integrator.

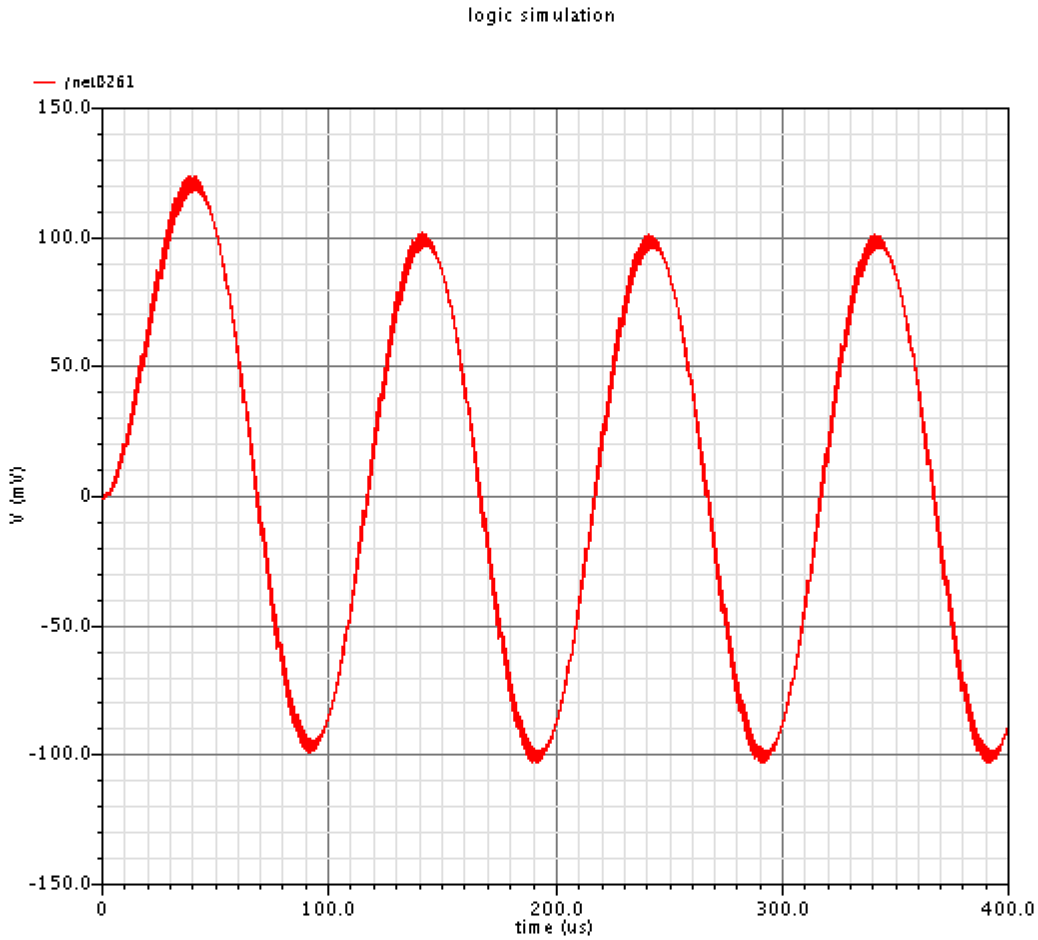

Figure 8.18. Output of the Charge Sharing Switched Capacitor Lossy Integrator

As mentioned at the integrator offset part, lossy integrator configuration causes phase error which can easily be seen in Figure 8.18.

8.4.5. Design Considerations of Charge Sharing Switched Capacitor Integrator

Designing charge sharing switched capacitor integrator is almost the same as designing conventional switched capacitor integrator with several additions. In general, main emphasis must be considering the size of the capacitances and the size of the switches at the design of switched capacitor integrators. Accomplishing charging and discharging events are very important for the overall performance of the system. If noise specifications are satisfactory, choosing the size of capacitances as small as possible is very important for both performance and power considerations. This is very important for two reasons; first reason is that reducing the sampling capacitance will cause reduction of the integration capacitance which will in turn result in reducing the power consumption. Second reason of choosing capacitances as small as possible is to reduce the charging and discharging time. As mentioned previously, charging and discharging time constant is the product of the capacitance and switching transistor resistance. Generally, seven times of this time constant is accepted to be accurate enough for proper charging and discharging. For high frequencies, to obtain small charging and discharging times, choosing capacitances small is desirable.

The design task becomes more complicated when considering all parasitic effects and performance criteria. Prior design specifications must be chosen first; then, other design criteria must be included into the design phase and in each step, the design must be rechecked against desired specifications.

Another design issue about charge sharing switched capacitor integrator is making charge sharing capacitance relatively big compared to the main sampling capacitance. Main sampling capacitance is chosen according to timing specifications of both switch resistance and sampling capacitance and at high frequency designs most probably it will work border of the maximum allowable limits. This means that choosing the charge sharing capacitance larger than the main capacitance can violate charging and discharging timings. However, this problem can be overcome by making charge sharing capacitance switches larger than main sampling capacitance switches.

8.4.6. Low Power Charge Sharing Switched Capacitor Integrator

General approach to reduce the power consumption of a circuit is to decrease the quiescent current of the circuit and to decrease the capacitances and the resistive loads. To decrease the power consumption of the switched capacitor integrator all capacitances must be reduced to allowable limits to decrease the load of the output stage of the opamp. Less load to the output stage will allow to use less quiescent current at the output stage of the opamp. Considering that main power consumption of the opamp comes from the output stage, means that reducing the quiescent current of the output stage will cause less power consumption of the overall integrator.

For previous switched capacitor and charge sharing switched capacitor integrator designs, the current passing through the integration capacitance was relatively small (10 nA) and the integrator was working at 10 KHz of input signal and 1 MHz of sampling signal. At this frequency, power consumption will be also low. Actually it is a well known trend that increasing frequency result in increasing power consumption. In switched capacitor integrators, increasing the sampling frequency causes increasing the transferred charge in a given time which will result increasing of the current as main integration signal. So, to test the effectivity of charge sharing switched capacitor integrator about power consumption, high frequency input and sampling signals can be used.

For power consumption comparison, conventional switched capacitor integrator and charge sharing switched capacitor integrator will be designed at same output, input and sampling specifications. 100 mV amplitude and 1 MHz sine signal is applied at the input of the two integrators with 100 MHz sampling frequency. Minimum sampling capacitance is chosen as 1 pF rather than 0.1 pF, because making sampling capacitance 1 pF cause ten times current passing through the integration capacitance and needs ten times current at the output of the opamp which will be very useful to test the effectivity of the charge sharing switched capacitor integrator compared to the conventional one.

$$V_{in} = 0.1V \sin 2\pi 10^6 t \quad \& \quad f_s = 10^8 \tag{8.20}$$

$$\mathrm{C}_s = 1pF \quad \& \quad \mathrm{C}_{\mathrm{int}} = 15.9\mathrm{pF} \tag{8.21}$$

$$V_{out}(\mathrm{t}) = \frac{V_{in}.C_s.f_s}{C_{\mathrm{int}}.2\pi f} \tag{8.22}$$

$$V_{out}(\mathrm{t}) = \frac{0{,}1.10^{-12}.10^8}{15{,}910^{-12}.2\pi 10^6} = 0{,}1V \tag{8.23}$$

current passing through integration capacitance is:

$$I_{C\mathrm{int}} = V_{in}.C_s.f_s = 0{,}1.10^{-12}.10^8 = 10^{-5}A = 10\mu A \tag{8.24}$$

Thus, for proper functioning of this conventional integrator, output stage must provide at least 10 μA for integration capacitance. Another current consumption will be at the load capacitance, and for 1 pF load capacitance current consumption is

$$R_s = \frac{1}{C_L.2\pi f} \tag{8.25}$$

$$I_{load} = V_{out}.C_L.2\pi f = 0{,}1.10^{-12}.2\pi.10^{6} = 0{,}618.10^{-6} = 0{,}618\mu A \tag{8.26}$$

For 10 pF load 6.18 μA will be needed, however, for low power integrator design output load will be small considering general power reduction of the system not for only reduction at the integrator part. For this reason, 1 pF load will be used as capacitive load for both conventional switched capacitor and charge sharing switched capacitor integrator. Also, it must be remembered that for low power applications self loads of the output stages must be taken into account too.

For different output stage quiescent currents, output signal is plotted for comparison. First, 2.22 μA output stage quiescent current is used for simulation and it obvious that integrator will not respond correctly because of 6.18 μA demanding of integration capacitance for proper integration of conventional switched capacitor integrator, however, for comparison, it is simulated and result can be seen in Figure 8.19. Phase error of the integrator can easily be seen in Figure 8.19.

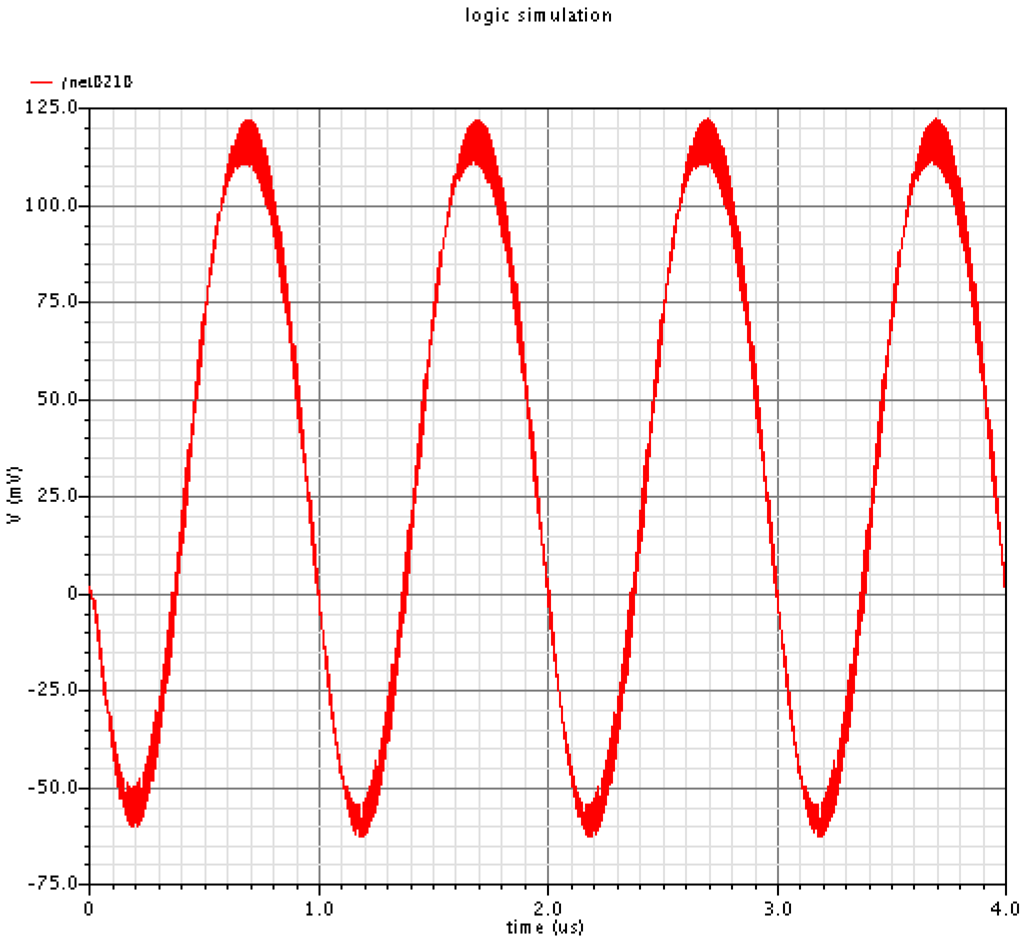

Figure 8.19. Conventional Switched Capacitor Integrator with 2.22 µA output stage

Second simulation is done with the opamp whose output stage quiescent current is 21.5 µA and result can be seen in Figure 8.20. Phase error is less compared to 2.22 µA output stage quiescent current opamps, but phase error is still a problem for this configuration.

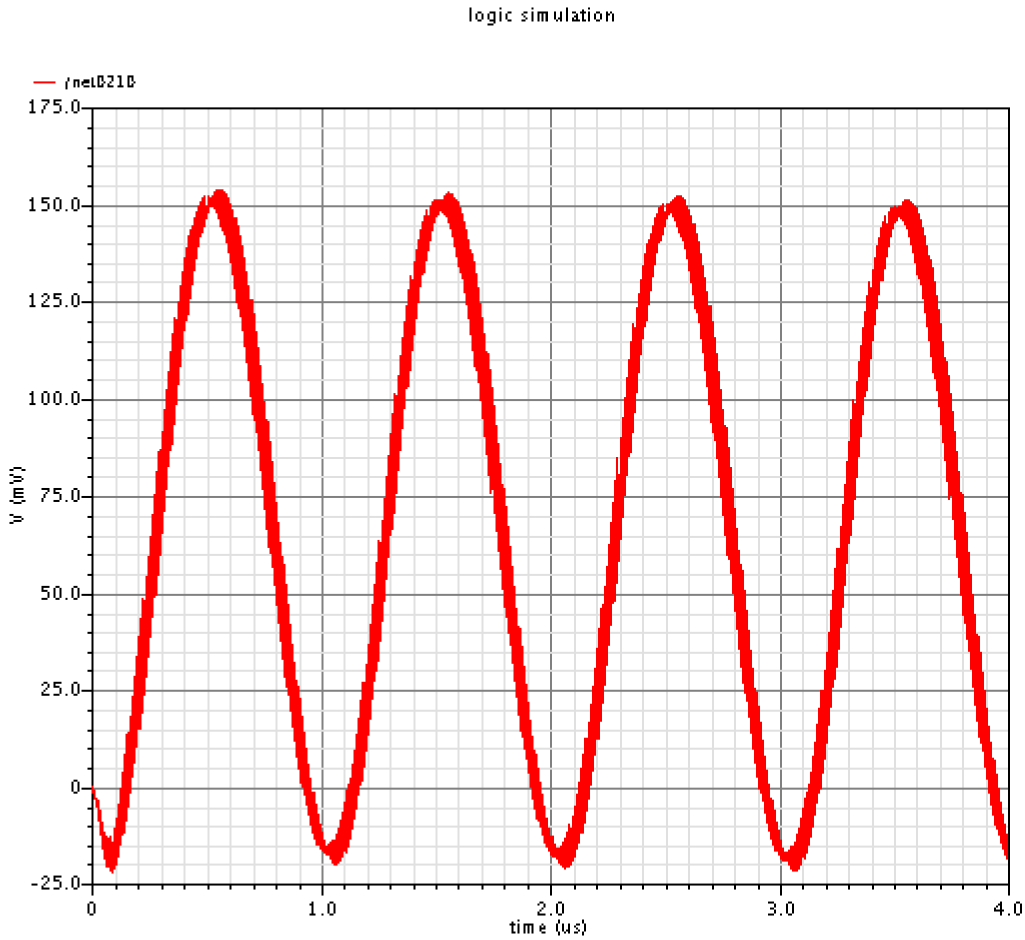

Figure 8.20. Conventional Switched Capacitor Integrator with 21,5 µA output stage

For the output stage of having 224 µA quiescent current, output signal is depicted in Figure 8.21. Its phase error is almost zero as can be seen in figure.

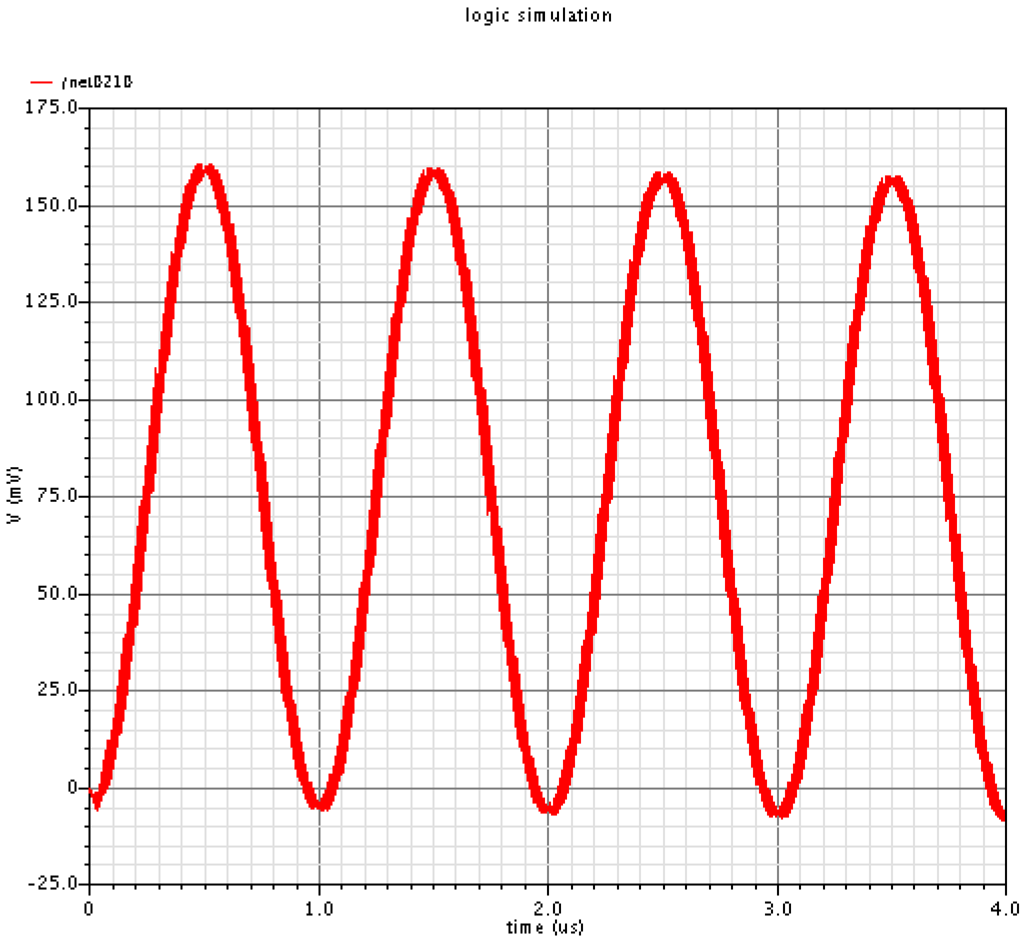

Figure 8.21. Conventional Switched Capacitor Integrator with 224 µA output stage

For charge sharing switched capacitor integrator design at high frequency, input signal and sampling signal specifications are same and main sampling capacitor is same as previous conventional one. Charge sharing capacitance is nine times of the main sampling capacitance which is 9 pF. To reduce the effective sampling capacitance by ten times, integration capacitance can be done ten times smaller which is 1.59 pF. Output signals amplitude can be given by

$$V_{in} = 0{,}1V \sin 2\pi 10^6 t \quad \& \quad f_s = 10^8 \tag{8.27}$$

$$\mathrm{C}_s = 1pF \quad \& \quad \mathrm{C}_{shr} = 9\mathrm{pF} \quad \& \quad \mathrm{C}_{\mathrm{int}} = 1.59\mathrm{pF} \tag{8.28}$$

$$V_{out}(\mathrm{t}) = \frac{V_{in}.C_s.f_s}{(C_s + C_{shr}).C_{\mathrm{int}}.2\pi f} \tag{8.29}$$

$$V_{out}(\mathrm{t}) = \frac{0{,}1.10^{-12}.10^8}{(10^{-12} + 9.10^{-12})1.5910^{-12}.2\pi 10^6} = 0{,}1V \tag{8.30}$$

current passing through integration capacitance is:

$$I_{C\text{int}} = V_{in}.C_{s\_effective}.f_s = 0{,}1.10^{-13}.10^{8} = 10^{-6}A = 1\mu A \tag{8.31}$$

For comparison of the output signals with the same quiescent output stage currents of the conventional switched capacitor integrator, first, charge sharing switched capacitor integrator is simulated with 2.22 µA output stage quiescent current and it is depicted in Figure 8.22. Phase error of the output signal is little but it exists and amplitude is less than expected and less than the conventional ones; however, the output signal has very small internal oscillation errors due to having ten times smaller integration capacitance.

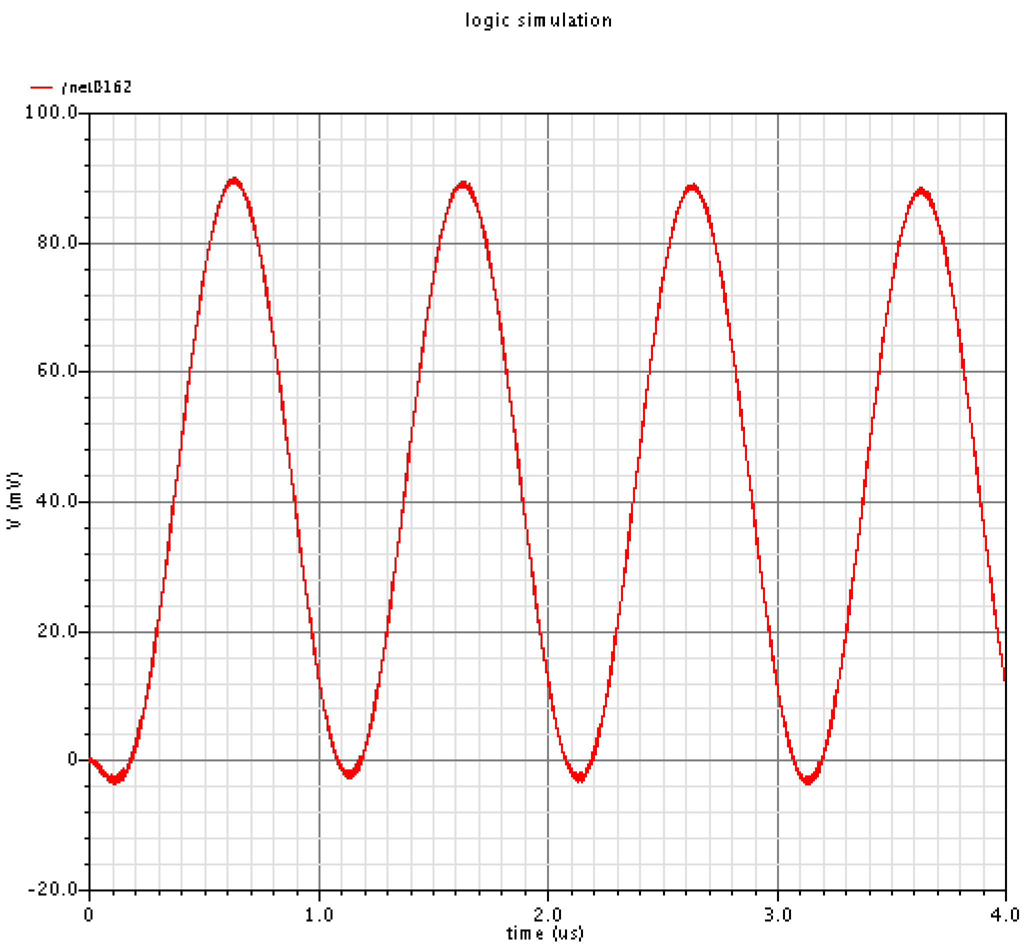

Figure 8.22. Charge Sharing Switched Capacitor Integrator with 2.22 µA output stage

For the output stage having 21.5 µA quiescent current, output signal can be seen in Figure 8.23. Its phase error is almost zero.

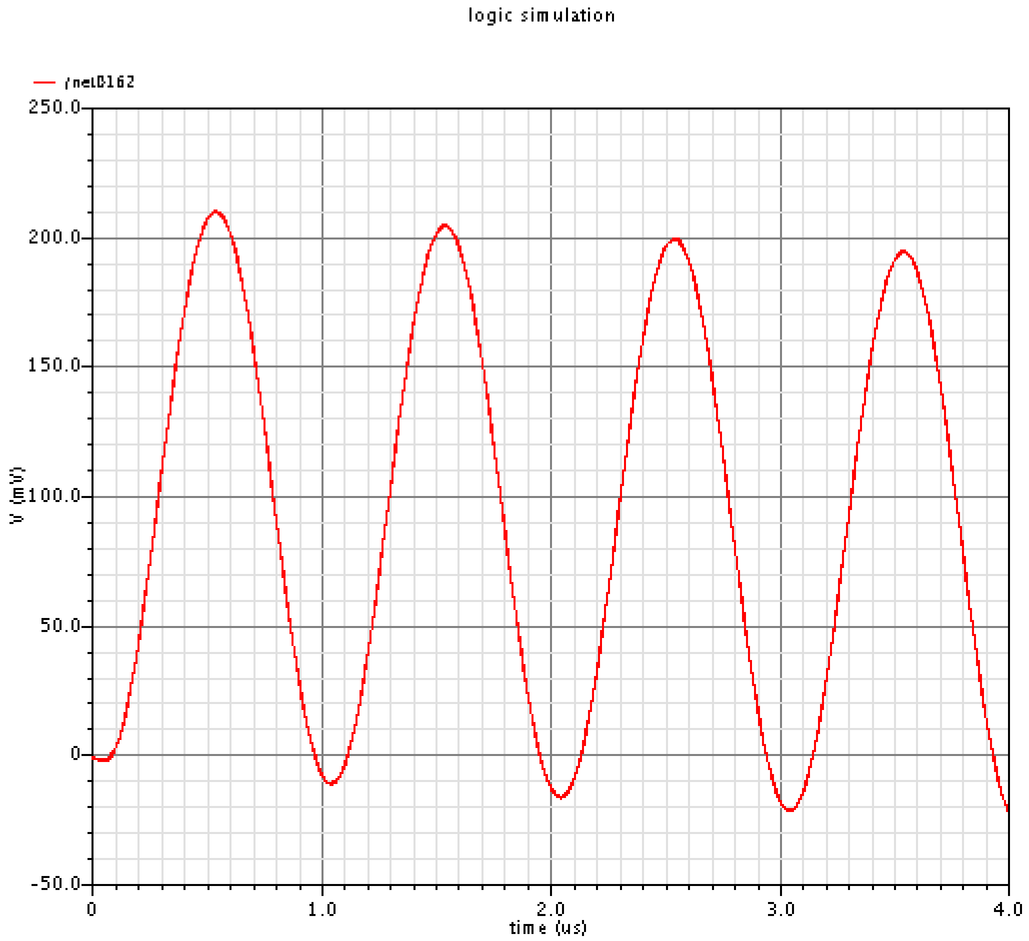

Figure 8.23. Charge Sharing Switched Capacitor Integrator with 21.5 µA output stage

For the output stage having 224 µA quiescent current, output signal is depicted in Figure 8.24.

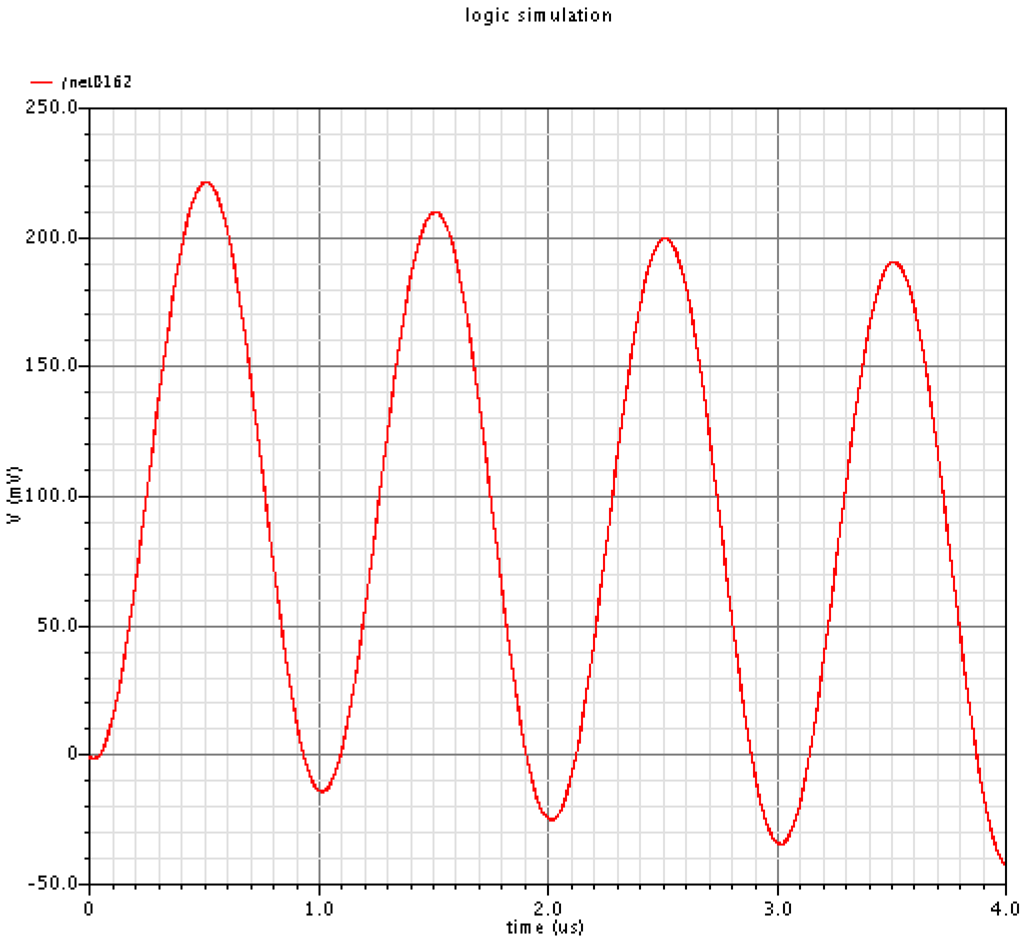

Figure 8.24. Charge Sharing Switched Capacitor Integrator with 224 μA output stage

9. CONCLUSION AND FUTURE WORK

9.1. Conclusion

In this work, switched capacitor integrator design is investigated mainly for power consumption consideration. Its main power basically comes from the opamp; however, all parts are closely related to each other including the switching part and the capacitances. Because of this inter dependency; designing a switched capacitor integrator becomes a hard task to accomplish.

Mainly from basic switching part to the overall integrator design, in each step, it has been tried to be examined thoroughly, including parasitic effects with advantages and disadvantages perspective.

At relatively low input frequencies and sampling signals, low power design can be achieved without much effort, because switches can be achieved much smaller which will result less charge injection and clock feedthrough error. And at low frequencies, the quiescent currents of the opamp will be less with less slew rate requirement. However, when it comes to design at high frequencies, all design parameters must be examined carefully with regarding of the other integrator parts demands. Two main problems arise; one is designing fast switches with as small as possible dimensions to minimize clock feedthrough and charge injection error and the other problem is current which is needed for proper integration process increases at high frequencies. Actually the integration current doesn’t increase directly by the main signals frequency. However, to maintain the output signals shape, sampling frequency must be increased with the increasing frequency of the input signal.

It is a real challenge to design fast, accurate enough and low power consuming switched capacitor integrator. To overcome these limitations with a feasible power budget, the charge sharing switched capacitor integrator is designed and tested with simulations. Simulation results are consistent with the expected results. In this architecture, a charge sharing capacitance is added to the conventional architecture. This charge sharing capacitance is added for charge sharing with the main sampling capacitance to reduce the main sampling capacitances charge. In this way, current which is passing through the integration capacitance becomes very small compared to the conventional switched capacitor integrators integration current. To maintain the same output signal with less integration current, integration capacitance can be done smaller which will in turn result less power consumption. Another main advantage of reducing the integration capacitance is that it will take less time to settle the integrators output signal because of less charge storage on the small integration capacitance.

In addition to those advantageous, charge sharing switched capacitor integrator can be used at very large time constant integrator configurations with less power consumption and much less chip area than the conventional integrator architectures.

Charge sharing switched capacitor integrator advantages can be summarized as:

- Reduced effective sampling capacitance
- Reduced integration capacitance
- Less power consumption
- Reduced settling time
- Stray insensitive
- Less phase error
- Less chip area
- Less internal integration signal settling
- Very useful for very large time constant integrators

9.2. Future work

In this work generally, power consumption based approach is applied as prior design subject, however, clock feedthrough and charge injection errors must be examined carefully and it will be the next step after this work. Different architectures must be investigated for clock feedthrough and charge injection error minimizations. Another work must be done about conduction of the switches for high frequency applications. Switches must be large which will cause more error and maybe yet not enough conduction for proper charging and discharging. With new technological opportunities, MOS transistors which have very small channel lengths are available for designers. Decreasing the channel length will both affect positively at the perspective of clock feedthrough, charge injection error and small conduction resistance.

Another important future work issue will be the slew rate relation with opamp, switching part and output signals phase. It will be a good opportunity to know the slew rate limitation with the overall integrator performance, switching speed and opamp design specifications.

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