

**A HIGH LINEARITY S-BAND CRYOGENIC LOW NOISE AMPLIFIER
USING 180 nm CMOS TECHNOLOGY FOR SPACE APPLICATIONS**



M.Sc. THESIS

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Department of Electronics and Communications Engineering

Electronics Engineering Programme

14 JUNE 2019

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**UZAY UYGULAMALARI İÇİN 180 nm CMOS TEKNOLOJİSİYLE
GERÇEKLENMİŞ YÜKSEK DOĞRUSALLI KRIYOJENİK S-BANT DÜŞÜK
GÜRÜLTÜLÜ KUVVETLENDİRİCİ**

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To my parents,



FOREWORD

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ABBREVIATIONS

CMOS	: Complementary Metal Oxide Semiconductor
LNA	: Low Noise Amplifier
BiCMOS	: Bipolar Complementary Metal Oxide Semiconductor
HBT	: Heterojunction Bipolar Transistor
HEMT	: High Electron Mobility Transistor
MOSFET	: Metal Oxide Semiconductor Field Effect Transistor
OIP3	: Output Third-Order Intercept Point
IIP3	: Input Third-Order Intercept Point
ESA	: European Space Agency
TUBITAK	: The Scientific and Technological Research Council of Turkey
NF	: Noise Figure
TID	: Total Ionization Dose
SiGe	: Silicon Germanium
NMOS	: N-type metal-oxide-semiconductor
SiO₂	: Silicon Dioxide
SEE	: Single Event Effect
STI	: Shallow Trench Isolation
ELT	: Enclosed Layout Transistors
PCB	: Printed Circuit Board
CS	: Common Source
CG	: Common Gate
ESD	: Electrostatic Discharge
CDM	: Charge Device Model
NP0	: Negative-Positive 0 ppm/°C
LN2	: Liquid Nitrogen
DUT	: Device Under Test
ENR	: Excess Noise Ratio



SYMBOLS

V	: Voltage
C	: Capacitance
L	: Inductance
R	: Resistance
Hz	: Hertz
F	: Farad
H	: Henry
W	: Watt
K	: Kelvin
Rad	: Unit of Radiation Dose
dB	: Decibel
m	: Meter
g_m	: Transconductance
V_{TH}	: Threshold Voltage
f_T	: Cutoff Frequency
T_e	: Equivalent Noise Temperature



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A HIGH LINEARITY S-BAND CRYOGENIC LOW NOISE AMPLIFIER USING 180 nm CMOS TECHNOLOGY FOR SPACE APPLICATIONS

SUMMARY

Cryogenic circuit design has recently been a focus of research due to multiple fast-developing low-temperature applications. In space electronics, sensors and communication circuits should operate at temperatures below 100 K due to harsh ambient conditions. Furthermore, in order to increase the sensitivity, cryogenic cooling of the receiver front-end is commonly used in infrared sensors and bio-molecular detectors, with which the contribution of the thermal noise is reduced. Finally, circuits for quantum computing should be designed to work below 20 K so that they can interact with quantum bits that are held under 1 K to leverage maximum processing power within their coherence time.

Many cryogenic low noise amplifiers (LNAs) that have been designed using different device technologies exist in literature. However, the performance of CMOS LNAs at cryogenic temperatures has not been sufficiently reported. Cryogenic CMOS circuits have been recently of particular interest due to their improved analog, radio frequency, and digital design performance at short channel lengths and low cost of fabrication in comparison to competing device technologies such as heterojunction-bipolar-transistors (HBT), and silicon-on-insulator transistors (SOI). Typically, CMOS LNA gain tends to increase at low temperatures due to higher carrier mobility and the noise figure (NF) decreases mostly proportional to the decline in temperature. Nevertheless, a corresponding increase in the threshold voltage and the pronounced impact of layout mismatches complicate the design process. Among the relevant work to cryogenic LNAs in general, only one paper presents IIP3 performance at room and cryogenic temperatures with measurement results, where it is stated that IIP3 degrades as the temperature drops. Nevertheless, the LNA is driven by a three-stage amplifier. The total linearity depends on the gain performance of other stages; therefore, it is difficult to deduce the actual linearity performance of the LNA at cryogenic temperatures.

The novelty of this work resides in the linearity analysis and improvement of a cryogenic cascode LNA using the linearity theory for the first time. The classical LNA design methodology is based on simultaneous input and noise matching thereby optimizing the linearity by proper sizing of transistors. This methodology has been modified to accommodate cryogenic conditions thereby retaining IIP3 performance characteristics. An LNA design using this methodology is implemented in 180 nm CMOS technology and demonstrated at 77 K, which corresponds to the liquid nitrogen temperature. Temperature minimums across space can vary significantly ranging from 39 K near Pluto to 153 K near Mars. In this work, it is assumed that 77 K would cover most of the critical applications involving space electronics. Matching circuits of the LNA have been designed off-chip. As a result, precise impedance matching, which is required for reliable measurement results, has been experimentally achieved at

both cryogenic and room temperatures. Also, appropriate DC operating points, which satisfy almost the same current density at both 77 K and 297 K, have been chosen so that any impedance matching degradation and current density reduction as well as their impact on the linearity of the LNA at 77 K are mitigated. One of the key challenges in the design of circuits for space applications is the ionizing radiation damage. In that regard, the LNA here designed with standard RF CMOS transistors has been irradiated by gamma rays with a total dose of 650 krad. Post-irradiation measurement results show that the performance of the LNA is not susceptible to gamma radiation.



UZAY UYGULAMALARI İÇİN 180 nm CMOS TEKNOLOJİSİYLE GERÇEKLENMİŞ YÜKSEK DOĞRUSALLI KRIYOJENİK S-BANT DÜŞÜK GÜRÜLTÜLÜ KUVVETLENDİRİCİ

ÖZET

Son yıllarda artan uzay araştırmaları sebebiyle uzayın zorlu şartlarına dayanıklı elektronik devrelere olan ihtiyaç artmaktadır. Bu zorlu şartlar, başlıca uzayda mevcut olan yüksek radyasyon ve düşük sıcaklıklardır. Bu sebeple, uzay uygulamaları için elektronik devrelerin özellikle radyasyona karşı dayanıklılığı ve soğuktaki performansları incelenmektedir. Uzayda elektronik devreler yaklaşık olarak 100 krad toplam iyonlaştırıcı doza (total ionization dose, TID) maruz kalmaktadırlar ve Güneş'e en uzak olan gezegen Pluton'daki sıcaklık 39 K seviyelerine düşebilmektedir. Elektronik elemanların piyasada kriyojenik sıcaklıklar için mevcut modellerinin olmaması sebebiyle literatürde bu konuda önemli birçok çalışma bulunmaktadır. Buna rağmen, kriyojenik devrelerin büyük çoğunluğu halen standart devre modelleri kullanılarak tasarlanmaktadır.

Uzay uygulamalarına ek olarak, kuantum bilgisayarlardaki gelişmeler de kriyojenik devrelere olan ihtiyaç ve ilgiyi arttırmıştır. Günümüzdeki mevcut kuantum bilgisayarları mutlak sifıra yakın sıcaklıklarda çalışabilmektedir. Dolayısıyla, entegre bir yapı oluşturmak amacıyla kuantum bilgisayarlarda kullanılan elektronik devreler de kriyojenik sıcaklıklarda çalıştırılmaktadır.

Uzay uygulamaları için devre tasarımlarında radyasyona dayanıklı ve çok iyi RF özelliklerine sahip olmaları sebebiyle genelde yüksek elektron mobiliteli transistör (high electron mobility transistor, HEMT) ve heterojonksiyon bipolar transistör (heterojunction bipolar transistor, HBT) teknolojileri kullanılmıştır. Ancak bütünüleyici metal oksit yarıiletken (complementary metal oxide semiconductor, CMOS) teknolojilerinin son yıllarda boyutlarının hızla küçülmesiyle performansları da büyük ölçüde iyileşmiştir ve radyasyona olan dayanıklılıkları artmıştır. Ayrıca CMOS teknolojisinin diğer teknolojilere göre daha ucuz olması ve çok geniş ölçekli entegre devre tasarımına olanak vermesi nedeniyle uzay ve kriyojenik uygulamalarda CMOS devrelerin kullanımı yaygınlaşmaya başlamıştır.

Bu tez TÜBİTAK (Türkiye Bilimsel ve Teknolojik Araştırma Kurumu) 1001 "Uzay Araştırmaları için Analog ve Radyo Frekansı Metal-Oksit-Yarıiletken-Alan-Etkili-Transistör (MOSFET) Modellemesi ve Tümlleşik Devre Tasarımı" projesinin bir parçasıdır. Bu tezin temel amacı 180 nm UMC CMOS Mixed-Mode/RF teknolojisini kullanarak, uzay uygulamaları için S bandında (2 GHz) çalışacak bir düşük gürültülü kuvvetlendiricinin tasarlanması ve tasarlanan kuvvetlendiricinin kriyojenik ortamda ve radyasyona maruz kaldıktan sonra performansının ölçülmesidir. Uzay uygulamaları için ayrılan S bandındaki frekans aralığı (2.025 GHz - 2.12 GHz), kuvvetlendiricinin çalışma frekansı olarak belirlenmiştir. Kriyojenik sıcaklıkta ve radyasyona maruz kaldıktan sonra

kuvvetlendirici metriklerindeki deęişimleri kolayca analiz edebilmek için devre topolojisi olarak tek katlı kaskod yapısı seçilmiştir. Mevcut kriyojenik kompakt transistör modeli olmaması sebebiyle düşük gürültülü kuvvetlendirici standart transistör modelleriyle oda sıcaklığına göre tasarlanmıştır. Fakat daha önce yayınlanmış çalışmalardaki transistörün kriyojenik sıcaklıklardaki davranışları incelenerek kuvvetlendiricinin DC kutuplama noktaları bu çalışmalardaki verilerden faydalanarak seçilmiştir. Ayrıca literatürdeki kriyojenik düşük gürültülü kuvvetlendiricilerin düşük sıcaklıklardaki performansları incelenmiş olup kuvvetlendirici metriklerinin soğuktaki deęişimleri hakkında bilgi elde edilmiştir.

Birçok çalışmada gösterildięi gibi soğukta düşük gürültülü kuvvetlendiricilerin kazancı, yük taşıyıcısının mobilitesi arttığı için artmaktadır. Aynı zamanda, termal enerjinin düşmesiyle kuvvetlendiricilerin gürültü katsayısı da (noise figure, NF) önemli ölçüde azalmaktadır. Bunun yanında, kriyojenik sıcaklıklarda kuvvetlendiricilerin doğrulsallığıyla ilgili yeteri bilgi bulunmamaktadır. Şuana kadar sadece bir çalışma, kriyojenik düşük gürültülü kuvvetlendiricinin doğrusallığının hem kriyojenik hem de oda sıcaklığındaki ölçüm sonucunu sunmaktadır. Bu sonuçlara göre, soğukta kuvvetlendirici doğrusallığı azalmaktadır. Bu deęişim, esas olarak kazancın çok fazla artmasına dayandırılmıştır. Fakat şimdiye kadar doğrusallık ile ilgili herhangi bir analiz yapılmamıştır. Literatürdeki bu boşluk sebebiyle bu tez içerisinde bu konuya odaklanılmıştır. Bu tezde tek katlı bir kaskod kuvvetlendiricisinin doğrusallık analizi yapılmıştır. Oda sıcaklığına göre tasarımı yapılan düşük gürültülü kaskod kuvvetlendiricilerin, kriyojenik sıcaklıklarda kazancı artarken doğrusallık performansını korumasını sağlayacak bir tasarım yöntemi sunulmuştur.

TÜBİTAK projesi kapsamında kriyojenik ölçümler için sıcaklık olarak 77 K (Sıvı azot sıcaklığı) seçilmiştir. Kriyojenik sıcaklıkta gürültü katsayısı ölçümünde yüksek doğruluk için kriyojenik zayıflatıcı yöntemi kullanılmaktadır. Bu yöntemin kullanılabilmesi için test edilecek tasarımın bir devre kartı üzerine lehimlenmesi gerekmektedir. Bu, tasarlanan çipin paketlenmesi anlamına gelmektedir. Çipin paketlenmesi, aynı zamanda empedans uyumlama devresini ayrıık elemanlarla gerçekleştirme imkanı vermektedir. Bu sayede giriş ve çıkış empedans uyumu uygun ayrıık elemanlar seçilerek deneysel olarak hem oda sıcaklığında hem de 77 K’de sağlanmıştır. Bu yöntemle birlikte 77 K’de giriş ve çıkış yansıma kayıpları yüksek tutularak empedans uyumsuzluğunun doğrusallık ve kazanç gibi dięer metrikleri kötüleştirmesinin önüne geçilmiştir. Tasarımda, UMC 180 nm kütüphanesindeki RF transistörler kullanılmıştır. Bu transistörlerin serimleri en az parazit kapasite ve direnç içerecek şekilde düzenlenmiş olarak teknoloji kütüphanesinde hazır bir şekilde tasarımcıya sunulmuştur. Buna ek olarak, bu transistörlerin etrafında bir koruma halkası (Guard ring) bulunmaktadır. Önceki yapılan çalışmalar radyasyondan kaynaklanan bozulmaların koruma halkaları sayesinde önemli ölçüde azaltıldığını göstermiştir.

Tasarlanan kuvvetlendiricinin 300 K’deki kazancı, gürültü katsayısı ve üçüncü dereceden giriş kesişim noktası (third-order input intercept point, IIP3) sırasıyla 15.5 dB, 1.6 dB ve 2.1 dBm’dir. 77 K’deki ölçüm sonuçlarına göre kuvvetlendiricinin kazancı, gürültü katsayısı ve üçüncü dereceden giriş kesişim noktası sırasıyla 18 dB, 0.5 dB ve 3.4 dBm’dir. Hem 300 K’de hem de 77 K’de giriş ve çıkış yansıma kayıpları 10 dB’den fazladır ve güç tüketimi 15 mW’dır. Bu sonuçlara göre kuvvetlendiricinin bütün metrikleri 77 K’de iyileşmiştir. Kriyojenik gürültü katsayısı ölçümünün

detaylı doğruluk analizi yapılmıştır. Tasarlanan kuvvetlendirici 650 krad toplam iyonlaştırma dozu (total ionization dose, TID) ile gamma ışınım testine sokulmuştur. Işınım testinden sonra oda sıcaklığında yapılan testler sonucu kuvvetlendiricinin RF performanslarında herhangi bir değişim gözlemlenmemiştir ve koruma halkalarının 180 nm CMOS teknolojisi için 650 krad'a kadar yeterli korumayı sağladığı sonucuna varılmıştır.





1. INTRODUCTION

Circuit design for space applications was always challenging due to extreme conditions in space. The temperature on the surface of the Moon can change from approximately 43 K to 473 K during a lunar day and the mean temperature is 39 K on the farthest planet, Pluto, on our solar system [14]. In addition, being exposed to a lot of radiation in space also deteriorates the performance of electronic devices and shortens their lifetime. To prevent electronic devices from experiencing such extreme conditions, warm boxes and radiation shields has been preferred to use. However, this method causes systems to occupy more space and consume more energy. As an alternative approach, robust devices to high irradiation have been developing to eliminate the need for radiation shields. For instance, it has been proven that SiGe heterojunction bipolar transistor (HBT) and bipolar complementary metal oxide semiconductor (BiCMOS) processes maintain their performance under total ionization dose (TID) radiation. By the same token, circuit design with respect to very low temperatures has been a focus for decades to avoid using excessive energy and space. However, available devices in the market have been characterized mostly for commercial, industrial or military grade operating temperature, which means that their models are reliable between -55 °C and 125 °C temperature in the best case; yet, electronic devices in space should be able to work properly below 100 K. Thus, the lack of compact device models for cryogenic temperatures, which is the definition of temperature values below -180 °C, is the biggest challenge for cryogenic circuit design. For this reason, modeling of electronic devices is an important step of researches on cryogenic circuit design.

In addition, interest in cryogenic circuit design has been rising in the last decade due to emerging quantum computing technologies. It has been shown that a spin in silicon can hold a bit of quantum information [15]. This demonstration makes CMOS technology attractive to be utilized for designing front-end circuits to read and control states of spin quantum bits. Since quantum bits are held under 1 K temperature to keep the thermal

noise at the minimum level, electronic control circuits are also required to operate at temperatures near to absolute zero, which is usually around 4 K [10].

Communication circuits are prevalently used in both space and quantum computing applications. Since low noise amplifiers (LNAs) are the second stage of the receivers, cryogenic LNAs are a significant part of the research on cryogenic circuit design in the literature. LNAs are supposed to amplify the received signal by adding very low noise power to the signal to satisfy high signal-to-noise ratio. In the high-frequency range, significant noise contribution comes from the thermal noise. That's why LNAs are preferred to cool down to minimize the thermal noise in applications, which require high sensitivity. Because of being tolerant to radiation, high electron mobility transistor (HEMT) and HBT technologies have been mostly employed in LNA design for space conditions [6, 7, 9, 28–40]. However, CMOS LNAs have been rarely investigated, and CMOS transistors with scaling of the technology become comparable other superior technologies. Furthermore, CMOS technologies are much cheaper. These assets make CMOS technologies very promising for cryogenic circuit design.

1.1 Purpose of Thesis

In this thesis, an LNA implemented in UMC 0.18 μm CMOS Mixed-Mode/RF technology is presented and it is specifically targeted for space applications. Because of having no available cryogenic transistor model in the market, the LNA has been designed with standard device models with respect to room temperature. However, if it is considered that the temperature in space can swiftly vary in large range and electronic circuits will exposure to high radiation in space conditions, the LNA should exhibit good performance at both cryogenic and room temperatures, and its performance should sustain after TID radiation. To achieve this, the characteristic of employed devices in extreme environments have been investigated by utilizing from previously published works in the literature.

The operation frequency of LNA has been chosen according to frequency bands of space communications reported in Deep Space Network of California Institute of Technology document [16]. LNAs are employed at the receiver part of communication circuits; therefore, only uplink frequency bands in the document have been considered.

At S-Band, deep space and near earth bands for uplink are 2110 - 2120 MHz and 2025 - 2110 MHz, respectively. The frequency bandwidth has been selected as 2025 - 2120 MHz to cover all allocated frequencies for space communications at S-band.

Since lower bound of temperature across space can change significantly ranging from 39 K near Pluto to 133 K near Mars, it is assumed that 77 K would include most of the critical applications within space electronics [14]. Hence, the performance of the LNA for low temperatures has been demonstrated at 77 K. Moreover, the radiation test has been done by applying 650 krad TID radiation, which is also a sufficient level for most cases, to the LNA at room temperature.

This thesis is a part of The Scientific and Technological Research Council of Turkey (TUBITAK) project “Analog and Radio Frequency Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Modeling and Integrated Circuit Design for Space Research”. The primary aim of this project is to extract transistor models of 0.18 μm CMOS technology at cryogenic temperatures and under radiation and to design RF circuits operating in such extreme environments. Specifications of the LNA have been designated according to objective metrics in the project proposal. In this regard, a minimum of 15 dB voltage gain and a maximum of 1 dB noise figure (NF) have been targeted to be at 80 K. Input and output return losses have been aimed to be higher than 10 dB within the operating frequency band. Output third-order intercept point (OIP3) higher than -10 dBm has been desired while the LNA consumes maximum 40 mW power.

Within this project, a test chip comprises different types of transistors with various sizes has been firstly designed to extract cryogenic transistor model. Before using this model for circuit design, this LNA has been designed to gain insight with experimental data acquired in space conditions. Afterward, a cryogenic LNA with utilizing both cryogenic device models and experimental data will be designed to assess the success of the cryogenic model.

1.2 Literature Review

The characteristic of transistors in various technology at very cold temperatures has been studied well in the past years and mainly DC properties of transistors have been

characterized and presented. Furthermore, numerous publications for other electronic devices in this subject exist in the literature. Besides, there are several cryogenic LNAs implemented in HBT and HEMT technologies, and only one available work about cryogenic CMOS LNA has been recently published. Regarding the experimental data in these publications, it is deduced that gain and NF of LNAs improve and impedance matching can degrade at very low temperatures. However, measurement results for the linearity performance of LNAs at both cryogenic and room temperatures are very limited. Even though the resilience of some RF circuits to radiation has been presented using some layout techniques, radiation robustness of CMOS LNAs has not been investigated enough, which indicates that this field is open to further researches.

1.3 Hypothesis

Performance of CMOS transistors has been shown to increase at cryogenic temperatures. Therefore, LNAs exhibit better performance in terms of gain and NF. On the other hand, one paper shows that the linearity of the presented LNA degrades at very low-temperature. In another paper, it is claimed that linearity degradation occurs due to current reduction; however, it is not supported by any measurement results. In this thesis, it is proven for the first time with experimental data that linearity performance of an LNA can be preserved and improved by keeping the current constant at cryogenic temperatures. Besides, input and output return losses have been adjusted to be high enough at both 77 K and 300 K so that mismatch losses do not significantly affect other metrics of the designed LNA. Consequently, this study presents an LNA satisfy good performance at both cryogenic and room temperatures.

CMOS transistors whose oxide thickness is lower than 10 nm are asserted to be radiation tolerant. Since submicron CMOS technologies are in this category, 0.18 μm CMOS devices are promising for space applications. Moreover, it is demonstrated with measurement results that 0.5 μm CMOS transistor with the guard ring layout technique can be robust to TID radiation up to 600 krad - 1.7 Mrad depending on the type of radiation source. Therefore, the LNA in this study has been designed by adopting the guard ring technique, and it is presented that the designed LNA does not show any performance degradation up to a TID of 650 krad.

1.4 Thesis Organization

The first chapter introduces the challenges of circuit design for space applications, the novelty of this study, and its contributions to the literature. In the second chapter, electronic devices at cryogenic temperatures are examined and the performance of cryogenic LNAs in the literature is discussed. Also, their tolerance against TID radiation is investigated. The third chapter starts with the noise, gain, linearity and matching theories. Subsequently, the design of 2 GHz LNA is explained. In the fourth chapter, the measurement results of the LNA are provided. Finally, the conclusion of the thesis is presented and the novelty of this study is discussed.





2. LOW NOISE AMPLIFIERS IN EXTREME CONDITIONS

Extreme conditions for space environment are very low and high-temperature values and exposure to high radiation dose. In most of the space applications, electron devices usually operate at a very cold environment rather than extreme high temperatures; thus, in this study researches on cryogenic conditions have been investigated as well as radiation robustness of electronic devices.

2.1 Devices and LNAs at Cryogenic Temperatures

Characteristic of electronic devices at cryogenic temperatures have been studying for a long time. Thus, cryogenic features of the devices are well-known, and various cryogenic LNAs exist in the literature. To analyze behaviors of complex circuits correctly at cryogenic temperatures, it is crucial to comprehend the characteristics of individual elements. In this section, previous works on cryogenic electronic devices, particularly transistors are revised. Afterward, previously published cryogenic LNAs are examined.

2.1.1 Devices at cryogenic temperatures

Research on the characterization of transistors at cryogenic temperatures dates back to 1980s. In those years, CMOS devices were more prevalent. With the dazzling advance in other technologies like SiGe HBT and HEMT, they have become more popular especially for high-speed applications. The studies about SiGe HBTs have been compiled by Cressler [1]. The improvement pace in the current gain of Si-based bipolar technologies has accelerated by Ge implantation in silicon as denoted with the last two SiGe measurement results in Fig. 2.1, and this enhancement is more prominent at low temperatures. Moreover, it has been also reported that cooling the device increases the cut-off frequency of the SiGe HBTs as given in Fig. 2.2. These results are also supported by other studies.

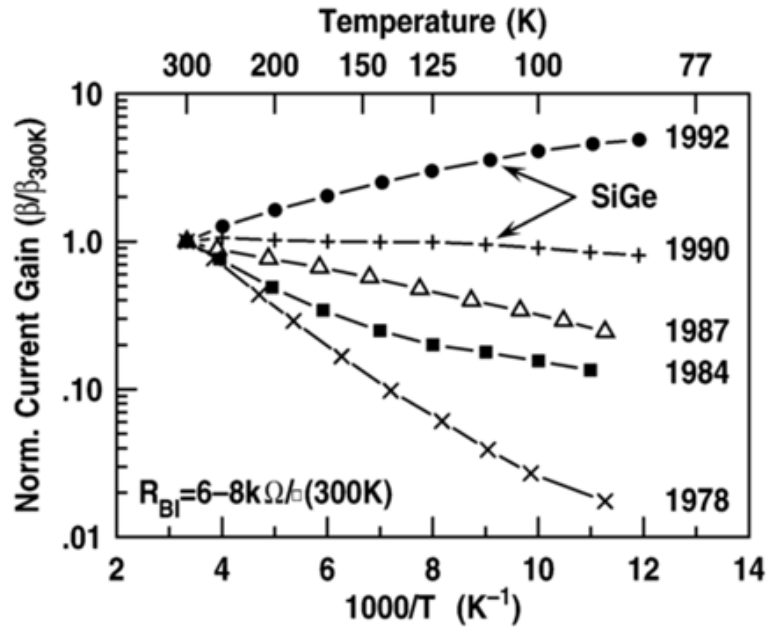


Figure 2.1 : Advance in the current gain of Si-based bipolar devices versus temperature over the years [1].

In addition to SiGe HBT technologies, HEMT technologies have been extensively studied for cryogenic applications. For instance, a $Ga_{0.51}In_{0.49}P/GaAs$ HEMT device which exhibits good performance at cryogenic temperatures has been introduced in 1990 [2]. As illustrated in Fig. 2.3, the transconductance of the HEMT device with $1 \mu m \times 150 \mu m$ sizes rises from 163 mS/mm to 213 mS/mm when the temperature lowers to 77 K, and it leads drain-source current to increase. Although these results belong to a long channel device, recent technologies also have a similar behavior at very low temperatures.

Because of the superior characteristics of HEMTs and SiGe HBTs, the majority of the cryogenic circuits in the literature has been designed by SiGe HBT and HEMT technologies. However, these technologies are expensive compared to CMOS technologies and HEMTs are non-integrated devices. With the scaling of CMOS technologies, CMOS devices exhibit excellent performance; therefore, CMOS technologies are very promising for low-temperature applications and there are numerous works on modeling and characterization of MOSFET devices at cryogenic temperatures [4, 5, 10, 17–25]. These studies mostly focused on DC characterizations; hence, variations in drain current, threshold voltage, transconductance, carrier mobilities, and substrate current are well-known at cryogenic temperatures. However,

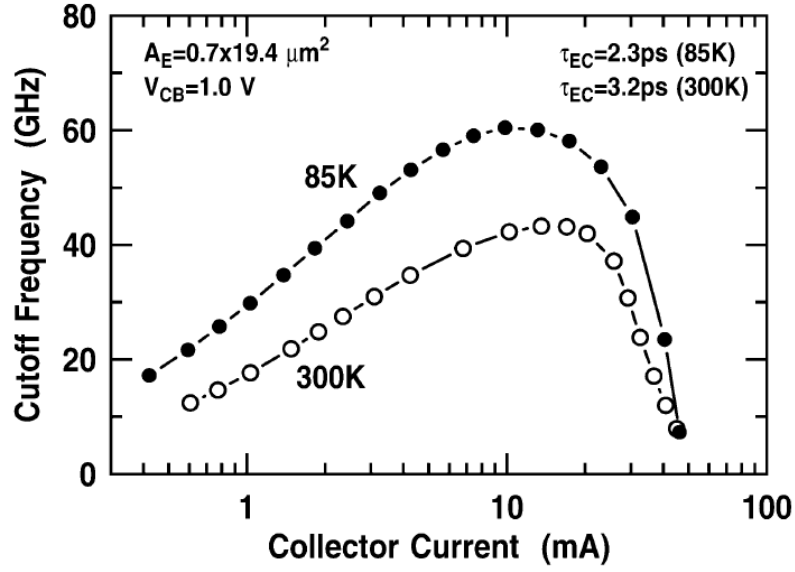


Figure 2.2 : Cutoff frequency versus collector current of an optimized SiGe HBT for 77 K at both 85 K and 300 K [1].

the RF properties of cryogenic devices have not been adequately examined [4, 5]. To enable RF circuit design at very low temperatures, more research should be conducted.

As the first step of the TUBITAK project of modeling and RFIC design for space applications, DC properties of RF transistors in UMC 180 nm CMOS technology have been measured [3]. Measurement results belong to an RF transistor with 35 μm width and 0.18 μm length are given in Figs. 2.5 and 2.4. As given in Fig. 2.6, threshold voltage (V_{TH}) considerably increases at 77 K. The intrinsic doping concentration of silicon is exponentially dependent on the temperature. Thus, the required gate voltage to form the same charge concentration in the channel at 77 K is more compared to room temperature. Furthermore, lowering the temperature leads to a larger surface potential, and in lower thermal energy channel dopants slowly ionize. Consequently, these effects lead to rising in V_{TH} . Despite the increase in V_{TH} , as shown in Fig. 2.5 the current of the CMOS transistor rises, as well. As temperature decreases, phonon scattering also reduces, which causes the carrier mobility to improve. That is why the rise in the current at 77 K is mainly due to the increase at the carrier mobility. Mobility improvement also increases the transconductance of the CMOS devices.

In addition, the increase in the transconductance results in higher cutoff frequency (f_T) due to that f_T is directly proportional to the transconductance as seen in Eq. 2.1 where C_{gg} is the gate capacitance.

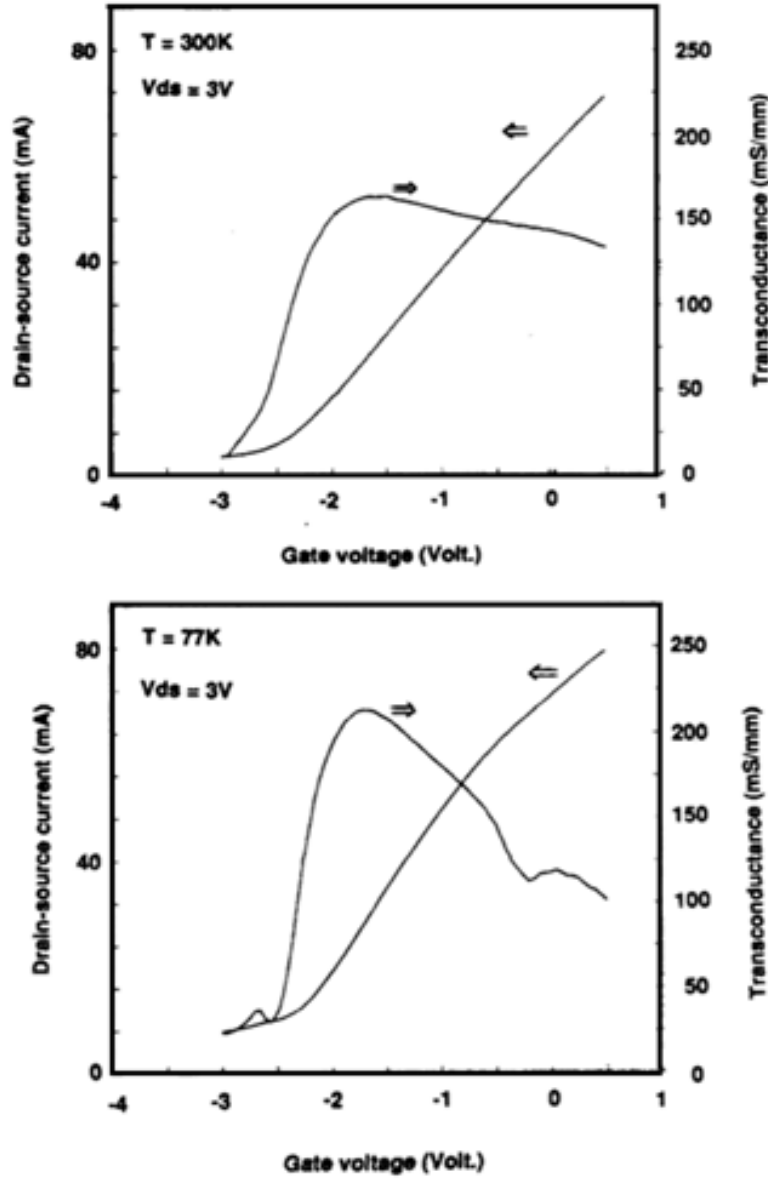


Figure 2.3 : Normalized transconductance and drain-source current versus gate voltage of HEMT at both 77 K and 300 K [2].

$$f_T = \frac{g_m}{2\pi C_{gg}}. \quad (2.1)$$

One study demonstrates the relationship between the cutoff frequency and transconductance [4]. As shown in Fig. 2.6, the cutoff frequency of N-type MOS (NMOS) with SiO_2 dielectric material in 100 nm CMOS technology linearly rises until 100 K. However, after 100 K, it starts to decrease, and it is attributed to carrier freeze-out at low temperatures. The carrier freeze-out, which has been also extensively studied, is another important issue at cryogenic temperatures, and it occurs because of low thermal energy, which causes carriers to lose their energy easily [24–27]. To

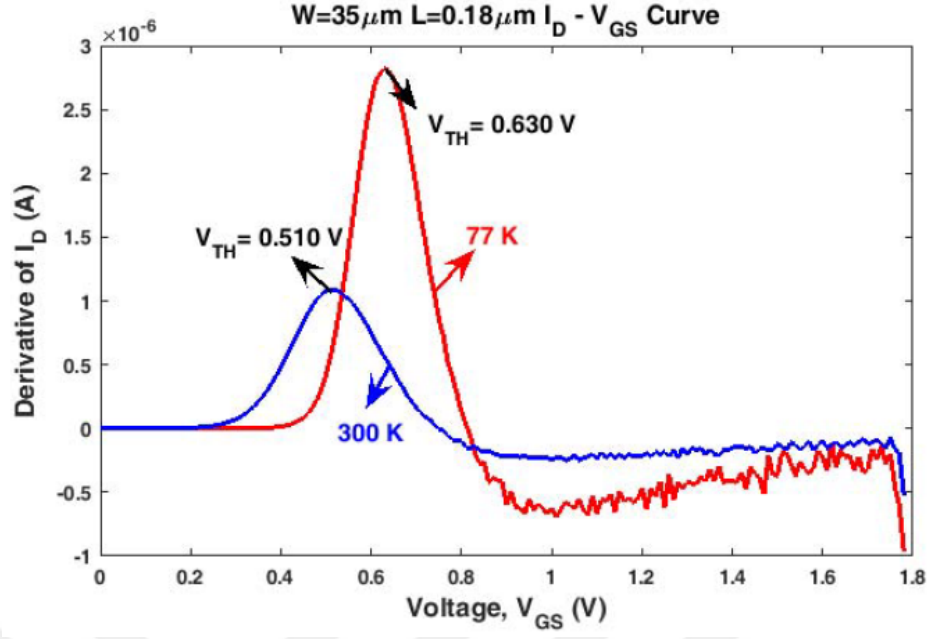


Figure 2.4 : Second-derivative method of V_{TH} extraction of an RF transistor at both 77 K and 300 K [3].

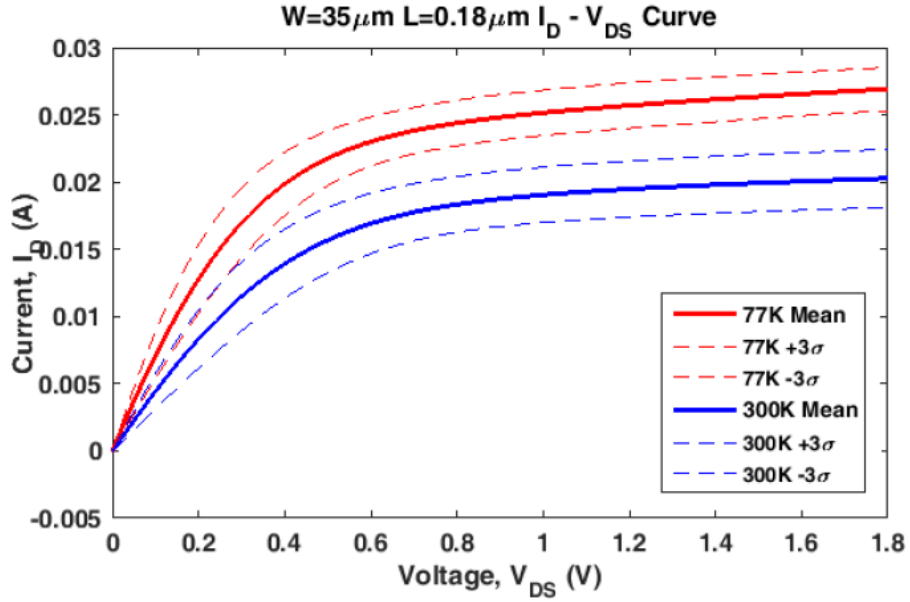


Figure 2.5 : Drain current of an RF transistor with process variations at both 300 K and 77 K [3].

mitigate this issue, high-k dielectric materials are used as a gate dielectric in some applications. For instance, unlike to SiO_2 , HfO_2 dielectric material achieves to alleviate freeze-out effect as indicated in Fig. 2.6.

The interior capacitance values of the transistor at cryogenic temperatures is also an important subject since the dielectric of the materials changes with temperature. In Fig.

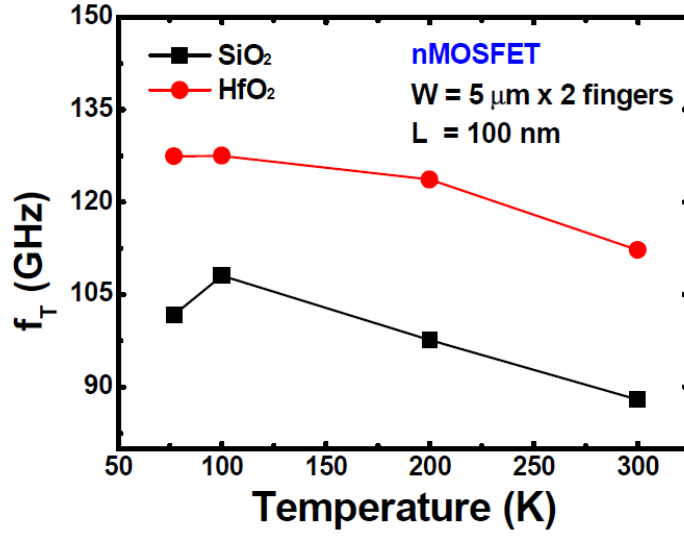


Figure 2.6 : Cutoff frequency versus temperature for NMOS with both SiO_2 and HfO_2 gate dielectrics [4].

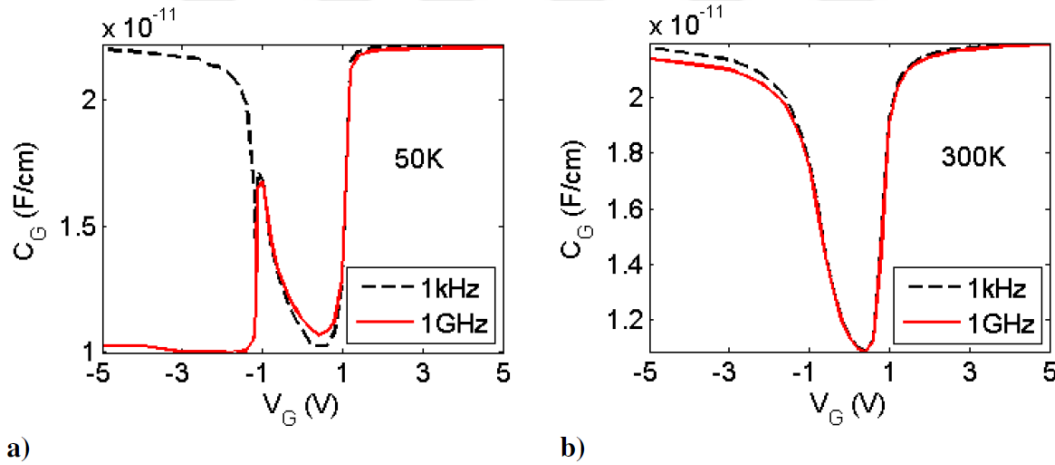


Figure 2.7 : Total gate capacitance at a) 50 K and b) 300 K [5].

2.7, for two different frequencies, total capacitance at the gate for both 50 K and 300 K is compared with each other. In the inversion region, the gate capacitance slightly increases at 50 K for both 1 kHz and 1 GHz. However, there are less free carriers due to lack of thermal energy in the bulk at 50 K, and it causes the bulk to respond slowly; therefore, there is a huge difference in capacitance values at between 50 K and 300 K for high frequencies in the accumulation mode of operation.

2.1.2 LNAs at cryogenic temperatures

SiGe HBT and HEMT are widely used technologies for cryogenic LNAs in literature. For this reason, LNAs based on SiGe HBTs and HEMTs are mainly examined

in this section. Only one CMOS LNA has been presented by now; however, as discussed in the previous section, different technologies exhibit similar behavior at low temperatures. Hence, investigating cryogenic SiGe HBT and HEMT LNAs will provide considerable design insight.

2.1.2.1 SiGe HBT-based LNAs

The presented cryogenic SiGe HBT LNAs are usually wideband, and their frequency of operation goes up to 12 GHz [6, 7, 28–33]. Moreover, measurements of SiGe HBT LNAs exist at different ambient temperatures like 293 K, 200 K, 80 K, 40 K, 15 K. Even though impedance matching of a cascode LNA presented in [6] deteriorates at 15 K, the gain increases 5 dB in all band. This improvement occurs thanks to the rise in carrier mobility.

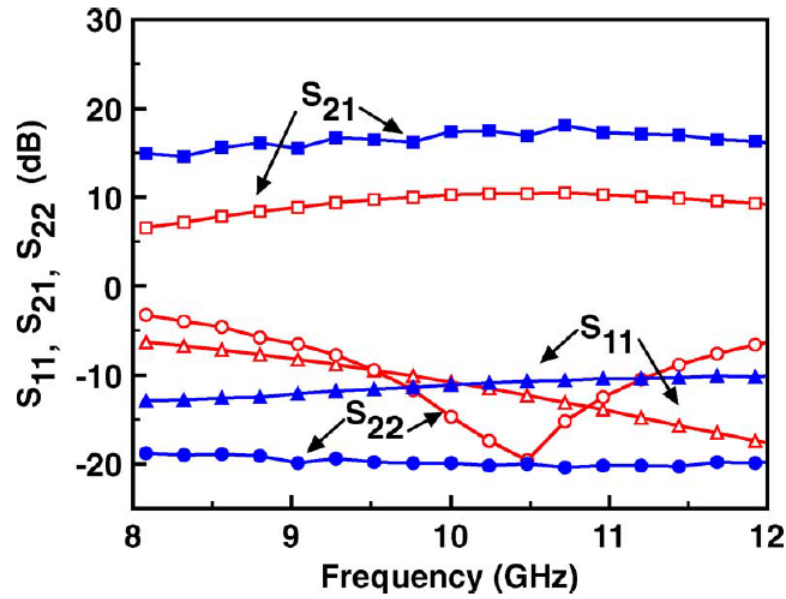


Figure 2.8 : An S-parameters comparison of a cascode SiGe HBT LNA at 15 K and 300K, which are represented by closed and open symbols, respectively [6].

The noise of LNAs is another metric gives better results at cryogenic temperature. It is usually expressed by equivalent noise temperature (T_e) for cryogenic LNAs instead of noise figure. However, the conversion between noise figure and equivalent noise temperature can be done using Eq. 2.2. Unit of T_e and T_{ref} are Kelvin, and T_{ref} is usually taken as 290 K.

$$NF(dB) = 10 \times \log_{10}\left(\frac{T_e}{T_{ref}} + 1\right) \quad (2.2)$$

In Fig. 2.9, noise measurement of a SiGe HBT transistor is given, and it appears that noise of an individual transistor is nearly commensurate with the temperature between 40 K and 293 K and amounts of measured noise at 15 K and 40 K are almost identical. However, measured noise values at 15 K and 40 K are close to measurement accuracy. For this reason, measurements performed at 40 K and below are not reliable. Consequently, Fig. 2.9 shows that thermal noise is a dominant noise source of a SiGe HBT transistor. By the same token, it is shown in Fig. 2.10 that it is possible to achieve the noise temperature as low as 2 K at cryogenic temperatures.

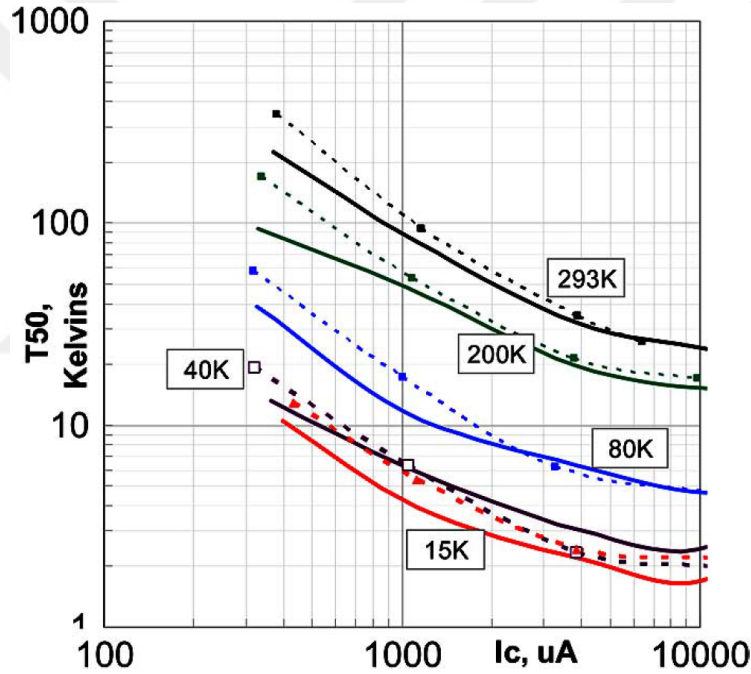


Figure 2.9 : Measured (dashed line) equivalent noise temperature versus collector current for 180- μm IBM 8-HP SiGe HBT at different ambient temperatures when the impedance of noise generator is 50 ohm. The given values are the mean of noise temperatures between 0.2 GHz and 1.2 GHz [7].

2.1.2.2 HEMT-based LNAs

Variations on the performance of LNAs designed by HEMT devices at cryogenic temperatures are similar to SiGe HBT LNAs as demonstrated in [9, 34–40]. In Figs. 2.11 and 2.12, gain and noise temperature of a HEMT-based LNA at 15 K and 300 K are compared. As expected, the noise temperature considerably decreases at 15 K, and

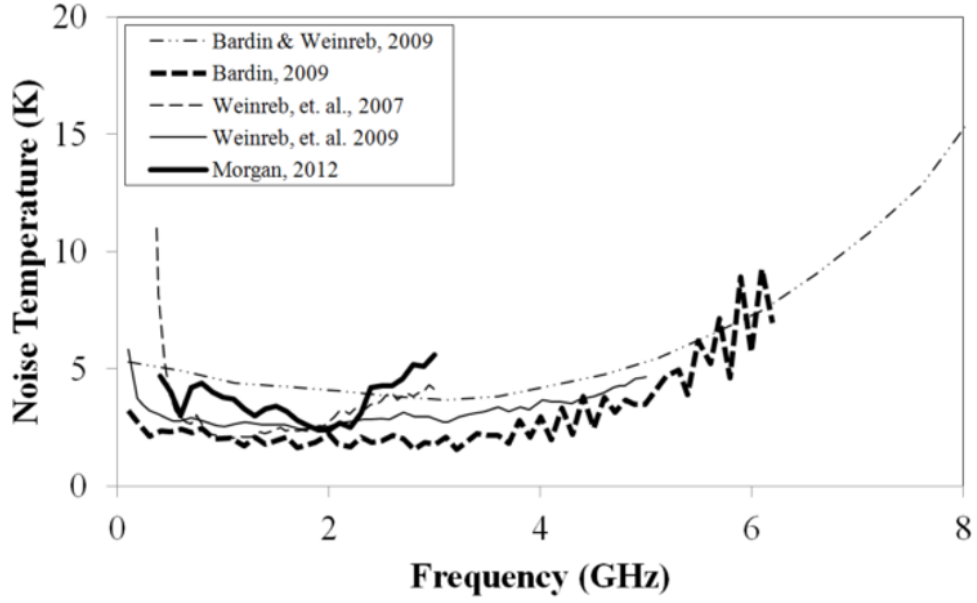


Figure 2.10 : Cryogenic SiGe amplifiers give the best equivalent noise temperatures presented in recent years [8].

gain slightly increases. As distinct from SiGe HBT LNAs, HEMT LNAs in literature usually operate at higher frequencies, which proves that LNA metrics can be improved by cooling LNAs at very high frequencies, as well.

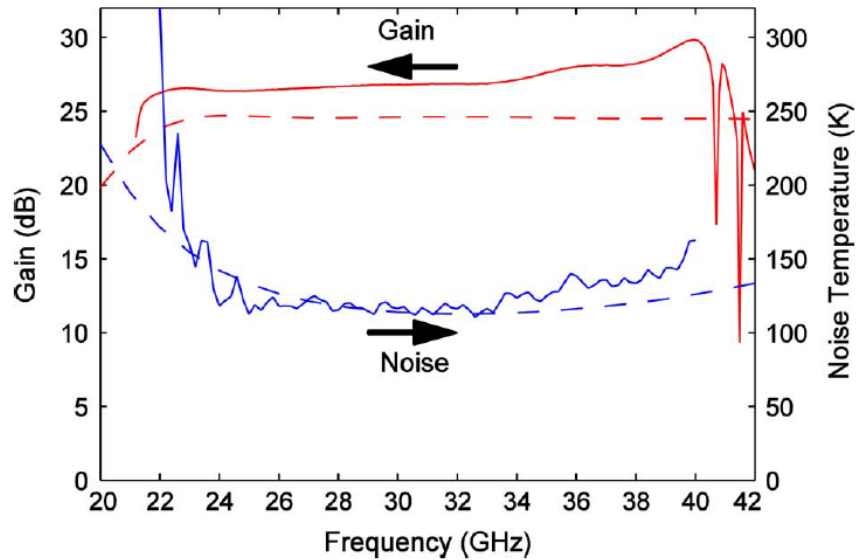


Figure 2.11 : Measured (solid line) gain and noise temperature of a HEMT-based LNA at 300 K [9].

2.1.2.3 CMOS-based LNAs

In the literature, just one cryogenic CMOS LNA exists [10]. It is specifically aimed for quantum computing applications. Today's quantum computing processes are

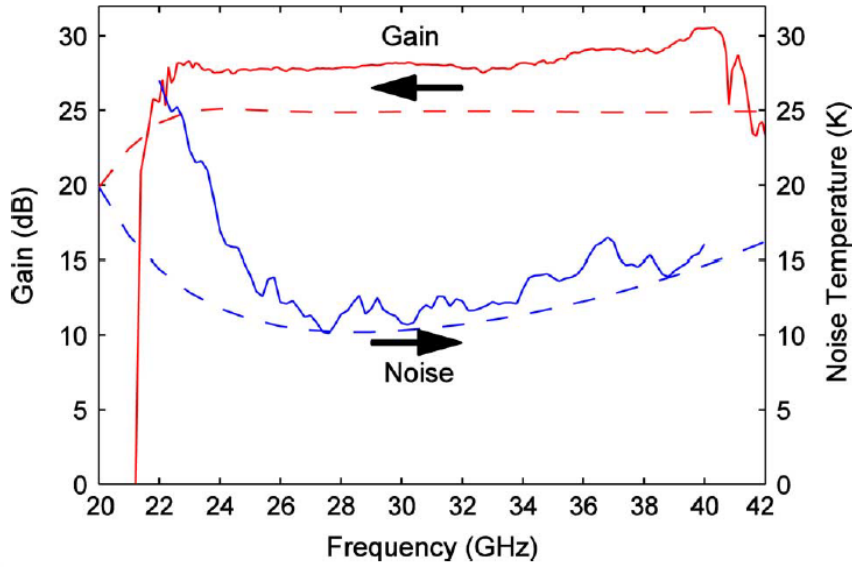


Figure 2.12 : Measured (solid line) gain and noise temperature of a HEMT-based LNA at 15 K [9].

performed at near 0 K. Control and read-out circuit are proposed to operate at 4 K to achieve an integrated structure for quantum computing. Therefore, the performance of the LNA is presented at 4 K. As given in Fig. 2.13, NF significantly improves in high frequency as in HEMT and SiGe HBT LNAs. Since the flicker noise is the dominant noise source in low frequency, NF slightly decreases despite the significant decrease in the temperature. It is stated that the peaks occur due to external electromagnetic interference. Similar to other cryogenic LNAs, the gain of the CMOS LNA increases at cryogenic temperatures as shown in Fig. 2.14.

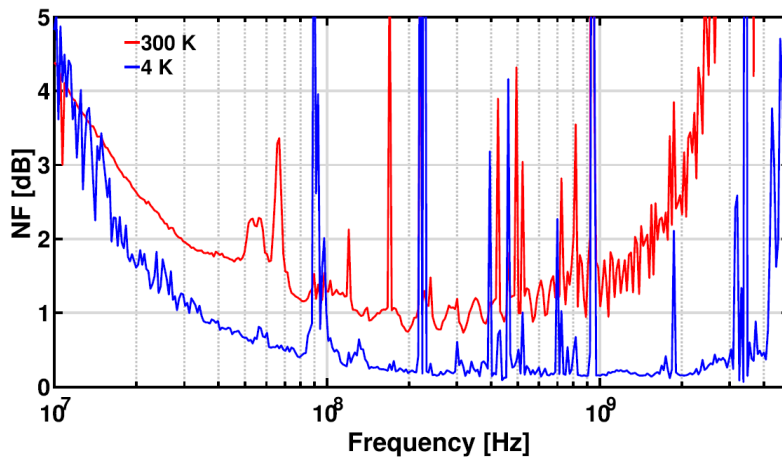


Figure 2.13 : Measured noise figure of the cryogenic CMOS LNA at both 4 K and 300 K [10].

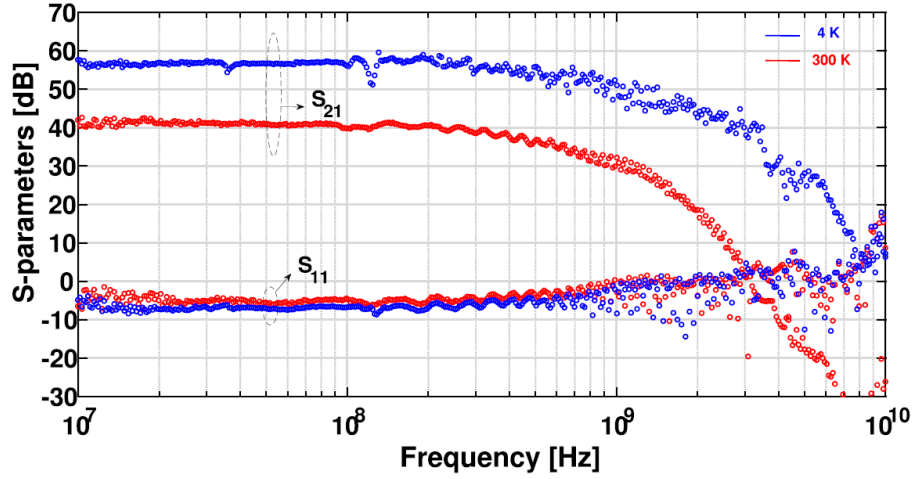


Figure 2.14 : Measured S-parameters of the cryogenic CMOS LNA at 4 K and at 300 K [10].

In [10], the linearity performance of a cryogenic LNA has been presented for the first time. As indicated in Fig. 2.15, the input third-order intercept point (IIP3) degrades 10 dB at 4 K compared with the room temperature and it is attributed in the paper to the rise in the gain and the reduction in the overdrive voltage, which is caused by the increase of the threshold voltage. However, this study does not provide any detailed analysis of linearity. The LNA has a complex structure and it includes noise cancellation circuit and additional 3-stage amplifier. For these reasons, it is difficult to evaluate the linearity variation of the LNA itself at 4 K; yet, this study points to important factors like gain and threshold voltage, which must be taken into account while the linearity performance at cryogenic temperatures is examined.

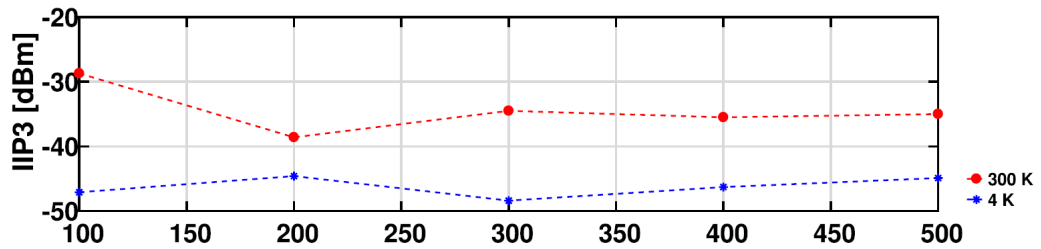


Figure 2.15 : Measured IIP3 of the cryogenic CMOS LNA at 4 K and at 300 K [10].

2.2 CMOS Devices and LNAs under Radiation

Electronic devices for space applications should work properly under high radiation dose. Electronic devices robustness to radiation are usually investigated by single event effect (SEE) and total ionization dose tests. Previous studies show that TID

permanently influences the performance of analog and digital circuits, while SEE is mainly a concern for digital applications. Therefore, TID is the main focus of this study. During exposure to radiation, ionization happens only when photons have enough energy to release an electron from the atom and it damages bonds in molecules thereby creating dangling bonds, which are usually expressed as charge traps. In this section, the effects of these flaws on CMOS devices and LNA circuits has been examined.

2.2.1 CMOS devices under radiation

Under radiation, insulating layers of CMOS devices degrade due to formed charge traps [41]. Those traps constitute in the gate oxide of the transistors in former CMOS technologies [42]. Charges trapped in the oxide of NMOS and PMOS transistor cause negative and positive shift in the absolute of the threshold voltage, respectively [43]. Moreover, charge traps induce mobility degradation in the channel, and these traps cause low-frequency operation noise of transistors to increase due to their slow behavior of capturing and releasing electrons [44, 45]. While these effects are more prominent in the long devices, the scaled devices are more resilient to ionizing radiation thanks to having thinner gate oxide [46–48]. However, shallow trench isolation (STI) is used to isolate adjacent semiconductor devices in the scaled technologies and their thicknesses are more than 100 nm, which makes them be very susceptible to radiation. The charge trapping in the trench oxides also causes V_{th} shift; furthermore, it inverts the channel of the parasitic transistor in NMOS transistors thereby leading leakage current [11, 41, 49, 50]. Therefore, charge traps at the edge of transistors are the main reason for performance deterioration in narrow channel transistors.

Impacts of charge trapping in the trench oxide of a 130 nm commercial CMOS technology are studied in detail in [11]. As given in Fig. 2.16, the V_{th} of devices without any radiation hardness techniques is getting less during TID radiation and after annealing, transistors with large width substantially recover the V_{th} shift. However, the V_{th} of enclosed layout transistors (ELTs), which is also known as annular gate transistors, fluctuates much less compared to other transistors and it totally heals at the end of the annealing. Moreover, while the leakage current of standard transistors

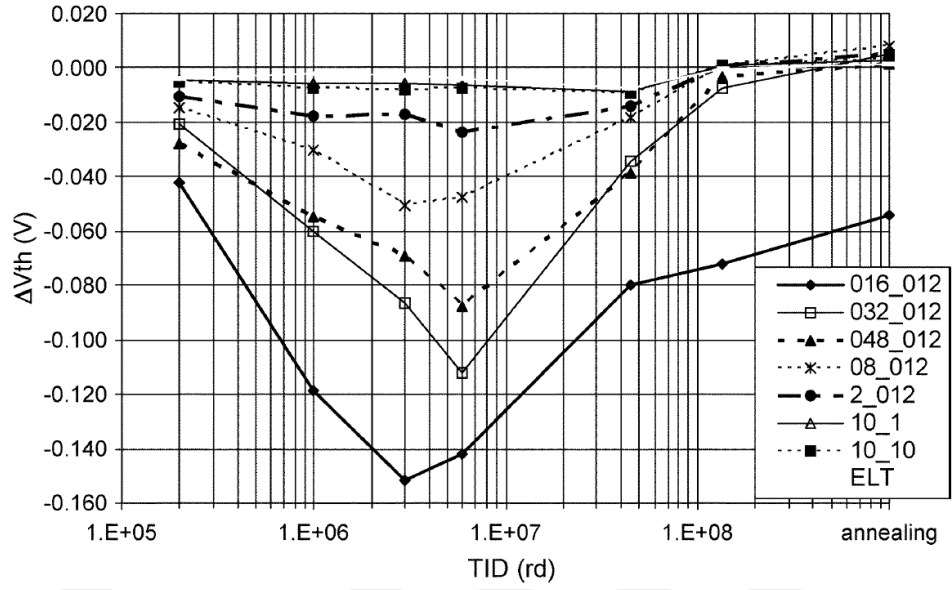


Figure 2.16 : V_{th} change from pre-rad to end of the annealing with TID up to 136 Mrd for different NMOS transistor size [11].

increases under TID radiation, the leakage current of ELTs remains the same between pre-rad and annealing as indicated in Fig. 2.18. In addition to ELTs, the guard ring structure is employed as another protection technique in the layout against radiation effects, and they provide enough protection to minimize variations on leakage current and the threshold voltage [51]. Guard ring structure brings less parasitic capacitance compared to ELTs; thus, the guard ring technique is more appropriate to be employed in RF circuits.

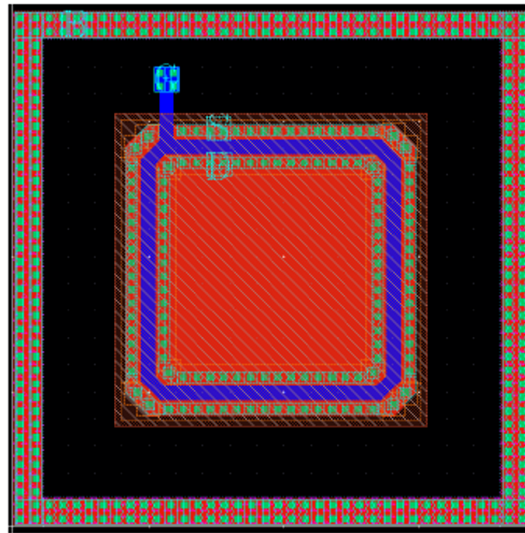


Figure 2.17 : The layout of an Enclosed layout transistor [12].

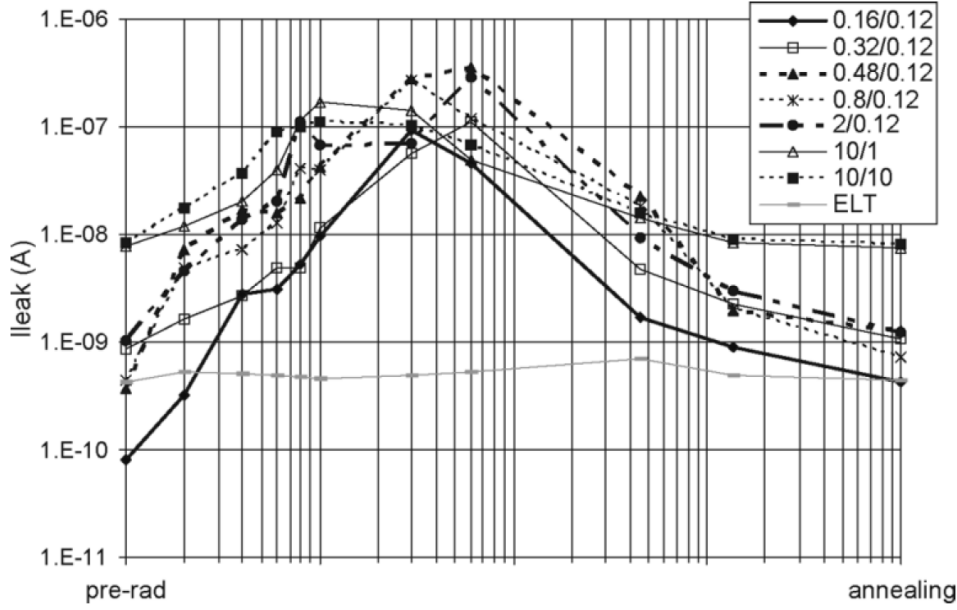


Figure 2.18 : The leakage current from pre-rad to end of the annealing for different NMOS transistor size. TID goes up to 136 Mrd during the radiation test [11].

2.2.2 CMOS LNAs under radiation

Robustness of LNAs under radiation has been rarely reported [13, 52]. After-radiation measurement results of an LNA implemented in 130 nm CMOS technology are presented in [13]. Annular gate transistors are used in the LNA design for radiation protection and the LNA has been tested after 500 krad TID radiation has been applied to the LNA using a Co-60 gamma-ray source. As shown in Figs. 2.19 and 2.19, NF

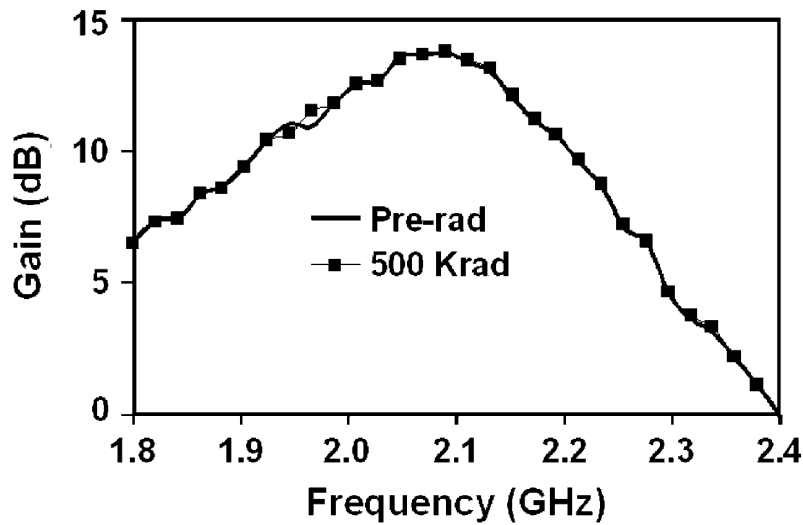


Figure 2.19 : Measured gain of the LNA circuit with annular gate transistors before and after irradiation [13].

and gain of the LNA are not degraded by TID radiation thanks to the annular gate transistors (or ELTs). Therefore, these results show that annular gate transistors are resilient against the TID radiation.

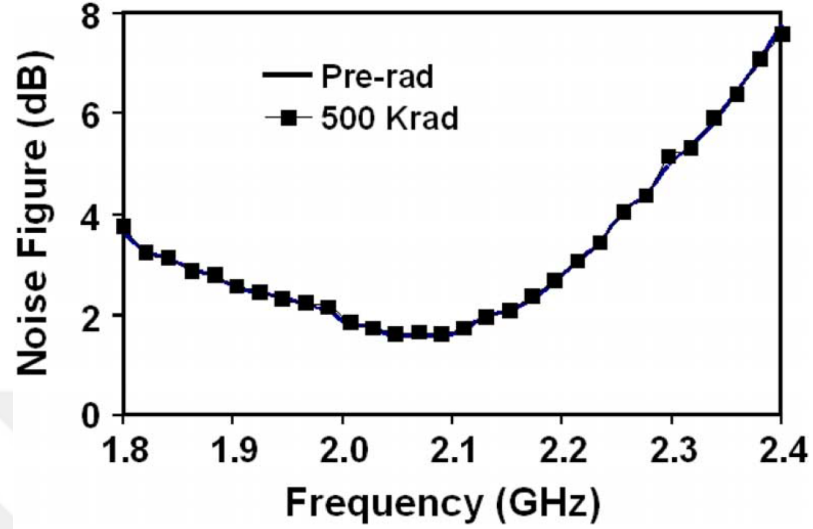


Figure 2.20 : Measured NF of the LNA circuit with annular gate transistors before and after irradiation [13].

In the literature, there is no LNA circuit with the guard ring structure tested under a TID radiation. In this study, guard rings are preferred as a radiation protection structure instead of annular gate transistors, since guard rings around NMOS devices do not create any additional parasitic capacitance affects transistors' RF characteristic. Moreover, transistors with a guard ring occupy less space.



3. LOW NOISE AMPLIFIER DESIGN

LNA circuit topology has been chosen according to specification goals in the TUBITAK project “Analog and Radio Frequency Metal Oxide Semiconductor Field Effect Transistor Modeling and Integrated Circuit Design for Space Research” and another aim is to analyze variations on the LNA performance at cryogenic temperature. By the same token, LNA design has been performed such that the LNA performance will be preserved in terms of all metrics of the LNA at 77 K. A simple circuit topology has been preferred to ease the analysis and to observe explicitly relations between LNA metrics and temperature-dependent parameters. For this purpose, the cascode structure has been selected for the LNA design.

3.1 Theory of a Cascode LNA Design

In this section, the gain, noise figure, and linearity theories of source degenerated cascode LNA are examined. The theory of a cascode LNA is a very well-known and well-studied topic; therefore, analyses of the LNA metrics in previous studies are presented here.

3.1.1 Noise and gain of a cascode LNA

The voltage gain of the conventional cascode LNA in Fig. 3.1 is extracted in [53]. The voltage gain expression is given in Eq. 3.1, where R_1 and C_{CG1} are the series resistance on L_1 and the internal capacitance between source and gate of the M_1 transistor, respectively, and $\omega_T = g_{m1}/C_{GS1}$. Eq. 3.1 is found by assuming that the input impedance of the LNA is matched to the output impedance of the input source ($R_S = (g_{m1}L_1)/C_{GS1}$). As clearly seen in Eq. 3.1, the gain mainly depends on values of R_1 and L_1 .

$$\frac{V_{OUT}}{V_{IN}} \cong \frac{R_1}{2L_1\omega_0} = \frac{\omega_T R_1}{2\omega_0 R_S}, \quad (3.1)$$

where

$$\omega_0 = \sqrt{\frac{1}{(L_1 + L_G)C_{GS1}}}, \quad (3.2)$$

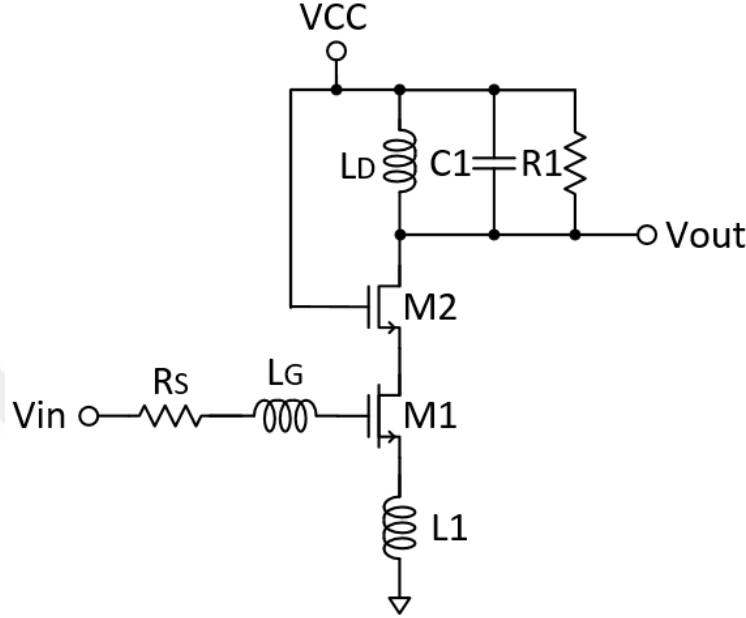


Figure 3.1 : A cascode RF LNA with inductive degeneration.

The noise figure of a source generated LNA is given in Eq. 3.3, where γ is the coefficient of channel thermal noise [54]. α is one for long-channel devices and it is less than one for short-channel devices. R_l is the series resistance on L_G inductor and R_g is the gate resistance of the M_1 device. In Eq. 3.4, δ is the coefficient of gate noise and c is the correlation coefficient between drain and gate noise. The noise contribution of R_1 is neglected since the output of the LNA is isolated from the input due to the high voltage gain. C_{GD} is also neglected to simplify the analysis.

$$NF \cong 1 + \frac{R_l}{R_S} + \frac{R_g}{R_S} + \frac{\gamma}{\alpha} \frac{\chi}{Q_L} \left(\frac{\omega_0}{\omega_T} \right), \quad (3.3)$$

where

$$\chi = 1 + 2cQ_L \sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma} (1 + Q_L^2), \quad (3.4)$$

$$Q_L = \frac{\omega_0(L_1 + L_G)}{R_S} = \frac{1}{\omega_0 R_S C_{GS1}}, \quad (3.5)$$

According to Eq. 3.3, NF increase with higher R_l value and the value of parasitic resistance R_l depends on the quality factor of L_G . The quality factor of spiral inductors are typically 5. Thus, the second term in Eq. 3.3 can be a dominant term of noise figure if an inductor with high value is used for input impedance matching. Eq. 3.3 suggests that NF can be improved by larger transconductance. By the same token, the NF expression includes terms which are proportional to Q_L and inversely proportional to Q_L . It means that minimum NF can be achieved only for a specific Q_L .

3.1.2 Linearity analysis of a cascode LNA

Despite the fact that cascode is a one-stage amplifier, it can be also viewed as a two-stage structure for the sake of linearity as in [55, 56], then the overall AIP3 will be:

$$\frac{1}{AIP3_{OV}^2} \cong \frac{1}{AIP3_{CS}^2} + \frac{\alpha_1^2}{AIP3_{CG}^2}, \quad (3.6)$$

where α_1 is the gain of the common source (CS) stage. If the gain of the CS stage is more than one, AIP3 of the common gate (CG) amplifier is the dominant term in the Eq. 3.6. This implies that linearity change of the CG amplifier due to temperature determines the overall temperature-based AIP3 change. Hence, the CG amplifier in Fig. 3.2 has been analyzed for its AIP3. R_D is the real impedance of the load matching circuit at the operation frequency, and R_S is the output impedance of the CS transistor.

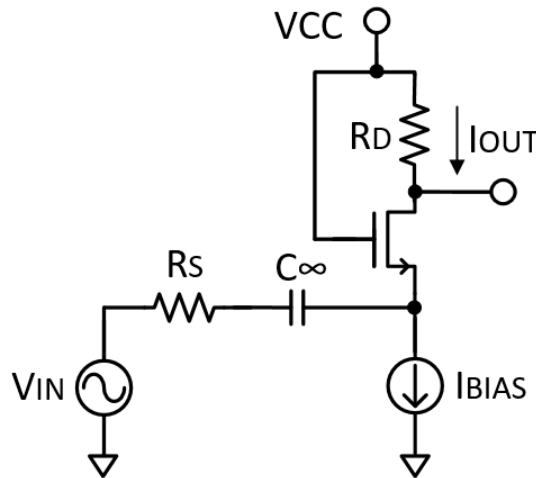


Figure 3.2 : CG amplifier with DC bias.

A linearity analysis performed by neglecting the channel length modulation and the body effect is presented for CS amplifiers in [53]. Derived coefficients for CS amplifiers can be used to express AIP3 of CG amplifiers, as well. Since the input signal is applied to the source of the CG amplifier, only the signs of α_1 and α_3 in the drain current (i_{out}) expression in (3.7) differ from the coefficients given for CS amplifiers. Thus, the AIP3 expression for CS amplifiers provided in [53] can be adopted to represent the AIP3 of the CG amplifier as given in (3.8),

$$i_{out}(v_{in}) = \alpha_1 v_{in} + \alpha_2 v_{in}^2 + \alpha_3 v_{in}^3 \cdots, \quad (3.7)$$

$$AIP3_{CG} \cong \sqrt{\frac{4}{3} \left| \frac{\alpha_1}{\alpha_3} \right|} = \sqrt{\frac{2g_m}{3R_S} \frac{(1 + g_m R_S)^2}{K}}, \quad (3.8)$$

where $K = (1/2)\mu_n C_{ox}(W/L)$. Considering that the output impedance of the CS transistor is high, it can be assumed that $g_m R_S \gg 1$, then (3.8) becomes:

$$AIP3_{CG} \cong 8I_D R_S^2 \sqrt{\frac{I_D}{3R_S(V_G - V_{TH})}}. \quad (3.9)$$

According to Eq. 3.9, the linearity of the LNA strongly depends on the current and it is also proportional to the transconductance of the CG stage. In this analysis, the effect of the gain on linearity is not taken into account. Increase on the current can also improve the gain which may suppress and degrade the linearity as stated in [10].

3.2 LNA Design Procedure

Cryogenic circuit design can be done by using cryogenic transistor models. As an alternative, the circuit designed with standard device models can be modified for cryogenic conditions by analyzing the behavior of transistors at cryogenic temperatures. In this work, due to its more practical nature, the second approach has been preferred. The design has been accomplished such that the biasing of the LNA can be tuned to attain desired specifications at 77 K. Moreover, cascode LNA structure instead of more sophisticated topologies has been selected to explicitly show the dependence of LNA metrics on different design parameters at 77 K. The frequency operation bandwidth (2.025 - 2.12 GHz) has been selected according to the allocated

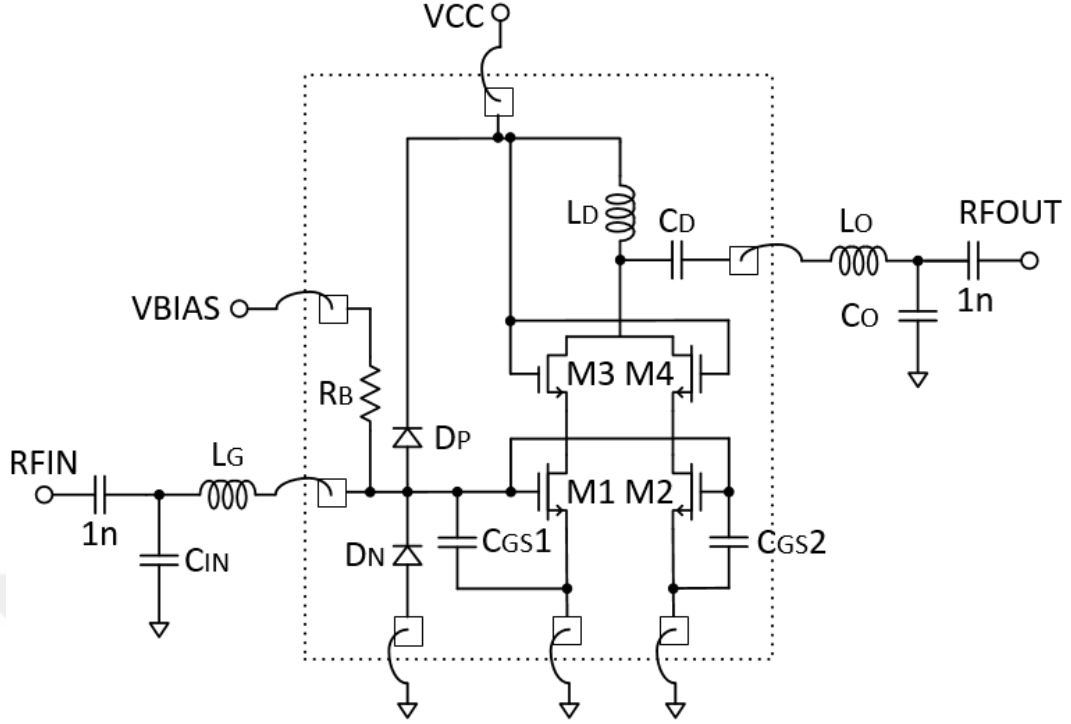


Figure 3.3 : Schematic of the LNA including external components. Dotted lines indicate the chip boundaries.

frequency bands for space communications [16]. The schematic of the designed cascode LNA is given in Fig. 3.3. RF transistors of a commercial 180 nm technology, whose layouts are optimized to diminish parasitic capacitance and resistance, have been used.

Previous studies on cryogenic LNAs show that LNA performance improves at very cold temperatures in terms of gain and NF. Nevertheless, one paper demonstrates that linearity can degrade at low temperatures [10]. Therefore, in the cryogenic LNA design procedure, it does not require significant attention to achieve a high gain and low NF; yet, optimization of DC operating points, impedance matching, and linearity at cryogenic temperatures are the main concerns in cryogenic LNA design. The expression in (3.9) asserts that IIP3 can be retained by preserving the room temperature I_D at cryogenic temperatures. Moreover, linearity can also improve since the threshold voltage increases. Given the DC characteristics measurements of the same RF CMOS transistor, $I_D - V_{GS}$ curves at 77 K and 300 K intersect each other around a V_{GS} value 0.75 V [3]. By considering the impact of V_{DS} and process variations on the exact value of this intersection point, the cascode LNA can be designed to properly operate at a gate bias voltage of 0.7 - 0.8 V for the CS transistor. Therefore, an adjustable biasing

structure is employed and V_{bias} has been chosen as 0.74 V, which is near to the intersect point of currents at 77 K and 300 K.

A very high-value resistor R_B has been placed between V_{bias} and the CS gate to minimize the noise contribution of V_{bias} input to overall NF. Furthermore, the impedance matchings of the LNA have been done off-chip. In order to perform NF measurements with the cryogenic attenuator method, LNA should be bonded to a printed circuit board (PCB). This implies that bond wire inductances will be involved in input and output impedance matchings. However, it is difficult to estimate the exact inductance value of bond wire inductors a priori. Moreover, the uncertainty in the quality factor value of on-chip inductors may degrade the impedance matching at cryogenic temperatures, mainly due to reduced parasitic resistances. Thus, the input and output impedance matchings have been realized by discrete passive components in the simulation. It also allows to realize the impedance matchings experimentally thereby averting any possible deterioration in the impedance matchings comes from the aforementioned uncertainties.

In addition, bond wires instead of spiral inductors have been used as source degeneration inductors to reduce the total area of the chip. Bond wires have a higher quality factor than spiral inductors, which means that they comprise less parasitic resistance and their noise contribution is lower compared with on-chip inductors. As clearly shown in Eq. 3.1, the value of source degeneration inductor should be small to obtain a high gain. The bond wire inductances are proportional to bond wire lengths; therefore, their inductance values have been roughly calculated according to the lengths of bond wires. The length of bond wires depends on the size of the chip package; thus, the smallest available package, QFN16 with $5 \times 5 \text{ mm}^2$ size, has been chosen to lower the inductance value of bond wires. However, the inductance values are still high even with the smallest chip package. As a practical solution, two bond wires have been used in parallel.

Width of the CS transistor is set to a high value to improve NF and IIP3, but the power consumption rises, as well. A capacitor (C_{GS}) is inserted between the gate and source of the CS transistor for NF matching. As stated in Section 3.1.2, minimum NF exists only for a matching point. As illustrated in Fig. 3.4, minimum NF point has been shifted towards to the unit circle in the Smith Chart by adding the C_{GS} capacitor.

Even though adding the C_{GS} leads the minimum NF value increase as indicated in Eq. 3.3, it has been observed that NF improves. In conclusion, the value of C_{GS} and the width of the CS transistor have been optimized for NF and real part of input impedance matching. Afterward, both NF and input impedance can be matched to 50 ohm by adding series inductor L_G to the RF input. However, parasitic capacitances of added electrostatic discharge (ESD) protection diodes lower the real part of input impedance. Thus, L-matching network is preferred to achieve both imaginary and real parts of input impedance matching. Since the source degeneration inductor is not adjustable, the objective gain has been achieved by L_D . L-matching network has been also employed at the output stage.

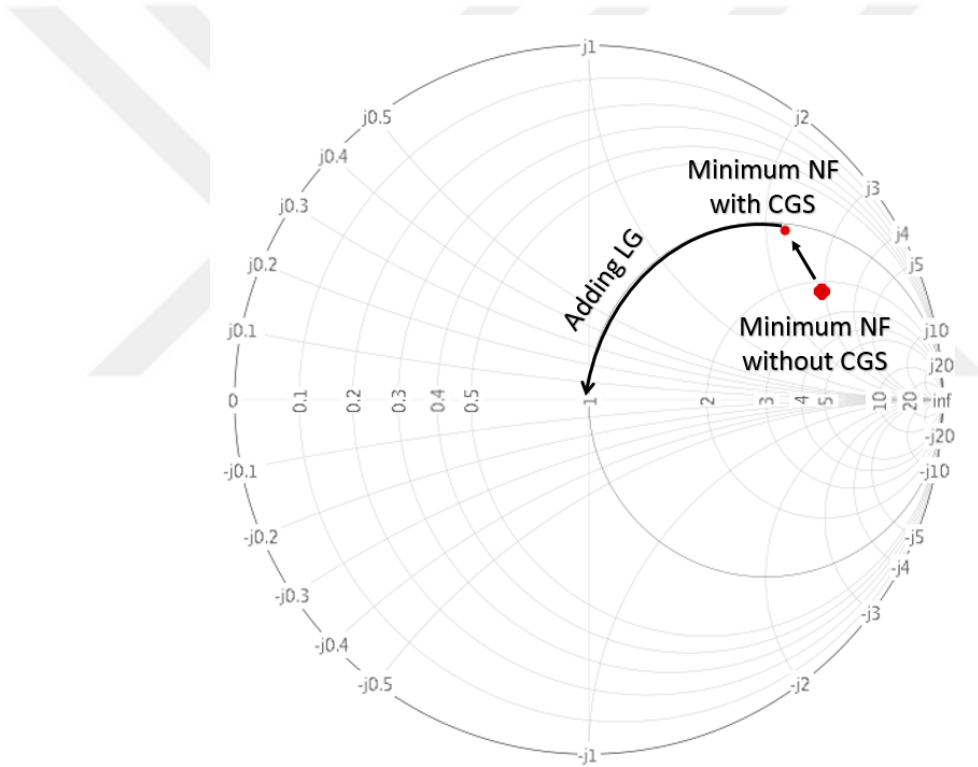


Figure 3.4 : NF optimization with C_{GS} and L_G on the Smith Chart.

A parallel transistor has been added to both CG and CS transistors due to the number of finger constraint on RF transistors. Parallel transistors are shown separately since sources of CS transistors are not connected to each other to make layout design straightforward.

ESD diodes, D_N and D_P have been added to the transistor gates to prevent them from the damage occurring due to the charge device model (CDM) event during the wire bonding process. ESD structures also enable safety during handling of the LNA in

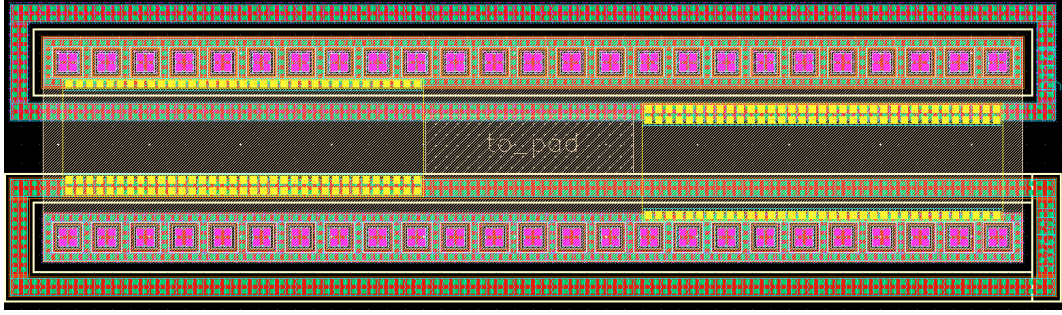


Figure 3.5 : The layout of the designed dual-diode ESD structure with 25 fingers.

Table 3.1 : Parameters of Circuit Elements

Parameter	Value
Width of M1, M2, M3, M4	65 μm
Length of M1, M2, M3, M4	180 nm
R_B	113 K
C_{GS1} and C_{GS2}	103 fF
L_D	4.8 nH
C_D	600 fF
L_O	2.5 nH
C_O	1.5 pF
L_G	9 nH
C_{IN}	1 pF
V_{BIAS}	740 mV

cryogenic measurements. The dual-diode structure is a potent ESD protector, yet it has large junction capacitance, which severely degrades NF due to signal loss. As discussed in [57], the junction capacitance value is principally proportional to the bottom plate of the diode. Since diode current passes through the p-n junction wall, the robustness of dual-diode can be directly assessed with their junction perimeter. Multiple finger structure has been utilized to minimize the total junction capacitance of ESD diodes while making the perimeter longer [58]. The UMC 0.18 μm technology allows minimum 940 nm as width and length of diodes; thus, finger sizes are set to the minimum value to maximize the junction perimeter in the unit area. Finger number of these diodes has been determined according to the recommended CDM

protection level. It is stated in [59] that CDM ESD protection up to 250 V should be satisfied for safe manufacturing. CDM peak current is commensurate with chip package size [60]. The current can go up to 1 A for 25 mm² package size at 250 V stress voltage [59]. In [61], it is showed that ESD dual diodes with 107.5 μm junction perimeter are resilient up to 1.8 A current. To keep the parasitic capacitances low as much as possible, the finger number of the dual-diodes at the RF input has been chosen as 25 thereby providing 94 μm junction perimeter, which is presumed by utilizing the results in [61] that it will yield protection up to 1 A CDM current level. The inputs connected to other transistor gates are protected by much larger ESD diodes since their impact on the LNA performance is negligible.

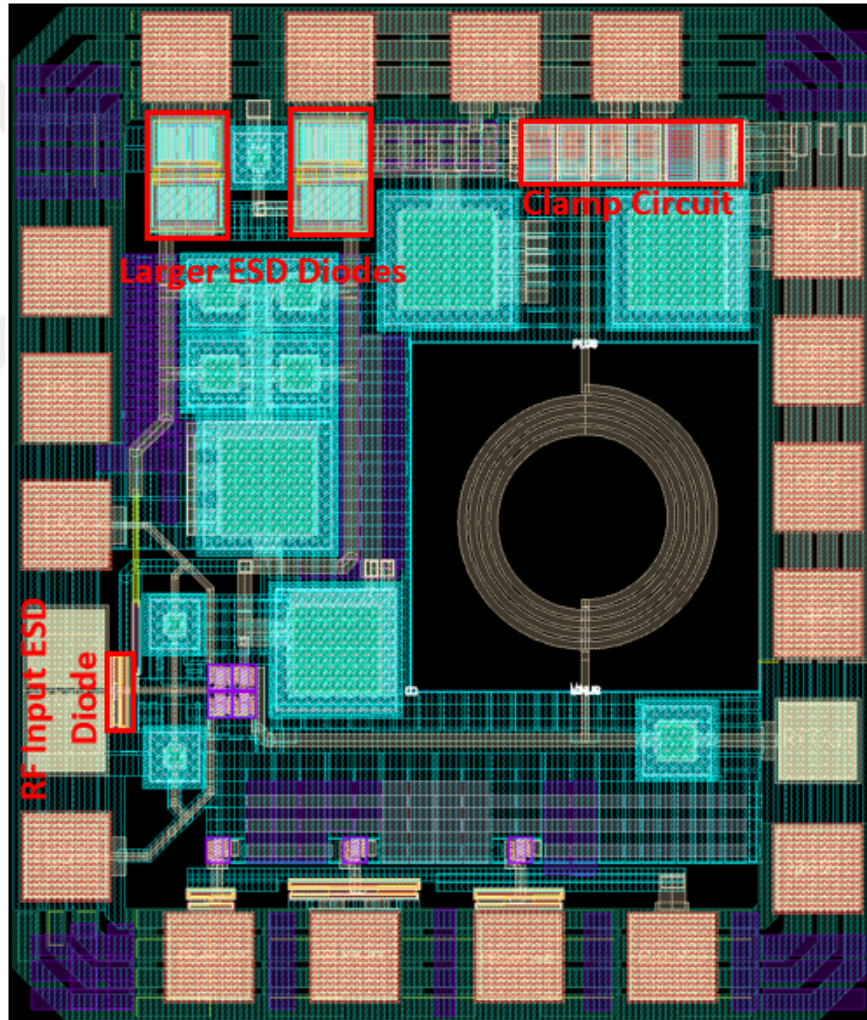


Figure 3.6 : The layout of the designed LNA (754 x 654 μm^2).

The layout of the designed LNA is given in Fig. 3.6. After parasitic extraction of the whole layout is performed, component values have been optimized. Values of the components in the LNA design are shown in Table 3.1. It occupies an area less than

500 μm^2 . In addition to ESD diodes, a clamp circuit, which includes 6 series diodes, has been added to make charges flow from VCC to the ground when an instantaneous positive ESD voltage occurs.

3.3 Post-layout Simulation Results

In this section, post-layout simulation results are presented at 300 K. According to these simulation results, both input and output return losses are higher than 10 dB within 2.025-2.12 GHz frequency bandwidth as seen in Figs. 3.7 and 3.8. Also, the gain is around 15.5 dB within this bandwidth as given in Fig. 3.9 and NF is approximately 1.6 dB as indicated in Fig. 3.10. Finally, 2 dBm IIP3 has been obtained as shown in Fig. 3.11.

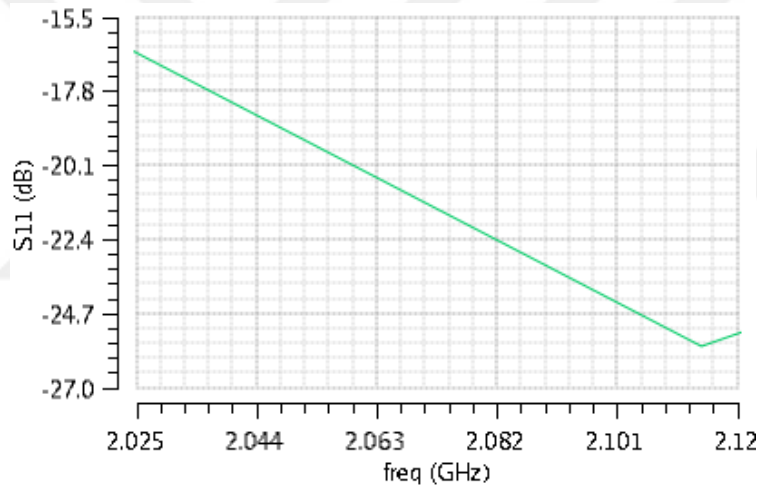


Figure 3.7 : Simulated S11 of the designed LNA.

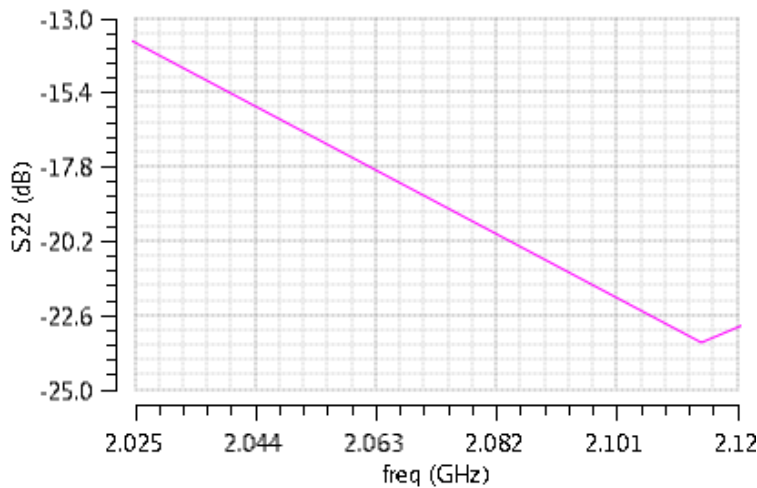


Figure 3.8 : Simulated S22 of the designed LNA.

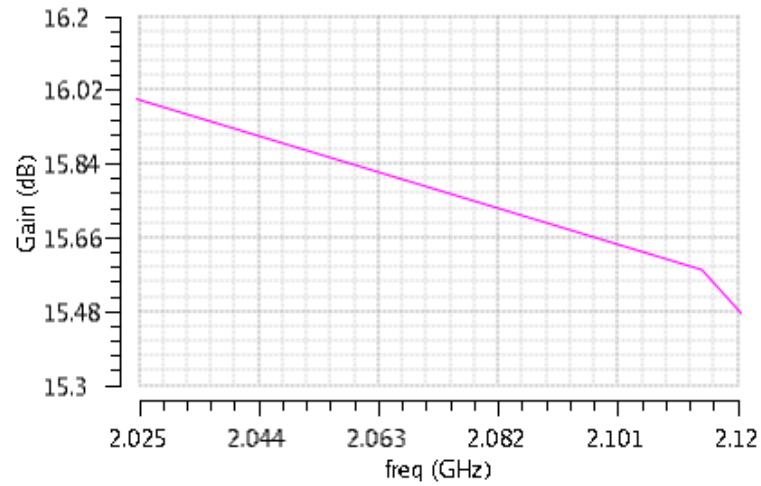


Figure 3.9 : Simulated gain of the designed LNA.

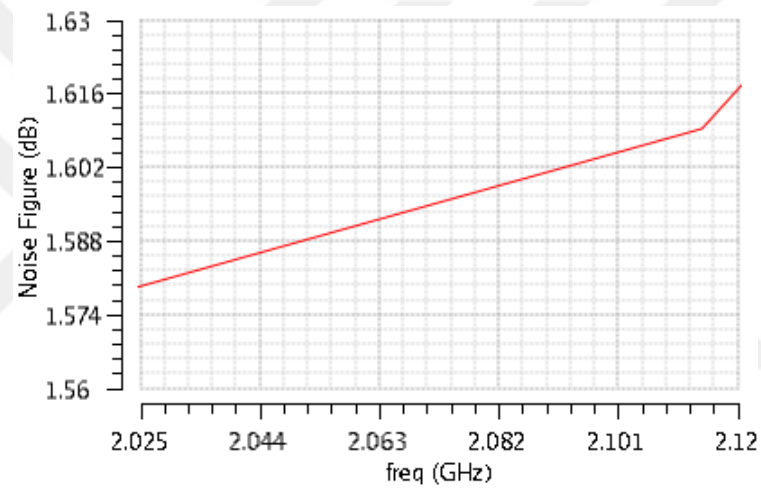


Figure 3.10 : Simulated NF of the designed LNA.

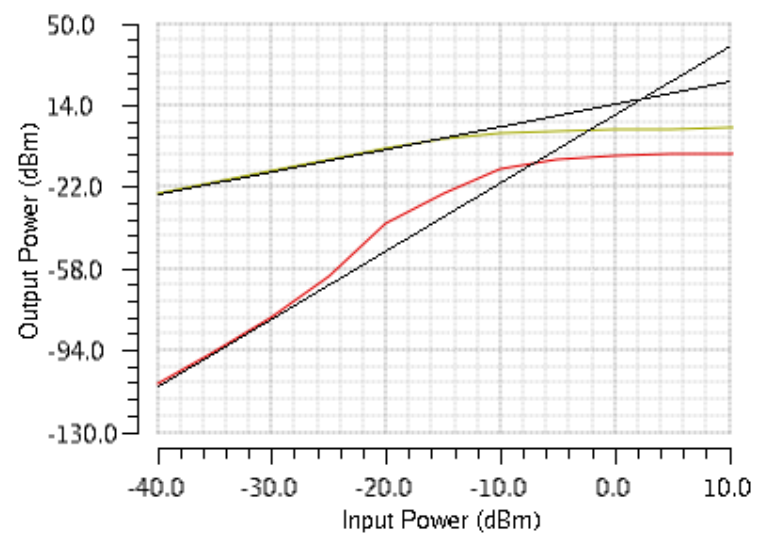


Figure 3.11 : Simulated IIP3 of the designed LNA.



4. MEASUREMENT RESULTS

Measurements of the designed LNA have been performed at 77 K and 300 K. Variations on the performance of the designed LNA at 77 K are discussed in this section. Moreover, the LNA has been measured at 300 K after the LNA is irradiated by gamma radiation and the results are compared with pre-rad measurements.

4.1 Measurement Results at Room and Cryogenic Temperatures

Micrograph of the fabricated chip is shown in Fig. 4.1. The chip has been soldered onto a PCB, which has been designed specifically for the fabricated LNA. The test board of the fabricated LNA is presented in Fig. 4.2. Up-side of the chip package has been left open to provide direct exposure of the chip during the total ionizing dose radiation test.

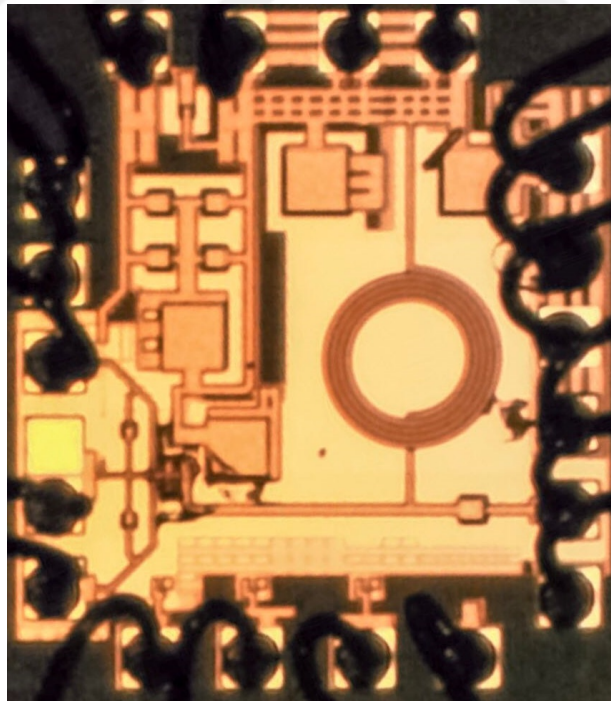


Figure 4.1 : Micrograph of the fabricated LNA.

For input and output impedance matchings, high-Q inductors have been employed to reduce parasitic resistance and ceramic capacitors of Johanson Technology with

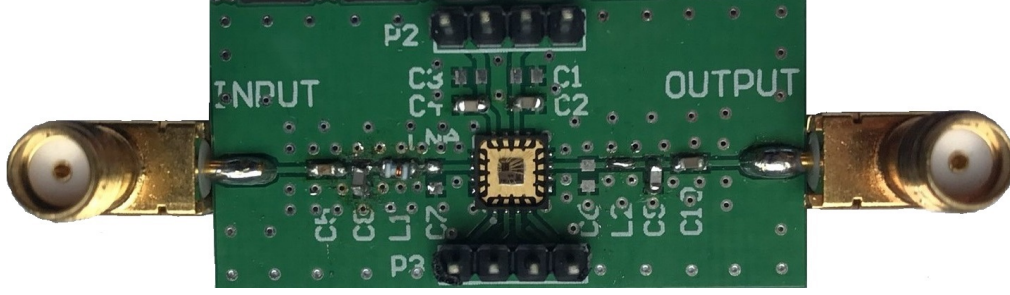


Figure 4.2 : Test board of the fabricated LNA.

negative-positive 0 ppm/°C (NP0) dielectric have been used to keep matching variations very low at cryogenic temperatures. As reported in [62], the NP0 capacitances rise by approximately %2 from 300 K to 77 K. Values of the discrete passive components have been experimentally chosen such that S_{11} and S_{22} will be below -10 dB at both room and cryogenic temperatures. Discrete components differ from their amounts in the simulation due to the variability in device process and inductance values of bond wires and selected component values are given in Table 4.1.

Table 4.1 : Values of Discrete Components

Element	Value
L_O	6.2 nH
C_O	0.7 pF
L_G	2.2 nH
C_{IN}	3.3 pF

Measurements of the cryogenic LNA have been performed by using liquid nitrogen (LN2) in a thermos as illustrated in Fig. 4.3. Initially, it has been verified with controlled experiments that the thermos does not affect the accuracy of measurements. The current consumption of the LNA is 8.31 mA and 8.53 mA at 77 K and 297 K, when $V_{bias} = 0.74$ V, respectively. This yields almost the same current for the LNA at 77 K and 297 K, thereby mitigating the linearity degradation based on reduced current densities due to V_{TH} increase at cryogenic temperatures. Even though the minimum noise current density may somewhat change at cryogenic temperatures, since the noise figure comes down significantly, the current difference leads to a very small deviation

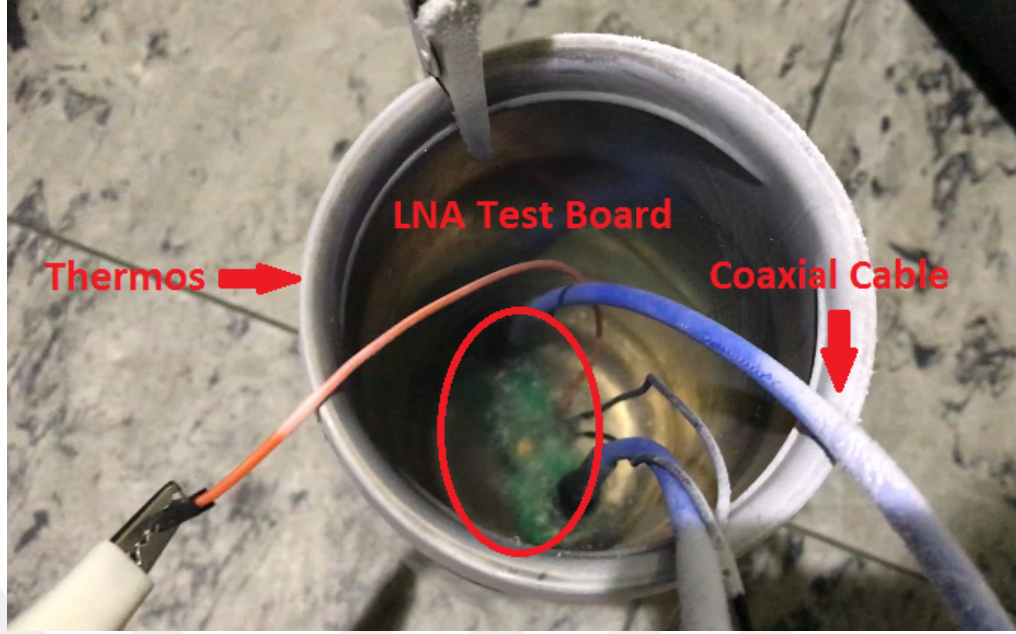


Figure 4.3 : Cryogenic measurement setup of the LNA.

from the minimum noise figure, which can essentially be neglected. Therefore, it is not very rewarding in terms of NF to determine the biasing point according to minimum noise current density.

As given in Figs. 4.4 and 4.5, input and output return losses are greater than 10 dB at 77 K and 297 K. Due to the increase of ceramic capacitor values, input and output matching resonances shifted towards to lower frequencies. The amount of capacitance

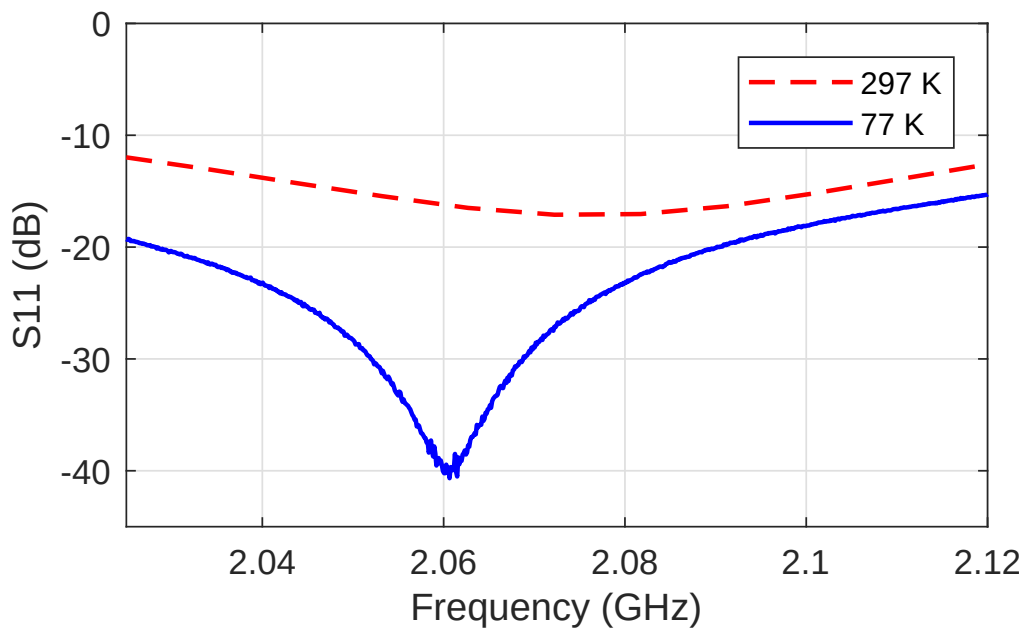


Figure 4.4 : Measured S_{11} of the fabricated LNA at 297 K and 77 K.

variation in the input matching is higher compared to the one in the output matching since a larger capacitor has been employed in the input matching circuit. That's why, S_{11} varies more than S_{22} at 77 K.

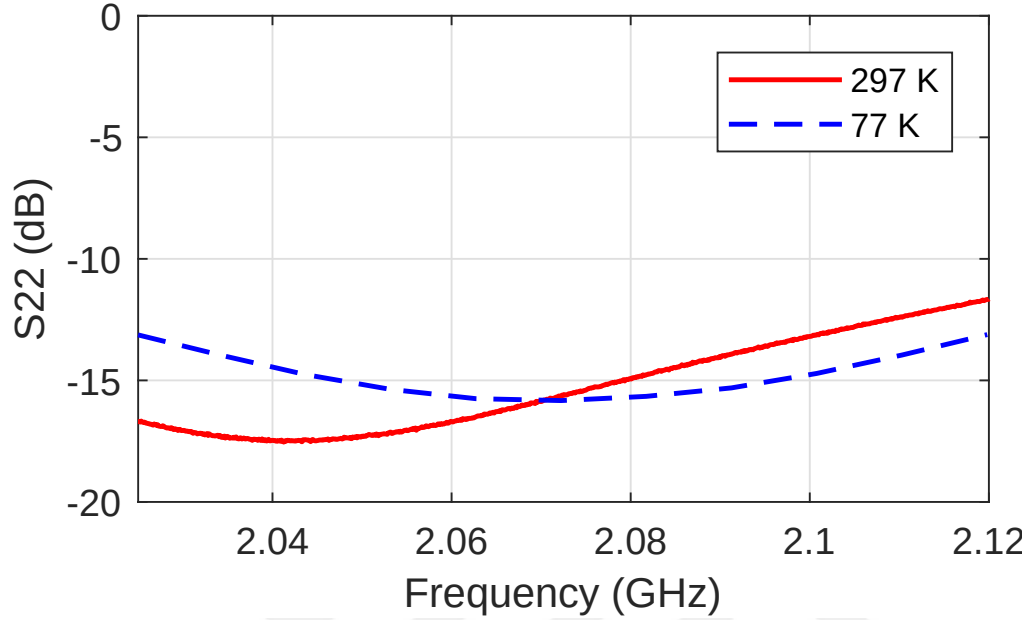


Figure 4.5 : Measured S_{22} of the fabricated LNA at 297 K and 77 K.

S_{21} of the LNA reaches approximately 15.5 dB at 297 K (Fig. 4.6). The gain rises at low temperatures because of the increase in electron mobility as demonstrated in previously published LNAs. Accordingly, the gain of the designed LNA here has improved by 2.3 dB at 77 K.

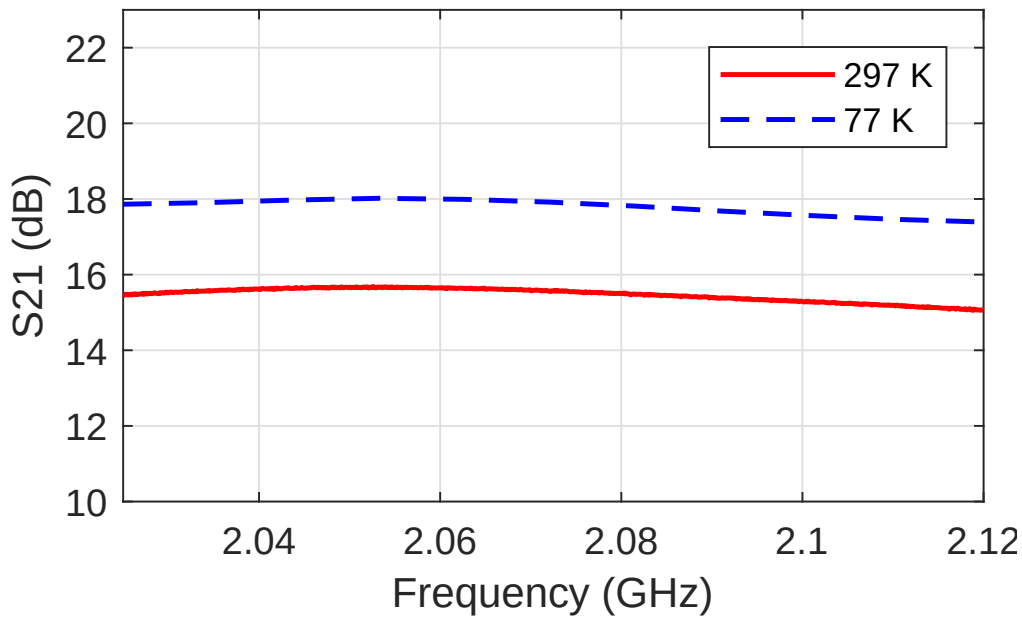


Figure 4.6 : Measured S_{21} of the fabricated LNA at 297 K and 77 K.

IIP3 and 1-dB compression point are 2.1 dBm and -16.2 dBm at 297 K, respectively as shown in Fig. 4.7. IIP3 degradation did not occur, since the same current density has almost been preserved at 77 K as presented in Fig. 4.8. Moreover, IIP3 has approximately improved by 1 dB. It has been verified by simulation that the CS stage has a gain value more than unity; therefore, AIP3 of the CG amplifier is the dominant term in the overall linearity expression in Eq. 3.9. According to Eq. 3.9, the 1 dB improvement occurs due to the rise of the threshold voltage.

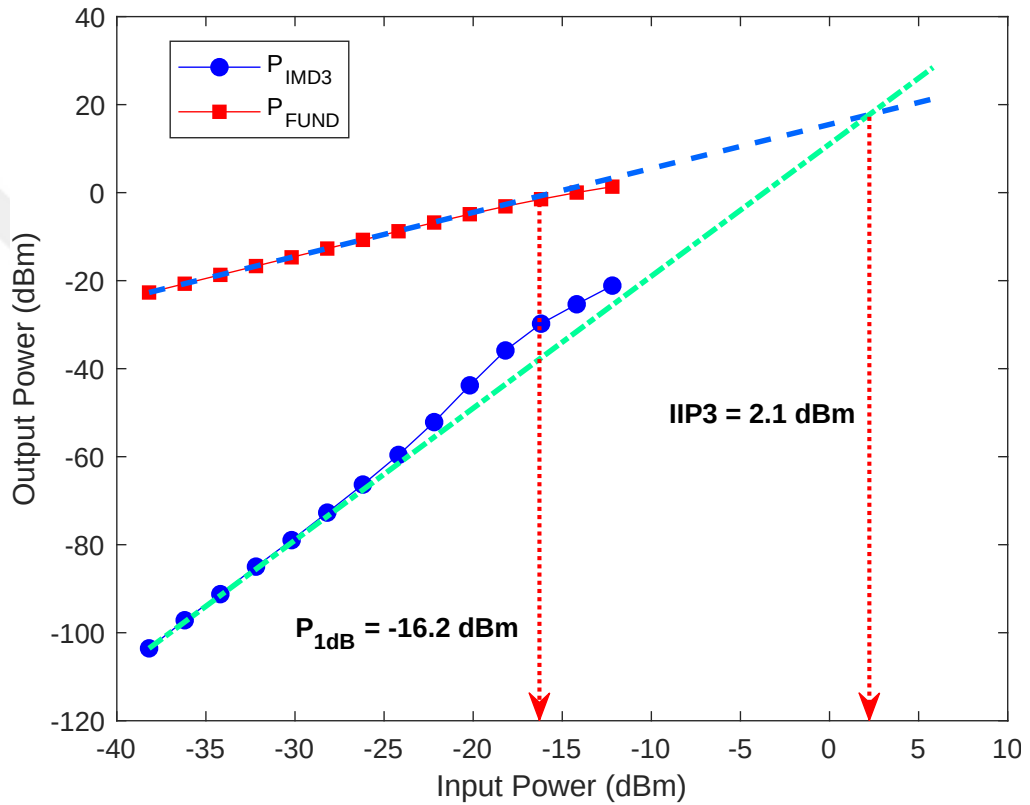


Figure 4.7 : Measured IIP3 and P1dB of the fabricated LNA at 297 K.

Only one of the previously published cryogenic LNAs presents its IIP3 performance at both room and cryogenic temperatures and according to its measurement results, IIP3 degrades when the temperature goes down, which has been attributed to the gain improvement in [10]. Therefore, in order to evaluate the variation on the IIP3 accurately, it is also important to verify that increase on the gain does not suppress IIP3 improvement. This interaction between gain and IIP3 can alter for different bias points. Thus, a graphic of IIP3 vs. gain for different current values around the normal bias point is provided to examine this relationship for the designed LNA. In this design, gain improvement does not restrict the linearity performance of the LNA. On the contrary, both gain and IIP3 increase with the rise in current (Fig. 4.8).

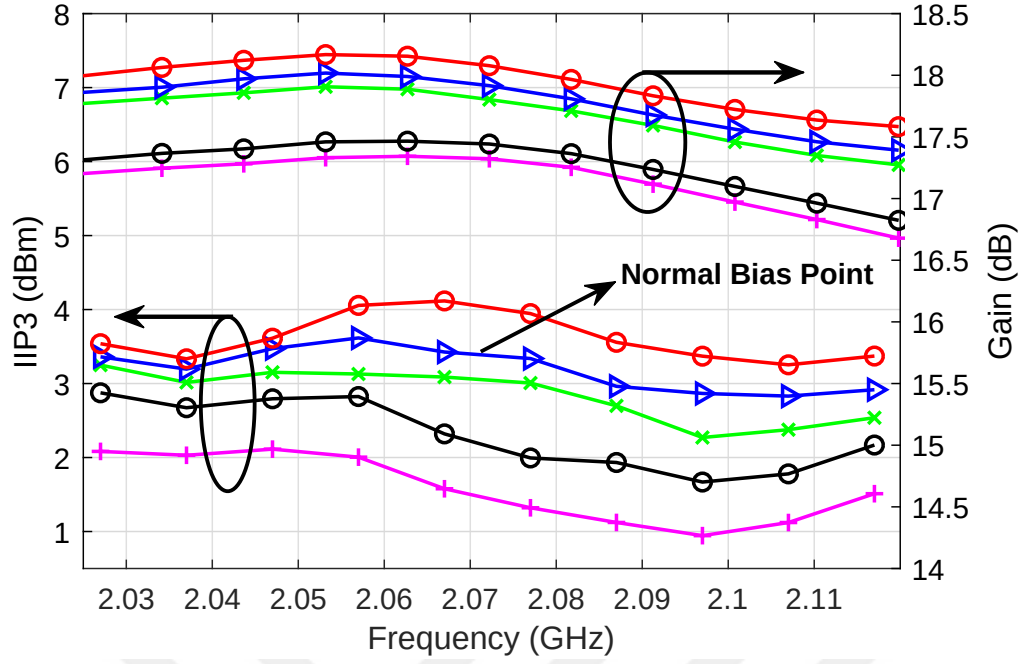


Figure 4.8 : IIP3 vs. gain graph at different bias points of the LNA at 77 K. Current values of each bias point for both IIP3 and gain lines are 5.95, 6.5, 7.7, 8.31, and 9.6 mA from bottom to top, respectively. The second IIP3 line from the top indicates the IIP3 performance of the fabricated LNA at the normal bias point.

On-chip NF measurement at cryogenic temperatures is possible through advanced probe stations; nevertheless, their experimental setup is very expensive [63]. In addition, high accuracy NF measurement can be performed with some advanced measurement devices like Keysight PNA-X Series Network Analyzers [64]. Their advantage is to mitigate the effect of the two largest error sources, which are impedance mismatches between devices and non-ideal match of the noise source interacting with noise generated by the device under test (DUT). However, their measurement accuracy is still deeply affected by excess noise ratio (ENR) uncertainty, which is usually around ± 0.2 dB. Since NF of the DUT at room temperature is usually much higher than the improved uncertainty level provided by such advanced measurement devices, the accuracy level is very satisfactory for room temperature NF measurements. Notwithstanding this situation, the uncertainty level can be comparable to the NF of the DUT at cryogenic temperatures. As a practical solution to this issue, NF measurement using a cryogenic attenuator is the most prevalent method, where the cryogenic attenuator significantly reduces measurement errors, especially the error introduced by the ENR uncertainty of the noise source as elaborated in [65]. Therefore,

a cryogenic attenuator has been employed in cryogenic NF measurements to obtain reasonably accurate experimental results. Standard Y factor method has been utilized by a Keysight PXA spectrum analyzer at both room and cryogenic temperature NF measurements. Usage of a large attenuator helps to minimize measurement errors by lowering the ENR value. However, the lowest ENR value is determined by the criterion (4.1), which is required for accurate NF measurements [66]. This criterion also limits the maximum attenuator value that can be used,

$$ENR_{dB} > NF_{dB}^{SA} + 3dB, \quad (4.1)$$

where NF_{dB}^{SA} is the total NF seen after the DUT. According to (4.1), the most eligible attenuator value is around 13 dB for our measurement setup; thus, a 10 dB cryo-attenuator, which was the best available component below 13 dB, has been chosen for cryogenic NF measurements. As depicted in Fig. 4.9, both the 10 dB-cryogenic attenuator and the LNA are in LN2 environment during cryogenic NF measurements. Since ENR of the noise source has been calibrated at 290 K, ambient temperature has been fixed to 290 K to prevent any further measurement uncertainty. A preamplifier with a good input matching has been utilized to improve the measurement accuracy by lowering the total NF after DUT as well as NF_{dB}^{SA} to yield a larger attenuation. The noise source and the LNA are connected to the attenuator and the preamplifier with coaxial cables, respectively. The noise source and the preamplifier stand inside a bench-top oven whose inner temperature has been adjusted to 290 K to prevent penetration of the cold from LN2 to them via the cables. Insertion loss on coaxial cables varies with temperature. Since temperatures at the two ends of the coaxial cables are different, a temperature gradient occurs over the parts of the cables remaining outside of the oven. Although their insertion losses are known at 290 K, it is hard to predict their total loss due to the temperature gradients over them. Thus, it makes the loss compensation procedure difficult. To simplify, the average temperature over the outside parts of the cables has been assumed as the middle point of the cold and hot temperatures. However, this assumption can cause serious uncertainty. To reduce it as much as possible, coaxial cables with very low insertion loss have been used, and only small portions of these cables stand outside of the oven. Furthermore, all NF measurements have been performed in a Faraday cage to prevent any contribution of other noise components in the air to the measured NF.

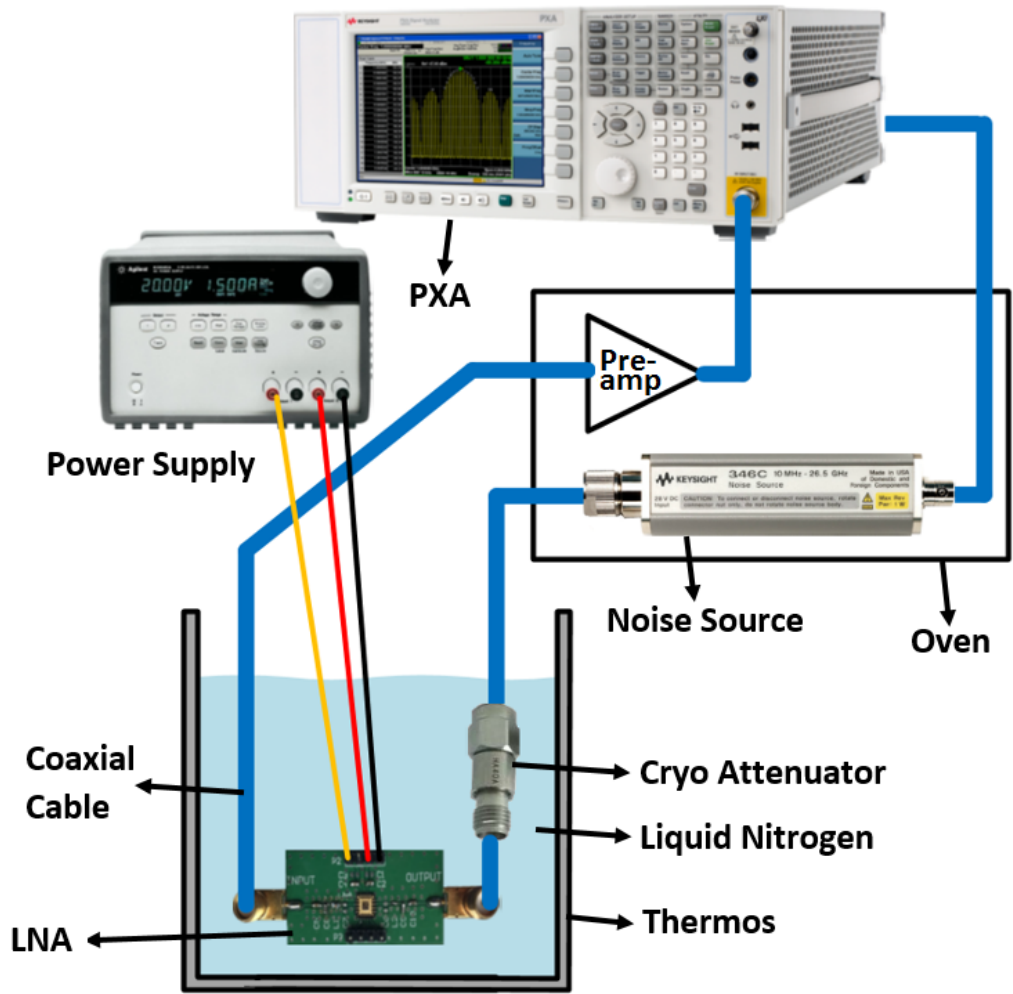


Figure 4.9 : Cryogenic NF measurement setup.

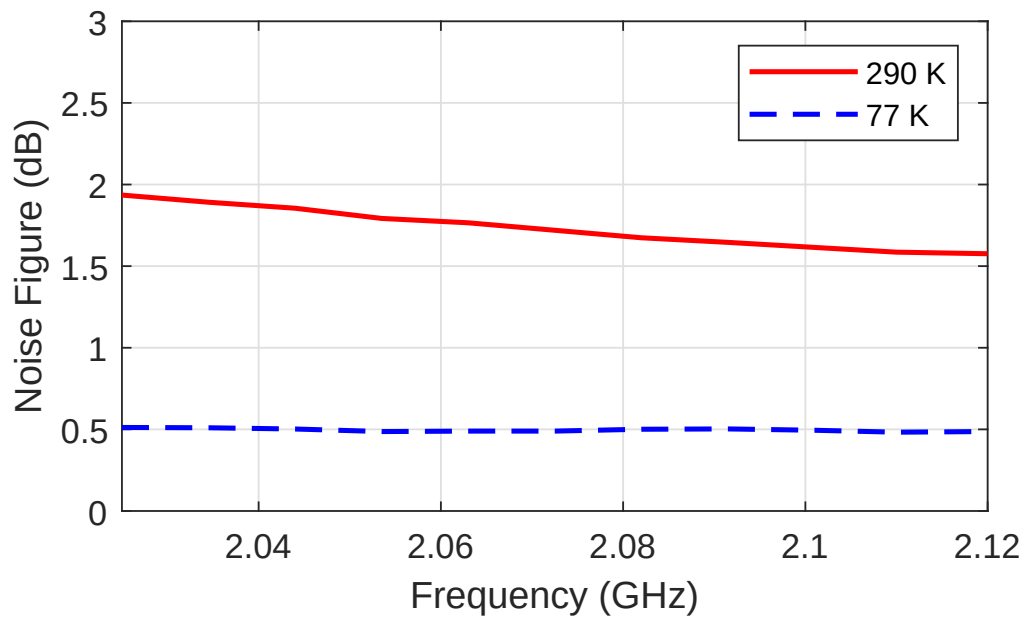


Figure 4.10 : Measured NF of the fabricated LNA at 297 K and 77 K.

Table 4.2 : Uncertainty of Cryogenic NF Measurement

Parameter	Nominal Value	Tolerance	Resultant Error (K)
ENR	14.36 dB	± 0.19 dB	± 5.847
Room Temperature	290 K	± 0.5 K	± 0.008
Cold Temperature	77.2 K	± 0.25 K	± 0.226
Cryogenic Attenuator Loss	9.84 dB	± 0.01 dB	± 0.259
Input Cable Loss	0.44 dB	± 0.01 dB	± 0.278
Input Cable Average Temperature	183.5 K	± 106.5 K	± 1.305
Output Cable Average Temperature	183.5 K	± 106.5 K	± 0.048
Impedance Mismatch		Mismatch Loss	Resultant Error (K)
Noise Source-Preamplifier		0.033 dB	± 0.053
Noise Source-Attenuator-LNA		0.004 dB	± 0.11
LNA-Preamplifier		0.05 dB	± 0.081
Total Error			± 8.215 K

Table 4.3 : Uncertainty of NF Measurement at Room Temperature

Parameter	Nominal Value	Tolerance	Resultant Error (K)
ENR	14.36 dB	± 0.19 dB	± 19.35
Room Temperature	290 K	± 0.5 K	± 0.243
Impedance Mismatch		Mismatch Loss	Resultant Error (K)
Noise Source - Preamplifier		0.033 dB	± 0.081
Noise Source - LNA		0.044 dB	± 1.54
LNA - Preamplifier		0.046 dB	± 0.113
Total Error			± 21.327 K

Thermal noise is the main noise source of MOSFETs at high frequencies. Therefore, input referred noise power of circuits decreases proportional with the reduction of temperature as illustrated by many cryogenic LNAs in literature. Fig. 4.10 depicts that the NF of the designed LNA is between 1.5 dB and 2 dB in the frequency band of operation at 290 K, which decreases to 0.5 dB at 77 K. As provided with detail in Tables 4.2 and 4.3, resultant errors of all sources of uncertainty have been calculated for a single frequency (2.075 GHz) by assuming that they are uncorrelated. Total measurement uncertainty has been reduced from ± 21 K (± 0.3 dB) to ± 8 K (± 0.12 dB) by including a cryogenic attenuator in the measurement setup. The main improvement comes from the reduction in ENR error. Errors due to mismatches also decrease mainly because of amelioration of LNA input matching at 77 K. The uncertainty arising from the temperature gradient over the coaxial cables is acceptable. The total error is still dominated by the ENR uncertainty. The obtained total error at the cryogenic temperature is commensurate with the operating temperature. At much lower ambient temperatures, it is possible to use an attenuator with a higher loss, which is leading to further improvement of measurement errors. The trade-off between attenuator loss and attenuator physical temperature can be clearly seen in (4.2) by assuming a minimum ENR value [65]. T_{ON} and T_{OFF} are noise temperatures when noise source is on and off, respectively. L_{att} is the loss of the attenuator, and T_{att} is the physical temperature of the attenuator.

$$ENR_{new} = \frac{T_{ON} - T_{OFF}}{T_{OFF} + T_{att} \cdot L_{att} - T_{att}}. \quad (4.2)$$

The equivalent noise temperature of the designed LNA is greater than the noise figure of prior cryogenic LNAs mainly because of having higher ambient temperature and the presence of ESD protection (Table 4.4). The designed LNA has a moderate power consumption compared to other cryogenic LNAs. However, the selected bias point of the CS transistor, which mainly determines the power consumption, yields high linearity at 77 K.

Table 4.4 : Performance Comparison of the Designed Cryogenic LNAs with Prior Work

Ref.	This Work	[10]	[29]	[30]	[67]	[31]	[6]	[7]	[68]
Tech. (nm)	CMOS (180)	CMOS (160)	SiGe HBT (120)	SiGe HBT	HEMT	SiGe HBT (130)	SiGe HBT (130)	SiGe HBT (180)	SiGe HBT (120)
Freq. (GHz)	2.025 - 2.12	0.01 - 0.5	1.5	0.1 - 1	2.2 - 2.3	0.5 - 4	8 - 12	1	1 - 20
T_e (K)	35.4	6.8	4.3	8	12.4	8	21	2.1	18
Power (mW)	15	54.9	20	0.7	-	8.3	2.25	4.2	60
S_{11} (dB)	<-15	-8	-14.1	<-10	-22	<-10	-10	-	<-10
S_{22} (dB)	<-13	-	-17.3	<-10	-18	<-10	-20	>-12	<-10
S_{21} (dB)	18	57	31.7	>20	22.8	>25	15	28	23
IIP3 (dBm)	3.4	-47	-25.8	-	-	-	-	-	-5
ESD	Yes	-	-	Yes	-	-	-	-	-
Temp. (K)	77	4	15	12	77	19	15	15	17

4.2 Measurement Results After Irradiation

The designed LNA has been irradiated by 650 krad total ionizing dose (in 4 hours) using a Co-60 gamma-ray source to investigate the robustness of the LNA against radiation. During the radiation test, the designed LNA has been biased with the normal V_{bias} value (740 mV). The test has been conducted at room temperature following the standards of European Space Agency (ESA) for radiation testing of electronic equipments [69]. Post-irradiation measurements of the LNA have been performed 48 hours after the irradiation. Pre- and post-irradiation measurement results of S-parameters, NF, and IIP3 are compared in Figs. 4.11 and 4.12. Measurement results show that there are variations by 3 dB and 1 dB on the input and output impedance matching, respectively. This variation may primarily stem from the capacitance change of ceramic capacitors after gamma radiation [70]. However, LNA performance has not been affected in terms of NF, gain, and IIP3. Although some radiation-hardening techniques like annular gate structures have been used to satisfy protection against irradiation for space applications [71], our experimental results

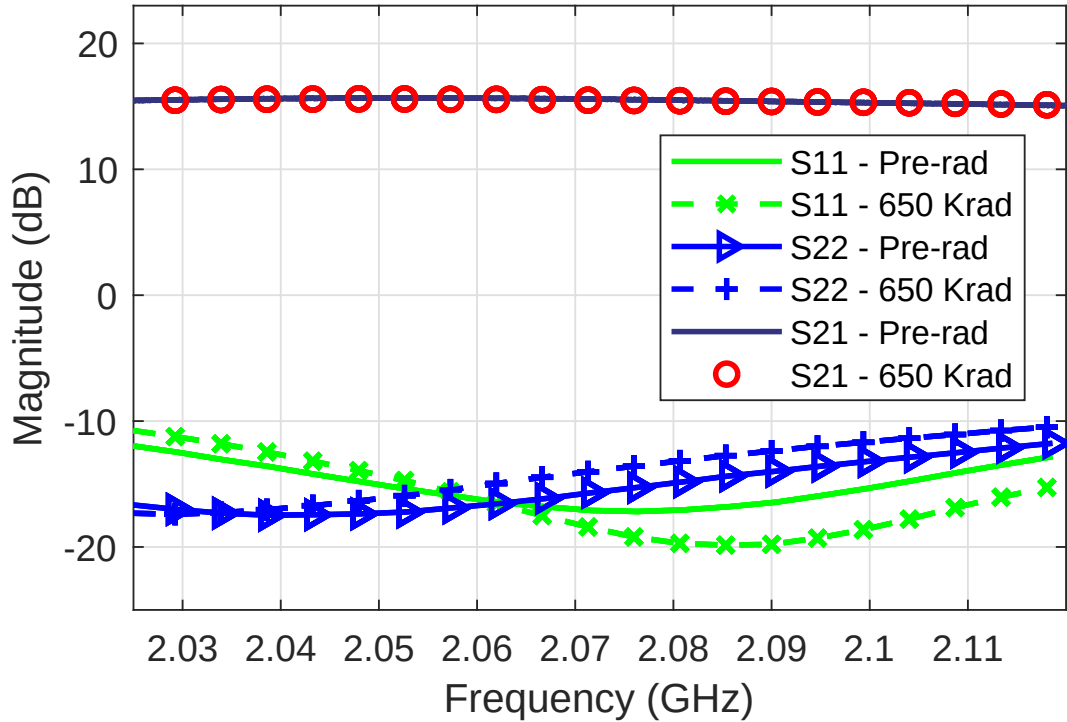


Figure 4.11 : Measured pre- and post-irradiation S-parameters of the fabricated LNA at 297 K.

demonstrate that the RF NMOS transistor, whose layout comes with a guard ring around it for substrate-coupled noise protection, from the utilized 180 nm CMOS technology has enough resilience against gamma radiation, and it does not require any further radiation-hardening techniques to be applied.

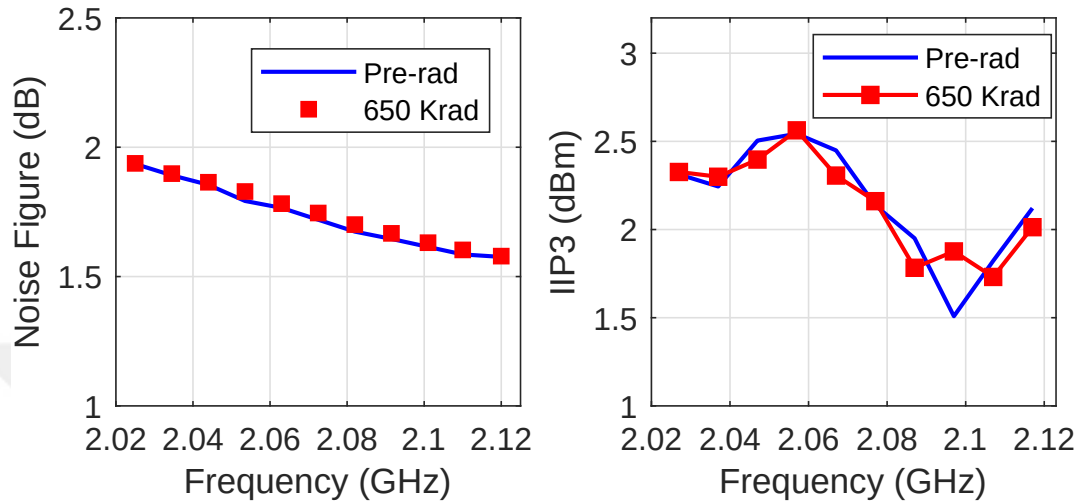


Figure 4.12 : Measured pre- and post-irradiation noise figure (*on the left*), and IIP3 (*on the right*) of the fabricated LNA at 297 K.



5. CONCLUSIONS AND RECOMMENDATIONS

This thesis focuses on the design of a high linearity LNA at both room and cryogenic temperatures. Linearity performance of the cryogenic CMOS LNA has been examined in detail for the first time. It has been demonstrated that both gain and IIP3 improvements can be achieved without utilizing a cryogenic CMOS model if the current density is preserved at cryogenic temperatures with proper biasing. Thus, it has been verified that all performance metrics of an LNA can be improved through this approach. A detailed analysis of the cryogenic noise measurement has been performed to properly estimate the measurement uncertainty involved. Furthermore, it is shown that RF CMOS transistors of the employed 180 nm CMOS technology with no specific radiation protection is robust enough against gamma radiation, and LNAs designed in this technology can sustain their performance up to 650 krad total ionizing dose. Consequently, they can safely be utilized in space applications.



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