ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

A NOVEL SYMMETRIC LATTICE-BASED WIDEBAND-WIDE PHASE RANGE DIGITAL PHASE SHIFTER DESIGN

Ph.D. THESIS

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Department of Electronics and Communication Engineering

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

SİMETRİK KAFES YAPILI GENİŞ BANTLI-GENİŞ FAZ ARALIKLI ÖZGÜN SAYISAL FAZ KAYDIRICI TASARIMI

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Celal Avcı, a Ph.D. student of ITU Graduate School of Science Engineering and Technology student ID 504122204, successfully defended the thesis/dissertation entitled "A NOVEL SYMMETRIC LATTICE-BASED WIDEBAND-WIDE PHASE RANGE DIGITAL PHASE SHIFTER DESIGN", which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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To my wife Habibe, my children Güven and Değer, and my parents

FOREWORD

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May 2019 Celal AVCI

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ABBREVIATIONS

TPG	**:** Transducer Power Gain
GHz	**:** Gigahertz
MHz	**:** Megahertz
CMOS	**:** Complementary Metal Oxide Semiconductor
MOSFET	**:** Metal Oxide Semiconductor Field Effect Transistor
NMOS	**:** N-Channel Metal Oxide Semiconductor
PMOS	**:** P-Channel Metal Oxide Semiconductor
SOI	**:** Silicon on Insulator
GaAs	**:** Gallium Arsenide
KCL	**:** Kirchoff Current Law
KVL	**:** Kirchoff Voltage Law
RMS	**:** Root Mean Square
P1dB	**:** 1dB Compression Point
IP3	**:** Third Order Interception Point
IM	**:** Intermodulation
PDK	**:** Process Design Kit
EM	**:** Electromagnetic
3D	**:** Three Dimension
IC	**:** Integrated Circuit
MMIC	**:** Milimeter Microwave Integrated Circuit

SYMBOLS

C	**:** Capacitance
L	**:** Inductance
R	**:** Resistance
F	**:** Farad
H	**:** Henry
Ω	**:** Ohm
†	**:** Paraconjugate
$\boldsymbol{\omega}$	**:** Angular velocity
t	**:** Time
θ	**:** Phase
Z	**:** Impedance
S	**:** Scattering parameter
N	**:** Numerator of polynomials
D	**:** Denominator of polynomials
Γ	**:** Reflection coefficient
dB	**:** Decibel
$\boldsymbol{\tau_d}$	**:** Time delay
l	**:** Length of a transmission line
$\boldsymbol{v_p}$	**:** Group velocity
ρ	**:** Magnitude
δ	**:** Perturbation

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A NOVEL SYMMETRIC LATTICE-BASED WIDEBAND-WIDE PHASE RANGE DIGITAL PHASE SHIFTER DESIGN

SUMMARY

Digital phase shifters are the major building blocks of electronically steered smart antenna array systems. Next generation communication system, 5G requires the control of the direction of the signal radiation which is called beamforming. Beamforming can be done by turning the antenna physically and directing the signal accordingly. However this needs extra precise mechanical components to steer the antenna, which are indeed cost hungry. In modern communication systems, beamforming is accomplished using phased array systems which are utilized to direct the signal digitally via phase shifters. The phase shifters within phased array systems are the key control elements to focus the radiated signal to the desired direction.

In practice, a phase shifter module is placed in the back of each antenna. A phase shifter module consists of cascade connection of phase shifting cells. A phase shifting cell is a lossless, reciprocal, passive two-port constructed with interconnection of reactive immittances. For example, a 3-bit phase shifter module consists of cascade connection of 45^0, 90^0 and 180^0 phase shifting cells. The expression "digital phase shifter" stems from the operation of phase shifting cells. In other words, each phase shifting unit includes perhaps more than one solid-state switches manufactured as PIN diodes or CMOS transistors etc. In one state, say in "State-A", each switch is either ON or OFF. In this switching state, at a specified frequency f_0, the phase shift from the input to the output of the cell under consideration is measured as θ_A. Similarly, in the other switching state, say, in "State-B", one obtains a phase shift of θ_B. Thus, the net phase shift between State-A and State-B is $\Delta\theta = \theta_B - \theta_A$. Each phase shifting cell possesses two-level or binary switching states. It is either one (State-A) or zero (State-B).

Many thousands of phase shifters are placed on a single plate. Therefore, their power consumptions are highly crucial. Many applications, such as software defined radios, radars, electronic warfare systems, point to point or directed communication systems employ "low loss, low power consumption, broadband and wide phase range" passive digital phase shifters. Thus, in this thesis, a novel passive, broadband, wide phase range, compact digital phase shifter topology is introduced.

In the new topology, CMOS transistors are used as switching elements. By properly switching, proposed topology resembles the operation of either "symmetrical LC-all pass" with lagging-phase or "symmetrical LC-all pass" with leading-phase.

Proposed compact topology can provide any phase shift between 0^0- 360^0 by proper selection the passive component values. In this thesis, design details, and practical MMIC implementation issues are covered. Eventually, complete design of 45^0, $90^0$and 180^0 digital phase shifting cells are presented. It is shown that proposed digital phase shifter topology provides wide phase shifting capability over broad frequency band with reasonable loss.

SİMETRİK KAFES YAPILI GENİŞ BANTLI-GENİŞ FAZ ARALIKLI ÖZGÜN SAYISAL FAZ KAYDIRICI TASARIMI

ÖZET

Faz kaydırıcılar, radar uygulamalarında özellikle antene gelen veya antene gönderilecek olan ana sinyalin farklı açısal eşleniklerini oluşturmada kullanılan önemli yapı elemanlarıdır. Yeni nesil iletişim sistemleri, geniş bantlı, geniş faz aralığına sahip ve düşük kayıplı faz kaydırıcı devrelerine olan ihtiyacı arttırmıştır.

Sayısal faz kaydırıcılar yaygın olarak akıllı anten dizimi uygulamalarında, elektronik işlemcilerle veya sürücülerle sağlanan 1 veya 0 durum değerleriyle fazın değerini değiştirme işlevinde kullanılırlar. Pratik olarak, her bir anten elemanının arkasına bir faz kaydırıcı modülü konmaktadır. Her bir faz kaydırıcı modülü ise ardışık dizilmiş faz kaydırıcı ünitelerinden oluşmaktadır. Bu faz kaydırıcı üniteleri, ideal olarak kayıpsız, resiprok, pasif iki kapılı eleman olup, reaktif elemanların birbiri ile bağlanmasından oluşur. Örneğin, üç bit dijital faz kaydırıcı modülü 45^0, 90^0 ve 180^0 faz kaydırıcı ünitlerin ardışık birbiri ile bağlanması şeklinde oluşturulabilir. Buradaki sayısal faz kaydırıcı kavramı, faz kaydırıcı ünitelerin çalışma şekliyle belirlenir. Başka bir deyişle, her bir faz kaydırıcı birimi bir veya birden fazla CMOS transistör veya PIN diyot gibi katı hal anahtarlama eleman teknolojilerinden oluşabilir. Bu elemanların durumlarından birinde, mesela Durum-A, anahtarlama elemanları AÇIK durumda veya KAPALI durumda olabilir. Bu anahtarlama durumunda, belirli bir frekans değeri için, girişten çıkışa olan faz kaydırma miktarı θ_A olarak belirlenir. Benzer olarak, diğer anahtarlama durumunda, mesela Durum-B, girişten çıkışa olan faz kaydırma miktarı θ_B olarak belirlenir. Bu durumda, Durum-A ve Durum-B arasındaki girişten çıkışa net faz farkı miktarı $\Delta\theta = \theta_B - \theta_A$ olarak tanımlanır. Her bir faz kaydırma birimi iki değerli anahtarlama durumundan oluşur, Durum-A ve Durum-B. Durum-A ve Durum-B arasındaki anahtarlama geçişleri, sayısal kontrol ile belirlenir.

Yeni nesil iletişim sistemlerinde anten dizimlerinin fazını ayarlamak için binlerce faz kaydırıcının tek bir modüle girmesi öngörülmektedir. Bu yüzden, faz kaydırıcı devrelerinin güç tüketimi değerinin önemi artmıştır. Yazılım tanımlı telsiz, radar, elektronik harp ve benzeri sistem uygulamalarında, düşük kayıplı, düşük güç tüketimli, geniş faz kaydırma özellikli ve geniş bantlı pasif faz kaydırıcı devrelerine ihtiyaç duyulmaktadır. Bu yüzden, bu çalışmada özgün, pasif, geniş faz kaydırmalı, geniş bantlı sayısal faz kaydırıcı devre tasarımı hedeflenmiştir.

Literatürdeki bazı çalışmalarda T ve Pi LC Ladder yapıları kullanılmıştır. Fakat bu çalışmalarda kullanılan faz kaydırıcı yapıları, her ne kadar düşük faz hatası ve düşük kayıp ile tasarlanmış olsa da, T ve Pi yapılarının faz kaydırma için kullanılması nedeni ile geniş bantta sonuç alınamamıştır.

Bir başka makalede faz kaydırma çiftli bölümler ve üniform iletim hatları kullanılarak yapılmıştır. Bu faz kaydırıcı tasarımının geniş bantlı olabilmesi için çiftli bölümlerin birbiri ile yüksek eşlenikte olması gerekir ki bu da gerçekçi bir uygulama değildir.

Yansıtıcı tipinde faz kaydırıcı devrelerinin de literatürde kullanımı oldukça yaygındır. Bu tasarımların bazılarında, toplu öğeli elemanlar hat kuple devreleri yerine kullanılmıştır. Ancak bu elemanlar, sonuç olarak düşük bant ve yüksek kayıpların olmasına neden olmaktadır.

Literatürde, aktif vektör modülatörlere bağlı faz kaydırıcı devreleri de mevcuttur. Bu topoloji kullanılarak geniş bantlı bir sonuca ulaşılamamıştır.

Ayrıca, monolithic microwave integrated circuit (MMIC) aktif faz kaydırıcılarda değişken rezonant devreleri de kullanılmaktadır. Bu tip aktif faz kaydırıcılar, sadece düşük bant ve yüksek giriş kaybı ile gerçeklenebilmektedir.

Anahtarlama modu yapısı kullanan sayısal faz kaydırıcı devreleri de literatürde yer almaktadır. Bu çalışmalarda mikrostrip hatlar faz kaydırıcı elemanı olarak kullanılmış olup pin diyotlar anahtarlama elemanı olarak kullanılmıştır. Bu yöntem her ne kadar düşük kayıp ve düşük faz hatasına sahipse de, geniş bant gerçeklenmesi için uygun değildir.

Bu çalışmada, geniş bantlı, düşük güç kayıplı, düşük faz hatalı, kompak, sayısal bir tasarım elde etmek için, literatürde ilk kez simetrik tüm geçiren kafes yapıları faz kaydırıcı birimleri olarak kullanılmıştır.

Tüm geçiren simetrik LC kafes yapıları ikiye ayrılırlar, önde faz kaydırıcı yapısı (Tip-1) ve geride faz kaydrıcı (Tip-2) yapısı. Önde faz kaydırcı yapısı kullanıldığında sadece 0^0'den 180^0'ye kadar olan faz kaydırma değerlerine ulaşmak mümkün iken, arkada faz kaydırıcıların kullanılması durumunda, 0^0 'den -180^0'ye kadar olan faz kaydırma sonuçlarını almak mümkündür. Eğer bu iki faz kaydırıcı, aralarında anahtarlama yapılarak birlikte kulllanılırsa 0^0-360^0 'ye kadar olan tüm faz çemberinde faz kaydırma işlemini yapabilir hale getirilebilir.

Her iki faz kaydırıcı birimi, paralel olarak kullanılıp, giriş ve çıkıştaki elektronik anahtarlar ile birbiri arasında anahtarlanarak 0^0-360^0 arasında faz kaydırıcı elde etmek mümkündür. Ancak bu uygulama, biri giriş bölümünde, diğeri çıkışta olmak üzere, iki adet tek giriş, çift çıkış anahtarlama devre elemanı gerektirmektedir. Ayrıca Tip-1 ve Tip-2 faz kaydırıcı devrelerinin ayrı ayrı kullanılması ve bu iki devrenin birbiri ile bağlanması için gerekli bağlantılar hem geniş bir serim alanı kaplamasına hem de bu bağlantı yollarından kaynaklı olmak üzere parazitik endüktans, kapasite ve direnç eklenmesine neden olur. Bu fazladan gelen parazitik elemanlar, devrenin elektriksel performansını çok ciddi şekilde etkilerler. Özellikle, bu parazitik elemanlardan kaynaklı performans düşüklüğü en çok geniş bant gereksinimini etkilemektedir. Bu sebeple, Tip-1 ve Tip-2 yapılarının giriş ve çıkışta anahtarlama ile kullanılma yöntemi yüksek performans ihtiyaçlarını karşılamak için uygun değildir.

Bu sebeple, bu tezde uygulaması hem kolay olan, hem de faz kaydırıcı performansı var olan literatürden daha iyi olan özgün bir sayısal faz kaydırıcı yapısı önerilmiştir.

Özgün ve yüksek performanslı sayısal faz kaydırıcı tasarımı, özgün bir anahtarlama yöntemi kullanılarak gerçekleştirilmiştir. Önerilen faz kaydırıcı yapısı, çip alanını azaltmakta ve parazitik elemanlardan kaynaklı etkileri en aza indirgemektedir. Bunun sonucunda devrenin kaybı azalmakta ve faz kaydırıcının kullanılabildiği frekans genişliği artmaktadır. Bu yeni yöntem geniş faz kaydırma özelliğini geniş bant içerisinde sağlamakta olup, düşük faz hatası ve kazanç kaybı ile yüksek performans elde edilmesini sağlamaktadır. Bu fikrin en temel özelliği, Tip-1 ve Tip-2 yapıdaki simetrik kafes faz kaydırıcı birimlerini tek bir devre altında birleştirmesidir. Bu devre, bu sebeple tez boyunca 'Basit ve Tekil-Simetrik Sayısal Faz Kaydırıcı' (Single and

Single-Symmetrical Digital Phase Shifter ya da SSS-DPS ya da 3S-DPS) olarak adlandırılmıştır.

Önerilen 3S-DPS yapısı, anahtarların AÇIK ve KAPALI konumuna göre ya Tip-1 tüm geçiren simetrik kafes yapısı ya da Tip-2 tüm geçiren simetrik kafes yapısı gibi davranmaktadır.

Önerilen 3S-DPS yapısının her bir kolunda seri bir kondansatör ve bobin bulunur. Bu kondansatör ve bobinin her birinin paralelinde bir NMOS transistör bulunmaktadır. Bu NMOS transistör anahtarlama elemanı olarak kullanılmaktadır. NMOS transistör KAPALI hale getirilerek, paralelindeki bobin veya kondansatör kısa devre yapılabilir. Bu şekilde, simetrik kafes yapısının ilgili kolu sadece bobin olarak (kondansatörün paralel NMOS'u KAPALI iken) veya kondansatör olarak (bobinin paralel NMOS'u KAPALI iken) davranarak Tip-1 veya Tip-2 tüm geçiren simetrik kafes yapıları gibi davranışı, bir yapıyla sağlanmış olmaktadır. Bu tezde, 3S-DPS'nin Tip-1 gibi davrandığı durumuna Durum-1 hali, benzer şekilde, 3S-DPS'nin Tip-2 gibi davrandığı durumuna Durum-2 hali adı verilmiştir.

Bu tezde, yeni bir buluş olan 3S-DPS yapısının tasarım denklemleri ayrıntılı olarak ele alınmıştır. Öncelikle yeni buluşun bütün devre elemanları ideal olarak düşünülmüş ve bu ideal elemanlı yapının devre çözüm denklemleri çıkartılmıştır. Bunun sonrasında ideal devrenin adım adım nasıl tasarlanacağı anlatılmıştır. Bunun üzerine, yapının algoritmik olarak tasarım adımları oluşturulmuş ve tasarım algoritması MATLAB ortamında denenmiştir.

Sonrasında, ikinci aşamada yeni buluşun pratik devre elemanları ile tasarımı yapılmıştr. Bu tasarım için kolay bulunabilirlirliği ve kavram ispatı için yeterli olması nedeniyle TSMC 0.18µm CMOS prosesi kullanılmıştır. Bu ikinci aşamada, ilk olarak yapının devre çözüm denklemleri çıkartılmıştır. Sonrasında, devrenin çıkış fazını belirlemek için 3S-DPS devresinin Durum-1 ve Durum-2 hallerinin istenilen merkez frekansındaki fazlarının nasıl bir dağılımda olduğu, devrenin performansını ciddi bir şekilde etkilediği gözlemlenmiştir. Bu dağılım genel olarak üç durumda incelenmiştir. Birincisi merkez frekansta Durum-1 ve Durum-2 fazlarının eşit olma durumudur. İkincisi merkez frekansta Durum-1 ve Durum-2'nin fazlarının eşit olmama ve aynı zamanda Durum-2 fazının pozitif olma durumudur. Üçüncüsü ise, merkez frekansta Durum-1 ve Durum-2'nin fazlarının eşit olmama ve negatif olma durumudur. Bu üç durum da ayrıntılı olarak incelenmiştir.

Pratik devre tasarım denklemleri ve algoritmaların kavram ispatı, 3 bit faz kaydırıcı blokları olan 45^0, 90^0 ve 180^0 faz kaydırıcı devrelerini tasarlamakta kullanılmıştır. Öncelikle, devreye ait denklemlerin çıkarılmasından sonra oluşturulan algoritma MATLAB ortamında denenmiştir. İlk olarak 45^0 faz kaydırıcı tasarımlarının sonuçları karşılaştırılmıştır. Merkez frekansta Durum-1 ve Durum-2 fazlarının eşit olma durumunu kullanan algoritma en düşük frekans bandında çalışmakta olup, merkez frekansta Durum-1 ve Durum-2'nin fazlarının eşit olmamakla beraber her ikisinin de negatif olma durumu en geniş frekans bandında çalıştığı gözlemlenmiştir.

Kavram ispatını silikon üzerinde göstermek için, Cadence ortamında TSMC 0.18µm CMOS proses PDK kütüphanesi kullanılarak şematik tasarımı ve benzetimi yapılmıştır. Şematik benzetim sonuçlarında, algoritmik olarak MATLAB ortamında alınan sonuçlara oldukça yakın sonuçlar elde edilmiştir. Bu deney sonucunda, hem önerilen devrenin üstün performansta çalıştığı gösterilmiş, hem de yeni buluşun teorik açıklaması ve bunun üzerine oluşturulan algoritmanın doğruluğu ispatlanmıştır.

Yazılan algoritma, ilgili tasarımcının hızlı bir şekilde tasarlamak istediği devrenin eleman değerlerini bulmasına olanak sağlamaktadır.

TSMC 0.18µm CMOS prosesinde tasarlanan şematik sonrasında proses ve Monte-Carlo analizleri yapılarak performansın ne kadar değiştiği gözlemlenmiştir. Devre, prosesten ve uyumsuzluktan etkilenmeyecek şekilde tasarlandığı için, sonuçlarda nominal değerlerden çok az sapma oluşmuştur.

Yüksek frekans devrelerinde devre eleman tasarımı kadar, devrenin serimi önemlidir. Yüksek frekanslı uygulamalarda, devre seriminden kaynaklı parazitikler ve yollar arasndaki kuplajlar elektriksel performansı çok etkilemektedir. Bu sebeple, devrenin serimi çizilmiş ve çizilen serimin 3D EM analizi yapılmıştır. Devrenin serimi, yüksek frekans önceliklerine uyularak yapıldığı için, ciddi bir performans kaybı olmamıştır.

Alınan sonuçları diğer son teknoloji tasarımlarla kıyasladığımızda, önerilen devrenin, benzer faz hatası oranında diğerlerinden çok daha geniş frekans bandında çalıştığı kavramsal olarak ispat edilmiştir.

Sonuç olarak, bu tez çalışmasında, önerilen devrenin, hem teorik, hem de pratik olarak kavramsal ispatı gerçekleştirilmiştir. 'Basit ve Tekil-Simetrik Sayısal Faz Kaydırıcı' devrenin, geniş bantta düşük faz ve düşük kazanç kaybı ile gerçeklemesini sağlayarak, yeni nesil iletişim sistemlerinde kullanılabilecek önemli bir yapı elemanı olduğu kavramsal olarak ispatlanmıştır.

1. INTRODUCTION

1.1 Phase Shifters for Modern Communication Systems

Phase shifters are the key elements in modern communication and radar applications. Next generation communication system, 5G requires the control of the direction of the signal radiation which is called beamforming. Beamforming can be done by turning the antenna physically and directing the signal accordingly. However, this needs extra precise mechanical components to steer the antenna, which are indeed cost hungry. In modern communication systems, beamforming is accomplished using phased array systems which are utilized to direct the signal digitally via phase shifters. The phase shifters within phased array systems are the key control elements to focus the radiated signal to the desired direction. The transmitter chain example for an phased array system is given in Fig. 1.1.

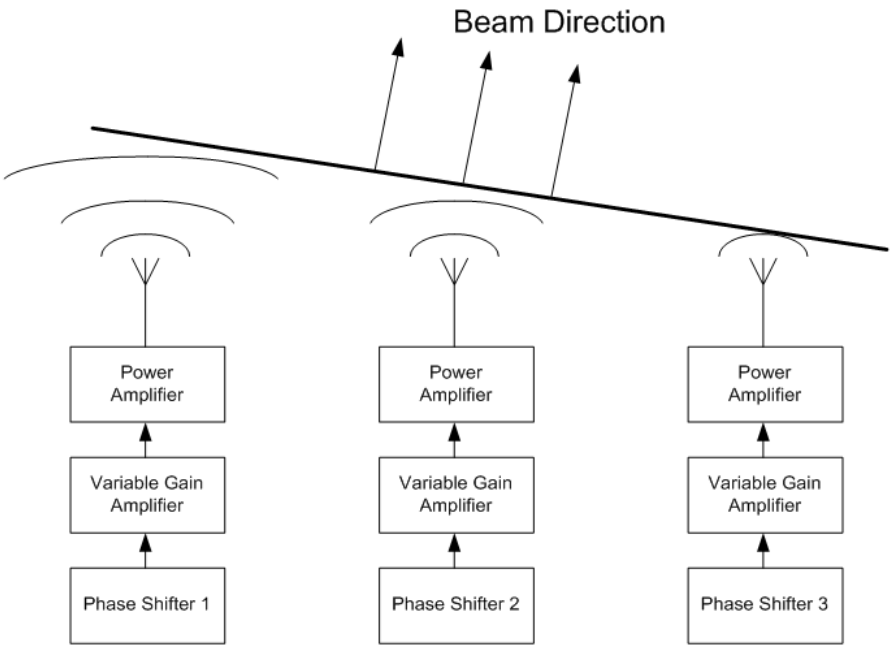


Figure 1.1 : Phase shifter at transmitter chain of phased array system.

In Fig. 1.1, the main beam directed in a particular direction is defined by the phase of each signal radiated from the antenna array system. The phase of the signal is defined

by the phase shifter block. Then, the signal is amplified by the power amplifier and radiated through the antenna with a proper power and direction.

The receiver chain of the phase array systems is given in Fig. 1.2.

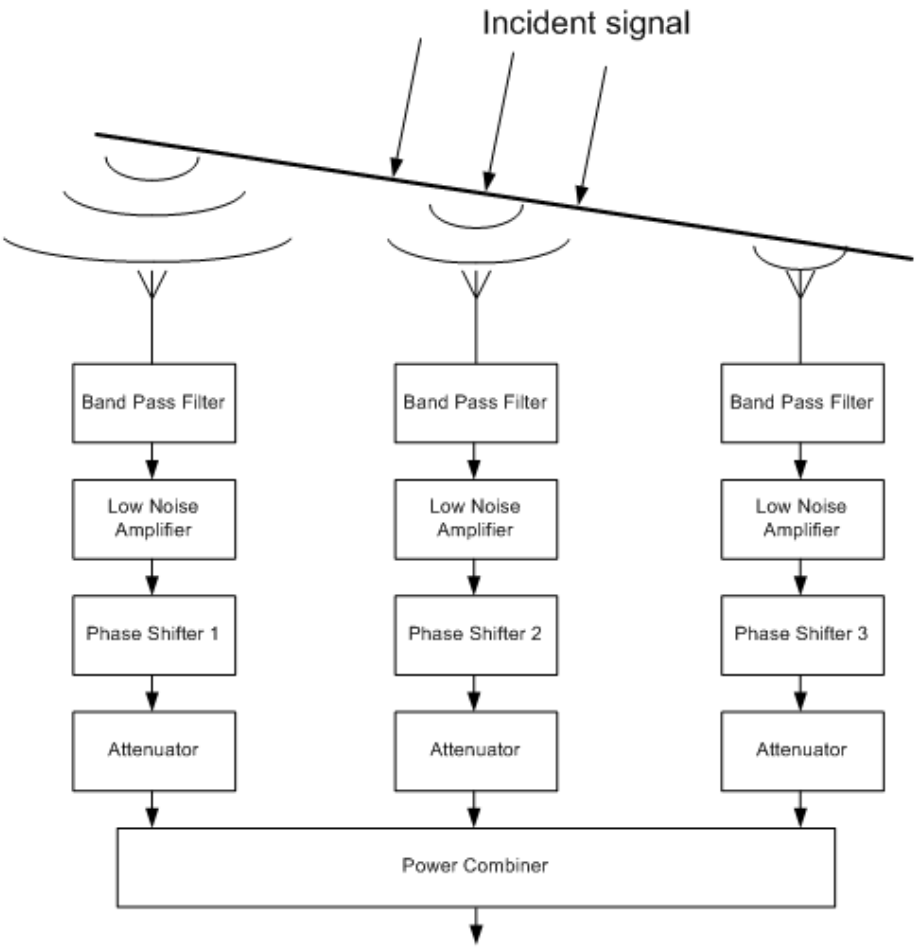


Figure 1.2 : Phase shifter at receiver chain of phased array system.

As given in Fig. 1.2, the phase shifter is also one of the key elements in the receiver architecture. The receiver consists of band pass filter, low noise amplifier, phase shifter, and power combiner. The signal is received from each antenna element and then the signal is bandpass filtered. The filtered signal is then amplified by using low noise amplifier. The phase shifter is used to compensate the phase variations occurring between each antenna element. Then, the signal can either pass through a variable gain amplifier or attenuator to compensate the amplitude variation between each antenna element. The resultant signals coming from each antenna element signal chain are then combined by the power combiner.

Considering the phased array systems, a phase shifter block is needed both in transmitter and receiver. For this reason, it is crucial to design a compact and low power phase shifter.

1.2 Literature Survey and Trends in Phase Shifters

In the literature, there are different approaches on phase shifter implementation. These approaches mainly optimize the bandwidth, phase range, insertion loss, phase resolution, linearity, area and power consumption. Owing to the growth of the wireless communication industry together with new communication standards such as 5G, the wideband operation together with low power consumption of phase shifters within these multiple antenna transceiver systems become crucial.

In the early classical digital phase shifter literature, P-I-N diodes are used as switching elements to switch from low pass to high pass based, filter like, $LC-T\ or\ \pi$ network topologies [1-8]. These implementations cannot give good result for low cost standard process due to their diode performance. Also, despite the fact that these circuits provide improved phase shifting performance, they still suffer from narrow bandwidth operation. This fact is the result of the design concept which is based on the phase shifting properties of three element low pass and high pass LC ladders.

One of the broadband phase shifter concepts given in the literature is shown by B. M. Shiffmann in early 1950s [9]. Based on Shiffmann phase shifter, coupled transmission line and uniform transmission line sections are used to generate broadband differential phase shifter. Shiffmann has suggested that by careful selection of the lengths of the coupled and uniform sections, a constant phase shift can be achieved over wide frequency band. However, broadband operation of Shiffman phase shifter mainly depends on the performance of the coupled sections. In order to achieve wide frequency range, the coupled sections should be tightly coupled, unfortunately, which is not practical in todays technology nodes.

In the modified Schiffman phase shifter [10-11], different configurations of coupled lines or parallel connected coupled lines are exhibited which are used with a uniform transmission line, other coupled lines, or parallel connected coupled lines, to obtain a differential phase shifter. The papers claim that even with loose coupled lines, the same performance of original Schiffman phase shifter can be achieved. However, there is

still a coupling issue in these structures and it is difficult to obtain a phase shift more than 90^0 due to a limited coupling ratio realizable in a coupled line.

Another type of loaded line phase shifters are stub loaded phase shifters[12-19]. Stub line loading of transmission lines is a well-known technique for building simple low insertion loss phase shifters for many circuit applications, such as switchable diode phase shifters realized in microstrip or high-power coaxial line configurations. However this type of phase shifters is only suitable for small phase shifts and the bandwidth of only around 10% can be achieved due to the frequency behaviour of stub loads.

A reflective type phase shifter topology is presented where phase control range of 210° and 360° are achieved at the C-band [20]. In the implementation, lumped elements are used instead of branch line coupler, however, this replacement comes with low frequency band and high losses. A vector modulator-based phase shifter is presented in [21]. This phase shifter topology also cannot offer wide frequency band and wide phase range.

In the literature of reflective type phase shifters, using the varactor diode as the reflective load element is first published in [22]. However, using varactor diode as the reflective load element limits the achievable phase shift range. For this reason, further developments on maximizing the relative phase-shift range are done. In order to maintain whole phase shift range of 0^0-360^0, special arrangements of multiple varactors with quarter-wavelength transmission lines were proposed in [23-28]. Realizing the extension of phase shift range trades off with dramatic insertion loss variation, which comes from the parasitic resistance of the varactor diode. The same root cause of the severe insertion loss variation also limits the bandwidth 10% around the center frequency.

Switched line phase shifting technique is one of the simplest and most direct techniques to generate the desired phase shift [29-33]. Switched line phase shifters use the time delay difference between two direct paths and by switching in between, the net phase difference between two paths defines the desired phase shift. The switched line phase shifters are also suitable for digital phase shifting. However, for switched line phase shifters, the implementation of large phase shift values is not practical since this type of phase shifters uses phase difference between two transmission lines in two

different paths to generate the phase shift. Also, the mismatch between the two transmission lines generates phase error which may not be acceptable for many applications.

In a typical LC lumped-elements phase shifter, phase shift between the switching states are accomplished by means of single pole double throw (SPDT) and/or double pole double throw (DPDT) switches as described by [34]. In this type of phase shifters, the above mentioned switches introduce undesirable parasitic elements, which in turn results in reduction of bandwidth with increased loss and chip area. The maximum achievable bandwidth is 15% around the center frequency.

Vector sum phase shifting method is one of the well-known design technique used within active phase shifters [35-38]. This method is based on the principle of the vector sum of phase separated variable vectors to achieve a phase change. Variable phase shifts and gains are obtained by adjusting the relative amplitudes of the vectors. A vector sum active phase shifter with small chip size is reported in [38]. It offers small chip size ($0.3\ mm^2$), high power dissipation (28mW DC) with ± 10 % frequency band at 5 GHz.

Another type of phase shifter is varactor loaded active phase shifter [39-43]. The varactor loaded phase shifters can maintain any number of phase states, by which it is possible that the applicable range of the analog phase shifter is wider than digital phase shifter. However, these structures are mainly area and power hungry. A Microwave Monolithic Integrated Circuit (MMIC) active phase shifter topology that utilizes tunable resonant circuit is reported in [43]. This circuit can only achieve narrow band (2.38-2.42 GHz) with $2\ dB$ insertion loss by consuming more than $90\ mW$ power, which is not suitable for the next generation wireless communication systems.

A 60 GHz true time delay phase shifter constructed with transmission lines, tunable varactors and inductors is reported in [44-45]. Transmission line phase shifters offer narrow phase range capability due to the limited varactor capacitance tuning. Furthermore, it is difficult to have a good matching within the tuning range of the capacitance. Thus, [45] focuses on enhancing the phase shift range while improving the input/output matching of the transmission line phase shifter. However, these phase shifters are not good candidates for designing wideband and phase range due to narrow

bandwidth capability of transmission lines. The reported bandwidth of [45] is $\pm 5.8\%$ around the center frequency.

1.3 Thesis Organization

In this thesis, firstly, phase shifter fundamentals are presented (section 2). In this section, phase shifter performance parameters and phase shifter topologies are introduced. In section 3, properties of generic symmetrical LC lattice structures and their phase shifting properties are investigated. Section 4 is devoted to the proposed "Simple and Single Symmetrical Digital Phase Shifter" topology. In short, this architecture is referred as "SSS-DPS or equivalently 3S-DPS". In section 4, the explicit equations are also investigated both for proposed architecture with ideal components and practical components. In Section 5, we introduce the design algorithms of 3S-DPS topology. The practical MMIC implementation of 3S-DPS topology is given in section 6. Also step-by-step design implementation examples are covered. In the last part of section 6, the comparison with the state-of-art literature is given.

2. PHASE SHIFTER FUNDAMENTALS

2.1 Phase Shifter Performance Parameters

Phase Shift Error

Phase shift error (or phase error) is the main performance parameter of a phase shifter. Phase error is the phase deviation amount from the ideal desired phase shift value. Generally the transmitter/receiver system requirements set the maximum phase shift error of phase shifter over the frequency band of interest. For the multibit phase shifters, the phase shift error performance is evaluated using root mean square (RMS) phase error. The RMS phase error is defined as,

$$RMS\ Phase\ Error(f) = \sqrt{\frac{\sum_{i=1}^{N}\left|\theta_{i,error}(f)\right|^2}{N}} \tag{2.1}$$

where,

$\theta(f)_{i,error}$ is the phase shift error of the bit-state i as a function of frequency.

N is the total number of phase bit-states.

Gain/Insertion Loss Error

The insertion loss defines the amount of loss from its input to output terminals. Insertion loss should be analyzed over the frequency band of interest. For multibit systems, it is also critical to consider the insertion loss with the variation of the selected phase shift. The insertion loss variance is desired to be low between different phase shift selection states in multi-bit phase shifters. For multi-bit phase shifter designs, besides the absolute value of the gain loss, RMS gain error is also a parameter that highlights the gain variance over frequency. The RMS gain error is defined as,

$$RMS\ Gain\ Error(f) = \sqrt{\frac{\sum_{i=1}^{N}\left|A_i(f) - A_{reference}\right|^2}{N}} \tag{2.2}$$

where,

$A_i(f)$ is the insertion loss of the bit-state i as a function of frequency, and $A_{reference}$ is the insertion loss in the reference state over frequency.

N is the total number of phase bit-states.

In this thesis, maximum loss over bandwidth is given for analyzing the implemented phase shifters.

Size

As given in Section 1, for next generation communication systems, such as 5G phased array system, phase shifters are used at each antenna unit both in receiver and transmitter side. Reducing size of the phase shifter both improves the connectivity between the phase shifter and other components and reduces the cost of the system drastically.

Power Consumption

Because phase shifters are used extensively both in transmitter and receiver chains of phased array systems, their power consumption should be as low as possible. Passive circuits do not consume static power by nature, so it is beneficial to consider the system with passive implementation if possible within next generation transmitter systems.

Input/Output Return Loss

Input and output return loss are measure of the power reflected by the circuit caused by an imperfect match. In many applications, 50 ohm is used as the nominal reference impedance of the system and input/output impedance of the phase shifter need to be close to 50 ohm in order to have minimum reflection at both input and output terminals. The return loss over the frequency band of interest is also important and needs to be constant for many applications.

Linearity - P1dB

P1dB is 1-dB compression point of the gain, which is defined as the input signal level that results a 1dB reduction in the ideal value of the gain, which is shown in Fig. 2.1.

P1dB is a measure of maximum input power that can be supplied to the input port of the circuit. If the input power is increased further, there comes a point where the circuit saturates and output power will not increase.

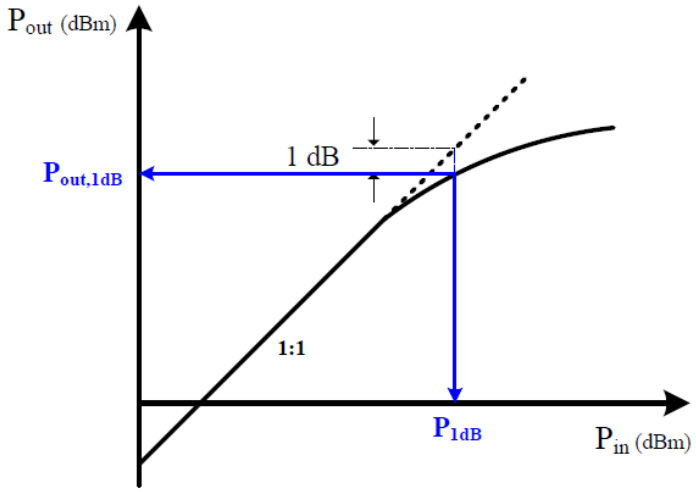


Figure 2.1 : Definition of 1 dB compression point.

Linearity – IP3

Third order intercept point is a measure of the intermodulation performance of a nonlinear system. IP3 is measured applying two-tone test and measuring the ratio between third order intermodulation (IM) products to the amplitude of the fundamental frequency component. The two-tone test is visualized in Fig. 2.2.

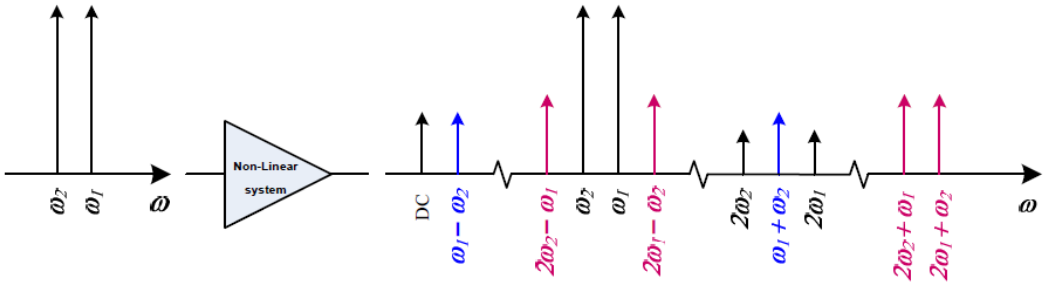


Figure 2.2 : Intermodulation products in a two-tone test.

When increasing the input power, third order IM products increase more than the fundamental component and third order IM products become equal to the amplitude fundamental component. This point is called third order intercept point, IP3. The input third order intercept point (IIP3) and output third order intercept point (OIP3) graphical representation is given in Fig. 2.3.

Switching Time

Switching time is the measure of time that is needed to be consumed to reach steady state after switching between states of the phase shifter.

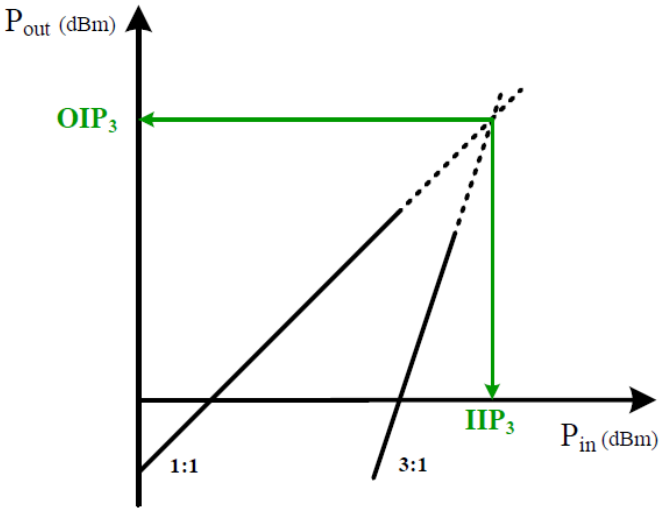


Figure 2.3 : Definition of third order intercept point.

2.2 Phase Shifter Topologies

2.2.1 Reflection type phase shifters

The reflection type phase shifter is one of the main phase shifter topologies in literature [22-28]. The general concept is illustrated in Fig. 2.4.

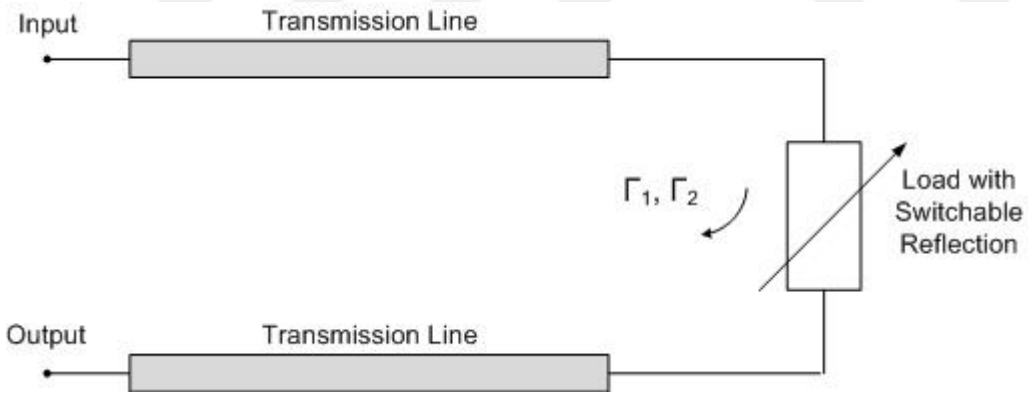


Figure 2.4 : Reflection type phase shifter topology.

As given in Fig. 2.4, a switchable reflection load is used in order to generate a phase shift between the switching states. Assuming the reflection coefficient phase of switching states as θ_1(with the reflection coefficient Γ_1 for switching state 1) and θ_2 (with the reflection coefficient Γ_2 for switching state 2), the phase shift of the reflected signal between these states becomes $\Delta\theta = \theta_2 - \theta_1$.

One of the main implementation of the reflection type phase shifter is hybrid coupled phase shifters as shown in Fig. 2.5.

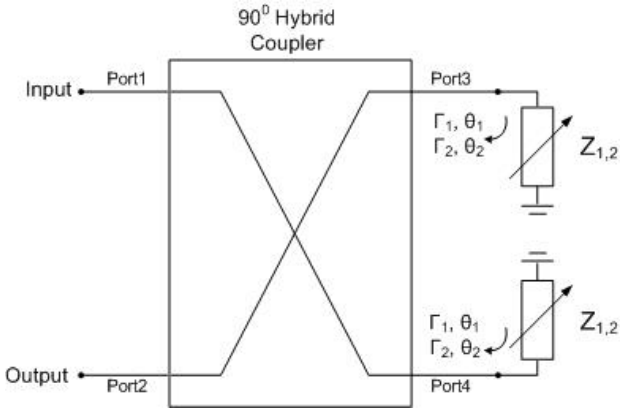


Figure 2.5 : Reflection type phase shifter with 90^0 hybrid couplers.

Hybrid coupled reflection type phase shifters can achieve low insertion loss and flat phase response with employing 90^0 coupler with 3 dB power split and good match. In the Fig. 2.5, port 1 is input and a signal of unity magnitude is given to input. The reflecting switch impedances are at the port 3 and 4 of the coupler. The port 2 of the coupler is the output of the phase shifter. As shown in Fig. 2.5, the transmitted signals from port1 to port 3 and 4 are $\frac{1}{\sqrt{2}}\angle 0$ and $\frac{1}{\sqrt{2}}\angle -90$, respectively. The reflected signal from port 3 and port 4 are $\Gamma\frac{1}{\sqrt{2}}\angle 0$ and $\Gamma\frac{1}{\sqrt{2}}\angle -90$. The reflected signals pass through the coupler and at port 1 their sum is;

$$\Gamma\frac{1}{\sqrt{2}}\angle -180 + \Gamma\frac{1}{\sqrt{2}}\angle 0 = -\Gamma\frac{1}{\sqrt{2}}\angle 0 + \Gamma\frac{1}{\sqrt{2}}\angle 0 = 0 \tag{2.3}$$

That means, the reflected signals cancel each other at input, port 1. The reflected signals pass through the coupler and at port 2 their sum is;

$$S_{21} = \Gamma\frac{1}{\sqrt{2}}\angle -90 + \Gamma\frac{1}{\sqrt{2}}\angle -90 = \Gamma\angle -90 \tag{2.4}$$

By switching the load, the reflection from port 3 and 4 changes to $\Gamma\angle\theta$ and the signal at output port now becomes $\Gamma\angle(-90+\theta)$. The phase between the two switching states is θ, which is set by the load reflection coefficient phase.

Advantages of reflection type phase shifters are their good return loss characteristics. Also reflection type phase shifters can realize variable delay. However, matching of the loads of port 3 and port 4 is crucial in order not to generate amplitude imbalance, which makes this type of phase shifters hard to implement. Also, since transmission lines are used as loads, it is very hard to implement large phase shift values.

2.2.2 Loaded line phase shifters

Loaded line phase shifters are used extensively in the literature [12-19]. Loaded line phase shifters are composed of two admittances separated by a transmission line generally having a quarter wavelength as shown in Fig. 2.6. Each admittance can be either inductance or capacitance.

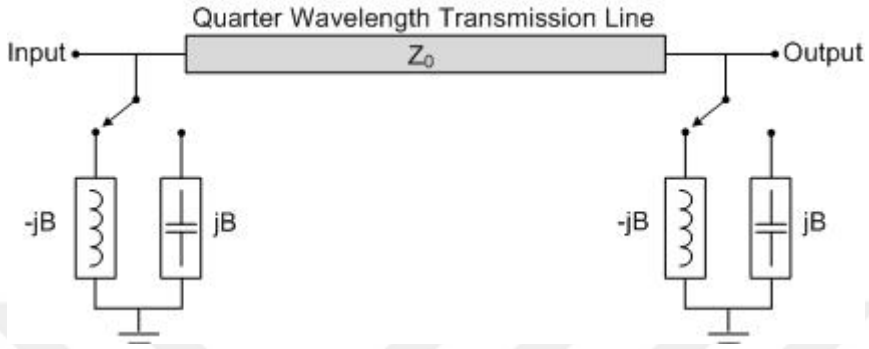


Figure 2.6 : Loaded line phase shifter topology.

For this topology the phase shift amount can be derived as

$$\Delta\theta = 2tan^{-1}\left(\frac{1}{BZ_0} - \frac{BZ_0}{2}\right) \tag{2.5}$$

One of the advantages of the loaded line phase shifters is their compatibility for digital implementation. Also for small phase shift (<45^0) implementation, these phase shifters can achieve wideband operation, however for large phase shift operation, it can only achieve narrow frequency band. Moreover, in this topology, it is hard to implement good input matching, which is also highly dependent on the phase shift value.

2.2.3 Switched line phase shifters

This type of phase shifters are also named as true time delay phase shifters [29-33]. Switched line phase shifters are composed of transmission lines which are switched between each other both at the input and output ends of the phase shifter, as shown in Fig. 2.7.

The time delay of a transmission line having a length of l_1 is

$$\tau_{d1} = \frac{2\pi l_1}{v_p} \tag{2.6}$$

where v_p is group velocity of the signal.

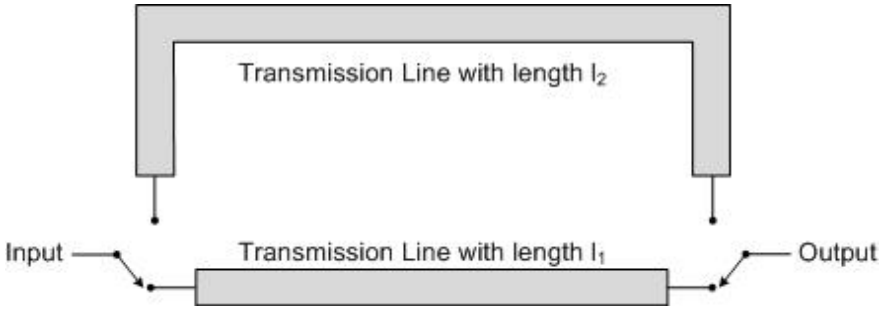


Figure 2.7 : Switched line phase shifter topology.

Similarly, the time delay of l_2 at another switch state is

$$\tau_{d2} = \frac{2\pi l_2}{v_p} \tag{2.7}$$

The true time delay between two phase switching state can be found easily by

$$\Delta\tau_d = \frac{2\pi(l_2 - l_1)}{v_p} \tag{2.8}$$

However, given in (2.8), as the phase shift/time delay value is increased, the length of the transmission line should also be increased, which indeed increases the loss of the system. Also, by getting the phase shift from two unequal length transmission lines will have different loss from input to output, which creates amplitude imbalance.

2.2.4 LC ladder based phase shifters

The LC ladder phase shifters types are composed of low pass and high pass π and T sections [1-8]. These circuits offer compact implementation solution suitable for monolithic implementation. The design of low pass/high pass π and T structures can be designed at a given frequency f_0 such that the 3-element phase shifter achieves zero insertion loss.

The four types of LC ladder topologies are given in Fig. 2.8.

First of all, high pass T section LC ladder topology is analyzed. The S_{21} insertion loss of this topology is given.

$$S_{21} = \frac{2LC^2s^3}{2LC^2s^3 + (2LC + C^2)s^2 + 2Cs + 1} \tag{2.9}$$

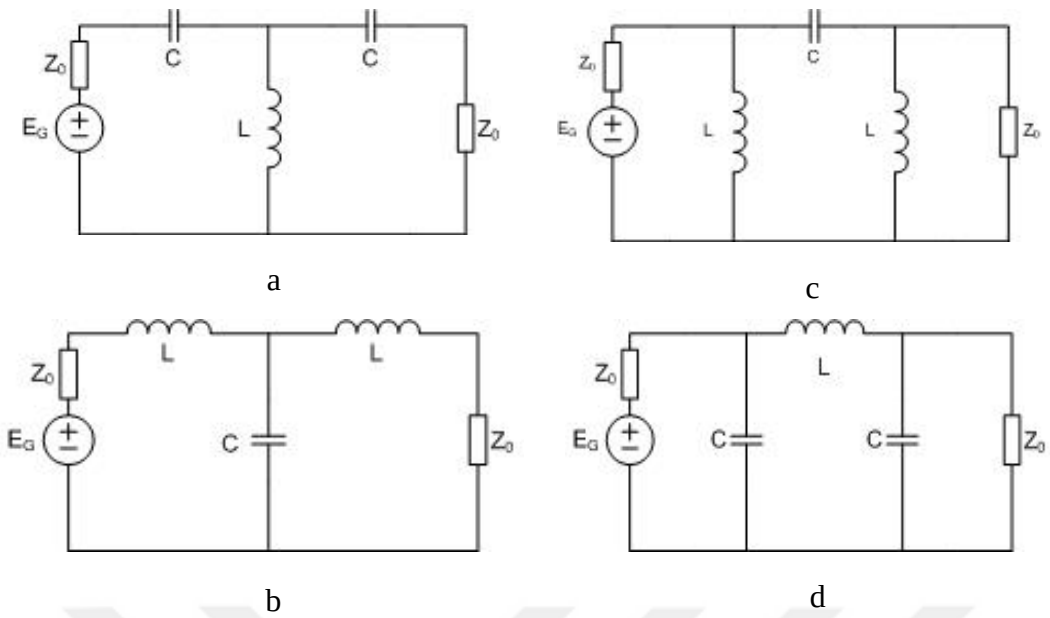


Figure 2.8 : LC Ladder Structures : a) High Pass T topology b) Low Pass T topology c) High Pass $\boldsymbol{\pi}$ topology d) Low Pass $\boldsymbol{\pi}$ topology.

and defining S_{21} as

$$S_{21} = \rho_{21} e^{j\theta_{21}} \tag{2.10}$$

The magnitude and phase components can be found as

$$\rho_{21}^2 = \frac{4L^2C^4\omega^6}{(2C\omega - 2LC^2\omega^3)^2 + [1-(2LC+C^2)\omega^2]^2} \tag{2.11}$$

and

$$\theta_{21} = \frac{\pi}{2} - tan^{-1}\left(\frac{2C\omega - 2LC^2\omega^3}{1-(2LC+C^2)\omega^2}\right) \tag{2.12}$$

In order to have zero insertion loss for the desired phase shift at the center frequency of f_0, we need to satisfy,ω_0

$$\omega_0^2 = \frac{1}{2LC - C^2} \tag{2.13}$$

We can introduce a phase shift dependent parameter

$$\eta = \tan\left[\frac{\pi}{2} - \phi_{21}(\omega_0)\right] = \tan\left(\frac{\pi}{2} - \phi_s\right) \tag{2.14}$$

Rearranging the equation by using the equation (2.12) to define θ_{21},

$$\eta = \frac{2C\omega_0 - 2LC^2{\omega_0}^3}{1 - (2LC + C^2)\omega_0} \tag{2.15}$$

Solving the equations for the desired zero insertion loss condition at normalized center frequency of $\omega_0 = 1$, the component value C can be found as:

$$C = \eta + \sqrt{\eta^2 + 1} \tag{2.16}$$

From 2.15 and 2.16, we can compute L as

$$L = \frac{1 + C^2}{2C} \tag{2.17}$$

The component values depending on the phase shift and normalized center frequency of the desired bandwidt are computed for high pass T configuration. The zero loss design approach can also be implemented for high pass π, low pass T and low pass π sections. The resultant element values regarding zero loss condition at center frequency for a given desired phase shift are given in Table 2.1.

Table 2.1 : LC ladder based phase shifters element values.

High Pass T	Low Pass T	High Pass π	Low Pass π
$C = \eta + \sqrt{\eta^2 + 1}$	$C = \frac{\frac{2}{L}}{1 + (\frac{1}{L})^2}$	$C = \frac{1}{\eta + \sqrt{\eta^2 + 1}}$	$C = \frac{1}{\eta + \sqrt{\eta^2 + 1}}$
$L = \frac{1 + C^2}{2C}$	$L = \frac{1}{\eta + \sqrt{\eta^2 + 1}}$	$L = \eta + \sqrt{\eta^2 + 1}$	$L = \frac{\frac{2}{C}}{1 + (\frac{1}{C})^2}$

The phase response of this topology, as given in (2.12) is inversely proportional to the input frequency. For this reason, it is not feasible to implement wideband phase shifter using these structures.

3. SYMMETRICAL LC LATTICE STRUCTURES

In this section, we present the properties of symmetrical LC lattice ladder structures. In the following, symmetric lattice based phase shifting analysis is covered.

3.1 Properties of Lossless Symmetrical Latice Structures

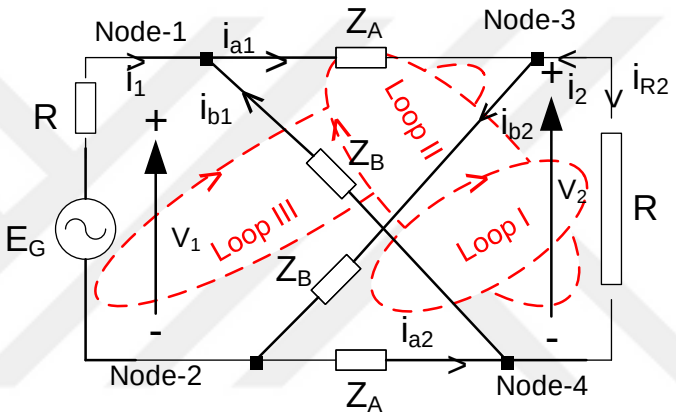


Figure 3.1 : General lattice structure.

In Fig. 3.1, a typical symmetrical lattice section, which can be utilized as the building blocks of broadband digital phase shifters, is shown. The actual impedance Z_A is called the series arm impedance. Similarly, the actual impedance Z_B is referred as the cross-arm impedance. Ideally, phase shifter circuits are lossless two-ports. Therefore, impedances Z_A and Z_B are Foster functions.

The symmetrical lattice structure is derived by an independent voltage source E_G with an internal resistor R.

In practice, at RF and microwave frequencies, a two-port, such as a lossless lattice, is described in terms of its real normalized scattering parameters. For the case under consideration, port normalization is selected as the terminating resistors R. The scattering parameters of symmetrical lattice structure can be found by loop and node analyses using the Fig. 3.1.

For the sake of simplicity, we will use normalized impedance for KCL and KVL analysis. The normalized values of the components given in Fig. 3.1 are shown.

$$z_a = \frac{Z_a}{R} \tag{3.1}$$

$$z_b = \frac{Z_b}{R} \tag{3.2}$$

$$r = \frac{R}{R} = 1 \tag{3.3}$$

Using the normalized impedances, the scattering parameters S_{21} and S_{11} can be calculated as

$$S_{21} = \frac{2i_{R2}}{v_1 + i_1} \tag{3.4}$$

$$S_{11} = \frac{v_1 - i_1}{v_1 + i_1} \tag{3.5}$$

First let us write the KCL node analysis for the given nodes, node 1, node 2, node 3 and node 4.

$$i_{a1} = i_1 + i_{b1} \tag{3.6}$$

$$i_{b2} = i_{a2} + i_1 \tag{3.7}$$

$$i_{a1} = i_{R2} + i_{b2} \tag{3.8}$$

$$i_{b1} = i_{R2} + i_{a2} \tag{3.9}$$

Also KVL loop analysis can be written considering loop 1, loop 2 and loop 3.

$$v_{34} + v_{42} + v_{23} = 0 \tag{3.10}$$

$$v_{34} + v_{42} + v_{23} = 0 \tag{3.11}$$

$$v_{34} + v_{42} + v_{23} = 0 \tag{3.12}$$

We can rewrite the equation by adding impedances and branch currents,

$$r.i_{r2} - z_a.i_{a2} - z_b.i_{b2} = 0 \tag{3.13}$$

$$z_b.i_{b1} + r.i_{r2} + z_a.i_{a1} = 0 \tag{3.14}$$

$$-v_1 + z_a.i_{a1} + z_b.i_{b2} = 0 \tag{3.15}$$

By using the equation , we can rewrite the equations as,

$$i_{r2} = z_a.i_{a2} + z_b.i_{b2} \tag{3.16}$$

$$i_{r2} = -z_b.i_{b1} - z_a.i_{a1} \tag{3.17}$$

Combining these equations, we can generate

$$z_a.(i_{a1} + i_{a2}) + z_b.(i_{b1} + i_{b2}) = 0 \tag{3.18}$$

Using the equations, we can conclude that the series branch currents are equal to each other with opposite polarity. Similarly, cross branch currents are also equal to each other with opposite polarity.

$$i_{a1} = -i_{a2} \tag{3.19}$$

$$i_{b1} = -i_{b2} \tag{3.20}$$

We can rewrite the equation as

$$v_1 = z_a.i_1 + (z_a - z_b).i_{b1} \tag{3.21}$$

Also, we can generate

$$i_{b1}.(z_a + z_b + 2) + i_1.(z_a + 1) = 0 \tag{3.22}$$

Combining these equations, we can write v_1 in terms of i_1.

$$v_1 = i_1.\frac{z_a + z_b + 2z_a z_b}{z_a + z_b + 2} \tag{3.23}$$

Also, we can write i_{R2} in terms of i_1.

$$i_{R2} = i_1 . \frac{z_b - z_a}{z_a + z_b + 2} \tag{3.24}$$

Finally, we can generate S_{21}, S_{12}, S_{11} and S_{22}.

$$S_{21} = S_{12} = \frac{z_b - z_a}{z_a + z_b + z_a z_b + 1} \tag{3.25}$$

$$S_{11} = S_{22} = \frac{z_a z_b - 1}{z_a + z_b + z_a z_b + 1} \tag{3.26}$$

We can write scattering parameters using actual impedances, instead of normalized impedances as follows.

$$S_{21} = S_{12} = \frac{(Z_b - Z_a)R}{(Z_a + Z_b)R + Z_a Z_b + R^2} \tag{3.27}$$

$$S_{11} = S_{22} = \frac{Z_a Z_b - R^2}{(Z_a + Z_b)R + Z_a Z_b + R^2} \tag{3.28}$$

Over the entire actual frequencies ($p = j\omega_a$), it is interesting to note that, from input to output, perfect signal transmission requires

$$S_{11}(jw_a) = S_{22}(jw_a) = 0 \tag{3.29}$$

where $\omega_a = 2\pi f_a$ is the actual angular frequency with f_a being the actual frequency itself.

The above condition yields that

$$Z_a(p) Z_b(p) = R^2 \tag{3.30}$$

Let the normalized impedances are defined as

$$z_a(p) = \frac{Z_a(p)}{R} = \frac{N_a(p)}{D_a(p)} = O_a(p) \tag{3.31}$$

$$z_b(p) = \frac{Z_b(p)}{R} = \frac{N_b(p)}{D_b(p)} = O_b(p) \tag{3.32}$$

where the letters N and D designate the numerator and denominator polynomials in complex variable $p = \sigma + j\omega$ of $z_a(p)$ and $z_b(p)$ respectively. Notice that, $O_a(p)$ and $O_b(p)$ must be odd functions since $z_a(p)$ and $z_b(p)$ are Foster functions. In this regard, it is immediately concluded that

$$z_a^{\dagger} = z_a(-p) = O_a(-p) = -O_a(p) = -z_a(p) \tag{3.33}$$

$$z_b^{\dagger} = z_b(-p) = O_b(-p) = -O_b(p) = -z_b(p) \tag{3.34}$$

where the sign "†" designates the para-conjugate of the complex variable p. Then, perfect transmission condition yields that

$$\left[\frac{N_a(p)}{D_a(p)}\right]\left[\frac{N_b(p)}{D_b(p)}\right] = 1 \tag{3.35}$$

or normalized algebraic form of $z_a(p)$ and $y_b(p) = \frac{1}{z_b(p)}$ must satisfy the following equations.

$$z_a(p)z_b(p) = 1 \tag{3.36}$$

$$z_a(p) = \frac{1}{z_b(p)} = y_b(p) \tag{3.37}$$

Referring to Fig. 3.1, let us recapitulate the properties of a lossless symmetrical lattice two-port [N].

Ideally, a lossless symmetrical lattice two-port [N] must possess Foster impedances $Z_A(p)$ and $Z_B(p)$ at the series and cross arms respectively.

Two-port [N] must possess a real normalized, bounded-real para unitary scattering matrix $S(p) = \begin{bmatrix} S_{11}(p) & S_{12}(p) \\ S_{21}(p) & S_{22}(p) \end{bmatrix} = \begin{bmatrix} S_{11}(p) & S_{21}(p) \\ S_{21}(p) & S_{11}(p) \end{bmatrix}$ is described such that

$$S(p)S^T(-p) = S(p)S^{\dagger}(p) \tag{3.38}$$

$$S(p)S^{\dagger}(p) = \begin{bmatrix} S_{11}(p) & S_{12}(p) \\ S_{21}(p) & S_{22}(p) \end{bmatrix}\begin{bmatrix} S_{11}(-p) & S_{21}(-p) \\ S_{12}(-p) & S_{22}(-p) \end{bmatrix} = I \tag{3.39}$$

The sign "†" designates the para conjugate-transpose of a matrix; the letter "*I*" refers to identity matrix. For the case under consideration, termination resistors *R* are selected as the port normalization number for $S(p)$.

Open form of (3.39) yields that

$$S_{11}(p)S_{11}(-p) + S_{21}(p)S_{21}(-p) = 1 \tag{3.40}$$

An ideal symmetrical lattice is designed as a phase shifting unit under perfect transmission over the entire frequency axis such that $S_{11}(p) = 0$, which yields $z_a(p)z_b(p) = 1$ as in (3.36).

Furthermore, (3.40) results in

$$S_{21}(p)S_{21}(-p) = 1 \tag{3.41}$$

Employing the normalized impedances in (3.27) and (3.28), scattering parameters of $[N]$ are re-written as,

$$S_{11}(p) = S_{22}(p) = \frac{z_a z_b - 1}{z_a z_b + (z_a + z_b) + 1} \tag{3.42}$$

$$S_{21}(p) = S_{12}(p) = \frac{(z_b - z_a)}{z_a z_b + (z_a + z_b) + 1} \tag{3.43}$$

Under perfect transmission (i.e. for Foster z_a and z_b satisfying $z_b = \frac{1}{z_a}$ condition), (3.42) and (3.43) become

$$S_{11}(p) = S_{22}(p) = 0 \tag{3.44}$$

$$S_{21}(p) = S_{12}(p) = \frac{(1 - z_a^2)}{(1 + z_a^2) + 2z_a} = \frac{1 - z_a(p)}{1 + z_a(p)} \tag{3.45}$$

At this point, (3.41) must be verified for $z_b = \frac{1}{z_a}$ case. This proof is straightforward.

Normalized impedances are odd functions of p as described by $z_a(p) = O_a(p)$ and $z_a(-p) = -O_a(p)$. Then, using (3.33), (3.34), (3.41) and (3.42), we construct $S_{21}(p)S_{21}(-p)$ as follows.

$$S_{21}(p)S_{21}(-p) = \left[\frac{1 - O_a}{1 + O_a}\right]\left[\frac{1 + O_a}{1 - O_a}\right] = 1 \tag{3.46}$$

Hence, verification is completed.

In the following, we will investigate the phase shifting properties of lossless symmetrical lattice structures with simple impedance forms.

3.2 Lossless Symmetrical Latice Structure Utilized as a Phase Shifter

As discussed in the above section, perfect transmission condition or equivalently "all pass condition" imposes two-major restrictions on the series and the cross arm impedances of a lossless symmetrical lattice section.

1. Symmetrical arm impedances Z_A and Z_B or equivalently normalized impedances $z_a(p)$ and $z_b(p)$ must be Foster functions. Therefore, they must be odd functions in complex variable p such that $z_a(-p) = -z_a(p)$ and $z_b(-p) = -z_b(p)$.
2. Algebraic form of the normalized Foster impedance $z_a(p)$ must be equal to the inverse of $z_b(p)$. In other words, $z_a(p) = 1/z_b(p)$.

Thus, one can construct variety of lossless symmetrical lattice all-pass sections as long as z_a and z_b are Foster functions and they satisfy $z_a(p) = 1/z_b(p)$ condition.

Regarding the design of a phase shifter unit, let $x_1, x_2, \dots, x_m$ be the unknown element values of the normalized Foster impedance $z_a(j\omega, x_1, x_2, \dots, x_m) = O_a(j\omega) = jx_a(\omega)$.

Then, by (3.45)

$$S_{21}(p) = \frac{1 - jx_a}{1 + jx_a} = 1.e^{j\varphi_{21}(\omega)} = e^{-2jtan^{-1}[x_a(\omega)]} \tag{3.47}$$

or

$$\varphi_{21}(\omega) = -2tan^{-1}[x_a(\omega)] \tag{3.48}$$

Hence, at a specified frequency f_0 or equivalently angular frequency $\omega_0 = 2\pi f_0$, desired phase shift θ is obtained by setting

$$\theta = -2tan^{-1}[x_a(\omega_0, x_1, x_2, \dots, x_m)] \tag{3.49}$$

(3.46) leads to the solution of unknown components values $x_1, x_2, \dots, x_m$.

In this thesis, we concern with two simple lossless (L) symmetrical (S) lattice (L) sections (S) or in short ($LSLS$). The first one utilizes a simple-single (SS) normalized inductor $x_1 = L_1$ in the series arms, and a simple single (SS) capacitor $C_1 = L_1$ in the cross arms. This is a lagging phase shifter, which provides almost linear negative phase shift in the neighborhood of an operating frequency f_0.

The second one is called the leading $LSLS$ with capacitors C_2 in the series arms and inductors $L_2 = C_2$ in the cross arms. This structure yields almost linear positive phase shift in the neighborhood f_o.

In the following sub-sections, operation of lagging and leading $LSLS$ is detailed.

3.2.1 Lagging Lossless Symmetrical Lattice Section

The lagging $LSLS$ is depicted in Fig. 3.2. This configuration is also referred as "$Type - I$" phase shifting unit or equivalently phase shifting cell.

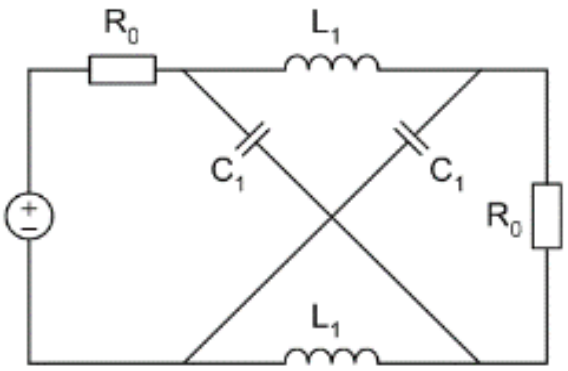


Figure 3.2 : LC lattice topology with lagging phase shift (Type-I topology).

For the above unit, let the actual impedances be $\mathrm{Z_A}(j\omega_a) = j\omega_a L_A$ and $Z_B = \frac{1}{j\omega_a C_B}$.

Then, by perfect transmission we have,

$$\frac{(j\omega_a L_A)/R}{(j\omega_a C_B)R} = 1 \tag{3.50}$$

In the above formulation, $\omega_a = 2\pi f_a$ refers to actual angular frequency for which f_a is the actual frequency itself.

At a given specific actual frequency f_0 or equivalently angular frequency $\omega_0 = 2\pi f_0$, normalized inductor L_1 and capacitor $C_1$is defined as

$$L_1 = \frac{\omega_0 L_A}{R} = \frac{2\pi f_0 L_A}{R} \tag{3.51}$$

$$C_1 = \omega_0 R C_A = 2\pi f_0 R C_A \tag{3.52}$$

Let the normalized frequency f be

$$f = f_a / f_0 \tag{3.53}$$

Then, the normalized angular frequency ω is given by

$$\omega = 2\pi f = \frac{\omega_a}{\omega_0} = \frac{f_a}{f_0} \tag{3.54}$$

Based on the above nomenclature, (3.36) and (3.37) yields that

$$L_1 = C_1 \tag{3.55}$$

Thus, in (3.47) by setting $x_{an}(\omega) = \omega L_1$, we have the following transfer scattering parameter S_{21n}

$$S_{21n}(j\omega) = \frac{1 - j\omega L_1}{1 + j\omega L_1} = 1.\, e^{j\varphi_{21n}(\omega)} \tag{3.56}$$

where

$$\varphi_{21n}(\omega) = -2tan^{-1}(\omega L_1) \tag{3.57}$$

In the above formulation, subscript "n" refers to negative phase shifting property of $Type - I$ structure.

3.2.2 Leading Lossless Symmetrical Lattice Section

As opposed to lagging phase shifter ($Type - I$), leading phase shifter topology has capacitors on the series paths and inductors on the cross paths as shown in Fig. 3.3. This configuration is called $Type - II$ phase shifting unit.

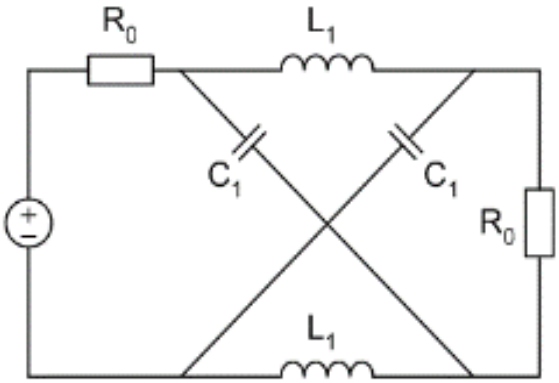


Figure 3.3 : LC lattice topology with leading phase shift (Type-II topology).

In (3.47) by setting $x_{ap}(\omega) = -\frac{1}{\omega C_2}$ and $L_2 = C_2$, $Type - II$ phase shifter configuration must possess the following transfer scattering parameter $S_{21p}(j\omega) = 1.e^{j\varphi_{21p}(\omega)}$.

$$S_{21p}(j\omega) = S_{12p}(j\omega) = \frac{1 - 1/j\omega C_2}{1 + 1/j\omega C_2} = \frac{1 + j\dfrac{1}{\omega C_2}}{1 - j\dfrac{1}{\omega C_2}} = 1.e^{j\varphi_{21p}} \tag{3.58}$$

where

$$\varphi_{21p}(\omega) = +2tan^{-1}\left[\frac{1}{\omega C_2}\right] \tag{3.59}$$

In the above formulation subscript "p" refers to positive phase shifting property of $Type - II$ configuration.

3.3 Switching Between Symmetrical Latice Sections

In Fig. 3.4, one can obtain a wide phase shift by switching between Type − I and Type − II sections. In doing so, one is able to cover complete phase plane (i.e. $0^0 - 360^0$). The phase state of Type − I section is called "State-A". Similarly, the phase state of Type − II section is called "State-B". Then, the phase difference between State-B and State-A is given by

$$\Delta\theta(\omega) = \theta_B(\omega) - \theta_A(\omega) \ = 2[arctan\left(\frac{1}{\omega C_2}\right) + arctan(\omega L_1)] \tag{3.60}$$

where θ_A and θ_B refers to phase states of $\text{Type} - \text{I}$ and $\text{Type} - \text{II}$ sections respectively.

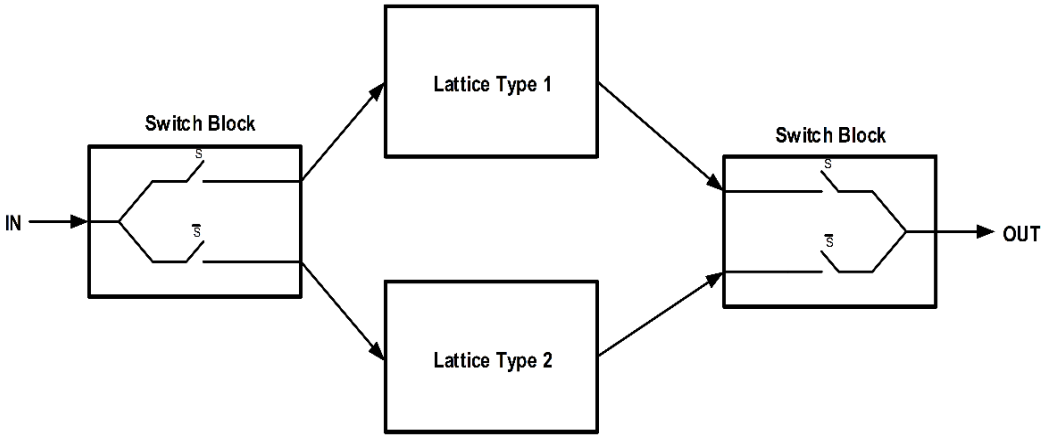


Figure 3.4 : Swiching between Type-I and Type-II topologies.

During target phase shift $\Delta\theta_0 = |\theta_{B0} - \theta_{A0}|$ selection, one is free to choose either even or un-even phase distributions between the states. In other words, we can either choose $\theta_{B0} = \theta_{A0}$ or $\theta_{B0} \neq \theta_{A0}$.

Thus, (3.60) indicates that by switching from State-A to State-B, one is able to cover complete 360^0 phase range.

Once the element values are computed, phase shifting performance of Fig. 3.4 can be investigated by plotting the transfer scattering parameter $S_{21}(j\omega)$ over a wide frequency band for both State-A and State-B. In this regard, generic form of the scattering parameter of (3.42) and (3.43) must be programmed as a function of the normalized angular frequency ω such that

$$S_{21(\text{A or B})}(j\omega) = \frac{z_a - z_b}{z_a z_b + (z_a + z_b) + 1} \tag{3.61}$$

and

$$S_{21(\text{A or B})}(j\omega) = R_{21(A\ or\ B)}(\omega) + jX_{21(A\ or\ B)}(\omega) \tag{3.62}$$

$$S_{21(\text{A or B})}(j\omega) = \rho_{21(\text{A or B})}(j\omega)e^{\varphi_{21(\text{A or B})}(\omega)} \tag{3.63}$$

In the above representation subscripts A and B refers to S_{21} at State-A and State-B respectively. Signal attenuation performance of the phase shifting sections is measured by means of the Transducer Power Gain (TPG). TPG is generated by

$$\mathrm{Gain}(\omega) = \rho_{21}^2(\omega) = \mathrm{R}_{21}^2(\omega) + \mathrm{X}_{21}^2(\omega) \tag{3.64}$$

or in dB,

$$\mathrm{TPG_{dB}}(\omega) = 10\log_{10}\rho_{21}^2 = 20\log_{10}\rho_{21}(\omega) \tag{3.65}$$

The phase response is

$$\varphi_{21}(\omega) = \tan^{-1}\left[\frac{\mathrm{X}_{21}(\omega)}{\mathrm{R}_{21}(\omega)}\right] \tag{3.66}$$

For an ideal digital phase shifter, the target phase shift $\Delta\theta(\omega) = \varphi_{21\mathrm{B}}(\omega) - \varphi_{21\mathrm{A}}(\omega)$, must be flat and $\mathrm{TPG}(\omega) = \rho_{21}^2(\omega)$ must be unity for both State-A and State-B over the frequency band of interest.

Flatness of the $\Delta\theta(\omega)$ may be simply achieved if waveforms of $\varphi_{21\mathrm{B}}(\omega)$ and $\varphi_{21\mathrm{A}}(\omega)$ are the same and shifted from each other by $\Delta\theta_0$. The simplest generic form of these functions may be two parallel lines as depicted in Fig. 3.5. However, in practice, this is not the case. (3.66) indicates that, phase curves of State-A and State-B are specified as arctangent functions. Therefore, the phase range and the bandwidth of the phase shifter must lay within a quasi-linear region of (3.66). Referring to Fig. 3.5, for example, if we select the target phase shift as $\Delta\theta_0 = 90^0$ at $\omega_0 = 1$, State-A phase is $\varphi_{21\mathrm{A}} = \arctan(\omega \mathrm{L}_1)$ (red curve) and in State-B $\varphi_{21\mathrm{B}} = \arctan[1/(\omega \mathrm{C}_2)]$ (blue curve). If we define the quasi linear region within 10% of the target phase shift (yellow curve) then, the bandwidth runs from normalized angular frequency $\omega_1 = 0.561$ to $\omega_2 = 1.782$ which is about 1.588 octave. This example clearly indicates that symmetrical lattice-based topologies provide substantial bandwidth over the classical phase shifter circuits presented in the literature [1-45]. At this point, let us discuss the practical implementation of the above digital phase shifter configuration. At the first glance, our target is to design multi-purpose compact digital phase shifter units to be utilized over the X band in variety of different commercial and military applications such as smart antenna array systems.

Considering the overall cost of the physical implementation, choice of 0.18μm Silicon based Microwave Monolithic Integrated Circuit (MMIC) technology may be attractive.

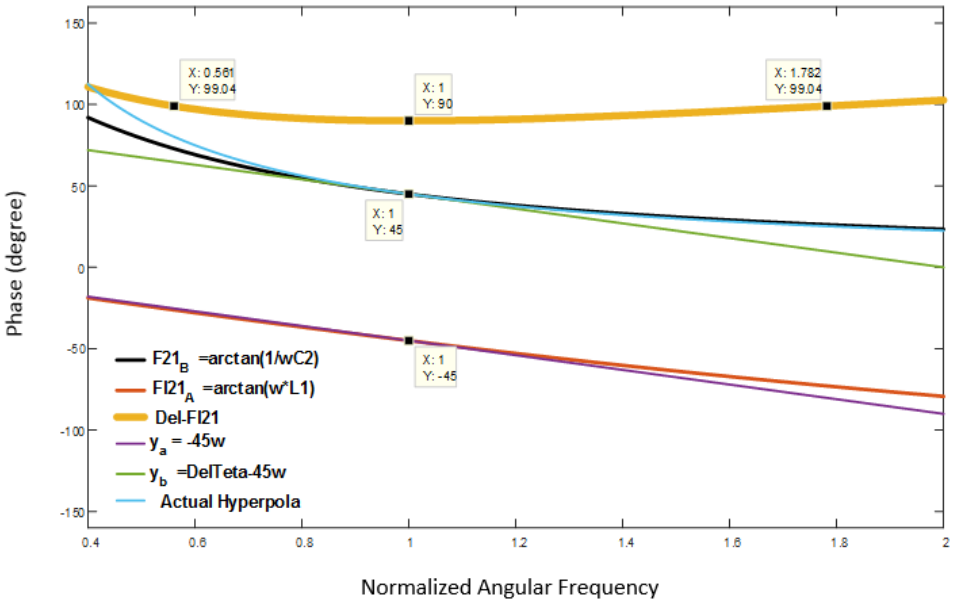


Figure 3.5 : Two parallel phase curves shifted by desired phase shift.

In this regard, straightforward implementation of Fig. 3.4 requires two-bulky "single pole-double throw" switches (one is for the input and the other is for the output). Furthermore, layout connection of Type – I and Type – II lattice topologies may occupy large chip area together with several parasitic elements that highly complicates the realization. Therefore, this approach is not feasible by cost and technology wise. Hence, one needs to come up with a new idea to reduce the utilization of structure and bulky switches in the circuit design. This way of thinking leads us, perhaps, to reduce the number of lattice sections from two to one, which saves substantial chip area, reduces the number of parasitic elements, which in turn reduces the overall loss of the circuit, and thus, improves the bandwidth.

4. PROPOSED SIMPLE-SINGLE AND SYMMETRICAL DIGITAL PHASE SHIFTER

In this thesis, we propose a novel digital circuit topology together with a switching scheme to implement the operation of Fig. 3.4. Proposed compact phase shifter topology saves substantial chip area, reduces the number of parasitic elements, which in turn reduces the overall loss of the circuit, and thus, improves the bandwidth. The new approach offers wide phase shift range over broad frequency band with low phase error and insertion loss. The crux of the idea is to combine the operation of Type – I and Type – II sections under one-compact symmetrical circuit topology. This circuit is called the "Simple and Single-Symmetrical Digital Phase Shifter (SSS-DPS or 3S-DPS)". In Fig. 4.1, 3S-DPS is constructed with ideal switches. Depending on the position of the switches, 3S-DPS either acts as Type – I or Type – II topology. In the following section, detail operation of 3S-DPS using ideal switches is explained with explicit design equations.

4.1 Analysis of Simple and Single-Symmetrical Digital Phase Shifter

The proposed ideal 3S-DPS configuration is depicted in Fig. 4.1.

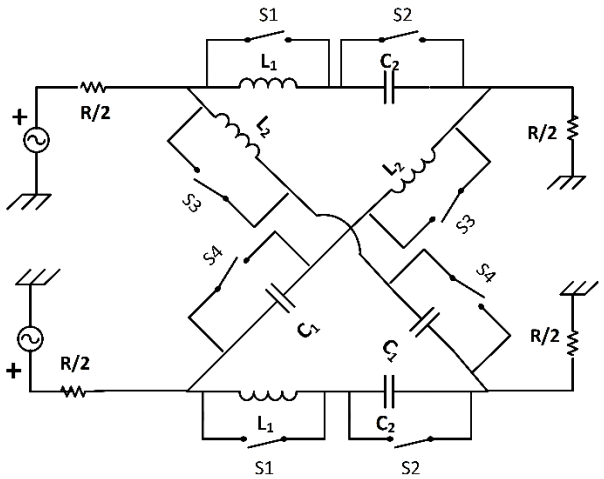
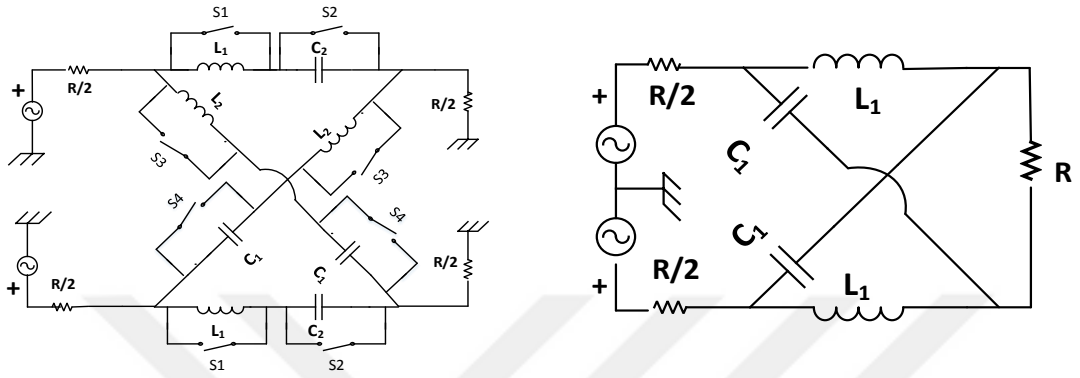


Figure 4.1 : Proposed compact phase shifter with ideal elements.

In this figure, series arms (top and bottom) include inductors L_1 with parallel switches S1 and series capacitors C_2 with parallel switches S2. Similarly, cross arms consist of

inductors L_2 with parallel switches S3 and series capacitors C_1 with parallel switches S4.

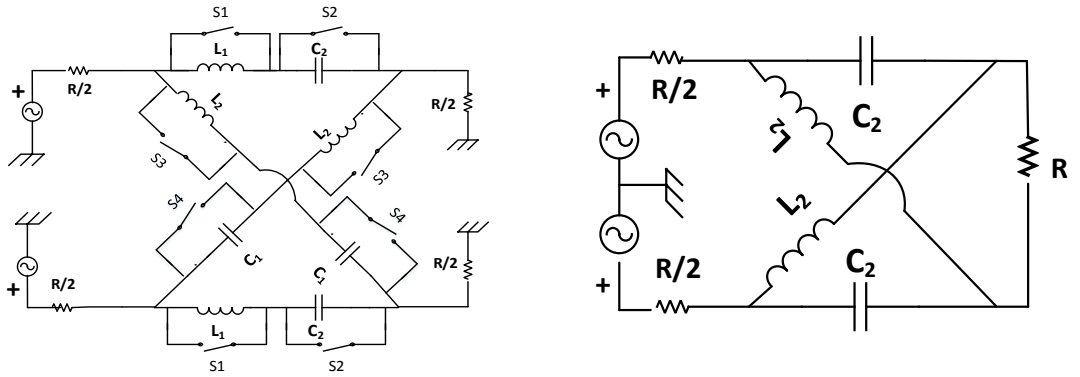
When S1&S4 are OFF and S2&S3 are ON (Switching State-A), the phase shifting circuit resembles the operation of Type − I symmetrical lattice structure as shown in Fig. 4.2.



a b

Figure 4.2 : a) 3S-DPS with ideal switches in State A. b) Equivalent circuit of 3S-DPS with ideal switches in State A.

In a similar manner, when S1&S4 are ON and S2&S3 are OFF (Switching State-B), then the 3S-DPS resembles the operation of Type − I symmetrical lattice section as shown in Fig. 4.3.



a b

Figure 4.3 : a) 3S-DPS with ideal switches in State B. b) Equivalent circuit of 3S-DPS with ideal switches in State B.

At the normalized angular frequency $\omega_0 = 1$, let $\Delta\theta_0 = \varphi_{12B}(\omega_0) - \varphi_{12a}(\omega_0)$ be the target phase shift between the State-B and State-A respectively. Let us further assume that, for each state, $\Delta\theta_0$ is evenly distributed. In other words, for $\text{State} - \text{A}$ $\theta_A = \varphi_{12A}(\omega_0) = -\frac{\Delta\theta(\omega_0)}{2}$ and for $\text{State} - \text{B}, \theta_B = \varphi_{12B}(\omega_0) = \frac{\Delta\theta(\omega_0)}{2}$.

Regarding $\mathrm{State}-\mathrm{A}$ operation, at $\omega = \omega_0$, desired phase shift $\varphi_{12\mathrm{A}} = -\frac{\Delta\theta(\omega_0)}{2}$ is determined using (3.57) as

$$\varphi_{12\mathrm{A}} = -2\arctan(\omega_0 \mathrm{L}_1) \tag{4.1}$$

or normalized value of the series arm inductors L_1 is given by

$$\mathrm{L}_1 = \left(\frac{1}{\omega_0}\right)\tan\left(\frac{\Delta\theta_0}{4}\right) = \tan\left(\frac{\Delta\theta_0}{4}\right) \tag{4.2}$$

and the normalized value of the cross-arm capacitors C_1 are determined as in (3.55). Hence,

$$\mathrm{C}_1 = \mathrm{L}_1 \tag{4.3}$$

Similarly, in $\mathrm{State}-\mathrm{B}$, at $\omega_0 = 1$, series arm capacitors C_2 are computed using (3.59) as

$$\mathrm{C}_2 = \frac{1}{\omega_0 \tan\left(\frac{\Delta\theta_0}{4}\right)} = \frac{1}{\tan\left(\frac{\Delta\theta_0}{4}\right)} = \frac{1}{\mathrm{L}_1} \tag{4.4}$$

and the normalized value of the cross-arm inductors L_2 are

$$\mathrm{L}_2 = \mathrm{C}_2 = \frac{1}{\mathrm{L}_1} \tag{4.5}$$

Thus, the net phase shift $\Delta\theta = \theta_\mathrm{B} - \theta_\mathrm{A}$ between the states A and B is given by

$$\Delta\theta(\omega) = \varphi_{12B}(\omega) - \varphi_{12A}(\omega) = 2\left[tan^{-1}\left(\frac{1}{\omega C_2}\right) + tan^{-1}(\omega L_1)\right] \tag{4.6}$$

Clearly, the above equation yields the desired phase shift $\Delta\theta_0 = \Delta\theta(\omega)$ at $\omega = \omega_0 = 1$. However, as we move away from ω_0, a deviation or perturbation δ_θ $(in\ percentage\ of\ \Delta\theta_0)$ is observed. Literally, phase perturbation is defined as the percentage of the target phase shift $\Delta\theta_0$ such that

$$\delta_\theta = \frac{\Delta\theta(\omega) - \Delta\theta_0}{\Delta\theta_0} \times 100 \tag{4.7}$$

It is expected that δ_θ is tolerable over at least one octave bandwidth due symmetrical lattice operation. This fact can easily be observed by means of a simple example.

Example 1.

At $\omega_0 = 1$, let the target phase shift be $\Delta\theta = 45^0$. Find the normalized component values of an 3S-DPS of Fig. 4.1 and plot the phase-shift $\Delta\theta(\omega)$ and observe its perturbation over a large bandwidth.

Answer:

Solution of (4.2-4.5) yields the normalized component values of 3S-DPS as listed in Table 4.1.

Table 4.1 : Normalized component values of ideal 45^0 3S-DPS.

Type 1 Parameters	Type 2 Parameters
$L_1 = C_1 = \left[\frac{1}{\omega_0}\right]\left[tan\left(\frac{45}{4}\right)\right] = 0.1989$	$C_2 = L_2 = \left[\frac{1}{\omega_0}\right]\left[\frac{1}{tan\left(\frac{45}{4}\right)}\right] = 5.0273$

The phase shift $\Delta\theta(\omega) = \varphi_{12B}(\omega) - \varphi_{12A}(\omega)$ is depicted in Fig. 4.4.

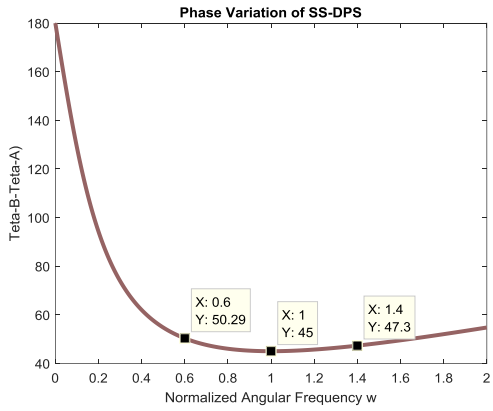


Figure 4.4 : Plot of $\Delta\theta(\omega) = \theta_B - \theta_A$ for example 1.

Also separate plots of $\theta_B(\omega)$ and $\theta_A(\omega)$ are shown in Fig. 4.5. Close examination of Fig. 4.5 reveals that, at the normalized angular frequency $\omega = 1$, the net phase shift between the states is $\Delta\theta(\omega) = 45^0$ as desired.

Over an octave bandwidth (i.e.$0.6 \leq \omega \leq 1.2$), maximum phase deviation δ_θ is about $\delta_\theta = \frac{50.29-45}{45} \times 100$ =11.76%.

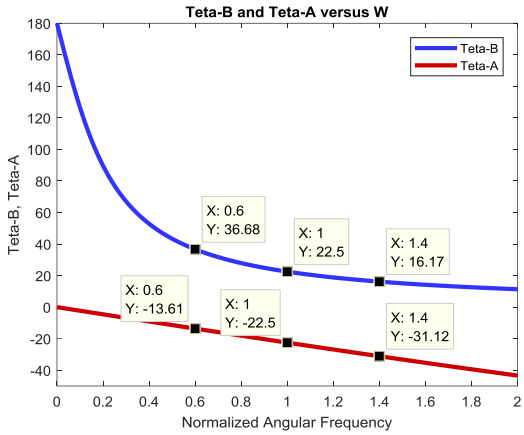


Figure 4.5 : Plots of θ_A and θ_B for example 1.

Perturbation of the phase curves away from the center frequency is due to nonlinear behavior of arctangent curves of (4.6). Nonlinearity is dominant at the lower frequencies since $arctan\left(\frac{1}{\omega C_2}\right)$ jumps to 180^0 at $\omega = 0$. The bandwidth improves as the net phase shift between the states becomes larger. It is ideal when $\Delta\theta(\omega) = 180^0$. Let us investigate this situation in the following example.

Example 2.

At $\omega_0 = 1$, let the target phase shift be $\Delta\theta = 45^0, 90^0, 135^0 and\ 180^0$. Plot the phase-shift $\Delta\theta(\omega)$ and observe its perturbation over a large bandwidth.

Answer:

After solving (4.2-4.5), normalized component values for $\Delta\theta = 45^0, 90^0$, 135^0 and 180^0 are found as in Table 4.2.

Table 4.2 : Normalized component values of 3S-DPS with different phase shifts.

Phase Shift	$L_{p1} = C_{p2} = 1/C_{p1}$	$C_{p1} = L_{p2} = 1/L_{p1}$
$\Delta\theta = 45^0$	0.1989	5.0273
$\Delta\theta = 90^0$	0.4142	2.4142
$\Delta\theta = 135^0$	0.6682	1.4966
$\Delta\theta = 180^0$	1	1

Corresponding net phase shift $\Delta\theta$ is depicted in Fig. 4.6. As it is seen from this figure, $\Delta\theta_0 = 180^0$ case or $\frac{\Delta\theta_0}{4} = 45^0$ case yields perfect phase spread over the entire frequencies due to the nature of (4.6). As the target phase shift $\Delta\theta_0 = \Delta\theta(\omega_0)$ increases from 45^0 to 180^0, phase perturbation decreases down to zero.

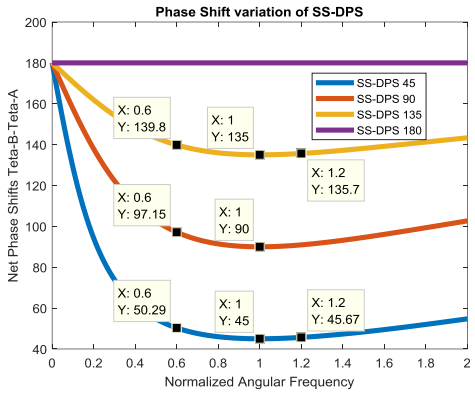


Figure 4.6 : Plots of $\Delta\theta(\omega) = 45^0, 90^0, 135^0, and\ 180^0$ for example 2.

In Fig. 4.7, maximum phase perturbation δ_θ is depicted. In this figure, ordinate is assigned to maximum deviation in percentage over an octave bandwidth. The abscissa is linked with the target phase shifts 45^0, 90^0 135^0, 180^0 of the phase curves. In this regard, let $\omega_0 = 1$ be the center frequency of the "one octave bandwidth" of $0.6 \leq \omega \leq 1.2$. Also let the maximum phase shift deviation in percentage be δ_θ. It is noted that maximum deviation or perturbation occurs at the lower end of the band. In this case, at $\omega_1 = 0.6$, the phase shift is given by

$$\Delta\theta(\omega_1) = \Delta\theta_1 = \Delta\theta_0 + \delta_\theta\Delta\theta_0 \tag{4.8}$$

Maximum phase deviation of (4.7) can be computed for each phase-curve as tabulated in Table 4.3.

Table 4.3 : Maximum phase perturbation δ_θ on the phase curves.

Phase Shift	$\Delta\theta_1$ @ $\omega_1 = 0.6$	$\delta_\theta = \frac{\Delta\theta_1 - \Delta\theta_0}{\Delta\theta_0}$ (%)
$\Delta\theta = 45^0$	50.29^0	11.76
$\Delta\theta = 90^0$	97.15^0	7.944
$\Delta\theta = 135^0$	139.8^0	3.5556
$\Delta\theta = 180^0$	180^0	0

In this case, perturbation δ_θ may be expressed in terms of target phase shifts $\Delta\theta_0$ and its maximum value $\Delta\theta_1$ over the selected frequency band of operation such that $\delta_\theta = \delta_\theta(\Delta\theta_0, \Delta\theta_1)$. Hence, Table 4.3 is depicted in Fig. 4.7 as a three dimensional plot. So far, we have dealt with ideal switches and lossless circuit components. Unfortunately, this is not case in daily practice. Therefore, in the following section, we concern with actual implementation of the proposed 3S-DPS constructed with NMOS transistors.

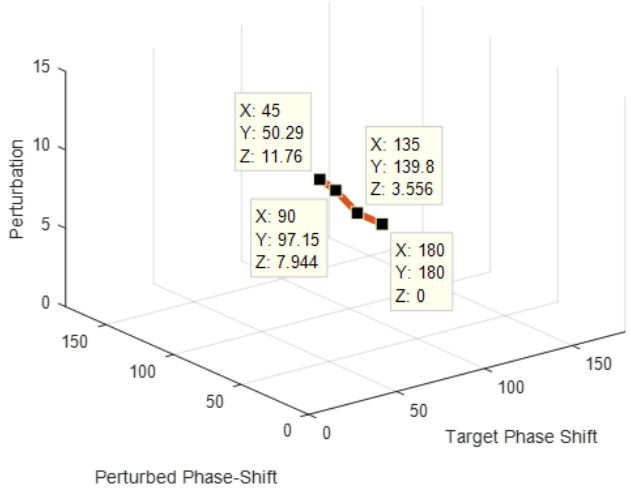


Figure 4.7 : 3D Plot of perturbation δ_θ for example 1.

4.2 Analysis of Simple and Single-Symmetrical Digital Phase Shifter with CMOS Switches

The ideal switches shown in Fig. 4.1 can be replaced by MOSFET switches for the practical implementation of the 3S-DPS topology. The practical implementation is shown in Fig. 4.8.

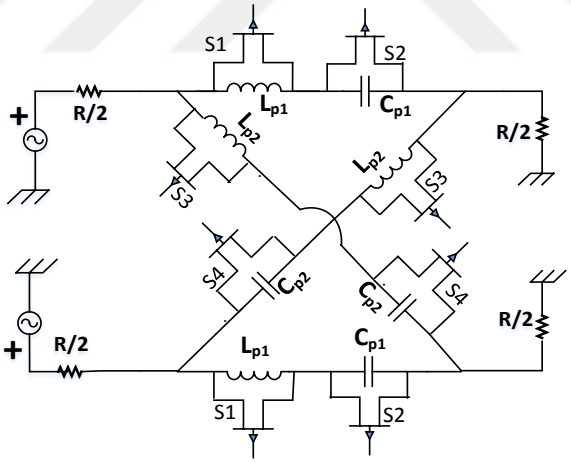


Figure 4.8 : Practical implementation of 3S-DPS topology.

In order to analyze the simple and single symmetrical digital phase shifter with practical CMOS switches, we should analyze MOSFET transistor utilized as a switch. The Metal Oxide Semiconductor Field Effect Transistors (MOSFET) are widely used in RF and microwave integrated circuit switch applications. Transistor frequency performance is associated with its transit frequency f_T. f_T is the frequency upon which the current-gain is unity. f_T values for different CMOS processes such as 0.25µm, 0.18µm, 0.13µm and 90nm are 30, 50, 75 and 110 GHz respectively. In this work, we

have the freedom to use TSMC's $0.18\mu m$ NMOS transistors as switching elements. ON and OFF modes of an NMOS $0.18\mu m$ transistor can be modeled as shown in Fig. 4.9.

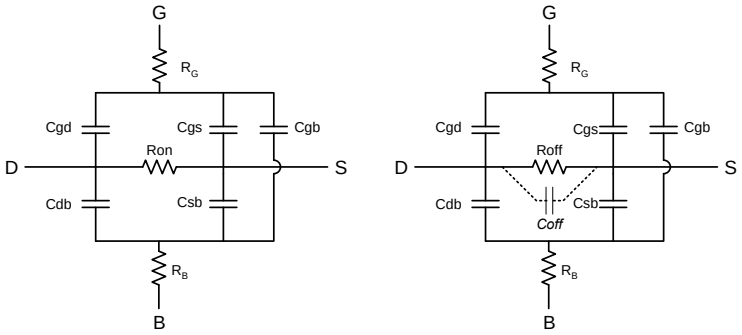


Figure 4.9 : NMOS equivalent circuits of ON state (left) and OFF state (right).

At the "ON" state ($V_{GS} = 1.8\,V$), most effective component of the model is the channel resistor R_{on}. For the process under consideration, selected R_{on} varies from 7.5Ω ohm to 60Ω. At the "OFF" state ($V_{GS} = 0\,V$), transistor simply exhibits a capacitor $C_{DS} = C_{off}$. For the selected gate length $L = 180\,nm$, the product of $R_{on} \times C_{off}$ of the 0.18µm TSMC process is constant and it is given by

$$R_{on}(\Omega) \times C_{off}(Farad) = 672 \times 10^{-15} \tag{4.9}$$

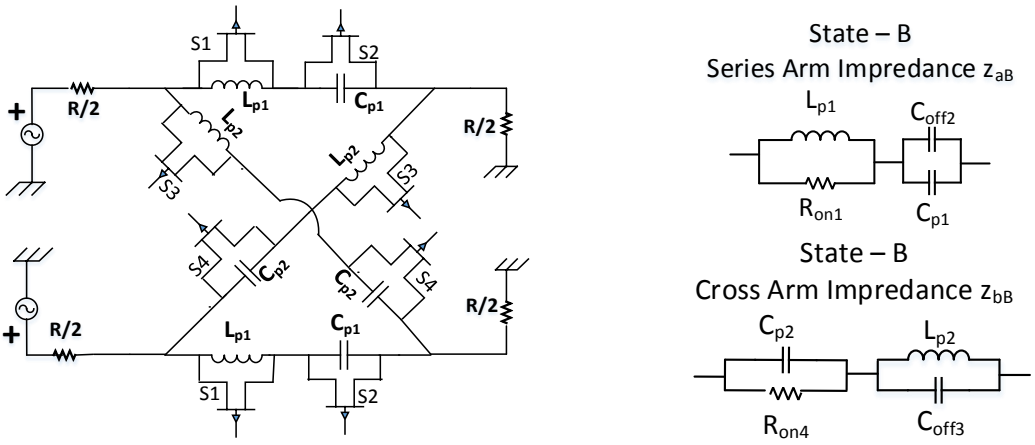
where R_{on} is the ON state resistance; C_{off} is the OFF state capacitor of the NMOS transistor respectively.

In this case, for the selected-ON state channel resistor R_{on}, OFF state capacitor C_{off}, actual components of the 3S-DPS cell is determined. Considering the simplified models of the CMOS switches, let us investigate State-B and State-A modes of a SSS-DPS (3S-DPS) cell. In the following section details of 3S-DPS topology is presented.

4.2.1 Operation of 3S-DPS Topology at Leading State (State-B)

The branch models of the 3S-DPS topology at State-B operation is given in Fig. 4.10. Referring to Fig. 4.10, in State-B, the series arms switch S1 is ON. Therefore, NMOS transistor loads the inductor L_{p1} with the channel resistor R_{on1}. In this mode of operation, S2 is OFF. Then, the capacitor C_{p1} is loaded with the switch capacitor C_{off2}.

In this case, the series arm impedance is given by



a b

Figure 4.10 : a) Proposed 3S-DPS unit cell topology b) Equivalent circuit of 3S-DPS in State B.

$$z_{aB}(j\omega) = \left(R_{on1} \parallel j\omega L_{p1}\right) + \frac{1}{j\omega\left(C_{p1} + C_{off2}\right)} \tag{4.10}$$

or

$$z_{aB}(j\omega) = \frac{\omega^2 R_{on1} L_{p1}^2}{R_{on1}^2 + \omega^2 L_{p1}^2} + j\frac{\omega R_{on1}^2 L_{p1}}{R_{on1} + j\omega L_{p1}} + \frac{1}{j\omega\left(C_{p1} + C_{off2}\right)} \tag{4.11}$$

Using straight forward algebraic derivations, open form of $z_{aB}(j\omega)$ is found as

$$z_{aB}(j\omega) = \left[\frac{\omega^2 R_{on1} L_{p1}^2}{R_{on1}^2 + \omega^2 L_{p1}^2}\right] + j\left[\frac{\omega R_{on1}^2 L_{p1}}{R_{on1}^2 + \omega^2 L_{p1}^2} - \frac{1}{\omega\left(C_{p1} + C_{off2}\right)}\right] \tag{4.12}$$

In (4.12), it is expected that R_{on1} is small enough so that series arm impedance is approximated as

$$z_{aB}(j\omega) \cong \frac{1}{j\omega\left(C_{p1} + C_{off2}\right)} \tag{4.13}$$

In this mode of operation, at $\omega_0 = 1$, ideally, it is desired that $z_{aB} = \frac{1}{j\omega C_2}$. Thus, the unknown capacitors of the series arms are estimated as

$$C_{p1} = C_2 - C_{off2} \geq 0 \tag{4.14}$$

It is crucial to note that, (4.14) imposes a serious restriction on switch S2 such that

$$C_2 \geq C_{off2} \tag{4.15}$$

or in the worst case $C_{p2} = 0$ requires that maximum value of C_{off2} must not exceed C_2 such that

$$\left(C_{off2}\right)_{max} = C_2 \tag{4.16}$$

At this point, we may control the value of C_{off2} by defining a positive real number k_2 such that

$$C_{off2} = k_2\left(C_{off2}\right)_{max} \tag{4.17}$$

where k_2 is called the capacitor control coefficient of S2.

Equation (4.17) guides the design of the second switch S2. Clearly, OFF mode capacitance of NMOS transistor switch cannot exceed the capacitor C_2. We should also consider an optimum value for the OFF mode NMOS transistor switch capacitors. Let the actual and normalized values of the optimum switch capacitor be C_{a-opt} and C_{n-opt} respectively. In this case, if one wishes to make the digital phase shifter design based on the optimum value of the switch capacitor $C_{n-opt} = C_{off2}$, then the value of k_2 capacitor control coefficient is determined as

$$k_2 = \frac{C_{off2}}{\left(C_{off2}\right)_{max}} = \frac{C_{\mathrm{n-opt}}}{C_2} \leq 1 \tag{4.18}$$

If the above condition is not satisfied, the best choice for k_2 is unity which makes $C_{p1} = 0$.

Let us further continue with the computations in State-B mode when the switch transistor S3 is OFF and switch transistor S4 is ON. In this mode of operation (State-B), the cross-arm impedances z_{bB} is evaluated as

$$z_{bB}(j\omega) = \left(R_{on4} \parallel j\omega C_{p2}\right) + (j\omega L_{p2}) \parallel \left(\frac{1}{j\omega C_{off3}}\right) \tag{4.19}$$

or

$$z_{bB}(j\omega) = \frac{R_{on4}}{1 + j\omega R_{on4} C_{p2}} + j\frac{\omega L_{p2}}{1 - \omega^2 L_{p2} C_{off3}} \tag{4.20}$$

$$z_{bB}(j\omega) = \frac{R_{on4}}{1 + \left(\omega R_{on4} C_{p2}\right)^2} + j\omega\left[\frac{L_{p2}}{1 - \omega^2 L_{p2} C_{off3}} - \frac{R_{on4}^2 C_{p2}}{1 + \left(\omega R_{on4} C_{p2}\right)^2}\right] \tag{4.21}$$

In a similar manner to that of (4.12), in (4.21), R_{on4} must be small enough to be neglected as compared to the term $\frac{L_{p2}}{1-\omega^2 L_{p2} C_{off3}}$. Furthermore, in this mode of operation, for the target phase shift $\Delta\theta_0$, which is specified at the normalized angular center frequency ω_0, the term $\frac{L_{p2}}{1-\omega^2 L_{p2} C_{off3}}$ must be equal to ideal cross arm inductors L_2. Hence, the unknown cross arm inductor L_{p2} is estimated as

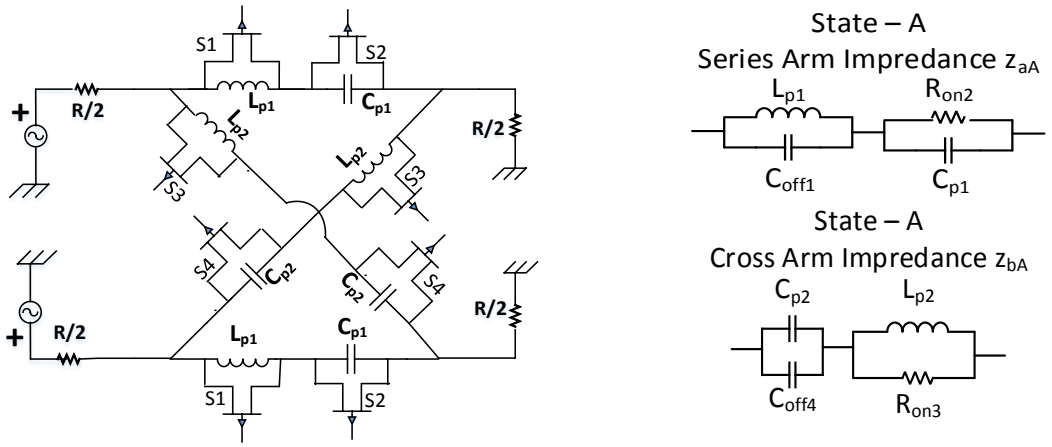
$$L_{p2} = \frac{L_2}{1 + \omega_0^2 L_2 C_{off3}} \tag{4.22}$$

It is nice to report that (4.22) does not impose any restriction on L_{p2}.

In summary, in State-B operation, for a given phase shift $\Delta\theta_0$, we were able to roughly estimate series arm capacitors as $C_{p1} = C_2 - C_{off2}$ and cross arm inductors as $L_{p2} = L_2/\left(1 + \omega_0^2 L_2 C_{off3}\right)$.

4.2.2 Operation of 3S-DPS Topology at Lagging State (State-A)

The branch models of the 3S-DPS topology at State-B operation is given in Fig. 4.11.



a b

Figure 4.11 : a) Proposed 3S-DPS unit cell topology b) Equivalent circuit of 3S-DPS in State A.

In State-A, when switches S1 is OFF and S2 is ON, the series arm impedance z_{aA} is given by

$$z_{aA}(j\omega) = \left(R_{on2} \parallel j\omega C_{p1}\right) + (j\omega L_{p1}) \parallel \left(\frac{1}{j\omega C_{off1}}\right) \tag{4.23}$$

or

$$z_{aA}(j\omega) = \frac{R_{on2}}{1 + j\omega R_{on1} C_{p1}} + j\frac{\omega L_{p1}}{1 - \omega^2 L_{p1} C_{off1}} \tag{4.24}$$

By simple algebraic manipulation,

$$\mathrm{z_{aA}(j\omega)} = \frac{\mathrm{R_{on2}}}{1 + \left(\omega \mathrm{R_{on2}} \mathrm{C_{p1}}\right)^2} + \mathrm{j\omega}\left[\frac{\mathrm{L_{p1}}}{1 - \omega^2 \mathrm{L_{p1}} \mathrm{C_{off1}}} - \frac{\mathrm{R_{on2}^2 C_{p1}}}{1 + \left(\omega \mathrm{R_{on2}} \mathrm{C_{p1}}\right)^2}\right] \tag{4.25}$$

In a similar manner to that of (4.12), the term $\left(R_{on2} \parallel 1/j\omega C_{p1}\right)$ can be neglected due to small size of R_{on2}. At $\omega_0 = 1$. the second term $\left(j\omega L_{p1}\right) \parallel \left(\frac{1}{j\omega C_{off1}}\right) = \frac{L_{p1}}{1-\omega^2 L_{p1} C_{off1}}$ must yield the ideal series arm inductor L_1. Thus, L_{p1} is estimated without any restriction as

$$\mathrm{L_{p1}} = \frac{\mathrm{L_1}}{1 + \omega_0^2 \mathrm{L_1} \mathrm{C_{off1}}} = \frac{\mathrm{L_1}}{1 + \mathrm{L_1} \mathrm{C_{off1}}} \tag{4.26}$$

In cross arms, when switches S3 is ON and S4 is OFF, the equivalent impedance z_{bA} is found as

$$\mathrm{z_{bA}(j\omega)} = \left(\mathrm{R_{on3}} \parallel \mathrm{j\omega L_{p2}}\right) + \frac{1}{\mathrm{j\omega}\left(\mathrm{C_{p2}} + \mathrm{C_{off4}}\right)} \tag{4.27}$$

or

$$\mathrm{z_{bA}(j\omega)} = \left[\frac{\omega^2 \mathrm{R_{on3}} \mathrm{L_{p2}^2}}{\mathrm{R_{on3}^2} + \omega^2 \mathrm{L_{p2}^2}}\right] + \mathrm{j}\left[\frac{\omega \mathrm{R_{on3}^2} \mathrm{L_{p2}}}{\mathrm{R_{on3}^2} + \omega^2 \mathrm{L_{p2}^2}} - \frac{1}{\omega\left(\mathrm{C_{p2}} + \mathrm{C_{off4}}\right)}\right] \tag{4.28}$$

Setting $R_{on3} \cong 0$, and $C_1 = \left(C_{p2} + C_{off4}\right)$, the unknown cross arm capacitor C_{p2} is estimated as

$$C_{p2} = C_1 - C_{off4} \geq 0 \tag{4.29}$$

As it can be seen from (4.29), maximum value of C_{off4} must be equal to C_1. More explicitly,

$$(C_{off4})_{max} = C_1 \tag{4.30}$$

This is the restriction imposed on the fourth switch. In a similar manner to that of (4.18), value of C_{off4} may be controlled by means of a capacitor control coefficient k_4 such that

$$C_{p2} = C_1 - k_4(C_{off4})_{max} = C_1 - k_4 C_1 \geq 0 \tag{4.31}$$

where

$$k_4 = \frac{C_{off4-opt}}{C_1} \leq 1 \tag{4.32}$$

As in (4.18), the best value of k_4 is unity which makes $C_{p2} = 0$.

It should be mentioned that, from the practical point of view, NMOS switches must be designed in such a way that, optimum value of the OFF-mode capacitor should satisfy the following condition

$$C_{off-opt} \leq \min(C_1, C_2) \tag{4.33}$$

As the explicit equations are given both for 3S-DPS topology with ideal and practical switches, in the next section design algorithms are generated to estimate the element values of 3S-DPS topology.

5. DESIGN ALGORITHMS OF 3S-DPS TOPOLOGY

In this section, the design algorithms to design 3S-DPS topology are investigated. First, 3S-DPS with ideal switch design algorithm is investigated.

5.1 Design Algorithm of 3S-DPS with Ideal Switches

In this part, the design algorithm for 3S-DPS as shown in Fig. 4.1 with ideal switches is given. The target phase shift $\Delta\theta_0$ is the main input parameter. Since normalized impedances are used to analyze the 3S-DPS topology, we take normalized center frequency, $\omega_0 = 1$. At the normalized center frequency $\omega_0 = 1$, for a given target phase shift $\Delta\theta_0$, let us define the "major design parameter" μ as

$$\mu = \tan\left(\frac{\Delta\theta_0}{4}\right) \tag{5.1}$$

Using the major design parameter, the component values can be found out generating a design algorithm as follows:

Inputs: Desired phase shift $\Delta\theta_0$.

Computational steps:

Step 1: Compute the major design parameter μ at $\omega_0 = 1$: $\mu = tan\left(\frac{\Delta\theta_0}{4}\right)$

Step 2: Compute the normalized series arm inductor L_1: $L_1 = \frac{1}{\omega_0}\mu$

Step 3: Compute the normalized series arm capacitor C_2: $C_2 = \left(\frac{1}{\omega_0}\right)\left(\frac{1}{\mu}\right)$

Step 4: Compute the normalized cross arm capacitor C_1: $C_1 = L_1$

Step 5: Compute the normalized cross arm inductor L_2: $L_2 = C_2$

It is important to note that a symmetrical lattice network must be derived by means of a symmetrical voltage source so that the ground is isolated from the input and the output port terminals. If the internal impedance of each voltage source is $R_G = 50\Omega$, then the equivalent internal impedance of the driving $Thevénin$ source will be

$R = 2R_G = 100\Omega$. In a similar manner, at the output port, in order to isolate the ground from the output terminals, each terminal is connected to a $R_L = 50\Omega$ so that equivalent output port termination resistor is $R = 2R_L$=100Ω. These practical considerations are clearly shown in Fig. 4.1, Fig. 4.2 and Fig. 4.3. In this case, for the sake of simplicity, the scattering parameters of 3S-DPS or simple and single symmetrical lattice sections is defined with respect to $R = 100\Omega$ and elements values of the actual 3S-DPS is calculated using $R = 100\Omega$. Let us run an example to clarify the remark.

Example 3.

Referring to Example 1, calculate the actual element values 3S-DPS for phase shift $\Delta\theta_0 = 45^0$ at $10\ GHz$. Here, we assume that 3S-DPS is derived using two identical voltage source each having $R_G = 50\Omega$ internal impedance.

Answer:

Since $R_G = 50\Omega$, normalization number for S parameters must be $R = 2R_G = 100\Omega$.

By Example 1, normalized element values are given by

Table 5.1 : Computed normalized element values for ideal 3S-DPS.

$L_1 = C_1 = 0.1989$
$L_2 = C_2 = 5.0273$

Then the actual element values can be computed from the normalized impedances as given in Table 5.2.

Table 5.2 : Computed actual element values for ideal 3S-DPS.

$L_{1a} = \frac{L_1}{\omega_0}R = \frac{0.1989}{2x\pi x10x10^9}x100 = 316\ pH$
$C_{1a} = \frac{C_1}{\omega_0 R} = \frac{0.1989}{2x\pi x10x10^9x100} = 31.65\ fF$
$L_{2a} = \frac{L_2}{\omega_0}R = \frac{5.0273}{2x\pi x10x10^9}x100 = 8\ nH$
$C_{2a} = \frac{C_2}{\omega_0 R} = \frac{5.0273}{2x\pi x10x10^9x100} = 800\ fF$

The normalized and actual values of the 3S-DPS topology is found by using the given design algorithm. In the next parts, design algorithms for practical 3S-DPS circuit will be introduced.

5.2 Design Algorithm of 3S-DPS with Switch Models

The practical design algorithms utilizes the explicit equations given in section 4.2. The design algorithms can be differentiated each other by the selection of phase distribution between the State-A and State-B states of the 3S-DPS topology.

The designer can freely choose phase shift distribution between states and select the algorithm accordingly, but there is a trade-off between algorithm accuracy and performance with the algorithm complexity.

First of all, evenly distrubuted phase shift between the states of the 3S-DPS topology is investigated.

5.2.1 Design Algorithm of 3S-DPS for Evenly Phase Distribution between States

The phase shift of the states, State-A and State-B can be denoted as θ_{A} and θ_{B}. And also since the phase is distributed evenly in this part, the phase shift of the states should be

$$\theta_A = \theta_B = \frac{\Delta\theta_0}{2} \tag{5.2}$$

As an initial note, the actual components are indicated by subscript "a" and all other components are normalized.

Inputs:

Desired phase shift $\Delta\theta_0$ specified at the normalized centered frequency $\omega_0 = 1$.

Actual center frequency f_{0a} $(in\ Hz)$

Actual normalizing Resistor R_a $(It\ may\ be\ selected\ as\ R_a = 100\Omega)$

Optimum switch capacitor values for S1 and S3 which is designated by $C_{off-opt}$ (for the selected $TSMC$ $0.18\mu m$ CMOS process, it may be appropriate to choose it about 90 fF).

Note that $C_{off2} \leq C_2$ and $C_{off4} \leq C_1$.

Computational Steps:

Computational steps are given in Table 5.3.

Table 5.3 : 3S-DPS design algorithm of evenly distributed phase between states.

Part 1: Design of Basic Lattice Sections	Design of ideal Type-1 and Type-2 element values	$\mu = tan\left(\frac{\Delta\theta_0}{4}\right)$
		$L_1 = \frac{1}{\omega_0}\mu$
		$C_1 = L_1$
		$C_2 = \frac{1}{\omega_0}\frac{1}{\mu}$
		$L_2 = C_2$
Part 2: NMOS Switch Designs	Select the optimum value for off-mode switch capacitor C_{off1a} and compute its normalized value C_{off1}	$C_{off1a} = C_{off-opt}$
		$C_{off1} = (2\pi f_{0a})(R_a C_{off1a})$
	Compute the ON state switch channel resistor	$R_{on1a} = \frac{672\ (fF-\Omega)}{C_{off1a}(fF)}$
	Select the normalized value of switch capacitor of S2	$(C_{off2})_{max} = C_2$
	Compute the actual value of $(C_{off2a})_{max}$	$(C_{off2a})_{max} = \frac{(C_{off2})_{max}}{(R_a)(2\pi f_{0a})}$
	Compute ON state resistor R_{on2}	$R_{on2a} = \frac{672\ (fF-\Omega)}{C_{off2a}(fF)}$
	Select the optimum value for C_{off3a}	$C_{off3a} = C_{off1a} = C_{off-opt}$
	Compute normalized value C_{off3}	$C_{off3} = (2\pi f_{0a})(R_a C_{off3a})$
	Select the normalized value of $(C_{off4})_{max}$	$(C_{off4})_{max} = C_2$
	Compute the actual value of $(C_{off4a})_{max}$	$(C_{off4a})_{max} = \frac{(C_{off4})_{max}}{(R_a)(2\pi f_{0a})}$
Part 3: Computation of normalized component values	Compute series arm component value L_{p1}	$L_{p1} = \frac{L_1}{1+\omega_0^2 C_{off1n}}$
	Compute series arm component value C_{p1}	$C_{p1n} = C_2 - k_2 C_{off2-max} \geq 0$
	Compute cross arm component value L_{p2}	$L_{p2} = \frac{L_2}{1+\omega_0^2 C_{off3}}$
	Compute cross arm component value C_{p2}	$C_{p2} = C_1 - k_2 C_{off4-max} \geq 0$
Part 4: Computation of actual component values	Compute actual element values of $L_{p(1,2)a}$	$L_{p(1,2)a} = \frac{L_{p(1,2)}}{2\pi f_{0a}} R_a$
	Compute actual element values of $C_{p(1,2)a}$	$C_{p(1,2)a} = \frac{C_{p(1,2)}}{2\pi f_{0a} R_a}$

Using the above algorithm, let us design a practical 3S-DPS cell for $\Delta\theta = 45^0$.

Example 4.

Let us design a phase shifter using 3S-DPS topology for phase shift of 45^0 at the center frequency of $f_{0a} = 10\,GHz$. For the implementation process, let us assume the optimum capacitor for switch to be $C_{off-opt} = 90\,fF$.

Answer:

For all the calculations, Fig. 4.8, Fig. 4.10 and Fig. 4.11 are used to mention the component names.

As in the part 1 of the algorithm, we can compute the Type-I and Type-II ideal lattice components.

Table 5.4 : Computed normalized element values of example 4 part 1.

$L_1 = C_1 = 0.1989$
$L_2 = C_2 = 5.0273$

Also, we can calculate the actual values of these elements as well.

Table 5.5 : Computed actual element values of example 4 part1.

$L_{1a} = 316.58\,pH$
$C_{1a} = 31.658\,fF$
$L_{2a} = 8.001\,nH$
$C_{2a} = 800.1\,fF$

After finding the component values of Type-I and Type-II ideal lattice section component values, NMOS design part can be executed as given in design algorithm part 2.

The S1 is designed based on $C_{off1a} = 90\,fF$ and $R_{on1a} = \frac{672}{C_{off1}} = 7.46\,\Omega$ or $R_{on1} = 0.0746$.

S2 is designed for $C_{\text{off2}a-max} = C_{2a} = 8.0013e-13\,F$, $k_2 = 1, C_{\text{off2}} = C_{\text{off2}-max}$ which yields $R_{on2a} = \frac{672}{C_{off2a}} = 0.8399\,\Omega$ or normalized $R_{on2} = 0.0084$.

S3 is identical to S1 or equivalently, $C_{off3a} = 90\,fF$ and $R_{on3a} = 7.46\,\Omega$ or $R_{on3} = 0.0746$.

S4 transistor is designed using $C_{\text{off1}a-max} = C_{1a} = 3.1658e-14\,F$, $k_4 = 1$ and $R_{on4a} = \frac{672}{C_{off4a}} = 21.22\ \Omega$ or $R_{on4} = 0.212$.

In part 3, normalized element values of 3S-DPS are computed as

Table 5.6 : Computed normalized element values of example 4 part 3.

$L_{p1} = \frac{L_1}{1 + L_1 C_{off1}} = 0.1788$
$C_{p1} = C_2 - C_{off2} = 0$
$L_{p2} = \frac{L_2}{1 + L_2 C_{off3}} = 1.308$
$C_{p2} = C_1 - C_{off4} = 0$

In part 4, actual elements are computed as follows.

Table 5.7 : Computed actual element values of example 4 part 4.

$L_{p1a} = 284.5$ pH
$C_{p1a} = 0$ F
$L_{p2a} = 2.082$ nH
$C_{p2} = C_1 - C_{off4} = 0$

In the algorithm above, for a specified normalized-optimum value of the NMOS OFF state capacitor $C_{off-opt}$, ON mode switch channel resistors $R_{on(i)}$ and OFF mode NMOS switch capacitors $C_{off(i)}$ are automatically determined to minimize the overall loss of the phase shifting section. In this regard, series arm capacitor is determined as

$$C_{p1} = C_2 - C_{off2} \geq 0 \tag{5.3}$$

where

$$C_{off2} = k_2 C_2 \tag{5.4}$$

The reasonable choice for k_2 is given by

$$k_2 = \frac{C_{off-opt}}{C_2} \leq 1 \tag{5.5}$$

At this point, one must be careful since C_2 is calculated from $\Delta\theta_0$ and $C_{off-opt}$ is selected by considering the technology process to manufacture the digital phase

shifting cell as an MMIC. As the result of these restrictions, k_2 may turn out to be greater than 1. If this is the case, it is set to unity automatically which in turns makes the capacitor $C_{p1} = 0$.

Similarly, C_{p2} is determined by

$$C_{p2} = C_1 - C_{off4} \geq 0 \tag{5.6}$$

where

$$C_{off4} = k_4 C_1 \tag{5.7}$$

and

$$k_4 = \frac{C_{off-opt}}{C_1} \leq 1 \tag{5.8}$$

If k_4 becomes greater than one, then it is set to unity for which $C_{p2} = 0$.

Also the capacitor C_{p1} can be chosen such that the parallel switching transistor is set to be at the optimum value as previously mentioned. In this case, after running the algorithm accordingly, we can generate the component values as below.

Table 5.8 : Computed actual element values of 3S-DPS topology in example 4.

Components	Actual Values	Channel Resistors	Actual Values	OFF State Capacitors	Actual Values
$L_{p1}(nH)$	0.2845	$R_{on1}(\Omega)$	7.4667	C_{off1}(fF)	90
$C_{p1}(nF)$	0.7101	$R_{on2}(\Omega)$	7.4667	C_{off2}(fF)	90
$L_{p2}(nH)$	2.0821	$R_{on3}(\Omega)$	7.4667	C_{off3}(fF)	90
$C_{p2}(fF)$	0	$R_{on4}(\Omega)$	21.226	C_{off4}(fF)	31.66

It should be noticed that, in the above design, the series arm capacitor C_{p2} is set to zero (i.e. $k_4 = 0$ chosen) and the off-state capacitor of switch 4 is found as $31.66\,fF$. Corresponding on state resistor is $R_{on4} = 21.22\Omega$. Obviously, this resistor introduces considerable amount of loss in State-B.

Phase performance of the 3S-DPS is depicted in Fig. 5.1. In Fig. 5.1, we can analyze the phase variations as a function of normalized angular frequency ω. At $\omega = 0$, in State-B, phase $\varphi_{21B}(\omega)$ jumps from -180^0 to $+180^0$. This sudden jump is due to the nature of the arctangent function and it may be interpreted as a discontinuity.

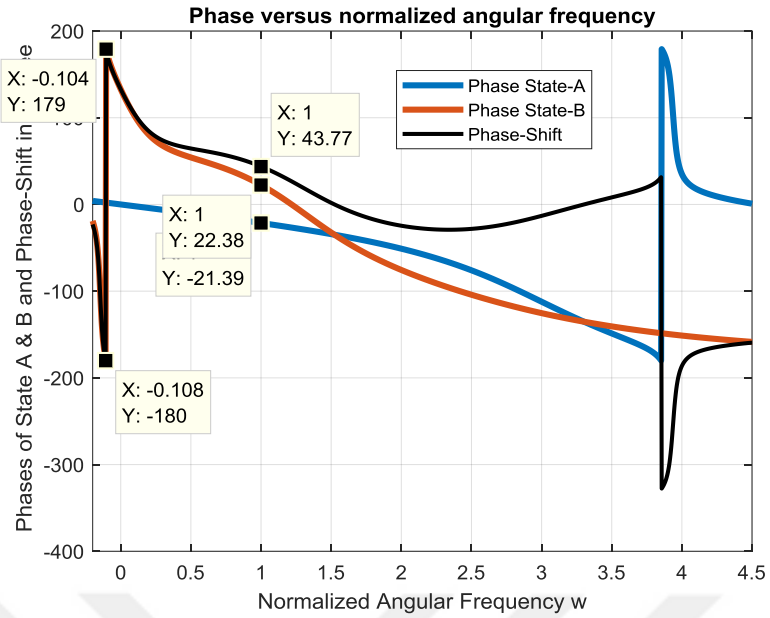


Figure 5.1 : Phase plots of 45^0 phase shifter for example 4.

However, $\mp 180^0$ are the same points on the phase plane. It is expected that at $\omega = 1$, leading phase of State-B should come down from $+180^0$ to $+22.5^0$. Also, close examination of Fig. 5.1 reveals that, at $\omega = 1$, the State-B phase $\varphi_{21B}(1) = +22.38^0$. The small discrepancy $\varepsilon_{\varphi_{21B}}(1) = 0.12$ is due to the losses of the switches, as expected. When we zoom into the phase curves of Fig. 5.2, the useful bandwidth may be selected from 0.9 to 1.1 (or equivalently 9 to 11 GHz). In this interval, it is found that the maximum phase for State-B is $\theta_{21B-max} = \theta_{21B}(0.9) = 30.7$ and minimum phase for State-B is $\theta_{21B-min} = \theta_{21B}(1.1) = 12.77$. In similar manner, maximum phase for State A is $\theta_{21A-max} = \theta_{21A}(0.9) = -19.08$ and minimum phase for state A is $\theta_{21A-min} = \theta_{21A}(1.1) = -23.77$. The zoomed phase performance of designed phase shifter is given in Fig . 5.2.

The average phase shift given is defined as

$$\theta_{AVP} = \left(\frac{\Delta\theta_{max} + \Delta\theta_{min}}{2}\right) \tag{5.9}$$

Also phase fluctuation ($\Delta\theta_\delta$) is defined as the phase difference between the actual phase ($\Delta\theta$) and average phase shift (θ_{AVP}) for a given frequency.

$$\Delta\theta = \theta_{AVP} \pm \Delta\theta_\delta \tag{5.10}$$

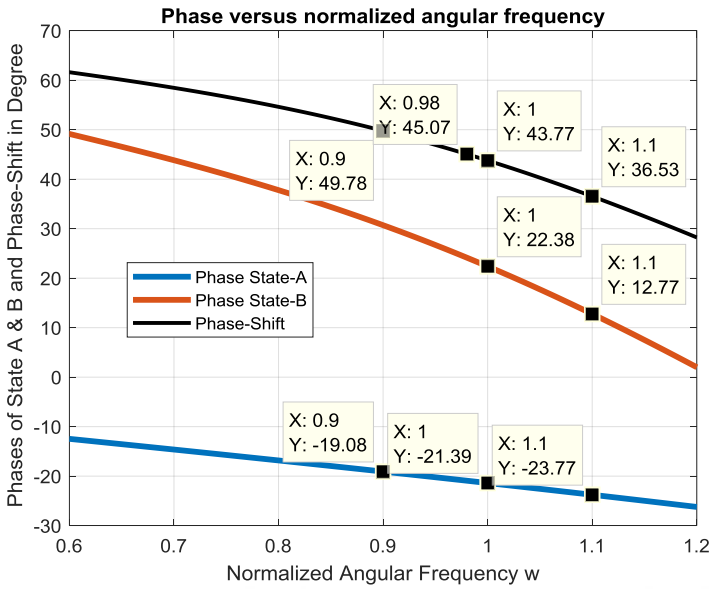


Figure 5.2 : Zoomed phase plots of 45^0 phase shifter in example 4.

The performance metrics of the desined 45^0 phase shifter is given.

Table 5.9 : Performance parameters of 3S-DPS with evenly phase distribution.

$\Delta\theta_{max}$	$\Delta\theta_{min}$	θ_{AVP}	Bandwidth	$\Delta\theta_{\delta}$	$\Delta\theta$
49.78^0	36.53^0	43.15^0	0.2 (2GHz)	6.63^0	$43.15^0 \pm 6.63^0$

Power transfer performance curves of 3S-DPS-45^0 is depicted in Fig. 5.3.

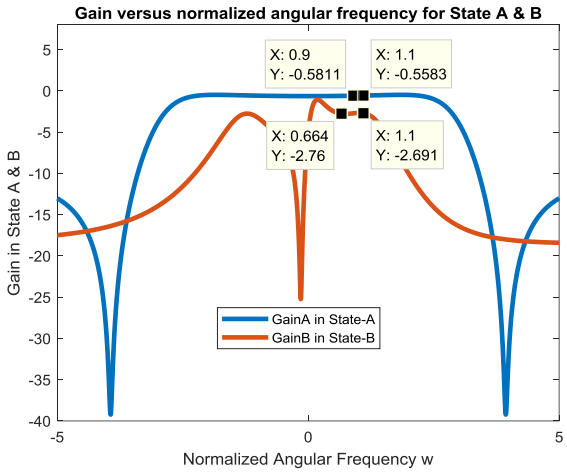


Figure 5.3 : Gain plots of 45^0 phase shifter in example 4.

In State-A, Transducer Power Gain (TPG) is almost flat and above -0.6 dB over a wide frequency band ($0 \leq \omega \leq 4$). In State-B, TPG is above -3 dB over one octave bandwidth ($0.6 \leq \omega \leq 1.2$). The zoomed version of the power transfer performance is given in Fig. 5.4.

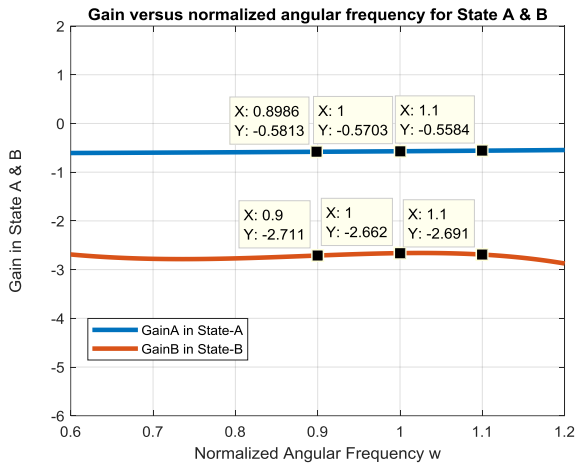


Figure 5.4 : Zoomed gain plots of 45^0 phase shifter in example 4.

Now, let us compare the above results for the case where the switches are perfect. In other words, ON mode channel resistors of NMOS switches are all zero. In fact, we completed this exercise in Example 1 and 2 and plot the results in Fig. 4.5, and Fig. 4.6.

For the ideal case, TPG for both states are 0 dB and the bandwidth is one octave from 0.6 to 1.2 (6 $GHz\ to\ 12\ GHz$).

As we observe from the above results that switch losses severely penalized the bandwidth and shrink it from [0.6-1.2] down to [0.9-1.1].

For the ideal case, in State-A,

$$\theta_{21A}(\omega) = -2\tan^{-1}(\omega L_1) \tag{5.11}$$

is always negative since it belongs to a lagging symmetrical all pass lattice section. Furthermore, the major design parameter μ_A is defined as

$$\mu_A = \tan\left[\frac{|\theta_{21A}(\omega_0)|}{2}\right] = \omega_0 L_1|_{\omega_0=1} = L_1 \tag{5.12}$$

or the series arm normalized-inductor L_1 and normalized-cross arm capacitor C_1 is given by

$$L_1 = \frac{1}{\omega_0}\tan^{-1}(\mu_A) = C_1 \tag{5.13}$$

and the function

$$f(\omega L_1) = -2\tan^{-1}(\omega L_1) \tag{5.14}$$

may be approximated by a straight line such that

$$y_A(\omega) = [\theta_{21A}(1)][\omega] \tag{5.15}$$

On the other hand, wild behavior of State-B phase response stems from the quasi hyperbolic behavior of

$$f\left(\frac{1}{\omega C_2}\right) = 2\tan^{-1}\left(\frac{1}{\omega C_2}\right) \tag{5.16}$$

which may be approximated by the hyperbola

$$f(\omega) = [\varphi_{21B}(1)]\left[\frac{1}{\omega}\right] \tag{5.17}$$

where C_2 represents the equivalent normalized-series arm capacitor evaluated at $\omega = 1$ and it is determined in terms of the major design parameter

$$\mu_B = \tan\left(\frac{\varphi_{21B}(1)}{2}\right) \tag{5.18}$$

such that

$$C_2 = \frac{1}{\mu_B} = L_2 \tag{5.19}$$

Similarly, in State-B, the function

$$f\left(\frac{1}{\omega C_2}\right) = 2\tan^{-1}\left(\frac{1}{\omega C_2}\right) \tag{5.20}$$

can be approximated by a shift line

$$y_B(\omega) = [\Delta\theta_0] - [\theta_{21A}(1)][\omega] \tag{5.21}$$

All the above phase functions and their approximations are depicted in Fig. 5.5 for $\Delta\theta_0 = 45^0$.

Close examination of Fig. 5.5 reveals the following practical rules.

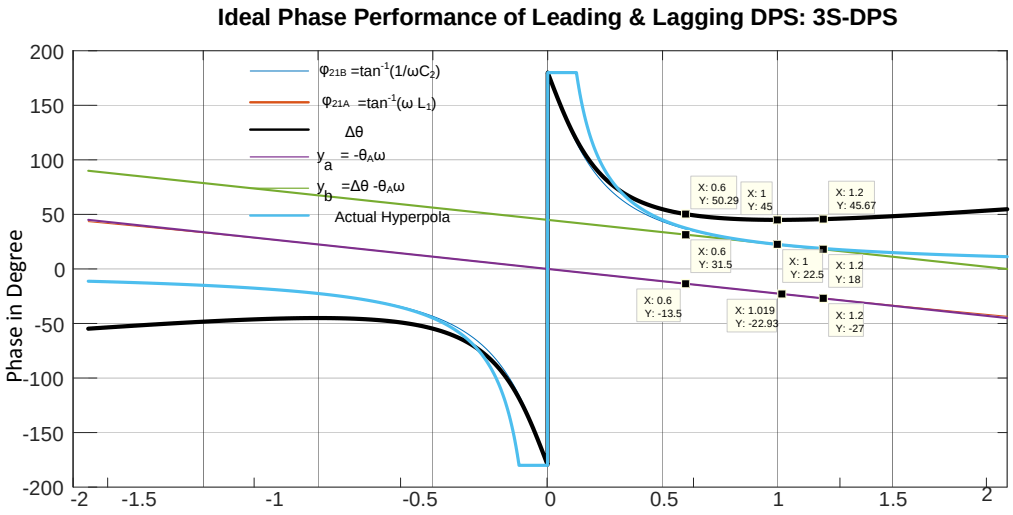


Figure 5.5 : Phase plots of $\Delta\theta(w) = 45^0$ for ideal 3S-DPS.

(a) In State-B, the function $f(\omega) = 2tan^{-1}\left(\frac{1}{\omega C_2}\right)$ pretty much traces the locus of the hyperbola given by $f(\omega) = [\varphi_{21B}(1)]\left[\frac{1}{\omega}\right]$; and both functions may be approximated by a straight line $y_B(\omega) = [\Delta\theta_0] - [\varphi_{21A}(1)][\omega]$ over a wideband such as $0.2 \leq \omega \leq 1.5$.

(b) In State-A, function $f(\omega) = -2tan^{-1}(\omega L_1)$ is a well behaved-smooth and it is closely approximated by a straight line $y_A(\omega) = [\varphi_{21A}(1)][\omega]$ over broadband $(-2 \leq \omega \leq +2)$.

(c) Due to quasi-hyperbolic behavior of $f(\omega) = 2tan^{-1}\left(\frac{1}{\omega C_2}\right)$, one would avoid utilizing the lower edge of the frequency axis ω in State-B, perhaps up $\omega = 0.1$.

(d) The useful frequency band can be selected in the region where the leading phase hyperbola overlaps with line $y_B(\omega)$ which secures the constant phase shift over line y_A.

Up to this point, we presume that, the phase shift $\Delta\theta_0$ is evenly distributed between the switching states. However, all the above points suggest that, if we work towards the high frequency end $(\omega > 0.5)$ of the hyperbolic function (i.e. in State-B) and distribute $\Delta\theta_0$ unevenly between the states, then we may have a chance to improve the phase range of 3S-DPS. In this regard, we may even consider moving the center frequency from unity to $\omega = 1 + \delta_\omega$ where δ_ω small positive number. Therefore, in the following section, we will investigate the effect of uneven distribution on the phase shift performance of 3S-DPS.

5.2.2 Design Algorithm of 3S-DPS for Uneven Phase Distribution between States

In State-A (ideal lagging symmetric phase section), the phase $\varphi_{21A}(\omega)$ is always a negative quantity. Let $\theta_A(\omega)$ be

$$\theta_A(\omega) = |\theta_{21A}(\omega)| = |-2tan^1(\omega L_1)| \geq 0;\ \forall\omega > 0 \tag{5.22}$$

and

$$\theta_{21A}(\omega) = -\theta_A(\omega) \leq 0;\ \forall\omega \tag{5.23}$$

Similarly, in State-B (ideal leading symmetric phase section) $\theta_{21B}(\omega)$ is always a positive quantity. For the sake of using balanced nomenclature, let $\theta_B(\omega)$ be

$$\theta_B(\omega) = \theta_{21B}(\omega) = 2tan^1\left(\frac{1}{\omega C_2}\right) \geq 0;\ \forall\omega \tag{5.24}$$

Then, the phase shift between State-B and State-A is given by

$$\Delta\theta(\omega) = \theta_{21B}(\omega) - \theta_{21A}(\omega) = \theta_B(\omega) + \theta_A(\omega) \tag{5.25}$$

or at $\omega = 1$, for specified $\Delta\theta_0$ and θ_{B0}, θ_{A0} is given by

$$\theta_{A0} = \Delta\theta_0 - \theta_{B0} > 0 \tag{5.26}$$

From the practical implementation point of view, all the switches are selected as NMOS transistor with actual on-state channel resistors $R_{ona(i)}$ and actual off-state capacitor $C_{offa(i)}$. Then, one can design an 3S-DPS using unevenly distributed phase shift as in the following algorithm.

Inputs:

Desired phase shift $\Delta\theta_0$ specified at the normalized centered frequency $\omega_0 = 1$.

θ_{B0}: Desired positive phase-shift of the leading symmetrical lattice structure (State-B)

Actual center frequency f_{0a}

Actual normalizing Resistor $R_a = 100\Omega$.

Optimum switch capacitor values $C_{off-opt}$ (for the $TSMC$ $0.18\mu m$ process it can be taken as $90fF$)

Computational Steps:

Step 1: Set θ_{A0} as $\theta_{A0} = \Delta\theta_0 - \theta_{B0} \geq 0$.

Step 2: Compute the major design parameters as $\mu_A = tand\left(\frac{\theta_A}{2}\right)$ and $\mu_B = tand\left(\frac{\theta_B}{2}\right)$ for State A & B respectively.

Step 3: Compute major component values for lagging and leading symmetrical LC lattice as

$$L_1 = \left(\frac{1}{\omega_0}\right)\mu_A = C_1 \tag{5.27}$$

and

$$C_2 = \left(\frac{1}{\omega_0}\right)\left(\frac{1}{\mu_B}\right) = L_2 \tag{5.28}$$

Step 4: Compute the actual major component values from normalized values.

Step 5: Compute the normalized value of the OFF-State Capacitor $C_{offa-opt}$

$$C_{off-opt} = (2\pi f_{0a})(RC_{offa-opt}) \tag{5.29}$$

Step 6: Compute NMOS switch sizes using the algorithm given in Table 5.2.

Step 7: Compute the switch control coefficients k_2 and k_4.

$$k_2 = \frac{C_{off-opt(2)}}{C_2} \tag{5.30}$$

$$k_4 = \frac{C_{off-opt(4)}}{C_1} \tag{5.31}$$

$$C_{off(2)} = k_2 C_2 \tag{5.32}$$

$$C_{off(1)} = k_4 C_1 \tag{5.33}$$

Step 8a: Compute the series arm capacitors C_{p1}

$$C_{p1} = C_2 - C_{off-opt(2)} \geq 0 \tag{5.34}$$

If C_{p1} is negative, then set $k_2 = 0$, $C_{p1} = 0$ and $C_{off(2)} = C_2$. Then, re-compute $R_{on(2)}$.

Step 8b: Compute the series arm capacitors C_{p2}.

$$C_{p2} = C_1 - C_{off-opt(4)} \geq 0 \tag{5.35}$$

If C_{p2} is negative, then set $k_4 = 0$, $C_{p2} = 0$ and $C_{off(4)} = C_1$. Then, re-compute $R_{on(4)}$.

Step 9: Compute the series arm inductors L_{p1}.

$$L_{p1} = \frac{L_1}{1 + \omega_0^2 L_1 C_{off(1)}} \tag{5.36}$$

Step 10: Compute the cross arm inductors L_{p2}.

$$L_{p2} = \frac{L_2}{1 + \omega_0^2 L_2 C_{off(3)}} \tag{5.37}$$

Step 11: Calculate actual impedances using normalized values.

Then, the designed circuit model performance can be investigated and performance parameters can be calculated and plotted.

Let us design a 45^0 phase shifter using the uneven design algorithm. For this design, we have freedom to choose State-B phase of $\theta_{B0} = 40^0$, State-A phase of $\theta_{B0} = 5^0$ and $C_{off-opt} = 90\ fF$.

After computing the actual component values with the switch model parameters R_{on} and C_{off} are computed. The actual component values with the switch model parameters R_{on} and C_{off} are given in Table 5.10.

Table 5.10 : Components of 3S-DPS ($\Delta\theta_0$=45^0 and $\Delta\theta_{B0}$=5^0) at 10 GHz.

Components	Actual Values	Channel Resistors	Actual Values	OFF State Capacitors	Actual Values
$L_{p1a}(nH)$	0.4804	$R_{on1}(\Omega)$	7.4667	C_{off1}(fF)	90
$C_{p1a}(pF)$	3.5552	$R_{on2}(\Omega)$	7.4667	C_{off2}(fF)	90
$L_{p2a}(nH)$	2.6127	$R_{on3}(\Omega)$	7.4667	C_{off3}(fF)	90
$C_{p2a}(fF)$	0	$R_{on4}(\Omega)$	11.600	C_{off4}(fF)	57.93

After computing the values using the design algorithm, the phase performance is given in Fig. 5.6.

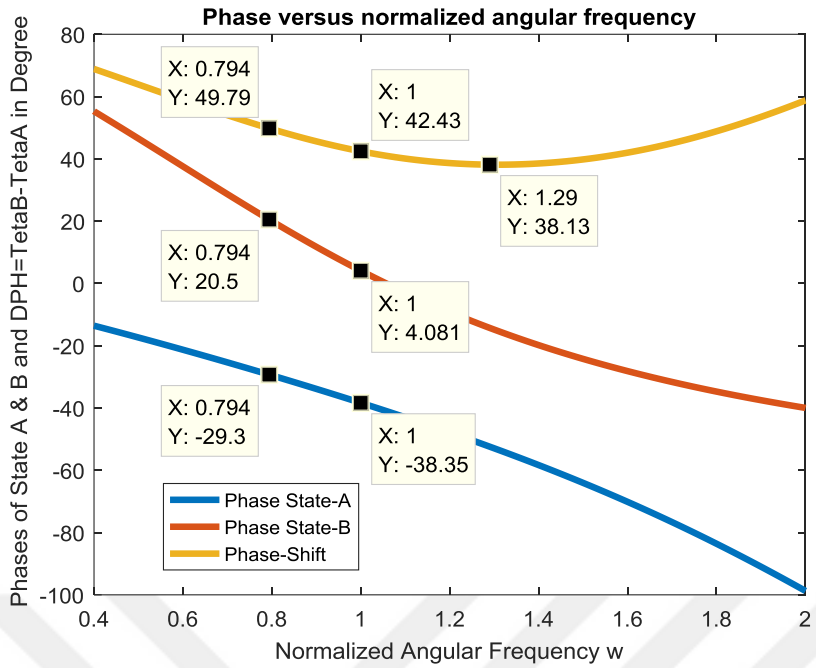


Figure 5.6 : Phase performance of $45^0$3S-DPS with switch models.

The phase performance summary is given in Table 5.11.

Table 5.11 : Performance parameters of 3S-DPS with uneven phase distribution.

$\Delta\theta_{max}$	$\Delta\theta_{min}$	θ_{AVP}	Bandwidth	$\Delta\theta_{\delta}$	$\Delta\theta$
49.79^0	38.13^0	42.96^0	0.496 (4.96GHz)	6.83^0	$42.96^0 \pm 6.83^0$

The power transfer response of the new design is depicted in Fig. 5.7.

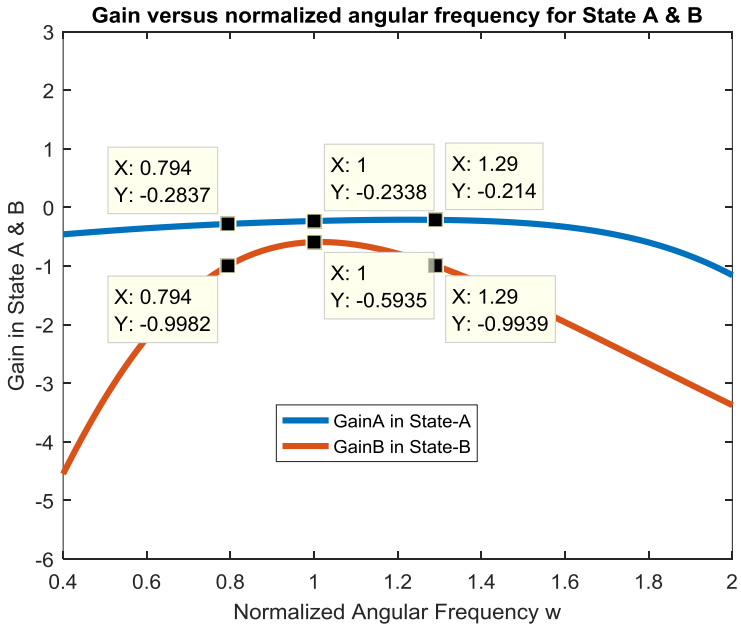


Figure 5.7 : Gain performance of $45^0$3S-DPS with switch models.

In State-A loss performance is smooth and TPG is above -0.6 dB even beyond $\omega = 1.29$. State-B performance is above -1 dB up to $\omega = 1.29$.

At this point, it is necessary to compare the introduced two algorithms, evenly phase distributed 3S-DPS design algorithm and unevenly phase distributed 3S-DPS design algorithm as in Table 5.12.

Table 5.12 : Comparison between even and uneven phase distributed 3S-DPS.

Design Parameters	3S-DPS Design Algorithm with Uneven Phase Distribution	3S-DPS Design Algorithm with Even Phase Distribution
Center Frequency	10 GHz	10 GHz
Target Phase Shift	45^0	45^0
State-A Phase Shift	5^0	22.5^0
State-B Phase Shift	40^0	22.5^0
Average Phase Shift	42.96^0	43.15^0
Phase Fluctuation	$\pm 6.83^0$	$\pm 6.63^0$
Bandwidth	4.96 GHz	2 GHz
Minimum TPG in State-A	-0.293 dB	-0.57 dB
Minimum TPG in State-B	-0.99 dB	-2.79 dB

Close examination of Table 5.12 reveals that digital phase shifter designed with uneven phase distribution provides superior frequency bandwidth over the one designed with even phase distribution.

5.3 Design Algorithm of 3S-DPS with Practical Switches Introducing Losses

So far, element values of an 3S-DPS is estimated using the ideal switches with no loss. In State-B, this approach theoretically yields always a positive leading phase $\theta_{21B}(\omega) \geq 0$.

However, in practice, lossy switches may result in negative $\theta_{21B}(\omega)$ as the frequency becomes large enough as depicted in Fig. 5.6.

In this section, we introduce a method to estimate the component values of a practical 3S-DPS for which all the switches include losses. In this way, we may further increase the bandwidth of an 3S-DPS working in the smooth region of the quasi-hyperbolic phase curve of State-B.

In the following derivations, first, we drive the series arm components L_{P1} and C_{P1}. Then, the cross-arm impedance components L_{P2} and C_{P2} are determined.

Referring to Fig. 4.10 and Fig. 4.11, in State-B, transfer scattering parameter $S_{21B}(j\omega)$ is given in terms of the series arm impedance Z_{aB} such that

$$S_{21B}(j\omega) = \frac{1 - z_{aB}}{1 + z_{aB}} = \rho_{21B}(\omega)e^{j\varphi_{21B}(\omega)} \tag{5.38}$$

provided that

$$z_{bB} = \frac{1}{z_{aB}} \tag{5.39}$$

The series arm impedance z_{aB} can be expressed as

$$z_{aB}(j\omega) = R_{aB}(\omega) + jX_{aB}(\omega) \tag{5.40}$$

where

$$R_{aB}(\omega) = \frac{\omega^2 R_{on1} L_{p1}^2}{R_{on1}^2 + \omega^2 L_{p1}^2} \tag{5.41}$$

and

$$X_{aB}(\omega) = \beta(\omega) - \frac{1}{\omega\left(C_{p1} + C_{off2}\right)} \tag{5.42}$$

and

$$\beta(\omega) = \frac{\omega R_{on1}^2 L_{p1}}{R_{on1}^2 + \omega^2 L_{p1}^2} > 0 \tag{5.43}$$

On the other hand, in State-A operation, the series arm inductors $L_{p1}$is given by

$$L_{p1} = \frac{L_1}{1 + \omega_0^2 L_1 C_{off1}} \tag{5.44}$$

where L_1 is computed for a specified lagging phase $\varphi_{21A}(\omega_0) = -\theta_A < 0$ of State-A or equivalently $\mu_A = tan(\theta_A) > 0$ as in (51) such that

$$L_1 = \frac{1}{\omega_0} tan^{-1}(\mu_A) = C_1 > 0 \tag{5.45}$$

Going back to State-B operation,

$$S_{21B}(j\omega) = \frac{(1 - R_{aB}) - jX_{aB}}{(1 + R_{aB}) + jX_{aB}} = \rho_{21B} e^{j\theta_{21B}} \tag{5.46}$$

where

$$\rho_{21B}^2(\omega) = \frac{(1 - R_{aB})^2 + X_{aB}^2}{(1 + R_{aB})^2 + X_{aB}^2} \tag{5.47}$$

Let

$$\theta_{1B} = tan^{-1}\left(\frac{X_{aB}}{1 - R_{aB}}\right) \tag{5.48}$$

and

$$\theta_{2B} = tan^{-1}\left(\frac{X_{aB}}{1 + R_{aB}}\right) \tag{5.49}$$

Then, the phase θ_{21B} of the transfer scattering parameter S_{21B} is expressed by means of θ_{1B} and θ_{2B} such that

$$\theta_{21B}(\omega) = \theta_{1B}(\omega) - \theta_{2B}(\omega) \tag{5.50}$$

Let $\mu_{1B} = tan(\theta_{1B})$. Then,

$$\mu_{1B} = tan(\theta_{1B}) = -\frac{X_{aB}}{1 - R_{aB}} = \frac{X_{aB}}{R_{aB} - 1} \tag{5.51}$$

Let $\mu_{2B} = tan(\theta_{2B})$. Then,

$$\mu_{2B} = tan(\theta_{2B}) = +\frac{X_{aB}}{1 + R_{aB}} = \frac{X_{aB}}{R_{aB} + 1} \tag{5.52}$$

Employing the trigonometric identity for $tan[\theta_{1B}(\omega) - \theta_{2B}(\omega)]$, we can write,

$$tan[\theta_{21B}(\omega)] = tan[\theta_{1B}(\omega) - \theta_{2B}(\omega)] = \frac{tan(\theta_{1B}) - tan(\theta_{2B})}{1 + \tan(\theta_{1B})tan(\theta_{2B})} \tag{5.53}$$

$$tan[\theta_{21B}(\omega)] = \frac{\mu_{1B} - \mu_{2B}}{1 + \mu_{1B}\mu_{2B}} \tag{5.54}$$

Let

$$\gamma_B = tan(\theta_B) \tag{5.55}$$

where

$$\theta_B = \theta_{21B}(\omega_0) \tag{5.56}$$

It is noted that θ_B may take positive or negative values depending on the selected frequency ω_0. Then, at a specified frequency ω_0,

$$\gamma_B = tan(\theta_B) = \frac{\frac{X_{aB}}{R_{aB}-1} - \frac{X_{aB}}{R_{aB}+1}}{1 + \frac{X_{aB}}{R_{aB}-1}\frac{X_{aB}}{R_{aB}+1}} = \frac{2X_{aB}}{(R_{aB}^2 - 1) + X_{aB}^2} \tag{5.57}$$

or

$$\gamma_B X_{aB}^2 - 2X_{aB} + \gamma_B(R_{aB}^2 - 1) = 0 \tag{5.58}$$

Solution of (5.58) yields two distinct X_{aB} namely $X_{aB,1}$ and $X_{aB,2}$ such that

$$X_{aB,1} = \frac{1 + \sqrt{1 - \gamma_B^2(R_{aB}^2 - 1)}}{\gamma_B} \tag{5.59}$$

and

$$X_{aB,2} = \frac{1 - \sqrt{1 - \gamma_B^2(R_{aB}^2 - 1)}}{\gamma_B} \tag{5.60}$$

Notice that the discriminant of the above equations must be always non-negative to end up with real solutions. In other words,

$$\Delta = 1 - \gamma_B^2(R_{aB}^2 - 1) \geq 0 \; or \; \gamma_B^2(R_{aB}^2 - 1) \leq 1 \tag{5.61}$$

Once $X_{aB}(\omega_0)$ is found, for a selected C_{off2}, C_{p1} is computed as follows.

$$X_{aB} = \beta(\omega_0) - \frac{1}{\omega_0(C_{p1} + C_{off2})} \tag{5.62}$$

$$\frac{1}{\omega_0(C_{p1} + C_{off2})} = \beta(\omega_0) - X_{aB} \tag{5.63}$$

Thus,

$$C_{p1} = \frac{1}{\omega_0[\beta(\omega_0) - X_{aB}]} - C_{off2} \geq 0 \tag{5.64}$$

The following remarks are found helpful for the designers.

Remarks:

a) The above formulations cover both positive and negative values of θ_B which is equivalent of having either positive or negative $\gamma = \tan(\theta_B)$.

b) Close examination of (5.59) and (5.60) reveals that if θ_B is selected as a positive quantity, then we must choose the solution which gives negative value for X_{aB} which in turn results in positive value for $X_{bB} = -\frac{1}{X_{aB}}$. On the other hand, if we start the design with negative value of θ_B then, positive value solution for X_{aB} must be selected which yields negative value for $X_{bB} = -\frac{1}{X_{aB}}$. These choices are mandatory to end up with realizable component values for the 3S-DPS topology.

c) Solution of the above equations to compute the unknown components $\{L_{p1},\ C_{p1}, L_{p2}, C_{p2}\}$ values are not exact. For the sake of simplicity, component values for $\{L_1, C_1\}$ and $\{L_2, C_2\}$ pairs are computed for the ideal switches. However, imaginary part X_{aB} of $Z_{aB} = R_{aB} + jX_{aB}$ is determined for the switches with on-mode channel resistors. Therefore, at the end of the explicit solutions, one may optimize the performance of the 3S-DPS unit for the target phase shift $\Delta\theta$ while minimizing the overall loss of State-A and B over the frequency band of operation. The optimization can be done manually.

d) Equation (5.64) must yield a positive C_{p1}. If this is not the case, the designer can set it to zero (i.e. $C_{p1} = 0$). In this regard, switch (S2) must be redesigned in such a way that $C_{off2} = C_2$ which in turn yields a positive $\theta_B = \theta_{21B}(\omega_0) > 0$. Hence, at the beginning of the computations, θ_B must be selected as a positive quantity, perhaps it is selected as a sufficiently small to have State-B phase curve to operate in the smooth phase region.

e) If Δ is positive, $X_{aB,i}$ of (5.61) could be either positive or negative. If we start designing the 3S-DPS unit from the series arm components using X_{aB}, then

(5.64) yields $C_2 = \frac{1}{\omega_0[\beta(\omega_0)-X_{aB}]} = C_{p1} + C_{off2} = L_2 > 0$. In this regard, $\beta(\omega_0)$ of (5.43) is always positive. Therefore, X_{aB} must be a negative quantity to yield positive $C_2 = L_2$. Hence, these computations demands a positive $\theta_B = \theta_{21B}(\omega_0)$.

f) In order to obtain a wide phase range over a broad frequency band, phase shift $\Delta\theta$ must be unevenly distributed between the states. As indicated above, phase of State-B may be selected small enough to have State-B phase operation in the smooth region of the phase curve. For example, for a $\Delta\theta = 45^0$ phase shift, if State-A phase $\theta_{21A}(\omega_0)$ is selected as -40^0 $(i.e.\theta_A = 40^0)$, State-B phase becomes $\theta_{21B}(\omega_0) = \theta_B = 5^0$ which corresponds to 12.5% of θ_A which may be considered as sufficiently small enough.

At this point, for State-B, we must determine cross arm impedance component values L_{p1} and C_{p2} when the all pass condition is satisfied. In this case, the cross arm impedance is given by

$$Z_{bB} = \frac{1}{Z_{aB}} = \frac{1}{R_{aB} + jX_{aB}} = \frac{R_{aB}}{R_{aB}^2 + X_{aB}^2} - j\frac{X_{aB}}{R_{aB}^2 + X_{aB}^2} \tag{5.65}$$

where

$$R_{bB} = \frac{R_{aB}}{R_{aB}^2 + X_{aB}^2} \tag{5.66}$$

And if R_{aB} is small enough, then,

$$X_{bB} = -\frac{X_{aB}}{R_{aB}^2 + X_{aB}^2} \cong -\frac{1}{X_{aB}} > 0 \tag{5.67}$$

On the other hand, the cross-arm impedance Z_{bB} is specified as

$$Z_{bB} = j\left[\frac{\omega L_{P2}}{1 - \omega^2 L_{p2} C_{off3}}\right] + \frac{R_{on4}}{1 + j\omega R_{on4} C_{P2}} \tag{5.68}$$

$$Z_{bB} = \frac{R_{on4}}{1 + \left(\omega R_{on4} C_{p2}\right)^2} + j\left[\frac{\omega L_{P2}}{1 - \omega^2 L_{P2} C_{off3}} - \frac{\omega R_{on4}^2 C_{p2}}{1 + \left(\omega R_{on4} C_{p2}\right)^2}\right] \tag{5.69}$$

where

$$R_{bB}(\omega) = \frac{R_{on4}}{1 + \omega^2 R_{on4}^2 C_{P2}^2} \tag{5.70}$$

and

$$X_{bB} = \omega \left[\frac{L_{P2}}{1 - \omega^2 L_{P2} C_{off3}} - \frac{R_{on4}^2 C_{p2}}{1 + \left(\omega R_{on4} C_{p2}\right)^2} \right] \tag{5.71}$$

which is computed by (5.70). Thus, at $\omega = \omega_0$, (5.71) results in

$$C_{p2} = \left[\frac{1}{\omega_0 R_{on4}} \right] \left[\sqrt{\frac{R_{on4} - R_{bB}(\omega_0)}{R_{bB}(\omega_0)}} \right] \geq 0 \tag{5.72}$$

In (5.71), if C_{p2} becomes negative, it is appropriate to set it to zero. On the other hand, for State-A, C_{P2} must approximately satisfy (4.29) such that

$$C_{p2} = C_1 - C_{off4} = \mu_A - C_{off4} \geq 0 \tag{5.73}$$

Obviously, if (5.70), (5.71) and (5.72) are not co-incidentally satisfied, it is difficult to have identical C_{p2} out of (5.70), (5.71) and (5.72).

Upon designer's choice, C_{p2} can be set to zero to minimize the overall loss of the phase shifter. If $C_{p2} = 0$ then, switch 4 (S4) must be redesigned in such a way that, off-mode capacitor C_{off4} is equal to C_1 (i.e. $C_{off4} = C_1$). In this state $\theta_{21A}(\omega_0)$ is always negative.

Similarly, (5.69) dictates that

$$X_{bB}(\omega) = \frac{\omega L_{p2}}{1 - \omega^2 L_{p2} C_{off3}} - \omega\alpha(\omega) \tag{5.74}$$

where

$$\alpha(\omega) = \frac{\omega R_{on4}^2 C_{p2}}{1 + \left(\omega R_{on4} C_{p2}\right)^2} \tag{5.75}$$

where X_{bB} is already known by (5.67). Thus, for negligible R_{on4} or $\alpha(\omega_0)$ at a specified ω_0, desired cross arm inductor L_{p2} is found as follows.

$$L_{p2} = \frac{[X_{bB}(\omega_0) + \omega_0\alpha(\omega_0)]}{\omega_0\{1 + \omega_0[X_{bB}(\omega_0) + \omega_0\alpha(\omega_0)]C_{off3}\}} \cong \frac{X_{bB}(\omega_0)}{\omega_0[1 + \omega_0 X_{bB}(\omega_0)C_{off3}]} \tag{5.76}$$

Based on the above derivations, one can design a 3S-DPS for a specified $\theta_B = \theta_{21B}(\omega_0) > 0$ using the following algorithm.

Inputs:

Desired phase shift $\Delta\theta_0$ specified at the normalized centered frequency $\omega_0 = 1$.

θ_{B0}: Desired positive phase-shift of the leading phase shift symmetrical lattice structure (State-B).

Actual center frequency f_{0a}.

Actual normalizing Resistor $R_a = 100\Omega$.

All switch capacitor values starts with $C_{off1,2,3,4} = C_{offopt}$. And for TSMC 0.18µm process, we have freedom to choose C_{offopt} as 90 fF.

Computational Steps:

Step 1: Set θ_{A0} as $\theta_{A0} = \Delta\theta_0 - \theta_{B0} \geq 0$.

Step 2: Compute normilized capacitances C_{off1} and C_{off2}.

$$C_{off1} = (2\pi f_{01})R_a C_{off1a} \tag{5.77}$$

$$C_{off2} = (2\pi f_{01})R_a C_{off2a} \tag{5.78}$$

Step 3: Compute actual ON state channel resistors R_{on1a} and R_{on2a} and their normalized values $R_{on1}$and R_{on2} respectively.

$$R_{on1a} = \frac{672(fF \times ohm)}{C_{off1a}(fF)} \tag{5.79}$$

$$R_{on2a} = \frac{672(fF \times ohm)}{C_{off2a}(fF)} \tag{5.80}$$

and

$$R_{on1} = R_{on1a}/R_a \tag{5.81}$$

$$R_{on2} = R_{on2a}/R_a \tag{5.82}$$

Step 4: Compute μ_A, γ_B, L_1 and L_{p1}.

$$\mu_A = tand\left(\frac{\theta_A}{2}\right) > 0 \tag{5.83}$$

$$\gamma_B = tan(\theta_B) \tag{5.84}$$

$$L_1 = \mu_A/\omega_0 \tag{5.85}$$

$$C_1 = L_1 \tag{5.86}$$

$$L_{p1} = \frac{L_1}{1 + \omega_0^2 L_1 C_{off1}} \tag{5.87}$$

Step 5: Compute $R_{aB}(\omega_0)$ and $\beta(\omega_0)$.

$$R_{aB}(\omega_0) = \frac{\omega_0^2 R_{on1} L_{p1}^2}{R_{on1}^2 + \omega_0^2 L_{p1}^2} > 0 \tag{5.88}$$

$$\beta(\omega_0) = \frac{\omega_0 R_{on1}^2 L_{p1}}{R_{on1}^2 + \omega_0^2 L_{p1}^2} > 0 \tag{5.89}$$

Step 6: Solve equation (5.58) to generate $X_{aB}(\omega_0)$.

$$X_{aB,1} = \frac{1 + \sqrt{1 - \gamma_B^2(R_{aB}^2 - 1)}}{\gamma_B} \tag{5.90}$$

$$X_{aB,2} = \frac{1 - \sqrt{1 - \gamma_B^2(R_{aB}^2 - 1)}}{\gamma_B} \tag{5.91}$$

At this point, we must check if $X_{aB,1}$ and $X_{aB,2}$ are real. If yes, then we have to check if they are positive or negative. For the case $\theta_B$is negative, positive value of X_{aB} is selected.

Step 7: Compute C_{p1} as in equation (5.64).

$$C_{p1} = \frac{1}{\omega_0[\beta(\omega_0) - X_{aB}]} - C_{off2} \geq 0 \tag{5.92}$$

In this step, check if C_{p1} is positive. If not, set $C_{p1} = 0$, then redesign switch S2 by setting

$$C_{off2} = \frac{1}{\omega_0[\beta(\omega_0) - X_{aB}]} \tag{5.93}$$

and

$$C_{off2a} = \frac{C_{off2}}{2 \times \pi \times f_{0a} \times R} \tag{5.94}$$

The actual channel resistor is given by

$$R_{on2a} = \frac{672 \times 10^{-15}}{C_{off2a}} \tag{5.95}$$

And its normilized value

$$R_{on2} = \frac{R_{on2a}}{R} \tag{5.96}$$

Step 8: Compute R_{bB} and X_{bB} as in equation (5.66).

$$R_{bB} = \frac{R_{aB}}{R_{aB}^2 + X_{aB}^2} \tag{5.97}$$

And if $R_{aB}$is small enough, then

$$X_{bB} = -\frac{X_{aB}}{R_{aB}^2 + X_{aB}^2} \cong -\frac{1}{X_{aB}} \tag{5.98}$$

Step 9: Compute C_{p2}.

$$C_{p2,I} = \left[\frac{1}{\omega_0 R_{on4}}\right]\left[\sqrt{\frac{R_{on4} - R_{bB}}{R_{bB}}}\right] \geq 0 \tag{5.99}$$

Check the result using equation (5.73)

$$C_{p2,II} = C_1 - C_{off4} = \mu_A - C_{off4} \geq 0 \tag{5.100}$$

Decide if C_{p2} is acceptable. If not, it is always preferable to select $C_{p2} = 0$ which in turn yields

$$C_{off4} = C_1 = \frac{1}{\omega_0}\mu_A = \tan(\theta_A)\,;\ \omega_0 = 1 \tag{5.101}$$

We re-design switch S4. In this case, off state actual switch capacitor is given by

$$C_{off4a} = \frac{C_1}{2 \times \pi \times f_{0a} \times R} \tag{5.102}$$

In this case, actual channel resistor of S4 is specified by

$$R_{on4a} = \frac{672 \times 10^{-15}}{C_{off4a}} \tag{5.103}$$

And its normalized value is

$$R_{on4} = \frac{R_{on4a}}{R_a} \tag{5.104}$$

Step 10: Compute L_{p2} as in equation (5.75).

$$L_{p2} = \frac{X_{bB}}{\omega_0\left(1 + \omega_0 X_{bB} C_{off3}\right)} \tag{5.105}$$

Step 11: Compute actual element values L_{p1a}, L_{p2a}, C_{p1a} and C_{p2a}.

$$L_{p1a} = \frac{L_{p1}R}{2 \times \pi \times f_{0a}} \tag{5.106}$$

$$L_{p2a} = \frac{L_{p2}R}{2 \times \pi \times f_{0a}} \tag{5.107}$$

$$C_{p1a} = \frac{C_{p1}}{2 \times \pi \times f_{0a} \times R} \tag{5.108}$$

$$C_{p2a} = \frac{C_{p2}}{2 \times \pi \times f_{0a} \times R} \tag{5.109}$$

This step completes the algorithm. At this point, we can clarify the algorithm steps and its performance with an example.

Example 5.

Let us design a phase shifter using 3S-DPS topology for phase shift of 45^0 at the center frequency of $f_{0a} = 8\ GHz$. Take $\theta_B = -10^0$ and $\theta_A = 55^0$. Also assume the optimum capacitors for switches to be $C_{off2a,3a,4a} = 90\ fF$ and $C_{off1a} = 25\ fF$.

Answer:

Step 1: θ_A and θ_B are given as input.

Step 2: Normalized NMOS off capacitances are found $C_{off1} = 0.1257$ and $C_{off2,3,4} = 0.4524$.

Step 3: Normalized NMOS resistances are found $R_{on1} = 0.2688$ and $R_{on2,3,4} = 0.0747$.

Step 4: Major design parameters are $\mu_A = 0.5206$, $L_1 = C_1 = 0.5206$, $L_{p1} = 0.4886$.

Step 5: Using L_{p1} and R_{on1}, $R_{aB} = 0.2063$ and $\beta = 0.1135$.

Step 6: Major design parameter of State-B $\gamma_B = -0.1763$.

Step 7: Using γ_B and R_{aB} we can find $X_{aB,1} = -11.4264$ and $X_{aB,2} = 0.0838$.

Step 8: We choose positive Using γ_B and R_{aB} we can find $X_{aB,1} = -11.4264$ and $X_{aB,2} = 0.0838$.

Step 9: Using the algorithm, $C_{p2} = 0.0682$ is calculated which can be chosen as 0.

Step 10: Cross arm inductor can be calculated as $L_{p2} = 2.7130$.

Step 11: The actual element values together with the switch parameters are given in Table 5.13.

Table 5.13 : Component values of 3S-DPS for $\Delta\theta_0=45^0$ of example 5.

Components	Actual Values	Channel Resistors	Actual Values	OFF State Capacitors	Actual Values
$L_{p1a}(nH)$	0.9720	$R_{on1}(\Omega)$	26.880	C_{off1}(fF)	25
$C_{p1a}(pF)$	6.6018	$R_{on2}(\Omega)$	7.4667	C_{off2}(fF)	90
$L_{p2a}(nH)$	5.3973	$R_{on3}(\Omega)$	7.4667	C_{off3}(fF)	90
$C_{p2a}(fF)$	13.568	$R_{on4}(\Omega)$	7.4667	C_{off4}(fF)	90

Remark:

Ideally, symmetrical lattice structures used in phase shifter designs are lossless. In this regard, phase of the transfer scattering parameter is determined directly from the reactive parts of the series or cross arm impedances of the symmetric lattice. In practice, to make computations simpler, target phases are determined directly from the reactive parts of the impedances which in turn results in the component values of the phase shifter. Inclusion of the real parts of the impedances, mostly effects the insertion loss characteristics of the phase shifter under consideration. Therefore, we have experienced that, in Step 7, in determining X_{bB} from X_{aB}, the form $X_{bB} \cong -\frac{1}{X_{aB}}$ yields better phase-shift performance than that of the form $X_{bB} = -\frac{R_{aB}^2}{R_{aB}^2+X_{aB}^2}$. Anyhow, these forms converge to each other as R_{aB} approaches to zero.

The graphical representations of the designed 3S-DPS model performance is shown in below. The phase preformance over frequency is in Fig. 5.8.

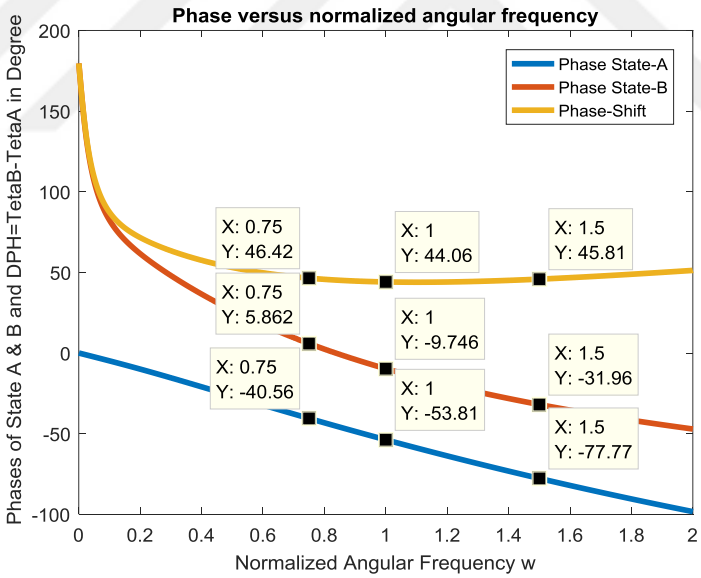


Figure 5.8 : Phase performance of $45^0$3S-DPS in example 5.

From Fig. 5.8, the relative phase error is read as

$$\delta_{\theta 0} = \frac{\Delta\theta_r - \Delta\theta_0}{\Delta\theta_0} = \frac{44.6 - 45}{45} = \frac{0.6}{45} = 1.33\% \qquad (5.110)$$

which is pretty good. At the input, the center frequency is located at $f_{0a} = 8\,GHz$ which corresponds to normalized angular frequency $\omega_0 = 1$.

From $f_1 = 0.75 * f_{0a} = 6\ GHz$ to $f_2 = 1.5 * f_{0a} = 12\ GHz$ the phase variation is given by $\Delta\theta = 45.24^0 \pm 1.18^0$. The loss characteristics of State-A and State-B is shown in Fig. 5.9.

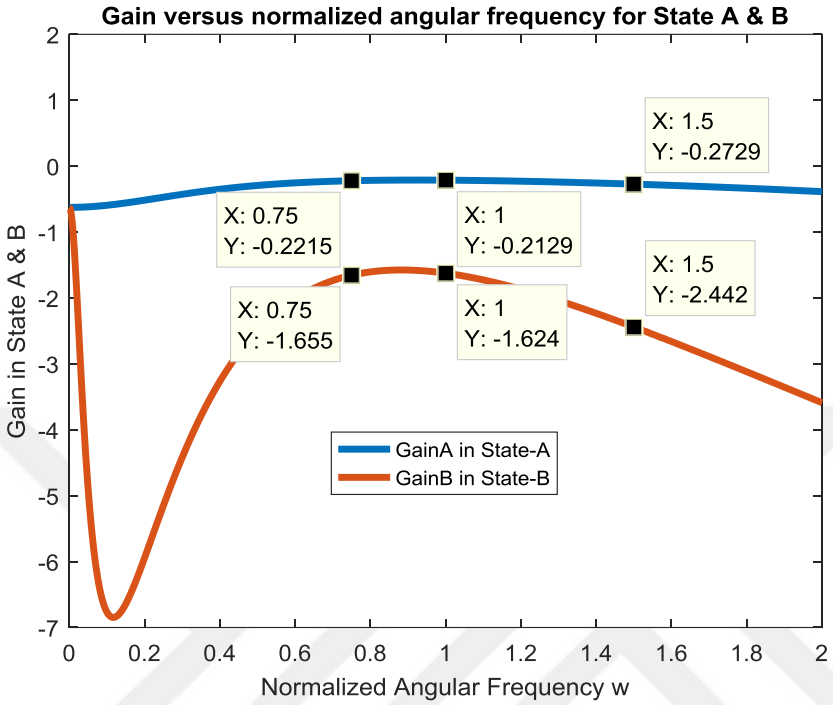


Figure 5.9 : Gain performance of $45^0$3S-DPS in example 5.

Close examination of the above figure reveals that over the frequency band of $\Delta F = 0.75 * 87 - 1.5 * 8\ GHz = 6\ GHz - 12\ GHz = 6\ GHz$, insertion loss for both states are above -2.5 dB which may be acceptable for many applications which requires insertion loss better than -3 dB.

In conclusion, we have exhibited that, the phase shifting performance of the 3S-DPS for uneven phase distribution between the states results in wider frequency band with less phase fluctuations over the same topology which performs even phase distributions between the states. In return, the new circuit yields relatively higher insertion loss in State-B. In the next part, an alternative approach of designing 3S-DPS topology with practical switch losses is introduced.

5.4 Design Algorithm of 3S-DPS with Practical Switches Introducing Losses: An Alternative Approach

In this section, we initiate the design of an 3S-DPS starting from the cross-arm impedance z_{bB} in State-B.

Let us consider S_{21B} for an all pass lattice structure.

$$S_{21B} = \frac{z_{bB} - 1}{z_{bB} + 1} \tag{5.111}$$

In (5.111), Z_{bB} is the normalized cross-arm impedance of the 3S-DPS in State-B and it is specified in terms of its real and imaginary parts as follows.

$$z_{bB} = R_{bB} + jX_{bB} \tag{5.112}$$

where R_{bB} is the real part and X_{bB} is the imaginary part of Z_{bB}.

Hence,

$$S_{21B} = \frac{R_{bB} + jX_{bB} - 1}{R_{bB} + jX_{bB} + 1} = \rho_{21B}(\omega)e^{j\varphi_{21B}(\omega)} \tag{5.113}$$

with

$$\theta_{21B}(\omega) = -\theta_B = \mp 180 - tan^{-1}\left(\frac{X_{bB}}{1 - R_{bB}}\right) - tan^{-1}\left(\frac{X_{bB}}{1 + R_{bB}}\right) \tag{5.114}$$

In (5.114), the phase θ_B is a positive quantity and it varies from $+0^0$ to $+180^0$. It is noted that, in the above expression " -1 " is represented by $e^{\mp j180^0}$. If $R_{bB} \ll 1$, then

$$-\theta_B \cong \mp 180 - 2tan^{-1}(X_{bB}) \tag{5.115}$$

or

$$tan^{-1}(X_{bB}) \cong \frac{\theta_B}{2} \mp 90^0 \leq 0 \tag{5.116}$$

or

$$X_{bB} \cong tan\left(\frac{\theta_B}{2} \mp 90^0\right) = -\frac{1}{tan\left(\frac{\theta_B}{2}\right)} = -\frac{1}{\mu_B} \leq 0 \tag{5.117}$$

where

$$\mu_B = tan\left(\frac{\theta_B}{2}\right) \tag{5.118}$$

On the other hand, by (5.71)

$$X_{bB}(\omega) = \omega\left[\frac{L_{p2}}{1-\omega^2 L_{p2}C_{off3}} - \alpha(\omega)\right] \tag{5.119}$$

where

$$\alpha(\omega) = \frac{R_{on4}^2 C_{p2}}{1+\left(\omega R_{on4}C_{p2}\right)^2} > 0 \tag{5.120}$$

In (5.120), on-mode channel resistance R_{on4} can be considered small enough so that $\alpha(\omega)$ is neglected as compared to $\frac{L_{p2}}{1-\omega^2 L_{p2}C_{off3}}$. Hence, $X_{bB}(\omega)$ is approximated as

$$X_{bB}(\omega) \cong \omega\left[\frac{L_{p2}}{1-\omega^2 L_{p2}C_{off3}}\right] \tag{5.121}$$

or at $\omega = \omega_0$

$$L_{p2} = \frac{[X_{bB}/\omega_0]}{\left(1+\omega_0^2[X_{bB}/\omega_0]C_{off3}\right)} > 0 \tag{5.122}$$

Now, let us derive the expression for C_{p1}. At this point, we consider the all pass impedance condition

$$z_{aB} = \frac{1}{z_{bB}} \tag{5.123}$$

or in the open form

$$R_{aB} + jX_{aB} = \frac{1}{R_{bB} + jX_{bB}} \tag{5.124}$$

If $R_{aB} \ll |X_{aB}|$ and $R_{bB} \ll |X_{bB}|$ then, all pass condition is approximated as

$$X_{aB} = -\frac{1}{X_{bB}} > 0 \tag{5.125}$$

$$X_{aB} = \left(\frac{\omega R_{on1}^2 L_{p1}}{R_{on1}^2 + \omega^2 L_{p1}^2} - \frac{1}{\omega\left(C_{p1}+C_{off2}\right)}\right) > 0 \tag{5.126}$$

Hence, at $\omega = \omega_0$ the total capacitor $C_T = C_{p1} + C_{off2}$ can be found using (5.126) as

$$C_{p1} + C_{off2} = \left[\frac{1}{\omega_0}\right] \frac{1}{\left(\frac{\omega_0 R_{on1}^2 L_{p1}}{R_{on1}^2 + L_{p1}^2} - X_{aB}\right)} = \left[\frac{1}{\omega_0}\right] \frac{1}{(\eta - X_{aB})} > 0 \tag{5.127}$$

where

$$\eta = \frac{\omega_0 R_{on1}^2 L_{p1}}{R_{on1}^2 + L_{p1}^2} \tag{5.128}$$

The expression given in (5.127) is satisfied if

$$\eta > X_{aB} = -\frac{1}{X_{bB}} = -\frac{1}{tan\left(\frac{\theta_B}{2} \mp 90^0\right)} = tan\left(\frac{\theta_B}{2}\right) > 0 \tag{5.129}$$

or

$$\eta = \frac{\omega_0 R_{on1}^2 L_{p1}}{R_{on1}^2 + L_{p1}^2} > tan\left(\frac{\theta_B}{2}\right) = \mu_B \tag{5.130}$$

In (5.130), L_{p1} can be specified such that

$$L_{p1} = \frac{L_1}{1 + \omega_0^2 L_1 C_{off1}} \tag{5.131}$$

where

$$L_1 = tan\left(\frac{\theta_A}{2}\right) = \mu_A \tag{5.132}$$

$$L_{p1} = \frac{tan\left(\frac{\theta_A}{2}\right)}{1 + \omega_0^2 C_{off1} tan\left(\frac{\theta_A}{2}\right)} = \frac{\mu_A}{1 + \omega_0^2 \mu_A C_{off1}} \tag{5.133}$$

Thus, (5.130) is expressed as

$$\eta = \frac{\omega_0 R_{on1}^2 L_{p1}}{R_{on1}^2 + L_{p1}^2} > tan\left(\frac{\theta_B}{2}\right) = \mu_B \tag{5.134}$$

where

$$R_{on1} = \frac{R_{on1a}}{R_a}, \quad R_{on1a} = \frac{672 \times 10^{-15}}{C_{off1a}(Farad)} \tag{5.135}$$

Hence, once ω_0, θ_A and θ_B are selected, switch S1 must be designed in such a way that (5.134) must be satisfied.

Finally, the cross-arm capacitors C_{p2} is determined as $C_{p2} = \mu_A - C_{off4} \geq 0$

If the above equation is not satisfied (i.e. if C_{p2} negative), then we should lover the value of C_{off4} until we end up with positive C_{p2}. Perhaps, the designer may prefer to set $C_{p2} = 0$. In this case, switch S4 is re-designed to yield $C_{off4} = \mu_A$.

In order to implement the above design equations, we propose the following algorithm.

Inputs:

Desired phase shift $\Delta\theta_0$ specified at the normalized centered frequency $\omega_0 = 1$.

θ_{B0}: Desired positive phase-shift of the leading symmetrical lattice structure (State-B)

Actual center frequency f_{0a}

Actual normalizing Resistor $R_a = 100\Omega$.

All switch capacitor values starts with $C_{off1,2,3,4} = C_{offopt}$. And for TSMC 0.18µm process, we have freedom to choose C_{offopt} as 90 fF or any suitable capacitor value.

Computational Steps:

Step 1: Compute the major design parameters μ_A and μ_B.

Step 2: Compute normalized off capacitances and on resistances using C_{offopt}.

Step 3: Compute series arm inductor L_{p1}.

Step 4: Compute η.

Step 5: Check if η is bigger than μ_B. If yes, then GOTO Step 6. If no, GOTO input-step to either change ω_0 or change C_{off1a}.

Step 6: Compute the imaginary part X_{bB} of the cross-arm impedance z_{bB} and compute the imaginary part X_{aB} of the series-arm impedance z_{aB}.

Step 7: Compute series arm components L_{p1} and C_{p1}.

Step 7a: Compute cross arm component L_{p1}. Check if L_{p2} is positive. If not, redesign switch S3 by reducing C_{off3a}.

Step 7b: Compute series arm component C_{p1}. Check if C_{p1} is positive. If not, redesign switch S2.

Step 8: Compute cross arm component C_{p2}.

Step 9: Compute all actual components using normalized values.

Let us run an example to implement all of above steps.

Example 6.

Let us design a phase shifter using 3S-DPS topology for phase shift of 45^0 at the center frequency of $f_{0a} = 8\ GHz$.

Take $\theta_B = -10^0$ and $\theta_A = 55^0$. Also assume the optimum capacitors for switches to be $C_{off-opt} = 90\ fF$.

Answer:

Step 1: Major design parameters are computed as $\mu_A = 0.5206$ and $\mu_B = 0.0875$.

Step 2: Normalized NMOS off capacitancesand on resistances are $R_{on(i)} = 0.0747; i = 1,2,3,4$ and $C_{off(i)} = 0.4524; i = 1,2,3,4$.

Step 3: Series arm inductor is computed as $L_{p1} = 0.4213$.

Step 4: Using the algorithm step 4, $\eta = 0.0128$.

Step 5: Check if $\eta = 0.0128 > \mu_B = 0.0875$. The answer is NO. C_{off1a} should be decreased. $C_{off1a} = 25fF$ is selected. Using new C_{off1a}; $C_{off1} = 0.1257$, $R_{on1} = 0.2688$, $L_{p1} = 0.4886$. Lets check if, $\eta = 0.1135 > \mu_B = 0.0875$. The answer is YES, so we can continue to step 6.

Step 6: Imaginary part of series and cross arms are computed as $X_{aB} = 0.0875$ and $X_{bB} = -11.4301$.

Step 7a: Compute $L_{p2} = 2.7405$.

Step 7b: Compute $C_{p1} = 37.9627$.

Step 8: Compute $C_{p2} = 0.0682$.

Step 9: All actual components are computed and given in Table 5.14.

Table 5.14 : Component values of 3S-DPS for $\Delta\theta_0=45^0$ of example 6.

Components	Actual Values	Channel Resistors	Actual Values	OFF State Capacitors	Actual Values
$L_{p1a}(nH)$	0.9720	$R_{on1}(\Omega)$	26.880	C_{off1}(fF)	25
$C_{p1a}(pF)$	7.55	$R_{on2}(\Omega)$	7.4667	C_{off2}(fF)	90
$L_{p2a}(nH)$	5.452	$R_{on3}(\Omega)$	7.4667	C_{off3}(fF)	90
$C_{p2a}(fF)$	13.65	$R_{on4}(\Omega)$	7.4667	C_{off4}(fF)	90

In Fig. 5.10, phase shifting performance between the states is depicted. At the first place, we should keep in mind that, derived design equations in this section are approximate and developed at the normalized central frequency ω_0. Therefore, we expect some discrepancies between the given data and the resulting performance. For example, for State B, at $\omega_0 = 1$, phase $\theta_{21B}(\omega_0)$ is fixed as $\theta_B = 10^0$. However, actual phase is found as $\theta_{21B}(\omega_0) = -10.2$ which introduces a relative phase error $\delta_{21\theta_B}$ as $\delta_{21\theta_B} = 2\%$.

In State-A, the relative phase error is given by $\delta_{21\theta_A} = 2.09\%$.

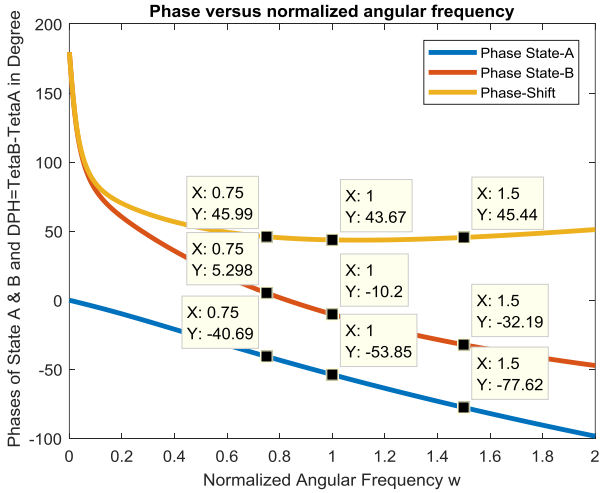


Figure 5.10 : Phase performance of $45^0$3S-DPS in example 6.

At the center frequency $\omega_0 = 1$, relative phase shift error $\delta_{21\theta}$ is given by $\delta_{21\theta} = 2.96\%$. Furthermore, over an octave frequency band, more specifically from 6 GHz ($\omega_1 = 0.75$) to 12 GHz ($\omega_2 = 1.5$), the phase shift $\Delta\theta(\omega)$ between the states is almost flat.

Referring to Fig. 5.10, let maximum phase-shift deviation over an octave bandwidth of 6-12 GHz be $\Delta\theta_{max}$. Then, $\Delta\theta_{max} = 45.99^0$. Over the same bandwidth, let the minimum phase-shift deviation be $\Delta\theta_{min}$. Then, $\Delta\theta_{min} = 43.67^0$. Similarly, let the average phase-shift be designated by $\Delta\theta_{av}$, which is computed as $\Delta\theta_{av} = 43.83^0$. Phase shift error, referred as $\epsilon_{\Delta\theta} = 1.16$. Then, over one octave bandwidth of 6 GHz-12 GHz, the phase-shift variation is given by $\Delta\theta(w) = \theta_{av} \pm \epsilon_{\Delta\theta} = 44.83^0 \pm 1.16^0$.

For the 45^0 phase-shift, loss characteristic of the proposed 3S-DPS configuration is depicted in Fig. 5.11.

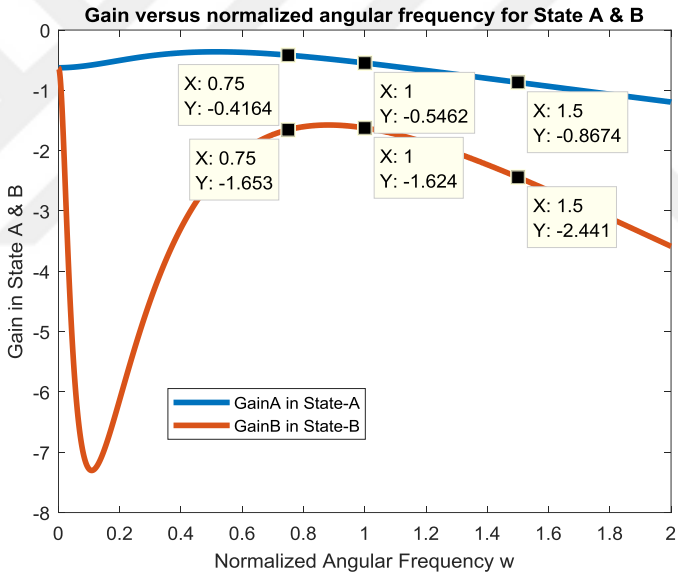


Figure 5.11 : Gain performance of $45^0$3S-DPS in example 6.

Close examination of this figure reveals that State-B loss of the proposed phase shifter is much higher than that of State-A (maximum loss of 2.441 dB of State-B versus maximum loss of 0.8674 of State-A). Anyhow, the maximum loss of State-B is still less than 3dB, which is acceptable.

The 3S-DPS phase shifting cells can be manufactured as MMIC using silicon 0.180 nm VLSI technology up to X or Ku Band respectively. In the next chapter, 3-Bit (45, 90 and 180 degree) digital unit cell phase shifter designs and their VLSI implementation process are introduced.

6. IMPLEMENTATION OF 3S-DPS TOPOLOGY

The 3S-DPS phase shifting cells are implemented using TSMC 0.18µm CMOS process. The schematics component values are determined using the design algorithms given in the section 5, and if applicable, optimization is done in order to obtain better performance over the band of interest.

As given in section 5, the even distributed phase value between State-A and State-B design procedure is much worse than the design procedure outcome of uneven phase distribution between State-A and State-B. For this reason, this section is dedicated to the implementation of design procedure of uneven phase distribution between State-A and State-B. The implementation of the proposed 3S-DPS topology is designed using TSMC 0.18µm CMOS process PDK.

6.1 Design of 3S-DPS unit cells with uneven distrubuted phase shift between State-A and State-B using the algorithm given in section 5.2.2

In this section, the component values determined in MATLAB environment using the algorithm given in section 5.2.2 is used to implement 3S-DPS unit cells within the TSMC 0.18µm CMOS process. 45^0 3S-DPS unit cell component values and transistor Ron-Coff parameters are given already in section 5.2.2.

After defining the component values of the transistors for TSMC 0.18µm CMOS process using transistors Ron-Coff parameter, the 45^0 3S-DPS unit cell schematic components are determined, which are given in Table 6.1.

Table 6.1 : Actual components of 3S-DPS for $\Delta\theta_0=45^0$.

Components	Actual Values	NMOS Sizes	W/L Values
$L_{p1a}(nH)$	0.62	Q_{S1}	$200\mu m/0.18\mu m$
$C_{p1a}(pF)$	4.46	Q_{S2}	$200\mu m/0.18\mu m$
$L_{p2a}(nH)$	4.01	Q_{S3}	$200\mu m/0.18\mu m$
$C_{p2a}(fF)$	0	Q_{S4}	$160\mu m/0.18\mu m$

Resulting electrical performances of the 45^0 3S-DPS cell are shown in Fig. 6.1 over wideband.

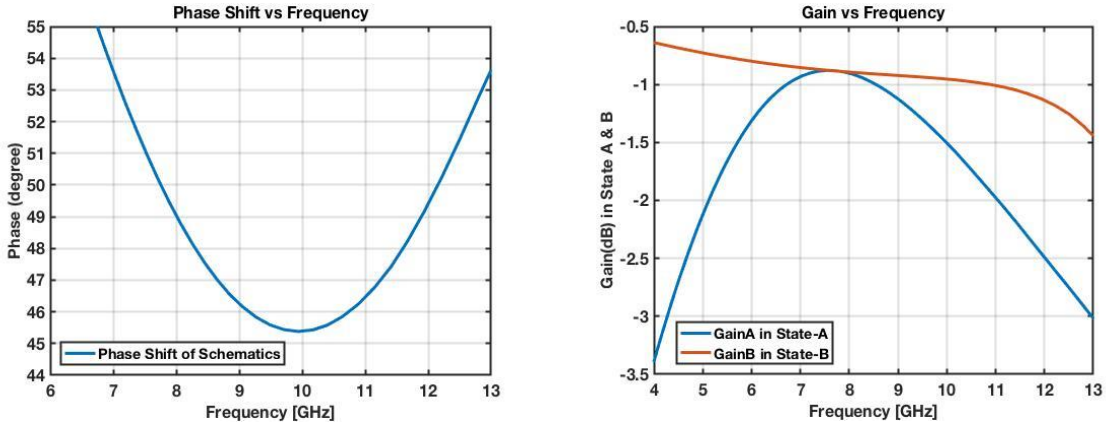


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Figure 6.1 : Phase and gain of proposed 45^0 phase shifter schematics using TSMC 0.18um PDK.

The phase and gain plots of Fig. 6.1 indicate that, the proposed 45^0 3S-DPS achieves 7.8-12 GHz bandwidth with 10% phase perturbation and 2.5dB loss over the 7.8-12 GHz bandwidth.

It should be noted that the designer can manually optimize the electrical performance of the proposed phase shifting unit by altering the component values.

In Table 6.2 the manipulated component values are shown.

Table 6.2 : Actual components of optimized 3S-DPS for $\Delta\theta_0=45^0$.

Components	Actual Values	NMOS Sizes	W/L Values
$L_{p1a}(nH)$	0.585	Q_{S1}	$200\mu m/0.18\mu m$
$C_{p1a}(pF)$	4.46	Q_{S2}	$200\mu m/0.18\mu m$
$L_{p2a}(nH)$	4.01	Q_{S3}	$200\mu m/0.18\mu m$
$C_{p2a}(fF)$	0	Q_{S4}	$150\mu m/0.18\mu m$

Corresponding phase shifter performance is depicted in Fig. 6.2.

Close examination of Fig. 6.2 reveals that 10% perturbation of the phase shift is accomplished over 7.3-13.2 GHz bandwidth with small variations on the component values as shown in Table 6.3. The gain within 7.3-13.2 GHz band is better than that of -3.2dB. The component values can be changed to improve the phase shift performance of the proposed circuit.

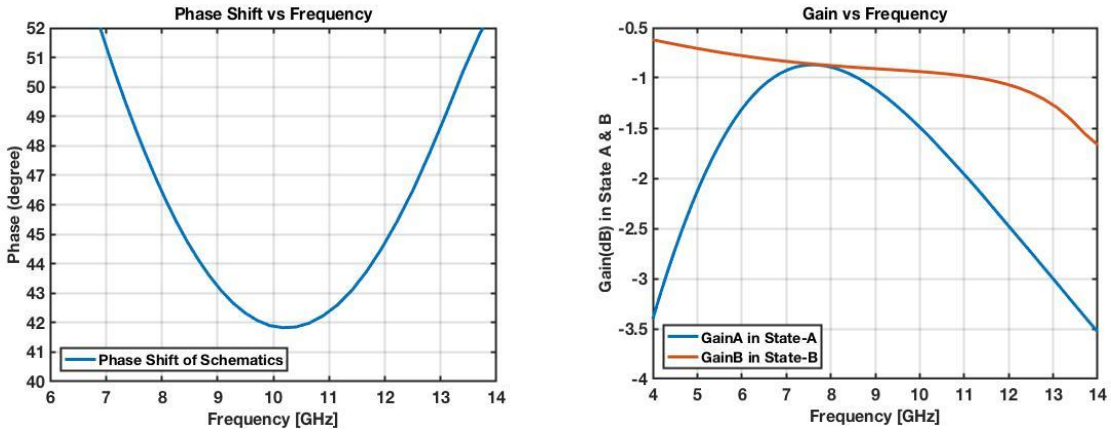

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Figure 6.2 : Phase and gain of improved 45^0 phase shifter schematics using TSMC 0.18um PDK.

Employing the same phase-shifter topology and the design algorithm and procedures, component values of the schematics of the 90^0 3S-DPS is given in Table 6.3.

Table 6.3 : Actual components of optimized 3S-DPS for $\Delta\theta_0=90^0$.

Components	Actual Values	NMOS Sizes	W/L Values
$L_{p1a}(nH)$	0.905	Q_{S1}	$200\mu m/0.18\mu m$
$C_{p1a}(pF)$	2.18	Q_{S2}	$200\mu m/0.18\mu m$
$L_{p2a}(nH)$	2.63	Q_{S3}	$200\mu m/0.18\mu m$
$C_{p2a}(fF)$	38	Q_{S4}	$200\mu m/0.18\mu m$

The electrical phase shifter performance of 90^0 3S-DPS is shown in Fig. 6.3.

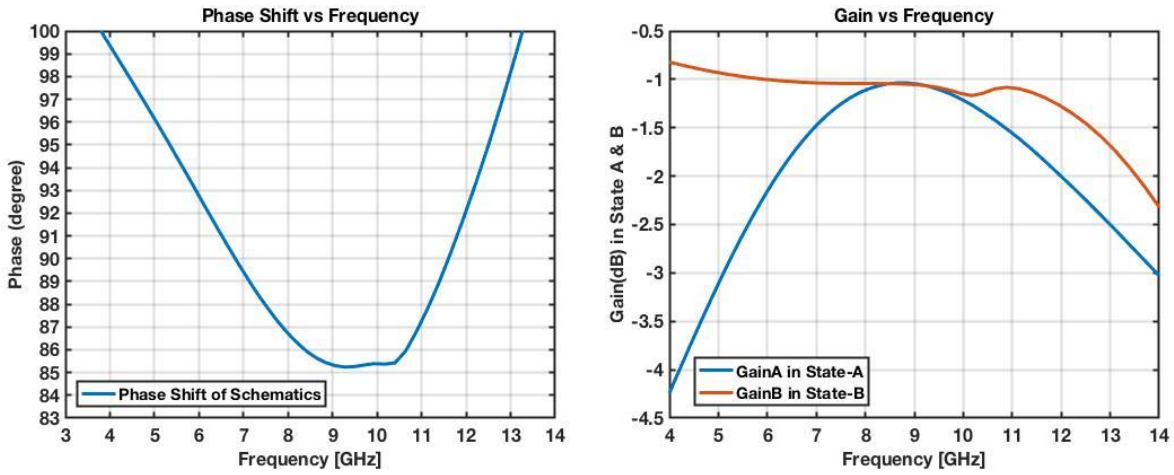

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Figure 6.3 : Phase and gain of proposed 90^0 phase shifter schematics using TSMC 0.18um PDK.

For 90^0 3S-DPS design exhibits 10% phase perturbation and 3.1dB loss over the 5-13.1 GHz bandwidth.

180^0 3S-DPS unit cell schematic components for the actual implementation using TSMC 0.18µm CMOS process PDK are given in Table 6.4.

Table 6.4 : Actual components of optimized 3S-DPS for $\Delta\theta_0=180^0$.

Components	Actual Values	NMOS Sizes	W/L Values
$L_{p1a}(nH)$	3.16	Q_{S1}	$200\mu m/0.18\mu m$
$C_{p1a}(pF)$	1.04	Q_{S2}	$200\mu m/0.18\mu m$
$L_{p2a}(nH)$	3.16	Q_{S3}	$200\mu m/0.18\mu m$
$C_{p2a}(fF)$	1.04	Q_{S4}	$150\mu m/0.18\mu m$

The electrical phase shifter performance of 180^0 3S-DPS is shown in Fig. 6.4.

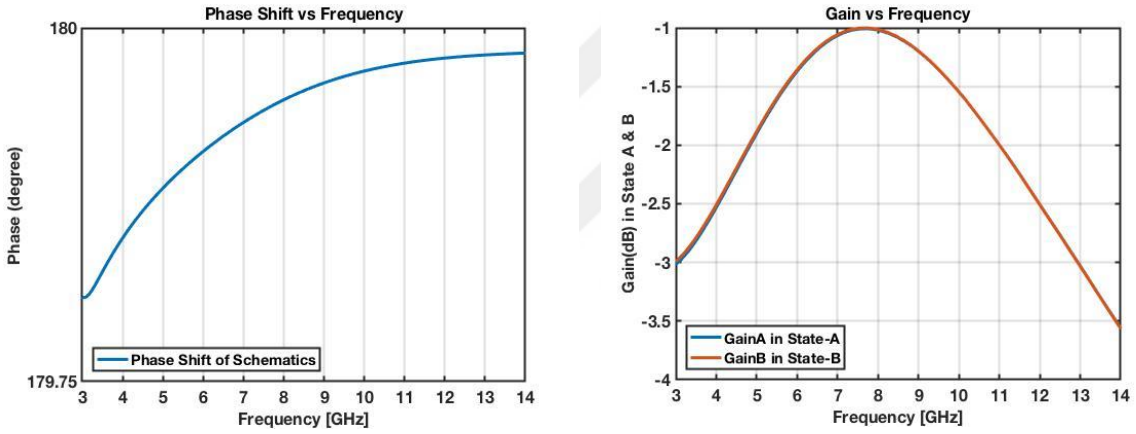

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Figure 6.4 : Phase and gain of proposed 180^0 phase shifter schematics using TSMC 0.18µm PDK.

Referring to Fig. 6.4, for 180^0 3S-DPS design exhibits less than 1% phase perturbation and the loss is better than 3dB over the frequency band of 3-13 GHz.

Also, in order to see the part to part variaton over process, the performance of each phase shifting cell is simulated employing the corner and mismatch Monte Carlo Statistical analysis tool provided by Cadence-ADEXL.

Corner and mismatch phase and gain performance of proposed 45^0 3S-DPS are given in Fig. 6.5.

Proposed 45^0 3S-DPS achieves 8.1-11.9 GHz bandwidth with 10% phase perturbation and 2.5dB loss over the 8.1-11.9 GHz bandwidth over corner and mismatch.

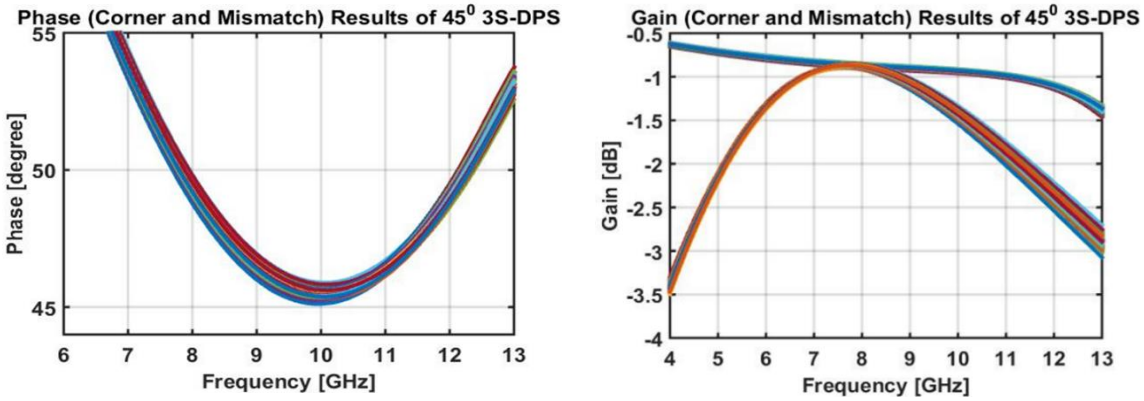

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Figure 6.5 : Phase and gain of proposed 45^0 phase shifter schematics using TSMC 0.18um PDK employing corner and mismatch analysis.

In addition, the optimized 45^0 phase shifter mismatch and corner analysis is shown in Fig. 6.6.

Fig. 6.6 reveals that 10% perturbation of the phase shift is accomplished over 7.5-13.1 GHz bandwidth with small variations on the component values. The gain within 7.5-13.1 GHz band is better than that of -3.2dB.

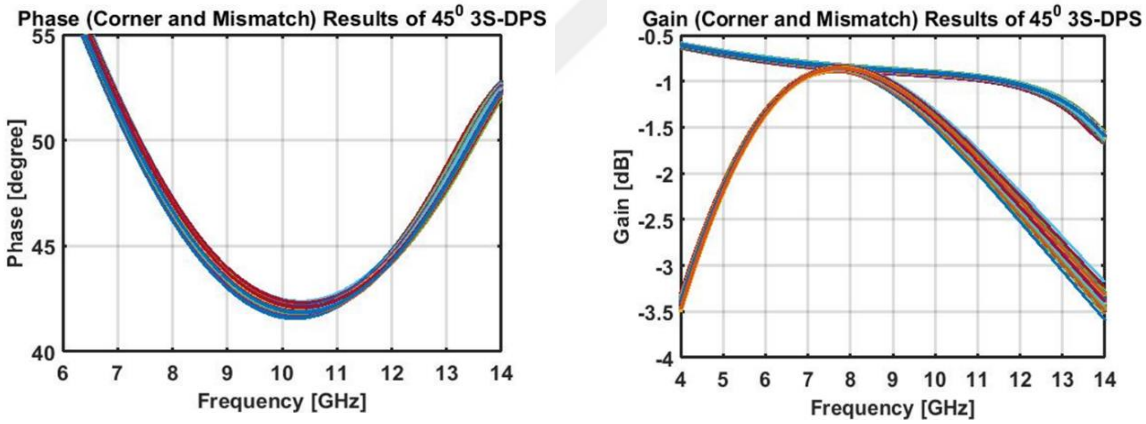

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Figure 6.6 : Phase and gain of optimized 45^0 phase shifter schematics using TSMC 0.18µm PDK employing corner and mismatch analysis.

90^0 phase shifter mismatch and corner analysis is shown in Fig. 6.7.

90^0 3S-DPS design exhibits 10% phase perturbation and 4 dB loss over the 4.3-13.0 GHz bandwidth under Monte Carlo and corner analysis as shown in Fig. 6.7. For the bandwidth of 7.5-13.0 GHz, the loss of 90^0 3S-DPS design exhibits 2.7 dB.

For the 180^0 3S-DPS design, corner and mismatch analysis are also investigated using TSMC 0.18µm PDKs employing Monte Carlo simulation tool.

Referring to Fig. 6.8, the 180^0 3S-DPS design exhibits less than 1% phase perturbation and the loss is better than 3.2 dB over the frequency band of 4-13 GHz under Monte Carlo and corner analysis.

Following the schematics design, layout of 3S-DPS units are drawn. Layouts for 45^0, 90^0 and 180^0 phase shifter unit cells are shown in Fig. 6.9.

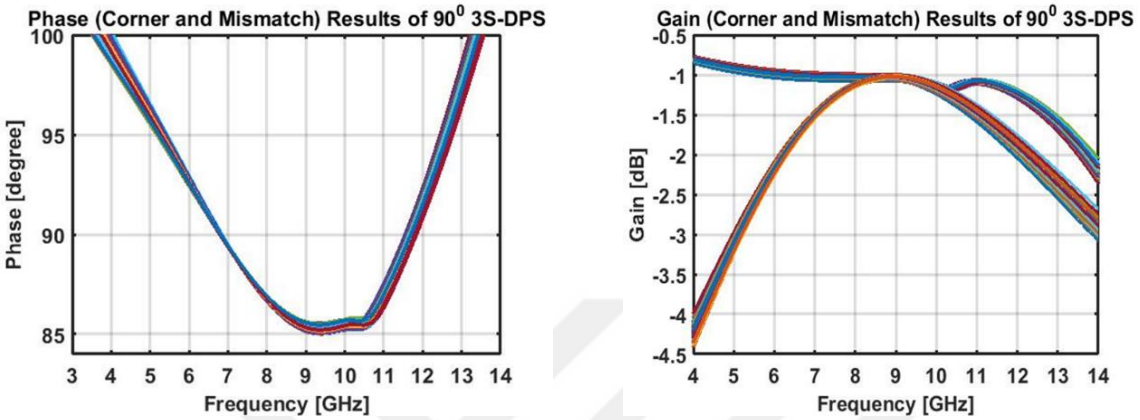

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Figure 6.7 : Phase and gain of optimized 90^0 phase shifter schematics using TSMC 0.18µm PDKs employing corner and mismatch analysis.

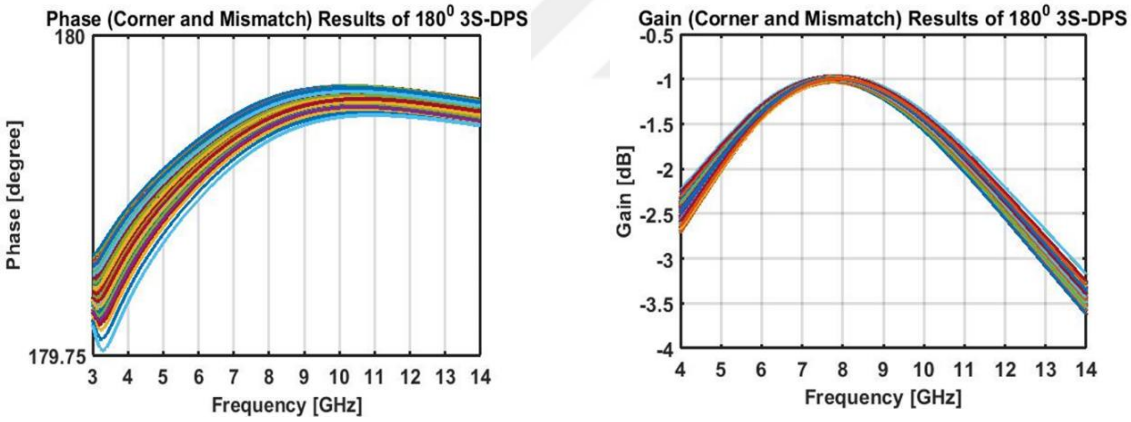

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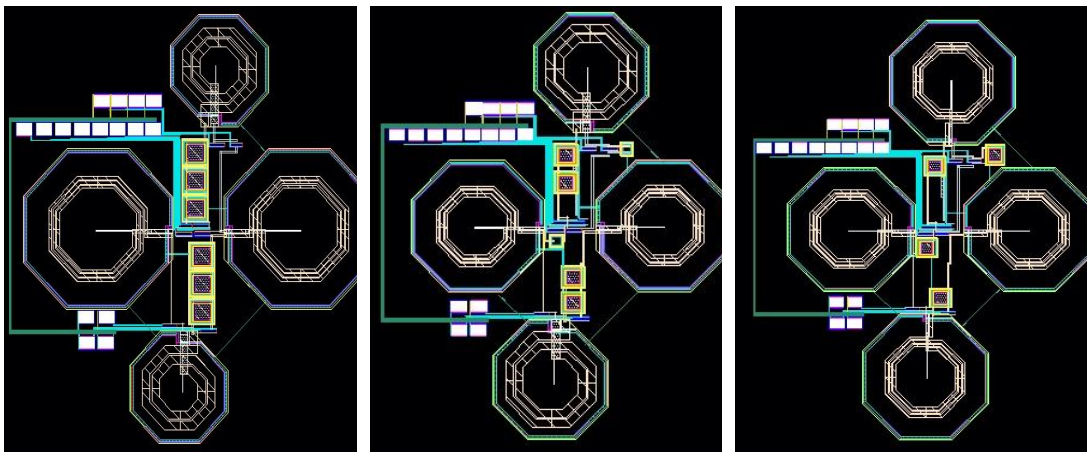
Figure 6.8 : Phase and gain of optimized 180^0 phase shifter schematics using TSMC 0.18µm PDKs employing corner and mismatch analysis.

Layout sizes are feasible and practical for implementing within TSMC 0.18µm CMOS process.

In section 5, it is already found in section 5.2.3 and section 5.2.4 that, the best performance can be captured by designing 3S-DPS with unevenlly phase distrubuted between State-A and State-B sections, together with State-B state having negative phase at the center frequency. This improved design approach impementations are investigated in the next section.



715µmx775µm *685µmx845µm* *730µmx925µm*

a b c

Figure 6.9 : Layout drawings of 45^0, 90^0 and 180^0 phase shifter schematics using TSMC 0.18µm PDK.

6.2 Design of 3S-DPS unit cells with uneven distrubuted phase shift between State-A and State-B: State-B with negative phase shift at center frequency

In section 5.2.3 and section 5.2.4, the step-by-step design algorithms are given with explicit equations. Also the performance of the design algorithm is obtained through the modeling using MATLAB environment. The performance results of the design algorithms given in section 5.2.3 and section 5.2.4 are already showed superior performance than the results of the design algorithms given in section 5.2.2 using MATLAB environment. It is already seen that, the design flow using the uneven deistrubuted phase shift between State-A and State-B using the phase shift of State-B as negative at the center frequency exhibits better performance. In this section, the actual implementation of the 3S-DPS unit cells are completed and the results are investigated in detail.

As already mentioned before, the implementaion is done with TSMC 0.18µm CMOS process PDKs and the performance is observed using Cadence Spectre simulator. The schematics components are initially found from the design algorithm of section 5.2.3 and section 5.2.4 and TSMC 0.18µm CMOS process Pcell components are determined.

The final optimized schematics component values for 45^0 3S-DPS unit cell are given in Table 6.5.

Table 6.5 : Actual components of 3S-DPS for $\Delta\theta_0=45^0$ of section 6.2.

Components	Actual Values	NMOS Sizes	W/L Values
$L_{p1a}(nH)$	0.35	Q_{S1}	$200\mu m/0.18\mu m$
$C_{p1a}(pF)$	20	Q_{S2}	$200\mu m/0.18\mu m$
$L_{p2a}(nH)$	17	Q_{S3}	$200\mu m/0.18\mu m$
$C_{p2a}(fF)$	30	Q_{S4}	$150\mu m/0.18\mu m$

The electrical phase shifter performance of 45^0 3S-DPS is shown in Fig. 6.10.

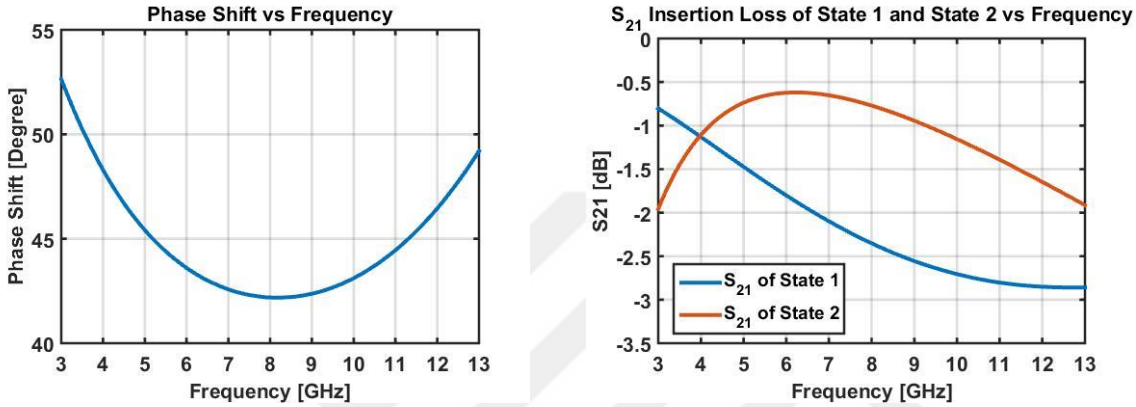


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Figure 6.10 : Phase and gain of optimized 45^0 phase shifter schematics using TSMC 0.18µm PDK with uneven design flow.

Results of Fig. 6.10 reveals that 10% perturbation of the phase shift is accomplished over 3.5-13 GHz bandwidth with small variations on the component values as shown in Table 6.6. The gain within 3.5-13 GHz band is better than that of -3dB. Also if we analyze the circuit over 3-13 GHz, the perturbation is 16.5% and gain loss is better than 3dB.

Employing the same phase shifter topology and the uneven phase distrubution design algorithm and procedures, component values of the schematics of the 90^0 3S-DPS are given in Table 6.6.

Table 6.6 : Actual components of 3S-DPS for $\Delta\theta_0=90^0$ of section 6.2.

Components	Actual Values	NMOS Sizes	W/L Values
$L_{p1a}(nH)$	0.55	Q_{S1}	$200\mu m/0.18\mu m$
$C_{p1a}(pF)$	1.6	Q_{S2}	$150\mu m/0.18\mu m$
$L_{p2a}(nH)$	5	Q_{S3}	$200\mu m/0.18\mu m$
$C_{p2a}(fF)$	100	Q_{S4}	$50\mu m/0.18\mu m$

The electrical phase shifter performance of 90^0 3S-DPS is shown in Fig. 6.11.

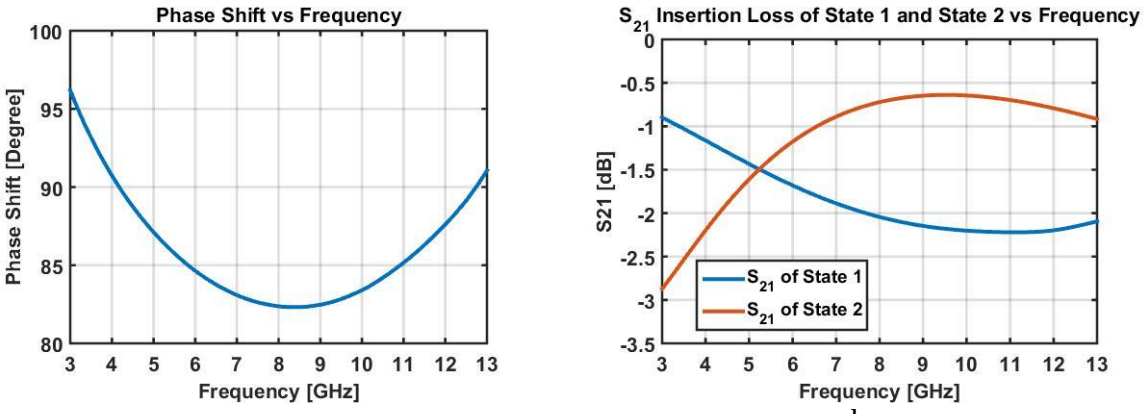


Figure 6.11 : Phase and gain of optimized 90^0 phase shifter schematics using TSMC 0.18µm PDK with uneven design flow.

90^0 3S-DPS design exhibits 10% phase perturbation and 3dB loss over the 3-13 GHz bandwidth.

Using the uneven phase distrubution algorithm allowing negative phase shift values, for the large phase shift values (i.e $>170^0$), C_{p1} and C_{p2} capacitors of generic proposed phase shifter topology are found too small to be printed with CMOS process. Therefore, we have used the freedom to implement and use the OFF capacitance of the MOSFET transistors. In order to implement large phase shift values, an alternative proposed digital phase shifter topology is invented which is given in Figure 6.12.

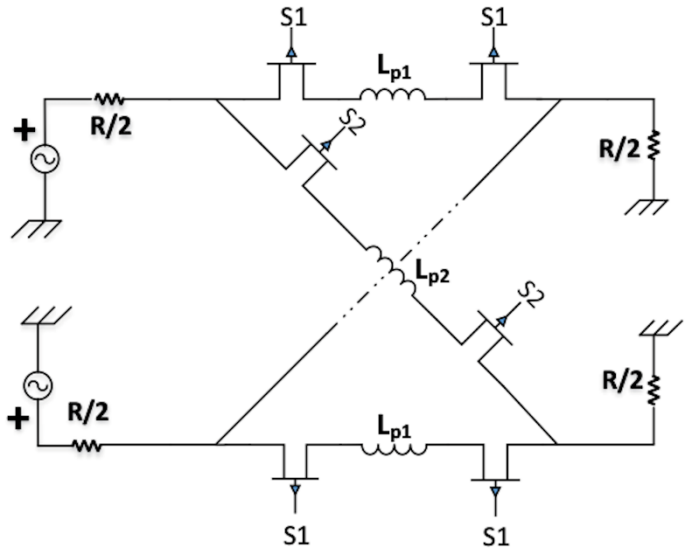


Figure 6.12 : Proposed 3S-DPS topology for large phase shifts.

In Fig. 6.12, MOSFET transistors S1 and S2 are employed as the switching elements. In State-A, S1 transistors are biased such that they operate at linear region and S2 transistors are open and operate at cut-off region. In this state of operation, the circuit

resembles the operation of Type-I symmetrical lattice by having equivalent inductors in the series arms and equivalent capacitors in the cross arms as shown in Fig. 6.13.

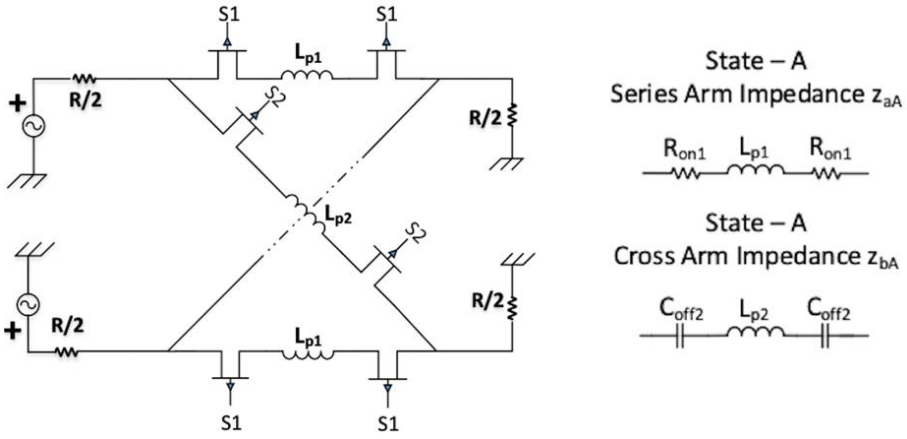


Figure 6.13 : Proposed 3S-DPS topology for large phase shifts at State A.

In State-A, the series arm switches S1 are ON and operating at linear region, which can be modelled as their channel resistor R_{on1}. In this mode of operation S2 are OFF and operating at cut-off region, which can be modelled as OFF capacitance C_{off2} . The equivalent impedance of series branch is found as

$$z_{aA} = 2R_{on1} + \mathrm{j}\omega L_{p1} \tag{6.1}$$

By design, R_{on1} must be small compared to the term $j\omega L_{p1}$ for the frequency band of interest. Furthermore, in this mode of operation, for the target phase shift $\Delta\theta_0$, normalized impedance of L_{p1} must be equal to Type-I lattice structure series arm impedance. The series arm inductor L_{p1} can be estimated as

$$L_{p1} = L_1 \tag{6.2}$$

In cross arms, when the S2 transistors are ON and S1 transistors are OFF, the equivalent impedance z_{bA} is found as

$$z_{bA} = \mathrm{j}\omega L_{p2} + \frac{2}{j\omega C_{off2}} \tag{6.3}$$

Using (6.3), the unknown cross arm capacitance can be found as

$$C_{off2} = \frac{2C_1}{1 + \omega^2 L_{p2} C_1} \tag{6.4}$$

In order to calculate C_{off2} value, cross arm inductor L_{p2} should already be found. The cross arm inductor L_{p2} will be found during the State-B confguration calculations.

In State-B, S1 is OFF and S2 is ON. In this state of operation, the circuit resembles the operation of Type-II symmetrical lattice by having equivalent capacitors in the series arms and equivalent inductors in the cross arms as shown in Fig. 6.14.

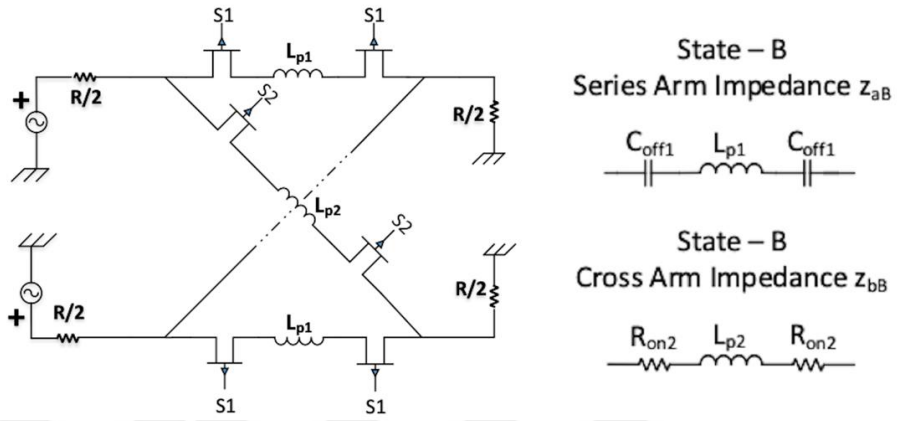


Figure 6.14 : Proposed 3S-DPS topology for large phase shifts at State B.

Similar to State-A configuration series arm, the cross arm of State-B configuration equivalent impedance is found as

$$z_{bB} = 2R_{on2} + j\omega L_{p2} \tag{6.5}$$

The R_{on2} resistor must be designed to be smaller than $j\omega L_{p2}$ term for the frequency band of interest. With this condition, cross arm inductor can be estimated as

$$L_{p2} = L_2 \tag{6.6}$$

The series arm impedance of the State-B configuration can be found as

$$z_{aB} = \mathrm{j}\omega L_{p1} + \frac{2}{j\omega C_{off1}} \tag{6.7}$$

The unknown capacitance is found as

$$C_{off1} = \frac{2C_2}{1 + \omega^2 L_{p1} C_2} \tag{6.8}$$

Series inductor value is found already in (6.2). Using (6.2) within (6.8), S1 transistor OFF capacitance value is found in terms of Type-I and Type-II ideal components as

$$C_{off1} = \frac{2C_2}{1 + \omega^2 L_1 C_2} \tag{6.9}$$

Also in (6.6), series arm inductor is found. Using (6.6) within (6.4), S2 transistor OFF capacitance value is found as

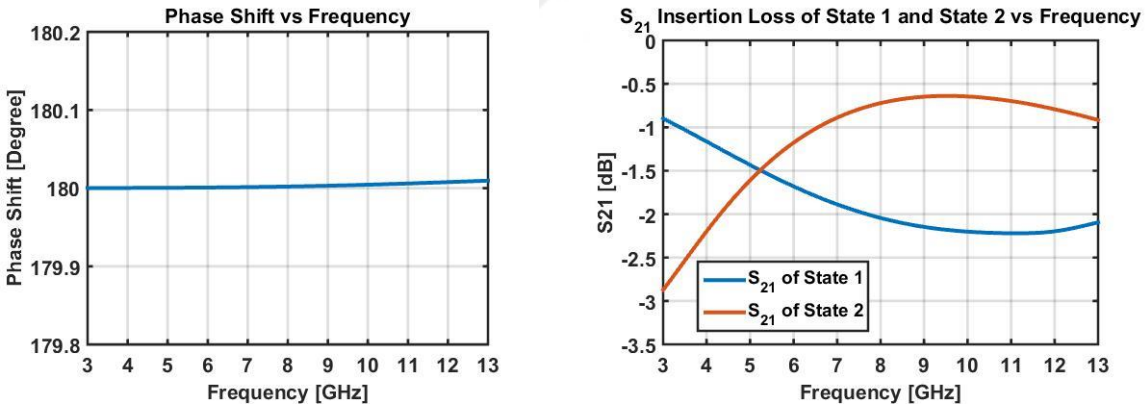
$$C_{off2} = \frac{2C_1}{1 + \omega^2 L_2 C_1} \tag{6.10}$$

Using the equations given in this part together, 180^0 3S-DPS topology given in Fig. 6.12 can be designed. The component values of the schematics of the 180^0 3S-DPS of Fig. 6.12 is given in Table 6.7.

Table 6.7 : Actual components of 3S-DPS for $\Delta\theta_0=180^0$ of section 6.2.

Components	Actual Values	NMOS Sizes	W/L Values
$L_{p1a}(nH)$	1.6	Q_{S1}	$200\mu m/0.18\mu m$
$L_{p2a}(nH)$	1.6	Q_{S2}	$200\mu m/0.18\mu m$

The electrical phase shifter performance of 180^0 3S-DPS is shown in Fig. 6.15.



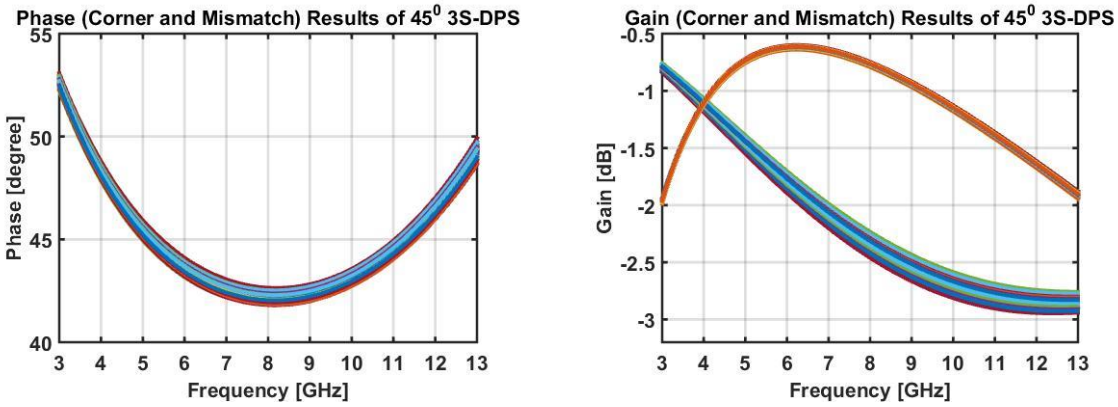
a b

Figure 6.15 : Phase and gain of proposed 180^0 phase shifter schematics using TSMC 0.18µm PDK with uneven design flow.

In order to see the variaton over process, the performance of the designed phase shifting units cells in this section are simulated employing the corner analysis tool provided by Cadence-ADEXL.

As shown in Fig. 6.16, corner and mismatch phase and gain performance of proposed 45^0 3S-DPS achieves 3.6-12.8 GHz bandwidth with 10% phase perturbation and 3 dB

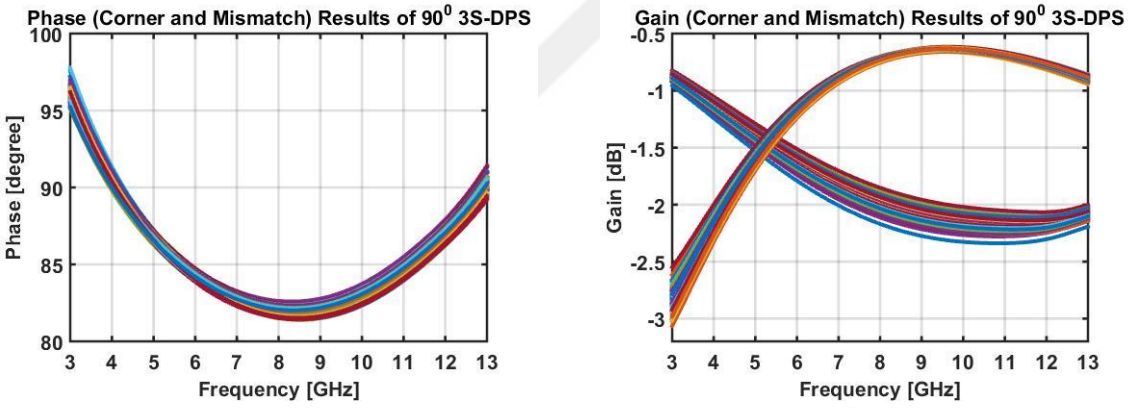
loss over the 3-13 GHz bandwidth. Also %17 phase perturbation achieved with 3-13 GHz bandwidth with 3 dB loss.



a b

Figure 6.16 : Phase and gain of proposed 45^0 phase shifter schematics using TSMC 0.18µm PDK with uneven design flow employing corner analysis.

90^0 phase shifter mismatch and corner analysis is shown in Fig. 6.17. 90^0 3S-DPS design exhibits 10% phase perturbation and 3.1 dB loss over the 3-13 GHz bandwidth under Monte Carlo and corner analysis as shown in Fig. 6.17.



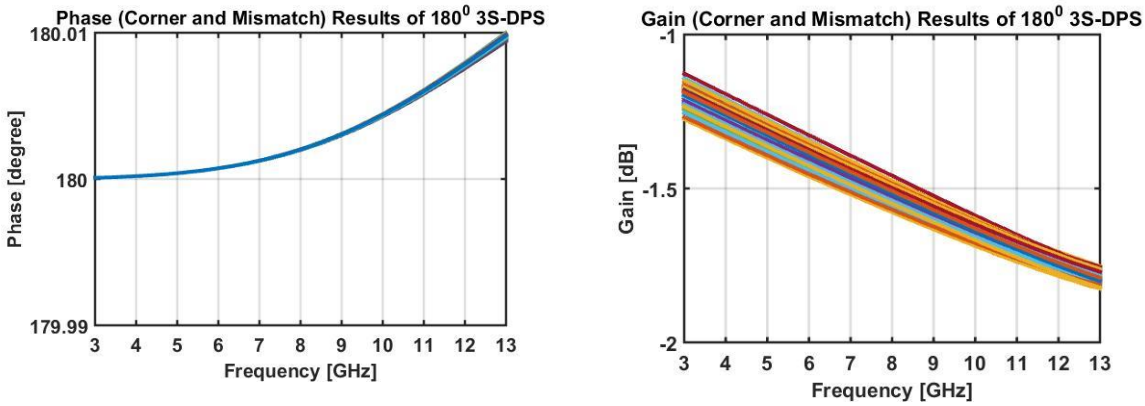
a b

Figure 6.17 : Phase and gain of optimized 90^0 phase shifter schematics using TSMC 0.18µm PDK with uneven design flow employing corner and mismatch analysis.

Referring to Fig. 6.18, the 180^0 3S-DPS design exhibits less than 1% phase perturbation and the loss is better than 1.8 dB over the frequency band of 3-13 GHz under Monte Carlo and corner analysis.

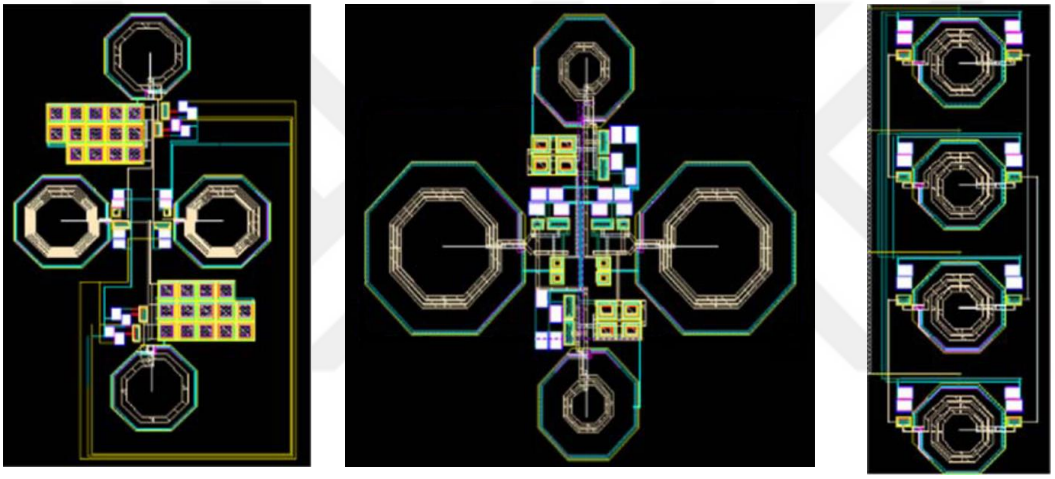
Following the schematics design, layout of 3S-DPS units are drawn. Layouts for 45^0, 90^0 and 180^0 phase shifter unit cells are shown in Fig. 6.19.

Layout sizes are feasible and practical for implementing within TSMC 0.18µm CMOS process.



a b

Figure 6.18 : Phase and gain of optimized 180^0 phase shifter schematics using TSMC 0.18µm PDK with uneven design flow employing corner and mismatch analysis.



900µmx1300µm *850µmx900µm* *400µmx950µm*

a b c

Figure 6.19 : Layout drawings of a) 45^0, b) 90^0 and c) 180^0 phase shifter schematics with uneven design flow using TSMC 0.18µm PDK.

In next section, 3D EM analysis of 45^0, 90^0 and 180^0 unit cell phase shifter design drawn layouts are going to be investigated.

6.3 3D EM Analysis of 3S-DPS 45^0, 90^0 and 180^0 Unit Cell Designs

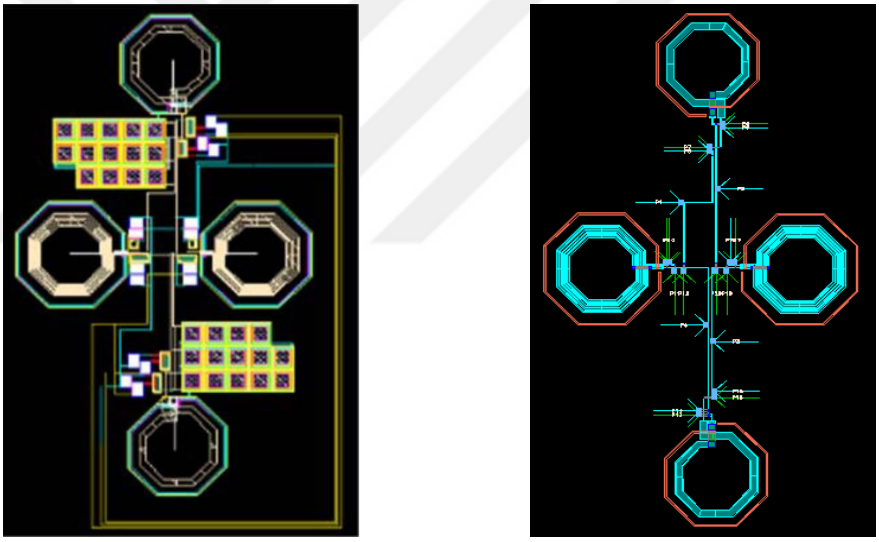
For the circuits operating at high frequency band, the routing parasitics and inductor couplings between each other and routings affect the performance. If the layout is not drawn with the concerns of the high frequency rule of thumbs, it is possible to get severe performance degradation. Also the inductor quality factor is affected by the layout drawing of the inductor and the coupling with the other inductors and routings.

In order to get the performance of the 3S-DPS unit cells together with coupling and parasitics of the layout, we analysed the phase shifter cells with 3D-EM tool. In this analysis, we used Momentum as the electro magnetic simulator.

The layout of the inductors and all routings of the unit cells are transferred to the Momentum environment. The ports are connected to the transistors and capacitors connections. The Momentum 3D-EM analysis is completed with the appropriate ports and related s-parameter .sNp file is captured.

The mix-mode simulation is done within Cadence environment having PDK Pcells of transistors and capacitors and .sNp nport having inductors together with couplings and parasitics of the inductors and routings.

The 45^0 phase shifter layout is exported to EM tool (Momentum) and appropriate ports are added as shown in Fig. 6.20.



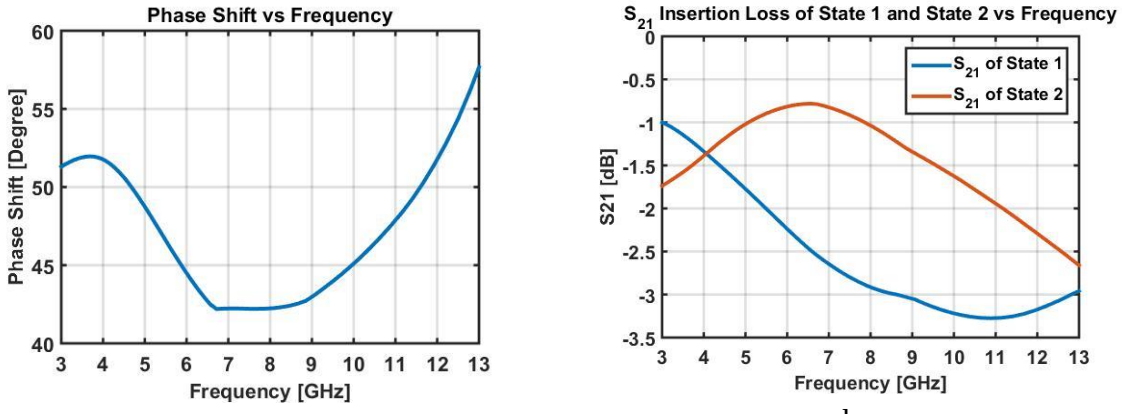
a b

Figure 6.20 : a) 45^0 3S-DPS layout b) 45^0 3S-DPS exported drawing to ADS Momentum and simulation ports.

The mix-mode simulation results are shown in Fig. 6.21.

3D-EM mixed mode simulation results exhibit 10% phase perturbation and 3.3 dB loss over the 4.9-11.5 GHz bandwidth.

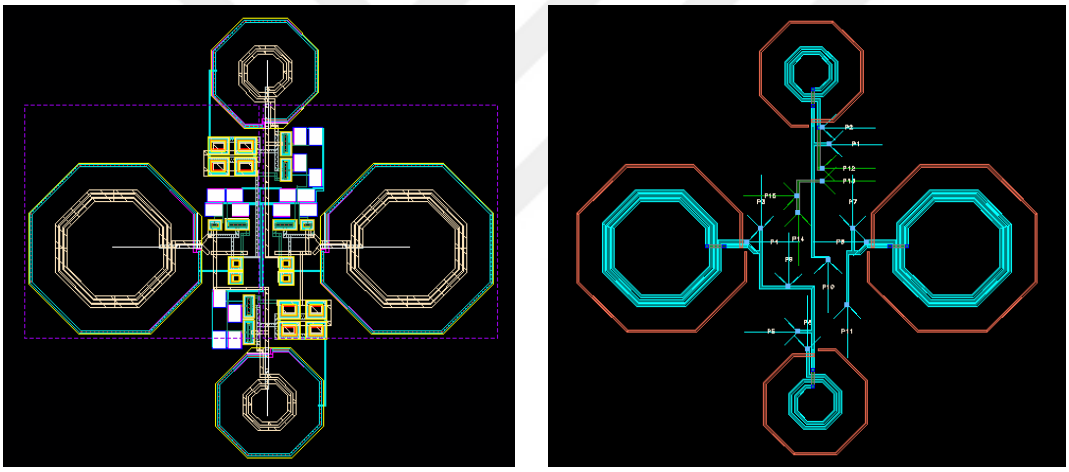
Also within 3-13 GHz bandwidth, proposed 3S-DPS circuit achieves 12.5^0 phase error and 3.3 dB gain loss.



a b

Figure 6.21 : Phase and gain results of 45^0 3S-DPS phase shifter employing 3D-EM analysis.

The 90^0 phase shifter layout is exported to EM tool (Momentum) and appropriate ports are added as shown in Fig. 6.22.



a b

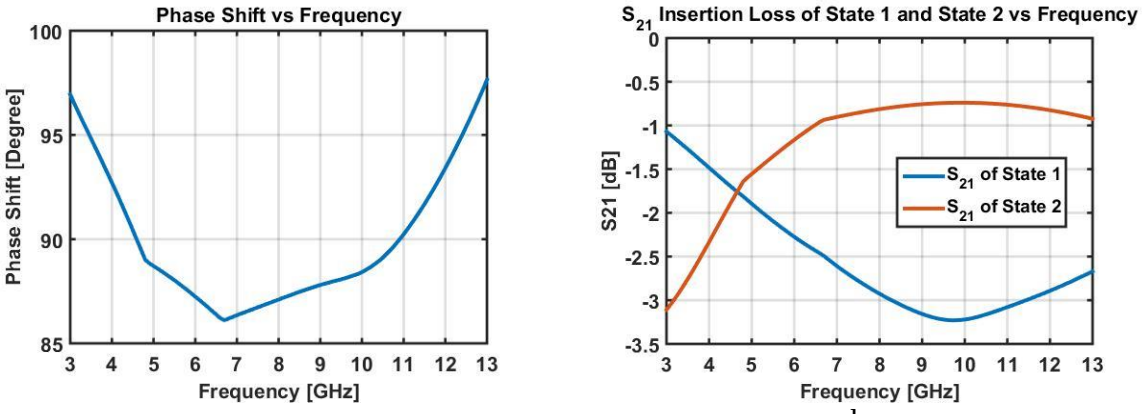
Figure 6.22 : a) 90^0 3S-DPS layout b) 90^0 3S-DPS exported drawing to ADS Momentum and simulation ports.

The mix-mode simulation results of 90^0 3S-DPS phase shifter are shown in Fig. 6.23.

As shown in Fig. 6.23, 3D-EM mixed mode simulation performance of proposed 90^0 3S-DPS achieves 3-13 GHz bandwidth with 10% phase perturbation and 3.3dB loss over the 3-13 GHz bandwidth.

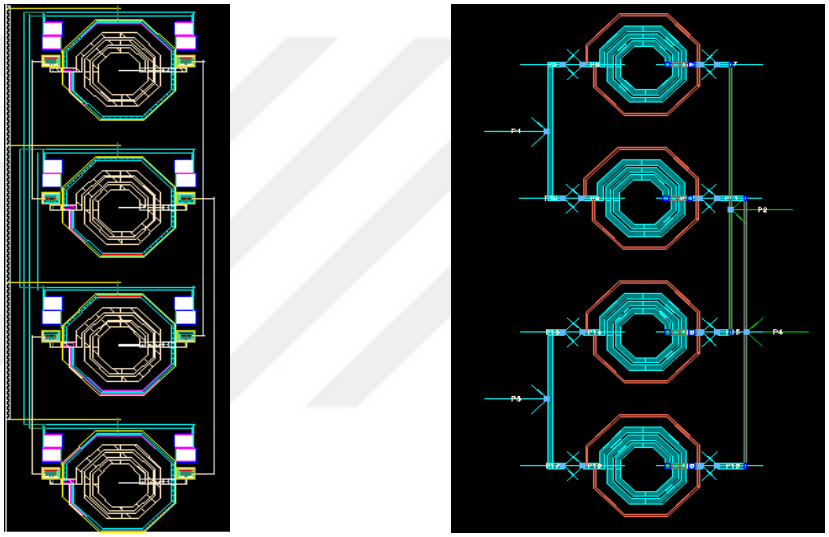
The 180^0 phase shifter layout is exported to EM tool (Momentum) and appropriate ports are added as shown in Fig. 6.24.

The mix-mode simulation results of 180^0 3S-DPS phase shifter are shown in Fig. 6.25.



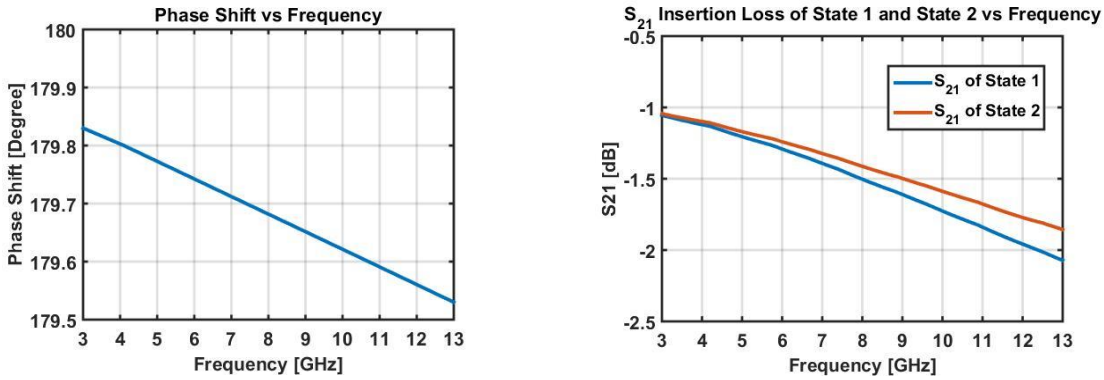
a b

Figure 6.23 : Phase and gain results of 90^0 3S-DPS phase shifter employing 3D-EM analysis.



a b

Figure 6.24 : a) 180^0 3S-DPS layout b) 180^0 3S-DPS exported drawing to ADS Momentum and simulation ports.



a b

Figure 6.25 : Phase and gain results of 180^0 3S-DPS phase shifter employing 3D-EM analysis.

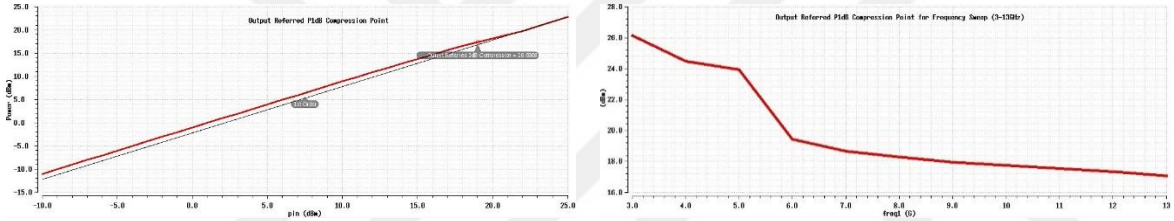
180^0 3S-DPS design exhibits less than 1% phase perturbation and the loss is better than 2.1 dB over the frequency band of 3-13 GHz under 3D-EM mixed mode analysis.

6.4 Linearity Analysis of 3S-DPS Topology Employing 3D-EM Tools

Linearity is one of the most crucial performance metric for phase shifters. In order to highlight the state-of-art proof of concept performance of 3S-DPS unit cells, linearity metrics such as IP3 and P1dB, are analyzed in this section.

The linearity analysis results are captured using mix-mode simulation, which is done within Cadence environment having PDK Pcells of transistors and capacitors and .sNp nport having couplings and parasitics of the inductors and routings.

The output referred P1dB compression point analysis for 45^0 3S-DPS is given in Fig. 6.26.



a b

Figure 6.26 : a) 45^0 3S-DPS output referred P1dB result for 8GHz input. b) 45^0 3S-DPS output referred P1dB result for input frequency sweep between 3-13 GHz.

Output referred 1 dB compression point analysis results show that 45^0 3S-DPS cell has more than 17 dBm output referred P1dB for frequencies between 3 GHz to 13 GHz.

IP3 performance results of 45^0 phase shifter swept for -10 dBm to 15 dBm is given in Fig. 6.27.

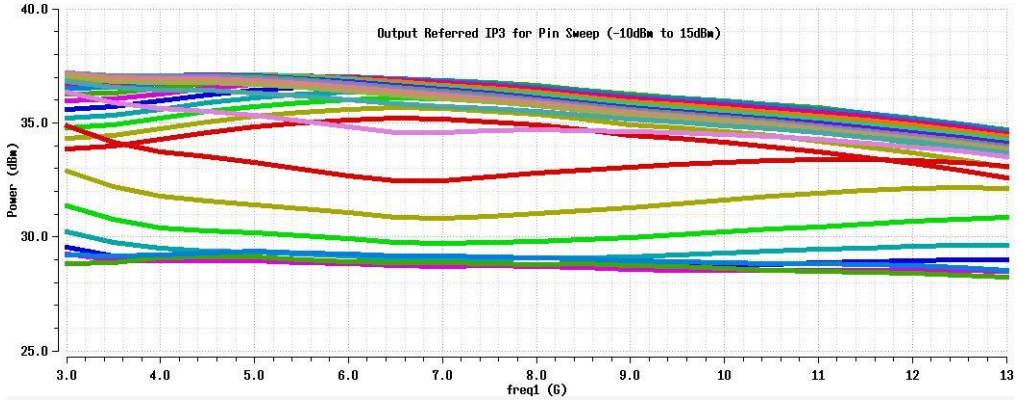
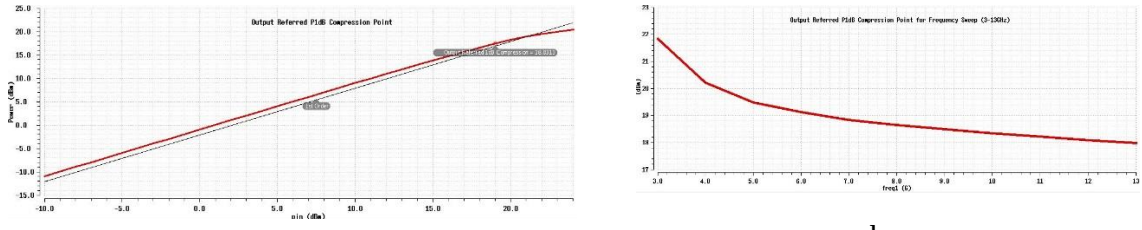


Figure 6.27 : Output referred IP3 results of 45^0 3S-DPS unit cell.

45^0 3S-DPS achieves more than 28 dBm output referred IP3 for input power between -10 dBm to 15 dBm.

Referring to Fig. 6.28, 90^0 3S-DPS design exhibits more than 17.9dBm output referred P1dB for frequencies between 3 GHz to 13 GHz.



a b

Figure 6.28 : a) 90^0 3S-DPS output referred P1dB result for 8GHz input. b) 90^0 3S-DPS output referred P1dB result for input frequency sweep between 3-13 GHz.

90^0 3S-DPS output referred IP3 analysis results are shown in Fig. 6.29.

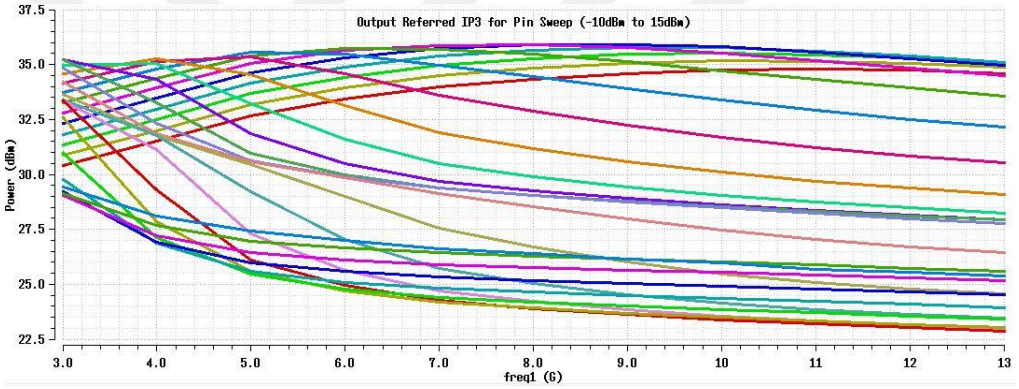
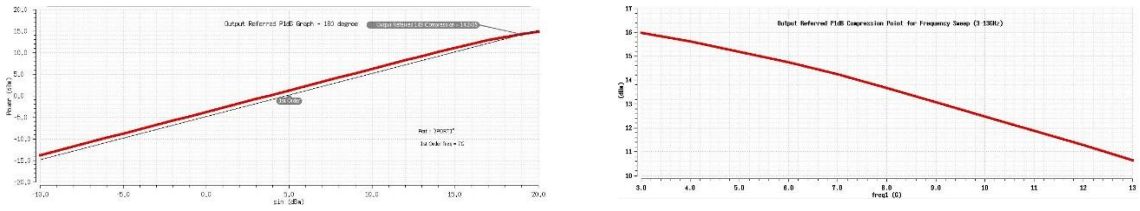


Figure 6.29 : Output referred IP3 results of 90^0 3S-DPS unit cell.

Third order intercept point of 90^0 3S-DPS achieves more than 22.5 dBm output referred IP3 for input power between -10 dBm to 15 dBm.

The output referred P1dB compression point analysis for 180^0 3S-DPS is given in Fig. 6.30.



a b

Figure 6.30 : a) 180^0 3S-DPS output referred P1dB result for 8GHz input. b) 180^0 3S-DPS output referred P1dB result for input frequency sweep between 3-13 GHz.

Output referrred 1dB compression point analysis results show that 180^0 3S-DPS cell has more than 10.5dBm output referred P1dB for frequencies between 3GHz to 13 GHz.

IP3 performance results of 180^0 phase shifter swept for -10dBm to 15dBm is given in Fig. 6.31.

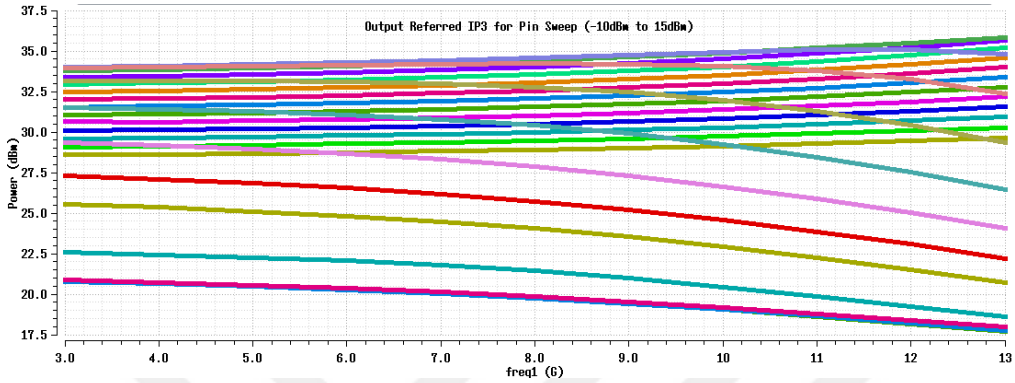


Figure 6.31 : Output referred IP3 results of 180^0 3S-DPS unit cell.

Output referred IP3 of 180^0 3S-DPS achieves more than 17.5dBm for input power between -10dBm to 15dBm.

The linearity summary of 3S-DPS unit cells are given in Table 6.8.

Table 6.8 : Output referred linearity performance of 3S-DPS unit cells.

3S-DPS unit cell	IP3 between -10dBm and 15dBm input power	P1dB between 3-13GHz input
45^0	28 dBm	17 dBm
90^0	22.5 dBm	17.9 dBm
180^0	17.5 dBm	10.5 dBm

Proposed 3S-DPS shows good performance of linearity. Since the phase shifters are generally located after the LNA at receiver and before the power amplifier at he transmitter, more than 10dBm output referred P1dB and 17.5 dBm IP3 are good performance metrics for next generation communication systems.

6.5 Comparison of 3S-DPS with State-of-Art Phase Shifter Topologies

After the introduction of next generation commuication systems, such as 5G protocol, the importance of phase shifters within the system of these protocols is increased. For this reason, as given in introduction section, there are many state-of-art researches are

done. In the Table 6.9, a comparative analysis results are summarized between the proposed 3S-DPS and other state-of-art phase shifter designs.

Table 6.9 : Comparison of phase shifters presented in literature.

	Phase Shifter Architecture	Technology	Bandwidth (GHz)	RMS Phase Error	S21 Loss
[20]	Reflective type phase shifter	0.6µm GaAs	5.15-5.7	1.5^0	6.4dB
[21]	Vector modulated phase shifter	0.6µm GaAs	4.7-5.7	7^0	9dB
[34]	LC lumped element based phase shifter	0.13µm CMOS	8-11	7.3^0	14dB
[38]	Vector sum based phase shifter	0.13µm CMOS	4.9-5.9	9.7^0	0.1dB
[43]	Active phase shifter with variable resonant circuit	0.3µm GaAs	2.38-2.42	4^0	2dB
[45]	Transmission line based phase shifter	45nm CMOS	57-64	NA	3.2dB
This Work	3S-DPS Topology	0.18µm CMOS	4.9-11.5	4.9^0	3.3dB

When compared with existing digital phase shifter circuits, proposed phase shifter topology offers better phase shifting capability over much wider frequency band. For example, [21] describes a Vector Modulated Based (VMB) digital phase shifter topology over 4.7-5.7 GHz bandwidth with 7^0 RMS phase error and 9 dB loss whereas our newly proposed 3S-DPS topology yields wider bandwidth (4.9-11.5 GHz) with better RMS phase error (4.9^0) and loss (less than 3.3 dB).

7. CONCLUSIONS AND RECOMMENDATIONS

In this thesis, a novel lattice-based wideband-wide phase range digital phase shifter topology is proposed. Novel and high performance digital phase shifting capability is realized owing to the invented switching technique. Using this new switching technique, the proposed topology resembles the operation of either "symmetrical LC-all pass" with lagging-phase (Type-I LC lattice) or "symmetrical LC-all pass" with leading-phase (Type-II LC lattice).

The crux of the idea is to combine the operation of Type-I LC lattice and Type-II LC lattice sections under one-compact symmetric circuit topology. For this reason, the invented phase shifter is called "Single and Simple-Symmetrical Digital Phase Shifter" or in short "3S-DPS".

The proposed 3S-DPS topology reduces the connection routing between the components such that the parasitic element sizes coming from these routings reduce drastically. This drastic reduction enables the high performance capability of the proposed "Single and Simple-Symmetrical Digital Phase Shifter". In addition, the invented switching technology reduces the component count when compared with the straightforward realization of the phase shifter architecture using standalone Type-I LC lattice and Type-II LC lattice together with two SPDT switches. As a result of this, the proposed switching technology reduces cost significantly.

In this thesis, the explicit design equations of "Single and Simple-Symmetrical Digital Phase Shifter" topology are also investigated both for ideal components and practical components. In order to compute the component values, we also provide the implementation algorithm to facilitate the construction of the novel digital phase shifter circuit. In order to come up with realistic results, TSMC 0.18μm process transistor models are used throughout the design algorithm steps. The design algorithm investigation starts with the even phase distribution between the states of State-A (resembles Type-I LC lattice) and State-B (resembles Type-II LC lattice). In addition, uneven phase distribution oriented design algorithm is also studied and using this algorithm, higher performance results are obtained. To further improve the bandwidth

of the 3S-DPS topology, practical switch losses are investigated throughout the explicit design equations and two new design algorithms are proposed. It is shown that the design algorithms using practical switch losses exhibit higher bandwidth with reasonable loss.

After investigating and proposing the design algorithms, schematics implementation of 3S-DPS is completed. First of all, design algorithm with uneven phase distribution between State-A and State-B is used to obtain component values of the 45^0, 90^0 and 180^0 3S-DPS unit cells. The implementation is simulated using corner and mismatch analysis and 7.5-13 GHz bandwidth with reasonable loss of 3 dB is achieved for 45^0, 90^0 and 180^0 3S-DPS unit cells. Then, another implementation of 45^0, 90^0 and 180^0 3S-DPS unit cells is completed using the design algorithm with practical switch losses. At this point, it is observed that, for large phase shift values such as 180^0 phase shifter design, the capacitor values within the proposed 3S-DPS topology are found to be small. In order to use this feature, another novel topology is proposed for the large phase shift values and it is observed that the performance of the 3S-DPS phase shifter is improved significantly. The new topology is also deeply investigated and explicit design equations are driven. The 180^0 3S-DPS unit cell is designed using the proposed topology for large phase shift values. The 45^0, 90^0 and 180^0 3S-DPS unit cell designs are simulated over corner and mismatch. The proposed 3S-DPS unit cell designs of 45^0, 90^0 and 180^0 achieve 4-12.5 GHz bandwidth for 10% phase perturbation and 3 dB gain loss. In addition to the corner and mismatch simulations, 3D-EM analysis is also completed. The 3D-EM analysis results achieve 4.9-11.5 GHz bandwidth for 10% phase perturbation and 3.3 dB gain loss.

In this thesis, the proof of concept of 3S-DPS topology is accomplished by designing separate 3-bit phase shifting units, namely 45^0, 90^0 and 180^0 cells with their layouts and simulation results. It is exhibited that proposed digital phase shifter topology results in superior phase shift range over wide bandwidth as compared to the ones cited in the current literature.

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