ISTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY

2.4 GHZ LC-VCO DESIGN BASED ON ACTIVE INDUCTORS

M.Sc. Thesis by
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2.4 GHZ AKTİF ENDUKTANS TABANLI LC VCO TASARIMI

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June, 2008 **Alphan ŞAHİN**

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ABBREVIATIONS

VCO	: Voltage Controlled Oscillator
AM	: Amplitude Modulation
FM	: Frequency Modulation
GSM	: Global System for Mobile Communication
SNR	: Signal to Noise Ratio
Wi-Fi	: Wireless Fidelity
WLAN	: Wireless Local Area Networks
OFDM	: Orthogonal Frequency Division Multiplexing
CCK	: Complementary Code Keying
DQPSK	: Differential Quadrature Phase Shift Keying
DBPSK	: Differential Binary Phase Shift Keying
DSSS	: Direct Sequence Spread Spectrum

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LIST OF SYMBOLS

L	**:** Inductor
C	**:** Capacitor
R	**:** Resistor
$\mathbf{P_{carrier}}$	**:** Power of carrier signal
$\boldsymbol{\omega_0}$	**:** Resonant frequency
Q	**:** Quality factor
F	**:** Excess noise factor
$\mathbf{K_{VCO}}$	**:** Gain of VCO
gm	**:** Transconductance of transistor
$\boldsymbol{\Delta\omega}$	**:** Offset frequency
k	**:** Constant of Boltzman
T	**:** Temperature
M	**:** Noise factor of active inductor

2.4 GHZ AKTİF ENDÜKTANS TABANLI LC VCO TASARIMI

ÖZET

Bu tez çalışmasında, UMC013 0.13 μm CMOS prosesi ile 2.4GHz merkez frekanslı aktif endüktans tabanlı LC osilatörleri tasarlanmıştır. IEEE 802.11b,g standartlarına faz gürültüsü açısından sağlayan bir LC VCO yapılması hedeflemiştir. LC VCO yapısında bulunan elemanların faz gürültüsüne etkileri ayrı ayrı incelenerek aktif endüktans ile yapılan bir LC tankının etkisinin oldukça baskın olduğu analitik olarak hesaplanmış ve simulasyonlarda görülmüştür. Bu yüzden LC tankın faz gürültüsüne katkısı minimum olacak şekilde aktif endüktans tasarlanmıştır.

LC VCO yapılarının faz gürültüsü performanslarını karşılaştırmak amacıyla 4 ayrı aktif endüktans tabanlı LC VCO tasarlanmıştır. Ayrıca UMC013 prosesiyle pasif endüktans kullanılarak elde edilebilen minimum faz gürültülü LC VCO bulunup, tüm sonuçlar birlikte değerlendirilmiştir.

Faz gürültüsü açısından en iyi elde edilebilen aktif endüktanslı LC VCO devresi, bağlantı ucu NMOS olan aktif endüktans ve PMOS çapraz bağlı negatif direnç yapısı ile elde edilmiştir. Optimize edilen faz gürültüsünün şematik değeri 1MHz ofset frekansında -89dBc/Hz olarak bulunmuştur. Devre, 2.14GHz-2.71GHz frekans bölgesinde osilasyon yapabilmekte ve 1mA-3mA arasındaki akım değerleri ile osilasyon frekansı ayarlanabilmektedir. 1.2V besleme geriliminden çekilen akım ise 20.69mA değerindedir.

Bu tezin giriş bölümünde alıcı ve verici mimarileri, VCO'nun yeri ve kablosuz haberleşme standartları anlatılmıştır. Tez çalışmasının hedefleri belirlenmiştir.

İkinci bölümde osilasyon teorisi ve VCO yapıları üzerinde durulmuştur. Aynı zamanda VCO için gürültüden bahsedilmiştir. LC tank yüzünden oluşan gürültü incelenmiş ve osilatörlerin en önemli tasarım parametrelerinden biri olan faz gürültüsü, LC VCO için analiz edilmiştir.

Üçüncü bölümde aktif endüktans incelenmiş ve pasif endüktanslar ile karşılaştırılmıştır. Bu bölümde, aktif endüktansın gürültü özellikleri dikkate alınarak LC VCO için faz gürültüsü tekrar incelenmiştir.

Dördüncü bölüm tezin tasarım kısmının anlatıldığı bölümdür. Aktif endüktans yapısı için önerilen devre topolojisi verilmiş ve aktif endüktans kullanarak aynı güç harcamasına sahip 4 ayrı LC VCO tasarımı yapılmıştır. Aynı devreler, aktif endüktans yerine pasif eşdeğerleri ile birlikte tekrar analiz edilip faz gürültüsü açısından tartışılmıştır.

Beşinci bölümde literatürde yer alan VCO yapıları incelenmiş ve aktif endüktans kullanılarak tasarlanan LC VCO göre karşılaştırılmıştır.

Altıncı bölüm sonuç bölümüdür. Çalışmanın genel değerlendirmesi yapılmıştır.

2.4 GHZ LC-VCO DESIGN BASED ON ACTIVE INDUCTORS

SUMMARY

In this work, 2.4GHz LC VCO based on active inductor is designed via 0.13 μm UMC013 CMOS process. Designing a LC VCO which supports IEEE 802.11b,g wireless communication standards is objected. Phase noise contribution of all LC VCO's circuitries are analyzed separately and, contribution of LC tank based on active inductor to noise is shown in schematic simulations and calculated analytically as dominant respect from other circuitries of LC VCO noise contribution. Therefore, active inductor is designed to get minimum noise contribution of LC tank to VCO for a low phase noise.

Four different LC VCOs based on active inductors are designed for comparisons of phase noise performance. In addition, a low noise LC-VCO with passive inductor is designed via UMC013 process to evaluate all phase performance via this process.

Among these LC VCO based on active inductors, best achievable phase noise is succeed with NMOS active inductor and PMOS cross-coupled LC-VCO structure. Optimized phase noise value is obtained as -89dBc/Hz at 1 MHz offset frequency. LC-VCO's frequency range is between 2.14GHz and 2.71GHz and frequency tuning current is between 1mA and 3mA. Current consumption of VCO is 20.69mA under 1.2V power supply.

In the introduction, transceiver architectures, role of VCO in transceiver and wireless communication standard are given. The goal of this work is defined.

Second chapter covers oscillation theory and structures of VCOs. Also, the topic of noise is analyzed. Noise sources in LC tank are examined and effects of these noise sources on phase noise performance are analyzed for LC VCO.

The third chapter is about active inductor. Active inductor structure and comparison with passive inductor are given. Phase noise performance of LC VCO is analyzed again considering contribution of active inductor noise.

The design processes of this work are explained in the fourth chapter. The circuit topology of active inductor and four different LC VCO design based on active inductor are given in this section. Designed oscillators are reanalyzed with passive equivalent inductor model of active inductor, and phase noise performance of oscillators are discussed,

In the chapter six, some VCOs published in the literature are discussed and compared with designed LC VCO based on active inductor.

Seventh chapter is the conclusion, and whole thesis is discussed.

1. INTRODUCTION

1.1 Transceiver Architectures

The term of transceiver, which is key part of wireless communication systems, stems from transmitter and receiver. The transmitter transforms digital data at baseband to signal at radio frequency using a modulation, and propagates this RF signal via an antenna. The receiver demodulates signals coming from an antenna, and converts signals to digital data at baseband again.

Radio transceivers have been used since 1900s with the intention AM and FM modulation. First mobile transceiver for mobile telecommunication was developed in the 1980s with GSM and DECT standards. With the demand for high data rates, many wireless communication standards has been improved using same communication concepts such as 802.11a and 802.11b,g. Moreover as a result of industry pressure to reduce the cost of communication chips, transceivers with higher levels of integration which means power, size and cost becomes necessary and critical.

1.2 Receiver Problems Based on VCO

In transceiver topologies, one of the main elements is voltage controlled oscillator (VCO) which roles as a local oscillator and converts RF signal of desired channel to IF signal.

An ideal oscillator outputs may be shown as equation 1.1 which ω_0 is resonant frequency, and ϕ_0 is phase, V_0 is amplitude of oscillator.

$$V_{osc} = V_o \sin(\omega_0 t + \phi_0) \quad \textbf{(1.1)}$$

However, in a practical oscillator, short term frequency instabilities occur due to noise and interference sources such as thermal, shot and flicker noise. The output function of a practical oscillator can be expressed as equation 1.2. $A(t)$ and, $\phi(t)$ changes with time.

$$V_{osc} = V_o(1 + A(t))\sin(\omega_0 t + \phi(t)) \quad \textbf{(1.2)}$$

One sided spectrum of an ideal oscillator and a practical one with random fluctuations is shown in Figure 1.1. Output spectrum of a practical oscillator doesn't only consist of an impulse at resonant frequency. There exists harmonics of ω_0 and sidebands which represents phase noise sidebands.

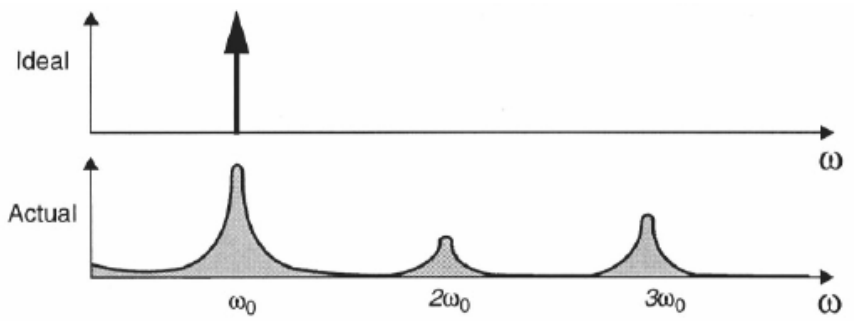

Figure 1.1 : Ideal and practical oscillator output frequency spectrum

Receiver problems are generally caused by these sidebands. If desired channel is weaker than adjacent channel, and also a VCO with a high noise converts RF signal to IF signal, desired channel and adjacent channel will interfere as shown in Figure 1.2. It is clear that using a low phase noise oscillator will increase SNR ratio of system.

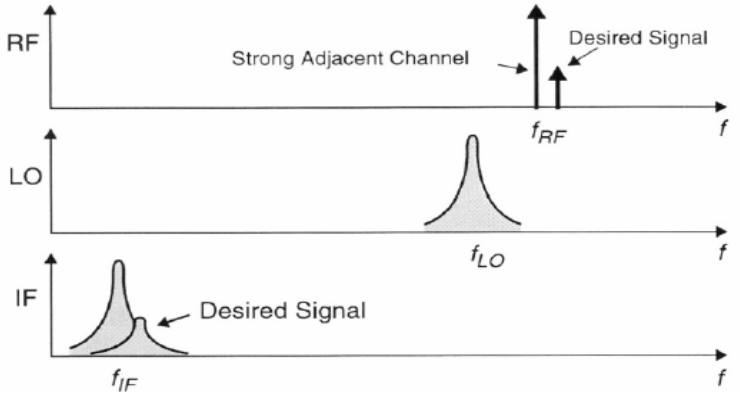

Figure 1.2 : Destructive effect of a VCO with high noise

Phase noise is defined as (1.3) where $P_{Sidebands}(\omega_0 + \Delta\omega, 1Hz)$ represents total noise in 1 Hz bandwidth at $\Delta\omega$ form the carrier ω_0, and $P_{Carrier}$ represents carier power as shown in Figure 1.3.

$$L(\Delta\omega) = 10.\log\left[\frac{P_{Sidebands}(\omega_0 + \Delta\omega, 1Hz)}{P_{Carrier}}\right] \quad \textbf{(1.3)}$$

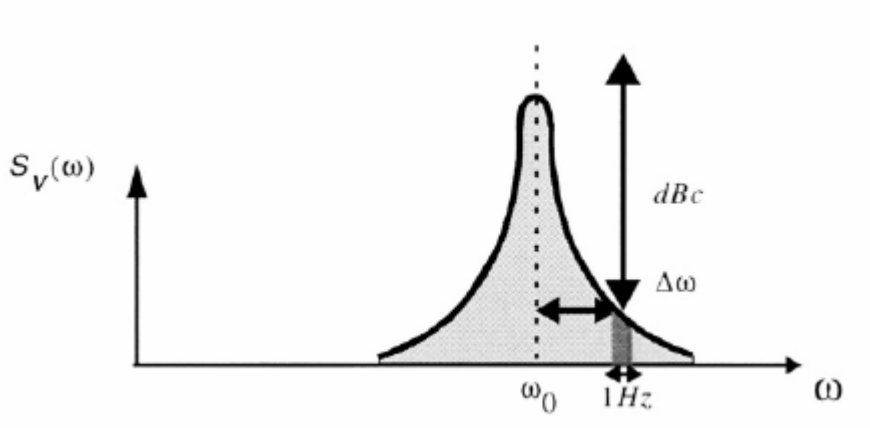

Figure 1.3 : Definition of phase noise

1.3 Popular Wireless Communication Standards

Wireless communication standards are defined by IEEE, ITU commonly. There exists lots of wireless communication standards widely used around, and varies to usage area. Some of generally used wireless communication standards are listed below.

1.3.1 Bluetooth

Bluetooth is a WPAN (Wireless Personal Area Network) standard. WPAN is the general name of wireless communication standards for small area such as home, office for personal usage. It is useful for communication between mobile phones, PDAs or computer hardware. The carrier frequency of Bluetooth is 2.4GHz and communication distance as low as 10 meters.

1.3.2 Wi-Fi

These standards cover much more are than WLANs, and it is valuable for communication between homes, networking applications.

1.3.2.1 802.11a

802.11a provide a high bandwidth and high date rates for data communications. The carrier frequency changes between 5.140GHz to 5.820GHz. It uses OFDM modulation technique.

1.3.2.2 802.11b

802.11b is cheapest and most popular standard in Wi-Fi, however data throughput is low as 11 Mbit/s. It uses demodulation technique as DQPSK, DBPSK. The carrier frequency of this standard varies between 2.4GHz to 2.483GHz. Channel spacing is between 1.5MHz to 20 MHz.

1.3.2.3 802.11g

The carrier frequency of 802.11g is between 2.4GHz to 2.5GHz. Also, this standard provides higher data throughputs (54Mbit/s) than 802.11b. It uses OFDM modulation technique like 802.11g.

Table 1.1 : Popular wireless communications standards specifications [1]

Standard	**Bluetooth**	**802.11a**	**802.11b**	**802.11g**
Usage	WPAN	WLAN	WLAN	WLAN
İdeal data rate	721kbps	54Mbps	11Mbps	54Mbps
Pratical data rate	500kbps	32Mbps	5Mbps	54Mbps
Distance	10m	100m	<100m	100m
Frequency	2402-2480 (EU)	5140-5250 (USA)	2402-2462 (America)	2402-2480
	2447-2473 (Spain)	5250-5350 (USA)	2412-2472 (EU)	
	2473-2495 (Japan)	5725-5820 (USA)	2483 (Japan)	
	2448-2482 (France)			
Modulation	Shaped Binary FM	OFDM: QPSK, QAM	FHSS: GFSK	
		OFDM: BPSK (5.5Mbps)	DSSS: DBPSK (1Mbps), DQPSK (2Mbps)	
		OFDM: 16QAM (26Mbps)	CCK: QPSK (11Mbps)	
		OFDM: 64QAM (54Mbps)		
User per channel	7 active, 200 passive	127	127	127
Channel Space	1MHz	OFDM: 20MHz	1.5MHz	1.5MHz
			FHSS: 1MHz	FHSS: 1 MHz
			DSSS: 25MHz	DSSS: 25 MHz
Number of channel	79		FHSS: 79	FHSS: 79
			DSSS: 11	DSSS: 11
Phase noise at VCO	-120dBc/Hz at 3MHz	-115dBc/Hz at1MHz	-115dBc/Hz at 1MHz	-115dBc/Hz at 1MHz

1.4 Objectives

Discussing pros and cons of active inductors on LC VCO is main objective of this thesis and, to design a LC VCO based on active inductors which supports 802.11b and 801.11g wireless communication standards via UMC013 0.13 µm CMOS

process and, to get analysis of active inductor effects on VCO performance is aimed. From previous considerations, design objectives can be listed as Table 1.2.

Table 1.2 : Design objectives

Design Method	LC VCO based on active inductor
Minimum Tuning Range	2.4GHz - 2.5GHz
Phase Noise at 1MHz	< -115dBc/Hz
Process	1.2V 0.13um UMC013

2. OSCILLATION THEORY AND OSCILLATORS

Oscillators are widely used in many analog or digital applications. Applications range from clock generations to carrier synthesis. Also, it can be designed for special applications such as random number generation circuit. [2]

Generally a VCO with a high performance phase noise is desirable in RF applications because of channel selection without interference with adjacent channels. In this section, oscillator theory and structures are explained.

2.1 Oscillation Theory

A feedback system is tender to oscillate and, it can be forced to oscillate. Some systems should be guarantied to not being in oscillation conditions such as amplifiers. Also, oscillator is a feedback system which depicted as Figure 2.1, and it is forced to oscillate.

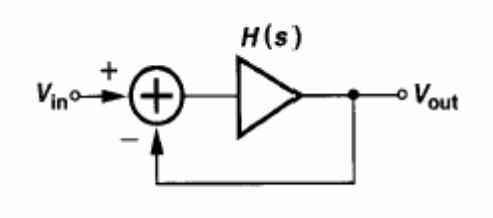

Figure 2.1 : Feedback systems

A system can oscillate when the gain of system should be infinite only at one frequency. If this condition is satisfied, the circuit amplifies its own noise and system will oscillate at this frequency without any input voltage. This meaning of this condition is given analytically as (2.1).

$$\frac{Vout(s)}{Vin(s)} = \frac{H(s)}{1+H(s)} = \infty \Rightarrow H(s) = -1 \qquad \textbf{(2.1)}$$

Other criteria for oscillation condition, total phase shift of closed loop should be 360 degrees. Whereas phase shift of H(s) should be 180 degree in a negative feedback

system, phase shift should be 360 degree in a positive feedback system for oscillation.

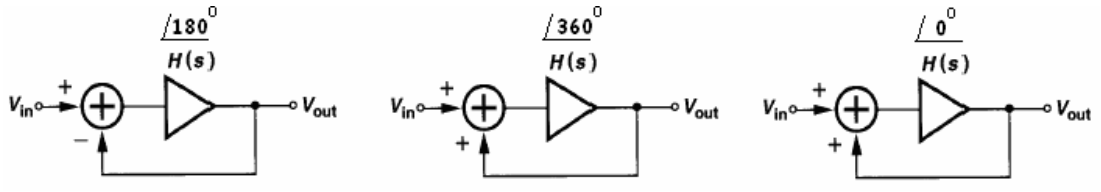

Figure 2.2 : Phase conditions of oscillation for negative and positive feedback systems

These two conditions are known as "Barkhausen's Criteria". Practically, loop gain, |H(s)| should be at least 3 or 4 to start up oscillation. While oscillation amplitude grows, the loop gain will decrease to 1 after oscillation starts.

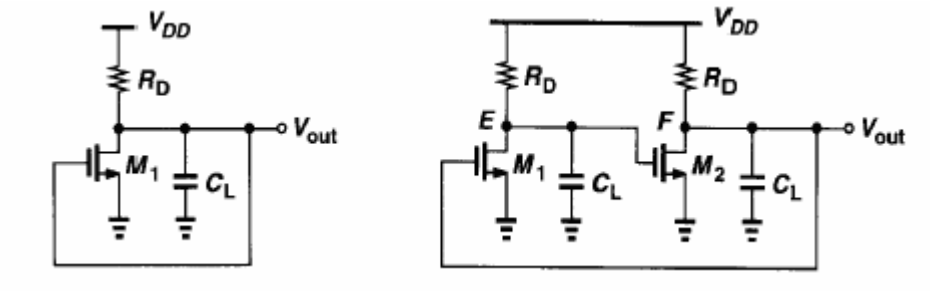

Figure 2.3 : Some feedback systems without oscillation

In Figure 2.3, first circuit will not oscillate because of maximum total phase shift 270 at infinite frequency. Second circuit exhibits a positive feedback near zero frequency and, system node voltages will remain at DC levels and do not oscillate. Analytically, when total phase shift is 360 degrees, the gain should be at least 1, and this condition is ensured at near zero frequencies.

Generally, oscillators are implemented as ring oscillators or LC oscillator in CMOS technology.

2.1.1 Ring Oscillators

Ring oscillators consist of at least three poles which ensure phase condition for a negative feedback system, so it needs at least three stages. Each stage introduces a maximum phase shift of 90 degrees in the closed loop function. For three stage ring oscillator, each stage introduces 60 degrees phase shift and total phase shift becomes 360 degrees for positive feedback configuration.

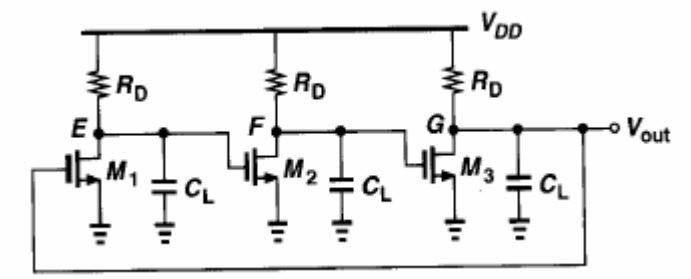

Figure 2.4 : Simple three stage ring oscillator

Ring oscillator can be implemented with three cascading common-sources stages as shown as Figure 2.4. If each stage is same, the circuit will oscillate at $\sqrt{3}\omega_0$ where ω_0 is definition of amplifier bandwidth. Oscillation frequency of this circuit depends on C_L capacitor so on rising and falling times. The oscillation frequency can be calculated as $1/(3(T_{rising} + T_{falling}))$.

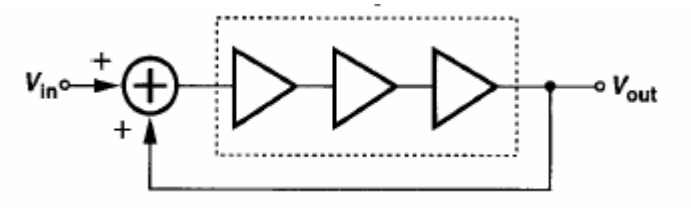

Figure 2.5 : Linear model of a simple ring oscillator

In literature, lots of ring oscillators are proposed. The major advantages of ring oscillator with negative feedback there is no need inductor which decrease size and cost. Major disadvantages of ring oscillator, there is no noise filtering element behavior like a LC tank. As a result, phase noise performance of ring oscillators generally poor in comparison with LC VCO [3].

2.1.2 LC Oscillators

The second circuit of Figure 2.3 doesn't oscillate since the positive feedback circuit has a gain at near dc frequencies. If the circuit has only one gain at desired frequency, this circuit can oscillate. The block of diagram of desired oscillator using a resonator circuit is given below.

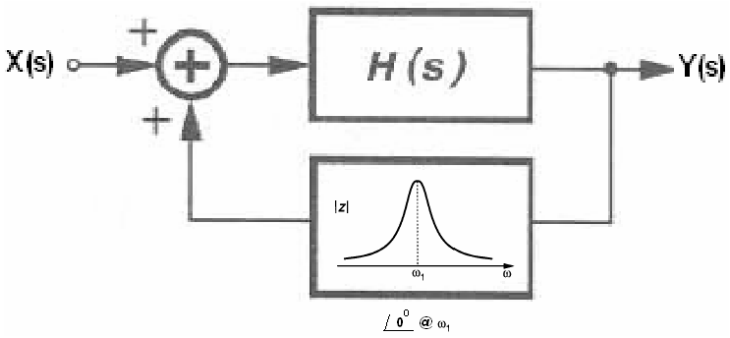

Figure 2.6 : Block diagram of LC oscillator

The block diagram can be implemented using LC tank a resonator circuit. Resonator frequency of an ideal LC tank is given as (2.2).

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.2}$$

An ideal LC tank consists of parallel inductor and capacitor, and gain is infinite at resonant frequency. However a practical LC tank has parasitic resistive elements and gain of resonator is not infinite.

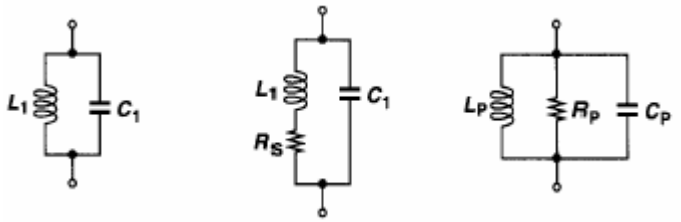

Figure 2.7 : Oscillator tank models: Ideal LC tank, LC tank with series resistance of inductor, LC tank with parallel resistance

Quality factor is definition of stored energy over dissipated energy ratio which can be an indication of how much of the energy is lost. Quality factor is infinite for an ideal LC tank. Quality factor of LC tank with series resistance of inductor can be calculated as (2.3).

$$Q = \frac{L_1 \omega}{R_s} \tag{2.3}$$

Moreover, LC tank with series resistance of inductor can be represented as LC tank with parallel resistance as shown in Figure 2.7.

$$C_p = C_1 \tag{2.4}$$

$$L_p \approx L_1 \tag{2.5}$$

$$R_P \approx Q^2 R_S \tag{2.6}$$

$$\omega_0 = \frac{1}{\sqrt{L_p C_p}} \tag{2.7}$$

Resonant frequency of LC tank with parallel resistance is given below. The Bode diagram of LC resonator is shown as Figure 2.8.

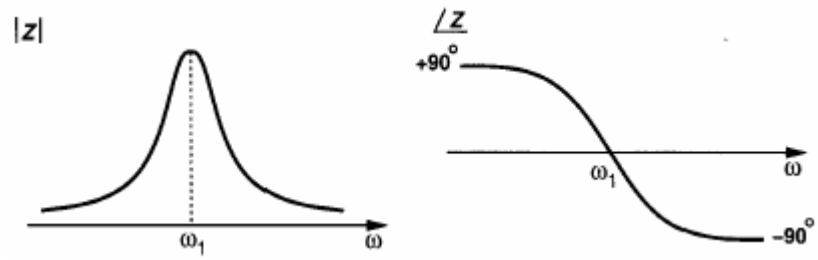

Figure 2.8 : Characteristics of an LC resonator

2.1.2.1 Crossed-Coupled Oscillators

If a LC tank is used as a load at stages instead of resistor in second circuit of Figure 2.3, the circuit can oscillate since the total phase shift around the loop is zero at resonance frequency. The loop gain should be at least $g_{m1}R_p g_{m2}R_p \geq 1$ for start-up of oscillation. Cross-coupled oscillator structure is depicted in Figure 2.9.

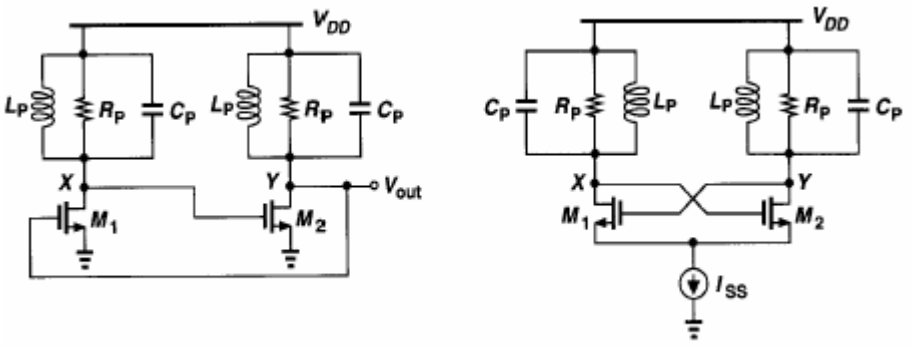

Figure 2.9 : Cross-coupled oscillator and redraw of cross-coupled oscillator

The crossed-coupled oscillator structure is fully symmetric, and if sizes of stages are the same, node Vx and node Vy oscillate differentially. Vy/Vx and Vx/Vy voltage gain should be equal due to the equal stages. Vy=-Vx is obtain due to the -180 degrees phase shift. At the beginning of oscillation, Vx and Vy are equal to V_{DD}, and the current of M1 and M2 transistor is equal Iss/2. When system oscillates, a stage should steer tail current more than a other stage instantaneously which means Vx and Vy behave differentially.

Differential oscillation capability provides a more linear oscillation due to the elimination of odd harmonics of output.

2.1.2.2 Colpitts Oscillators

Oscillators can be implemented with one transistor which provides a sufficient gain such as Colpitts oscillators as shown if Figure 2.10.

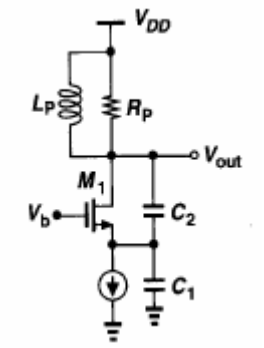

Figure 2.10 : Colpitts Oscillator

Colpitts oscillator needs four times larger gm from respect to cross-coupled topology which means eight times larger area for M1 transistor (4 times larger area for NMOS crossed-coupled oscillator). This is also critical if quality factor of the inductor is low. [4]

2.2 Analysis of One Port Oscillators

Oscillators can be analyzed with "negative resistance" concept which is an alternative point of oscillation phenomenon. When an impulse is stimulated to a simple LC tank without any parasitic resistance, LC tank keeps this energy and oscillates at resonant frequency. If LC tank has a parasitic resistance, the energy will be consumed by parasitic resistance, and the oscillation will be weaken in every cycle. If an LC oscillator oscillates, active element should behave like negative resistance which equal to parasitic resistance Rp shown as Figure 2.11.

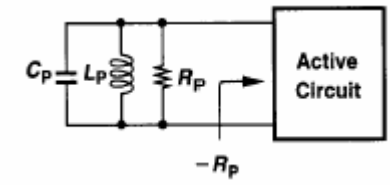

Figure 2.11 : Using active circuit as a negative resistance

In Figure 2.12, negative resistance of a crossed-coupled LC oscillator is analyzed. To calculate resistance between Y and X nodes, tail current is opened, and Vz voltage is applied.

$$Vy = Vz + Vx \tag{2.8}$$

$$Iz = gmVx \tag{2.9}$$

$$gmVx = -gm(Vz + Vx) \tag{2.10}$$

By combining (2.9) and (2.10), negative resistance is calculated as below (2.11).

$$\frac{Vz}{Iz} = -\frac{2}{gm} \tag{2.11}$$

The resistance between node X and node Y is twice as Rp so; gm value is given in (2.12).

$$-\frac{2}{gm} = 2R \Rightarrow gm = \frac{1}{Rp} \tag{2.11}$$

Practically, gm value should be designed 3-4 times larger than 1/R.

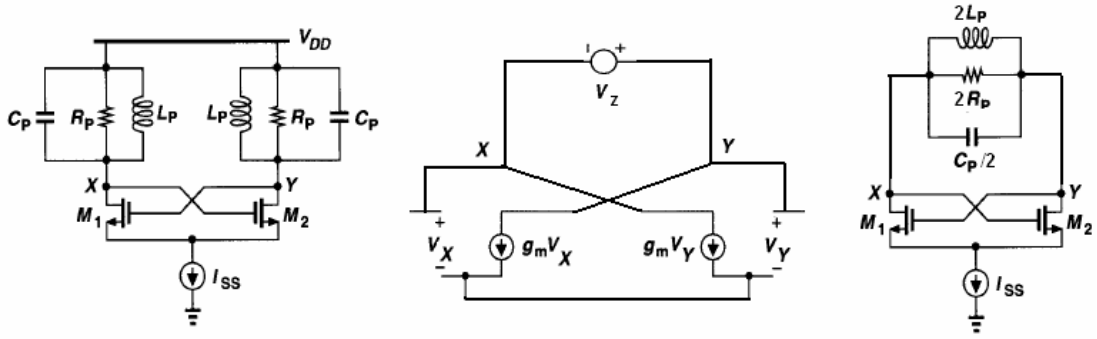

Figure 2.12 : A Crossed-coupled oscillator, Negative resistance calculation of crossed-coupled oscillator, Analysis of cross-coupled oscillator based on negative resistance

Moreover, using negative resistance concept the following circuit shown in Figure 2.13 can be implemented. [4]

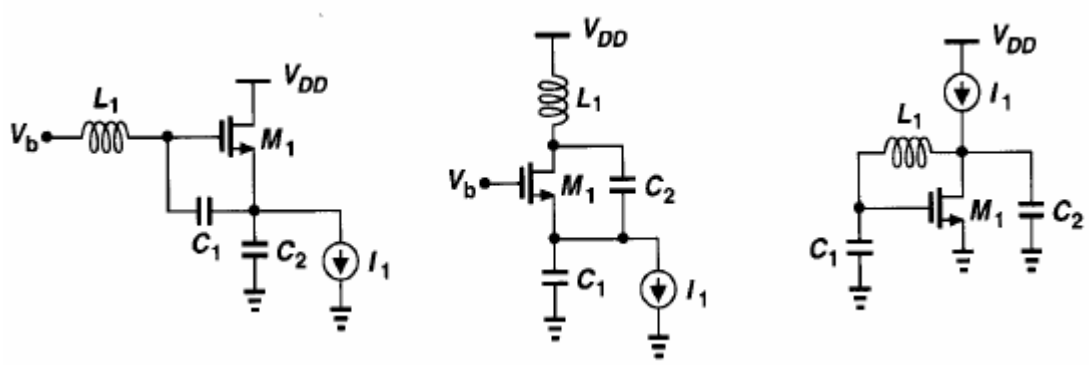

Figure 2.13 : Oscillator topologies derived from negative resistance concept

2.3 VCO Design Considerations

2.3.1 Center Frequency

Center frequency of VCO depends on application and the center frequency varies up to 140GHz [5]

2.3.2 Tuning Range

Variation of center frequency with process and temperature, and application determine tuning range. To prevent process variation, a larger tuning range is desired.

Another important thing is noise sensitivity of control voltage or current which directly turn to phase noise. Gain of VCO is defined as (2.14). Gain of VCO must be minimized considering required minimum gain of VCO.

$$K_{VCO} = \frac{\omega_2 - \omega_1}{V_2 - V_1} \tag{2.14}$$

2.3.3 Tuning Linearity

Generally, a linear K_{VCO} is desired for settling behavior of PLL. [4]

2.3.4 Output Amplitude

Large output amplitude is preferred because of make less sensitive to noise to oscillator.

2.3.5 Power Dissipation

Power dissipation is generally important when all system is considered since tradeoffs between speed, noise and power consumption. [4]

2.3.6 Supply and Common-Mode Rejection

Oscillator's noise immunity to supply and common-mode noise is desired high. Especially single-ended oscillator is suffered, and differential path for oscillation and control line is preferable.

2.3.7 Phase noise

Phase noise is related with signal purity. Oscillator outputs are not perfectly periodic, and it varies at vicinity of oscillation frequency. Phase noise and jitter is very important for wireless communications.

2.4 Phase Noise Analysis of a Basic LC VCO

A basic LC tuned oscillator can be shown as Figure 2.14. Rp represents parallel resistance of LC tank, Rc is parasitic series resistance of capacitor C, and Rl, which mostly effective on phase noise, symbolizes parasitic series resistance of inductor L.

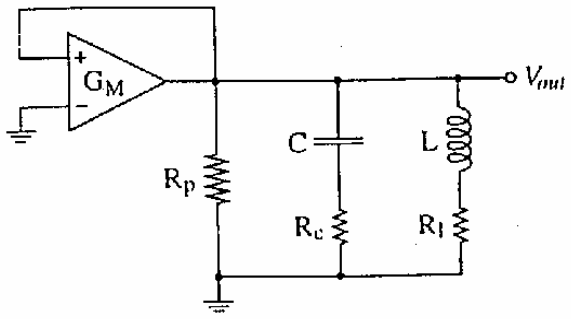

Figure 2.14 : Configuration of a basic LC tuned oscillator

To analyze phase noise, noise contributions of each parasitic should be analyzed separately. [6]

2.4.1 Noise Contribution of Parallel Resistance

If Figure 2.15 is redrawn with a noisy parallel resistance Rp, a noise source $\overline{di}_{Rp}^2$ which is associated with temperature is included to oscillator. Noise source $\overline{di}_{Rp}^2$ is expressed as (2.15) and, shown in Figure 2.15.

$$\overline{di}_{Rp}^2 = \frac{4kT}{Rp} df \tag{2.15}$$

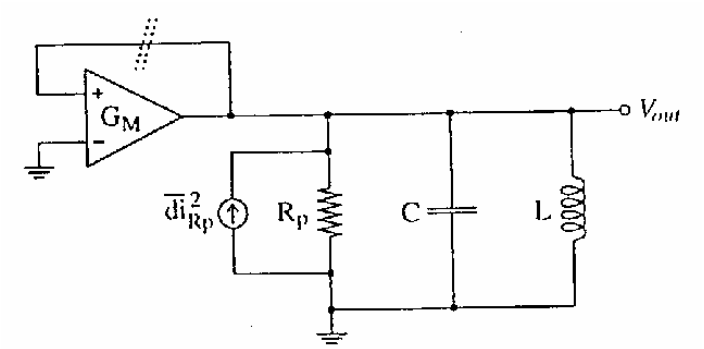

Figure 2.15 : Configuration of a basic LC tuned oscillator with noisy Rp

To calculate oscillation frequency of this configuration the loop transfer function is extracted by cutting dot lines in Figure 2.15. The loop transfer function is calculated as shown in (2.16).

$$T_{loop,Rp}(s) = G_M \frac{sL}{1 + s\frac{L}{Rp} + s^2 LC} \tag{2.16}$$

If the system is in oscillation, the imaginary part of poles must be zero. Imaginary part can be expressed as (2.17).

$$IMAG\left(T_{loop,Rp}(s)\right) = G_M \frac{\omega L.(1-\omega^2 LC)}{(1-\omega^2 LC) + \omega^2\left(\frac{L}{C}\right)^2} \tag{2.17}$$

And imaginary part is zero when (2.18) is satisfied.

$$IMAG\left(T_{loop,Rp}(s)\right) = 0 \Rightarrow \omega = \omega_0 = \frac{1}{\sqrt{LC}} \tag{2.18}$$

Moreover, loop transfer function should be one at resonant frequency due to the oscillation of system. This condition is stratified when Gm transconductance compensates loses of system as expressed in (2.19).

$$G_M = \frac{1}{Rp} \tag{2.19}$$

To calculate noise of this parasitic parallel resistance Rp on oscillator output, noise source $\overline{di}_n^2$ must be processed in close loop using transfer function shown as (2.20).

$$T_{loop,Rp}^2(s) = \frac{\overline{dV}_{out}^2}{\overline{di}_{Rp}^2}(s) = \left[\frac{sL}{1 + sL(G_M - \frac{1}{R_p}) + s^2LC}\right]^2 \tag{2.20}$$

Phase noise is defined at $\Delta\omega$ form the carrier ω_0, so $T_{loop,Rp}^2(\omega_0 + \Delta\omega)$ is necessary to calculate noise $\Delta\omega$ form the carrier ω_0. Because inverse of $T_{loop,Rp}(\omega_0 + \Delta\omega)$ simplifies the calculation of noise at oscillator, $H_{loop,Rp}(\omega_0 + \Delta\omega)$ is defined as (2.21) to get equation of $T_{loop,Rp}^2(\omega_0 + \Delta\omega)$.

$$H_{loop,Rp}(\omega_0 + \Delta\omega) = \frac{1}{T_{loop,Rp}(\omega_0 + \Delta\omega)} \tag{2.21}$$

If (2.21) is approximate with a linearization at resonant frequency, it can be shown as (2.22).

$$H_{loop,Rp}(\omega_0 + \Delta\omega) = H_{loop,Rp}(\omega_0) + \frac{dH_{loop,Rp}(\omega_0 + \Delta\omega)}{d\omega}\Delta\omega \tag{2.22}$$

At oscillation, $H_{loop,Rp}(\omega_0)$ is equal to zero, and second part can be expressed as (2.23).

$$\frac{dH_{loop,Rp}(\omega_0 + \Delta\omega)}{d\omega}\Delta\omega = \frac{dH_{loop,Rp}(\omega_0 + \Delta\omega)}{d\omega}\omega_0 . \frac{\Delta\omega}{\omega_0} = 2j\sqrt{\frac{C}{L}}\frac{\Delta\omega}{\omega_0} \tag{2.23}$$

So $T_{loop,Rp}^2(\omega_0 + \Delta\omega)$ can be calculate as (2.24),

$$T_{loop,Rp}^2(\omega_0 + \Delta\omega) \approx \left|\frac{1}{2j}\sqrt{\frac{L}{C}}\right|^2\left(\frac{\omega_0}{\Delta\omega}\right)^2 = \frac{1}{4(\omega_0 C)^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{2.24}$$

Consequently, noise density is calculated at very close to resonant frequency at the output of oscillator as;

$$\overline{dV}_{out}^2(\omega_0+\Delta\omega)=T_{loop,Rp}^2(\omega_0+\Delta\omega)\ \text{x}\ \overline{di}_n^2 \tag{2.25}$$

$$\overline{dV}_{out}^2(\omega_0+\Delta\omega)=\frac{1}{4(\omega_0 C)^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\ \text{x}\ \frac{4kT}{Rp}df \tag{2.26}$$

$$\overline{dV}_{out}^2(\omega_0+\Delta\omega)=kT\frac{1}{R_p(\omega_0 C)^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 df \tag{2.27}$$

(2.27) represents the noise contribution of parallel resistance at the output of oscillator. This equation shows that for a low noise contribution, tank capacitance should be selected as large and parallel parasitic resistance of tank should be high.

2.4.2 Noise Contribution of Inductor Series Resistance

The oscillator basic configuration with a noisy inductor is presented in Figure 2.16. The same noise contribution calculation of parallel resistance steps are performed for noisy inductor. First open loop transfer function, $T_{loop,R_L}(s)$, must be calculated, and $T_{loop,R_L}(s)$ is expressed in (2.28). Moreover, G_M transconductance when configuration is in oscillation and resonant frequency are obtained using open loop transfer function as (2.29) and (2.30).

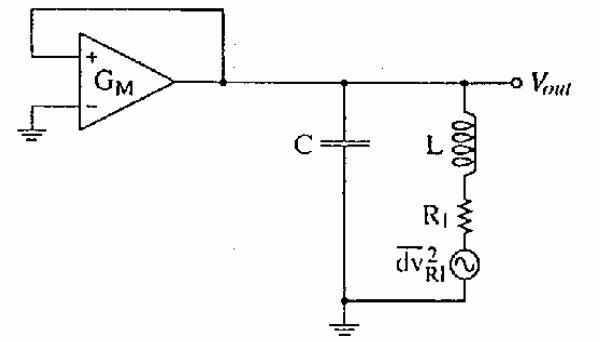

Figure 2.16 : Configuration of a basic LC tuned oscillator with noisy inductor

$$T_{loop,R_L}(s)=G_M\frac{R_l+sL}{1+sR_lC+s^2LC} \tag{2.28}$$

$$IMAG\left(T_{loop,R_L}(s)\right)=0\Rightarrow\omega=\omega_0=\frac{1}{\sqrt{LC}}\sqrt{1-\frac{R_l^2C}{L}} \tag{2.29}$$

$$G_M = R_l \frac{C}{L} \approx R_l (\omega_0 C)^2 \quad \textbf{(2.30)}$$

The noise transfer function at frequency close to carrier ω_0 as $\Delta\omega$ is found using same method as mentioned in noise contribution of parallel parasitic resistance, Rp. $T^2_{loop,R_L}(\omega_0 + \Delta\omega)$ is given in (2.31).

$$T^2_{loop,Rp}(\omega_0 + \Delta\omega) = \frac{\overline{dV}^2_{out}}{\overline{dV}^2_{R_L}}(s) \approx \left(-\frac{1}{2}\left(\frac{\omega_0}{\Delta\omega}\right)\right)^2 \quad \textbf{(2.31)}$$

$$\overline{dV}^2_{out}(\omega_0 + \Delta\omega) = T^2_{loop,Rp}(\omega_0 + \Delta\omega) \text{ x } \overline{dV}^2_{R_L} \quad \textbf{(2.32)}$$

$$\overline{dV}^2_{out}(\omega_0 + \Delta\omega) = \frac{1}{4}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \text{ x } 4kTR_L df \quad \textbf{(2.33)}$$

$$\overline{dV}^2_{out}(\omega_0 + \Delta\omega) = kTR_L\left(\frac{\omega_0}{\Delta\omega}\right)^2 df \quad \textbf{(2.34)}$$

(2.34) represents the noise contribution of series resistance of inductor at the output of oscillator. This equation shows that for a low noise contribution of inductor, series parasitic resistance of inductor should be as much as low.

2.4.3 Noise Contribution of Capacitor Series Resistance

Noise contribution of capacitor series resistance, R_C can be analyzed with same method as R_L. The transconductance G_M expression and noise contribution of R_C are given in (2.35) and (2.36).

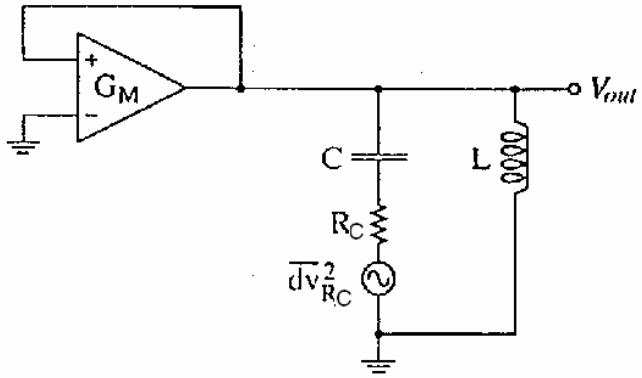

Figure 2.17 : Configuration of a basic LC tuned oscillator with noisy capacitor

$$G_M = R_C \frac{C}{L} \approx R_C(\omega_0 C)^2 \tag{2.35}$$

$$\overline{dV}_{out}^2(\omega_0 + \Delta\omega) = kTR_C\left(\frac{\omega_0}{\Delta\omega}\right)^2 df \tag{2.36}$$

2.4.4 Definition Effective Resistance and Quality Factor of LC tank

Effective resistance is the one of the most import term in LC-VCO and it shows equivalent of all series parasitic resistances in one term. Effective resistance value play an important on phase noise also power consumption due to GM value. Effective resistance is defined as (2.37).

$$R\text{eff} = R_C + R_L + \frac{1}{R_P(\omega_0 C)^2} \tag{2.37}$$

Transconductance, G_M, of oscillator should be compensate all loses of LC tank behave as negative resistance. Its value is given (2.38).

$$G_M = R\text{eff}(\omega_0 C)^2 \tag{2.38}$$

The quality factor of LC tank is another important factor of LC tuned oscillators. It is combination of three quality factors due to the three parasitic resistances. The quality factor expression of three parasitic resistances can be shown as in Figure 2.18 separately.

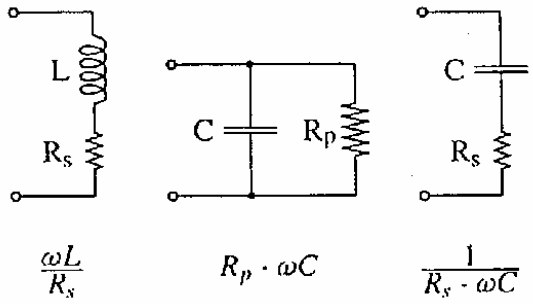

Figure 2.18 : Quality factors of some circuits

Quality factor of LC tank at resonant frequency can be express as a function of effective resistance shown as (2.39).

$$Q = \frac{1}{\frac{1}{Q_{R_p}} + \frac{1}{Q_{R_L}} + \frac{1}{Q_{R_C}}} = \frac{1}{\frac{1}{Rp(\omega_0 C)} + R_L(\omega_0 C) + R_C(\omega_0 C)} = \frac{1}{R\text{eff}(\omega_0 C)} \tag{2.39}$$

Also, the total noise contribution of LC tank can be found as (2.40) as function of Reff.

$$\overline{dV}^2_{out}(\omega_0 + \Delta\omega) = kTR\text{eff}\left(\frac{\omega_0}{\Delta\omega}\right)^2 df \quad \textbf{(2.40)}$$

2.4.5 Noise Contribution of Negative Resistance

Negative resistance is an active element and, also it is a noise source. It can be modeled as output current noise source as (2.41).

$$\overline{di}^2_{G_M} = 4kTF_{G_M} G_M df \quad \textbf{(2.41)}$$

F_{G_M} is the excess noise factor of amplifier in (2.41), The noise contribution of active element is calculated like noise contribution of parallel resistance Rp because of parallel noise source of LC tank. It can be obtained as (2.42).

$$\overline{dV}^2_{out}(\omega_0 + \Delta\omega) = kT\frac{F_{G_M} G_M}{(\omega_0 C)^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 df \quad \textbf{(2.42)}$$

If system oscillates, (2.42) can be modified as (2.43) by substitution of G_M with its equivalent as shown (2.38)

$$\overline{dV}^2_{out}(\omega_0 + \Delta\omega) = kTR\text{eff}A\left(\frac{\omega_0}{\Delta\omega}\right)^2 df \quad \textbf{(2.43)}$$

A is definition of αF_{G_M} where α represents the amount noise the actual noisy amplifier generates in excess of an ideal oscillator and A is named as amplifier noise factor and usually larger than 1.

2.4.6 Total Noise and Phase Noise of LC VCO

The total noise of LC VCO output can be summarized as below equations. [6]

Total Noise: $\overline{dV}^2_{out}(\omega_0 + \Delta\omega) = kTR\text{eff}\left[1 + A\right]\left(\frac{\omega_0}{\Delta\omega}\right)^2 df \quad \textbf{(2.44)}$

Oscillation Frequency: $\omega_0 = \frac{1}{\sqrt{LC}} \quad \textbf{(2.45)}$

Effective Resistance: $R\text{eff} = R_C + R_L + \frac{1}{R_P(\omega_0 C)^2}$ **(2.46)**

Noise Amplication Factor: $A = \alpha F_{G_M}$ **(2.47)**

Transconductance: $G_M = R\text{eff}(\omega_0 C)^2$ **(2.48)**

Phase noise of LC VCO can be calculated as given (2.49). If oscillation amplitude of VCO is equal to V_A, phase noise can be expressed as below.

$$L(\Delta\omega) = 10\log\left[\frac{P_{Sidebands}(\omega_0 + \Delta\omega, 1Hz)}{P_{Carier}}\right] \quad \textbf{(2.49)}$$

$$L(\Delta\omega) = 10\log\left[\frac{\int_{\Delta\omega-0.5}^{\Delta\omega+0.5} kTR\text{eff}\left[1 + A\right]\left(\frac{\omega_0}{\Delta\omega}\right)^2 df}{(V_A)^2/2}\right] \quad \textbf{(2.50)}$$

$$L(\Delta\omega) = 10\log\left[\frac{kTR\text{eff}\left[1 + A\right]\left(\frac{\omega_0}{\Delta\omega}\right)^2}{(V_A)^2/2}\right] \quad \textbf{(2.51)}$$

It is sure that if the oscillator amplitude is larger, phase noise will decrease. Also, it will increase SNR ratio. However, there is a limitation of amplitude because maximum oscillation amplitude depends on IC process and structure of LC VCO. Besides amplitude of oscillation, as it seen Reff is one of the most important factors on phase noise.

For instance to get phase noise -115dBc/Hz at 1MHz offset when oscillation frequency is 2.4GHz and, amplitude is 1V, Maximum Reff should be 16.7 ohms as shown in (2.52).

$$R\text{eff} = \frac{10^{\frac{-115dBc/Hz}{10}}.(1)^2/2}{0.41.10^{-21}\left[1+3\right].\left(\frac{2.4GHz}{1MHz}\right)} = 16.7ohms \quad \textbf{(2.52)}$$

3. ACTIVE INDUCTORS

In many blocks such as oscillators, filters, phase shifters, low noise amplifiers, impedance matching circuitry, biasing needs inductor, an essential component in RF and, popularly on-chip inductor are implemented as a passive element which still remains a challenging task. [7, 8, 9, 10, 11] However inductors can be implemented as using active components. Using active inductors bring some advantages and disadvantages to circuits in comparison passive inductors.

3.1 Advantages of Active Inductors

3.1.1 Chip Area

The increasing popularity and growth of wireless communications, the cost of chips becomes more important especially in CMOS technology due to the shrinking of sizes and low cost availability of the process. Increasing size of chips can cause to increase costs too and, most of the time, the inductor will be a main reason in determining the total chip area where higher inductance values are necessary.

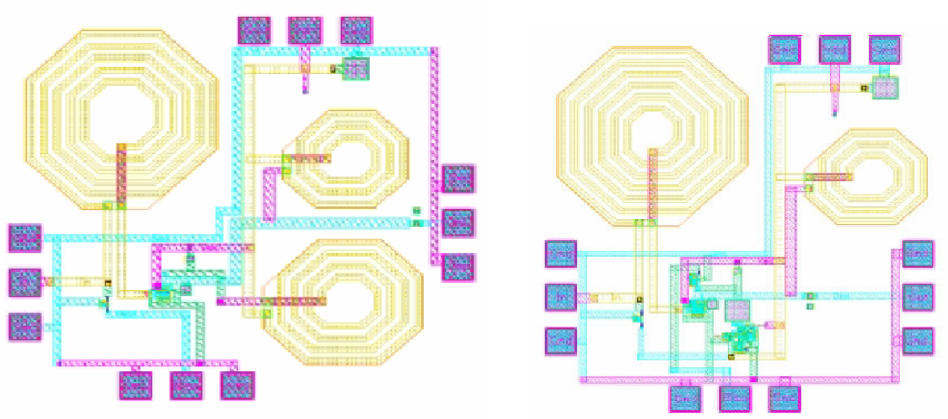

Figure 3.1 : LNA implementation with passive and active inductor

In Figure 3.1, LNA implementation is shown in 0.3um CMOS. Silicon area of the entire LNA without active inductor requires A=0.83 mm^2 but, silicon area is A=0.6 mm^2 with active inductor. The required silicon is reduced by more than 25% due to the active inductor. [12]

3.1.2 Tunability

Active inductor implies a tuning facility of inductor value. Inductor value depends on active elements' transconductances and transconductance can be tuned by current source with a wide variety.

Moreover, tunability function of active inductors is an advantage in comparison tunability of varactors. Capacitance are controlled by a voltage in varactors, but generally, the voltage-capacitance characteristic can only be considered to be linear in a rather small range of the control. A nonlinear voltage-capacitance characteristic is more sensitive for noise on the control voltage and in turn directly to noise.

3.1.3 High Quality Factor

Quality factors of active inductors can be higher than on-chip passive inductors since active inductor parasitic series resistance and inductor value can be modified separately. Some quality factor of active inductor values are given in Table 3.1 on literature.

3.1.4 Higher Inductance Value

It is hard to design an on-chip passive inductor with a high value. Whereas spiral inductor value varies between 0.9nH and 12nH in UMC013 process, the active inductor values varies at a wide range between 2.5nH-300nH as shown as Table 3.1

Table 3.1 : Comparison of active inductor on literature

Technology	0.13um/1.5 V[10]	0.35um/1.5 V [9]	0.6um [8]	0.13um/1.2 V [7]
Inductive bandwidth	n. a.	6.8MHz–2.97GHz	800MHz–2.5GHz	300MHz–7.32GHz
L (nH)	2.5–13	30.9	15–300	38–144
Qlmax	100@5GHz	434@1GHz	350@1GHz	3900@5.75GHz
Pdis (mW)	18.6/68	0.6	n. a.	1
Max. input voltage swing	n. a.	4.5 mV	n. a.	18 mV
Dynamic range	n. a.	30.8 dB	n. a.	30 dB
Noise	n. a.	91.3 uV*	n. a.	3.1 nV/Hz

*Integrated over 500 MHz bandwidth

3.2 Disadvantages of Active Inductors

3.2.1 Noise Contribution

Noise of active inductors is higher than on-chip passive inductors' noise and, associated with active indutors is the biggest problem due to the their noise contribution to the circuit. It will be shown in section 3.4 and section 3.5 that these noise sources have very bad effect on the phase noise of LC tuned oscillator.

3.2.2 Dynamic Range

Dynamic range of active inductors is lower than on-chip passive inductors because of input voltage swing of active inductor is too limited as tens of mV. The input voltage swing is norrow since the active elements operates in a limited region(this is saturation region for CMOS process) to keep inductor behaviour.

3.2.3 Bandwidth

Active inductors has an operation bandwidth. Impedance and phase characteristics of an active inductor has three regions in orders; resistive region, inductive region and capacitive region. These regions are defined as poles and zeros placement in root locus.

3.2.4 Power consumption

As it clear, active inductors consume power whereas on-chip passive inductors do not.

3.3 Realization of Active Inductors

Realization of active inductors can be implemented by using gyrator elements.

3.3.1 Gyrator: Impedance Inverter

An ideal gyrator is a linear two port network. Ideally, it doesn't consume energy and doesn't store energy. [11] The concept of gyrator was emerged by B.D.H Telegen. Also, gyrator can be called as positive impedance inverter. [13] Using a gyrator element a capacitor circuit can behave like active inductor and vice versa.

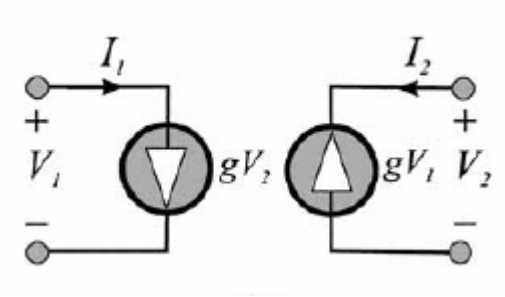

Figure 3.2 : The two port equivalent of an ideal gyrator

In Figure 3.2 ideal gyrator equivalent model is given by output voltages and corresponding currents. The basic characteristic of an ideal gyrator is defined below.

$$\begin{bmatrix} I1 \\ I2 \end{bmatrix} = \begin{bmatrix} 0 & g \\ -g & 0 \end{bmatrix} \begin{bmatrix} V1 \\ V2 \end{bmatrix} \tag{3.1}$$

The g parameter is called as gyration ratio of active network. If a capacitor is connected to output port of a gyrator as shown in Figure 3.3, input impedance can be found as (3.2).

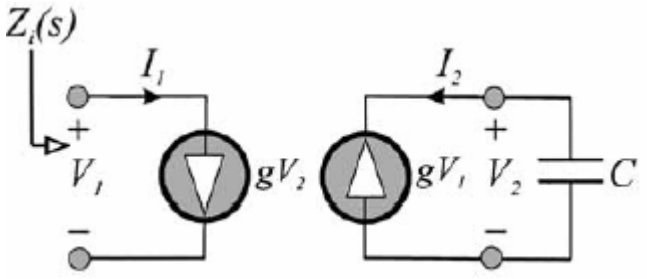

Figure 3.3 : A capacitive terminated gyrator

(3.2) proves that an ideal gyrator transforms an ideal capacitor at output port to an inductor at input port with a function of gyrator ratio g and capacitor.

$$Zi(s) = \frac{V1}{I1} = \frac{V1}{gV2} = \frac{V1}{g\dfrac{gV1}{sC}} = \frac{sC}{g^2} = \frac{C}{g^2}s \tag{3.2}$$

3.3.2 Gyrator Realization with Transconductors

Logical basis for the network realization of a gyrator can be provided by transconductor elements, OTAs. The equivalent model OTA and, gyrator realization terminated with a capacitor is shown as Figure 3.4

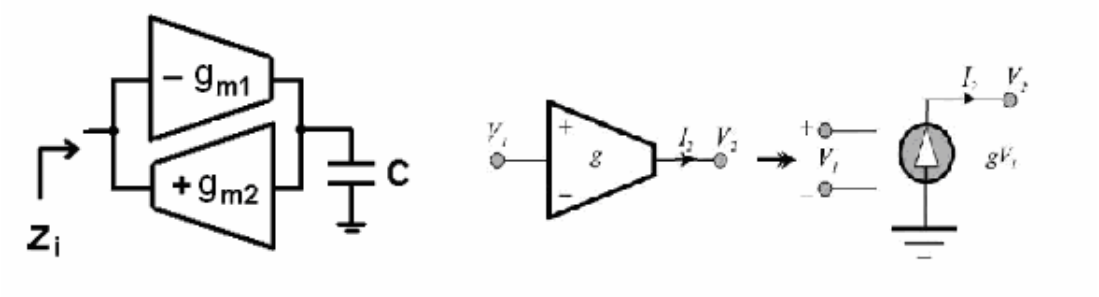

Figure 3.4 : Realization of active inductor with OTAs and equivalent model of OTA

The ideal active inductor value is given below based on OTAs' transconductance. The transconductance values can be design as function a control current or voltage sources so, inductor value can be tuned.

Practically, transconductance elements have parasitic resistances and capacitors. Input parasitic resistance of a transconductance element is generally too large because this input is driven as voltage. Output resistance of transconductance is ranging at least tens to several hundred kOhms. Input capacitance of transconductance is large due to the gate-source capacitance and gate-source overlap capacitance whose value varies ten to low hundreds of femtofarads in submicron MOS technologies. On the other hand, output capacitance value is changing between tens to a few hundreds when common-source MOS architecture is used. [6] Figure 3.5 shows gyrator-C realization with parasitic and its equivalent passive model.

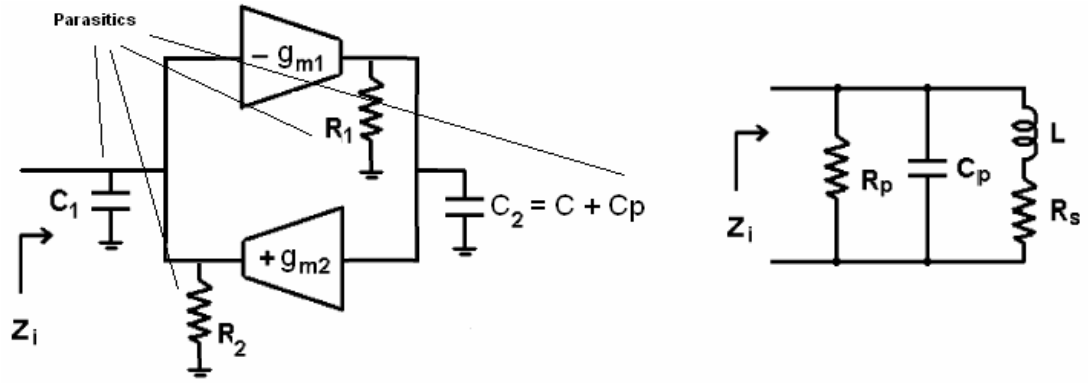

Figure 3.5 : Active inductor realization with OTAs with parasitic and its equivalent passive model

Input impedance of gyrator-C realization can be calculated as (3.3). Also, input impedance of equivalent model is given as (3.4).

$$Zi = \frac{\frac{1}{C_1}\left(s + \frac{G_2}{C_2}\right)}{s^2 + \frac{G_1C_2 + G_2C_1}{C_1C_2}s + \frac{g_{m1}g_{m2} + G_1G_2}{C_1C_2}} \quad \textbf{(3.3)}$$

$$Zi = \frac{\frac{1}{C_p}\left(s + \frac{R_S}{L}\right)}{s^2 + \frac{C_PR_SR_P + L}{C_PLR_P}s + \frac{R_S + R_P}{C_PLR_P}} \quad \textbf{(3.4)}$$

Values of passive equivalent model can be found by equalizing (3.3) and (3.4).

$$L = \frac{C_2}{g_{m1}g_{m2}} \quad \textbf{(3.5)}$$

$$R_s = \frac{G_2}{g_{m1}g_{m2}} \quad \textbf{(3.6)}$$

$$C_p = C_1 \quad \textbf{(3.7)}$$

$$R_p = \frac{1}{G_1} \quad \textbf{(3.8)}$$

It is obvious that gyrator-C realization has two poles and a zero from (3.4). Gyrator-C element has regions according to its behavior which are defined by zero and pole locations.

For instance, g_{m1}=5mS, g_{m2}=10mS, C_1=60fF, C_2=500fF, R_1=R_2=20kOhm is selected for gyrator-C realization and, the Bode diagram of that configuration is shown as Figure 3.6.

In the Figure 3.6, first region is defined as resistive region which is start with 0Hz to gyrator-C's zero location which is 179MHz in this example. In resistive region the magnitude of impedance is nearly constant so it is not modified by frequency.

Second region is defined as inductive region which starts with zero location and, it is limited by poles locations. Inductive region is between 179MHz and 6.5GHz in Figure 3.6. In inductive region, phase curve is close to 90 degree which is characteristic of an inductor. In practically, inductive region is not useful at full bandwidth because of phase degree and to get a constant inductor value.

In Figure 3.6, useful inductor bandwidth for a pure inductor starts with 1.36GHz since phase error is less than 1 degree and it ends up when inductor value is started to being modified by frequency. The limit of useful inductor value is 2.42GHz in Figure 3.6 because the derivation of magnitude (dB) of impedance starts to differ than 20dB/dec. The maximizing bandwidth will provide a constant inductor value and it depends on parasitic input capacitor of gyrator-C realization.[7]

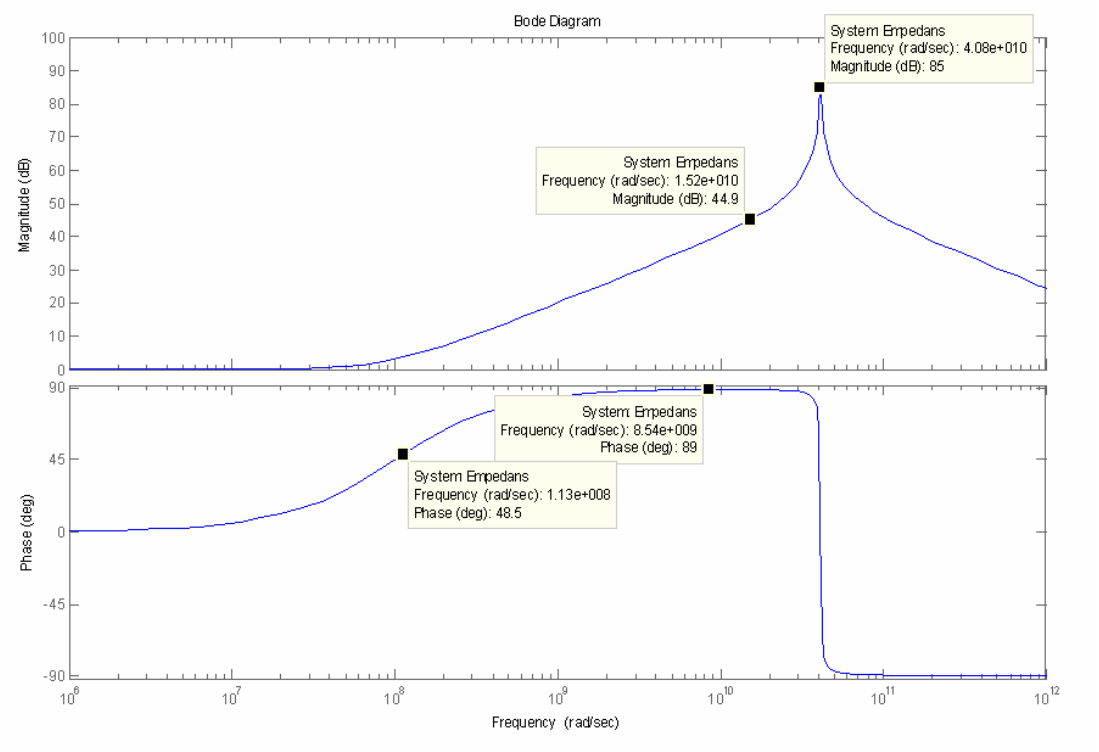

Figure 3.6 : A typical bode diagram of gyrator-C realization

Third region is defined as capacitive region which above than poles of gyrator-C whose magnitude is start to decrease with a slope of 20dB/dec. The capacitive region is above than 6.5GHz in Figure 3.6

In this configuration, equivalent passive model values are L=10nH, Rs=2, Rp=20kOhm, Cp= 60fF.

Gyrtor element is a feedback system and, the stability analysis must be performed. Since two poles are very close to each other, zero of gyrator-C must be selected as dominant such large C2 capacitance. [7] A large capacitance will improve stability of circuit.

The higher quality factor of active inductor can be designed in comparison with on-chip passive inductor. Quality factor of active inductor depends on C_2 and G_2

parasitic elements which can optimized for high quality factor values. Quality factor calculation is given in (3.9).

$$Q = \frac{\omega L}{R_s} = \frac{\omega C_2}{G_2} \tag{3.9}$$

3.4 Noise of Active Inductors

Noise of active inductors is the biggest problem in the circuits if a noiseless system with active inductors is desired. Noise contribution of active inductor is biggest problem in circuit. In Figure 3.7 noisy active inductor and equivalent noise sources are modeled. [6]

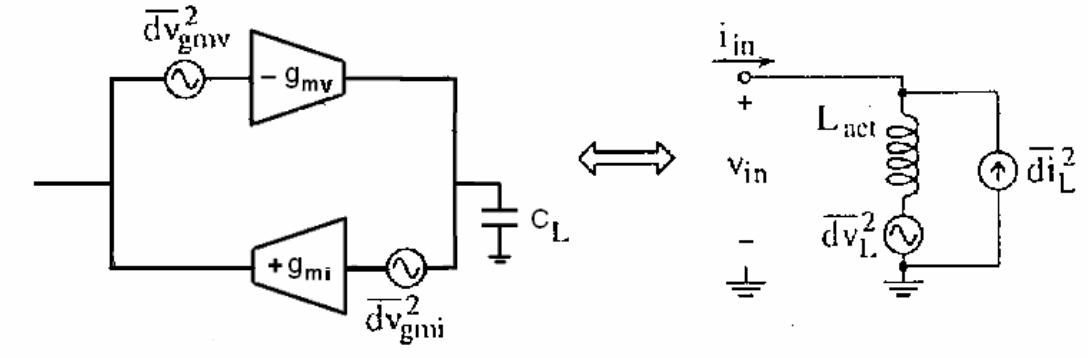

Figure 3.7 : Noisy active inductor and its equivalent noise source

To get expression of $\overline{di}_L^2$ and $\overline{dv}_L^2$,

Right part of Figure 3.10 is;

$$\overline{di}^2_{in_{right}} = \overline{di}^2_L + \frac{1}{(sL_{act})}\overline{dv}^2_L \tag{3.10}$$

Left part of Figure 3.11 is;

$$\overline{di}^2_{in_{Left}} = g^2_{mi}\left[\left(\frac{g_{mv}}{sC_L}\right)^2 \overline{dv}^2_{gmv} + \overline{dv}^2_{gmi}\right] \tag{3.11}$$

Since both equations are equivalent, we can extract expression of $\overline{di}_L^2$ and $\overline{dv}_L^2$ as shown (3.12) and equation (3.13).

$$\overline{di}^2_L = g^2_{mi}.\overline{dv}^2_{gmi} \tag{3.12}$$

$$\overline{dv}^2_L = \overline{dv}^2_{gmi} \tag{3.13}$$

For a transconductance equivalent input noise source, it can be expressed as (3.14) where F is excess noise of amplifier, and (3.15) and (3.16) can modify by substitution with this expression shown as (3.14).

$$\overline{dv}_{gm}^2 = 4kT\frac{F}{g_m}df \tag{3.14}$$

$$\overline{di}_L^2 = 4kTF_i g_{mi} df \tag{3.15}$$

$$\overline{dv}_L^2 = 4kT\frac{F_v}{g_{mv}}df \tag{3.16}$$

The (3.15) and (3.16) explain that the noise of active inductor is depends on transconductance values of amplifiers.

3.5 Noise Contribution of Active Inductor to LC VCO

3.5.1 Inductor Current Noise Source

Noise contribiton of inductor current noise source is calculated like section 2.4.1 and section 2.4.5. Output noise equation is given below.

$$\overline{dV}_{out}^2(\omega_0+\Delta\omega) \approx kT\frac{F_i g_{mi}}{(\omega_0 C)^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 df \tag{3.17}$$

3.5.2 Inductor Voltage Noise Source

Noise contribiton of inductor voltage noise source is calculated like section 2.4.3. Output noise equation is given below.

$$\overline{dV}_{out}^2(\omega_0+\Delta\omega) \approx kT\frac{F_v}{g_{mv}}\left(\frac{\omega_0}{\Delta\omega}\right)^2 df \tag{3.18}$$

3.5.3 Total Noise and Phase Noise of LC VCO based on active inductor

The total noise of LC VCO at the output can be calculated combining (3.17), (3.18) and (2.44) from previous section. The results expression is given in (3.19).

$$\overline{dV}_{out}^2(\omega_0+\Delta\omega) = kTR\text{eff}\left[1+A+\frac{1}{\omega_0 C}\left(\frac{F_i g_{mi}}{(\omega_0 C)}+\frac{F_v}{g_{mv}}(\omega_0 C)\right)\right]\left(\frac{\omega_0}{\Delta\omega}\right)^2 df \tag{3.19}$$

This formula can be rearranged as (3.20) by defining noise contribution factor of active inductor. The total noise of LC VCO based on active inductor output can be summarized as below equations.

Total Noise: $\overline{dV}^2_{out}(\omega_0 + \Delta\omega) = kTR\text{eff}\left[1 + A + MQ\right]\left(\frac{\omega_0}{\Delta\omega}\right)^2 df$ **(3.20)**

Oscillation Frequency: $\omega_0 = \frac{1}{\sqrt{LC}} = \sqrt{\frac{g_{mi}g_{mv}}{CC_L}}$ **(3.21)**

Effective Resistance: $R\text{eff} = R_C + R_L + \frac{1}{R_P(\omega_0 C)^2}$ **(3.22)**

Noise Amplication Factor: $A = \alpha F_{G_M}$ **(3.23)**

Noise Factor of Active Inductor: $M = \sqrt{\frac{g_{mi}}{g_{mv}}}\left(F_i\sqrt{\frac{C_L}{C}} + F_i\sqrt{\frac{C}{C_L}}\right)$ **(3.24)**

Transconductance: $G_M = R\text{eff}(\omega_0 C)^2 + gm_i + gm_v$ **(3.25)**

4. DESIGN OF LC VCO BASED ON ACTIVE INDUCTOR

In this section, LC VCO based on active inductor design methodologies is explained, and comparison between designs is performed.

4.1 Design of Active Inductor

The topology of active inductor shown as Figure 4.1 is based on reference [7]. It is based on gyrator-C realization.

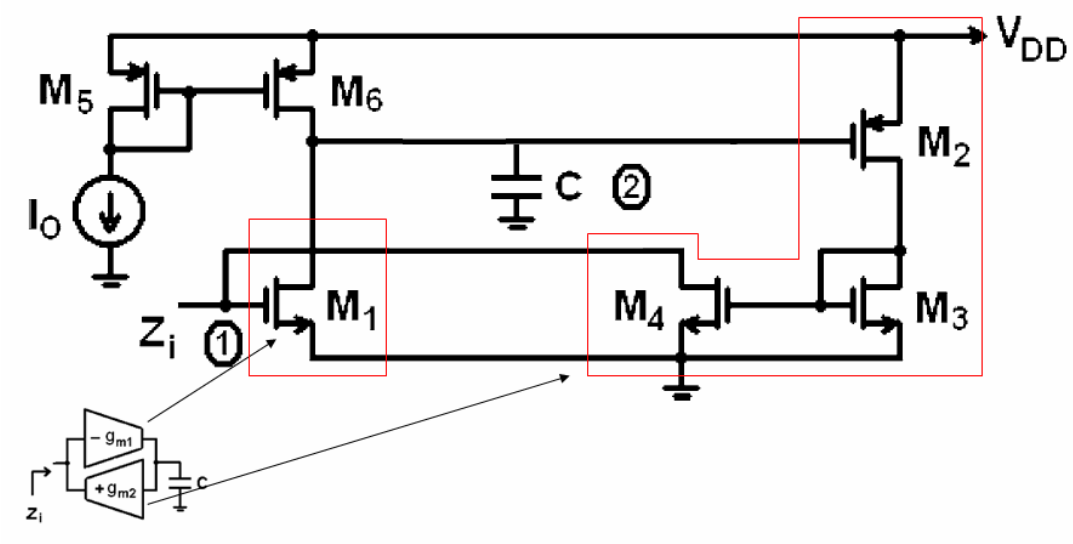

Figure 4.1 : Design of active inductor based on gyrator-C realization

The proposed active inductor topology inductor is compact and, there is no cascode structure, so circuit can operate in low VDD which improves power dissipation of active inductors. Moreover, there is no body effect suffering which alters gm values.

As an inductor, the circuit can provide a high quality factor value. To achieve high Q, an active inductor should provide high capacitance and low conductance at node 2 shown as Figure 3.5 and (3.9). Comparably, the proposed circuit topology provides low conductance at critical node 2 due to common-source configurations. [7]

Another advantage of proposed circuit, inductance value can be tuned using I_0 which can provide a tuning option for LC resonators, and being get rid of negative effects of varactors such as huge capacitance change with a small voltage change.

The negative transconductance is implemented as M1 transistor and, positive transconductance is realized as M2, M3 and M4 transistor. M3 and M4 transistor generate simple current source which invert the negative transconductance of M2. M5 and M6 transistors are used for biasing. The proper usage of circuit, gate of M1 must be biased. A current source should be added to the circuit shown as Figure 4.2 for M3 drain current in order to achieve biasing of M1 transistor.

Also, active inductor can be implemented as PMOS input by complementing all transistors in Figure 4.2. Input of active inductor as can be chosen as NMOS or PMOS for biasing purposes depended on application of circuit.

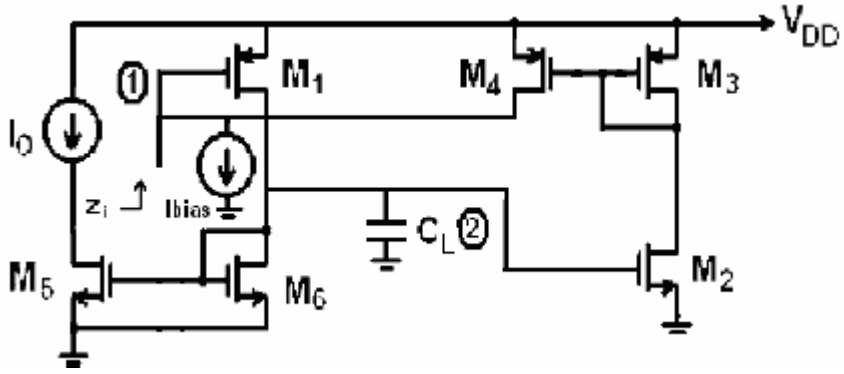

Figure 4.2 : PMOS input active inductors

The main disadvantage of active inductors is caused by input voltage swing. The input voltage swing is narrow since operating all transistors in saturation region.

4.1.1 Biasing of Proposed Circuit

For a proper operation, all transistors must be in saturation region. The conditions as given below should be performed for in order to guarantee all transistors in saturation region for circuit shown as Figure 4.3. Firstly, stages are cut from double line and, analysis of each stage is performed separately. After than, all equations are combined and saturation constraints is found for maximum input voltage swings.

From first transconductance, maximum and minimum input voltages can be found as (4.1) and (4.2) in order to saturate M1 and M6. V_{OD} means overdrive voltage of related transistor and V_{DD} is equal to 1.2. Maximum input voltage can be solved by iteratively with (4.2b) and (4.3).

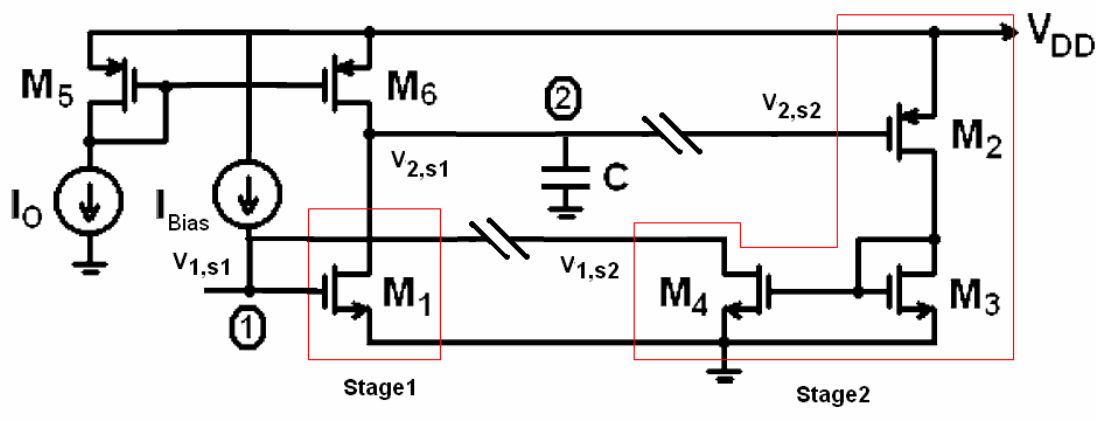

Figure 4.3 : Biasing analysis of proposed active inductor

$$\frac{1}{2}u_n C_{ox}\left(\frac{W_n}{L_n}\right)_1 (V_{1\max,S1}-V_{Tn})^2(1+\lambda_n V_{OD1}) = I_0(1+\lambda_p(1.2-V_{OD1})) \tag{4.1a}$$

$$V_{1\max,S1} = \sqrt{\frac{1+\lambda_p(1.2-V_{OD1})}{1+\lambda_n V_{OD1}}\frac{I_0}{\frac{1}{2}u_n C_{ox}\left(\frac{W_n}{L_n}\right)_1}} + V_{Tn} \tag{4.1b}$$

$$\frac{1}{2}u_n C_{ox}\left(\frac{W_n}{L_n}\right)_1 (V_{1\min,S1}-V_{Tn})^2(1+\lambda_n(1.2-V_{OD6})) = I_0(1+\lambda_p V_{OD6}) \tag{4.2a}$$

$$V_{1\min,S1} = \sqrt{\frac{1+\lambda_p V_{OD6}}{1+\lambda_n(1.2-V_{OD6})}\frac{I_0}{\frac{1}{2}u_n C_{ox}\left(\frac{W_n}{L_n}\right)_1}} + V_{Tn} \tag{4.2b}$$

$$V_{OD1} = V_{1\max,S1} - V_{Tn} \tag{4.3}$$

(4.4) and (4.5) which are obtained from first transconductance stage show maximum and minimum voltages at node 2 according to its input voltage represented in Figure 4.10 with red lines.

$$V_{2\min,S1} = (V_{OD1})_{V_1=V_{1\max,S1}} = (V_{1\max,S1}-V_{Tn})_{V_1=V_{1\max,S1}} \tag{4.4}$$

$$V_{2\max,S1} = (1.2-V_{OD6})_{V_1=V_{1\min,S1}} \tag{4.5}$$

Also, from second transconductance stage, maximum and minimum voltage at node 2 can be found as (4.5) and (4.6), in order to saturate M2 and M3. These equations represented in Figure 4.10 as blue.

$$\frac{1}{2}u_p C_{ox}\left(\frac{W_p}{L_p}\right)_2\left((1.2-V_{2\min,S2})-|V_{Tp}|\right)^2\left(1+\lambda_p V_{OD2}\right)=I_{bias}\left(1+\lambda_n\left(1.2-V_{OD2}\right)\right) \quad \textbf{(4.6a)}$$

$$V_{2\min,S2}=1.2-\sqrt{\frac{1+\lambda_n(1.2-V_{OD2})}{1+\lambda_p V_{OD2}}\frac{I_{bias}}{\frac{1}{2}u_p C_{ox}\left(\frac{W_p}{L_p}\right)_2}}-|V_{Tp}| \quad \textbf{(4.6b)}$$

$$\frac{1}{2}u_p C_{ox}\left(\frac{W_p}{L_p}\right)_2\left((1.2-V_{2\max,S2})-|V_{Tp}|\right)^2\left(1+\lambda_p(1.2-V_{Tp})\right)=I_{bias}\left(1+\lambda_n V_{Tp}\right) \quad \textbf{(4.7a)}$$

$$V_{2\max,S2}=1.2-\sqrt{\frac{1+\lambda_n V_{Tp}}{1+\lambda_p(1.2-V_{Tp})}\frac{I_{bias}}{\frac{1}{2}u_p C_{ox}\left(\frac{W_p}{L_p}\right)_2}}-|V_{Tp}| \quad \textbf{(4.7b)}$$

If stages are combined and, equations from stages are equaled, (4.8) must be checked for all transistors in saturation region.

$$\left(V_{2\min,S1}\right)_{V_1=V_{1\max,S1}}\le V_{2\min,S2}\le V_{2\max,S2}\le\left(V_{2\max,S1}\right)_{V_1=V_{1\min,S1}} \quad \textbf{(4.8)}$$

This means;

4.8 can be found as from 4.5 and 4.7b;

$$V_{2\max,S2}\le V_{2\max,S1}\Rightarrow 1.2-\sqrt{\frac{1+\lambda_n V_{Tp}}{1+\lambda_p(1.2-V_{Tp})}\frac{I_{bias}}{\frac{1}{2}u_p C_{ox}\left(\frac{W_p}{L_p}\right)_2}}-|V_{Tp}|\le 1.2-V_{OD6} \quad \textbf{(4.8)}$$

4.9 can be found as from 4.4 and 4.6b;

$$V_{2\min,S1}\le V_{2\min,S2}\Rightarrow V_{1\max,S1}-V_{Tn}\le V_{2\min,S2} \quad \textbf{(4.9)}$$

$$\sqrt{\frac{1+\lambda_p(1.2-V_{OD1})}{1+\lambda_n V_{OD1}}\frac{I_0}{\frac{1}{2}u_n C_{ox}\left(\frac{W_n}{L_n}\right)_1}}\le 1.2-\sqrt{\frac{1+\lambda_n(1.2-V_{OD2})}{1+\lambda_p V_{OD2}}\frac{I_{bias}}{\frac{1}{2}u_p C_{ox}\left(\frac{W_p}{L_p}\right)_2}}-|V_{Tp}| \quad \textbf{(4.10)}$$

Also, minimum input of active inductor voltage must be higher than overdrive voltage of M4.

$$V_{1\min,S2} \geq V_{OD4} \Rightarrow \sqrt{\frac{1+\lambda_p V_{OD6}}{1+\lambda_n (1.2-V_{OD6})} \frac{I_0}{\frac{1}{2} u_n C_{ox} \left(\frac{W_n}{L_n}\right)_1}} \geq V_{OD4} \qquad \textbf{(4.11)}$$

As a result, DC nodes voltages on nodes depend on I_{bias} and I_0. For node 1, when I0 increases, DC voltages for saturation limits will increase. For node 2, when I_{bias} increases, DC voltages for saturation limits will decrease.

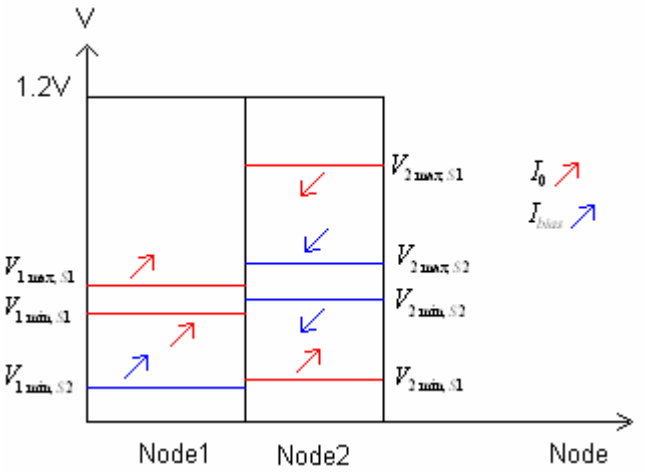

Figure 4.4 : Graphic representation and I_0 - I_{bias} dependency of (4.8) and (4.10) for saturation limits (Red is for stage 1 and blue is for stage 2)

Many of design can achieve the conditions given as (4.8) and (4.11) and graphic representation in Figure 4.4. For get a more linear characteristic, biasing point should be selected when DC voltage of node is equal to distance to saturation limits. For node 1 and node 2, biasing points should be select as (4.12) and (4.13) which are related by transistors' sizes and biasing currents.

$$V_1 = \frac{V_{1\max,S1} + V_{1\min,S1}}{2} \qquad \textbf{(4.12)}$$

$$V_2 = \frac{V_{2\max,S2} + V_{2\min,S2}}{2} \qquad \textbf{(4.13)}$$

Another important point is derivation of stages output due to the linearity. Active inductor can operate a limit region because of saturation limit. In this limited region, derivation of transconductance output should be constant.

The Figure 4.5 is a DC sweep analysis to find proper DC biasing points of active inductor. First OTA must be bias at "A" point due to same distance to saturation limits, to keep derivation of transconductance output within a maximum voltage

input as a constant. Second OTA's input is output of first OTA, so $V_{2\max,S2}$ and $V_{2\min,S2}$ should be in saturation region (vinicity of "A" point) of first OTA output which provides to keep in saturation region of second OTA's transistors when circut operates as an inductor. Proper bias current must be selected as derivation of second OTA is a constant too.

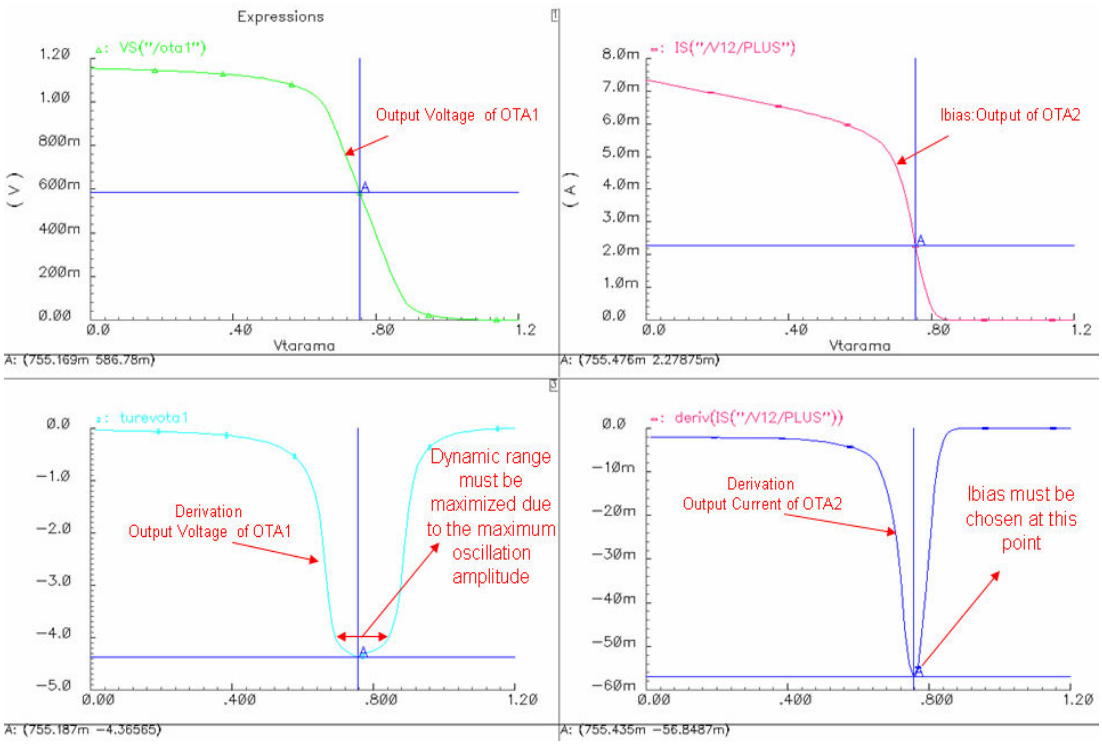

Figure 4.5 : Selecting biasing of active inductor circuit

4.1.2 Input Voltage Swing of Proposed Circuit

Input voltage swing of circuit (Node 1) can be expressed as below.

$$V_{Swing,1} = V_{1\max,S1} - V_{1\min,S1} \tag{4.14}$$

From (4.1) and (4.2);

$$V_{Swing,1} = \sqrt{\frac{1+\lambda_p(1.2-V_{OD1})}{1+\lambda_n V_{OD1}} \frac{I_0}{\frac{1}{2}u_n C_{ox}\left(\frac{W_n}{L_n}\right)_1}} - \sqrt{\frac{1+\lambda_p V_{OD6}}{1+\lambda_n(1.2-V_{OD6})} \frac{I_0}{\frac{1}{2}u_n C_{ox}\left(\frac{W_n}{L_n}\right)_1}} \tag{4.15}$$

$$V_{Swing,1} = \left(\sqrt{\frac{1+\lambda_p(1.2-V_{OD1})}{1+\lambda_n V_{OD1}}} - \sqrt{\frac{1+\lambda_p V_{OD6}}{1+\lambda_n(1.2-V_{OD6})}}\right) \sqrt{\frac{I_0}{\frac{1}{2}u_n C_{ox}\left(\frac{W_n}{L_n}\right)_1}} \tag{4.16}$$

As it clear, increasing I0 which means higher power consumption will increase input voltage swing at the input. Moreover, input voltage swing depends on λ parameters of PMOS and NMOS transistor.

For instance λ parameters is equal to 0.1 and, $V_{OD1,6}$=0.1, (4.17) is found.

$$V_{Swing,1} = \left(\sqrt{\frac{1+0{,}1(1{,}1)}{1+0{,}1.0{,}1}} - \sqrt{\frac{1+0{,}10{,}1}{1+0{,}1.1{,}1}} \right) \sqrt{\frac{I_0}{\frac{1}{2}u_n C_{ox}\left(\frac{W_n}{L_n}\right)_1}} = 0.094 \sqrt{\frac{I_0}{\frac{1}{2}u_n C_{ox}\left(\frac{W_n}{L_n}\right)_1}} \quad \textbf{(4.17)}$$

As a result, $V_{swing,1}$ is affected by λ parameters hugely. If λ parameters are zero, the voltage swing of circuit will be zero too. To increase $V_{swing,1}$, I_0 current should be increased, size of input transistor M1 should be small. However, lowering size of input transistor will decrease transconductance which causes to not achieve a low inductor value.

Another important point is swing at Node2;

$$V_{Swing,2} = V_{1\max,S1} - V_{1\min,S1} \quad \textbf{(4.18)}$$

$$V_{Swing,2} = \sqrt{\frac{1+\lambda_n(1.2-V_{OD2})}{1+\lambda_p V_{OD2}} \frac{I_{bias}}{\frac{1}{2}u_p C_{ox}\left(\frac{W_p}{L_p}\right)_2}} - \sqrt{\frac{1+\lambda_n V_{Tp}}{1+\lambda_p(1.2-V_{Tp})} \frac{I_{bias}}{\frac{1}{2}u_p C_{ox}\left(\frac{W_p}{L_p}\right)_2}} \quad \textbf{(4.19)}$$

$$V_{Swing,2} = \left(\sqrt{\frac{1+\lambda_n(1.2-V_{OD2})}{1+\lambda_p V_{OD2}}} - \sqrt{\frac{1+\lambda_n V_{Tp}}{1+\lambda_p(1.2-V_{Tp})}} \right) \sqrt{\frac{I_{bias}}{\frac{1}{2}u_p C_{ox}\left(\frac{W_p}{L_p}\right)_2}} \quad \textbf{(4.20)}$$

Like (4.16), voltage swing at node 2 is affected by λ parameters. In order to keep all transistors in saturation region, output voltage of first stage must be limited with $V_{1\max,S1}$ and $V_{1\min,S1}$ which is several mV at the input of active inductor.

4.2 Choosing LC-VCO topology

As VCO topology, crossed-coupled LC VCO is considered the more suitable structure than Colpitts and ring oscillator due to phase noise, and size of circuit which are explained in section 2.1.1 and 2.1.2 in detail.

From negative resistance concept crossed-coupled oscillator can be implemented in different ways. In Figure 4.6, several cross-coupled LC VCO has been introduced.

Top-biased NMOS and PMOS LC-VCO topology, which is also called as symmetrical LC oscillator, can achieve a better noise at a given power dissipation [14], however, it has cascoded cross-coupled couples. Process of designs will be UMC0.13 at 1.2V due to the low power consideration.

Top-biased NMOS LC VCO topology and top-biased NMOS and PMOS LC-VCO topology need floating inductors so, high frequency implementation with proposed active inductor is inconvenient. Proposed active inductor is not a floating inductor. If a floating inductor is necessary, it can be realized by using two gyrators.

Bottom-biased NMOS is chosen for designs since the circuit doesn't have cascode stages and floating inductors. Moreover, bottom-biases PMOS can be used for designs.

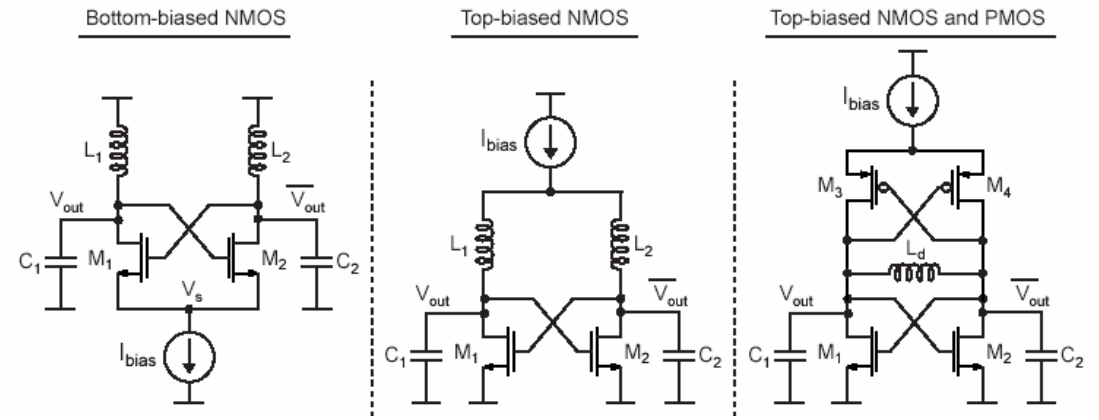

Figure 4.6 : Several crossed-coupled LC VCO topologies

In this work, the proposed active inductance circuit (input as NMOS and PMOS) and bottom-biased (NMOS-PMOS) crossed-coupled LC VCO topologies are combined. First design is realized with NMOS Cross-Coupled with PMOS input active inductor structure because considering noise contribution of input as PMOS inductor and, NMOS cross-coupled provides more higher amplitude. Other designs are based on same architecture which has same power dissipations and same currents on transistors.

4.2.1 VCO Design Considerations

The center frequency of oscillator will be 2.45GHz which is required for Bluetooth, 802.11b and 802.11g wireless communication standard. The tuning range must cover 2.4GHz to 2.5GHz shown as (4.21) and (4.22).

$$\omega_{\min} \geq \frac{1}{\sqrt{L_{\max}C}} = \sqrt{\frac{g_{m1\min}g_{m2}}{CC_L}} \tag{4.21}$$

$$\omega_{\max} \geq \frac{1}{\sqrt{L_{\min}C}} = \sqrt{\frac{g_{m1\max}g_{m2}}{CC_L}} \tag{4.22}$$

The second condition is related with start-up of oscillator. Practically, gm values of crossed-coupled transistors should be designed 3 times larger 1/Rp. (4.23) also shows the gain of stages should be higher than 3.

$$g_{m_{Mc1,MC2}} \geq \frac{3}{Rp} \tag{4.23}$$

The third condition is related with oscillation amplitude which is important for phase noise performance. At the oscillation frequency, L and C admittance cancel, and only Rp is leaving. The harmonics of the current are filtered by LC tank on I_{s1} where shown drain current crossed-coupled and, the induced current shown as in Figure 4.8 and (4.24) are given below;

$$I_{s1,fundamental} = \frac{2}{\pi} I_{tail}.\sin(\omega_0 t) \tag{4.24}$$

$$\omega_0 = \frac{2\pi}{T} \tag{4.25}$$

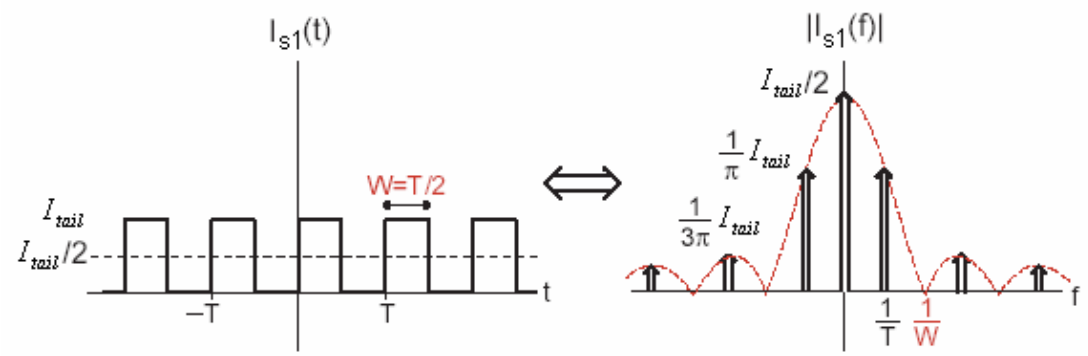

Figure 4.7 : Current source changes of I_{s1} on time and frequency domain

As a result, the amplitude of oscillation is calculated as (4.26) for differential output.

$$V_{\text{tank}} = \frac{4}{\pi} I_{tail}.Rp \tag{4.26}$$

This equation is valid when the mode of operation is referred as “current limited” and, tail current determines the amplitude of oscillation shown as Figure 4.8.

If tail current increases, the oscillation amplitude is affected by power supply which is called as “voltage limited” region. Transistor enters triode regions in voltage limited region, and tail current source spend much time in triode region [15]

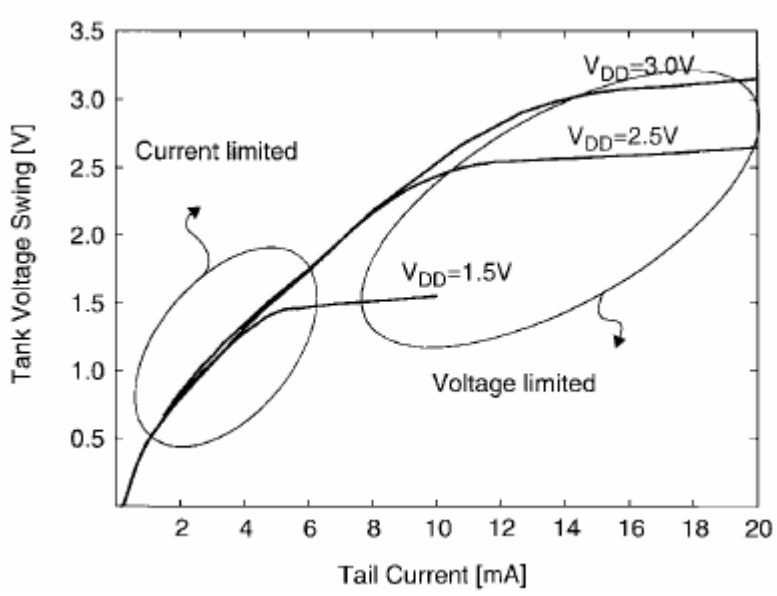

Figure 4.8 : Oscillation amplitude: voltage limited region and current limited region

Also, oscillation amplitude will be limited due to using active inductor. A proper DC voltage must be selected to achieve maximum oscillation amplitude since achieve a higher phase noise performance. For configuration shown as Figure 4.9;

To keep M1 transistor in saturation where ΔV is representing single;

$$V_{OUT_{DC}} + \Delta V \le V_{DD} - \left|V_{Tp}\right| \tag{4.27}$$

To keep crossed-coupled transistor in saturation;

$$V_{OUT_{DC}} + \Delta V - V_s \ge V_{Tn} \ , \ V_{OUT_{DC}} - \Delta V - V_s \ge V_{Tn} \tag{4.28}$$

$$V_{OUT_{DC}} - \Delta V - V_s \ge V_{DSsat} \ , \ V_{OUT_{DC}} + \Delta V - V_s \ge V_{DSsat} \tag{4.29}$$

To keep tail current source in saturation;

$$V_s \ge V_{DSsat} \tag{4.30}$$

For instance, considering V_{DD}=1.2, Vs = 0.2V (to prevent tail current source from entering triode region), Vdsat = 0.1V, Vtn=|Vtp|=0.35V, the maximum oscillation amplitude should be 0.3V for current limited region. The DC voltage at the output should be select as 0.7V.

$$V_{Tn} + V_S + \Delta V \le V_{OUT_{DC}} \le V_{DD} - \left|V_{Tp}\right| - \Delta V \tag{4.31}$$

$$0.55 + \Delta V \le V_{OUT_{DC}} \le 0.85 - \Delta V \tag{4.32}$$

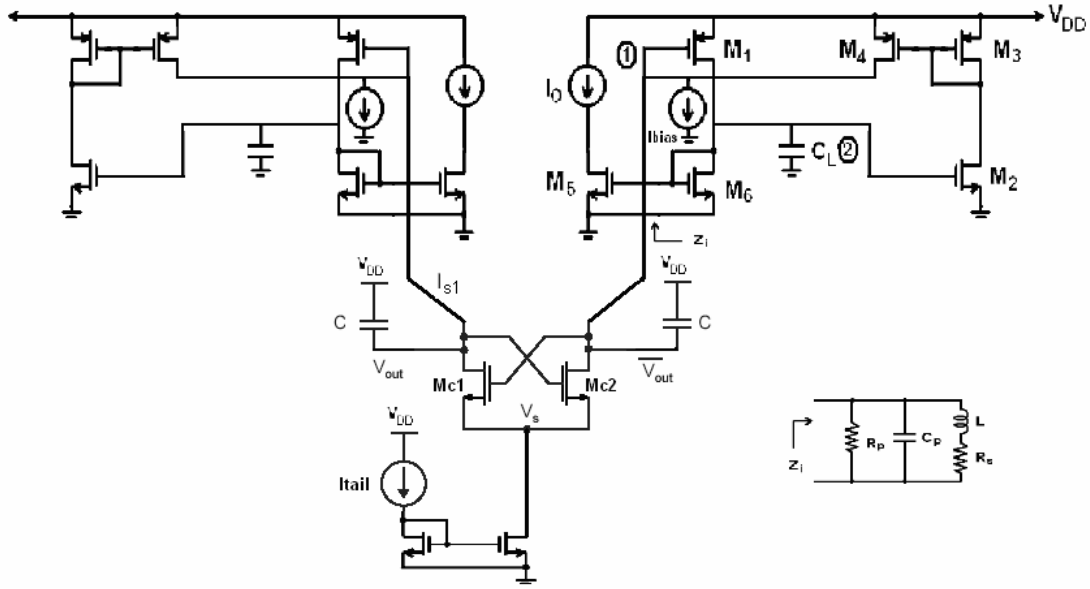

Figure 4.9 : NMOS crossed-coupled and PMOS input active inductor topology

4.3 Optimization of Phase Noise

LC VCO based on active inductor circuit's noise equations are given below which are derivated in section 3.4 and section 3.5 in detail.

Total Noise: $\overline{dV}^2_{out}(\omega_0 + \Delta\omega) = kTR\text{eff}\left[1 + A + MQ\right]\left(\frac{\omega_0}{\Delta\omega}\right)^2 df$ **(4.33)**

Oscillation Frequency: $\omega_0 = \frac{1}{\sqrt{LC}} = \sqrt{\frac{g_{mi}g_{mv}}{CC_L}}$ **(4.34)**

Effective Resistance: $R\text{eff} = R_C + R_L + \frac{1}{R_P(\omega_0 C)^2}$ **(4.35)**

Noise Amplification Factor: $A = \alpha F_{G_M}$ **(4.36)**

Noise Factor of Active Inductor: $M = \sqrt{\frac{g_{mi}}{g_{mv}}}\left(F_i \sqrt{\frac{C_L}{C}} + F_i \sqrt{\frac{C}{C_L}} \right)$ **(4.37)**

Transconductance: $G_M = R\text{eff}(\omega_0 C)^2 + gm_i + gm_v$ **(4.38)**

4.3.1 Noise Optimization of LC Tank Based on Active Inductors

To minimize noise, M noise factor of active inductor need to be minimized. At first sight, ratio $\sqrt{g_{mi} / g_{mv}}$ value seems to be minimized, however making g_{mv} larger than g_{mi} cause to larger swing as C_L than tank capacitance C and it will be limit the oscillation amplitude because of voltage swing at LC tank. Al least, transconductance value must be equal.

Minimizing M can be achieved by equalizing inductor capacitor C_L and LC tank capacitor C while supposing F_i and F_v are equal.

If transconductance value and capacitor values are designed equal, M can be achieved to be 2.

If oscillation amplitude of VCO is equal to V_A, phase noise of LC VCO based on active inductor can be expressed as below.

$$L(\Delta\omega) = 10\log\left[\frac{\int_{\Delta\omega-0.5}^{\Delta\omega+0.5} kTR\text{eff}\left[1 + A + MQ\right]\left(\frac{\omega_0}{\Delta\omega}\right)^2 \, df}{(V_A)^2 / 2} \right] \quad \textbf{(4.39)}$$

$$L(\Delta\omega) = 10\log\left[\frac{kTR\text{eff}\left[1 + A + MQ\right]\left(\frac{\omega_0}{\Delta\omega}\right)^2}{(V_A)^2 / 2} \right] \quad \textbf{(4.40)}$$

To get low phase noise it seems to be generating a low Q LC tank. However, it is not achieved by increasing Reff. It should be achieved by increasing tank capacitor C because noise contribution of active inductor is multiplication of Reff and M.Q value.

$$Q = \frac{1}{R\text{eff}(\omega_0 C)} \quad \textbf{(4.41)}$$

Another thing is increasing tank capacitor, an inductor with a low value is needed so, power consumption is increasing to implement high transconductance values for active inductor.

For instance if previous calculated system in section 2.4.6 is achieved by an active inductor, phase noise found previously -115dBc/Hz will be increase due to the noise contribution of active inductor. Its equation is given in (4.42)

$$L(\Delta\omega) = 10\log\left[\frac{0.41.10^{-21}.16{,}7\left[1+3+MQ\right]\left(\frac{2.4GHz}{1MHz}\right)^2}{(Va)^2/2}\right] \qquad \textbf{(4.42)}$$

The phase noise is related with oscillation amplitude directly. If phase noise calculation is evaluated by different MxQ values, Figure 4.10 is derivated. This Figure shows the importance of oscillation amplitude and relation between MxQ values and phase noises at 1MHz offset.

$$\frac{\text{Noise Contribution of Active Inductor}}{\text{Total Noise}} = \frac{\text{MQ}}{1+\text{A}+\text{MQ}} = \frac{12}{16} = \%75 \qquad \textbf{(4.43)}$$

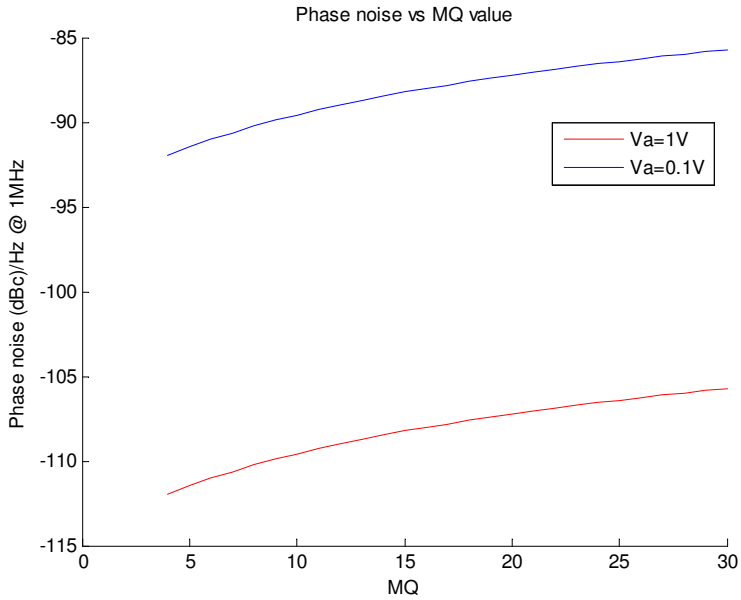

Figure 4.10 : Phase noise of LC VCO based on active inductor versus MxQ value and oscillation amplitude

Generally, M can be achieved close to 2 and if quality factor is selected as 6, the noise contribution of active inductor to total noise will be percent of 75. When oscillator amplitude is 1V, phase noise is calculated as108.9dBc/Hz at 1 MHz offset. When oscillator amplitude is 0.1V, phase noise is calculated as 88.9dBc/Hz at 1 MHz offset.

4.3.2 Noise Optimization of Crossed-Coupled Transistors of LC VCO

The noise of a MOS transistor is given as 4.44 where C_{OX} is the oxide capacitance per unit area, W and L are the width and length of MOS transistors, VGS is DC gate-source voltage and VT is threshold voltage. γ is 2-3 for short channel transistors.

$$di_n^2 = 4kT\gamma\mu Cox\frac{W}{L}(V_{GS} - V_T)df \quad \textbf{(4.44)}$$

$$di_{cc}^2 = \frac{1}{2}\left(di_{n,Mc1}^2 + di_{n,Mc2}^2\right) \quad \textbf{(4.45)}$$

The total differential noise of crossed-coupled transistors is given as (4.45) for Figure 4.9. [4] To optimizing noise performance, PMOS transistors must be selected for design because of μCox parameter.

4.3.3 Noise Optimization of Current Source of LC VCO

For a MOS transistor, extra energy rises between the gate oxide and the silicon substrate at low frequency levels because off dangling bonds. This interface traps some of charged carries and leave go of again with energy during the charged carrier movements. This noise source is called as flicker noise which is related with frequency as given (4.46).

$$di_{tail}^2 = \frac{K}{f}\frac{g_m{}^2}{WLC_{OX}{}^2}\Delta f \quad \textbf{(4.46)}$$

For tail current source, even harmonic such as $0, 2\omega_0, 4\omega_0$ of resonant frequency effects the total noise contribution of tail current, [16] so flicker noise is effective on noise. To optimize tail current noise, size of transistor should be large.

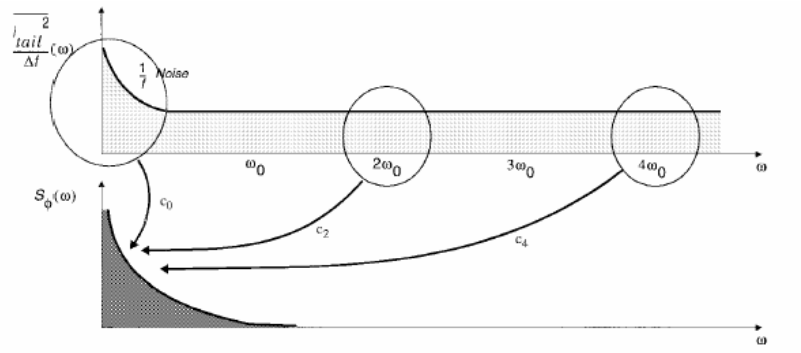

Figure 4.11 : Noise of tail current transistor

4.4 LC VCO Designs

4.4.1 Design of LC VCO with a passive inductor

Firstly, LC VCOs are designed ideally to obtain phase noise performance limits, noise contribution of elements and required inductor value for a given tank capacitor via UMC013 process.

If total capacitor of LC tank is selected as 600fF, required inductor value can be found as 7nH to achieve 2.45GHz resonant frequency. Minimum and maximum inductor value is obtained (4.48) and (4.49) for required tuning range 2.4GHz and 2.5GHz.

$$\omega = \frac{1}{\sqrt{LC}} \Rightarrow L = \frac{1}{\omega^2 C} \tag{4.47}$$

$$L_{\max} \le \frac{1}{\omega_{\min}{}^2 C} = \frac{1}{(2.\pi.2.4GHz)^2 x600\,fF} = 7.33nH \tag{4.48}$$

$$L_{\max} \ge \frac{1}{\omega_{\min}{}^2 C} = \frac{1}{(2.\pi.2.5GHz)^2 x600\,fF} = 6.76nH \tag{4.49}$$

Parasitic capacitor should be token into account to realize 600fF capacitor value since the capacitor of LC tank contains parasitic capacitors of crossed-coupled transistor. For PMOS crossed-coupled topology, this parasitic capacitor can be calculated as (4.47).

$$C_{parasitic} = 2C_{GD} + \frac{1}{2}C_{GS} + \frac{1}{2}C_{DB} \tag{4.50}$$

Another important thing is startup condition of oscillator given as (4.51) where Rp represent parasitic parallel resistance of LC tank, G_M represents conductance of tank, and $g_{O,P}$ represents output conductance of crossed-coupled transistors. This equation is related with quality factor of inductor, effective resistance and λ parameters of transistors, and it gives the transconductance value, gm, of crossed-coupled transistor.

$$g_{m_{Mc1,MC2}} \geq \frac{3}{Rp} = 3(G_M + g_{O,P}) = 3\left(\left(R_C + R_L + \frac{1}{R_P(\omega_0 C)^2}\right)(\omega_0 C)^2 + \lambda I_{tail}\right) \qquad \textbf{(4.51)}$$

Another condition is oscillation amplitude limitations, and it is related with tail current source. To keep oscillation in current limited region;

$$V_{\text{tank,max}} \leq \frac{4}{\pi} I_{tail}.Rp \qquad \textbf{(4.52)}$$

Six schematic simulations are realized considering these five conditions. Firstly, three simulations are realized by ideal LC tank with varies of tail current source depicted as Figure 4.12. The other there LC VCO designs are performed by using a spiral inductor which has already design on UMC013.

Initially, LC VCO is designed with ideal LC tank and ideal current source using PMOS crossed-coupled since noise performance. The parasitic capacitor value is calculated 150fF, so tank capacitor value is selected as 450fF. Selected sizes and current values are listed below.

Table 4.1 : Size of LC VCO design with passive inductors

Wcrossp	9.6um x 32
Wtailp	9.0um x 16
Lcrossp	120nm
L_tailp	360nm
Itailp	750uA

As a result, phase noise is calculated as -132.79dBc/Hz which is caused by only crossed-coupled transistors. If the same topology is realized by current mirror, the phase noise degrades to -117.5dBc/Hz.

The same topology can be designed using a resistor biasing instead of a current mirror. Using resistor provides a higher noise performance. While the current mirror transistors have a flicker noise which affects the total noise o VCO dominantly at

low offset frequency, noise of resistor is accepted as constant and, can be lower than MOS transistor flicker noise at low offset frequency.

If a resistor biasing is used which provides same tail current, phase noise performance increase to -127dB dBc/Hz. The phase noise performance of LC VCO with ideal tank is shown as Figure 4.13.

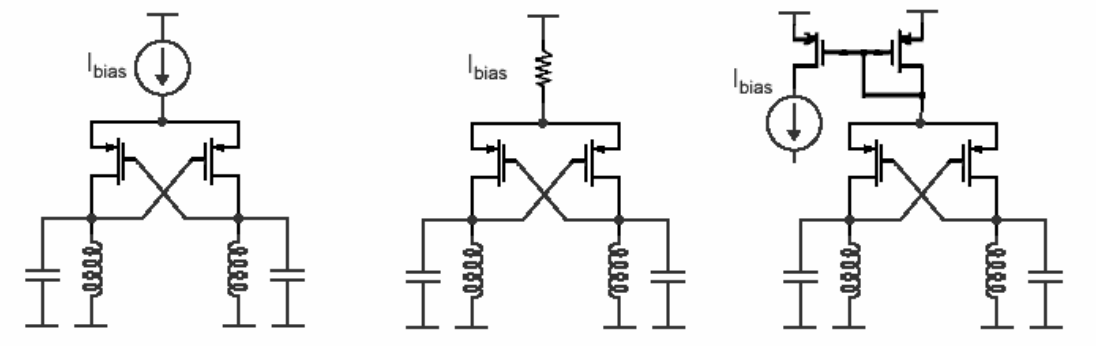

Figure 4.12 : LC VCO with ideal tail current source, LC VCO with a resistor biasing, LC VCO with current mirror

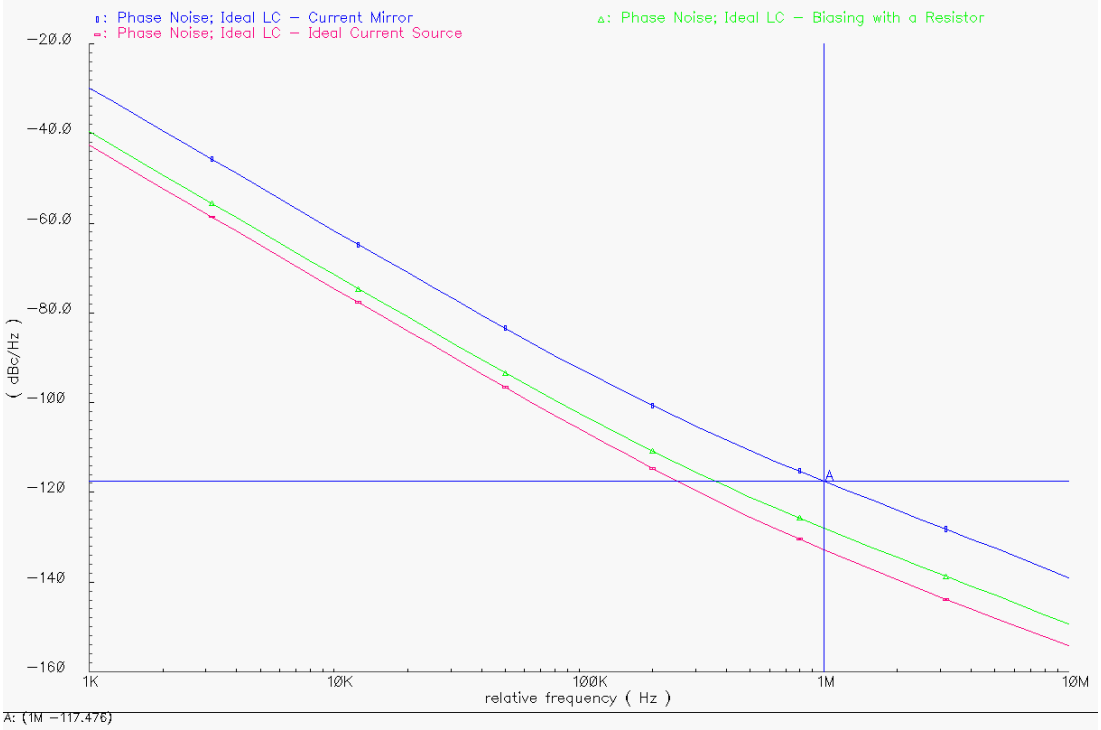

Figure 4.13 : Phase noise performance of LC VCO with ideal LC tank

Moreover, same simulations are performed by using a spiral inductor, so noise contribution of inductor can be shown. Spiral inductor can be designed between 0.3nH to 11nH at UMC013 process.

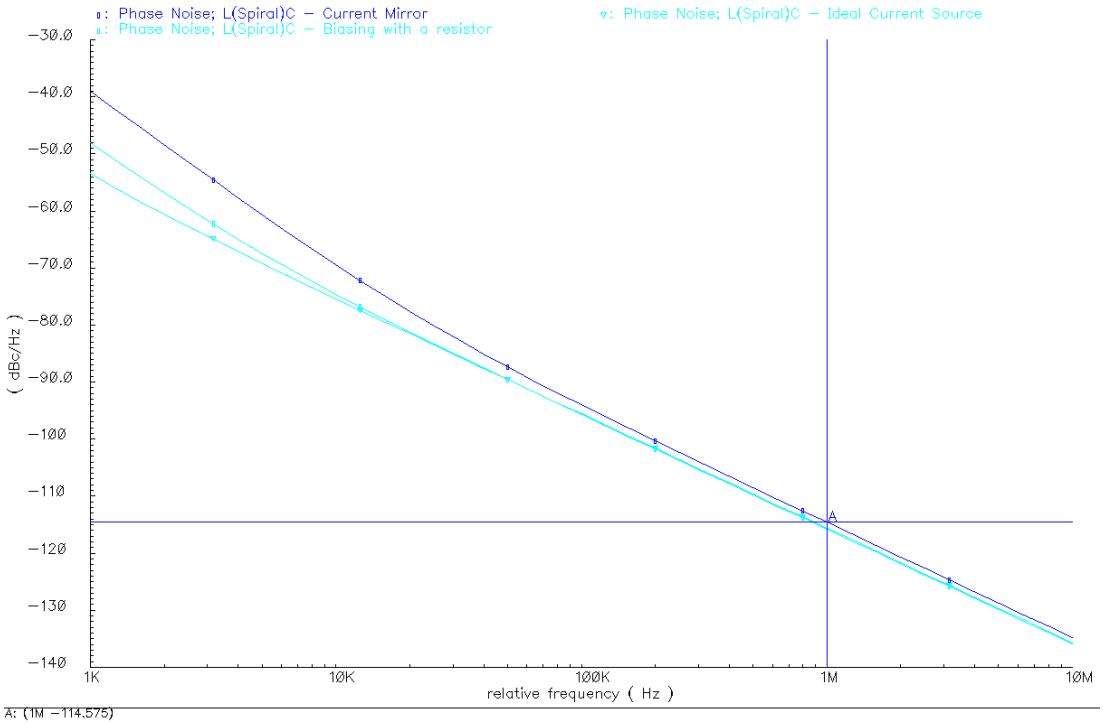

Figure 4.14 : Phase noise performance of LC VCO with spiral L

The phase noise performance decreases because of parasitic of spiral inductor in comparison with ideal inductor. The total comparison results are given below;

LC VCO with LC ideal – ideal current source:-132.79dBc/Hz

LC VCO with LC ideal – biasing with a resistor:-127dB dBc/Hz

LC VCO with LC ideal – current mirror:-117.5 dBc/Hz

LC VCO with LC spiral – ideal current source: -115.9dBc/Hz

LC VCO with LC spiral - biasing with a resistor: -115.8dBc/Hz

LC VCO with LC spiral – current mirror: -114.6dBc/Hz

Effect of using resistor for biasing at low offset frequencies can be shown in Figure 4.14, which get rid off the effect of tail transistor's flicker noise.

4.4.2 Design of LC Tank with PMOS Input Active Inductor

As mentioned in section 4.1.3, noise contribution of active inductor is dominant in comparison with other elements of LC VCO. As a result, Ctank must be large and C_L should be selected as equal to Ctank. Also, transconductance of stages must be equal each other in gyrator.

For a large capacitor, gm values are increased, so Ibias and Itune and size of transistor are selected high, which means power consumption. Realization of active inductor is given below

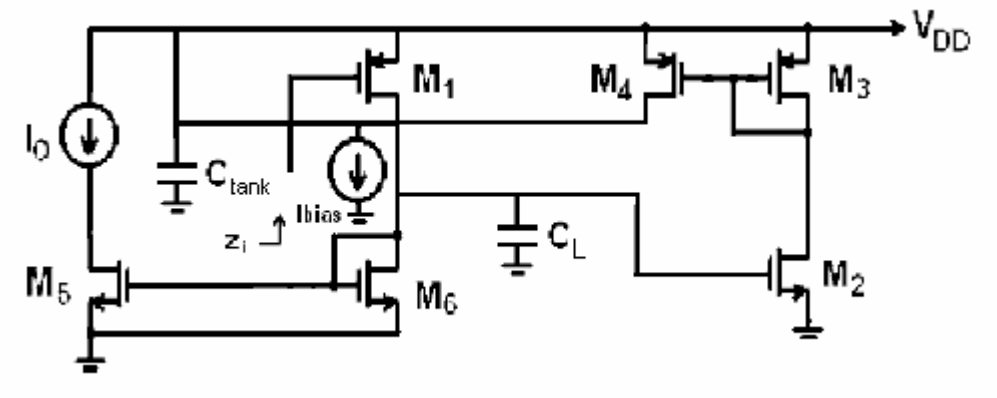

Figure 4.15 : PMOS input active inductor

Table 4.2 : Size and biasing of PMOS input active inductor

W_{M1}	7.2um x 10
$W_{M5,M6}$	8.0um x 2
W_{M2}	7.2um x 3
$W_{M3,M4}$	9.6um x 32
L	120nm
Ctank	300fF
C_L	450fF
Ibias	3.5mA
Itune	2.0mA-5.2mA
Estimated area within %20 error	$106.56um^2$
Power consumption	13.2mW-20.88mW

The important point of active inductor design is to providing maximum input swing since phase noise performance increases via oscillation amplitude. Oscillation node will be node “Zenductor” depicted as Figure 4.16. In Figure 4.16, first stage consists of M41 and second stage consists of M40, M42 and M43. As mention in 4.1.2 input voltage swing of active inductor is narrow and depends on saturation conditions of each transistor. For PMOS input active inductor, M42 and M41 determines maximum input voltage.

For M42, maximum input voltage is

1.2V-|-0171V|=1.029V

to provide V_{DSsat} and,

for M41, maximum input voltage is

1.2V-(|-567V|-|0.35V|) =0.983V

to provide V_{GS} in a proper value. The size of M42 is maximized due to get a higher maximum input voltage swing. Also, all other transistors are in saturation and have a suitable margin to keep all transistors in saturation region.

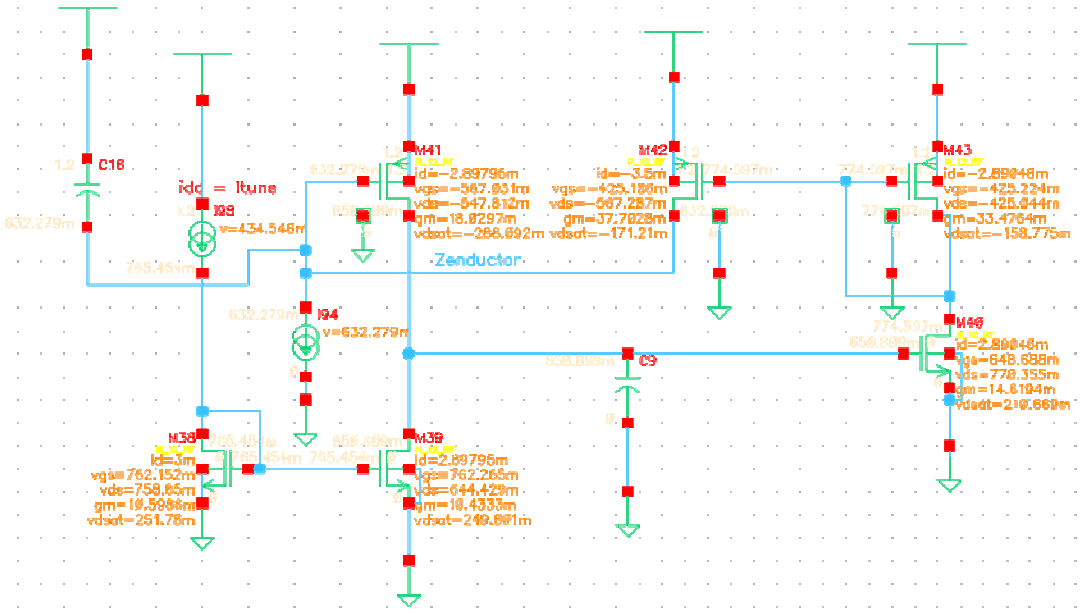

Figure 4.16 : DC values of PMOS input active inductor

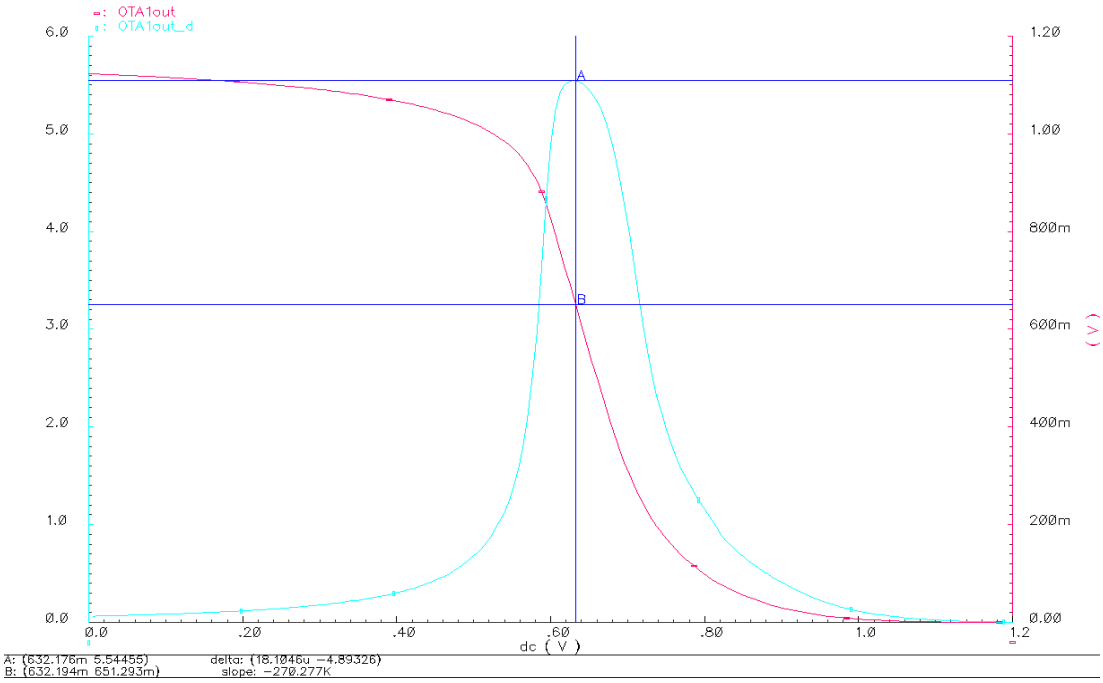

Figure 4.17 : Active inductor stage1's DC sweep analyses and negative derivation of output voltage

Figure 4.17 shows the stage1's output and derivation of output with DC sweep analysis of active inductor. This analysis helps to choose a proper Itune current. The Itune is selected when derivation of output peaks. For this configuration, Itune should be 3mA.

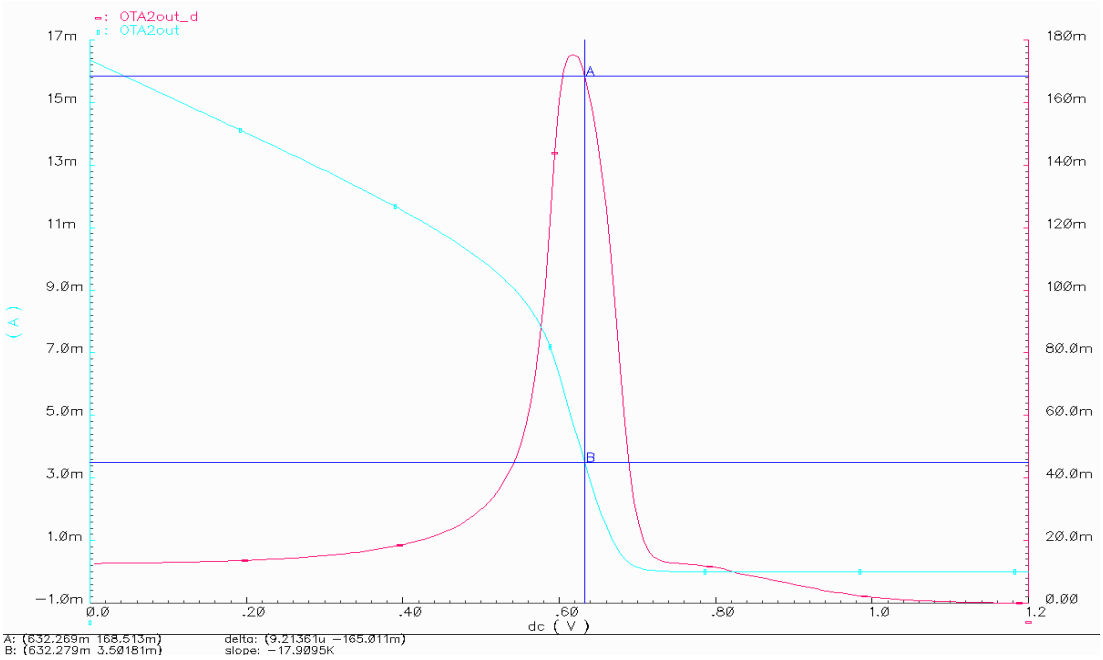

Figure 4.18 : Active inductor stage2's DC sweep analyses and negative derivation of output current

Moreover, second stages determine Ibias of active inductor. The size and currents of second stages should be selected as when input voltage of second stage is equal to output of first stage at Itune=3mA. Figure 4.18 shows that second stage output and its derivation when DC sweep analysis is performed for first stage. Maximum saturation margin should be guaranteed for transistors of second stage. Ibias is found as 3.5mA from Figure 4.18.

Figure 4.29 shows Bode diagram of active inductor as mention previously. The resonant frequency of LC tank is 3.29GHz. The resonant frequency of LC VCO will degrade due to parasitic of LC tank.

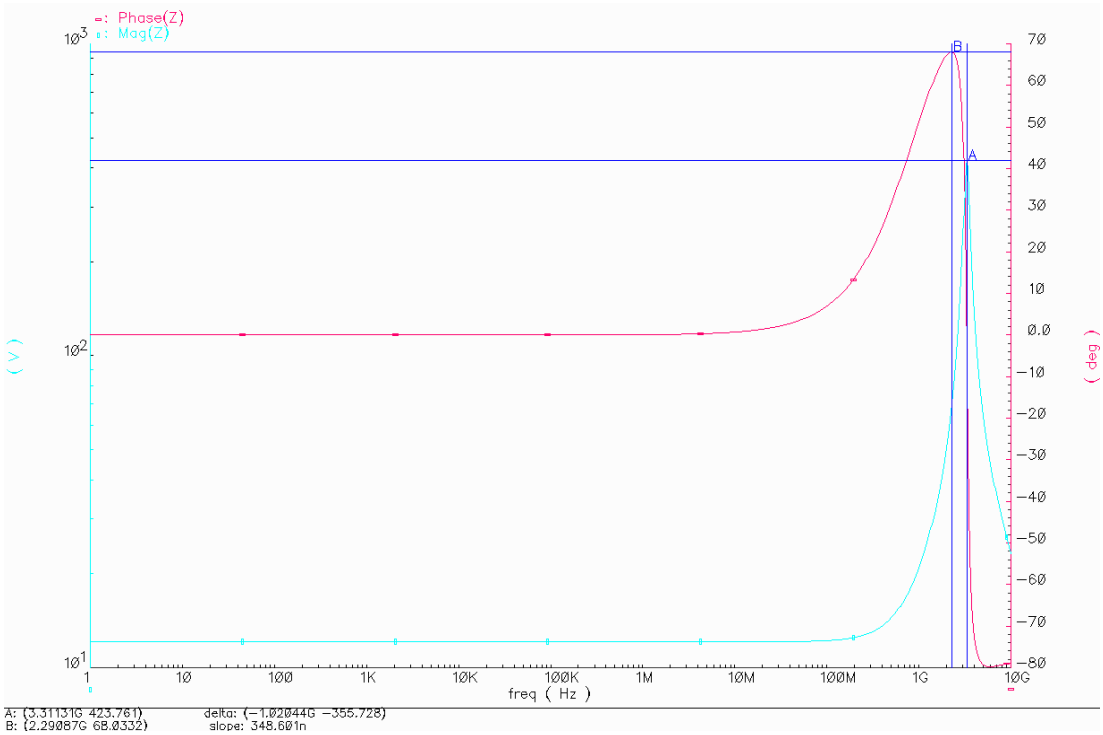

Figure 4.19 : Bode plot of realized active inductor

For stability analysis, poles and zeros analysis is performed because active inductor is a feedback system. The location of poles and zeros are depicted as Figure 4.20. Using poles and zeros, equivalent model of LC tank can be obtained.

L=2.96nH

C=Cp+Ctank=775fF

Rs=11.95Ohm

Rp=900Ohm

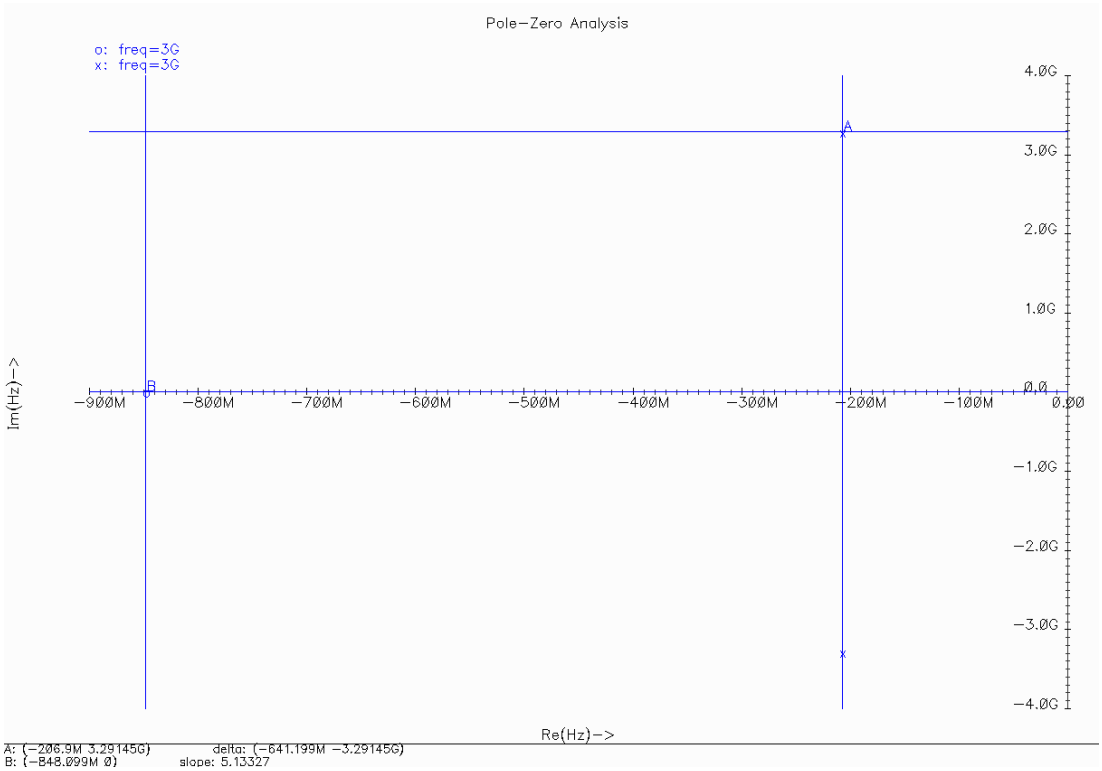

Figure 4.19 : Poles and zero of realized active inductor

4.4.3 Design of LC Tank with NMOS Input Active Inductor

Also, active inductor can be designed as NMOS input. In section 4.4.2, the PMOS active inductor is designed. To realize NMOS active inductor, the complement of PMOS input active inductor is used.

Complementing of a PMOS transistor means selecting size of NMOS transistor which provides same gate-source voltages at same drain-source current of PMOS transistor vice versa.

The size of transistor is small in comparison with PMOS input transistor, so the parasitic capacitances of transistor is small. The resonant frequency of LC tank with NMOS input active inductor will higher than PMOS input active inductor version. To provide same resonant frequency, there is two ways. One of them is increasing CL or Ctank. Increasing CL will be increase phase noise performance of VCO, but the topology won't be equal. Second way is decreasing Itune current. Decreasing Itune will provide lower power consumption in comparison with PMOS active inductor. Also, phase noise performance can be higher because gm of first stage will be decrease, shown as (4.44). Second way is preferred due because power dissipation of active inductor is too much.

As a result, the DC values shown as Figure 4.21 should be provided by NMOS input version. The circuit and sizes are given below as Figure 4.20 and Table 4.3.

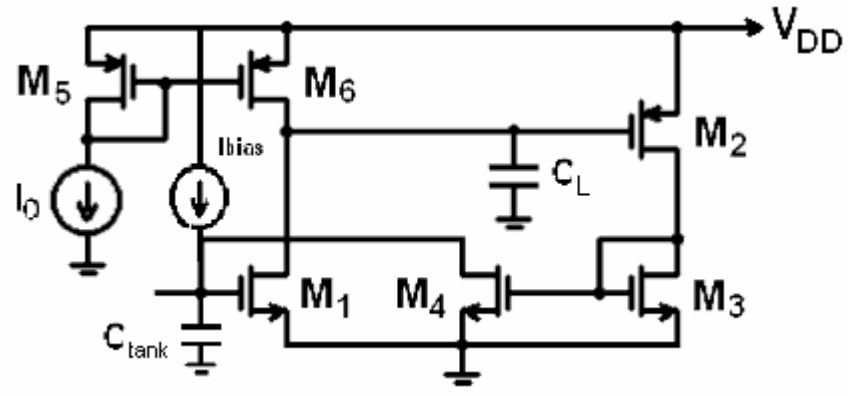

Figure 4.20 : NMOS input active inductor

Table 4.3 : Size and biasing of NMOS input active inductor

$W_{M6,M5}$	7.7um x 4
W_{M1}	6.1um x 6
W_{M2}	6um x 16 x 2
$W_{M3,M4}$	5.9um x 8
L	120nm
Ctank	300fF
CL	450fF
Ibias	3.5mA
Itune	1mA-3mA
Estimated area within %20 error	$76.23um^2$
Power consumption	10.8mW-15.6mW

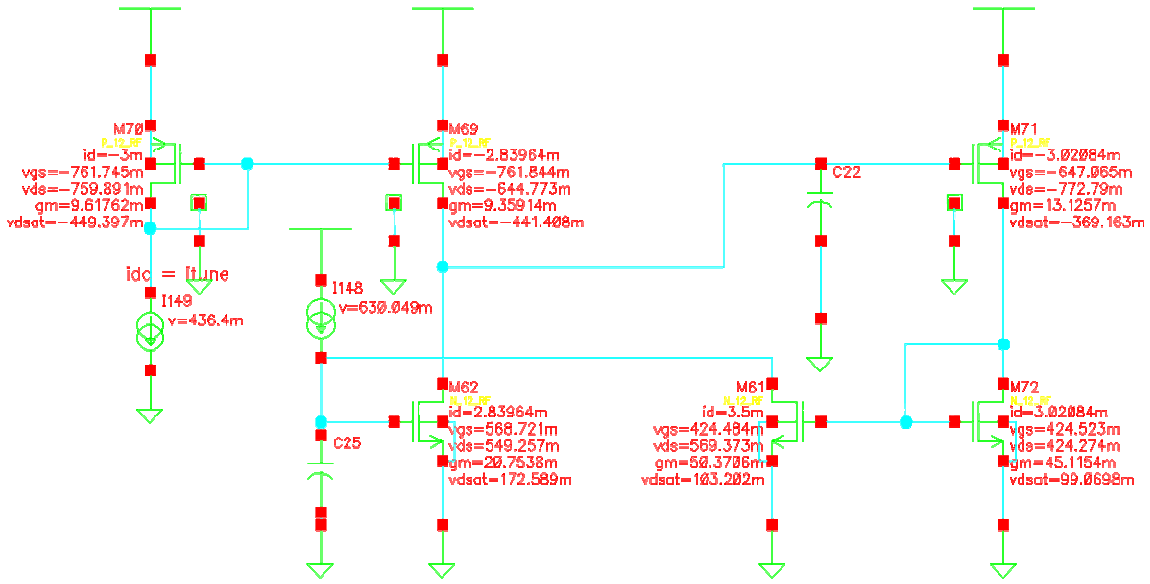

Figure 4.21 : DC Biasing of NMOS input active inductor

4.4.4 LC VCO Based on PMOS Input Active Inductor

In this section, NMOS and PMOS crossed-coupled LC VCO topologies are performed by PMOS active inductor.

4.4.4.1 Design with PMOS Cross-Coupled Topology

The first design based on PMOS crossed-coupled. The circuit is depicted as Figure 4.22 and sizes are given in Table 4.4.

Table 4.4 : Size and biasing of PMOS crossed-couple

$W_{Mc1,Mc2}$	9.6um x 32
W_{Mtail}	9.0um x 16
L	120nm
L_{Mtail}	360nm
Itail	750uA
Ibias	3.5mA
Itune	2.0mA-5.2mA
Estimated area within %20 error	$343um^2$
Power consumption via Itune	27.3mW-42.5mW

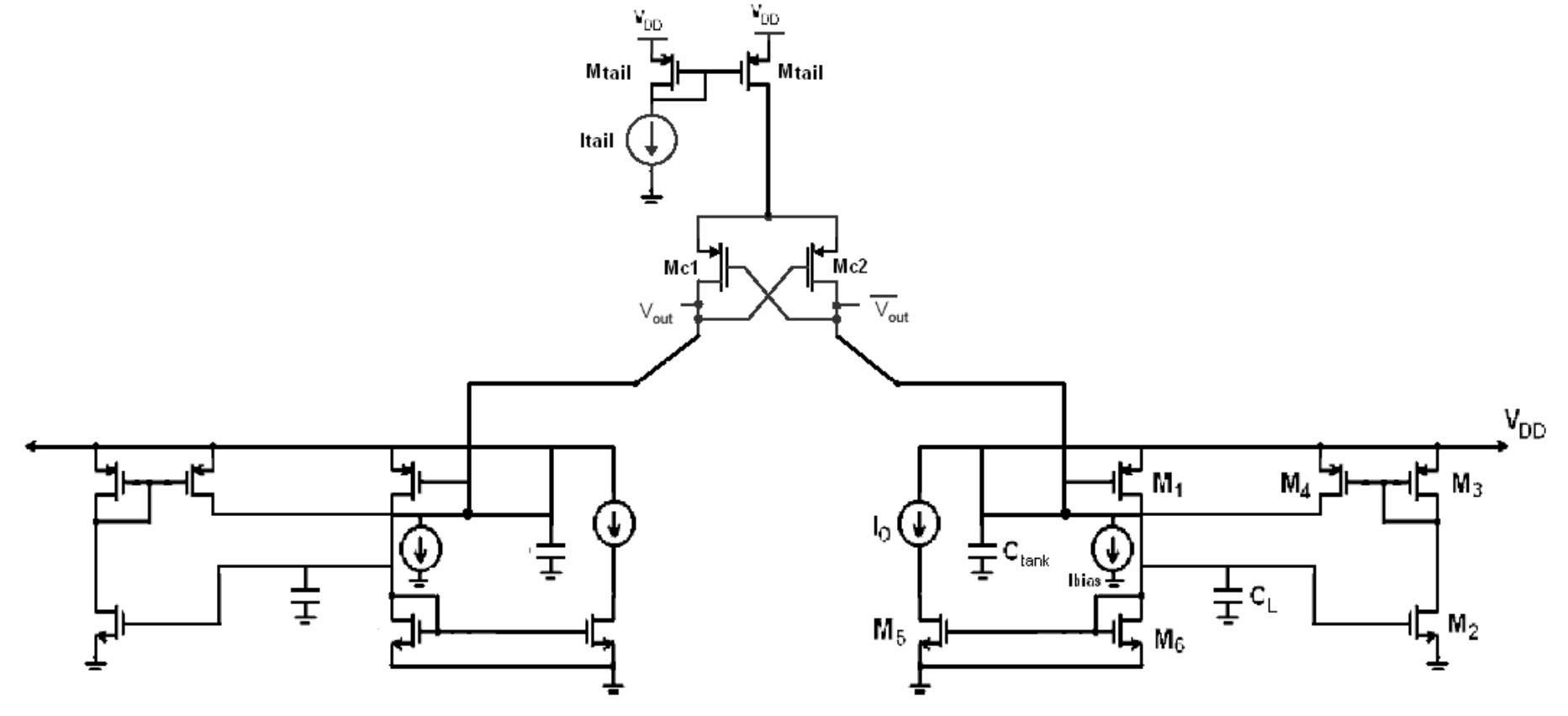

Figure 4.22 : LC VCO with PMOS crossed-coupled and PMOS input active inductor

This configuration is not good because of tail transistor. The tail transistor M50 must be always in saturation to provide same current to tank. The DC voltage of PMOS inductor is 0.632V when Itune=3mA. Drain source voltage of M50 is equal to -0.271V and V_{dssat} is equal to -0.215V. The margin is only 60mV to keep M50in saturation region. Increasing this margin means increasing size of crossed-coupled transistor in order to get a low V_{GS} voltage. However, increasing size of crossed-couple transistor means increasing noise contribution of VCO output too.

To lowering noise contribution of tail current, the size of current mirror is maximized and lengths of these transistors are selected as 360nm which is highest value for UMC013.

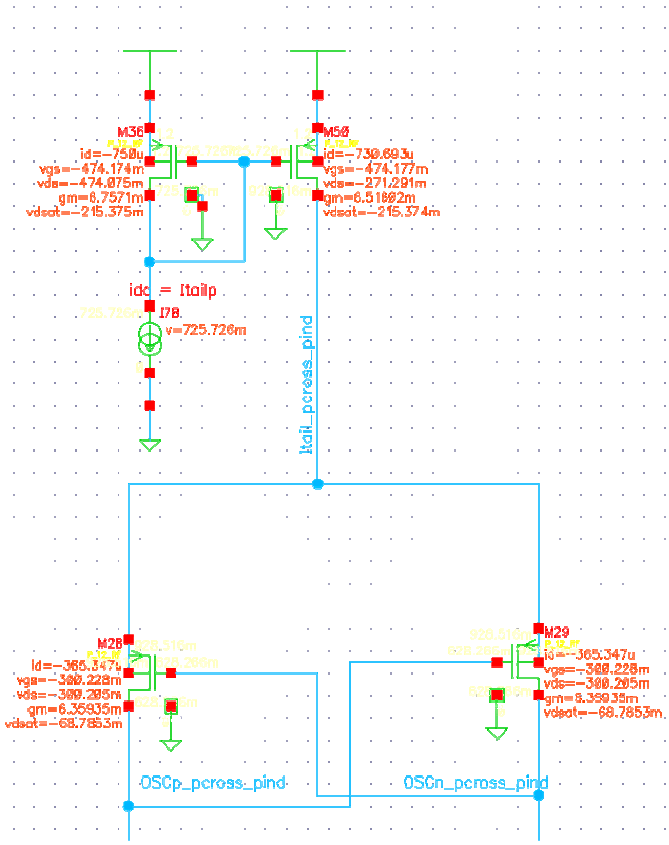

Figure 4.23 : DC of tail current and crossed-coupled PMOS structure

In Figure 4.24 transient analyses is given at Itune=3mA and, the amplitude of oscillation is 125mV which keeps all transistor in saturation region.

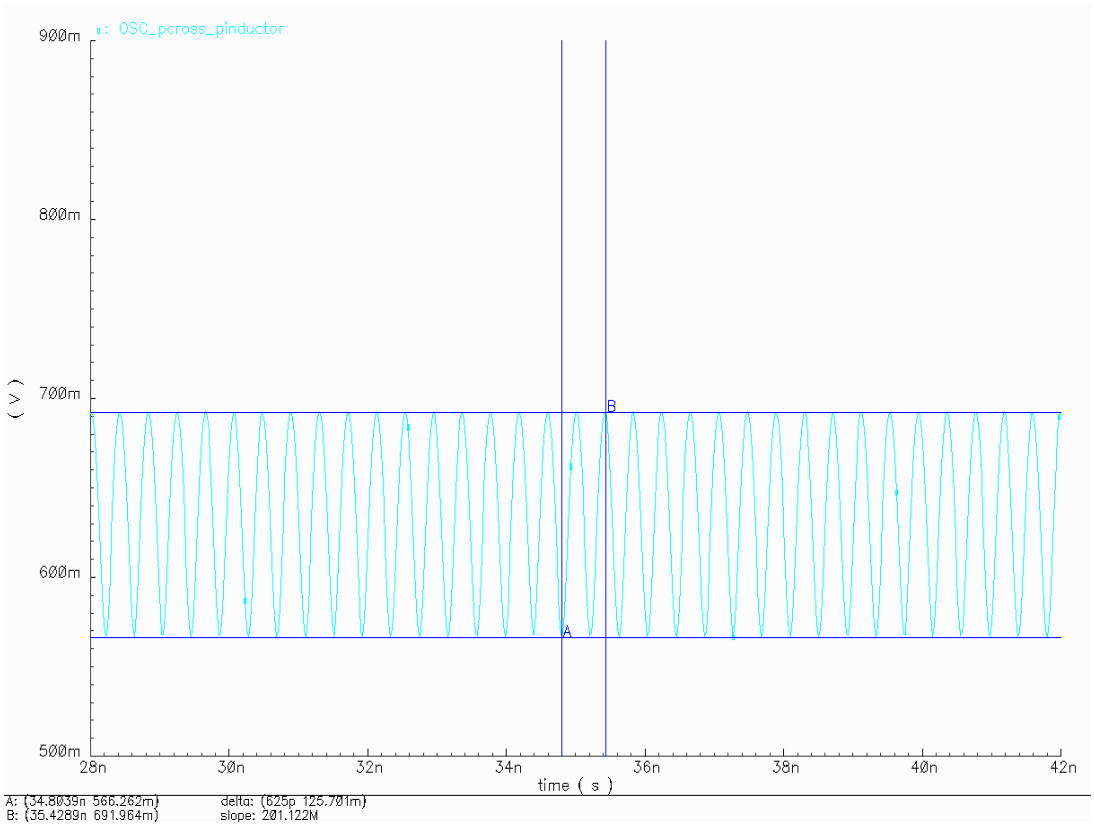

Figure 4.24 : Transient analysis of LC VCO

The amplitude of oscillation versus tuning current is depicted below, and it varies between 80mV to 125mV. The oscillation frequency can be tune by Itune (2mA to 5.2mA) and, the oscillation frequency is between 2.24GHz-2.65GHz.

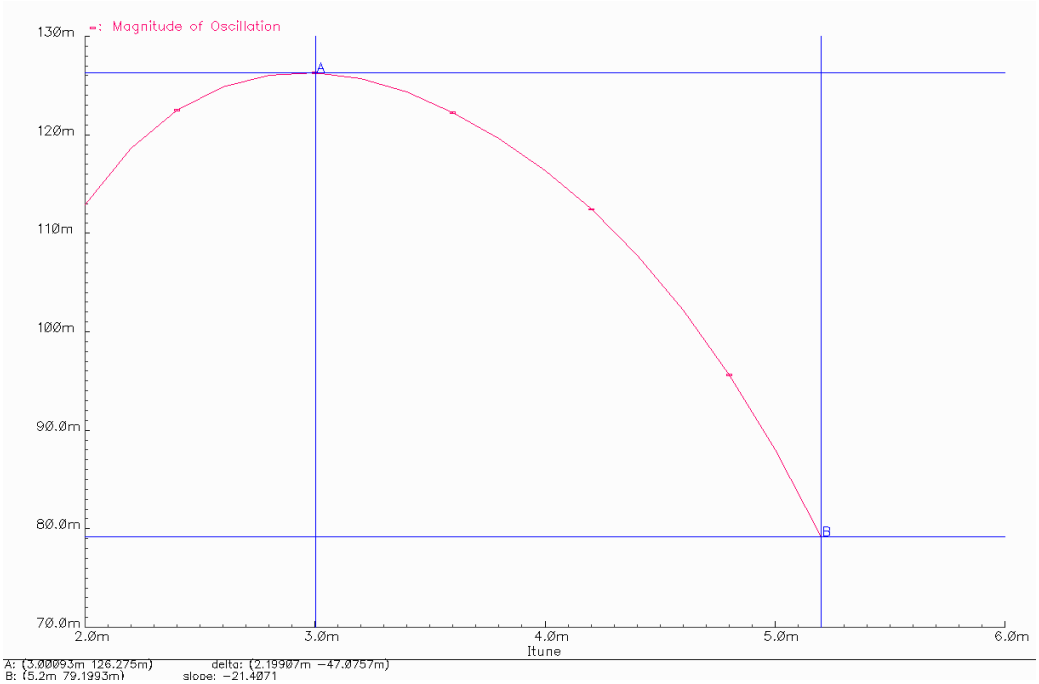

Figure 4.25 : Amplitude of oscillation versus tuning current

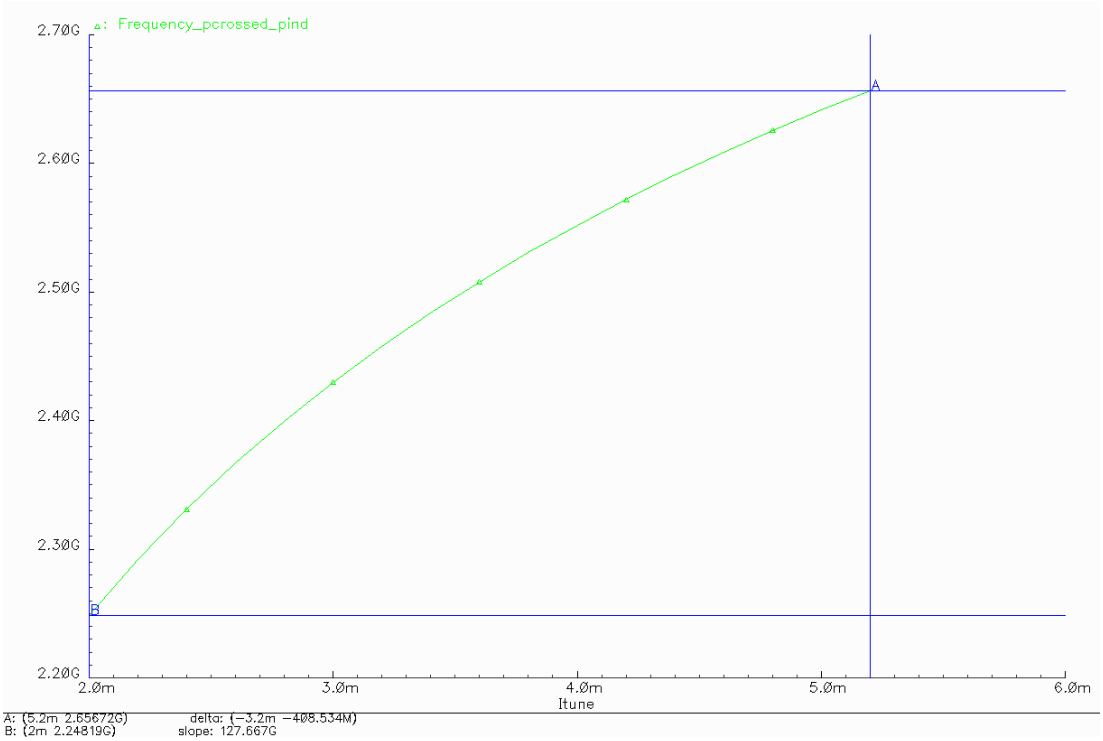

Figure 4.26 : Frequency tuning with tuning current Itune

Another important factor for oscillator is linearity. For linearity, periodic steady state analysis is performed, FFT of oscillation is calculated. As a result, Figure 4.27 is obtained. The even harmonics are suppressed and odd harmonics are gained as 6dB.

Table 4.5 : FFT of single and differential oscillator output

Frequency	Single output	Differential output
0	-4dB	-94.34dB
ω_0	-24.27dB	-18.25dB
$2\omega_0$	-45.26dB	-96.67dB
$3\omega_0$	-65dB	-59.03dB

As a result, SFDR value is 20.99dB for single output and 40.78dB for differentail output.

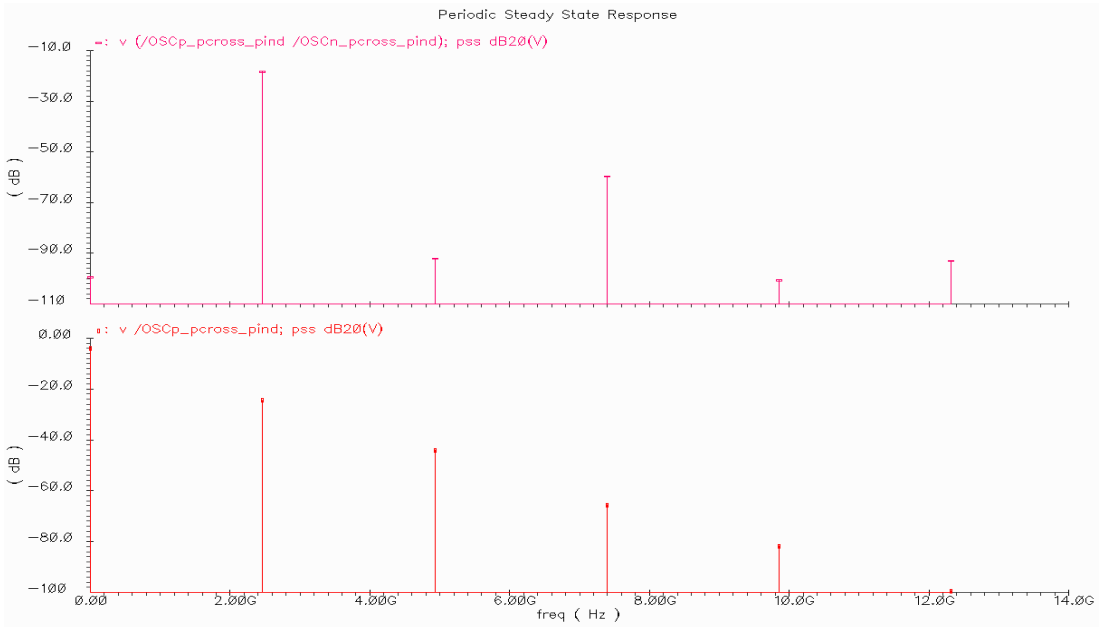

Figure 4.27 : FFT of single and differential oscillation

The calculated phase noise is -88.01dBc/hz at 1MHz offset. This bad result is expected and, it is caused by small oscillation amplitude and noise contribution of active inductor as explained in section 4.31.

Moreover, phase noise at 1MHz versus Itune is extracted in Figure 4.29, and phase noise varies -86dBc/Hz to -88dBc/Hz.

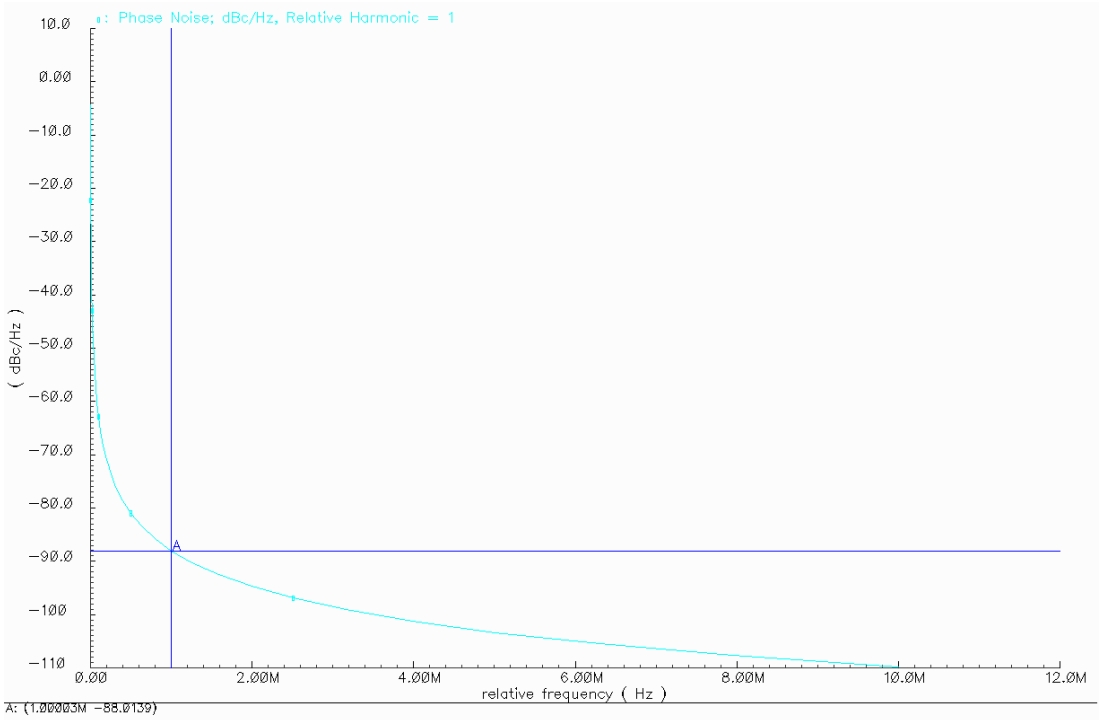

Figure 4.28 : Phase noise of LC VCO with PMOS crossed coupled and PMOS input inductor

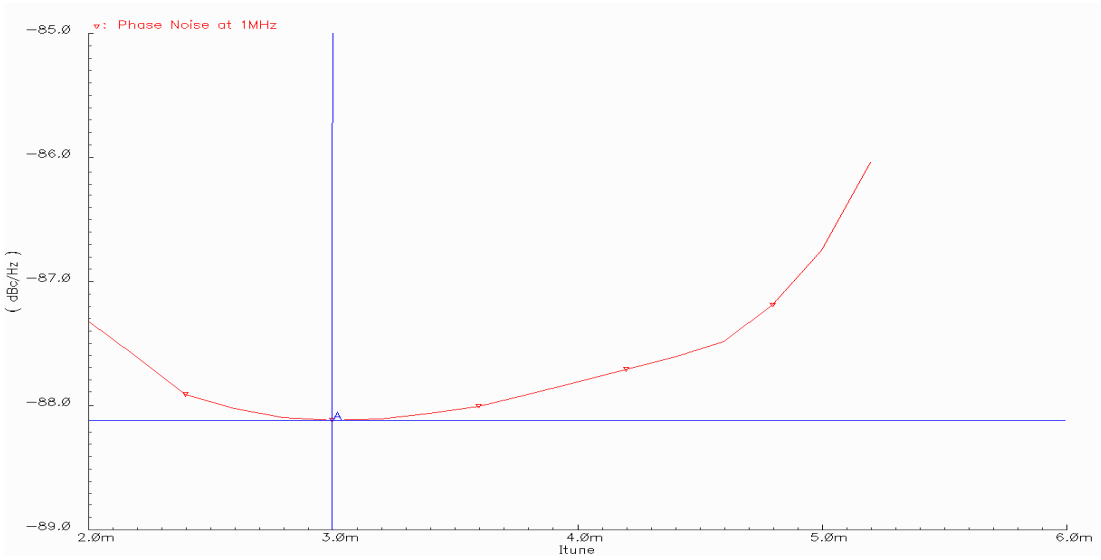

Figure 4.29 : Phase noise at 1MHz versus Itune of LC VCO with PMOS crossed coupled and PMOS input inductor

4.4.4.2 Design with NMOS Cross-Coupled LC Topology

The second design based on NMOS crossed-coupled. The circuit is depicted as Figure 4.30 and sizes are given in Table 4.6.

Table 4.6 : Sizes and biasing of NMOS crossed-couple

$W_{Mc1,Mc2}$	7.2µm x 16 x 2
W_{Mtail}	9.0µm x 16
L	120nm
L_{Mtail}	360nm
Itail	510µA
Ibias	3.5mA
Itune	2.0mA-5.2mA
Estimated area within %20 error	319µm^2
Power consumption via Itune	27mW-42.2mW

This configuration is better than PMOS crossed-coupled LC VCO because of tail transistor M1. The drain source voltages can be done a high value to keep M1 in saturation. The oscillation amplitude and frequency tuning versus Itune are shown as Figure 4.31. The oscillation amplitude is changing between 127mV to 95mV and frequancy can be tuned between 2.35GHz to 2.75GHz.

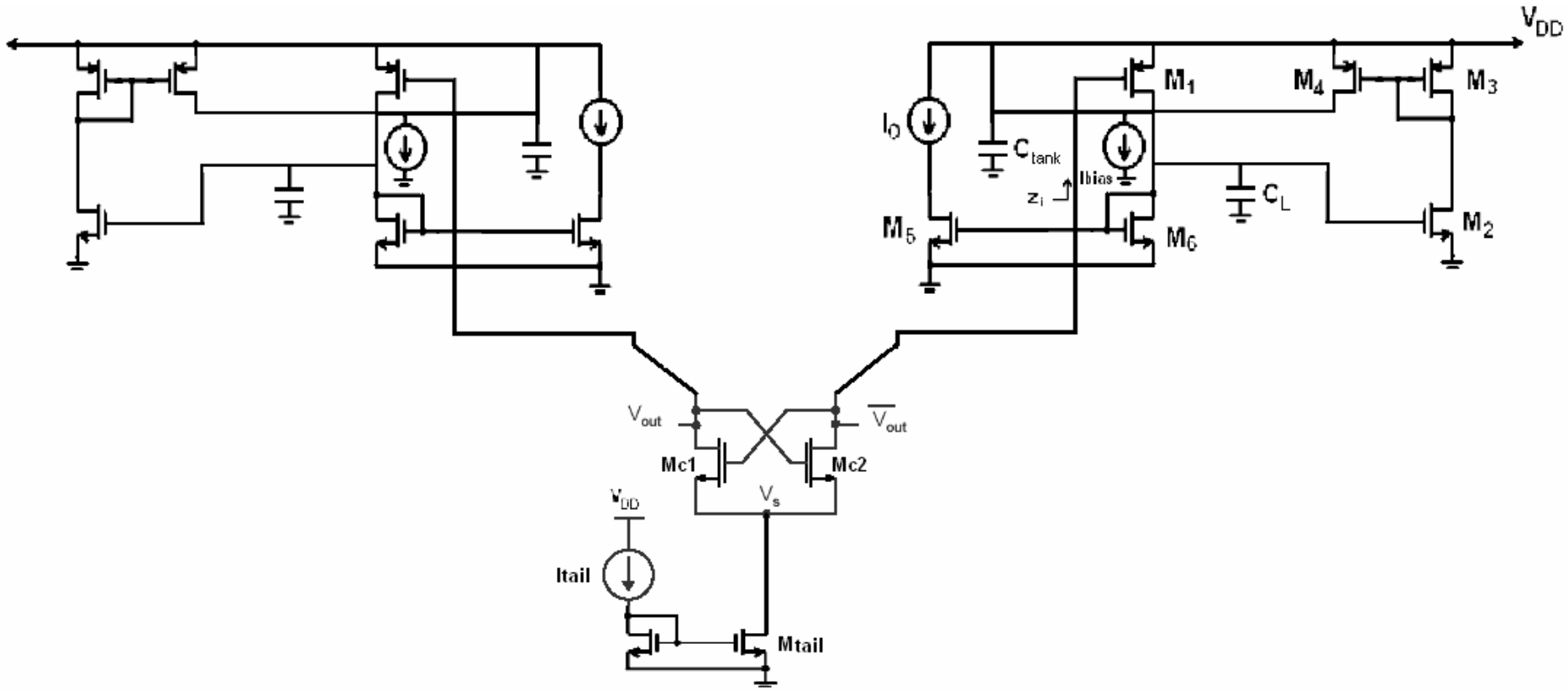

Figure 4.30 : LC VCO with NMOS crossed-coupled and PMOS input active inductor

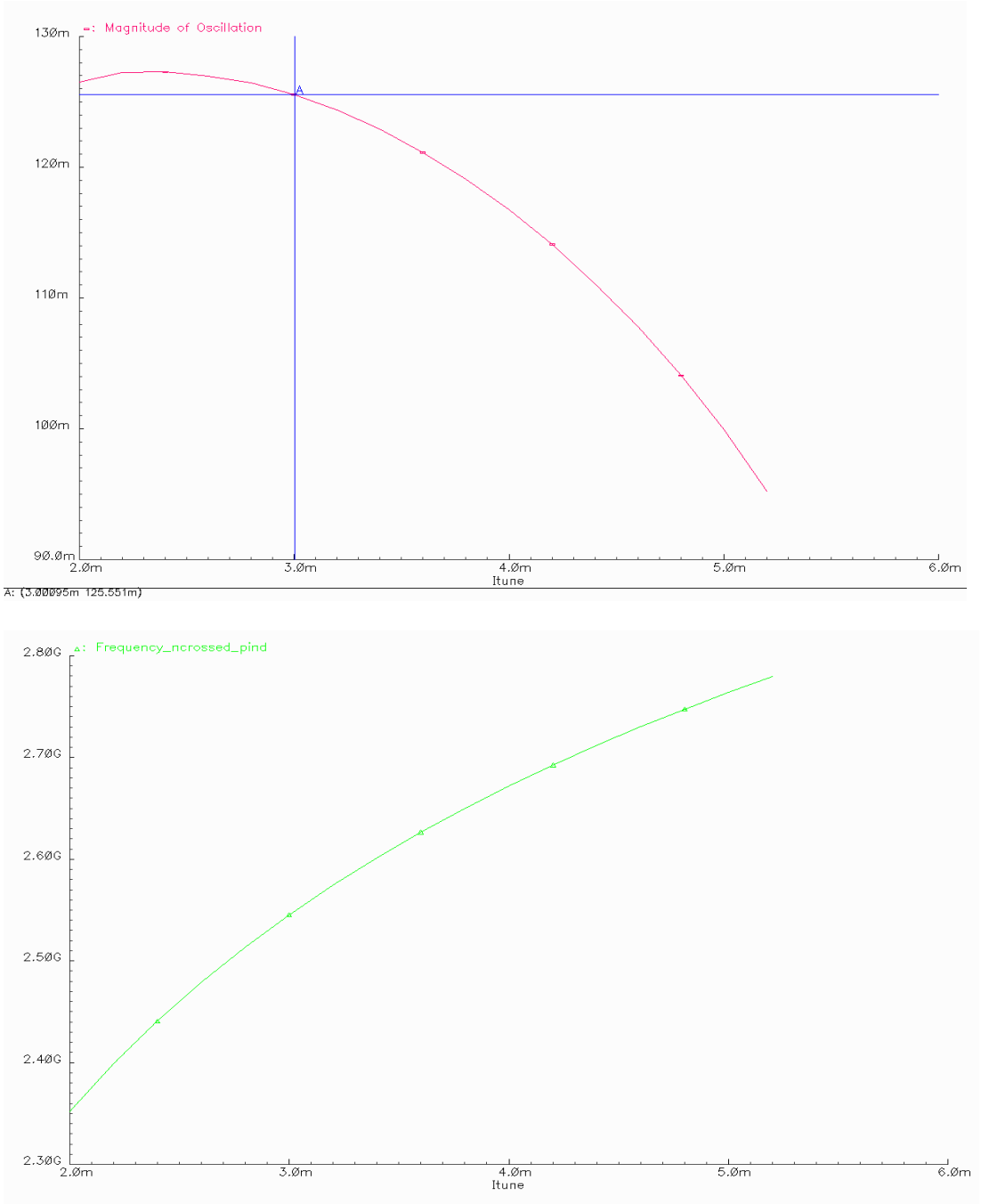

Figure 4.31 : Oscillation amplitude and frequency tuning versus Itune of LC VCO with NMOS crossed-coupled and PMOS input active inductor

The calculated phase noise is -88.7dBc/Hz at 1MHz offset. Phase noise performance of NMOS crossed coupled transistor is like previous design because NMOS crossed-coupled transistors are complement of PMOS crosses-coupled transistors.

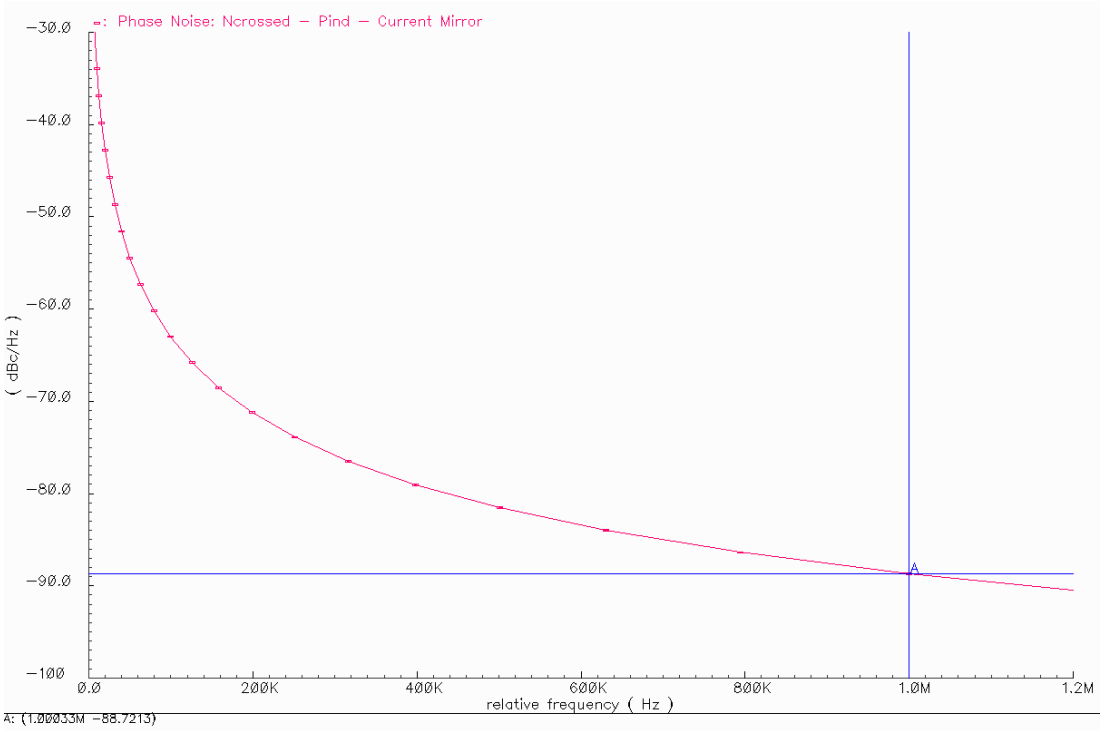

Figure 4.32 : Phase noise of LC VCO with NMOS crossed coupled and PMOS input inductor

FFT results are given in Table 4.7 for linearity of this VCO design. These values are nearly same values of PMOS crossed coupled LC VCO.

Table 4.7 : FFT of single and differential oscillator output of LC VCO with NMOS crossed coupled and PMOS input inductor

Frequency	Single output	Differential output
0	-4dB	-99.39dB
ω_0	-24.44dB	-18.42dB
$2\omega_0$	-44.02dB	-92.17dB
$3\omega_0$	-65.66dB	-59.68dB

4.4.5 LC VCO Based on NMOS Input Active Inductor

In this section, NMOS and PMOS crossed-coupled LC VCO topologies are performed by NMOS active inductor.

4.4.5.1 Design with PMOS Cross-Coupled Topology

The third design based on PMOS crossed-coupled. The circuit is depicted as Figure 4.33 and sizes are given in Table 4.8.

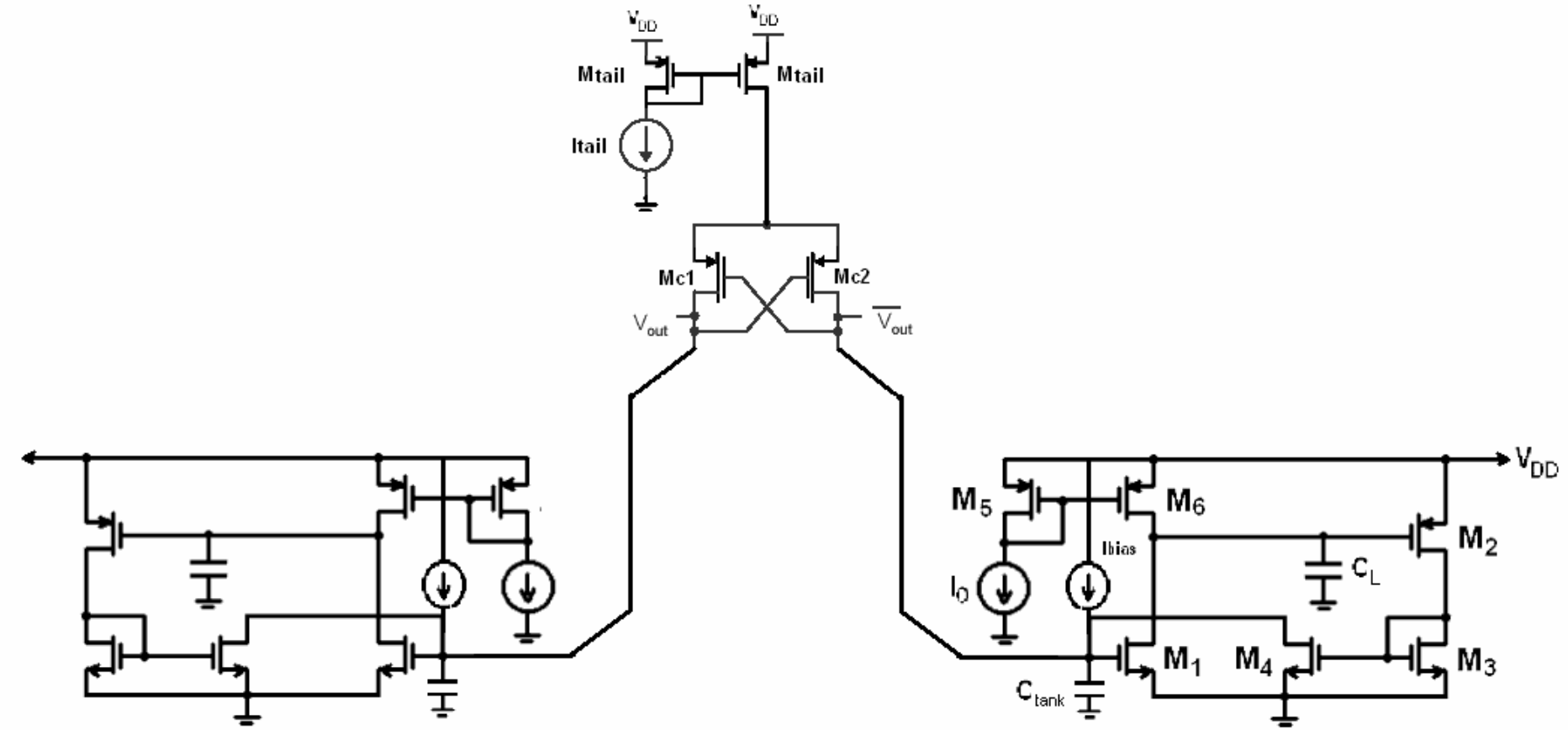

Figure 4.33 : LC VCO with PMOS crossed-coupled and NMOS input active inductor

Table 4.8 : Sizes and biasing of NMOS crossed-couple

$W_{Mc1,Mc2}$	9.6µm x 32
W_{Mtail}	9.0µm x 16
L	120nm
L_{Mtail}	360nm
Itail	690µA
Ibias	3.5mA
Itune	1mA-3mA
Estimated area within %20 error	282.4µm^2
Power consumption via Itune	22.42mW-32mW

This configuration is like NMOS crossed-coupled with PMOS input active inductor, so, it is a good configuration because of tail transistor M10. The drain source voltages can be done a high value to keep M10 in saturation. In this configuration V_{DS} is equal to -0.431V.

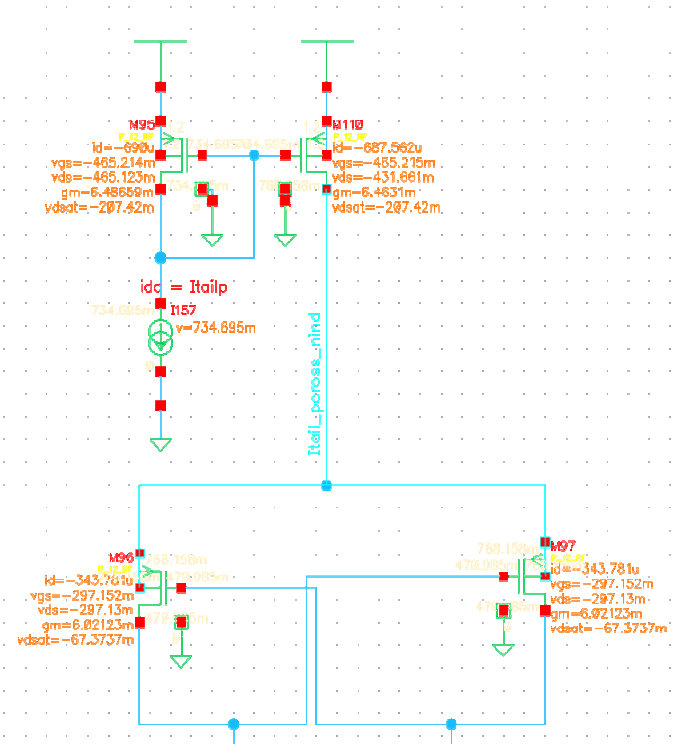

Figure 4.34 : DC values of tail and crossed-coupled transistors

The oscillation amplitude and frequency tuning versus Itune are shown as Figure 4.31. The oscillation amplitude is changing between 130mV to 65mV and frequency can be tuned between 2.14GHz to 2.71GHz.

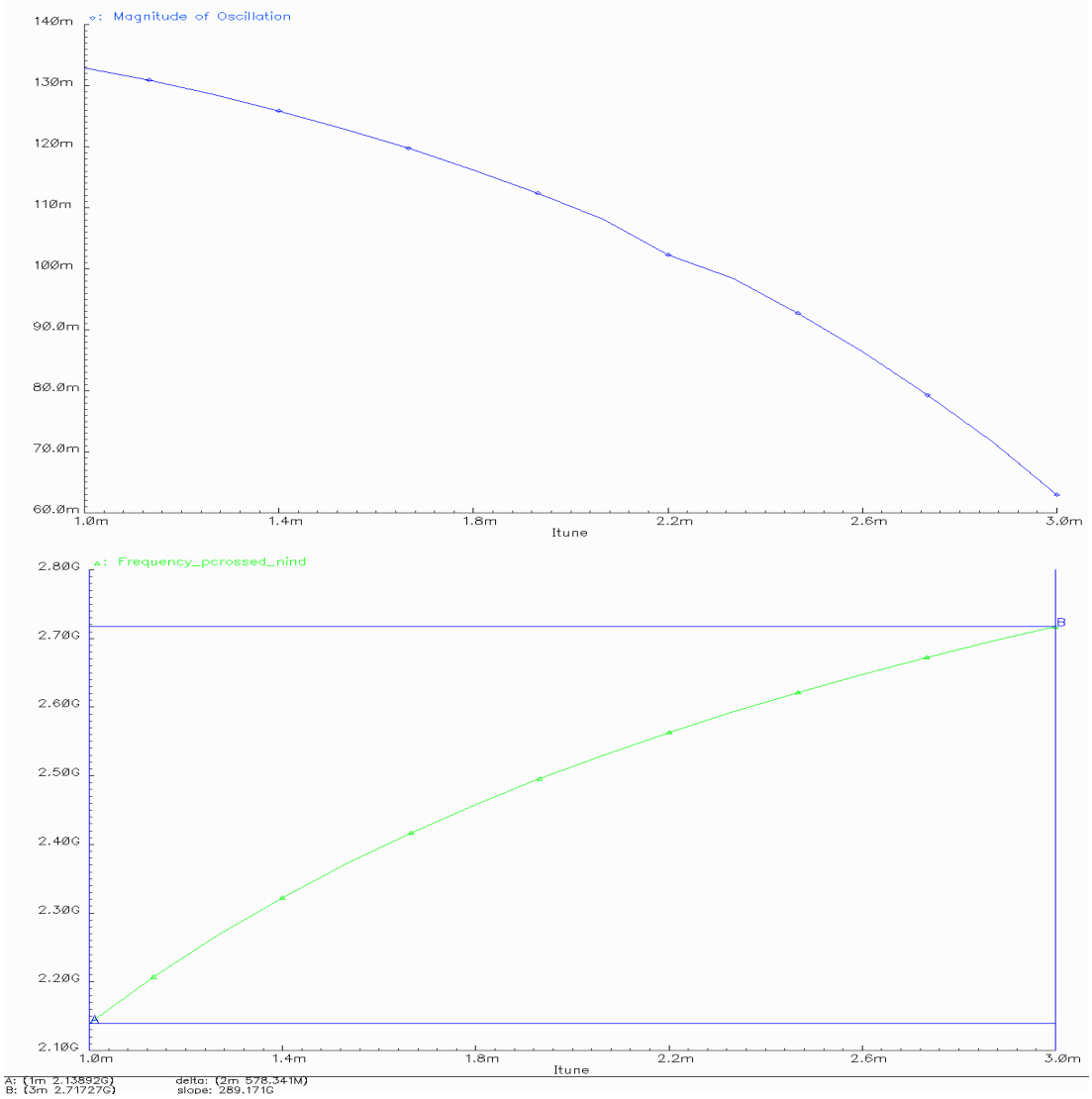

Figure 4.35 : Oscillation amplitude and frequency tuning versus Itune of LC VCO with PMOS crossed-coupled and NMOS input active inductor

The calculated phase noise is -89dBc/Hz at 1MHz offset. Phase noise performance is not changed like previous designs because complementing all transistors.

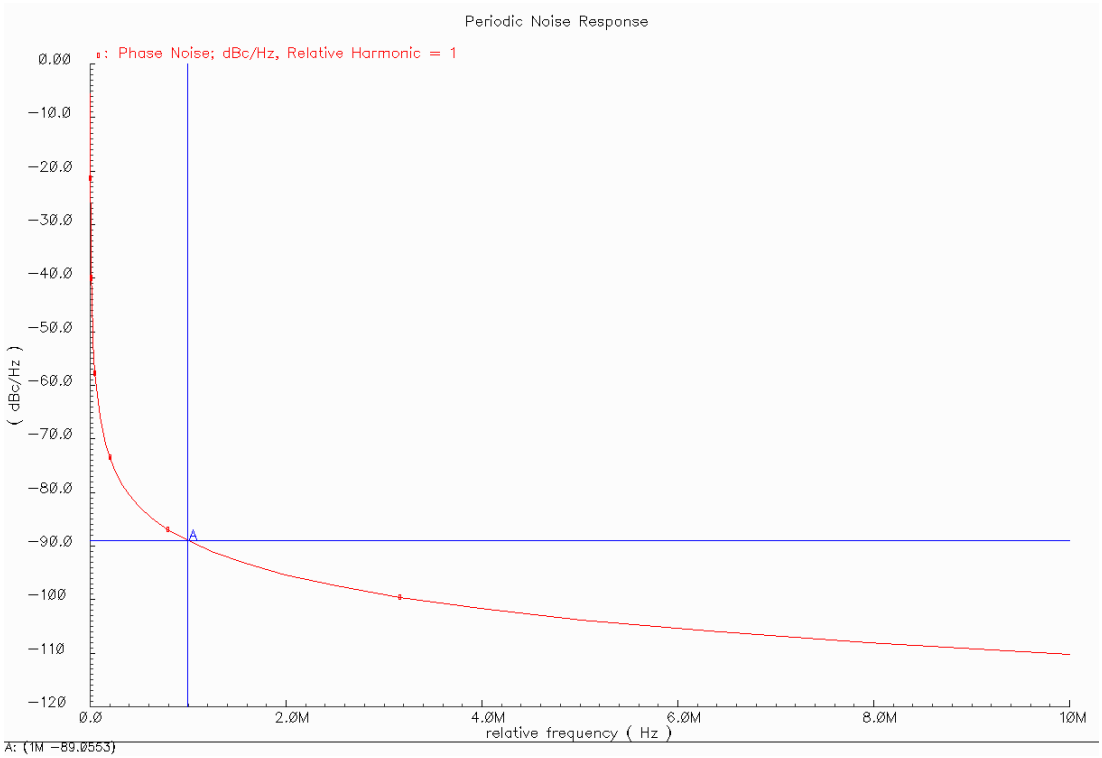

Figure 4.36 : Phase noise of LC VCO with NMOS crossed coupled and PMOS input inductor

FFT results are given in Table 4.9 for linearity of this VCO design. These values are nearly same values of previous LC VCO designs.

Table 4.9 : FFT of single and differential oscillator output of LC VCO with NMOS crossed coupled and PMOS input inductor

Frequency	Single output	Differential output
0	-6dB	-97dB
ω_0	-24.48dB	-18.46dB
$2\omega_0$	-42.41dB	-94.56dB
$3\omega_0$	-66.3dB	-60.22dB

4.4.5.2 Design with NMOS Cross-Coupled Topology

The fourth design is based on PMOS crossed-coupled. The circuit is depicted as Figure 4.37 and sizes are given in Table 4.10.

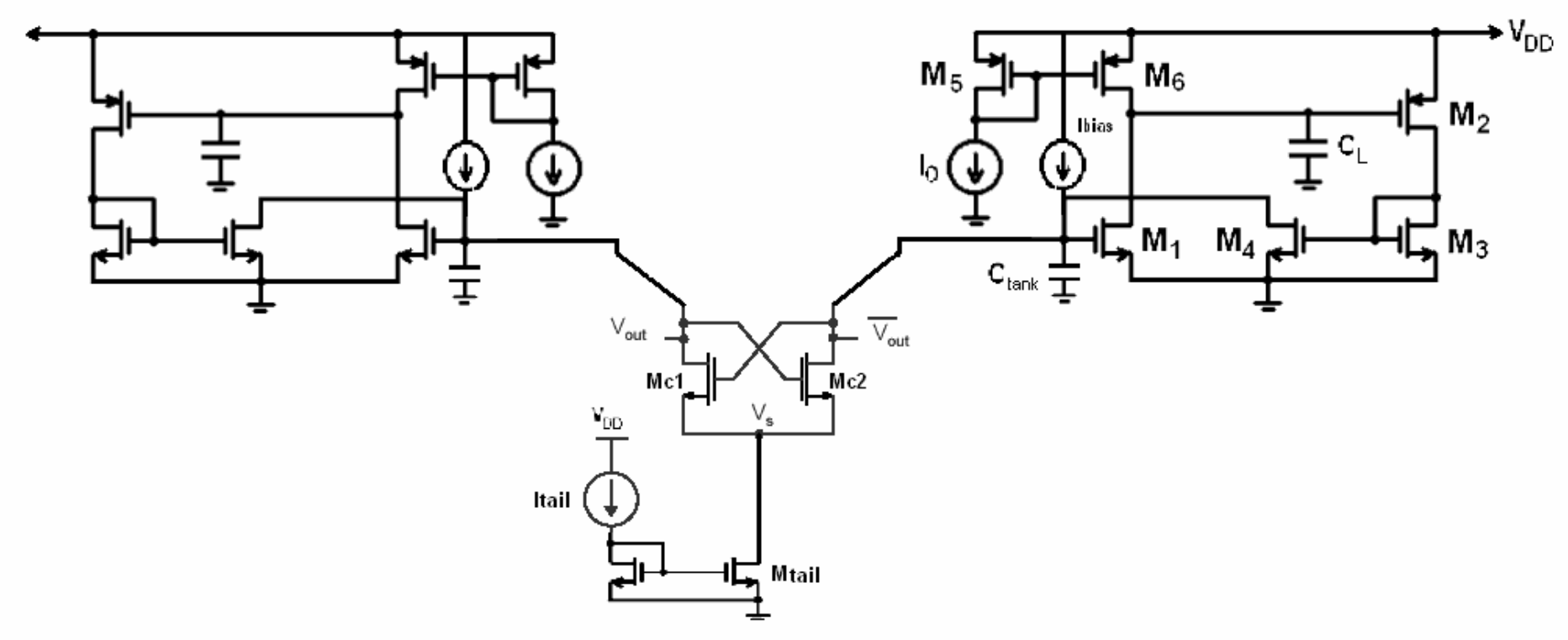

Figure 4.37 : LC VCO with NMOS crossed-coupled and NMOS input active inductor

Table 4.10 : Sizes and biasing of PMOS crossed-couple

$W_{Mc1,Mc2}$	7.2µm x 16 x 2
W_{Mtail}	9.0µm x 16
L	120nm
L_{Mtail}	360nm
Itail	450µA
Ibias	3.5mA
Itune	1.0mA-3mA
Estimated area within %20 error	209µm^2
Power consumption via Itune	22.14mW-31.74mW

This configuration is like PMOS crossed-coupled with PMOS input active inductor, so, it is not a good configuration because of tail transistor M81. The drain source voltages is low and -197mV where V_{DSsat} is equal to 156mV, so margin is 41mV in order to keep M80 in saturation region.

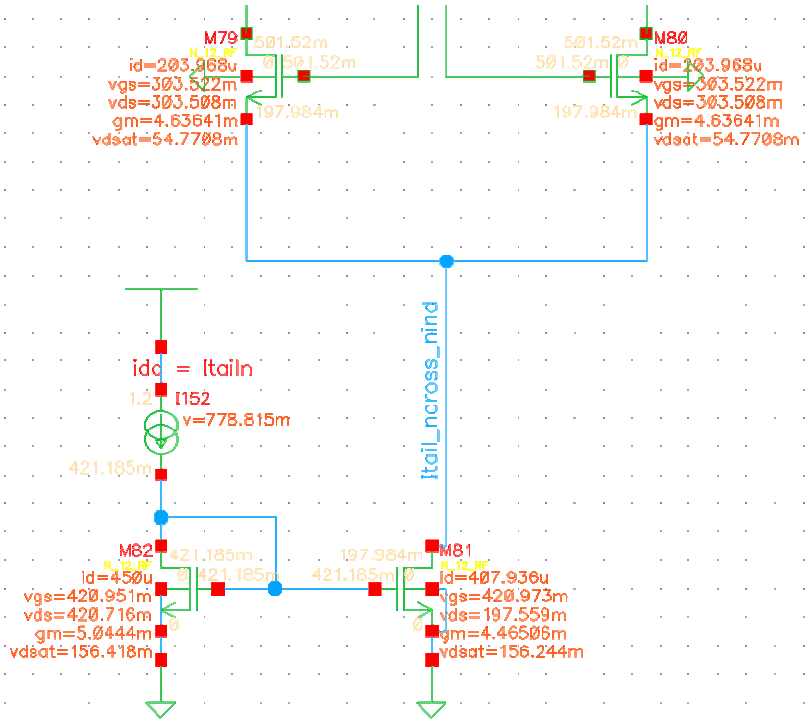

Figure 4.38 : DC values of tail and crossed-coupled transistors

The transient analysis is depicted as Figure 4.39 at Itune=1.5mA. The oscillation amplitude and frequency tuning versus Itune are shown as Figure 4.40 and Figure 4.41. The oscillation amplitude is changing between 100mV to 65mV and frequency can be tuned between 2.24GHz to 2.81GHz.

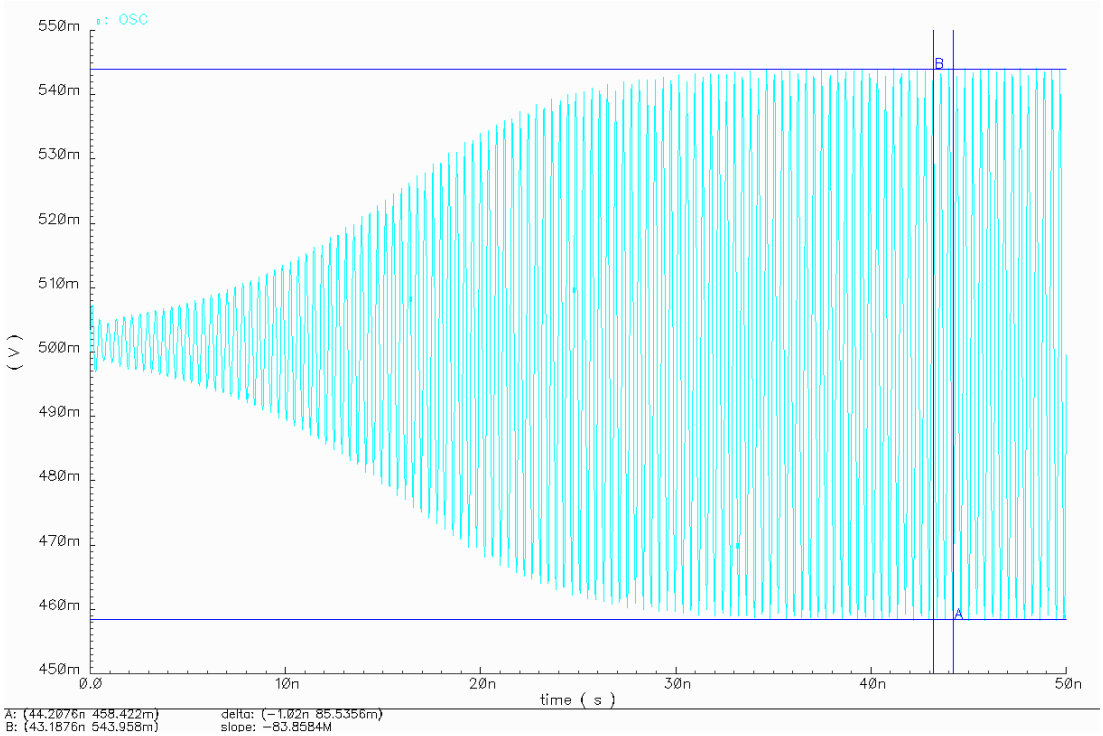

Figure 4.39 : Transient analysis of LC VCO with PMOS crossed-coupled and NMOS input active inductor (Itune=1.5mA)

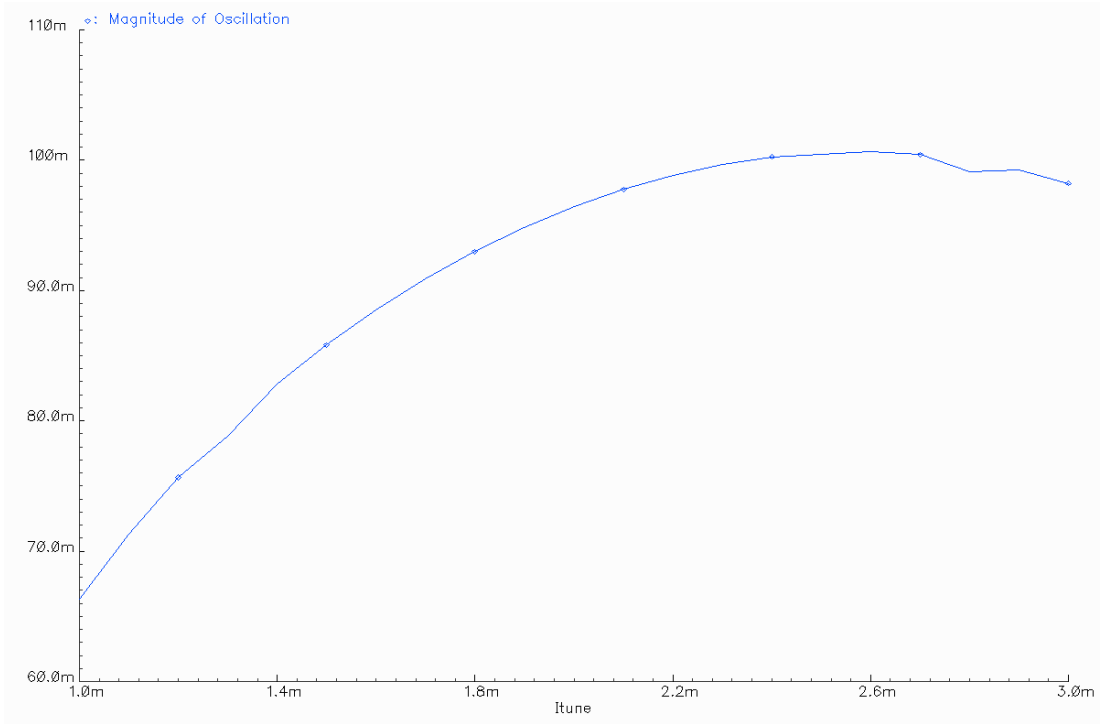

Figure 4.40 : Oscillation amplitude and frequency tuning versus Itune of LC VCO with NMOS crossed-coupled and NMOS input active inductor

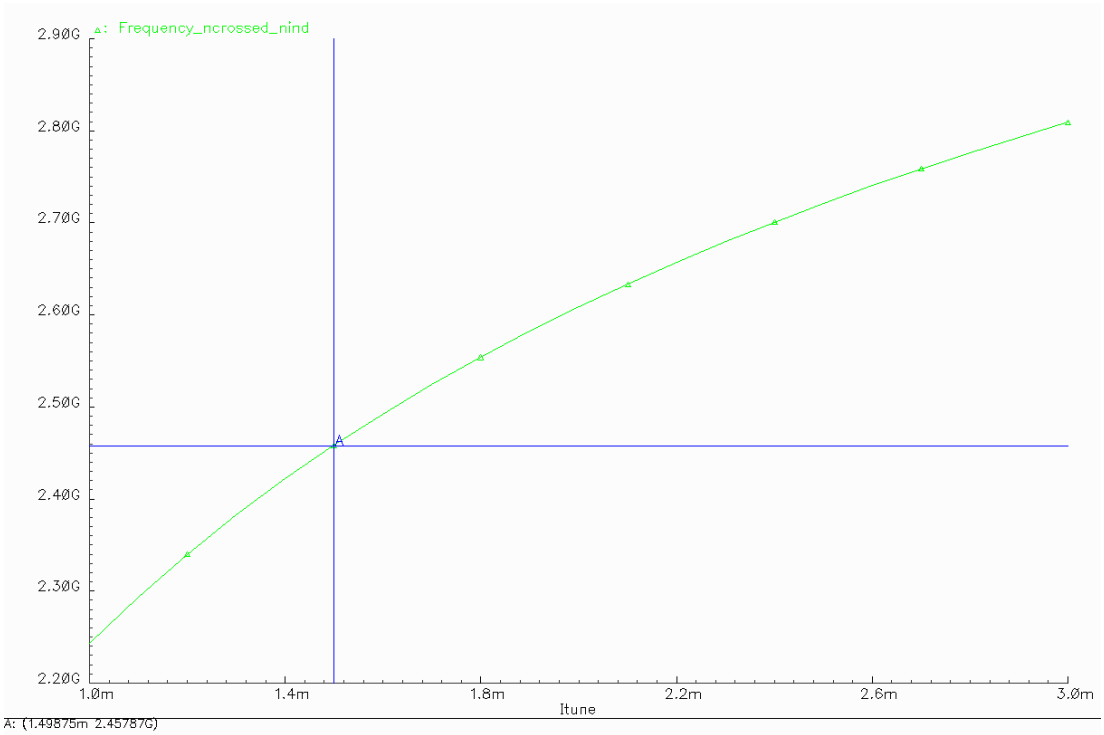

Figure 4.41 : Oscillation amplitude and frequency tuning versus Itune of LC VCO with NMOS crossed-coupled and NMOS input active inductor

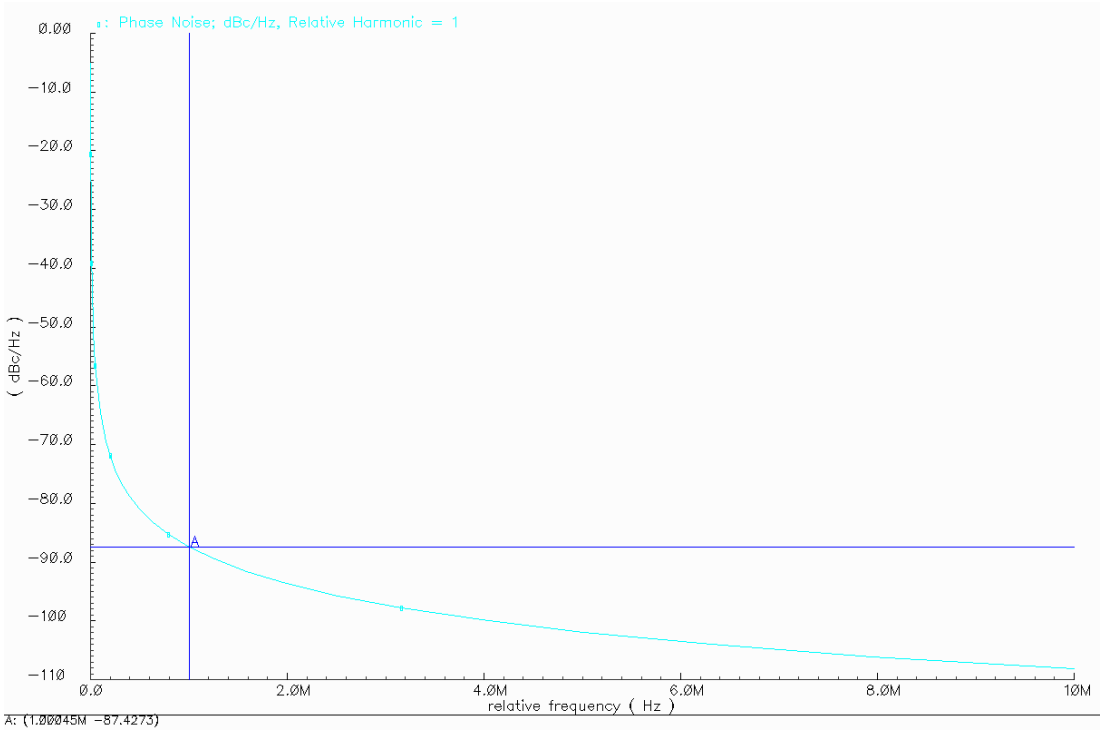

Figure 4.42 : Phase noise of LC VCO with NMOS crossed coupled and PMOS input inductor

The calculated phase noise is -87.4dBc/Hz at 1MHz offset. Phase noise performance is not changed like previous designs because complementing all transistors.

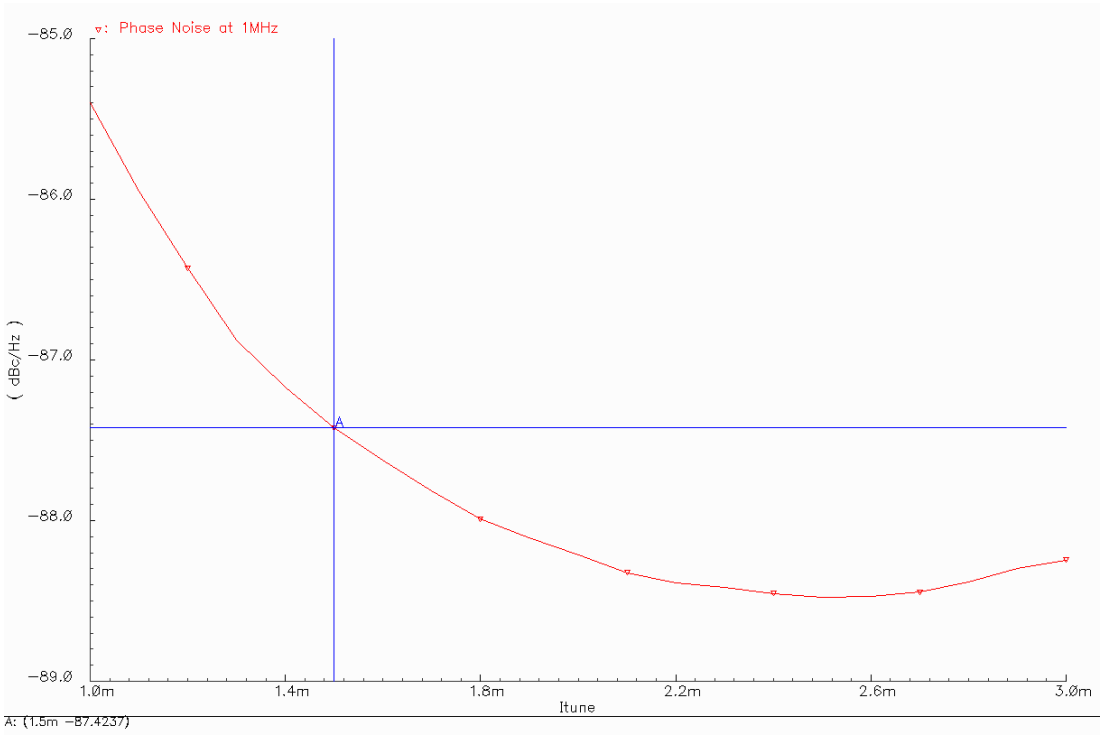

Figure 4.43 : Phase noise at 1MHz offset of LC VCO with NMOS crossed coupled and PMOS input inductor

FFT results are given in Table 4.11 for linearity of this VCO design. These values are nearly same values of previous LC VCO designs.

Table 4.11 : FFT of single and differential oscillator output of LC VCO with NMOS crossed coupled and NMOS input inductor

Frequency	Single output	Differential output
0	-6dB	-97.2dB
ω_0	-27.4dB	-21.4dB
$2\omega_0$	-53.23dB	-90.54dB
$3\omega_0$	-73.42dB	-67.46dB

4.5 Conclusion

As a result, the phase noise performance does not changed too much in different topologies due to the complementing all transistor. The phase noise is changing vicinity of -88dBc/Hz.

Moreover, the phase noise performance is calculated again when VCO biasing with a resistor which provides 750uA for PMOS crossed-coupled and PMOS input active inductor LC VCO topology. Calculated phase noise is 88.07dB which doesn't affect

phase noise at 1MHz offset frequency. However, phase noise performance is increasing at low frequency shown as Figure 4.44.

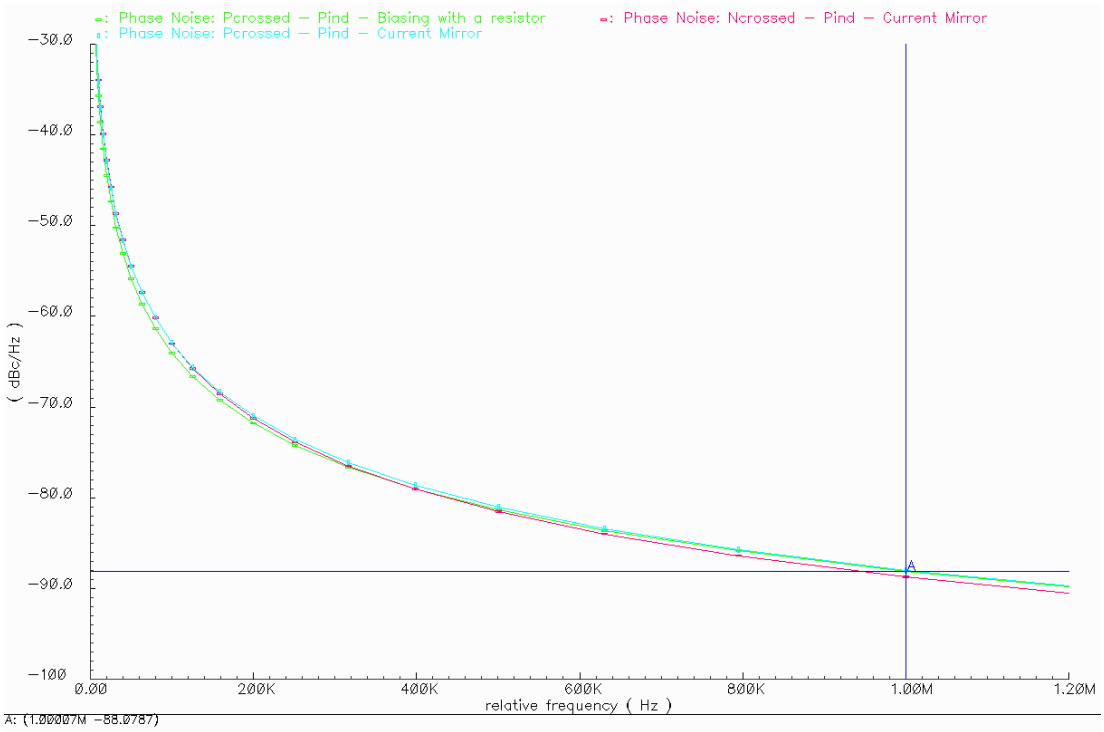

Figure 4.44 : Comparison of phase noise performance

Power consumption of LC VCO topologies with NMOS input active inductor is lower than PMOS input active inductor. Also, PMOS active inductors require larger areas which contribute more parasitic capacitor in comparison with NMOS active inductor.

Moreover, designing LC VCO based on NMOS crossed-coupled and NMOS active inductor, and PMOS crossed-coupled and PMOS active inductor is not a good configuration due to the tail current source. In Figure 4.45 and Figure 4.46, the drain voltages of tail current source transistor are depicted. The drain source voltages of "NMOS crossed-coupled NMOS input active inductor" and "PMOS crossed-coupled PMOS input active inductor" configuration are lower than "PMOS crossed-coupled NMOS input active inductor" and "NMOS crossed-coupled PMOS input active inductor" configuration.

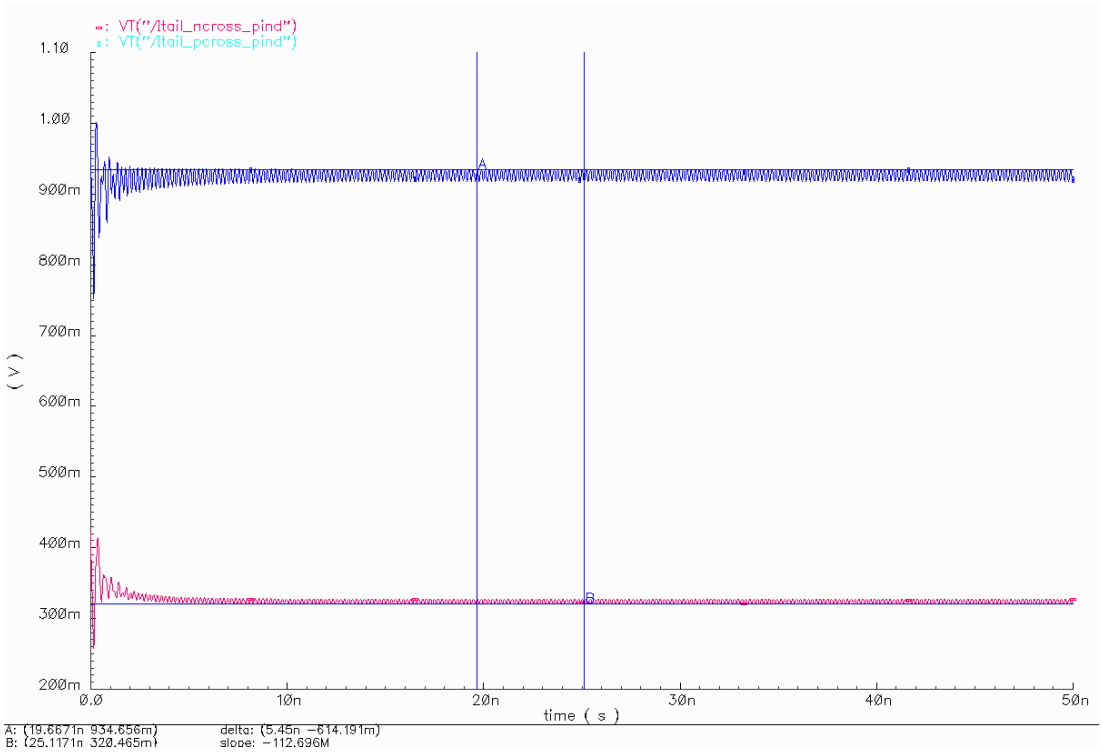

Figure 4.45 : Comparison of drain voltages of PMOS/NMOS crossed-coupled with PMOS active inductor

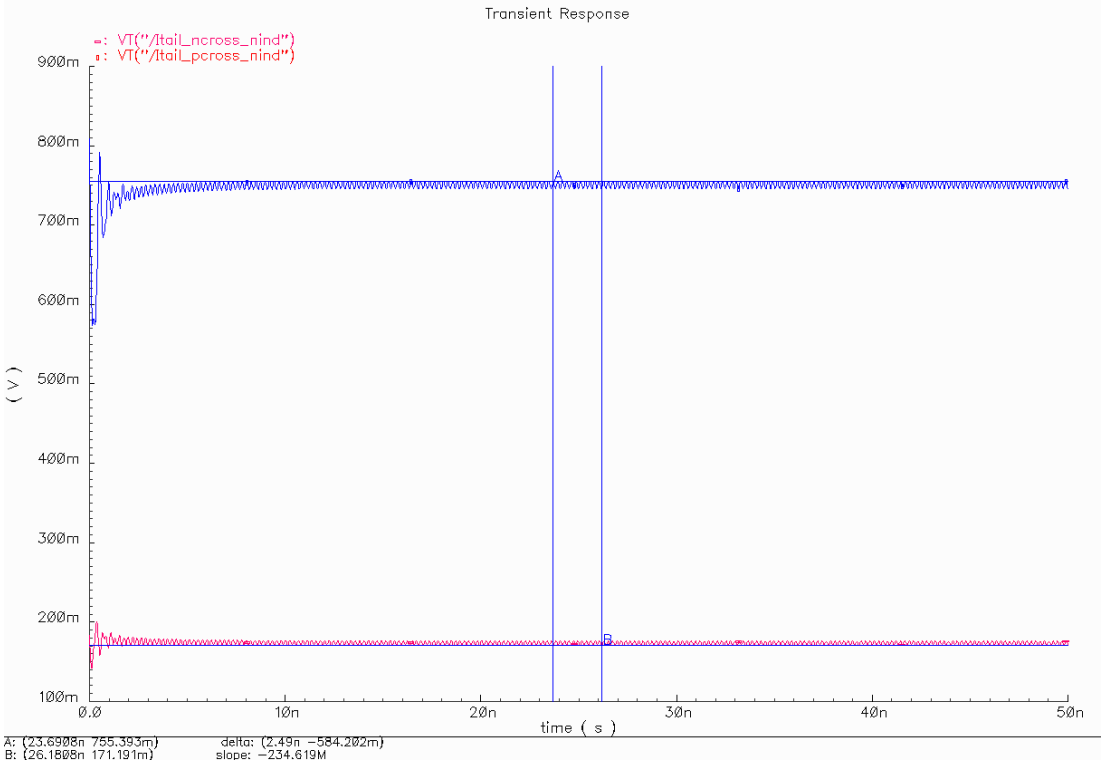

Figure 4.46 : Comparison of drain voltages of PMOS/NMOS crossed-coupled with NMOS active inductor

5. VCO LITERATURE AND COMPARISON

Publications based on different VCO topologies are mentioned for comparison in Table 5.1.

Table 5.1 : Comparison with other works

Ref.	Topology	Process	Area	Freq.	Pow.	Phase Noise
[17]	Quadrature NPN crossed-coupled	0.18µm SiGe 1.8V	0.25mm^2	6GHz	19.44mW	-106dBc/Hz @1MHz
[18]	NMOS crossed-coupled	0.25µm CMOS 2.5V	1mm^2	10GHz	50mW	-113dBc/Hz @600kHz
[19]	Quadrature NMOS crossed-coupled with active inductor	0.25 TSMC 2.5V	n.a.	2.4GHz	26mW	-79.42dBc/Hz @100kHz
[20]	Symmetrical LC VCO	0.35µm CMOS	0.43mm^2	1GHz	n.a	-135dBc/Hz @1MHz
[21]	Symmetrical LC VCO	0.24µm CMOS 2.5V	n.a	5.8GHz	12.5mW	-112dBc/Hz @1MHz
This Work	PMOS crossed-coupled LC VCO with active inductor	0.13µm UMC013 1.2V	209µm^2	2.4GHz	31.74mW	-89dBc/Hz @1MHz

Consequently, the most advantage of this work is die area, and estimated layout of this work is significantly smaller than all listed publications.

For phase noise performance, this work is not seem enough for wireless communication.

The power consumption of this work is comparable with the other works.

6. CONCLUSION

In this work, the noise properties of active inductors and LC VCO are analyzed. The wireless communication standards are aimed to be supported for VCO designs at 1.2V 0.13 μm UMC013 CMOS process.

Simulations and theoretical calculation shows that phase noise performance of the LC VCO based on active inductors is lower than classical LC VCO with passive inductors.

Consequently, the objective is not realized due to phase noise constraint. For Bluetooth and 802.11b, g, the required phase noise value is -115dBc/Hz at 1MHz offset. However, the implemented LC VCO oscillator phase noise is -89dBc/Hz at 1MHz. The reason of low phase noise is active inductor's low input swing and its noise contribution.

If input voltage swing of active inductor increases, the amplitude of oscillation will be increase too, so the signal to noise ratio will enlarge. To achieve this, another process which have a higher voltage supply such as 1.8V can be selected instead of UMC013 1.2V. However, using a higher V_{DD} will boost the power consumption of LC VCO.

Also the power consumption of LC VCO based on active inductor is high. Designed LC VCO consumes nearly 30mW at 2.71GHz.

Tuning range of designed oscillator covers 2.4GHz-2.5GHz as 2.14GHz-2.71GHz.

The advantage of using active inductor is area. The estimated layout area is 209 μm^2 with 20% estimation error. The area value is smaller than classic LC VCO designs with passive inductors.

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8. BIOGRAPHY

Alphan Şahin was born in Bandırma, Turkey in 1983. He received the B.Sc. degree in electronics engineering from Istanbul Technical University in 2005. He received the B.Sc. double major program degree in telecommunication engineering from Istanbul Technical University in 2006. He is currently working toward the M.Sc. degree at Istanbul Technical University.