REPUBLIC OF TÜRKİYE
ADANA ALPARSLAN TÜRKEŞ SCIENCE AND TECHNOLOGY UNIVERSITY

GRADUATE SCHOOL
ELECTRICAL AND ELECTRONIC ENGINEERING DEPARTMENT

IMPROVING THE NEAR INFRARED REGION SENSITIVITY OF CMOS IMAGE SENSORS

MUSTAFA ÖZBER YÜCEKUL

Ph.D.

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ADANA, 2025

Thesis Defence Date

11/12/2025

DECLARATION OF CONFORMITY

In this thesis study, which was prepared following the thesis writing rules of Adana Alparslan Türkeş Science and Technology University Institute of Graduate School, I declare that I provide all the information, documents, evaluations and results in accordance with scientific ethics and moral codes without resorting to any means or assistance that would be contrary to scientific ethics and traditions. I also declare that I refer to all of the articles I used in this study with appropriate references and accept all moral and legal consequences if a situation is found contrary to my statement regarding my work.

11/12/2025

[Signature]

Mustafa Özber YÜCEKUL

ÖZET

CMOS GÖRÜNTÜ SENSÖRLERİNİN YAKIN KIZILÖTESİ BÖLGE HASSASİYETİNİN İYİLEŞTİRİLMESİ

Mustafa Özber YÜCEKUL

Doktora, Elektrik-Elektronik Anabilim Dalı

Danışman: Prof. Dr. Mahmud Yusuf TANRIKULU

Aralık 2025, 87 sayfa

Silisyum tabanlı CMOS görüntü sensörleri, yakın kızılötesi (NIR) bölgede düşük soğurma katsayısına sahip olduğundan kuantum verimliliği sınırlı kalmakta ve biyomedikal görüntüleme, LiDAR, güvenlik, otonom sürüş ve makine görüşü gibi geniş spektral duyarlılık gerektiren uygulamalarda yetersiz performans göstermektedir. Bu tez, bu sınırlamayı aşmak amacıyla alt dalga boyu ışık tuzaklama, optik sınırlandırma, foton geri kazanımı ve hibrit malzeme entegrasyonuna dayanan dört CMOS-uyumlu piksel mimarisi önermektedir. Tüm yapılar üç boyutlu Finite-Difference Time-Domain (FDTD) yöntemiyle modellenmiş ve 3 μm kalınlığında fotodiyot içeren 2 × 2 μm Bayer desenli bir birim hücre kullanılmıştır. Optik verimlilik (OE) 400–1100 nm aralığında hesaplanmış, soğurma ve ışık hapsi davranışları güç ve alan yoğunluğu monitörleriyle analiz edilmiştir. Önerilen dört yapı; yarımküresel foton tuzaklama, Si–GaAs hibrit fotodiyodlar, metal dolgulu DTI ile ters piramit yüzey tekstürleri ve yansıtıcı altlıklarla bütünleşik SiO_2 tabanlı fotonik geometriler gibi tamamlayıcı iyileştirme mekanizmaları sunmaktadır. Sonuçlar, tüm yapıların referans arka aydınlatmalı (BSI) piksele kıyasla NIR bölgesinde belirgin iyileşme sağladığını göstermektedir. En yüksek performanslı yapı, 1100 nm'de 0.824 OE değerine ulaşarak yaklaşık %285 artış sunmaktadır. Bulgular, geometrik ve hibrit malzeme tabanlı stratejilerin silisyumun NIR bölgesindeki doğal sınırlamalarını etkili şekilde aşabildiğini doğrulamakta ve yeni nesil geniş bant CMOS görüntü sensörleri için sağlam bir temel oluşturmaktadır.

Anahtar Kelimeler: CMOS görüntü sensörü, NIR, FDTD, ışık hapsetme stratejisi

ABSTRACT

IMPROVING THE NEAR INFRARED REGION SENSITIVITY OF CMOS IMAGE SENSORS

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Silicon-based CMOS image sensors inherently exhibit low near-infrared (NIR) absorption, which limits quantum efficiency and restricts their use in applications requiring extended spectral sensitivity such as biomedical imaging, LiDAR, surveillance, autonomous navigation, and machine vision. This thesis addresses this limitation by proposing four CMOS-compatible pixel architectures designed to improve NIR performance through sub-wavelength light trapping, optical confinement, photon recycling, and hybrid material integration. The structures are analyzed using three-dimensional Finite-Difference Time-Domain (FDTD) simulations. A 2 × 2 μm Bayer-patterned unit cell with a 3 μm silicon photodiode is used consistently, and optical efficiency (OE) is evaluated over the 400–1100 nm range. Absorption and confinement behaviors are examined through power and field-intensity monitors, while a conventional backside-illuminated (BSI) CMOS pixel is used as the reference. The four proposed architectures employ complementary enhancement mechanisms, including hemispherical photon trapping, Si–GaAs hybrid photodiodes, inverted-pyramid texturing with metallic DTI, and SiO_2-based photonic structures integrated with reflective substrates. The results demonstrate that all designs significantly increase NIR sensitivity compared to the reference structure. The best-performing pixel achieves an OE of 0.824 at 1100 nm, corresponding to an approximate 285% improvement while maintaining visible-band performance. These findings confirm that geometrically engineered and hybrid-material-based strategies can effectively mitigate silicon's intrinsic absorption limitations and provide a strong foundation for developing next-generation broadband CMOS image sensors with enhanced NIR sensitivity.

Keywords: CMOS image sensor, NIR, FDTD, light trapping strategy

Dedication

This dissertation is dedicated to the memory of my beloved parents, Hikmet Yücekul and Şeref Yücekul, whose love and guidance continue to inspire me every day. I also dedicate it to my children, Mert and Berk, as an example and a keepsake for their future. And with the hope of making even the smallest contribution to humanity.

ACKNOWLEDGEMENTS

First and foremost, I would like to express my deepest gratitude to my supervisor, Prof. Dr. Mahmud Yusuf Tanrıkulu. Throughout this journey, his exceptional guidance, unwavering support, and profound insights have been invaluable. I consider it one of the greatest fortunes of my academic path to have had the opportunity to work under his supervision. His dedication to science, integrity, and generosity in sharing his knowledge have been a constant source of inspiration, and I hold him in the highest regard both as a scholar and as an individual.

I am also sincerely thankful to the members of my thesis monitoring committee, Prof. Dr. Mutlu Avcı and Amira Gürsel Tandiroviç, for their valuable time, constructive suggestions, and encouragement, which greatly contributed to the development of this thesis.

I would like to extend my heartfelt thanks to my wife, Aylin Yücekul, for her unwavering support, patience, and understanding throughout this journey. Her encouragement has been a constant source of strength.

I am also grateful to all my colleagues and friends who have contributed, directly or indirectly, to the realization of this study.

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LIST OF ABBREVIATIONS

ADC	: Analog to Digital Converter
Al	: Aluminum
APD	: Avalanche Photodiode
APS	: Active Pixel Sensor
ARC	: Anti-Reflection Coating
ARL	: Anti-Reflection Layer
BEOL	: Back-End-Of-Line
BSI	: Back Side Illumination
CC	: Conic Constant
CCD	: Charge-Coupled Device
CDS	: Correlated Double Sampling
CFA	: Color Filter Arrays
CIS	: CMOS Image Sensor
CMOS	: Complementary Metal-Oxide-Semiconductor
CMP	: Chemical-Mechanical Polishing
DCG	: Dual Conversion Gain
DR	: Dynamic Range
DTI	: Deep Trench Isolation
EQE	: External Quantum Efficiency
FDTD	: Finite-Difference Time Domain
FF	: Fill Factor
FPN	: Fixed-Pattern Noise
GaAs	: Gallium Arsenide
Ge	: Germanium
HDR	: High Dynamic Range
HD-Si	: Heavily Doped Silicon
InGaAs	: Indium Gallium Arsenide
InP	: Indium Phosphide
IPS	: Inverted Pyramid Structure

IR	: Infrared
KOH	: Potassium Hydroxide
LiDAR	: Light Detection and Ranging
NIR	: Near-Infrared
OE	: Optical Efficiency
PEC	: Perfect Electric Conductor
PML	: Perfectly Matched Layer
PPD	: Pinned Photodiode
PPS	: Passive Pixel Sensor
QE	: Quantum Efficiency
RGB	: Red Green Blue
RGGB	: Red Green Green Blue
ROC	: Radius of Curvature
ROIC	: Readout Integrated Circuit
Si	: Silicon
Si_3N_4	: Silicon Nitride
SiC	: Silicon Carbide
SiO_2	: Silicon Dioxide
SNR	: Signal-to-Noise Ratio
SWIR	: Short-Wave Infrared
TiN	: Titanium Nitride
TMAH	: Tetramethylammonium Hydroxide

LIST OF SYMBOLS

a	**:** Lateral dimension / pixel width
B	**:** Magnetic flux density
c	**:** Speed of light
cc	**:** Conic constant
d	**:** Thickness
D	**:** Dielectric displacement
E	**:** Electric field
EQE	**:** External quantum efficiency
h	**:** Height
H	**:** Magnetic field
J	**:** Current density
k	**:** Extinction coefficient
λ	**:** Wavelength
μ	**:** Permeability
n	**:** Refractive index
OE	: Optical efficiency
P	: Poynting vector
QE	: Quantum efficiency
R	: Radius of curvature
σ	: Electrical conductivity
SNR	: Signal-to-noise ratio
θ	: Incident angle

1. INTRODUCTION

1.1. Background

Light is the fundamental medium that enables humans to perceive and interpret their surroundings. In biological vision, this process begins when light from the environment enters the eye through the cornea, whose curvature initiates the focusing of incoming rays. The iris regulates the amount of light by adjusting the pupil diameter, while the crystalline lens provides fine focusing, directing the light precisely onto the retina. There, an array of photoreceptor cells converts the optical signals into electrical impulses, which are transmitted via the optic nerve to the brain, where they are processed into coherent images (Oyster, 1999).

A similar sequence occurs in modern imaging systems. Light first passes through an aperture functionally equivalent to the iris that controls illumination. Optical lenses then focus the light onto a photosensitive surface, typically an image sensor. At the sensor plane, photodetectors convert photons into electrical signals, which are subsequently processed to reconstruct a digital representation of the scene. This analogy between the human visual pathway and engineered imaging devices underscores how biological principles inspire the design and optimization of optical imaging systems (Nakamura, 2017). Figure 1.1 illustrates the analogy between the human visual pathway and modern imaging devices, showing how the eye's components correspond to the elements of an imaging system.

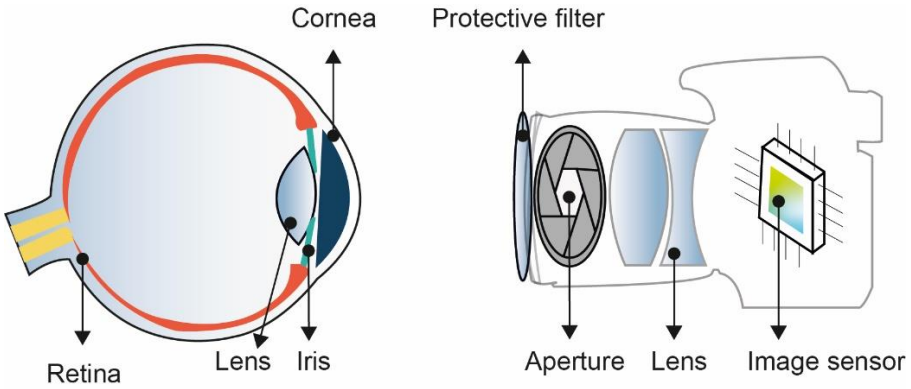

Figure 1.1. Comparison of the human visual pathway and a modern imaging chain

At the heart of modern imaging systems lie image sensors, semiconductor devices that convert incident light into electrical signals. The two primary sensor technologies, namely Charge-Coupled Devices (CCD) and Complementary Metal-Oxide-Semiconductor (CMOS) sensors, have each played a vital role in the evolution of digital imaging. While CCDs historically dominated due to their low noise and high image quality, CMOS sensors have become increasingly preferred thanks to their low power consumption, reduced manufacturing costs, and seamless integration with on-chip electronics (Bigas et al., 2006).

A CMOS image sensor consists of a matrix of pixels, each containing a photodiode that converts light into electrical charge. Unlike CCDs, CMOS sensors perform charge-to-voltage conversion at the pixel level, enabling faster readout and parallel data processing, which are key features for real-time imaging applications. However, despite continuous improvements, CMOS sensors still face limitations in specific spectral regions, particularly the Near-Infrared (NIR) band. The NIR spectral range, particularly 700 nm to 1100 nm, has become increasingly important for emerging technologies, such as autonomous driving, LiDAR (Raj et al., 2020), machine vision (Carsten Steger, Markus Ulrich, 2018; Liu et al., 2022), medical diagnostics (Heise, 2021), and surveillance systems (Kwon & Lee, 2021). However, silicon-based CMOS sensors exhibit reduced sensitivity in this region, primarily due to the lower absorption coefficient of silicon at longer wavelengths. This intrinsic material limitation restricts the performance of CMOS sensors in critical NIR applications.

This thesis focuses on addressing this limitation by proposing advanced pixel structures and optical strategies to enhance the NIR sensitivity of CMOS image sensors. Through simulation-based analysis, the study explores different design approaches, evaluates their performance using key metrics such as Optical Efficiency (OE), and provides insights for the development of high-performance sensors suitable for NIR applications.

1.2. Problem Statement and Motivation

In recent years, imaging systems have become indispensable in a wide range of technological domains, including biomedical diagnostics, autonomous vehicles, LiDAR systems, defense applications, industrial automation, and astronomical observations. Among the available sensor technologies, CMOS image sensors have gained dominance due to their low power

consumption, cost efficiency, scalability, and high level of on-chip integration. These attributes make CMOS technology the preferred choice for both consumer and high-performance imaging systems (El Gamal & Eltoukhy, 2005).

CMOS image sensors are generally responsive to wavelengths between approximately 400 nm and 1100 nm, encompassing both the visible and NIR spectral regions. In the visible spectrum (400–700 nm), the absorption characteristics of silicon allow for efficient photon-to-electron conversion, resulting in high quantum efficiency (QE). However, beyond ~700 nm, the absorption coefficient of silicon decreases sharply (Green, 2008). Figure 1.2 illustrates that crystalline silicon absorbs strongly in the visible band, but its absorption coefficient declines steeply in the near-infrared range. As photons at longer wavelengths penetrate deeper into the substrate, many pass beyond the active region of the photodiode without generating charge carriers, thereby reducing QE and overall sensor sensitivity. This sharp decrease in absorption beyond 700 nm represents a fundamental material limitation that constrains the NIR performance of silicon-based CMOS image sensors.

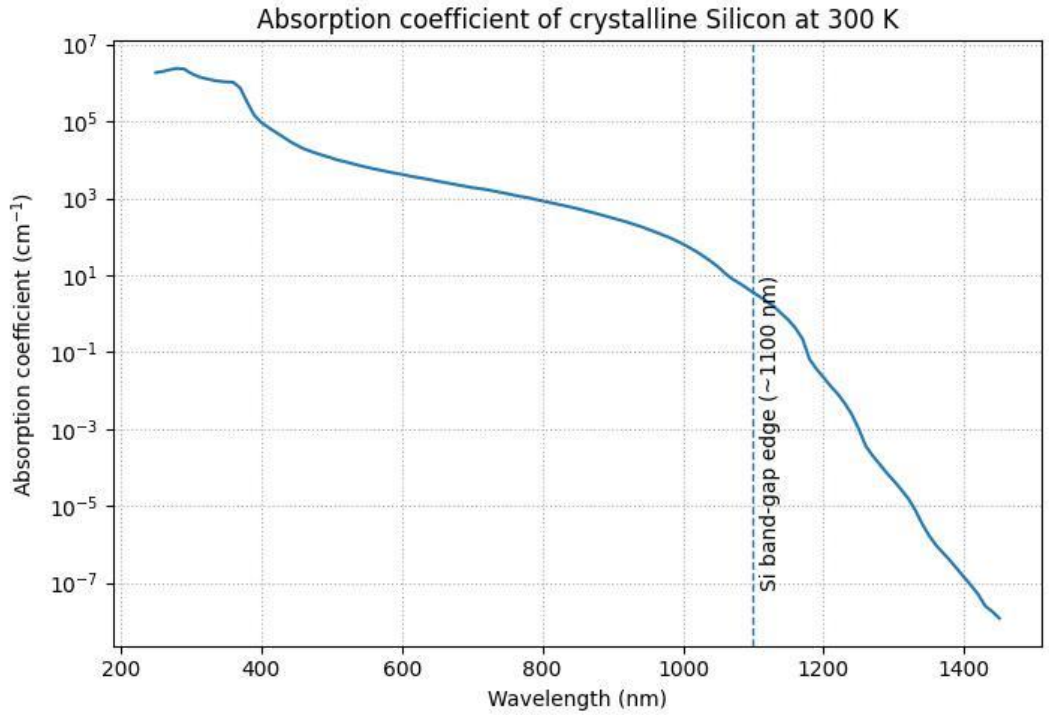

Figure 1.2. Absorption coefficient of crystalline silicon at 300 K as a function of wavelength

While this reduced NIR sensitivity may not significantly affect applications operating exclusively in the visible range, it poses a substantial limitation for NIR-dependent imaging systems. For example:

- Autonomous vehicles leverage NIR illumination to improve vision under low-light and adverse weather conditions (Zang et al., 2019).
- Biomedical imaging utilizes longer NIR wavelengths for deeper tissue penetration and enhanced contrast in non-invasive diagnostic techniques (Hong et al., 2017; Sordillo et al., 2014).
- LiDAR systems depend on efficient NIR detection for accurate depth sensing and high-resolution 3D mapping (Ito, 2021).

In all these cases, the system's performance is closely linked to the ability of the image sensor to absorb and convert NIR photons effectively.

This fundamental material limitation of silicon photodiodes necessitates the development of innovative design strategies aimed at enhancing NIR light absorption. The central objective of this thesis is to investigate and propose pixel-level structural modifications to improve the NIR sensitivity of CMOS image sensors. The study explores advanced architectures, including alternative materials and photon-trapping geometries, and evaluates their performance through comprehensive electromagnetic simulations.

The research aims to contribute to the advancement of CMOS image sensor technology by overcoming one of its fundamental limitations, thereby supporting a wide range of next-generation imaging applications that require enhanced NIR performance.

1.3. Theoretical Background

This section provides the theoretical foundation for the research, focusing on the operating principles of CMOS image sensors and their importance in modern imaging technologies. The discussion begins with the historical development of imaging technologies, highlighting the transition from optical–mechanical systems to electronic image sensors. Particular emphasis is placed on the comparative characteristics of CCD and CMOS sensors, outlining the factors that have led to CMOS becoming the dominant technology in most applications today.

Special attention is given to the physical and material limitations of silicon-based CMOS sensors in the NIR spectral range (700–1100 nm), particularly the reduced QE caused by silicon's low absorption coefficient (Green, 2008) at longer wavelengths. These limitations form the basis for the design strategies explored in this thesis, which aim to improve NIR sensitivity through advanced pixel architectures and optical enhancement techniques.

1.3.1 Evolution of Imaging Technologies

The desire to capture and preserve visual information has driven technological innovation for centuries. One of the earliest known imaging concepts was the camera obscura (Sabra, 1989). As illustrated in Figure 1.3, the camera obscura forms an inverted image through a small aperture, demonstrating the fundamental principle of light propagation and image formation. It was a darkened space with a small aperture that projected an inverted image of the outside world onto an internal surface. Although incapable of permanently recording images, it served as an important experimental tool for studying the behavior of light and the principles of perspective. The first detailed description of this device was given in the 11th century by Ibn al-Haytham (Alhazen) in his Book of Optics, a landmark work that established many of the foundations of geometrical optics (Tbakhi & Amr, 2007). The basic principle of image formation can be understood through the camera obscura, as depicted in Figure 1.3, where a small aperture projects an inverted image of the outside scene.

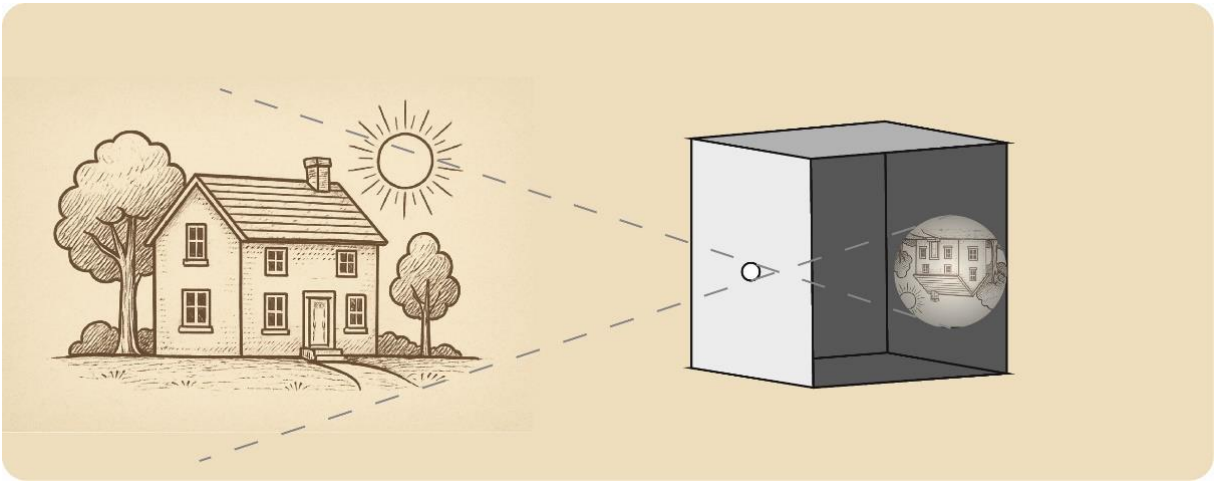

Figure 1.3. Illustrative view of inverted image formation in a camera obscura

In the early 17th century, Johannes Kepler improved the camera obscura by adding a convex lens, which increased image brightness and sharpness. He also drew parallels between the optical behavior of the camera and the human eye. Subsequent developments in optical science, such as Isaac Newton's studies of light dispersion and the invention of precision instruments like telescopes and microscopes, expanded the understanding of image formation and light behavior (Kepler & Larsen, 2025).

The 19th century marked a practical breakthrough with the invention of photography, which made it possible to permanently capture light information as images. In 1826, Joseph Nicéphore Niépce produced the first lasting photograph by exposing a bitumen-coated plate to light in a process called heliography. His method showed that light could be fixed onto a physical medium, but the images were faint and required very long exposure times. Louis Daguerre improved this approach in 1839 with the daguerreotype, which used silver-coated copper plates to create much sharper and more detailed images, reducing exposure time dramatically. Around the same period, William Henry Fox Talbot introduced the calotype, a process that used paper negatives to produce multiple positive prints, laying the foundation for modern photographic reproduction (Pavlidis, 2022). By the late 1800s, George Eastman revolutionized photography further with the invention of roll film and the Kodak camera (*History | Kodak*, n.d.). This made image capture simpler, portable, and commercially accessible, turning photography into a mass-market technology.

A major conceptual shift occurred with the rise of modern physics in the early 20th century. The works of Max Planck and Albert Einstein revealed the dual nature of light, showing that it behaves both as a wave and as discrete quanta of energy (photons). Einstein's explanation of the photoelectric effect in 1905 provided direct evidence of light's particle character and established the fundamental principle by which photons can generate electrical signals in matter (Giliberti & Lovisetti, 2024). This discovery became the cornerstone of semiconductor-based imaging devices.

Throughout the 20th century, photographic methods improved with advances in film chemistry, lens design, and camera mechanics. The emergence of color film in the 1930s and its widespread adoption by the 1960s further expanded the possibilities of visual documentation.

Yet film remained constrained by the physical limits of sensitivity, dynamic range, and processing time.

The transition to electronic imaging began in 1969 with the invention of the CCD by Willard Boyle and George E. Smith at Bell Labs (Boyle & Smith, 1970). Although originally developed as an electronic memory, Michael F. Tompsett soon demonstrated its capability for imaging, paving the way for digital photography and scientific imaging (Amelio et al., 1970). Silicon, with a bandgap well suited to absorb visible photons, became the material of choice for these devices.

By the late 20th century, CMOS image sensors emerged as an alternative to CCDs. Early CMOS devices offered lower image quality, but rapid improvements in fabrication and design made them highly competitive. CMOS technology became the preferred choice for most consumer and industrial imaging systems due to its lower power consumption, faster readout speeds, and the ability to integrate processing electronics directly onto the chip.

Today, imaging technologies are deeply embedded in daily life, from smartphones and medical devices to autonomous vehicles and space telescopes. The progression from simple optical projection to advanced digital sensors reflects a continuous pursuit of higher resolution, faster operation, and greater accessibility in visual data capture.

1.3.1.1 CCD and CMOS Image Sensors: Fundamentals and Comparison

CCD and CMOS image sensors are two fundamental technologies that form the basis of modern digital imaging systems. Both types of sensors are designed to convert light into electrical signals, but they differ significantly in their internal architectures, readout mechanisms, power consumption, and integration capabilities.

In both CCD and CMOS sensors, light is detected using a two-dimensional array of photodiodes. When light photons strike the photodiode in a pixel, they generate electrical charge through the photoelectric effect. The amount of charge generated corresponds to the intensity of the incoming light, enabling each pixel to record brightness information for image formation.

The key distinction lies in how this charge is read out:

- CCD sensors use a bucket-brigade transfer mechanism, in which charge packets are shifted across the sensor array toward a single output node. There, the charge is converted into a voltage, amplified, and digitized. This architecture yields high signal uniformity and low fixed-pattern noise, making CCDs ideal for applications requiring maximum image consistency and sensitivity, such as astronomy, microscopy, and certain scientific measurements. However, this serial transfer process is relatively slow, consumes more power, and demands precise timing control.
- CMOS sensors, by contrast, employ an Active Pixel Sensor (APS) architecture, where each pixel contains not only a photodiode but also transistors for charge-to-voltage conversion, amplification, and selection. Typical designs include 3-transistor (3T) or 4-transistor (4T) configurations, with the latter incorporating a pinned photodiode for lower noise. This arrangement allows each pixel to be addressed and read independently, enabling faster frame rates, lower power consumption, and easier integration with additional on-chip electronics such as analog-to-digital converters and image processing circuitry.

In contrast to the serial charge-transfer architecture of CCDs, CMOS sensors use a fundamentally different readout approach. Each pixel contains not only a photodiode but also additional transistors that perform charge-to-voltage conversion at the pixel level. This allows each pixel to be read independently, enabling faster image capture and lower power consumption. CMOS technology is also compatible with standard semiconductor manufacturing processes, which allows additional circuit elements such as analog-to-digital converters, timing generators, and signal processing blocks to be integrated on the same chip. This level of integration reduces the overall system size and cost while improving functionality.

Although both CCD and CMOS sensors can deliver high image quality, their architectural differences make them suitable for different applications. CCDs have traditionally been preferred in scientific imaging, astronomy, and other fields requiring high sensitivity and uniformity. CMOS sensors, on the other hand, are widely used in mobile devices, digital cameras, automotive systems, and surveillance applications due to their speed, low power consumption, and on-chip integration. The main performance metrics used to evaluate CMOS

image sensors are summarized in Table 1.1, which lists parameters such as quantum efficiency, dark current, dynamic range, and noise characteristics.

Table 1.1. Comparison of CCD and CMOS image sensors

Aspect	CCD Image Sensors	CMOS Image Sensors
Technology & Readout	Sequential charge transfer, uniform but slower	Parallel readout, faster operation
Power	Higher consumption	Lower consumption
Noise & Quality	Low noise, high uniformity	More noise, improved in modern designs
Speed	Limited frame rates	High frame rates
Integration & Cost	Specialized process, higher cost	Standard CMOS, lower cost, easy integration
Applications	Astronomy, scientific, high-end imaging	Consumer, industrial, automotive, mobile

In conclusion, CCD and CMOS sensors represent two distinct technological solutions for the same task: converting light into digital image data. Understanding their fundamental differences is essential for selecting the appropriate sensor type for a given imaging application. Both CCD and CMOS sensors share a common limitation in the NIR region due to the intrinsic absorption properties of silicon. However, the pixel-level design flexibility of CMOS sensors makes them more adaptable to structural modifications such as photon-trapping structures or alternative materials intended to enhance NIR sensitivity. This adaptability forms a key rationale for focusing on CMOS technology in the present research. The next section will explore the structure and working principles of CMOS image sensors in greater detail.

1.3.2 CMOS Image Sensors

CMOS image sensors have become a widely used imaging technology in various applications ranging from consumer electronics and automotive vision to biomedical imaging, due to their low power consumption, high integration capability, low cost, and fast readout speed. Fundamentally, CMOS image sensors are semiconductor devices designed to convert incoming light into digital signals, enabling the capture and processing of optical information. The architecture of a typical CMOS image sensor can be divided into four main functional subsystems:

1. Pixel Array

2. Analog Signal Processing Circuits
3. Row and Column Selectors (Addressing Circuitry)
4. Timing and Control Circuits

The signal flow in a CMOS image sensor is summarized in Figure 1.4, which presents the pixel array, analog processing, addressing circuits, and timing/ADC units.

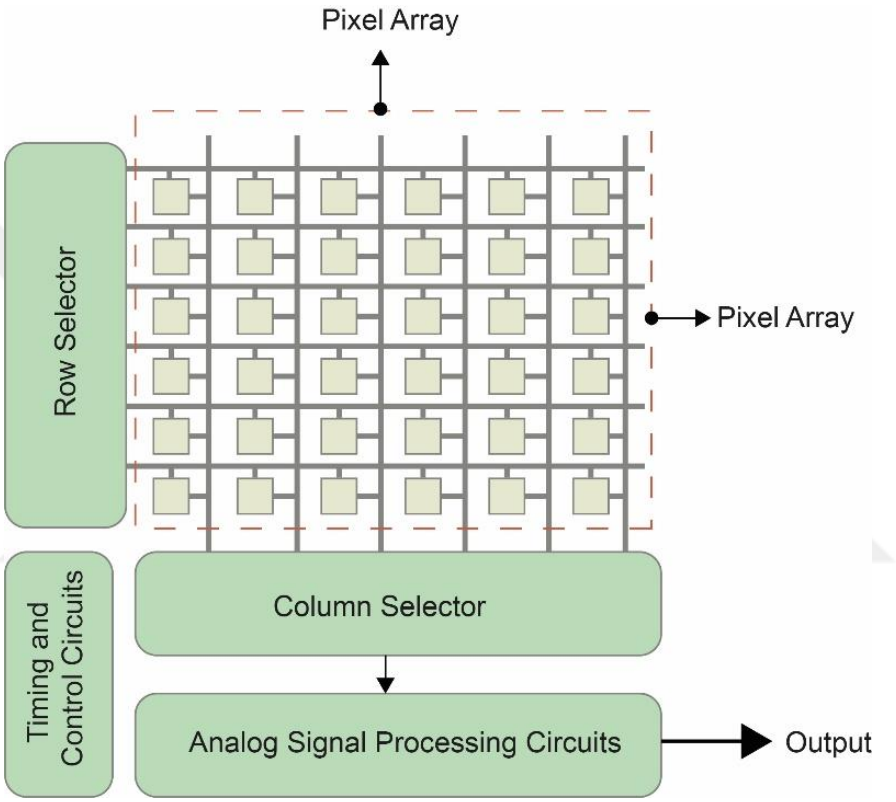

Figure 1.4. CMOS image sensor block diagram

Each of these subsystems plays a distinct role in the image acquisition pipeline, from light detection to the delivery of digital image data.

1. Pixel Array

The pixel array forms the photosensitive surface of the sensor and consists of a two-dimensional grid of pixels. Each pixel typically contains a photodiode for photon detection and associated transistors for signal readout. Incident photons generate electron–hole pairs in the photodiode through the photoelectric effect, and the resulting charge is stored until readout.

The pixel array determines both the spatial resolution (through pixel count and pitch) and the optical sensitivity of the sensor. The geometry, materials, and architecture of the pixels directly influence parameters such as noise performance and quantum efficiency. Various pixel designs such as Passive Pixel Sensors (PPS), APS, and Pinned Photodiode (PPD) structures have been developed to optimize performance for specific requirements. Detailed descriptions of these architectures are provided in the next section.

2. Analog Signal Processing

Once the charge is read out from the pixels, it passes through the analog processing stage, which conditions the signal prior to digitization. Common elements in this stage include:

- Correlated Double Sampling (CDS): Reduces reset noise and kTC noise.
- Amplifiers: Boost the signal amplitude to improve the Signal-to-Noise Ratio (SNR).
- Noise Filters: Suppress temporal noise and mitigate Fixed-Pattern Noise (FPN).

Many CMOS designs employ column-parallel processing, in which each column has a dedicated analog signal chain. This architecture enables high-speed readout by processing multiple pixel outputs simultaneously.

3. Row and Column Selectors

The addressing circuitry controls access to specific pixels during readout. The row decoder activates one row of pixels at a time, while the column multiplexer routes the output of the selected pixel to the signal processing chain. This systematic scanning typically implemented as a rolling shutter ensures efficient and orderly image capture.

4. Timing and Control

Timing and control blocks generate the precise clock and control signals required to coordinate pixel reset, exposure, charge integration, readout sequencing, and analog-to-digital conversion (ADC). In advanced CMOS designs, these circuits can be programmable, enabling multiple operating modes such as global shutter, rolling shutter, and high dynamic range (HDR) imaging.

In the context of this thesis, the pixel array is of primary interest, as the research aims to enhance the NIR sensitivity of CMOS image sensors. By introducing novel pixel structures and

photon-trapping strategies, the goal is to increase light absorption in the 700-1100 nm wavelength range and thereby improve OE without compromising visible-light performance. The proposed pixel architectures are analyzed using electromagnetic simulations, as described in the methodology chapter.

1.3.2.1 CMOS Image Sensor Pixel Structures

The pixel is the basic building block of a CMOS image sensor. It is the point where photons are converted into electrical signals, and its design directly determines the overall performance of the sensor. As requirements for higher resolution, lower noise, wider dynamic range and reduced power consumption have increased, the optimization of pixel structures has become one of the central challenges in image sensor technology.

A pixel typically contains a photodiode, which absorbs light and generates charge, together with a set of transistors that control charge integration, amplification, resetting and readout. The number, type, and configuration of these transistors, along with the photodiode structure, define the pixel architecture. This choice strongly affects sensitivity, noise characteristics, dynamic range, and power efficiency.

The evolution of CMOS pixel architectures can be understood by reviewing three main structures:

1. Passive Pixel Sensors (PPS)
2. Active Pixel Sensors (APS, 3T structure)
3. 4T Pixel with Pinned Photodiode (PPD)

The Passive Pixel Sensor is the earliest pixel design in CMOS image sensors. In this architecture, each pixel consists only of a photodiode and an access transistor. The photodiode integrates photo-generated charge during exposure, and the access transistor connects this stored charge to a column amplifier and readout circuit. Figure 1.5 shows the passive pixel sensor (PPS) design, consisting of a photodiode and a single access transistor, which provides high fill factor but suffers from poor noise performance.

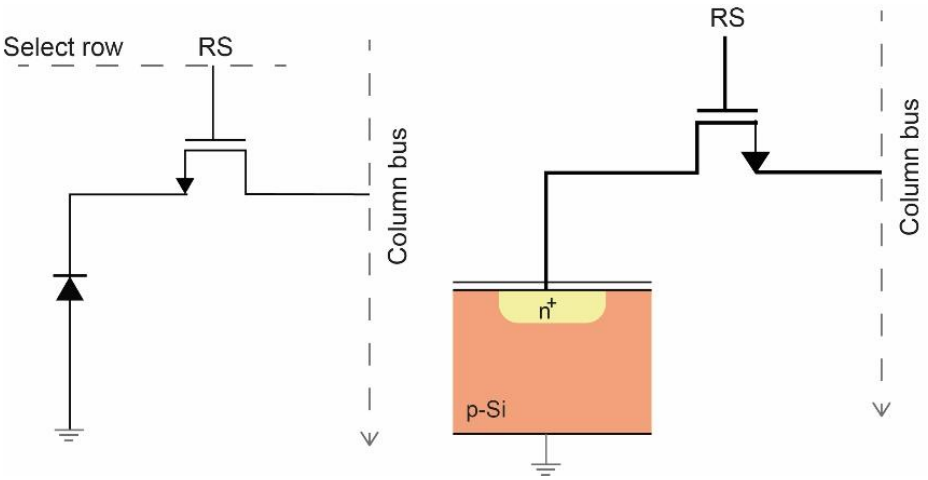

Figure 1.5. PPS structure: Pixel architecture consisting of a photodiode and an access transistor

While PPS structures are simple and offer high fill factors due to minimal in-pixel circuitry, they suffer from several drawbacks. Most notably, the lack of in-pixel amplification leads to poor noise performance and signal degradation due to parasitic capacitance and line resistance during readout. These limitations significantly restrict the scalability and signal integrity of PPS architectures, especially in high-resolution or low-light conditions.

To overcome the limitations of PPS, the APS was developed. In this design, signal amplification is integrated directly into each pixel, significantly improving performance. The most common form is the 3-Transistor (3T) pixel, which contains:

- A reset transistor (M1) to initialize the photodiode (PD),
- A source follower transistor (M2) that buffers the signal,
- A row select transistor (M3) that connects the pixel to the column readout circuit.

The integration of amplification at the pixel level increases the signal-to-noise ratio and enables faster and more reliable readout. Compared to PPS, 3T APS provides much better image quality, especially for video and high-speed applications. Nevertheless, 3T pixels still suffer from reset noise, which arises when the photodiode is reset before a new exposure. This noise limits dynamic range and degrades low-light performance. Despite these limitations, the 3T APS design was an important step toward modern high-performance CMOS sensors. The 3T active pixel structure, illustrated in Figure 1.6, integrates a reset transistor, an in-pixel amplifier, and a row-select switch, improving readout speed and signal-to-noise ratio.

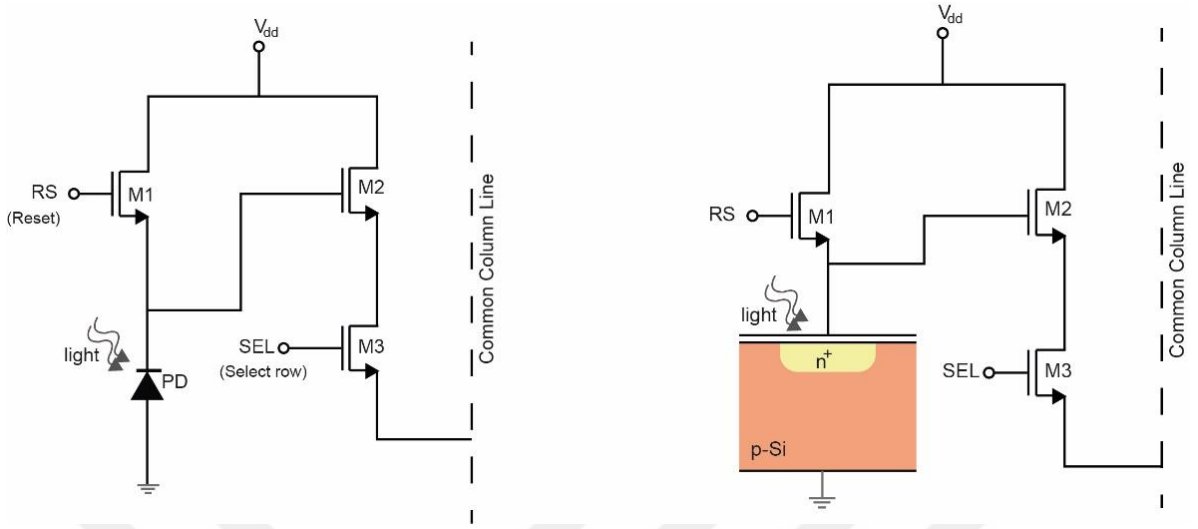

Figure 1.6. APS: Pixel design integrating a reset transistor, a source-follower amplifier, and a row-select switch

A major advancement in CMOS image sensor technology came with the development of the 4-Transistor (4T) pixel architecture combined with a Pinned Photodiode (PPD). This design added a transfer gate between the photodiode and the floating diffusion node, enabling CDS. In CDS, the pixel output is measured both before and after charge transfer. Subtracting these two values effectively cancels reset noise and reduces fixed-pattern noise.

The PPD itself is one of the most influential innovations in solid-state imaging. It was first introduced in CCD technology in the early 1980s by Nobukazu Teranishi and later adapted to CMOS image sensors in the 1990s. Earlier photodiodes suffered from two key problems: high dark current caused by surface leakage, and incomplete charge transfer that resulted in image lag. The PPD solved both issues. The concept of the PPD is based on controlling the surface potential of the photodiode. A shallow p+ layer is placed above the n-type region, which “pins” the potential at the surface. This structure suppresses unwanted surface charge generation and therefore reduces dark current significantly. At the same time, it allows nearly complete transfer of accumulated photoelectrons to the floating diffusion node, eliminating image lag. PD is the pinned photodiode that collects photo-generated charge, while FD is the floating diffusion node where the transferred charge is converted into a voltage for readout. Figure 1.7 presents the 4T pixel with a pinned photodiode, which enables correlated double sampling, reduces dark current, and eliminates image lag.

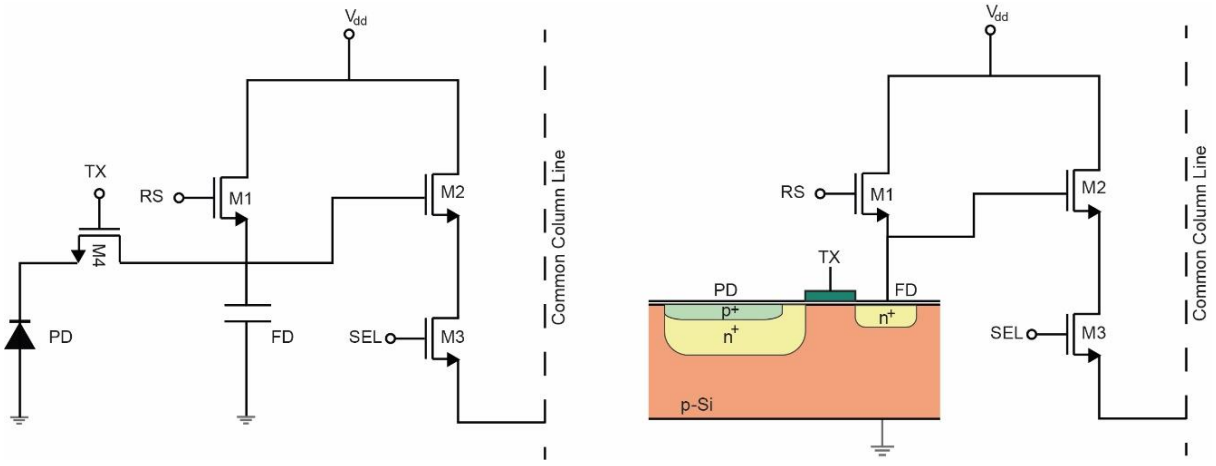

Figure 1.7. 4T Pixel with Pinned Photodiode: Pixel structure including a transfer gate and a pinned photodiode: This design supports correlated double sampling, suppresses dark current, and eliminates image lag, making it the prevailing standard in modern CMOS image sensors

The advantages of PPD pixels can be summarized as follows:

- Low dark current: Surface-generated carriers are strongly suppressed.
- Complete charge transfer: Eliminates image lag and improves temporal response.
- High quantum efficiency: Optimized doping and reduced surface recombination enhance sensitivity.
- Compatibility with low-noise readout: Enables effective correlated double sampling.

Thanks to these properties, the 4T pixel with a pinned photodiode became the dominant structure in CMOS image sensors. It is now the industry standard for almost all commercial applications (Fossum & Hondongwa, 2014). From smartphone cameras to medical devices and automotive vision systems, nearly every high-performance CMOS sensor relies on this architecture.

Beyond the mainstream pixel architectures, several specialized types have been developed to serve specific imaging requirements. For instance, 5T and 6T pixels are employed in global shutter designs to enable simultaneous integration across all pixels important in high-speed or industrial machine vision systems. Logarithmic response pixels support wide dynamic range imaging and are used in scenes with extreme brightness variations. Meanwhile, avalanche photodiode (APD)-based pixels enable single-photon detection and time-of-flight imaging, finding use in applications such as LiDAR and advanced biomedical imaging. Despite these

innovations, the PPS, 3T APS, and especially the 4T pixel with a PPD remain the dominant and most widely adopted architectures, forming the foundation of modern CMOS image sensor technology.

1.3.2.2 Key Performance Parameters in CMOS Image Sensors

The performance of a CMOS image sensor is determined by a combination of optical, electrical, and structural parameters. These metrics define the sensor's ability to capture, process, and reproduce visual information. A clear understanding of these parameters is essential for designing sensors that meet the requirements of diverse applications, ranging from scientific imaging to mobile photography and industrial automation.

This section presents the most important parameters, their definitions, and their impact on sensor optimization.

QE describes the ratio of collected photoelectrons to incident photons:

$$QE(\lambda) = \frac{N_{electrons}}{N_{photons}(\lambda)} \tag{3.1}$$

where $N_{electrons}$ is the number of generated electrons and $N_{photons}$ is the number of incident photons at wavelength λ.

Higher QE indicates better photon-to-electron conversion efficiency, resulting in improved sensitivity, especially in low-light conditions. QE depends on factors such as photodiode material, doping profile, wavelength of incident light, and optical enhancements like microlenses or anti-reflection coatings.

Fill Factor is the proportion of a pixel's area that is optically active:

$$FF = \frac{A_{photodiode}}{A_{pixel}} \tag{3.2}$$

where $A_{photodiode}$ is the photodiode's active area and A_{pixel} is the total pixel area.

In CMOS sensors, in-pixel transistors reduce FF compared to CCDs. To compensate, microlens arrays are widely used to redirect light toward the photodiode, thereby improving the effective fill factor without changing the pixel's physical design.

Dark current is the thermally generated charge that appears even in the absence of light. It is highly temperature-dependent and becomes a significant source of noise during long exposures or in low-light conditions. High dark current degrades image quality by increasing fixed-pattern noise.

Strategies for reducing dark current include:

- The use of pinned photodiodes to suppress surface leakage,
- Optimized doping and surface passivation,
- Active cooling in scientific or astronomical imaging systems.

Noise in CMOS image sensors arises from multiple sources:

- Thermal (Johnson–Nyquist) noise from resistive components,
- Shot noise due to photon arrival statistics,
- Readout noise from amplifiers and ADCs,
- Fixed-pattern noise (FPN) from pixel mismatches,
- 1/f noise dominant at low frequencies.

Noise reduction methods include Correlated Double Sampling (CDS)**,** column-parallel ADC architectures, and advanced digital post-processing techniques. Improving Signal-to-Noise Ratio (SNR) remains a central design goal in CMOS sensor development.

Dynamic Range (DR) represents the ratio between the maximum measurable signal and the minimum detectable signal above the noise floor:

$$DR = 20.\log_{10}\left(\frac{Q_{\max}}{N_{noise}}\right)[dB] \tag{3.3}$$

where is $Q_{\max}$ the maximum charge capacity of the pixel and N_{noise} is the total noise level.

A high DR enables the sensor to capture both bright and dark regions of a scene simultaneously. Techniques such as Dual Conversion Gain (DCG)**,** high-capacity photodiodes, and multiple-exposure or logarithmic-response pixels are commonly used to achieve wide dynamic range.

While QE measures photon-to-electron conversion, OE evaluates how effectively the entire pixel structure directs incident light to the photodiode.

$$OE = \frac{P_{absorbed}}{P_{incident}} \tag{3.4}$$

where is $P_{absorbed}$ the optical power reaching the photodiode and $P_{incident}$ is the total optical power incident on the pixel area. OE accounts for optical losses from metal wiring, dielectric layers, and pixel isolation structures. In this thesis, OE is used as the primary figure of merit for evaluating the proposed pixel designs in the NIR range.

Each performance metric provides a different perspective on sensor quality. Achieving superior performance requires a holistic optimization approach, balancing trade-offs between sensitivity, dynamic range, noise, and pixel density while considering the fabrication and cost constraints of the target application.

1.4. Objective of the Thesis

The rapid growth of imaging applications in fields such as medical diagnostics, security and surveillance, autonomous systems, and scientific instrumentation has created a strong demand for high-performance image sensors. In many of these areas, extending sensitivity into the NIR,

typically 700–1100 nm, is of particular importance, as NIR light provides information not accessible in the visible spectrum.

Conventional silicon-based CMOS image sensors, while offering advantages in terms of integration, power efficiency, and cost, face intrinsic challenges in the NIR range. The absorption coefficient of silicon decreases significantly at longer wavelengths, which reduces both optical efficiency and quantum efficiency. This results in a lower fraction of incident NIR photons being converted into electrical signals, ultimately limiting performance in applications that depend on reliable NIR imaging.

To overcome these limitations, researchers have explored several approaches including device material modifications, pixel architecture optimization, and advanced optical enhancement techniques. While many studies have focused on a single strategy, there remains a need for systematic investigation of combined structural and material-based solutions.

The objective of this thesis is to propose and evaluate novel CMOS pixel architectures that enhance NIR sensitivity through complementary mechanisms. Four different pixel structures are introduced and analyzed. These designs integrate light-trapping strategies that increase the effective optical path length of incoming photons, as well as material-based modifications that improve absorption efficiency in the NIR spectrum. By combining structural and material innovations, the proposed approaches aim to overcome the inherent absorption limitations of silicon while maintaining compatibility with CMOS fabrication processes.

The performance of the developed pixel architectures is assessed through detailed optical simulations using the Finite-Difference-Time-Domain (FDTD) method. This allows quantitative evaluation of their optical efficiency and quantum efficiency in the NIR, and comparison with conventional designs.

In this way, the thesis contributes both a deeper understanding of the physical and technological constraints that limit NIR performance in CMOS sensors, and a set of practical design strategies that may guide the development of future high-sensitivity imaging devices. The expected outcome is to demonstrate that innovative pixel-level engineering can significantly extend the

operational range of CMOS image sensors into the NIR domain without sacrificing manufacturability or integration potential.

1.5. Thesis Organization

This thesis is organized to guide the reader from the fundamental background of imaging science toward the detailed investigation of the proposed solutions for enhancing the NIR sensitivity of CMOS image sensors.

Chapter 1 introduces the motivation of the study, outlines the historical and theoretical foundations of imaging technologies, and states the main objectives of the research.

Chapter 2 provides a comprehensive literature review on CMOS image sensors, with a particular focus on their performance in the NIR region. Existing approaches are examined, their limitations are discussed, and the current research gaps that motivate this work are identified.

Chapter 3 presents the theoretical framework of the study. It introduces the FDTD simulation methodology and describes in detail the novel pixel architectures developed to improve NIR sensitivity.

Chapter 4 reports and analyzes the simulation results, comparing the performance of the proposed designs with conventional structures. The advantages and limitations of each design are evaluated in the context of NIR imaging requirements.

Chapter 5 concludes the thesis by summarizing the main findings, emphasizing the scientific contributions of the work, and suggesting possible directions for future research in advanced CMOS image sensor design.

2. LITERATURE REVIEW

The enhancement of NIR sensitivity in CMOS image sensors has been an active area of research due to its significance in diverse applications such as biomedical diagnostics, remote sensing, autonomous navigation, and industrial inspection. While CMOS technology offers clear advantages in terms of cost, power efficiency, and on-chip integration, its performance in the NIR spectral range is inherently constrained by the material properties of silicon and the compact nature of modern pixel architectures.

In recent years, researchers have explored a variety of approaches to overcome these limitations. These include architectural innovations such as backside illumination (BSI) and deep trench isolation (DTI) for improved light capture and reduced crosstalk, the incorporation of nanostructures and plasmonic elements for enhanced light trapping, the use of non-silicon materials with superior NIR absorption, and advanced optical stack designs to increase quantum efficiency.

This chapter reviews these advancements in detail. Section 2.1 discusses BSI optimization techniques, which have become a standard approach for improving photon capture. Section 2.2 examines DTI for crosstalk suppression in high-density pixel arrays. Sections 2.3 and 2.4 address nanostructure- and plasmonics-based light management as well as non-silicon materials for imaging. Section 2.5 focuses on light trapping structures, while Section 2.6 presents a critical assessment of the reviewed literature and identifies the research gaps that this thesis aims to address.

2.1. BSI Optimization

BSI is a key architecture for improving the OE of CMOS image sensors, especially in the NIR. In conventional front-side illuminated (FSI) structures, light must pass through several layers of metal interconnects, transistors, and insulating materials before it reaches the photodiode. These layers block part of the incident light and reduce the number of photons absorbed in the active region. As pixel sizes shrink, the share of non-sensitive area increases, which further

limits OE. This limitation is particularly critical in the NIR region, where silicon's absorption coefficient is lower and a longer optical path is required for effective photon capture.

As illustrated in Figure 2.1, BSI overcomes these problems by reversing the sensor structure so that light enters from the back surface of the silicon wafer, reaching the photodiode without passing through the front-side circuitry. This approach improves OE across both the visible and NIR wavelengths by eliminating obstructions in the optical path. It also increases the effective fill factor since the active area is no longer shadowed by front-side metal layers. In addition, BSI sensors exhibit better angular response, enabling more efficient light capture over a wider range of incidence angles, and provide superior low-light performance due to reduced optical losses and improved signal-to-noise ratio (SNR). These advantages make BSI a widely adopted architecture in high-performance imaging applications.

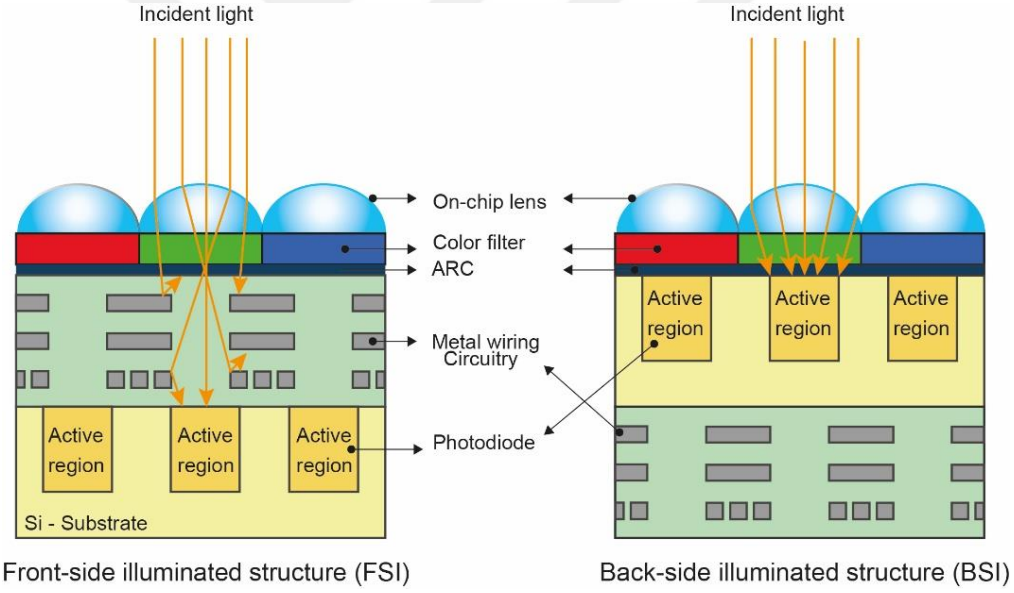

Figure 2.1. FSI and BSI comparison

Several studies have demonstrated the benefits of BSI for NIR enhancement. Lauxtermann et al. developed a high-resistivity silicon BSI CMOS image sensor with a thickness of 50 µm, achieving a dark current of 360 pA/cm² at 3.3 V reverse bias and a QE of 80% (Lauxtermann et al., 2014). Test images from their 640 × 512-pixel prototype confirmed strong NIR sensitivity. Oshiyama et al. combined a pyramid surface for diffraction (PSD) with DTI in a crystalline-silicon BSI sensor, achieving a 50% sensitivity improvement compared to a

flat-surface BSI device, and exceeding 30% QE at 850 nm in a 1.12 μm pixel of a 2-megapixel array (Oshiyama et al., 2018). Park et al. applied backside scattering technology (BST), optimized the anti-reflection layer (ARL), and adjusted the silicon thickness, achieving up to a 43% increase in infrared QE at 940 nm and analyzing optical crosstalk for various BST geometries (Park et al., 2019).

Despite its benefits, BSI introduces certain challenges. Wafer thinning can increase mechanical fragility, and the longer optical path in high-resistivity silicon may lead to crosstalk between pixels if not mitigated by isolation structures such as DTI. Uniform performance across large imaging arrays also requires precise control over backside processing steps, including anti-reflective coating deposition, surface passivation, and contamination prevention.

In this thesis, BSI is used as a foundational technology for further NIR sensitivity enhancement. The proposed pixel architectures build on the strengths of BSI and integrate CMOS-compatible light-trapping structures to further increase photon absorption in the 700–1100 nm range, while maintaining scalability and compatibility with standard fabrication processes.

2.2. Deep Trench Isolation (DTI) for Crosstalk Reduction

Modern CMOS image sensors continue to evolve through innovations aimed at enhancing sensitivity, minimizing crosstalk, and enabling smaller pixel sizes without compromising image quality. Two of the most influential advancements in this regard are BSI and DTI. These technologies are particularly important for high-resolution mobile cameras, scientific imaging, and advanced machine vision systems, where compact form factor and superior optical performance must coexist.

Crosstalk in CMOS image sensors occurs when unwanted signal coupling between adjacent pixels degrades image quality. This phenomenon can be classified into three main types:

1. Electrical crosstalk: Diffusion of photogenerated carriers across pixel boundaries, leading to charge sharing.
2. Optical crosstalk: Lateral propagation of photons within the silicon substrate before absorption.

3. Spectral crosstalk: Wavelength-dependent leakage between color channels in sensors with color filter arrays (CFA).

Deep Trench Isolation is a fabrication technique designed to mitigate crosstalk by physically separating each pixel. This is achieved by etching high-aspect-ratio trenches into the silicon substrate between adjacent pixels and filling them with dielectric or doped insulating materials. The resulting vertical barriers confine both electrical carriers and optical photons within their respective pixels.

The benefits of DTI include:

- Significant reduction of electrical crosstalk, improving signal fidelity in small pixels.
- Suppression of optical crosstalk, enabling better spatial resolution and color accuracy.
- Enhanced spectral separation in CFA-based sensors, reducing color contamination.

Several studies have validated the effectiveness of DTI in improving NIR performance. Oshiyama et al. implemented a BSI CMOS image sensor with a pyramid surface diffraction (PSD) structure combined with DTI, achieving a 50% sensitivity improvement over flat-surface devices and exceeding 30% QE at 850 nm for 1.12 μm pixels (Oshiyama et al., 2018). Yokogawa et al. demonstrated that a 400 nm pitch inverted pyramid array (IPA) integrated with DTI enhanced NIR sensitivity by ~80%, corresponding to over 30% QE at 850 nm for a 3 μm-thick c-Si photodetector (Yokogawa et al., 2017).

As illustrated in Figure 2.2, DTI forms deep, dielectric-filled trenches around each pixel, providing strong optical and electrical isolation. DTI is particularly valuable in BSI architectures, where the increased optical path length in high-resistivity silicon can amplify crosstalk effects. The combination of BSI and DTI maximizes both photon capture efficiency and pixel-level isolation, enabling high-resolution sensors (< 2 μm pixel pitch) to maintain low noise, wide dynamic range, and accurate color reproduction.

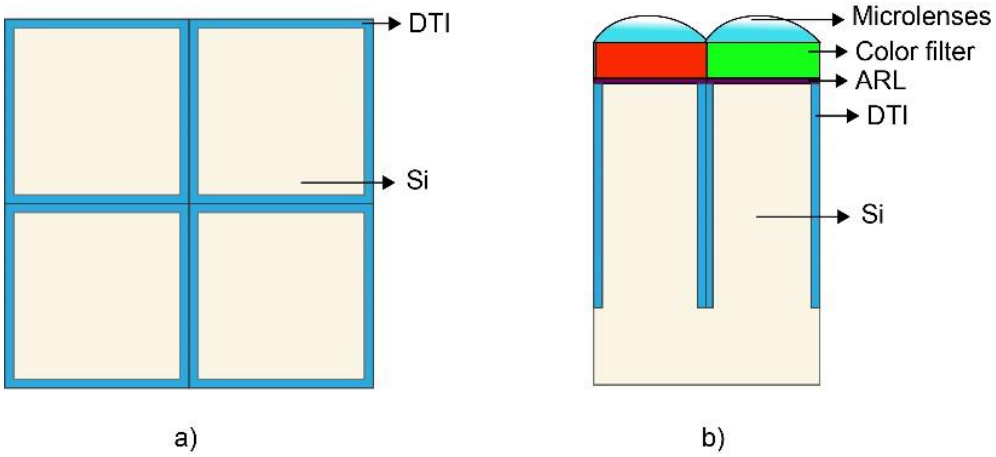

Figure 2.2. Schematic images of CMOS image sensor with DTI (a) Top view (b) Cross section view

The integration of DTI requires advanced semiconductor processing, including wafer bonding, chemical-mechanical polishing (CMP), high-aspect-ratio trench etching, and dielectric filling. While these steps add complexity and manufacturing cost, the substantial gains in sensitivity, spatial resolution, and NIR performance justify their adoption in flagship imaging systems.

In summary, DTI especially when implemented alongside BSI represents a cornerstone technology in modern CMOS image sensor design. By effectively isolating pixels both electrically and optically, DTI mitigates the inherent trade-offs between resolution, sensitivity, and crosstalk, enabling the next generation of compact, high-performance imaging systems for consumer, industrial, and scientific applications.

2.3. Nanostructures and Plasmonic Structures

The continuous scaling of pixel dimensions in CMOS image sensors, while essential for increasing resolution and reducing device footprint, imposes significant limitations on photon capture efficiency particularly in the NIR. As the active silicon layer thickness decreases and the fill factor becomes constrained by in-pixel circuitry, a substantial portion of incident photons is either reflected, scattered away, or absorbed in non-photosensitive regions. To address these losses, researchers have increasingly turned to nanostructures and plasmonic designs as advanced light management strategies.

Nanostructures refer to sub-wavelength scale surface or sub-surface patterns such as nanoholes, nanopillars, nanogratings, and metasurfaces engineered to modify the interaction between incident light and the photodetector. By inducing controlled diffraction, refraction, or scattering, these structures can increase the effective optical path length within the silicon, thereby enhancing absorption at longer wavelengths.

Plasmonic structures, on the other hand, exploit the excitation of surface plasmon resonances collective oscillations of free electrons at a metal–dielectric interface when illuminated by light of a specific wavelength. By integrating metallic nanostructures (e.g., gold or silver nanoarrays) into the pixel design, it is possible to concentrate electromagnetic energy into the underlying photodiode region, resulting in locally amplified optical fields and improved quantum efficiency.

In the context of NIR enhancement, both nanostructured and plasmonic approaches serve two critical purposes:

1. Light trapping redirecting and confining incident photons within the silicon absorption layer to increase the probability of electron–hole pair generation.
2. Spectral selectivity tailoring the device response to target wavelengths through structural resonance effects, allowing improved NIR performance without sacrificing visible-light imaging quality.

Several studies have demonstrated the effectiveness of these approaches. For instance, Devine et al. investigated nanohole arrays and micro-hole structures on CMOS pixels using FDTD simulations, achieving up to 70% NIR absorption in thin (3 μm) silicon layers (Devine et al., 2023; Ponizovskaya-Devine et al., 2022). Yoshinaga et al. demonstrated plasmonic diffraction structures capable of increasing photon confinement at 940 nm by a factor of 8.2 (Yoshinaga et al., 2022). Cobo et al. integrated polysilicon nanogrids with deep trench isolation, reporting a 33% improvement in external QE at 850 nm and a 7% reduction in crosstalk (Cobo et al., 2022). Miyamichi et al. developed plasmonic color filters with multiband transmission capability, enabling simultaneous visible and NIR imaging (Miyamichi et al., 2018). Junger et al. fabricated pixel-level plasmonic nanostructures directly on CMOS sensors, obtaining

high-quality visible images alongside enhanced NIR response without the need for separate detectors (Junger et al., 2014).

These results highlight that nanostructure and plasmonic integration is a promising and fabrication-compatible method for overcoming the inherent material limitations of silicon in the NIR range. In this thesis, such concepts are incorporated into the proposed pixel architectures in a manner that complements other enhancement techniques, such as backside illumination and deep trench isolation, to achieve superior optical efficiency between 700 and 1100 nm while maintaining compatibility with standard CMOS processes.

2.4. Non-Silicon Materials for Imaging Applications

Silicon has been the dominant material for CMOS image sensors due to its maturity in semiconductor manufacturing and cost-effectiveness. However, its relatively low absorption coefficient in the NIR range particularly beyond 700 nm limits sensitivity for applications requiring extended spectral response. To address this challenge, alternative materials with higher NIR absorption are being explored, often in hybrid architectures that combine the strengths of silicon-based readout circuits with non-silicon photodetectors.

Gallium arsenide (GaAs) is one of the most promising candidates for this purpose, owing to its direct bandgap (~1.42 eV) and high absorption efficiency in the 800–1000 nm range. In addition, GaAs offers superior electron mobility compared to silicon, enabling faster charge transport and potentially lower readout noise. Hybrid approaches typically involve bonding a thin GaAs photodiode layer to a silicon CMOS readout integrated circuit (ROIC) using techniques such as wafer bonding or flip-chip integration.

Several studies have demonstrated the potential of non-silicon integration. For example, InGaAs photodiodes have been successfully integrated with CMOS ROICs for extended NIR and short-wave infrared (SWIR) imaging, achieving high quantum efficiency in the 900–1700 nm range. Germanium (Ge) has also been explored (Chen et al., 2023) for its strong absorption up to ~1.6 μm, though lattice mismatch with silicon poses fabrication challenges that require advanced buffer-layer engineering (Ponizovskaya-Devine et al., 2022).

The integration of non-silicon materials introduces fabrication complexity, including thermal expansion mismatch management, defect reduction at the bonding interface, and optimization of antireflection coatings for broad spectral coverage. Nevertheless, the significant performance improvements in the NIR range make such hybrid approaches a compelling direction for next-generation CMOS image sensor development.

2.5. Light Trapping Structures

Light-trapping structures are widely used in CMOS image sensors to increase the optical path length of incident photons. This approach is particularly effective in the NIR region, where silicon has a low absorption coefficient. The goal is to redirect or confine light within the photosensitive region without relying on excessive substrate thickness, which can increase dark current and worsen pixel crosstalk.

Different strategies have been reported in the literature. Sub-wavelength gratings can diffract photons into guided modes. Backside texturing, such as inverted pyramids, nanocones, refracts and scatters light into oblique paths. Plasmonic or dielectric metastructures, on the other hand, concentrate the electromagnetic field near the photodiode and tailor the phase of incoming light. These methods are often combined with anti-reflection coatings and, in BSI sensors, with DTI to suppress lateral propagation between pixels.

The effectiveness of such designs has been demonstrated in numerous studies. Devine et al. showed that optimized nano- and micro-hole arrays could achieve up to ~70% NIR absorption in 3 μm-thick silicon layers (Devine et al., 2023; Devine, Qarony, et al., 2021). Yoshinaga et al. employed plasmonic diffraction to confine photons near 940 nm, reporting an 8.2-fold increase in confinement (Yoshinaga et al., 2022). Cobo et al. integrated a polysilicon nanogrid, which extended the photon path and improved external quantum efficiency (EQE) by 33% at 850 nm while reducing crosstalk by 7% (Cobo et al., 2022). Oshiyama et al. combined a pyramid-diffraction surface with DTI in a BSI sensor, obtaining a 50% sensitivity gain over flat-surface devices and more than 30% QE at 850 nm for 1.12 μm pixels (Yoshinaga et al., 2022). Park et al. further enhanced performance through backside scattering, optimized anti-reflection layers, and silicon thickness tuning, achieving a 43% QE improvement at 940 nm (Park et al., 2019). Junger et al. fabricated plasmonic nanostructures directly on CMOS

pixels, demonstrating both high-quality visible imaging and enhanced NIR response (Junger et al., 2014).

Despite their benefits, light-trapping designs involve trade-offs. Angular dependence may narrow the enhancement bandwidth, while fabrication limits can restrict feature size and aspect ratio. Increased lateral light propagation also requires careful isolation to prevent crosstalk. Nonetheless, when optimized alongside BSI optics, passivation, and DTI, light-trapping structures remain among the most effective and fabrication-realistic methods for overcoming silicon's intrinsic NIR limitations. They also form a core part of the simulation-driven designs developed in this thesis.

2.6. Critical Assessment and Research Gap

The literature review highlights significant progress in enhancing the NIR sensitivity of CMOS image sensors. BSI has reduced front-side optical losses, DTI has improved pixel-level isolation, and various nanostructures have been used to trap light and extend the optical path within silicon. In addition, alternative absorber materials such as Ge, InGaAs, and GaAs have been investigated to improve QE beyond the visible range. These efforts demonstrate that the fundamental limitations of silicon in the NIR region can be alleviated through architectural and material innovations.

Nevertheless, important gaps remain. Most prior studies have concentrated on a single enhancement strategy for example, a specific nanostructure, a plasmonic layer, or a hybrid material without proposing an integrated design that combines photon collection, absorption efficiency, and pixel isolation in a CMOS-compatible and scalable manner. Furthermore, demonstrations of non-silicon absorber integration are rare, and those reported often face challenges of fabrication complexity and limited compatibility with standard CMOS processes. Light-trapping approaches, while effective, have largely relied on conventional textures or periodic geometries, with limited exploration of three-dimensional structures that can simultaneously suppress reflection, redistribute light, and enhance NIR absorption.

This thesis directly addresses these gaps by following two complementary innovation paths. First, it proposes a GaAs–Si hybrid CMOS pixel architecture aimed at enhancing NIR

absorption in the 800–1000 nm range. While the design concept draws on integration techniques reported for heterogeneous photodetectors, its compatibility with CMOS readout circuits is considered at a conceptual level within the scope of this thesis. Second, it introduces a hemispherical photon-trapping design combined with refractive sub-surface geometries to reduce Fresnel reflections and increase the effective photon path length. Both strategies are integrated with DTI to suppress optical and electrical crosstalk, thereby preserving spatial resolution in the modeled structures.

By combining advanced light-trapping concepts with non-silicon absorber materials in a unified framework, this research moves beyond the fragmented approaches found in the literature. The outcome is a comprehensive and CMOS-compatible strategy for developing high-performance NIR image sensors that can address demanding applications in biomedical imaging, machine vision, autonomous systems, and scientific instrumentation.

3. MATERIALS AND METHODS

The physical nature of light has long been one of the most fundamental and debated questions in science (Raftopoulos et al., 2005). Early theories alternated between a particle-based description, such as Newton's corpuscular theory (Raftopoulos et al., 2005; Shapiro, 1980), and a wave-based explanation, such as Huygens' wave theory (Arnold, 2004; Belger et al., 1997; Junger et al., 2014; Kuehn, 2016). The true dual character of light was gradually revealed through pivotal experiments and theoretical advances during the 19th and 20th centuries (Raftopoulos et al., 2005).

In Thomas Young's double-slit experiment (1801), monochromatic light passing through two narrow slits produced an interference pattern of alternating bright and dark fringes (Gittinger, 2017). This phenomenon can only be explained if light propagates as a coherent wave capable of constructive and destructive interference. The far-field intensity distribution is expressed as:

$$I(\theta) = I_0 \cos^2\left(\frac{\pi d \sin\theta}{\lambda}\right) \tag{3.5}$$

where d is the slit separation, λ is the wavelength, and θ is the observation angle. This experiment provided one of the earliest pieces of quantitative evidence that light behaves as a wave, laying the foundation for the later development of wave optics.

In contrast, Arthur Compton's scattering experiment (1923) demonstrated the particle-like nature of light (Compton, 1923, 1929). When high-energy X-ray photons collided with nearly free electrons, the interaction resulted in a measurable wavelength shift due to the conservation of momentum and energy. This phenomenon, known as the Compton effect, provided direct proof that photons carry momentum. High-energy photons colliding with electrons exhibited momentum transfer, producing a measurable wavelength shift:

$$\Delta\lambda = \lambda' - \lambda = \frac{h}{m_e c}(1 - \cos\theta) \tag{3.6}$$

where h is the Planck's constant, m_e is the electron rest mass, c is the speed of light, and θ is the scattering angle (Williams et al., 1998). This effect could not be explained by classical wave theory, confirming the quantization of light into photons.

Louis de Broglie (1924) unified these perspectives by proposing wave–particle duality, assigning a wavelength to all matter according to :

$$\lambda = \frac{h}{p} \tag{3.7}$$

where p denotes the linear momentum of the particle. For photons, this relation reduces to $\lambda = c/\nu$, where ν denotes the photon frequency, thereby linking the particle's momentum to its wave nature through Planck's constant.

Albert Einstein's theory of the photoelectric effect (1905) established the direct role of photons in exciting electrons (Giliberti & Lovisetti, 2024; Klassen, 2009). A photon of frequency ν carries an energy

$$E_{photon} = h\nu = \frac{hc}{\lambda} \tag{3.8}$$

which can excite an electron across a potential barrier if $E_{photon} \geq \Phi$, where Φ is the material's work function. The maximum kinetic energy of the emitted electron is therefore

$$E_k = h\nu - \phi \tag{3.9}$$

providing one of the earliest confirmations of energy quantization in light–matter interactions.

In semiconductors, the relevant threshold is the bandgap energy E_g. Photons with $h\nu \geq E_g$ excite electrons from the valence band to the conduction band, generating electron–hole pairs. This process underpins the photoelectric conversion mechanism used in modern CMOS image sensors. The Fermi level E_F represents the probability of electron occupancy within the energy bands; optical excitation effectively modifies the carrier distribution around this level (Kahn, 2015; Mead & Spitzer, 1964). At the device level, the conversion of absorbed photons into measurable charge is quantified by the external quantum efficiency (EQE):

$$EQE(\lambda) = \frac{N_{e^-}(\lambda)}{N_{photon}(\lambda)} \tag{3.10}$$

where N_{e^-} is the number of collected photoelectrons and $N_{photons}$ the number of incident photons. The resulting photocurrent is expressed as

$$I_{ph}(\lambda) = q \cdot \phi(\lambda) \cdot EQE(\lambda) \tag{3.11}$$

with q the elementary charge and $\Phi(\lambda)$ denotes the incident photon flux. Thus, the number of absorbed photons directly determines the photoelectric conversion and ultimately the sensor's responsivity.

Although photons exhibit quantized energy (photoelectric effect) and particle-like interactions at high energies, light propagation inside micro and nano-structured pixel geometries is dominated by wave phenomena such as diffraction, interference, and near-field scattering. Therefore, this thesis treats light as an electromagnetic wave for propagation and scattering modeling, while using absorption (photon capture) results to infer photoelectric conversion. These foundations demonstrate that absorption, carrier excitation, and charge collection are governed by dual nature of light and its electromagnetic interaction with matter. For accurate modeling of image sensors, particularly at sub-wavelength scales relevant to modern CMOS pixels, light must be treated not as simple geometric rays but as a continuous electromagnetic

field governed by Maxwell's equations. This provides the conceptual bridge to the electromagnetic theory and numerical methods presented in the following sections.

The design and optimization of CMOS image sensor pixels, particularly for enhanced NIR sensitivity, require a precise and comprehensive optical simulation methodology (Han et al., 2020). While ray-tracing techniques are useful at macroscopic scales, they fail to adequately model diffraction, interference, and near-field scattering that become dominant at the micro and nano-scale dimensions of advanced pixel architectures (Crocherie et al., 2008). To overcome these limitations and accurately model light behavior within such complex geometries, this study employs a full-wave electromagnetic approach based on Maxwell's equations, solved numerically using the FDTD method (Crocherie et al., 2008). This framework enables quantitative prediction of photon propagation, absorption, and optical crosstalk across various pixel architectures, including both conventional silicon and hybrid structures.

3.1. Electromagnetic Wave Theory and Maxwell's Equations

Light, including both visible and NIR wavelengths, is an electromagnetic wave consisting of oscillating electric (E) and magnetic (H) fields that propagate in mutually perpendicular directions. The fundamental behavior of electromagnetic waves in materials is described by Maxwell's equations, which couple time-varying electric and magnetic fields and enable the prediction of light propagation, reflection, refraction, and interaction with matter. In differential form, Maxwell's four equations are expressed as:

Gauss's law for electricity:

$$\nabla . D = \rho_e \tag{3.12}$$

Gauss's law for magnetism:

$$\nabla . B = 0 \tag{3.13}$$

Faraday's law for induction:

$$\nabla xE = -\frac{\partial B}{\partial t} \tag{3.14}$$

Ampere-Maxwell law:

$$\nabla xH = \frac{\partial D}{\partial t} + J_e \tag{3.15}$$

where D is the dielectric displacement, ρ_e is the volumetric charge density, B is the magnetic flux density, E is the electric field, H is the magnetic field and J is the current density. For linear and isotropic materials there is the following relationship between D and B, E and H:

$$D = \varepsilon_0 E + P \tag{3.16}$$

$$D = \varepsilon_m \varepsilon_0 E \tag{3.17}$$

$$B = \mu_m \mu_0 H = \mu_0 H \tag{3.18}$$

$$J = \sigma E \tag{3.19}$$

where ϵ, μ, and σ represent the permittivity, permeability, and conductivity of the medium, respectively. Together, these equations demonstrate that electromagnetic waves are self-sustaining oscillations of electric and magnetic fields, capable of propagating through dielectric and semiconductor media without the need for a material carrier. In the context of CMOS image sensors, they form the physical foundation for modeling how photons interact with multilayer dielectric stacks, metallic interconnects, and sub-wavelength nanostructures.

Analytical solutions to Maxwell's equations exist only for idealized geometries, such as plane waves, parallel plates, or simple resonant cavities. However, realistic pixel architectures involve complex three-dimensional layouts, heterogeneous materials, and strong field coupling between layers. Under these conditions, numerical methods are indispensable for accurately resolving the propagation, scattering, and absorption of light within the sensor structure.

3.2. Finite-Difference Time-Domain (FDTD) Method

Given the computational complexity of solving Maxwell's equations analytically for realistic three-dimensional pixel geometries, numerical methods are indispensable. FDTD method, first introduced by Yee in 1966, provides a powerful numerical framework for solving Maxwell's curl equations in the time domain (Kane Yee, 1966). The method discretizes both space and time, replacing differential operators with finite differences. The computational domain is divided into a grid of Yee cells, within which the electric (E) and magnetic (H) field components are calculated at staggered spatial positions and time steps. This leapfrog updating scheme ensures numerical stability and accurately captures the coupled evolution of E and H, as illustrated in Figure 3.1.

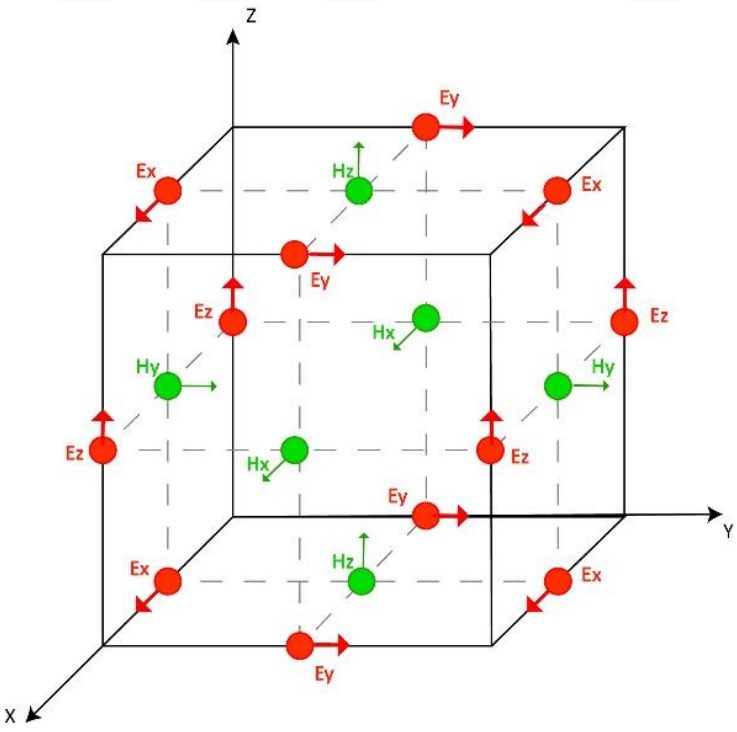

Figure 3.1. Schematic of the Yee cell

The discrete form of Maxwell's curl equations in the Yee lattice can be expressed as

$$\nabla \times E = -\mu \frac{\partial H}{\partial t}, \qquad \nabla \times H = \varepsilon \frac{\partial E}{\partial t} + \sigma E \tag{3.20}$$

These curl equations are discretized in space and time using central difference approximations. For example, the *x*-component of the electric field at grid point *(i,j,k)* and time step *n* is updated as:

$$E_x^{n+1}(i,j,k) = E_x^n(i,j,k) + \frac{\Delta t}{\varepsilon(i,j,k)}\left[\left(\frac{H_z^{n+\frac{1}{2}}(i,j,k) - H_z^{n+\frac{1}{2}}(i,j-1,k)}{\Delta y}\right) - \left(\frac{H_y^{n+\frac{1}{2}}(i,j,k) - H_y^{n+\frac{1}{2}}(i,j,k-1)}{\Delta z}\right)\right] \tag{3.21}$$

Similarly, the *y* and *z*-components of the electric field are computed in terms of spatial differences of the magnetic field. The magnetic field components are then updated in a staggered fashion ("leapfrog scheme"), for example:

$$H_x^{n+\frac{1}{2}}(i,j,k) = H_x^{n-\frac{1}{2}}(i,j,k) - \frac{\Delta t}{\mu(i,j,k)}\left[\left(\frac{E_z^n(i,j+1,k) - E_z^n(i,j,k)}{\Delta y}\right) - \left(\frac{E_y^n(i,j,k+1) - E_y^n(i,j,k)}{\Delta z}\right)\right] \tag{3.22}$$

This iterative scheme ensures that electric and magnetic fields propagate consistently in time, capturing wave propagation, diffraction, interference, and absorption phenomena at sub-wavelength resolution. FDTD discretizes both space and time, transforming the differential equations into finite difference equations solvable through iterative time-stepping.

In this work, simulations are conducted using Ansys Lumerical FDTD (*Ansys Lumerical FDTD Simulation of Photonic Components*, 2023), which provides robust implementations of the Yee algorithm and advanced boundary condition handling. The simulation setup includes:

- Mesh resolution: A non-uniform grid is applied, with 1–2 nm fine mesh in critical regions such as the silicon absorption layer and nanostructured interfaces, and coarser mesh elsewhere for efficiency.

- Boundary conditions: Perfectly Matched Layers (PML) are placed at the top and bottom boundaries to absorb outgoing waves without reflection. Bloch (periodic) boundaries are applied in the lateral directions (x, y) to emulate an infinite pixel array.
- Excitation source: A broadband plane wave spanning 400–1100 nm is used, allowing analysis of both visible and NIR response in a single simulation.
- Material models: Dispersive and wavelength-dependent material data are incorporated, using experimentally validated refractive index (n) and extinction coefficient (k) values for silicon, GaAs, SiO_2, and metals.

By iteratively updating the field components according to the discretized curl equations, the FDTD algorithm reveals the propagation, scattering, and absorption of light within each pixel structure, forming the computational foundation for the optical performance analysis in this thesis.

3.3. Simulation Domain and Proposed Pixel Structures

This study employs the FDTD method implemented in ANSYS Lumerical FDTD Solutions to investigate the optical performance of various pixel structures designed for enhanced NIR sensitivity in CMOS image sensors. The simulation approach has been structured to accurately represent real-world pixel behavior while maintaining computational efficiency. A broadband plane-wave source covering the 400-1100 nm wavelength range is used to illuminate the simulation domain. The simulated region represents a unit pixel cell based on a simplified Bayer filter configuration, as illustrated in Figure 3.2.

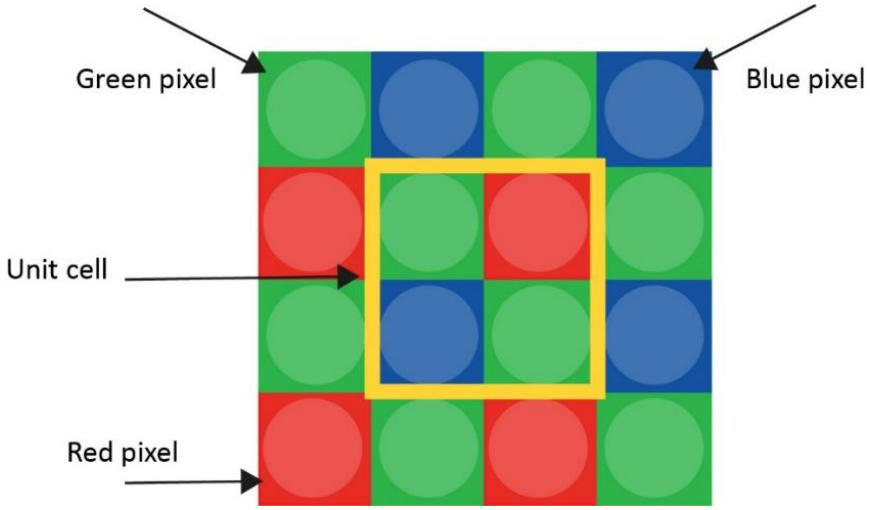

Figure 3.2. Top view of a unit pixel of a CMOS image sensor with a Bayer pattern

This assumption allows periodic tiling and analysis of individual pixel performance under uniform illumination conditions. The silicon layer, which serves as the photodiode and is responsible for photon absorption, is assigned a mesh override to ensure fine spatial resolution and higher numerical accuracy in the critical absorption region. To accurately simulate light interaction within the pixel, Bloch boundary conditions are applied along the x and y axes, assuming periodicity in the lateral directions. In the z-direction, Perfectly Matched Layers (PML) are used to absorb outgoing waves and eliminate artificial reflections.

Frequency-domain field and power monitors are placed at three key locations: near the input (light source), at the entrance of the silicon layer, near the exit of the silicon layer. These monitors allow precise tracking of the electromagnetic field behavior and the calculation of optical efficiency based on the transmitted power. The Poynting vector (**P**, unit: W/m^2), defined as the cross product of the electric (**E**) and magnetic (**H**) fields, represents the energy flux and is used to calculate the transmitted power as shown in Equation 3.23:

$$\vec{P} = \frac{1}{2}\oint\!\!\oint (\vec{E} \times \vec{H}) \cdot d\vec{A} \tag{3.23}$$

The optical efficiency is then calculated as the ratio of optical power absorbed within the active silicon (or hybrid) layer to the incident optical power (Han et al., 2020). Since recombination effects are not explicitly modeled, OE is considered directly proportional to the external QE,

making it the primary performance metric in this study. All investigated pixel configurations follow a BSI design, a structure favored for its high light collection efficiency. Metal contacts and interconnects beneath the silicon are not modeled in this study, as their influence on light absorption is considered negligible. The OE is calculated as:

$$OE = \frac{Absorbed\ \ power}{Source\ \ power} = \frac{P_{\text{in } Si} - P_{out\ Si}}{P_{Source}} \tag{3.24}$$

The study compares multiple structural variations:

- A flat baseline structure (flat reference pixel)
- Three light-trapping structures featuring geometric modifications to enhance absorption
- One hybrid structure, integrating an alternative semiconductor material with the silicon layer

The optical efficiency values obtained from simulations are used to evaluate and compare the performance of the proposed structures. Since quantum efficiency is linearly proportional to optical efficiency in the absence of recombination and reflection losses, optical efficiency serves as the primary performance metric.

The simulation domain reproduces the cross-sectional geometry of a single CMOS image sensor pixel, including:

- Silicon substrate and active layer
- Passivation and dielectric layers
- Microlens and color filter structures
- Nano or micro-scale light trapping structures positioned beneath or within the pixel

Monitors are strategically placed at multiple planes:

- Incident plane: To normalize input power.
- Silicon entry plane: To capture transmitted power entering the active layer.
- Silicon exit plane: To assess transmitted or absorbed power within the pixel.

Through this simulation framework, spatial and spectral optical responses are obtained, enabling quantitative comparison among the proposed structures and providing insights into their NIR sensitivity enhancement mechanisms.

3.3.1 Reference Flat Structure

All performance comparisons of the proposed pixel architectures are carried out relative to a flat reference structure, which represents the fundamental layout of a BSI CMOS image sensor without any additional light-trapping or hybrid modifications. This baseline design serves as the foundation for all subsequent geometrical enhancements investigated in this study. For each configuration, geometric and material optimizations were performed to maximize optical performance under identical illumination conditions.

Figure 3.3 illustrates the view of the flat structure.

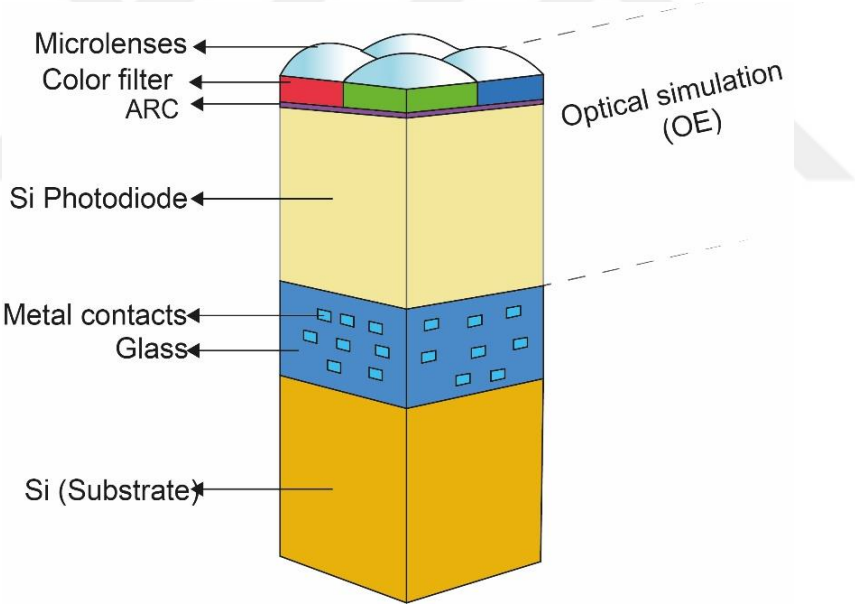

Figure 3.3. Perspective view of flat structure

In this configuration, the pixel size is defined as 2×2 μm², and the photodiode region, composed of silicon, has a thickness of 3 μm. A 70 nm anti-reflective coating (ARC) made of silicon nitride (Si_3N_4) is placed directly above the silicon layer to minimize surface reflection and enhance light transmission into the active region.

An RGB color filter layer, designed using colored glass-like material, is positioned on top of the ARC. This filter layer is 0.6 μm thick and replicates the Bayer pattern configuration. In order to analyze the optical behavior of the color filter array in the flat structure, the wavelength-dependent refractive index (n) and extinction coefficient (k) were considered. For each filter material (Red, Green, and Blue), the dispersion curves of Re and Im as functions of wavelength were obtained. The dispersion characteristics of the blue, green, and red filters are shown in Figure 3.4, Figure 3.5, and Figure 3.6, respectively.

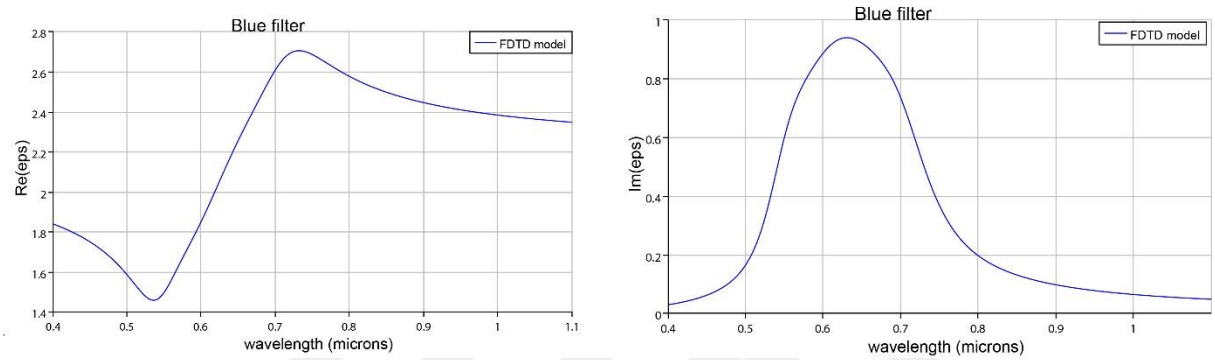

Figure 3.4. Blue color filter's refractive indexes (Re(eps)) and absorption coefficients (Im(eps))

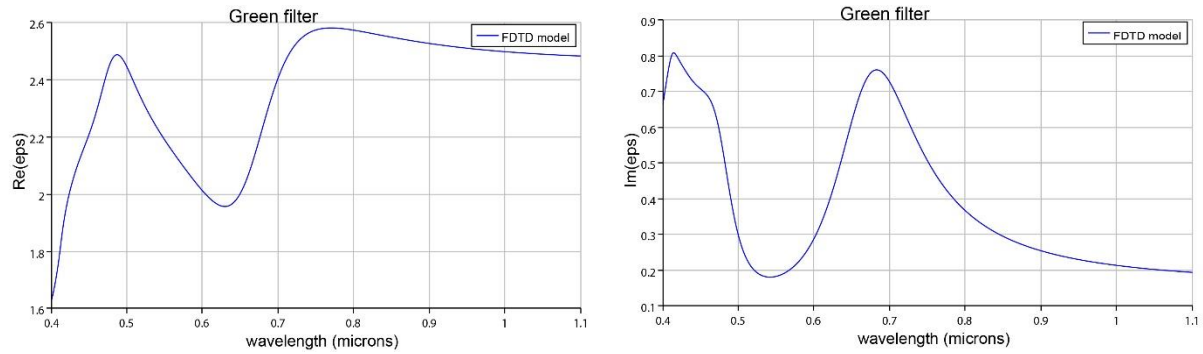

Figure 3.5. Green color filter's refractive indexes (Re(eps)) and absorption coefficients (Im(eps))

These parameters directly determine how the filter transmits or absorbs incident light in the visible spectrum, and therefore play a crucial role in defining the overall spectral response of the CMOS image sensor.

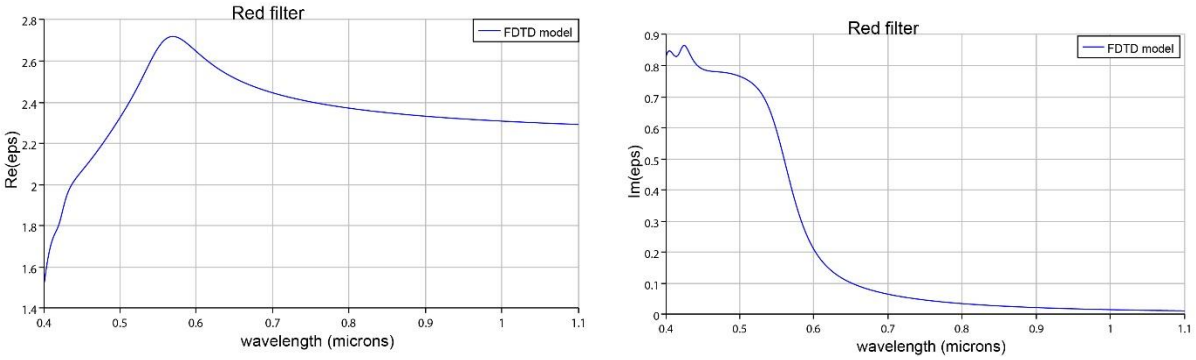

Figure 3.6. Red color filter's refractive indexes (Re(eps)) and absorption coefficients (Im(eps))

Above the color filter array (CFA), a microlens made of silicon dioxide (SiO_2) is incorporated to concentrate incoming light toward the underlying filter and active region. The microlens has a radius of curvature (ROC) of 2 µm and a thickness of 0.5 µm. The structural details of each component are summarized in Table 3.1.

Table 3.1. Structural and material properties of the flat reference pixel

Layer	Material	Width	Thickness	Radius of Curvature
Photodiode	Silicon	2×2 µm²	3 µm	–
AR Coating	Silicon Nitride	2×2 µm²	70 nm	–
Color Filter	Colored Glass	2×2 µm²	0.6 µm	–
Microlens	Silicon Dioxide	–	0.5 µm	2 µm

Simulations are performed using a unit cell comprising a 2×2 pixel array, arranged in a standard Bayer filter pattern (RGGB), enabling periodic tiling and accurate representation of array-level optical behavior under uniform illumination.

3.3.2 Structure-1

The first proposed design, hereafter referred to as Structure-1, introduces two major modifications to the flat reference pixel in order to enhance NIR sensitivity and suppress optical crosstalk between neighboring pixels. The first modification is the incorporation of DTI, implemented as vertical SiO_2 trenches positioned between adjacent pixels. These trenches, each 150 nm wide and 2 µm deep, extend through a significant portion of the photodiode region.

They act as optical barriers that prevent lateral photon propagation, thereby confining the optical signal within its corresponding pixel and reducing inter-pixel interference.

The second modification is the introduction of a hemispherical light-trapping structure, implemented from SiO_2 and located directly above the active silicon region. This hemispherical element, with a 250 nm radius and 1 μm vertical thickness, acts as a refractive lens. It redirects incident light into oblique paths, increasing the effective optical path length within the silicon to enhance NIR photon absorption. A schematic representation of Structure-1 is shown in Figure 3.7.

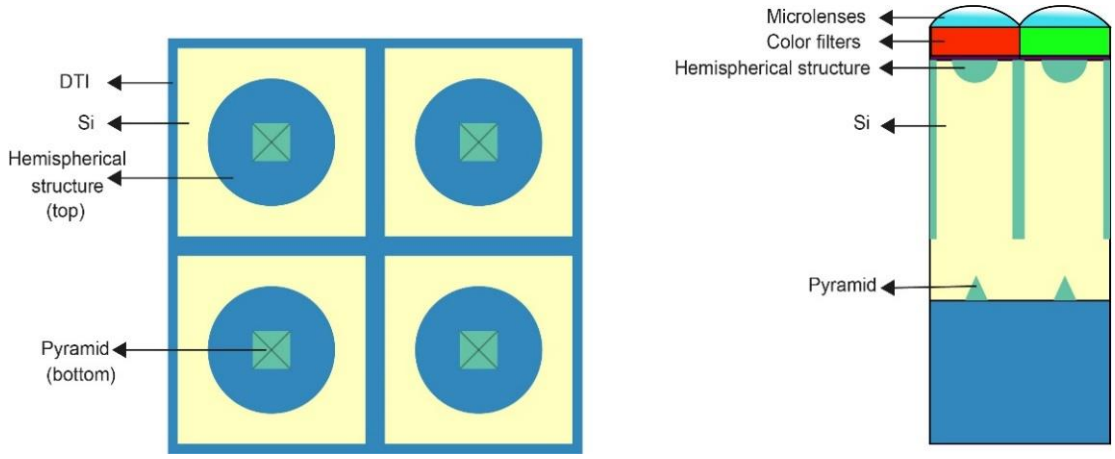

Figure 3.7. Schematic images of the designed structure: (a) Top view of the Structure-1 (b) cross-section of the Structure-1

To further improve light confinement, a pyramidal diffraction element is positioned at the bottom interface of the silicon layer. This SiO_2-based pyramid, with a height of 0.5 μm, is designed to scatter unabsorbed photons back toward the active region, effectively recycling incident light that would otherwise escape. The combined effect of the DTI, hemispherical, and pyramidal structures serves to confine light, reduce optical losses, and extend the photon-silicon interaction time, particularly in the NIR spectral range. The material and dimensional parameters of Structure-1 are summarized in Table 3.2.

Table 3.2. Structural and material parameters of Structure-1 pixel

					NIR structure		
	Photodiode	**ARL**	**Filter**	**Microlens**	**DTI**	**Hemisphere**	**Pyramid**
Material	Silicon	Si_3N_4	Colored Glass	SiO_2	SiO_2	SiO_2	SiO_2
Width	2x2 µm	2x2 µm	2x2 µm	-	150 nm	-	0.5 µm
Thickness	3 µm	70 nm	0.6 µm	0.5 µm	-	1 µm	-
Depth	3 µm	70 nm	0.6 µm	0.5 µm	2 µm	-	0.5 µm
Radius	-	-	-	ROC=2 µ cc=-1	-	250 nm	-

Collectively, these structural enhancements are expected to reduce optical losses, mitigate inter-pixel interference, and extend the photon–silicon interaction length, particularly in the near-infrared spectral range.

3.3.3 Structure-2

In the NIR spectral range, one of the primary challenges in CMOS image sensor design is to increase the amount of light absorbed within the photodiode layer, thereby improving photoelectric conversion efficiency. Previous studies have investigated three principal strategies to achieve this goal. The first relies on increasing the thickness of the silicon photodiode to extend the absorption depth (Cobo et al., 2022; Devine, Qarony, et al., 2021; Lauxtermann et al., 2014; Liu et al., 2022; Lu, 2022). The second focuses on light-trapping mechanisms that elongate the optical path length of incident photons through surface or sub-surface modifications (Teranishi et al., 2022; Yokogawa et al., 2017; Yoshinaga et al., 2022). The third explores the integration of alternative semiconductor materials with superior NIR absorption compared to silicon (Chen et al., 2023; Ponizovskaya-Devine et al., 2022). Figure 3.8 presents the schematic layout of Structure-2, showing both the top view and cross-section.

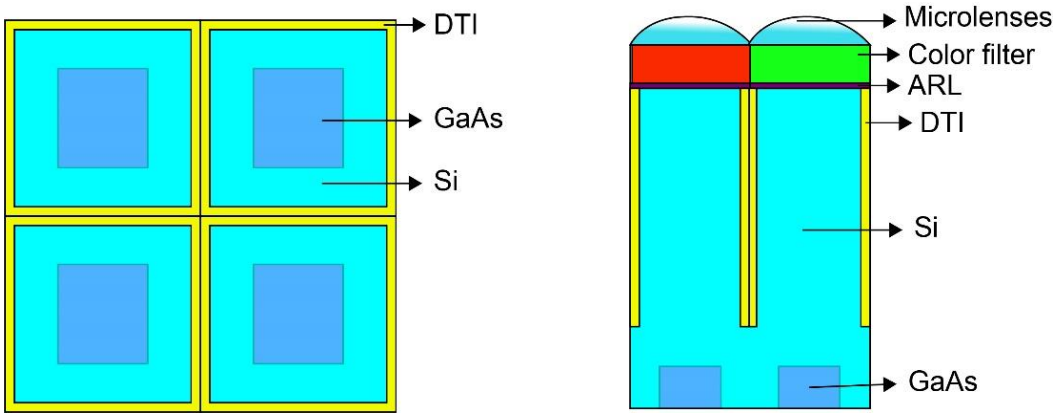

Figure 3.8. Schematic images of the designed structure-2: (a) Top view of the structure-2 (b) cross-section of the structure-2

Structure-2 has been designed based on this third approach. In this configuration, a gallium arsenide (GaAs) sub-layer is integrated beneath the silicon photodiode. GaAs, with its direct bandgap of approximately 1.42 eV and strong absorption in the 800–1000 nm wavelength range, serves as an efficient NIR absorber that complementing the weaker long-wavelength absorption of silicon. The GaAs region is patterned as a 1.5 × 1.5 μm^2 area with a 1 µm thickness, positioned directly below the silicon photodiode to enhance overall photon-to-electron conversion efficiency. Figure 3.9 provides a three-dimensional perspective view of Structure-2.

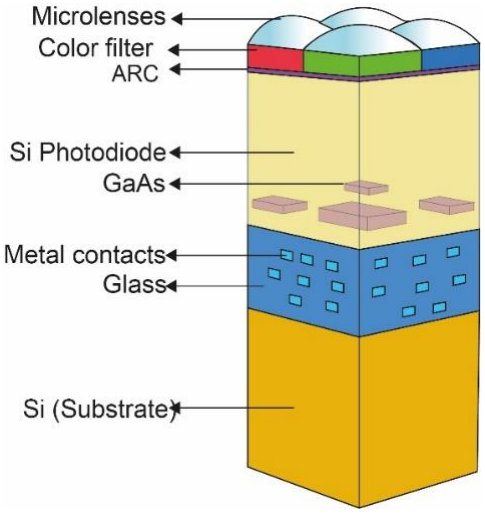

Figure 3.9. Perspective view of Structure-2

To further mitigate inter-pixel optical interference, DTI structures are incorporated. These SiO_2-filled trenches, 150 nm wide and 2 μm deep, surround each pixel and serve as vertical optical barriers that suppress lateral photon propagation. The inclusion of DTI ensures that the improved NIR sensitivity provided by the GaAs sub-layer is not degraded by optical crosstalk, thereby maintaining spatial resolution and image sharpness. The material and geometric parameters of Structure-2 are listed in Table 3.3.

Table 3.3. Structural and material parameters of Structure-2 pixel

					NIR structure	
	Photodiode	**ARL**	**Filter**	**Microlens**	**DTI**	**Semiconductor**
Material	Silicon	Si_3N_4	Colored Glass	SiO_2	SiO_2	GaAs
Width	2x2 μm	2x2 μm	2x2 μm	-	150 nm	1.5x1.5 μm
Thickness	3 μm	70 nm	0.6 μm	0.5 μm	-	1 μm
Depth	3 μm	70 nm	0.6 μm	0.5 μm	2 μm	-
Radius	-	-	-	ROC=2 μ cc=-1	-	-

This hybrid Si–GaAs configuration effectively exploits the direct bandgap absorption of GaAs to extend the near-infrared sensitivity while preserving pixel-level isolation through DTI. Although the present study focuses on the Si–GaAs combination, future research may explore alternative semiconductor integrations such as indium gallium arsenide (InGaAs), silicon carbide (SiC), or indium phosphide (InP) to further broaden the spectral response and evaluate their compatibility with standard CMOS fabrication processes.

3.3.4 Structure-3

Structure-3 introduces an inverted pyramid surface texture on the silicon photodiode, designed to improve light trapping and thereby enhance absorption in the NIR range (800–1100 nm). The central objective of this configuration is to increase the effective optical path length of incident photons, enabling stronger absorption without the need for excessively thick silicon layers, which could otherwise increase dark current or fabrication cost.

The inverted pyramids are patterned directly on the top surface of the silicon layer. Each pyramid has a lateral dimension of 0.9 × 0.9 μm and a depth of approximately 0.566 μm, consistent with geometries achievable through anisotropic wet etching processes. This etching technique exploits the crystallographic anisotropy of silicon, where the {100} planes etch at a faster rate than the more stable {111} planes in alkaline solutions such as KOH or TMAH. As a result, the inclined {111} planes naturally form the sidewalls of the pyramids, producing a characteristic angle of 54.74° between the (100) wafer surface and the (111) facets. The chosen lateral dimension and depth of the pyramids are therefore not arbitrary but are geometrically constrained by the tangent of this angle, ensuring process compatibility and reproducibility. This periodic texture facilitates multiple internal reflections and redirects photons into oblique paths, thereby prolonging their interaction within the silicon absorber. To further enhance light coupling, a 70-nm-thick silicon nitride (Si_3N_4) anti-reflection layer (ARL) is deposited above the textured surface.

A color filter array (CFA) is incorporated above the ARL to enable spectral band selection. Since experimental refractive index data for the filter glass was unavailable, a Lorentz oscillator model from the simulation library was employed to approximate its dispersive optical properties. A microlens is placed on top of the filter, with a radius of curvature (ROC) of 2 μm and a conic constant (cc) of –1, focusing incoming radiation onto the active region and improving photon throughput. Table 3.4 summarizes the material and geometric parameters of Structure-3.

Table 3.4. Structural and material parameters of Structure-3 pixel

					NIR structure	
	Photodiode	**ARL**	**Filter**	**Microlens**	**DTI**	**Inverted Pyramid**
Material	Silicon	Si_3N_4	Colored Glass	SiO_2	Aluminum	SiO_2
Width	2x2 μm	2x2 μm	2x2 μm	-	150 nm	0.9x0.9 μm
Thickness	3 μm	70 nm	0.6 μm	0.5 μm	-	0.566 μm
Depth	3 μm	70 nm	0.6 μm	0.5 μm	2 μm	-
Radius	-	-	-	ROC=2 μ cc=-1	-	-

To minimize optical crosstalk between adjacent pixels, DTI structures are included. These trenches are 150 nm wide and extend 2 μm into the silicon, and are filled with aluminum to act

as both optical and electrical barriers. In addition, the inclusion of a thin SiO_2 layer at the bottom of the structure reflects transmitted photons back into the silicon layer, creating multiple absorption opportunities and thereby further boosting quantum efficiency. Figure 3.10 presents the schematic layout of Structure-3, including the top view and the cross-section.

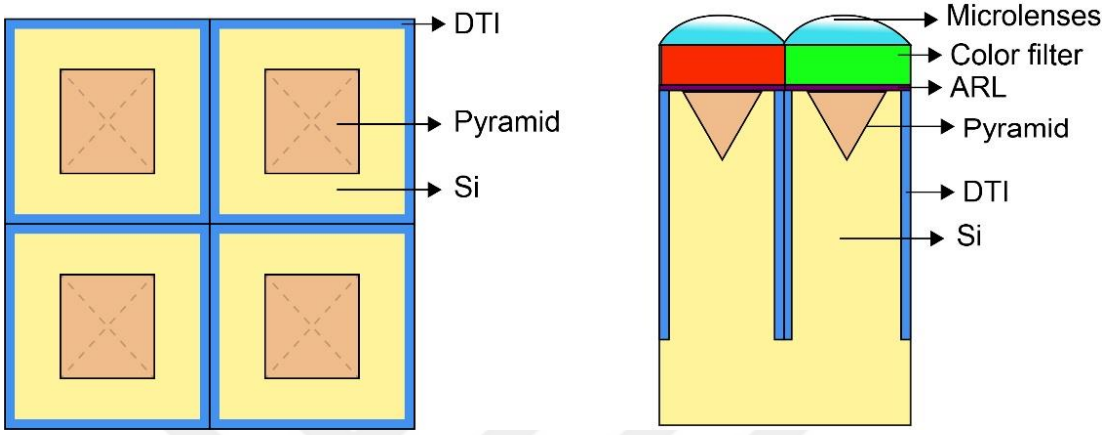

Figure 3.10. Schematic images of the designed Structure-3: (a) Top view of the Structure-3 (b) cross-section of the Structure-3

DTI trenches are modeled as metal-filled to emulate strong lateral reflection and optical isolation in NIR; this choice is used purely for optical performance benchmarking and will be discussed as an upper-bound configuration with electrical mitigations in the Results & Discussion section.

During simulations, fine mesh refinement was applied around the pyramid edges to resolve near-field scattering effects with high accuracy. Subsequent optimization steps will explore variations in pyramid geometry and ARL thickness to maximize absorption across the NIR spectral band.

Overall, the inverted pyramid texture effectively increases photon confinement within the silicon layer, while the aluminum-filled DTI structures preserve pixel-to-pixel isolation. When combined with the microlens focusing and bottom SiO_2 reflection, these design features create a compact yet highly efficient pixel architecture. This structure demonstrates strong potential for next-generation CMOS image sensors requiring enhanced NIR sensitivity without sacrificing spatial resolution or manufacturability.

3.3.5 Structure-4

To further enhance the NIR sensitivity of CMOS image sensors, Structure-4 was developed as a multi-layered design that integrates several complementary light-management strategies within a single pixel architecture. The goal of this approach is to simultaneously increase the effective optical path length, improve lateral confinement of light, and boost photon absorption in the 800–1100 nm spectral window, where the absorption coefficient of silicon is intrinsically low.

Figure 3.11 illustrates the schematic layout of Structure-4, including its top view and cross-section.

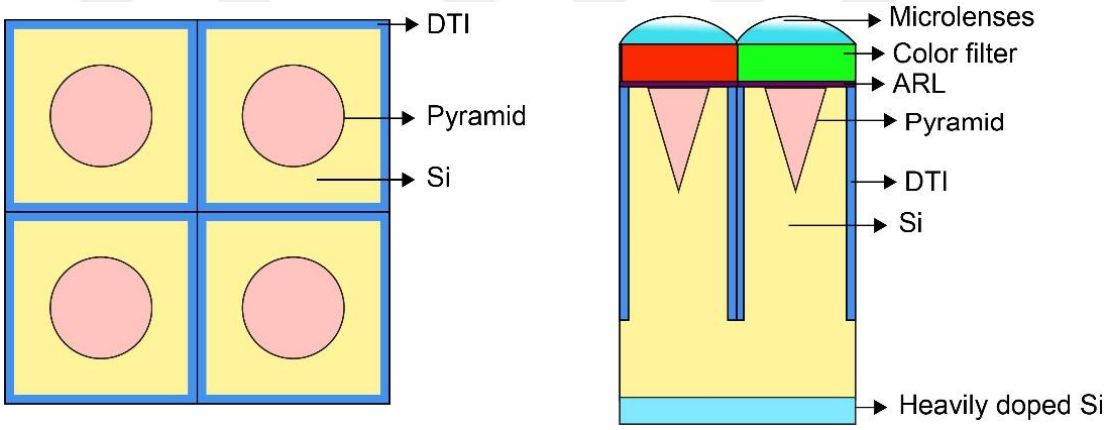

Figure 3.11. Schematic images of the designed Structure-4: (a) Top view of the Structure-4 (b) cross-section of the Structure-4

A silicon dioxide (SiO_2) inverted cone structure was introduced beneath the color filter layer. The tapered geometry of this feature promotes lateral scattering of incident photons, redistributing them into oblique trajectories inside the silicon photodiode. By lengthening the effective optical paths, this structure increases the probability of photon absorption without requiring additional substrate thickness.

Table 3.5 summarizes the material and geometric parameters of Structure-4.

Table 3.5. Structural and material parameters of Structure-4 pixel

						NIR structure		
	Photodiode	**ARL**	**Filter**	**Glass**	**Microlens**	**DTI**	**Inverted Cone**	**heavily doped Si**
Material	Silicon	Silicon Nitride	Filters	Silicon dioxide	Silicon dioxide	PEC	Silicon dioxide	Silicon dioxide
Width	2x2 µm	2x2 µm	2x2 µm	2 µm	-	150 nm	-	2 µm
Thickness	3 µm	70 nm	0.6 µm	2 µm	0.5 µm	-	-	0.3 µm
Depth	3 µm	70 nm	0.6 µm	2 µm	0.5 µm	2 µm	1 µm	-
Radius	-	-	-		ROC=2 µ cc=-1	-	Theta:75; 2 µm	-

Beneath the intrinsic silicon layer, a heavily doped silicon region with a thickness of approximately 300 nm was incorporated. The presence of this layer is motivated by concepts derived from metamaterial absorbers, in which carrier-rich layers act as auxiliary absorption zones. In the present design, the heavily doped region captures photons that penetrate through the intrinsic photodiode, effectively recycling light that would otherwise escape.

To suppress pixel-to-pixel interference, Perfect Electric Conductor (PEC) DTI barriers were implemented between adjacent pixels. Unlike conventional oxide-filled trenches, PEC boundaries provide stronger confinement of the optical field, preventing lateral photon leakage and thereby reducing optical crosstalk. This feature is particularly beneficial in densely packed pixel arrays, where maintaining spatial fidelity is essential for high-resolution imaging.

At the bottom of the stack, a 2 µm thick SiO_2 substrate was included as a reflective layer. This dielectric layer functions as a back reflector, redirecting transmitted photons upward into the active silicon region and providing multiple absorption opportunities. By coupling with the cone-induced scattering and the doped absorption layer, this substrate ensures more efficient utilization of the incident optical energy.

DTI trenches are modeled as PEC-filled in the optical simulations to emulate ideal reflection and complete lateral optical isolation. This assumption provides an optical upper bound, while electrical feasibility and mitigation strategies (e.g., dielectric-lined metal cores or all-dielectric reflective trenches) are discussed in the Results & Discussion chapter.

Collectively, the design combines lateral light scattering, additional absorption mechanisms, and strong optical isolation to maximize near-infrared sensitivity. Preliminary FDTD simulations confirm that Structure-4 exhibits a marked increase in optical efficiency and quantum efficiency relative to the baseline and earlier proposed architectures, underscoring its potential as a scalable solution for next-generation CMOS image sensors.

3.3.6 Limitations and Practical Considerations of Metal-Filled DTI

The optical simulations presented in this study demonstrate that aluminum-filled and PEC-modeled DTI can substantially enhance the NIR optical efficiency of CMOS pixels. These results highlight the strong optical confinement and photon redirection that reflective trench boundaries provide, particularly when combined with surface texturing and bottom reflectors. However, it is important to clearly define the scope and limitations of these results to prevent misinterpretation.

First, the simulations performed here are purely optical: they solve Maxwell's equations to capture light propagation, scattering, reflection, and absorption. Consequently, the DTI regions defined as aluminum or PEC act exclusively as optical media with wavelength-dependent refractive indices (Al) or as ideal reflectors without loss (PEC). The electrical consequences of placing metals in direct contact with silicon such as shorting, parasitic junction formation, and increased dark current are not considered in these models.

In practical CMOS fabrication, DTIs cannot consist of bare metal directly adjacent to the photodiode. Instead, a dielectric liner (e.g., SiO_2 or SiN) must be deposited between the silicon and the metal to ensure electrical isolation and to prevent recombination at the trench sidewalls. Furthermore, while PEC simulations provide an optimistic optical upper bound, real metals like aluminum introduce finite absorption losses. Some portion of incident NIR light is therefore dissipated as heat within the trench metal rather than being redirected into the active region.

Despite these limitations, the optical-only results remain highly valuable. They quantify the potential benefit of reflective trench boundaries and establish performance bounds: PEC results define the theoretical maximum, while Al results indicate achievable trends when realistic dispersive metal properties are included. The performance gap between these two cases

provides quantitative insight into the trade-off between enhanced optical confinement and parasitic absorption.

For comprehensive device-level validation, future studies should include (i) dielectric liners in the optical model, (ii) coupled opto-electrical simulations that link absorbed photon distributions to carrier generation, transport, and recombination, and (iii) experimental verification through fabricated test structures. Such an approach will clarify how much of the simulated NIR gain can be translated into real sensor performance without compromising dark current, fill factor, or fabrication compatibility.

In summary, the results presented here represent optical feasibility studies rather than complete device-level predictions. By explicitly distinguishing optical advantages from electrical constraints, this work establishes a realistic yet forward-looking framework for integrating reflective trench designs into next-generation NIR-sensitive CMOS image sensors.

3.4. Evaluations and Performance Parameters

The performance of the proposed pixel architectures was systematically evaluated using simulation-based metrics directly relevant to NIR sensitivity. To ensure both accuracy and reproducibility, the evaluation framework consisted of three main components: numerical validation, performance quantification, and comparative benchmarking. Convergence testing was performed to confirm the stability of the FDTD simulations. The spatial mesh was progressively refined until variations in calculated optical efficiency were below 1%. Similarly, the temporal resolution was adjusted to satisfy the Courant stability condition, ensuring that numerical artifacts did not distort the results. Boundary condition robustness was verified by repeating simulations with increased perfectly matched layer (PML) thickness and extended simulation domains.

The optical efficiency of each structure was calculated from the ratio of transmitted optical power into the active silicon region to the incident optical power, based on the Poynting vector formalism. QE was inferred under the assumption of negligible recombination losses, allowing a direct link between simulated absorption and photoelectric conversion. Additional parameters considered include:

- Spectral absorption profile: wavelength-dependent OE and QE between 400–1100 nm.
- Crosstalk analysis: lateral propagation of optical fields across pixel boundaries, quantified by integrating power flow into adjacent regions.
- Angular response: absorption efficiency as a function of incident angle, representing realistic imaging conditions.
- Material contribution: comparative role of Si, GaAs, and doped silicon in total absorption.

To assess the validity of the proposed designs, simulation results were compared against representative studies from the literature (Devine, Ahamed, et al., 2021; Yoshinaga et al., 2022). Agreement in spectral trends and enhancement factors confirmed that the models are consistent with established findings. Performance improvements obtained in this work were then analyzed relative to the baseline flat CMOS pixel design, providing a clear measure of structural benefits.

Through this multi-level evaluation strategy, the study not only verifies the correctness of the simulation framework but also provides a quantitative basis for identifying the most effective pixel architectures for enhanced NIR sensitivity. These results ultimately form the foundation for the design guidelines and recommendations presented in the concluding chapter.

4. RESULTS AND DISCUSSION

This chapter presents and discusses the optical simulation results for four pixel architectures specifically designed to enhance NIR sensitivity in CMOS image sensors. The simulations combine full-wave electromagnetic modeling and quantitative optical efficiency evaluation to assess how structural modifications influence photon absorption, confinement, and propagation at the pixel level.

All simulations were performed using the FDTD method implemented in ANSYS Lumerical, which numerically solves Maxwell's equations in the time domain. This approach enables accurate modeling of light–matter interactions in sub-micron-scale features, capturing diffraction, interference, and scattering phenomena that dominate in the NIR range (800-1100 nm).

The analysis focuses primarily on optical efficiency, defined as the ratio of optical power absorbed within the silicon photodiode to the incident power on the pixel surface. Simulations were conducted for the 400–1100 nm wavelength range, covering both visible and near-infrared bands, and repeated for Red, Green, and Blue color channels to account for the spectral filtering effect of the color filter array.

The simulation workflow consisted of the following steps:

- Accurate modeling of each pixel geometry and material dispersion (Si, GaAs, SiO_2, Si_3N_4, and metallic layers).
- Broadband plane-wave excitation under normal incidence to emulate realistic illumination conditions.
- Power monitor placement to record absorbed and transmitted fields in the active region.
- Extraction and visualization of field distributions to interpret photon confinement and optical pathways.

A conventional flat pixel was used as the reference structure, representing a standard BSI CMOS configuration without light-trapping features. The performance of the four proposed

architectures was then compared against this baseline to quantify relative improvements in the NIR band.

Results are presented as spectral optical efficiency curves (OE vs wavelength), supported by power density maps illustrating light propagation within each structure. Comparative plots and summary tables provide a concise overview of the optical gains achieved by each design, emphasizing the mechanisms responsible for enhanced NIR absorption and reduced optical crosstalk.

Collectively, this chapter bridges the theoretical framework established in Chapter 3 with the quantitative performance assessment of the proposed designs, laying the foundation for subsequent optimization and practical considerations.

4.1. Simulation Setup and Optical Efficiency Calculations

All electromagnetic simulations in this study were carried out using the ANSYS Lumerical FDTD Solutions software, which is widely used for analyzing light–matter interactions in nanoscale photonic devices. The primary goal of the simulations was to evaluate the optical efficiency of different CMOS pixel architectures, since OE directly influences QE and thus the overall sensitivity of image sensors in both the visible and NIR spectral regions.

The simulation domain was defined as a unit pixel cell with lateral dimensions of 2×2 μm², representing a single pixel within a periodic array. A typical RGGB Bayer pattern was modeled to ensure realistic color filtering and to maintain spectral completeness during analysis. The photodiode region consisted of a 3 μm-thick silicon layer, with additional layers such as the microlens, color filter, and anti-reflection coating (ARL) included depending on the structure under investigation.

The excitation source was modeled as a broadband plane wave incident normal to the pixel surface (–z direction). The spectral range of the source was set to 400–1100 nm, covering both the visible and NIR bands. The light source was positioned above the microlens to capture realistic focusing and coupling effects into the underlying active region.

Appropriate boundary conditions were applied to emulate the behavior of an infinite pixel array. Periodic boundaries were assigned along the x- and y-directions, while Perfectly Matched Layers (PML) were implemented along the z-direction to absorb outgoing fields and suppress spurious reflections. The computational mesh was adaptively refined, achieving 1–2 nm resolution in critical regions such as the silicon absorber and nanostructured interfaces, while coarser meshing was used elsewhere to optimize computational resources.

The OE was defined as the fraction of incident optical power absorbed by the photodiode. This was calculated using the Poynting vector (**S**), which represents the time-averaged energy flux of the electromagnetic field:

$$S = \frac{1}{2}\Re\left\{E \times H^{*}\right\} \tag{3.25}$$

where E and H are the complex electric and magnetic field vectors, and * denotes the complex conjugate. The absorbed optical power within the silicon region was computed by integrating the normal component of the Poynting vector over the surface enclosing the photodiode:

$$P_{abs} = \iint_{A} S \cdot \vec{n}\, dA \tag{3.26}$$

where A is the surface enclosing the silicon volume and $\hat{n}$ is the outward unit normal vector. The OE was then expressed as:

$$OE(\lambda) = \frac{P_{abs}(\lambda)}{P_{inc}(\lambda)} \tag{3.27}$$

where $P_{inc}(\lambda)$ denotes the incident optical power at wavelength λ. This procedure was repeated across the entire spectral range for red, green, and blue sub-pixels, enabling wavelength-resolved characterization of absorption performance.

The spatial mesh was iteratively refined until the variation in computed OE was below 1 % between successive refinements to ensure numerical accuracy and convergence. The Courant stability condition was also satisfied for all time-step selections. Field monitors were placed at three key planes just above the microlens (input normalization), at the silicon entry plane, and at the silicon exit plane to verify energy balance and to visualize internal power flow.

This simulation framework establishes a rigorous and reproducible basis for quantifying the optical behavior of each pixel structure. The wavelength-dependent optical efficiencies derived here constitute the foundation for the comparative performance analysis presented in the subsequent sections.

4.2. Performance Results and Analysis

This section presents the OE results obtained for the four proposed CMOS pixel architectures, each designed to improve NIR sensitivity through distinct structural modifications. All simulations were conducted under identical boundary, source, and material conditions to ensure strict comparability among the designs. The photodiode thickness was fixed at 3 μm, the excitation source was a broadband plane wave spanning 400–1100 nm, and periodic boundary conditions were applied along the lateral directions to emulate an infinite pixel array.

For each architecture, the OE spectrum was computed across the full visible-to-NIR range using power monitors positioned at the silicon entry and exit planes. Particular emphasis was placed on the 800–1100 nm region, where the intrinsic absorption coefficient of silicon declines sharply, making efficient light trapping and photon confinement essential for maintaining detector sensitivity.

The evaluation is organized in two stages. First, the performance of each individual structure is examined in detail, highlighting the specific optical mechanisms such as scattering, hybrid absorption, or confinement that contribute to NIR enhancement. These results are compared against the baseline flat pixel to demonstrate the relative gains achieved by each modification.

Second, a comparative discussion across all four designs is provided. This step identifies which strategies deliver the most substantial improvements in NIR optical efficiency while

maintaining stable performance in the visible spectrum. The combined findings allow a clear assessment of the trade-offs and advantages associated with each architectural approach. Collectively, these analyses form the foundation for the following subsections, which detail the wavelength-dependent optical behavior and internal field distributions of each proposed structure (Structure-1 through Structure-4).

4.2.1 Structure-1 Performance Analysis

Structure-1 is designed to improve NIR sensitivity by combining three main optical features: a hemispherical light-scattering layer above the photodiode, DTI for lateral optical confinement, and a pyramidal reflective structure below the silicon. These components work together to trap and redirect photons, especially those at longer wavelengths, increasing the chance of absorption within the active region.

The optical efficiency of Structure-1 was calculated for blue, green, and red pixels over the wavelength range of 400 nm to 1100 nm. The same simulation settings were used for both Structure-1 and a reference flat CMOS pixel, including a 3 μm silicon thickness, periodic boundary conditions, and broadband illumination. Figure 4.1 compares the OE values of Structure-1 with the flat structure.

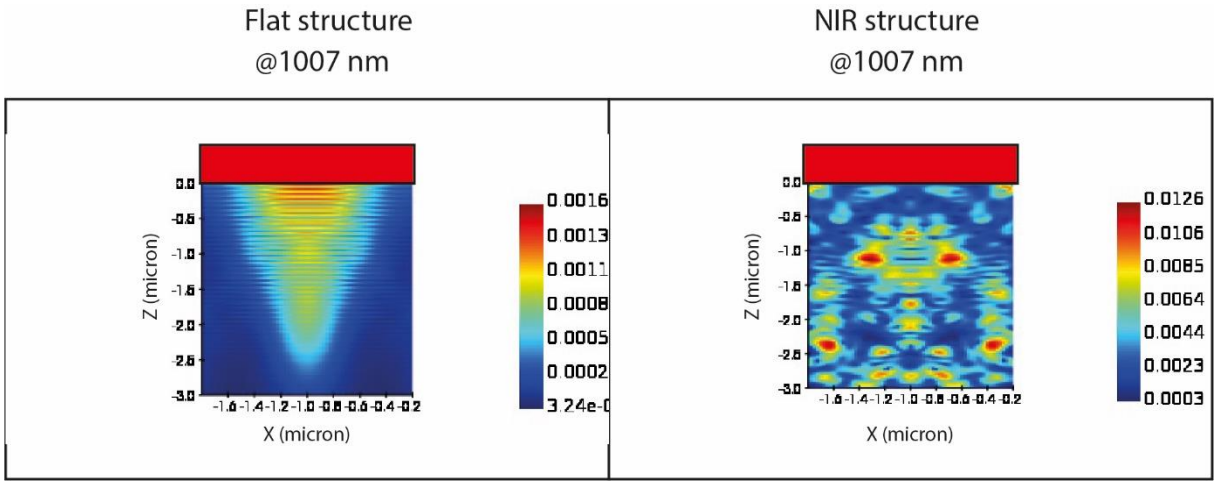

Figure 4.1. Power-flux (|S|) distribution at 1007 nm for flat reference and Structure-1 pixel. Enhanced photon recycling at the pyramidal reflector and oblique propagation within the silicon indicate more efficient energy trapping in Structure-1

In the NIR range, Structure-1 shows a clear improvement. For example, the red pixel OE at 1007 nm increases from 0.245 (flat) to 0.485 (Structure-1), which corresponds to a 98 % improvement.

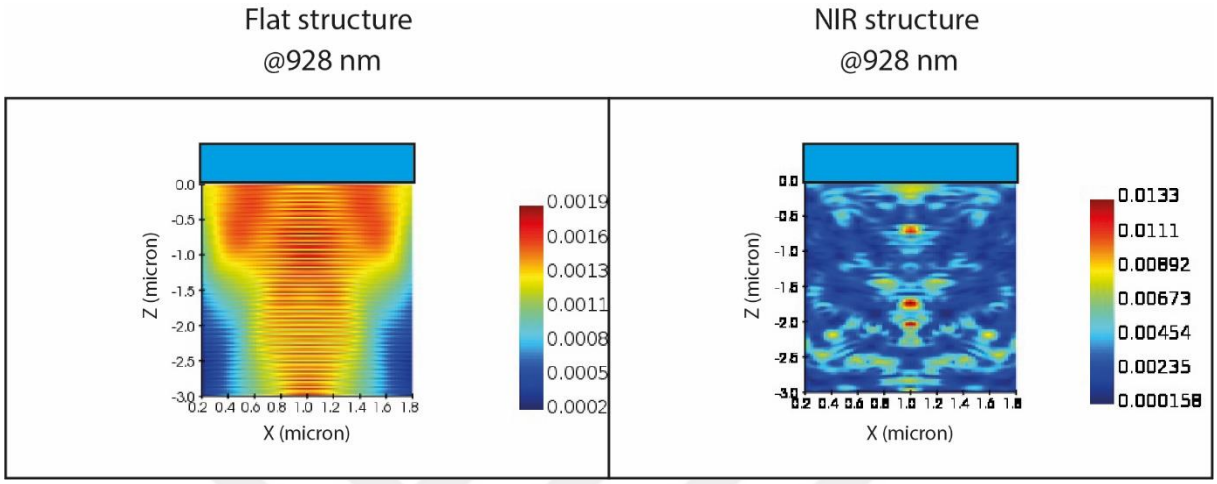

Figure 4.2. Power-flux (|S|) distribution at 928 nm for flat reference and Structure-1 pixel. Structure-1 demonstrates improved optical confinement within the silicon due to the hemispherical refraction and lateral isolation by DTIs

Similarly, the blue pixel OE increases from 0.220 (flat) to 0.509 (Structure-1) at 928 nm, indicating an improvement of approximately 131%. Although the improvement is smaller for green pixels, the NIR enhancement is still noticeable. In the visible range, both structures have similar OE performance, showing that the added features do not reduce efficiency in that region. To visualize the underlying mechanisms, Figure 4.2 illustrates the power-flux distribution at 928 nm, where the Structure-1 pixel exhibits stronger optical confinement within the silicon compared to the flat reference. The hemispherical element directs photons obliquely, while the DTI boundaries prevent lateral leakage. As can be seen in Figure 4.3, at 1007 nm, light penetration is deeper and the pyramidal reflector becomes dominant, redirecting residual flux upward and enhancing the effective absorption path length. These spatial distributions confirm that the proposed design achieves more efficient photon trapping at long wavelengths.

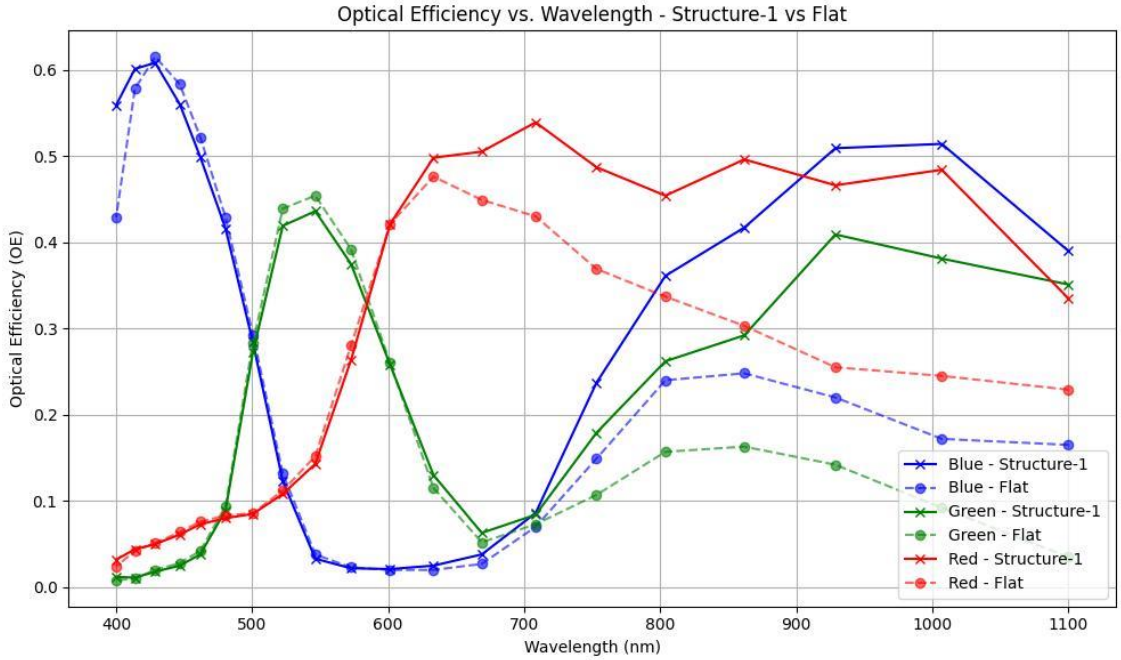

Figure 4.3. OE performance of Structure-1 and flat CMOS pixel for red, green, and blue filters across 400–1100 nm wavelength range

The improvement results from the combined effect of the three optical elements. The hemispherical layer scatters light, increasing the path length inside the silicon. The reflective pyramid helps redirect photons that might otherwise escape. DTIs reduce optical crosstalk by blocking lateral light spread.

In summary, Structure-1 achieves a substantial NIR-band OE improvement while preserving visible-band response. These results demonstrate that path-length extension, photon recycling, and lateral confinement are effective and mutually reinforcing strategies for boosting the NIR sensitivity of CMOS image sensors.

4.2.2 Structure-2 Performance Analysis

Structure-2 is designed to enhance NIR sensitivity by integrating a Gallium Arsenide (GaAs) layer beneath the silicon photodiode. GaAs exhibits a significantly higher absorption coefficient than silicon in the NIR range, particularly between 800 nm and 1000 nm, enabling more efficient conversion of long-wavelength photons into charge carriers. This hybrid semiconductor configuration addresses the intrinsic absorption limitation of silicon while maintaining compatibility with CMOS fabrication processes.

The simulated pixel cell measures 2 × 2 µm² and consists of a 3 µm-thick silicon photodiode positioned above a 1 µm-thick GaAs layer. The GaAs region serves as an additional photon-absorbing substructure for wavelengths that penetrate through the silicon. SiO_2-based DTI structures with a width of 150 nm and depth of 2 µm are incorporated around the photodiode to minimize lateral optical crosstalk between adjacent pixels. The stack also includes an anti-reflection layer (Si_3N_4, 70 nm thick), a color filter (0.6 µm thick), and a microlens with a radius of curvature of 2 µm.

The optical efficiency of Structure-2 is evaluated across the 400 nm to 1100 nm spectral range and is compared against a conventional flat CMOS pixel under identical simulation conditions. Figure 4.4 presents the wavelength-dependent OE results for red, green, and blue pixels. In this plot, solid lines with "x" markers indicate Structure-2 performance, while dashed lines with "o" markers represent the baseline flat structure.

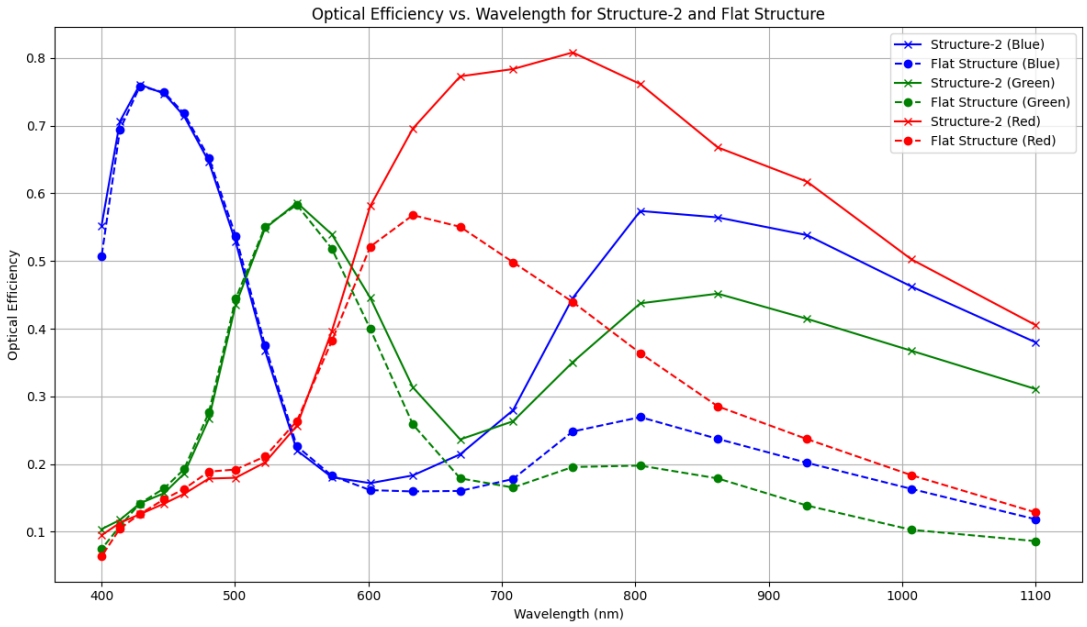

Figure 4.4. OE comparison of Structure-2 and flat CMOS pixel for red, green, and blue filters across 400–1100 nm wavelength range

A substantial enhancement is observed in the NIR band, particularly for red pixels. At 928 nm, the OE of the red pixel reaches 0.617 in Structure-2, compared to 0.237 in the flat structure, yielding an improvement of over 160%.

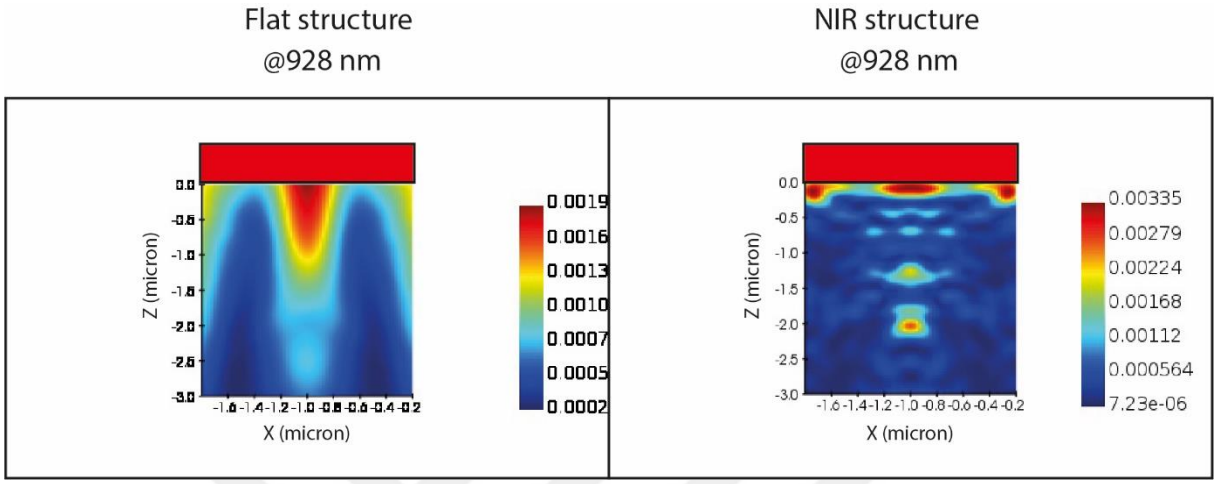

Figure 4.5. Power-flux (|S|) distribution at 928 nm for flat reference and Structure-2 red pixel

Similarly, for blue pixels, OE increases from 0.202 to 0.538, and for green pixels from 0.139 to 0.415 at the same wavelength. These gains highlight the effectiveness of the hybrid Si-GaAs configuration in extending photon absorption into the NIR region, where silicon alone becomes weakly absorbing. Figure 4.5 and Figure 4.6 illustrate the internal power-flux distributions for red and blue pixels at 928 nm, respectively, confirming that photons penetrate more deeply into the hybrid stack and are effectively captured by the GaAs sublayer. The enhanced field confinement and reduced transmission losses visible in these figures clearly demonstrate the superior NIR absorption capability of the Si–GaAs architecture compared to the flat reference pixel.

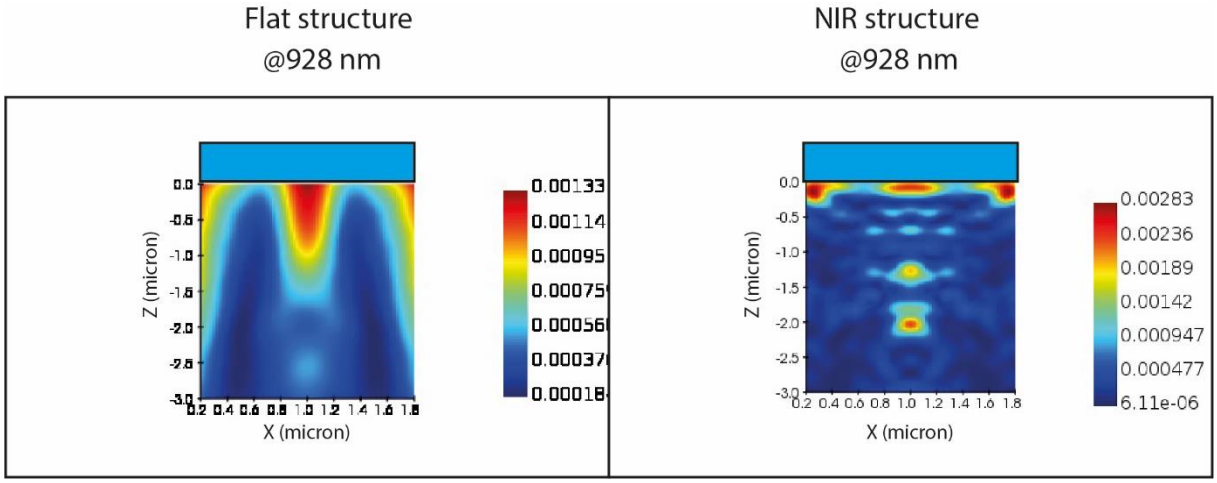

Figure 4.6. Power-flux (|S|) distribution at 928 nm for flat reference and Structure-2 blue pixel

In the visible range (400–700 nm), OE values for Structure-2 remain comparable to the flat reference, confirming that the addition of the GaAs sublayer does not degrade performance in the primary imaging band. The improvement is most pronounced for longer wavelengths, where silicon's absorption drops significantly but GaAs continues to absorb efficiently.

The performance gains result from the complementary absorption profiles of the two semiconductors: silicon captures shorter wavelengths effectively, while GaAs absorbs transmitted NIR photons that would otherwise escape. The incorporation of DTI structures further preserves spatial resolution by suppressing optical crosstalk, ensuring that the increased sensitivity does not come at the cost of image clarity.

Overall, Structure-2 demonstrates the potential of hybrid semiconductor architectures for extending the spectral response of CMOS image sensors into the NIR range. The combination of silicon and GaAs provides broadband sensitivity enhancement while remaining compatible with standard fabrication workflows, making it a promising solution for applications such as machine vision, biomedical imaging, and low-light surveillance.

4.2.3 Structure-3 Performance Analysis

Structure-3 employs an inverted pyramid surface texture on the top interface of the silicon photodiode to enhance light trapping, particularly in the NIR range of 800-1100 nm. This

surface modification increases the optical path length of incident photons, thereby improving absorption efficiency without increasing the overall thickness of the photodiode layer.

Each inverted pyramid measures 0.9 × 0.9 μm^2 laterally and has a depth of approximately 0.566 µm, consistent with dimensions achievable via anisotropic wet etching. Above the textured silicon surface, a 70 nm-thick silicon nitride (Si_3N_4) anti-reflection layer (ARL) minimizes Fresnel losses and improves light coupling. A color filter layer is positioned above the ARL, modeled using a Lorentz dispersion profile from the simulation library. A microlens with a radius of curvature (ROC) of 2 µm and a conic constant (cc) of –1 is integrated on top to focus light onto the active area. To limit lateral optical leakage, 150 nm-wide, 2 µm-deep aluminum-filled DTI structures are embedded around each pixel. Additionally, a thin SiO_2 layer is placed beneath the photodiode to reflect transmitted photons back into the silicon for secondary absorption. DTI trenches are modeled as metal-filled to emulate strong lateral reflection and optical isolation in the NIR.

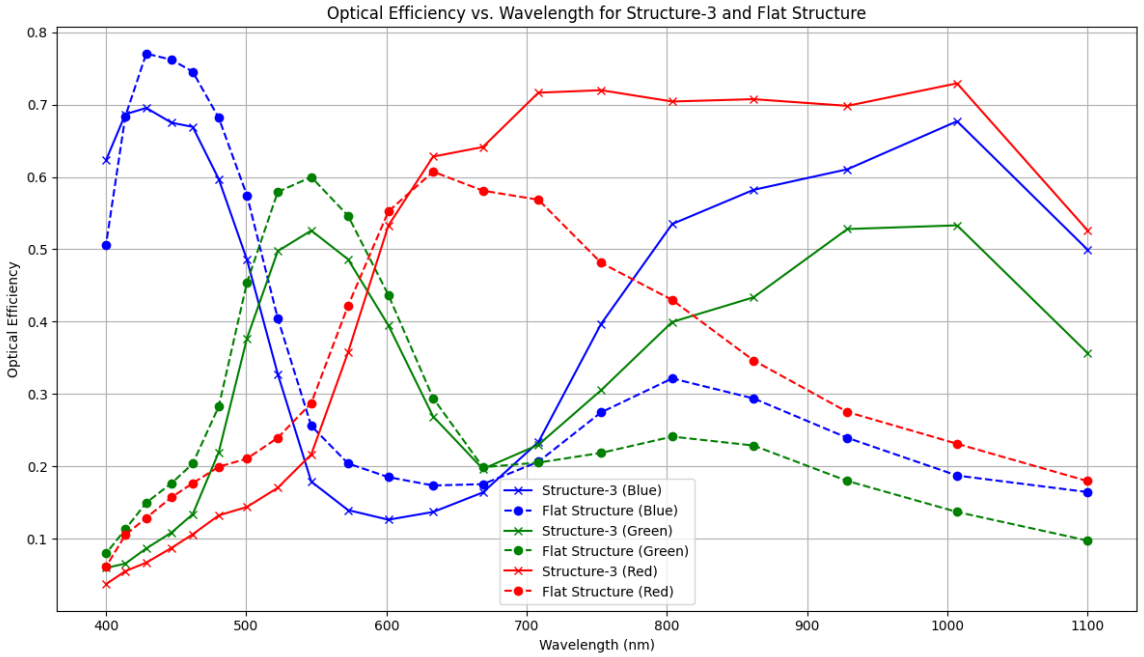

Figure 4.7. OE comparison of Structure-3 and flat CMOS pixel for red, green, and blue filters across the 400–1100 nm spectral range

Figure 4.7 compares the OE spectra of Structure-3 and a flat CMOS reference pixel for red, green, and blue channels under identical simulation conditions (3 µm silicon thickness,

broadband illumination from 400–1100 nm, and periodic lateral boundaries). Structure-3 shows substantial OE gains in the NIR range.

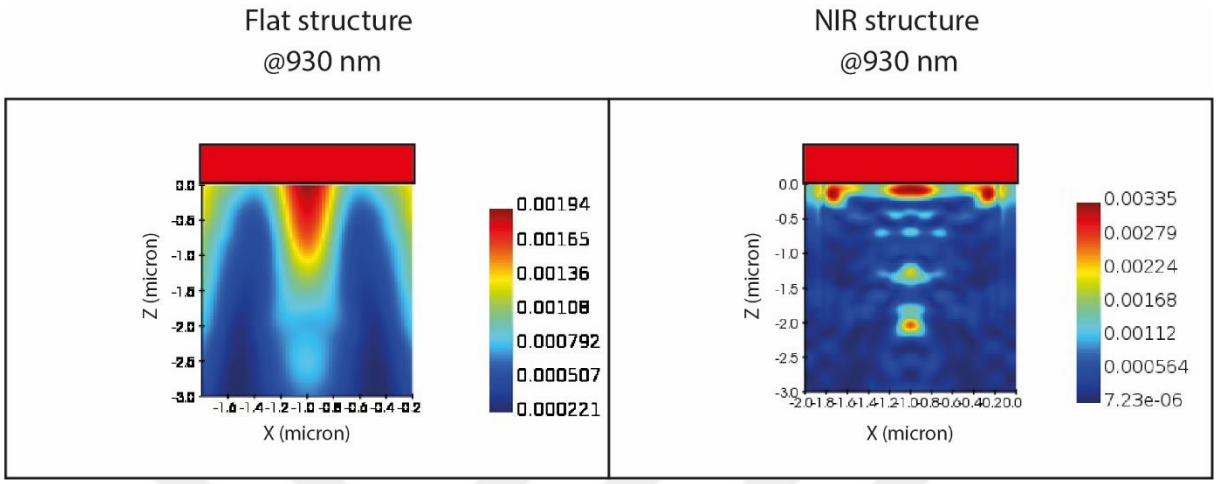

Figure 4.8. Power-flux (|S|) distribution at 930 nm for flat reference and Structure-3 red pixel

For example, at 930 nm, the red pixel OE increases from 0.275 (flat) to 0.698 (Structure-3), representing an enhancement of more than 154%. Blue and green pixels also exhibit significant improvements: at 860 nm, OE rises from 0.294 to 0.582 for blue pixels and from 0.228 to 0.434 for green pixels. To visualize the light-trapping mechanism, Figure 4.8 and Figure 4.9 show the power-flux distributions at 930 nm and 860 nm, respectively.

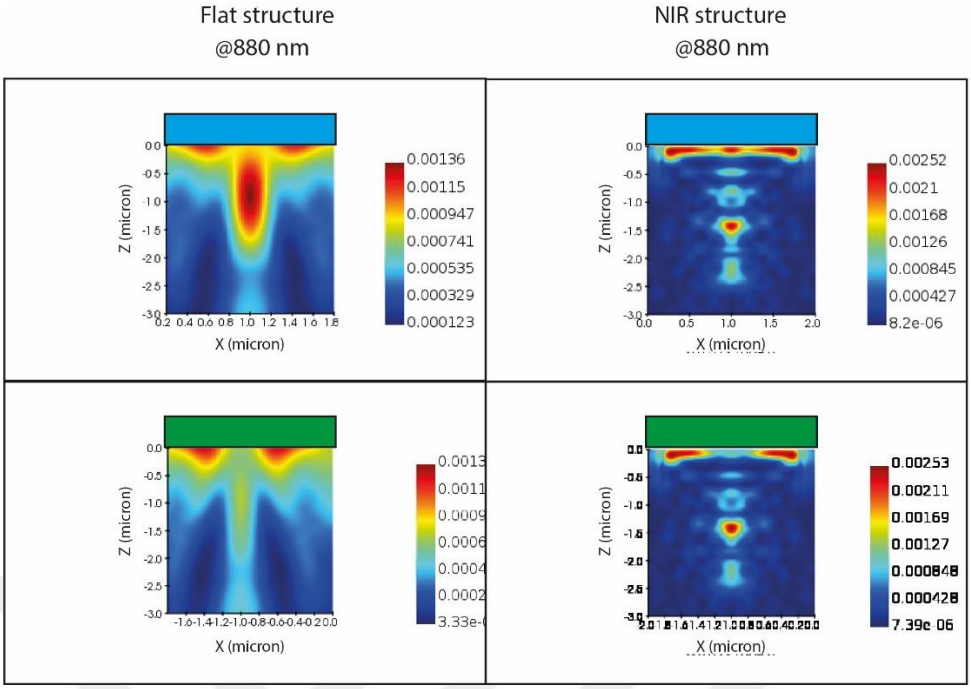

Figure 4.9. Power-flux (|S|) distribution at 860 nm for flat reference and Structure-3 blue and green pixels

In the visible spectrum (400–700 nm), Structure-3 maintains OE values comparable to the flat pixel, confirming that the inverted pyramid texture does not compromise performance in the primary imaging band. The observed NIR gains can be attributed to three synergistic effects:

1. Surface texturing via inverted pyramids increases photon path length through multiple internal reflections.
2. Aluminum-filled DTI structures confine light within individual pixels, reducing crosstalk and preserving spatial resolution.
3. Bottom SiO_2 reflection recirculates transmitted light back into the absorption volume for additional conversion opportunities.

In summary, Structure-3 achieves significant NIR-band OE enhancement while maintaining visible-band performance. The synergistic effects of path-length extension (pyramids), lateral confinement (DTI), and photon recycling (back reflector) establish an optical upper bound for geometry-driven light-trapping strategies in CMOS image sensors.

4.2.4 Structure-4 Performance Analysis

Structure-4 was developed to maximize NIR sensitivity by integrating multiple light-management mechanisms within a single CMOS pixel architecture. This design combines lateral photon scattering, enhanced sub-surface absorption, and strong optical confinement to prolong photon–silicon interaction and minimize optical losses within the 800–1100 nm spectral window.

The structure consists of four principal optical components:

1. SiO_2 inverted-cone scatterers positioned beneath the color-filter layer. These features laterally redistribute incoming photons, promoting oblique trajectories and extending their effective path length within the silicon photodiode.
2. A heavily doped silicon (HD-Si) layer approximately 300 nm thick, located below the intrinsic silicon region. Acting as an auxiliary photon absorber, this layer captures deeply penetrating NIR photons that would otherwise escape through the substrate.
3. Perfect Electric Conductor (PEC) DTI separating adjacent pixels. These trenches provide strong optical confinement, effectively suppressing lateral photon leakage and optical crosstalk.
4. A 2 μm-thick SiO_2 substrate acting as a back reflector, which redirects unabsorbed photons upward into the active region, increasing the probability of multiple absorption events.

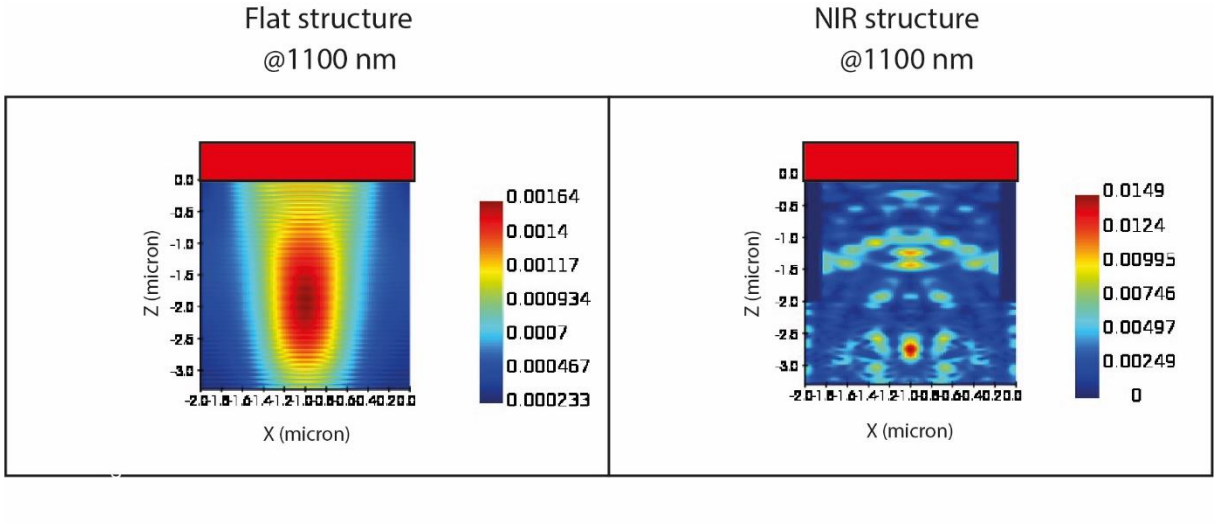

Figure 4.10. Power-flux (|S|) distribution at 1100 nm for flat reference and Structure-4 red pixel

As illustrated in Figure 4.10, at 1100 nm, the OE for red pixels in Structure-4 reaches approximately 0.824, a dramatic enhancement over the flat structure's 0.214. This improvement of nearly 285% indicates the successful redirection and confinement of long-wavelength photons within the silicon layer. Similar improvements are observed across the NIR spectrum. For example, at 930 nm, the red pixel's OE increases from 0.297 to 0.748, while the blue pixel's OE improves from 0.248 to 0.634.

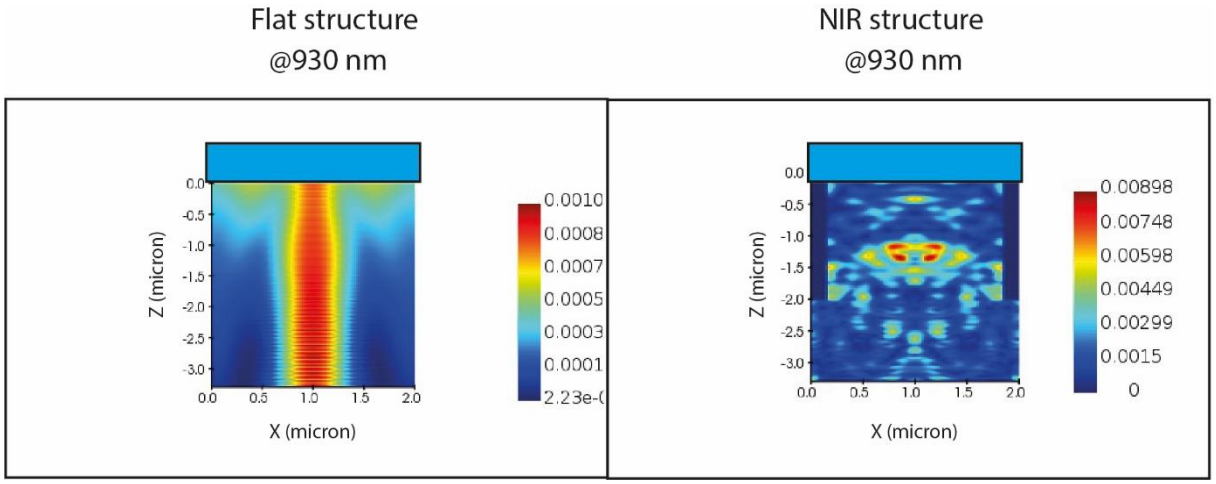

Figure 4.11. Power-flux (|S|) distribution at 930 nm for flat reference and Structure-4 blue pixel

The power-flux distribution at 930 nm is shown in Figure 4.11, highlighting the lateral confinement and scattering-induced oblique propagation. Even green pixels, which traditionally

exhibit weaker NIR response, show meaningful enhancement from 0.167 to 0.453 at the same wavelength.

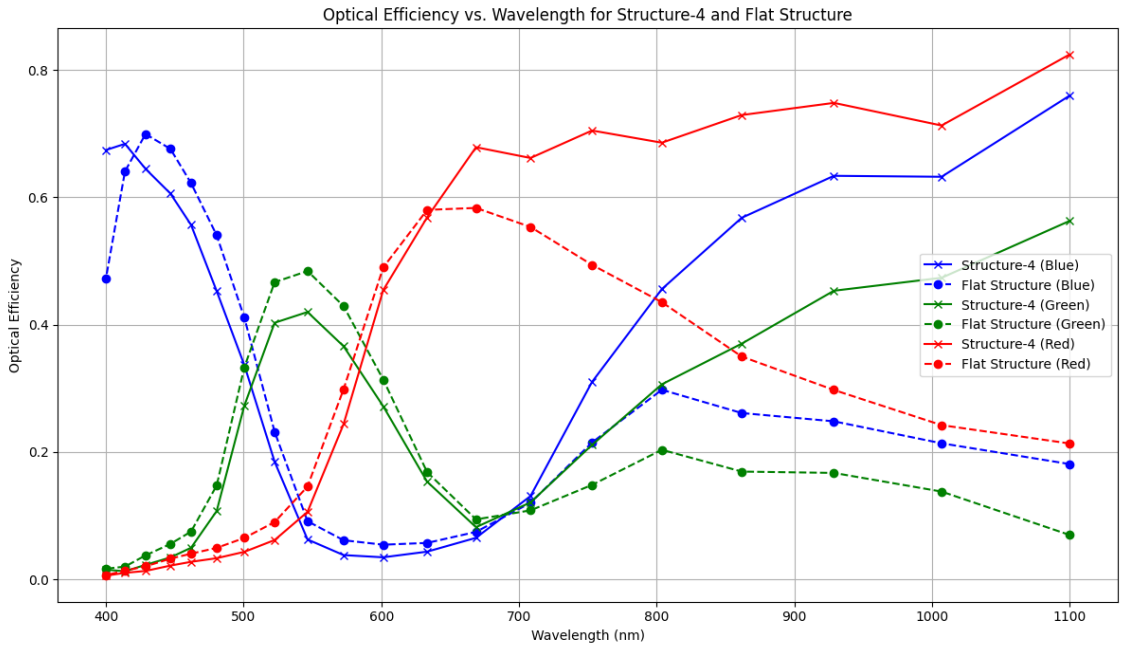

Figure 4.12. OE comparison of Structure-4 and flat CMOS pixels for red, green, and blue filters between 400–1100 nm

As shown in Figure 4.12, the observed improvements stem from the structure's dual mechanism: the inverted cone geometry aids in guiding incident light into the photodiode, minimizing surface reflection, while the HD-Si region increases photon absorption near the silicon-substrate interface. Though the heavily doped region may raise concerns regarding carrier recombination and potential parasitic junction effects, its role here is primarily optical, serving as a controlled photon absorber rather than a charge collection site. This ensures electrical performance is not severely compromised while optical gains are realized. Similar to Structure-3, the PEC-modeled DTIs serve as ideal reflectors in the optical domain, representing an upper-bound configuration for lateral confinement. In a real CMOS implementation, a thin dielectric liner (e.g., SiO_2 or SiN) would be required between the silicon and any conductive trench material to preserve electrical isolation.

Importantly, the visible light performance remains relatively stable. Between 400–700 nm, Structure-4 performs comparably to the flat structure. Slight drops in OE for some channels

(e.g., blue) are offset by the substantial NIR benefits. The balance between enhancing NIR sensitivity and preserving visible light response is key in imaging systems targeting extended spectrum performance, such as biomedical, security, or autonomous sensing applications.

In summary, Structure-4 achieves the highest NIR OE among the proposed pixel architectures. By coupling geometrical photon guidance with sub-photodiode absorption, the design facilitates deep photon penetration and efficient energy conversion at long wavelengths.
Although the HD-Si layer and PEC-DTIs are modeled as theoretical constructs, their inclusion provides valuable insight into the optical upper limit achievable through material-assisted design. This structure thus represents both a conceptually feasible enhancement and a stepping-stone toward hybrid CMOS pixels incorporating plasmonic or quantum-structured materials.

4.3. Performance Comparison of All Proposed Structures

This section provides a comparative evaluation of the optical performance of all four proposed CMOS pixel architectures, including the flat reference design. The primary objective is to quantify the improvements in NIR sensitivity achieved by each structural modification and to identify the dominant mechanisms contributing to enhanced photon absorption and confinement.

To assess the relative effectiveness of the proposed structures, the average OE values over the NIR band (defined as 800 nm to 1100 nm) are calculated separately for red, green, and blue pixels. Table 4.1 presents the aggregated OE values:

Table 4.1. Average OE of all structures over the 800–1100 nm NIR band

Structure	**Blue (Avg. OE)**	**Green (Avg. OE)**	**Red (Avg. OE)**
Flat Structure	0.210	0.118	0.274
Structure-1	0.435	0.339	0.449
Structure-2	0.503	0.396	0.591
Structure-3	0.581	0.451	0.674
Structure-4	0.610	0.434	0.740

The results clearly indicate a consistent and significant improvement in NIR optical efficiency with each successive structural enhancement. Structure-4, which incorporates an inverted conical scatterer and a heavily doped sublayer, provides the highest gains across all color channels, especially for red pixels. Compared to the flat reference, Structure-4 improves red pixel OE by about 170%, blue by 190%, and green by approximately 260% on average.

The evolution of these gains reflects the underlying design logic of each structure:

- Structure-1 employs hemispherical surface scattering, a reflective base, and SiO_2-filled DTI to lengthen photon trajectories and reduce lateral leakage.
- Structure-2 introduces a hybrid Si–GaAs absorber, where GaAs effectively captures transmitted NIR photons that silicon alone cannot absorb, thereby extending the spectral response without affecting visible-band performance.
- Structure-3 utilizes inverted-pyramid surface texturing to promote multi-path reflections and oblique photon propagation, enhancing light confinement in a purely silicon-based platform.
- Structure-4 integrates multiple optical control mechanisms, including SiO_2 inverted-cone scattering, a heavily-doped Si sublayer acting as a photon sink, PEC-modeled DTI for maximal lateral confinement, and a SiO_2 bottom reflector for photon recycling yielding the most significant NIR gain.

From an engineering perspective, the findings demonstrate that pixel sensitivity in the NIR range can be substantially increased without the need for non-standard materials or costly external layers. With proper process integration, even complex geometries such as pyramidal or conical trenches may be feasible in advanced CMOS fabrication lines. However, implementation of the heavily doped silicon layer (Structure-4) may require process calibration to minimize electrical parasitics.

Overall, the comparative summary provides a clear foundation for identifying optimal pixel designs for NIR-enhanced imaging, forming the basis for theoretical advancement and future experimental implementation.

4.4. Comparative Discussion with Literature

This section contextualizes the simulation results within the framework of existing literature while highlighting the novel aspects and scientific contributions of this research, including two peer-reviewed publications (Yucekul & Tanrikulu, 2025a, 2025b) derived from this work. Rather than reiterating the earlier literature review, the goal here is to provide a focused, comparative interpretation demonstrating how the proposed pixel architectures advance near-infrared sensitivity beyond typical strategies reported in previous studies.

In general, prior works have pursued three principal approaches to improving NIR performance in CMOS image sensors:

i. increasing the thickness of the silicon photodiode,
ii. implementing surface or sub-wavelength light-trapping structures, and
iii. integrating non-silicon absorbers or hybrid stacks.

Structure-1 combines hemispherical scattering, SiO_2-filled DTI, and a reflective pyramidal backstructure. The modelled effect is strong optical path-lengthening with reduced lateral leakage. For example, the red pixel's OE at 1007 nm increases from 0.245 to 0.485, corresponding to an improvement of about 98 %, while the blue pixel's OE at 928 nm rises from 0.220 to 0.509 (≈ 131 % gain). These gains arise from the combined scattering and photon recapture rather than from any single element alone. Comparable single-feature approaches in the literature generally achieve smaller, wavelength-limited improvements; Structure-1 demonstrates that a combined scattering + isolation + back-reflection approach can yield larger net NIR gains without compromising visible-band performance.

Structure-2 is a hybrid architecture that places a GaAs absorbing sublayer beneath the silicon photodiode, together with SiO_2-filled DTI for optical isolation. This hybrid arrangement is an original contribution of this thesis (reported in the author's publications). It achieves particularly large gains in the 900–1000 nm range; for example, at 930 nm the red pixel OE increases from 0.237 to 0.617 (≈160% gain), with similar improvements for blue (0.220 to 0.538) and green (0.139 to 0.415) pixels. By introducing an efficient NIR absorber directly below the silicon, Structure-2 captures long-wavelength photons that would otherwise transmit through the device a practical and high-impact route to NIR sensitivity enhancement near 1 μm.

Structure-3 uses inverted-pyramid surface texturing, a concept that has precedents in the literature, but here it is combined with aluminium-filled DTI and a bottom SiO_2 reflector. This combination traps photons more effectively and suppresses lateral crosstalk. At 930 nm, red OE increases from 0.275 to 0.698 (154% gain); at 860 nm, blue increases from 0.294 to 0.582 and green from 0.228 to 0.434. While inverted-pyramid texturing alone is not new, this specific integration of metallic-filled isolation and a reflective base is an original and performance relevant variant that provides stronger NIR enhancement while maintaining visible-light efficiency.

Structure-4 integrates multiple mechanisms: lateral scattering via an inverted SiO_2 cone, a heavily doped silicon absorbing sublayer, PEC (metallic) trench isolation, and a bottom SiO_2 reflector. This configuration achieves the highest average NIR optical efficiency across all color channels (see Table 4.1), with improvements of approximately 190 % for blue, 260 % for green, and 170 % for red pixels relative to the flat reference. The combination of extended path length, additional sub-silicon absorption, and strong optical isolation accounts for this broad, high-magnitude improvement. However, implementing the heavily doped silicon layer and PEC trenches may require process calibration to manage electrical parasitics.

Many recent studies have explored plasmonic metals, nanophotonic gratings, or exotic material stacks to enhance NIR response. While these methods can yield localized optical enhancement, they often introduce significant fabrication complexity or CMOS-incompatibility. In contrast, the architectures presented in this thesis deliberately emphasize CMOS-feasible solutions, including dielectric patterning, standard DTI processing, and selective hybrid material integration. This design philosophy ensures that optical improvements are accompanied by realistic manufacturability.

4.5. Evaluation of Research Hypothesis and Implications

This research was built upon the hypothesis that geometrical modifications compatible with standard CMOS fabrication can significantly enhance OE in the NIR spectral region. The simulation results obtained from the proposed pixel architectures provide strong and consistent evidence supporting this hypothesis.

Across the 800–1100 nm wavelength range, each proposed structure demonstrates a clear increase in OE relative to the flat reference design. For instance, Structure-4 achieves an OE of approximately 0.824 for red pixels at 1100 nm, whereas the flat structure yields only 0.214 under identical conditions. This improvement of nearly 285 % confirms that geometrical light-trapping and refractive guidance can effectively compensate for silicon's limited absorption in the NIR region.

Equally significant, within the visible spectrum (400–700 nm), the proposed architectures maintain comparable performance to the flat reference. This indicates that NIR-specific enhancements do not compromise visible-band response or overall image quality an essential balance for practical sensor integration.

Notably, Structure-1 (hemispherical scattering + reflective back-structure + oxide-filled DTI) and Structure-2 (Si–GaAs hybrid photodiode + oxide-filled DTI) represent original concepts introduced by the author for the first time in the literature. In particular, the hybrid GaAs sublayer in Structure-2 achieves exceptional gains near 1 μm, where pure silicon absorption sharply declines.

While Structure-3 employs an inverted-pyramid surface texture a concept known from previous research its specific integration with aluminum-filled DTI and a bottom reflective oxide layer is an innovative, performance-driven variation uniquely tailored in this work.

The implications of these findings are twofold:

1. For CMOS Image Sensor Design: The proposed geometries provide a process-compatible path to enhanced NIR sensitivity without relying on exotic materials or non-standard post-processing steps. This makes them suitable for a broad range of applications such as biomedical applications, automotive night vision, industrial inspection, and surveillance, where NIR illumination is widely used.

2. For Optical Design and Simulation: The findings emphasize the value of full-field electromagnetic simulations in pixel-level design. The use of FDTD modeling enables

precise evaluation of optical interactions within complex microstructures and allows optimization in the early stages of development. This approach allows accurate prediction of light–structure interactions and enables early-stage optimization before committing to fabrication, thereby reducing both cost and risk.

In summary, the findings strongly validate the original research hypothesis: well-engineered geometrical modifications can substantially increase NIR sensitivity while preserving visible-band performance. This establishes a practical and scalable design strategy for next-generation image sensors, with potential to be further extended through hybrid architectures that combine geometric optimization with advanced material integration.

5. CONCLUSION

5.1. General Overview

This doctoral research has comprehensively investigated light management and geometrical enhancement techniques to improve the NIR sensitivity of CMOS image sensors (CIS). The study arose from a fundamental limitation inherent to silicon-based imagers: their weak absorption beyond approximately 700 nm, which restricts QE and overall responsivity in the NIR.

The central hypothesis of this work proposed that geometrical modifications, when carefully optimized and modeled within standard CMOS-compatible design principles, can significantly enhance NIR optical efficiency without degrading visible-band performance. Through a series of four systematically designed pixel architectures, each incorporating distinct light-trapping, confinement, or absorption mechanisms, this hypothesis has been rigorously tested and validated using electromagnetic simulations.

FDTD method, implemented via ANSYS Lumerical, was employed to numerically solve Maxwell's equations and capture the electromagnetic behavior of light–matter interaction within sub-micron-scale pixel geometries. Broadband plane-wave excitation (400–1100 nm) and periodic lateral boundaries were applied to emulate realistic illumination and infinite array behavior. OE was calculated as the ratio of absorbed to incident optical power within the silicon region, based on Poynting vector integration across the active volume.

This methodological framework ensured quantitative comparability between all designs and allowed identification of the structural features most responsible for improved NIR performance. The results provide compelling evidence that engineered geometrical control rather than material substitution alone offers a robust and scalable route toward extended-spectrum CMOS sensors.

5.2. Summary of Key Findings

The four proposed pixel structures, benchmarked against a flat CMOS reference, yielded progressive and consistent optical improvements across the NIR band (800–1100 nm). Each architecture represents a specific evolutionary step in integrating optical confinement, scattering, and hybrid absorption into a manufacturable pixel design.

Structure 1 integrates three light-management elements: a hemispherical scattering layer above the photodiode, SiO_2-filled DTI surrounding each pixel for lateral optical confinement, and a pyramidal reflective back-structure beneath the silicon substrate. These features act synergistically to increase photon path length and reduce lateral leakage. The red pixel OE improves from 0.245 to 0.485 at 1007 nm (~98 %), while the blue pixel OE increases from 0.220 to 0.509 at 928 nm (~131 %). The configuration preserves visible-band efficiency, confirming that NIR enhancement can be achieved without compromising standard imaging performance. The core design philosophy of Structure-1 was originally introduced by the author in a peer-reviewed publication on hemispherical photon-trapping structures (Yucekul & Tanrikulu, 2025a), where the scattering-induced path-length extension mechanism was first demonstrated and validated as an effective approach for enhancing NIR absorption in CMOS pixels. The present study expands this concept by integrating additional confinement features such as DTI and a reflective back-structure, yielding a more comprehensive light-management architecture.

Structure 2 introduces a thin gallium arsenide (GaAs) layer (≈1 μm) beneath a 3 μm silicon photodiode. GaAs has a higher absorption coefficient in the NIR, particularly between 800-1000 nm, enabling capture of long-wavelength photons transmitted through silicon. SiO_2-filled DTIs isolate the pixel laterally, maintaining low crosstalk. This hybrid semiconductor stack an original contribution of this thesis and reported in Yücekul & Tanrıkulu (Yucekul & Tanrikulu, 2025b) achieves an OE improvement from 0.237 to 0.617 at 930 nm (~160 % for red pixels). Blue and green channels show comparable enhancement. The results verify that selective integration of non-silicon absorbers can broaden spectral response while remaining CMOS-feasible, providing a practical pathway for extended NIR detection.

Structure 3 applies inverted-pyramid texturing on the silicon surface to promote multi-reflection and oblique photon propagation. The design also features aluminum-filled DTIs (metallic reflectors) for superior confinement and a bottom SiO_2 reflector for photon recycling.

At 930 nm, the red pixel OE increases from 0.275 to 0.698 (>150 %), while at 860 nm, blue and green channels rise from 0.294 to 0.582 and 0.228 to 0.434, respectively. The structure maintains comparable visible-light performance. These results demonstrate that silicon-only architectures, when coupled with engineered microtextures, can achieve NIR sensitivity comparable to hybrid or doped systems.

Structure 4 combines multiple light-management strategies in a single CMOS-compatible stack:

- SiO_2 inverted-cone scatterers below the color filter layer (enhancing lateral scattering and oblique photon entry),
- a 300 nm heavily doped silicon (HD-Si) layer acting as a sub-surface absorber,
- PEC-filled DTIs serving as strong lateral reflectors, and
- a 2 μm SiO_2 substrate functioning as a back reflector.
- This comprehensive design yields the highest NIR performance: at 1100 nm, red pixel OE increases from 0.214 to 0.824 (~285 %), and similar trends appear across all channels (≈190 % blue, ≈260 % green).

Although the HD-Si and PEC trenches are modeled as idealized constructs, they represent an optical upper bound and inform future fabrication-oriented optimization.

5.3. Comparative Analysis and Scientific Contributions

Across all four architectures, a clear performance evolution is observed from simple scattering enhancement to full multi-mechanism integration. The average NIR optical efficiency (800-1100 nm) improves by 170–260 % relative to the reference design, confirming the effectiveness of cumulative light-management strategies.

The distinct scientific contributions of this thesis can be summarized as follows:

1. Development of CMOS-compatible pixel geometries capable of significantly improving NIR optical efficiency through structural rather than material modification. This contribution builds upon the author's previously published work on hemispherical photon-trapping structures (Yucekul & Tanrikulu, 2025a), where scattering-induced optical path-length extension was first demonstrated through full-wave electromagnetic simulations. The present thesis expands this foundation by introducing additional confinement mechanisms such as DTI integration and reflective back-structures thus establishing a more comprehensive and scalable geometrical light-management framework for NIR-enhanced CMOS image sensors.
2. Introduction of a hybrid Si–GaAs pixel architecture (Structure 2) as a novel and CMOS-feasible design, validated through quantitative optical modeling and supported by a peer-reviewed publication (Yucekul & Tanrikulu, 2025b).
3. Demonstration of inverted-pyramid and metallic DTI integration (Structure 3), achieving geometry-driven NIR enhancement in purely silicon-based pixels.
4. Proposal of a multi-mechanism, high-confinement pixel (Structure 4) representing the theoretical performance upper limit for monolithic CMOS-compatible NIR sensing.
5. Establishment of a rigorous FDTD-based simulation methodology enabling predictive, reproducible analysis of complex sub-micron light–matter interactions.

Together, these contributions advance the field of CMOS image sensors by establishing a design philosophy that balances performance, manufacturability, and scalability, bridging the gap between theoretical light management and practical device integration.

5.4. Implications for CMOS Sensor Design

The findings of this research carry significant implications for the design and future development of CMOS image sensors. The demonstrated pixel architectures show that NIR sensitivity can be substantially enhanced through carefully engineered geometrical modifications, without the need for exotic materials, compound semiconductor platforms, or non-standard fabrication steps. This outcome is particularly important because NIR performance has traditionally relied on III–V materials such as InGaAs and GaAs due to their inherently higher absorption coefficients at long wavelengths. The results of this thesis indicate that, with appropriate light-management strategies, standard silicon-based CMOS technology

can close much of this performance gap while preserving its inherent advantages in cost, scalability, and system-level integration. Consequently, the proposed designs position CMOS as a more competitive and sustainable alternative for NIR-intensive applications such as biomedical imaging, surveillance, depth sensing, automotive night vision, and machine-vision systems.

Potential application domains include:

- Biomedical imaging and spectroscopy, where 800–1000 nm light enables deeper tissue penetration;
- Autonomous vehicle sensing and night vision, requiring high sensitivity under low illumination;
- Industrial inspection and material sorting, exploiting reflectance contrasts in the NIR band;
- Surveillance and defense imaging, where wide dynamic range and spectral adaptability are critical.

The findings thus not only strengthen the scientific understanding of NIR light management but also offer practical design guidelines for future commercial sensors.

6. RECOMMENDATIONS

Building upon these findings, several directions are recommended to extend and experimentally validate the proposed concepts:

A. Process Integration and Prototyping: Fabrication of prototype pixels using standard CMOS back-end-of-line (BEOL) workflows, focusing on the manufacturability of sub-micron cavities, textured interfaces, and deep trenches. Special attention should be given to implementing the HD-Si sublayer through ion implantation or epitaxial techniques compatible with thermal budgets.

B. Electro-Optical Characterization: Coupling optical simulations with TCAD-based electrical modeling to evaluate carrier dynamics, dark current, noise, and fill-factor trade-offs. Prototype characterization should measure both OE and electrical performance to assess real-world sensor viability.

C. Material-Assisted and Plasmonic Enhancements: Further exploration of CMOS-compatible plasmonic and high-index dielectric materials (e.g., TiN, Si_3N_4 resonators), as well as emerging color-router–based light-separation structures, can enable enhanced spectral selectivity and improved NIR coupling efficiency. These color-routing metasurfaces are capable of directing different wavelength bands into distinct spatial channels, thereby improving photon utilization and reducing inter-pixel spectral crosstalk. Integrating such routers within the microlens stack or between the color filter and passivation layers may provide additional pathways for localized field confinement and guided-mode resonance, offering a promising route for further NIR absorption gains in next-generation CMOS image sensors.

D. Machine-Learning-Aided Optimization: Implement AI-driven inverse design algorithms to optimize pixel geometry, microlens shape, and filter thickness concurrently. Such data-driven approaches can uncover non-intuitive structural combinations that yield superior optical performance.

E. System-Level Integration and Testing: Evaluation of angular dependence, polarization response, and system-level imaging behavior under realistic illumination. Long-term reliability and thermal stability should be examined for industrial and outdoor environments.

F. Hybrid and Quantum-Enhanced Architectures: As a long-term vision, integrating quantum-dot or plasmonically engineered layers with CMOS-compatible pixels could bridge the gap between traditional semiconductor detectors and next-generation multispectral imagers.

This thesis has successfully demonstrated that geometrical and structural engineering within the CMOS process framework can overcome the intrinsic NIR absorption limits of silicon. By sequentially combining scattering, confinement, hybrid absorption, and photon recycling mechanisms, the proposed pixel architectures achieve broadband enhancement while preserving visible-band performance.

The validated simulation framework, coupled with the presented optical design philosophy, provides a foundation for future CMOS-based NIR sensors that are not only efficient but also manufacturable and scalable.

Ultimately, the outcomes of this research offer a pathway toward next-generation CMOS image sensors that merge physics-based design with data-driven optimization extending the operational spectrum of silicon technology into the deep NIR region and enabling its application across biomedical, industrial, and autonomous systems.

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