# 125PS LSB COLUMN PARALLEL TIME TO DIGITAL CONVERTER INTEGRATED CIRCUIT FOR LIDAR APPLICATIONS

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# ABSTRACT

## 125PS LSB COLUMN PARALLEL TIME TO DIGITAL CONVERTER INTEGRATED CIRCUIT FOR LIDAR APPLICATIONS

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This thesis presents a column-parallel time to digital converter (TDC) integrated circuit for light detection and ranging (LIDAR) systems. The design is based on direct time-of-flight (dToF) measurement. It is designed to be used with single-photon-avalanche photodiodes (SPAD) arrays. The TDC can measure the time differences up to 1μs with 125ps precision.

This TDC design consists of four main blocks. A counter, a phase-locked loop (PLL), a delay-locked loop (DLL), and a tapped delay line (TDL) are used together to implement fine timing resolution and long-range TDC. The counter is used to increase the time difference input range. The PLL multiplies the reference clock signal frequency. PLL's voltage-controlled oscillator (VCO) is a ring oscillator that has four differential stages. The outputs of these differential stages have 45-degree phase differences, and it is used to obtain better timing resolution (similar to DLL operation). The TDL is used to achieve a fine timing resolution. It contains several series delay cells with well-defined delay times. A dedicated DLL adjusts the delay time of the cells. To have lower power consumption, the TDL has an event-driven architecture.

The design is implemented in 180nm CMOS technology. The TDC has 128 columns with 26μm pixel pitch. The least significant bit (LSB) is 125ps, and the resolution is 13bit, the maximum input range results in 1024ns (150m in the distance). The INL and DNL of the system are +2/-1 LSB at maximum. The jitter noise is 8.4ps which is well below 0.5 LSB. The sampling rate is 1MS/s. The power consumption of the system (all the sub-blocks are included) is 20.5mW.

Keywords: Time to digital converter (TDC), Light detection and ranging (LIDAR), Phase-locked loop (PLL), Delay – locked loop (DLL), Tapped delay line (TDL)

# ÖZ

## LİDAR UYGULAMALARI İÇİN 125PS LSB KOLON PARALEL ZAMAN-SAYISAL ÇEVİRİCİ TÜMLEŞİK DEVRESİ

Özpınar, Oğuzhan
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği
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Bu tez ışık saptama ve uzaklık tayini (LIDAR) uygulamaları için kolon paralel zaman – sayısal çevirici (TDC) tümleşik devresini sunmaktadır. Tasarım direkt uçuş zamanı (dToF) ölçümü tekniğine dayanmaktadır. Tek foton çığ ışık diyotu (SPAD) dizilimi ile kullanılmak için üretilmiştir. TDC 1μs'lik zaman farklılıklarını 125ps hassasiyet ile ölçebilir.

Bu TDC 4 ana bloktan oluşmaktadır. Uzun mesafeli ve yüksek hassasiyetli TDC uygulayabilmek için sayaç, faz kilitlemeli döngüsü (PLL), gecikme kilitlemeli döngüsü (DLL), dallı gecikme hattı (TDL) birlikte kullanılmıştır. Sayaç zaman farkı giriş aralığını artırmak için kullanılmıştır. PLL referans saat işaretini frekansını artırır. PLL'in gerilim kumanda osilatörü bir halka salınıcıdır ve dört diferansiyel fazdan oluşur. Bu diferansiyel fazların çıktıları 45 derecelik faz farklılıklarına sahiptir ve daha iyi zamanlama çözünürlüğü elde etmek için kullanılır (DLL işlemine benzer). Hassas zaman çözünürlüğü sağlamak için TDL kullanılmıştır. TDL, iyi tanımlanmış gecikme sürelerine sahip bir dizi seri gecikme hücresi içerir. Hücrelerin gecikme süreleri özel bir DLL tarafından ayarlanır. Daha az güç tüketimi için TDL olay güdümlü mimariye sahiptir.

Tasarım 180nm CMOS teknolojisi ile uygulanmıştır. TDC 128 kolona sahiptir ve 26µm piksel aralığında uygulanmıştır. En az ağırlıklı bit (LSB) 125ps'dir ve çözünürlük 13bit'tir, maksimum giriş aralığı 1024ns (mesafede 150m) ile sonuçlanır. Sistemin INL ve DNL'si maksimum +2/-1 LSB'dir. Titreşim gürültüsü 8.4ps'dir ve 0.5LSB'nin oldukça altındadır. Örnekleme hızı 1MS/s'dir. Sistemin güç tüketimi (tüm alt bloklar dahil) 20,5mW'dir.

Anahtar Kelimeler: Işık saptama ve uzaklık tayini (LIDAR), Zaman – sayısal çevirici (TDC), Faz kilitlemeli döngüsü (PLL), Gecikme kilitlemeli döngü (DLL), Dallı gecikme hattı (TDL)

To my family and love

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# CHAPTER 1

# INTRODUCTION

Three-dimensional imaging is a key technology for different types of applications. Self-driving cars, augmented and virtual reality, and assembly-line robotics requires high-resolution 3D imaging. The light detection and ranging systems (LIDAR) is the fastest-growing class in this field. When the LIDAR systems are compared with the other 3D imaging techniques such as millimeter-wave (MMW) radars, stereo vision cameras, or ultrasonic sensors, the LIDAR offers fast detection, high spatial resolution, and reliable 3D mapping in an uncontrolled illuminance environment [1].

The MMW radar is the industry's choice for now. It is widely used in driving assistance systems, autonomous emergency braking, and adaptive cruise control systems. The angular resolution of the MMW radar is very small due to the wavelength of the radar. It is usually combined with stereo vision cameras to increase the resolution. Such systems require high computing power and process time to construct 3D images. Also, the stereo cameras are passive sensors. It works poorly under low illumination conditions.

LIDAR can offer higher spatial resolution due to the shorter optical wavelength. It can detect much smaller objects such as pillars, wires, animals, or defects on the road. The LIDAR is an active sensor, and it has an optical source so that it can provide reliable detection under any illumination.

The previous LIDAR solutions suffer from the low responsivity of the detectors. A scanning laser is used to increase the signal-to-noise ratio (SNR). But this approach requires rotating mechanical and optical systems. That increases the cost significantly. In recent years single-photon avalanche photodiodes (SPAD) becomes

more advance. Foundries offer CMOS SPAD solutions [2]. The sensor array and the readout can be implemented on the same chip. The SPAD has high responsivity. Because of that, there is no need for complicated mechanical scanning systems. That decreases the cost significantly. The works in the literature show promising results [3].

## 1.1 3D Imaging Techniques

There are three main approaches for ranging; ultrasonic, microwave, and optical techniques. Ultrasonic sensing techniques offer low power and high resolution. But the signal attenuation is so large that the system only can be used for short distances. On the other hand, microwave techniques have a large range. They are widely used in military applications, consumer products, and industry. It is a mature technology. However, the resolution is poor, and they have a very limited field of view (FOV). Optical sensing techniques combine these applications' advantageous sides; they offer high resolution with long-range and a large FOV. It is a fast-growing technology for industry and consumer fields.

In Figure 1.1 classification of the optical 3D imaging techniques is given. It is divided into two main categories; active and passive. In active systems, the scene is illuminated by a light source. On the other hand, the passive systems are using ambient light to construct 3D images.

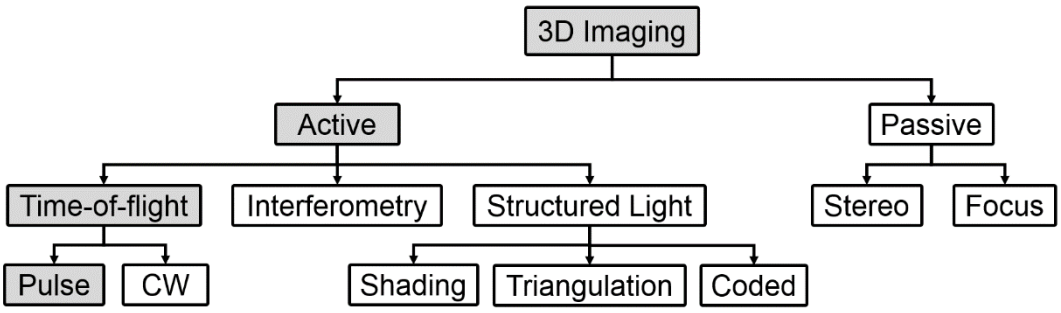



Figure 1.1. Optical 3D imaging techniques classification.

The passive systems require no illumination; it is always eye-safe. It is divided into two main categories. The first one is stereo imaging. It is similar to the human eye. Two or more images of the scene are taken with a stereo camera, and the 3D image is constructed from the differences between multiple images. These systems cannot work well under low light illumination. Also, if the scene has no texture or sharp objects, the system cannot construct depth information [4]. The second one is depth-from-focus. It requires only one camera. By changing the focus of the camera, depth information can be calculated. However, it has similar problems with stereo imaging. The system cannot construct depth information while looking at a flat wall, and it has poor performance under low light illumination [5, 6].

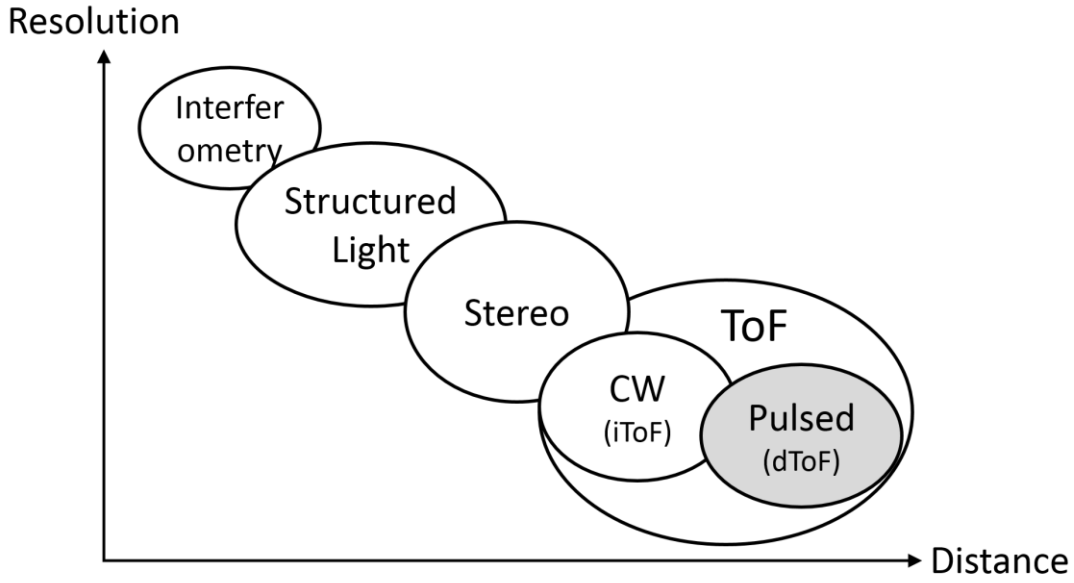



Figure 1.2. Resolution and distance comparison of different 3D imaging types.

In the active systems, the scene is illuminated with an LED or a laser source. It is divided into three main categories, as given in Figure 1.1. The first one is the interferometer technique. It has the best depth resolution, up to the nanometer range. However, the system's range is limited to a couple of millimeters [7, 8]. In the structured light techniques, the scene is illuminated with a codded 2D pattern. According to the distortion of the pattern, a 3D image is generated. The codding can be color [9] or position [10]. A famous application is Iphone’s face recognition

camera. These systems have good performances under controlled illumination environments such as house or warehouse applications. But the system suffers from detecting objects at large distances. The last technique is the time of flight. It has the largest range, can work up to hundreds of meters [11, 12]. The resolution for such systems is in the range of a couple of centimeters. The technique is explained in more detail in the next sections. The resolution and distance comparison of the different 3D imaging systems are given in Figure 1.2.

## 1.2 Single-Photon Avalanche Diode (SPAD)

SPAD is a p-n junction photo-diode. It is reverse biased above the reverse breakdown voltage. This region is called Geiger mode. In this region, the electric field in the depletion region is so large that the photo-generated electrons generate impact ionization and self-sustaining avalanche [13]. The optical gain in this region is infinite. Large currents can be generated with the absorption of a single-photon. The current needs to be limited to prevent permanent breakdown. It is limited to a quenching circuit; a simple example is a series resistor. The operation modes of the photo-diode are given in Figure 1.3.

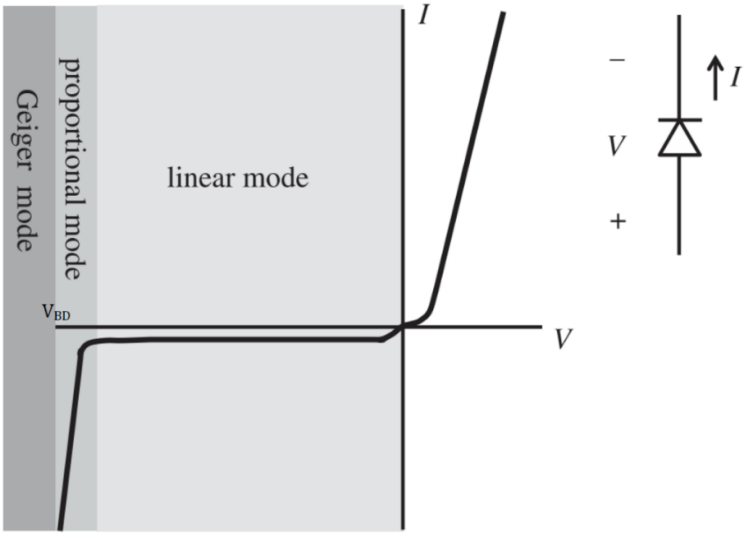



Figure 1.3. The operation modes of the photo-diode [14].

The SPAD sensors are compatible with a CMOS technology. Their size is in the order of tens of microns [15]. A SPAD array can be implemented in the same chip together with timing and read-out circuitry. That decreases the system complexity, cost, and power consumption dramatically.

The photon detection probability (PDP) of a SPAD sensor for incident wavelengths are given in Figure 1.4. It is a silicon detector, and the probability is very high in the visible wavelength region. The probability increases with the increasing reverse bias voltage. At maximum, the detection probability is around 50 percent.

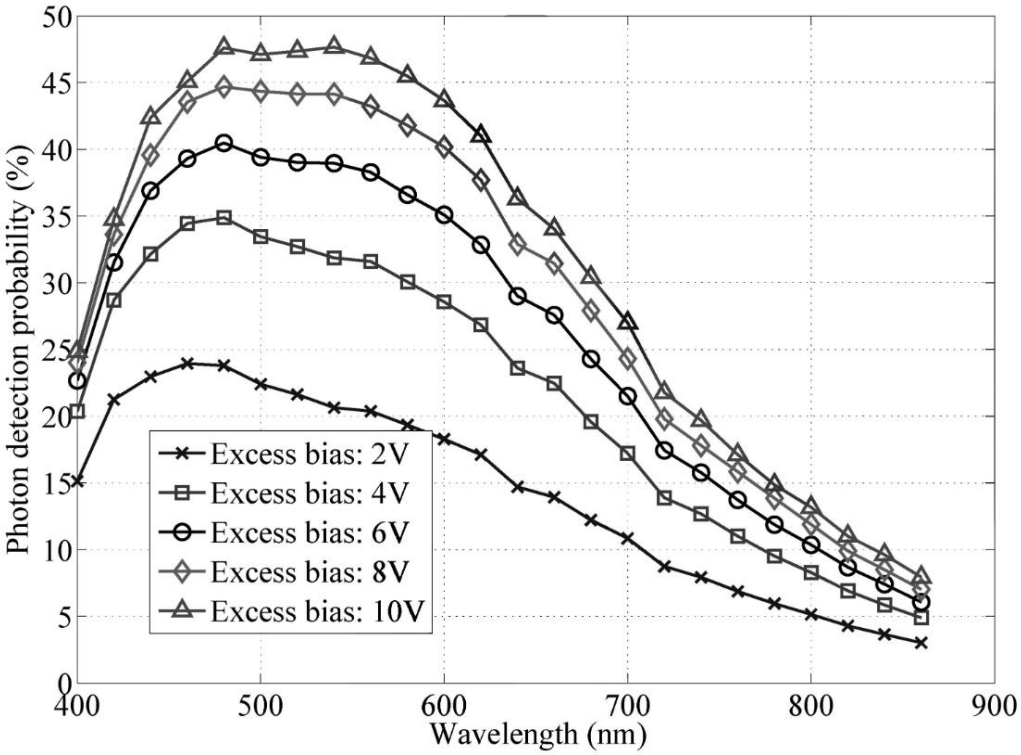



Figure 1.4. The photon detection probability (PDP) of a SPAD sensor for incident wavelengths [16].

The solar irradiance spectrum outside the atmosphere and at the sea level is given in Figure 1.5. Note that the photon detection probability and the solar irradiance are very high at the same wavelength range [16]. SPADs can be triggered by solar radiation rather than the illumination source. Also, the thermal generated and trap assisted electrons can start an avalanche and trigger the SPAD. That could lead a

false detection and background noise. The histogramming method can be used to cancel the false detection and suppress the background noise [3]. One can take the lots of sampling and create a histogram and take the mean of the histogram as actual distance data.

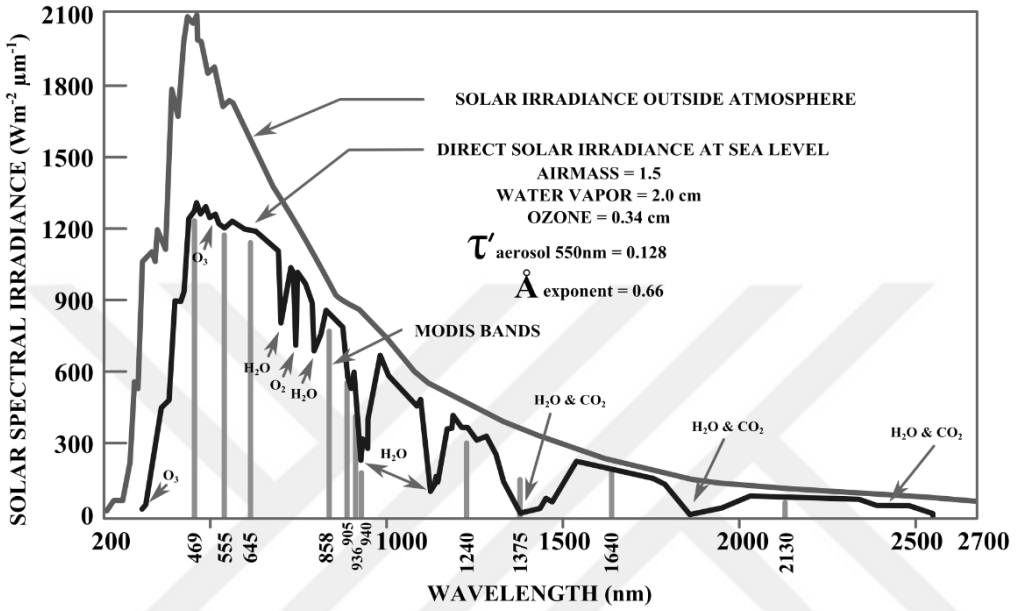



Figure 1.5. Solar irradiance spectrum outside the atmosphere and at the sea level [17]

## 1.3 Time of Flight Technique

The time of flight is an active sensing technique. The light is reflected in the scene. The light is reflected back onto the photo-detector array. The time of flight is measured indirectly (iToF) or directly (dToF). It is difficult the measure the light propagation time with p-i-n photodiode since the speed of light is extremely fast. Instead, time of flight can be calculated indirectly by measuring the phase or amplitude of the light [18]. If the reverse bias voltage of the photodiode further increased. It will work in Geiger – mode. The Geiger – mode photodiodes have virtually infinite gain and fast response time [14]. They can work as a single-photon avalanche photodiode (SPAD). It enables the measurement of the flight time directly.

### 1.3.1 Modulation Based

In the modulation-based technique, the time of flight is measured indirectly from the phase differences. The laser power is modulated by sine or square wave. The phase delay between the received and transmitted signals is measured. The time of flight can be measured with the following expression (1.1). Where the T is the modulation period, and the $\phi$ is the phase difference.

$$t_{ToF} = \frac{\phi}{2\pi} * T \tag{1.1}$$

The phase delay can be detected through a demodulation pixel. The schematic of the demodulation pixel is given in Figure 1.6. It has two transfer gates and two capacitors. With a certain integration cycle, the phase difference can be calculated from charge differences on C1 and C2 capacitances. The charging of the capacitances according to the modulation signal is given in Figure 1.7. Then the charges are digitized by an analog – to – digital converter (ADC) [1].

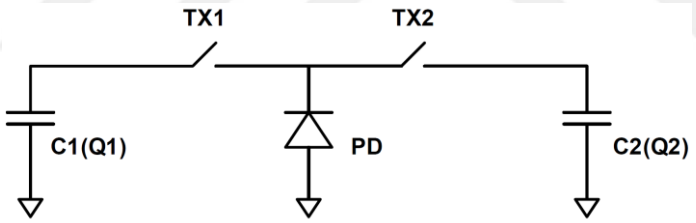



Figure 1.6. The demodulation pixel with transfer gates [1].

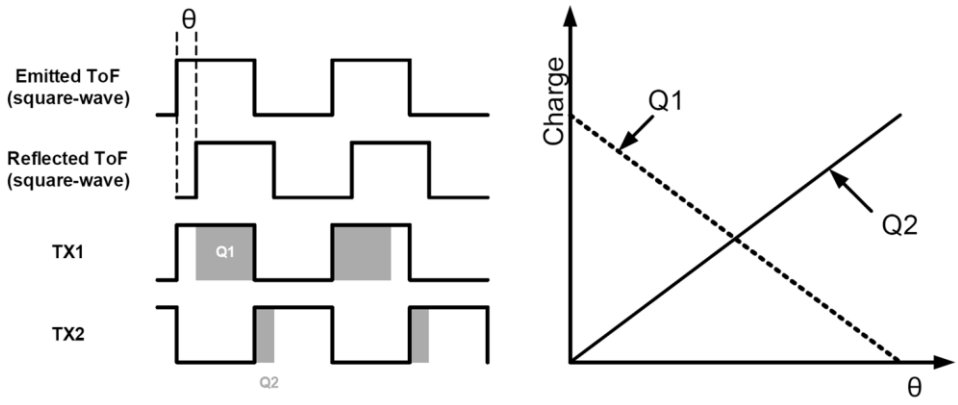



Figure 1.7. The charging of $C_1$ and $C_2$ according to the modulation signal [1].

### 1.3.2 Pulse Based

The pulse-based technique is the direct time of flight (dToF) measurement. The laser pulse is sent to the object, and the timing circuit starts counting. The counting stops with the arrival of the reflected signal. The distance is calculated with the following expression (1.2).

$$d = c * t_{ToF} * \frac{1}{2} \tag{1.2}$$

The "d" is the distance with the object, and "$t_{ToF}$" is the time of flight. Because the light travels the "d" distance two times, the light travels through the object and is reflected from the object, and it is divided by 2.

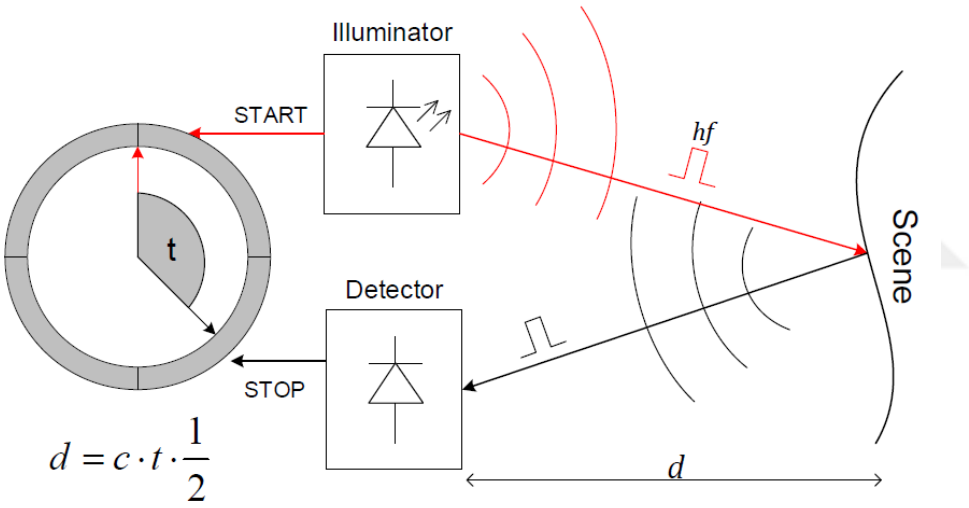



Figure 1.8. Operation diagram of the dToF technique [14].

In order to detect the short laser pulse, photo-detectors with fast timing response and high gain are required. Usually, single-photon-level sensitivity is needed in long-range applications. In recent year's semiconductor foundries offer avalanche photodiodes (APDs) and single-photon avalanche photodiodes (SPADs) in very small size [2]. The device size is tens of microns to hundreds of microns. They are available in conventional CMOS chip-level integration. It means that low power, low

cost, and high-resolution LIDAR sensors can be implemented in system-on-a-chip (SoC).

In this study time-digital converter for the pulse-based direct time of flight (dToF) technique is investigated and implemented.

## 1.4 Time – to – Digital Converters

The time-to-digital converters measure the time interval and convert it into a digital code. It measures the time difference between the start and stops signals.

They are used in many applications. The simplest form of a TDC is a stopwatch. More sophisticated forms are using in atomic and high energy physics or time-of-flight measurements where fast response and high precision are needed.

Different types of TDC architectures are investigated in the following of the thesis. The simplest one is a basic counter. Ramp and Vernier interpolator and the tapped delay line are introduced for fine time difference measurements.

### 1.4.1 Basic Counter

The basic counter is the most straightforward TDC architecture. It has a high-frequency counter that is incremented in every clock cycle. When the event occurs, the current state is captured.

The accuracy of the measurement depends on the clock frequency and the stability of the clock signal. A crystal oscillator can be used to generate the clock signal. They can offer intermediate frequencies such as 100MHz (10 ns resolution) [19]. A phase-locked loop (PLL) frequency multiplier can generate a faster clock and get better timing resolution. In that case, clock frequency increases up to gigahertz order.

In the best case, the basic counteroffers in the order of nanosecond resolution. It suffers from the high-frequency clock signal need. The power consumption is increasing due to high frequency.

### 1.4.2 Ramp Interpolator

When a further timing resolution is needed, analog methods can be used. One of the common solutions is the ramp interpolator. The method usually measures smaller intervals such as 100 ns.

In that method, a capacitor is charging with a constant current during the time interval. Initially, the capacitor discharged to zero volts. At the start event, the capacitance starts charging with a constant current, and the voltage on the capacitance slowly increases. At the stop signal, the charging-current is disconnected. The voltage on the capacitance is directly proportional to the time. The voltage on the capacitance is measured with an ADC. The resolution in such systems in the order of tens of picoseconds [20]. The interpolator requires a large layout area. It suffers from the random mismatch in capacitance value. Offset and gain calibration are needed before the measurement.

### 1.4.3 Vernier Interpolator

The Vernier method is a digital version of the ramp interpolator. The two oscillators with slightly different oscillation frequencies are needed $f_1$ and $f_2$. They start counting at the same time when the stop signal arrives; they record the count numbers $n_1$ and $n_2$. The time interval can be calculated with the following expression (1.3).

$$T = \frac{n_1 - 1}{f_1} - \frac{n_2 - 1}{f_2} \tag{1.3}$$

Highly reliable oscillators with stable and accurate frequencies are needed for the Vernier method. The system is challenging. It consumes high power and requires a large layout area.

### 1.4.4 Tapped Delay Line

The tapped delay line (TDL) combination of a number of gates with well-defined delay times. The start signal is propagated through the buffers or inverters. When the stop signal arrives, the current state of the gates is recorded. The schematic of a TDL is given in Figure 1.9.

TDL offers a moderate resolution. The power consumption of the TDL is very low compared to previous solutions. It requires a small silicon area. The biggest challenge is to have a well-defined delay time.

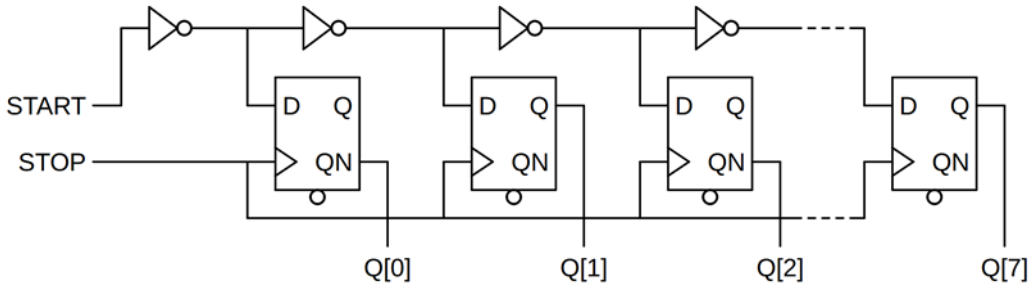



Figure 1.9. Schematic of a Tapped Delay Line (TDL).

### 1.4.5 Comparison of Different TDC Types

Comparison Different types of TDCs are compared in Table 1-1. The tapped delay line is more suitable for column-parallel TDC architectures due to the small layout area and high resolution.

Table 1-1. Comparison of different TDC types.

| TDC Type | Basic Counter | Ramp Interpolator | Vernier Interpolator | **Tapped Delay Line** |
|---|---|---|---|---|
| Resolution | Low | High | High | **Moderate** |
| Range | High | Moderate | Moderate | **Low** |
| Complexity | Low | Medium | High | **Low** |
| Silicon Area | Small | Medium | Large | **Small** |
| Power consumption | High | Low | Medium | **Low** |

## 1.5 Performance Parameter of a TDC

TDC performance parameters are similar to the ADC performance parameter. They can be summarized as follows.

- Time resolution: The smallest time interval that can be detected by the TDC. It defines the size of the LSB. It is in the order of picoseconds.

- Offset Error: The amount of difference between the ideal value and the recorded output. It can be expressed in terms of LSB. The offset can be canceled by measuring the reference time interval.

- DNL: The DNL error is defined as the difference between an actual step width and the ideal value of 1 LSB [21]. For an ideal TDC, each step equals 1 LSB, and the transition values are spaced exactly 1 LSB apart. The DNL results in 0 LSB. The DNL error is visualized in Figure 1.10.

- INL: The INL error is described as the deviation, in LSB or percent of full-scale range (FSR), of an actual transfer function from a straight line. The

INL-error magnitude then depends directly on the position chosen for this straight line. The INL error is visualized in Figure 1.10.

- TDC depth: The output samples are stored in binary form. So the resolution is expressed in binary depth. For example, TDC with a resolution of 8 bits can encode the data in $2^8 = 256$ levels. It defines the maximum count number and is represented by bits. The typical depth is 10 to 14 bits [11, 12].

- Sampling rate: The sampling rate for a TDC is defined as the number of output sampling in unit time.

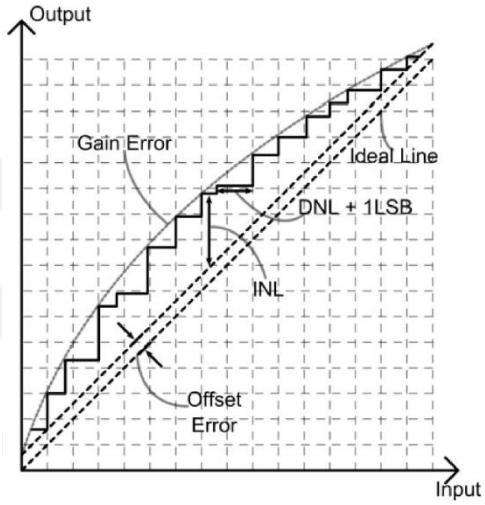



Figure 1.10. Visualization of INL and DNL [21].

## 1.6 The Motivation of the Thesis

Three-dimensional imaging is the key technology for different applications, such as advanced driving systems, augmented/virtual reality, and robotics. LIDAR systems offer promising solutions. It grows rapidly in the last decade with the standardization of the CMOS SPAD solutions.

This thesis's main purpose is to design and implement high precision, high speed, and low power consumption column-parallel TDC for SPAD-based LIDAR applications. The commercial LIDAR systems are using mechanically scanning

designs. That increases the fabrication and maintenance costs. The new technologies in CMOS fabrications such as APDs and SPADs, flash and rolling line LIDARs offer better resolution and low cost. They are available in conventional CMOS chip-level integration. It means that LIDAR sensors can be implemented in system-on-chip (SoC).

The column-parallel TDC is designed to be used with CMOS SPAD arrays. The TDC resolution is targeted 125ps (1.9cm resolution in distance). The maximum range of LIDAR is defined by the optical power of the system. The TDC maximum range is 1024ns (150m in the distance) which is larger than the typical optical range [3]. The aim of the sampling rate is 1MS/s. The objectives of the research can be summarized as in Table 1-2.

Table 1-2. Research objectives.

| | |
|---|---|
| CMOS tech. node (nm) | 180 |
| Pixel size (μm) | 26 |
| LSB (ps) | 125 |
| INL (LSB) | +0.5/-0.5 |
| DNL (LSB) | +0.5/-0.5 |
| Jitter (LSB) | < 0.5 |
| TDC Depth (bits) | 13 |
| Array size | 128 |
| Sampling rate | 1MS/s |
| Power consumption | 20mW |

## 1.7 Thesis Organization

In this thesis, design and implement high precision, high speed, and low power consumption column-parallel TDC for SPAD-based LIDAR applications is explained.

In Section 2, the system design of the TDC is discussed. The top design has three main sub-block, PLL, DLL, and TDL. Every sub-section is examined individually.

In Section 3, the implementation of the design is discussed. PLL and DLL blocks are explained, and simulation results are given individually. Under the column-parallel subsection, event-driven architecture (Stop Sampler), TDL, and memory are explained. The simulation results are given under each section. All the sub-blocks are brought together in the last sub-section. Top-level simulation results and floor planning is given under this section.

In Section 4, conclusions are made, and future works are discussed.

# CHAPTER 2

# SYSTEM DESIGN OF COLUMN PARALLEL TDC

In this chapter system-level design of the column-parallel TDC is analyzed. System-level investigation clarifies the operation of the design. Before going into implementation of the design, it has to be verified at the system level.

The first subsection explains the system-level operation. The top-level block diagram is given. The operation of the TDC is explained at the top-level together with the operations of the sub-blocks. The design has three major blocks; PLL, DLL, and TDL. Each block is investigated individually in a subsection.

## 2.1 Introduction

The top-level block diagram of the proposed column-parallel TDC is given in Figure 2.1. There are three main sub-blocks of the column-parallel TDC; a phase-locked loop (PLL), a delay-locked loop (DLL), and a tapped delay line (TDL).

The PLL multiplies the reference clock signal frequency and generates the necessary clock for the different sub-blocks. PLL's voltage-controlled oscillator (VCO) is a ring oscillator. It has four differential stages. The outputs of the stages are used as a DLL to have better timing resolution. They carried through all the columns. When the stop signal arrives, the current state of the outputs is recorded at the relevant column.

The TDL is used for the fine timing resolution. It contains a number of cells with well-defined delay times. Every column has a dedicated TDL. The delay cell of the TDL is a current starved inverter. A DLL is used to adjust the delay time of the current starved inverters. The DLL has the same current starved inverter as a delay

cell. The current starved inverter is biased in a DLL's closed loop. So the inverter does not suffer from process, voltage, and temperature (PVT) variations. The bias voltage is copied to the current starved inverters at the columns. In that way, TDL delay cells have well-defined delay times, and they are continuously corrected by the DLL.

A counter is used to increase the time difference input range. It is an 8 bit counter. The counter clock is two times faster than the system clock. The LSB of the counter is used for synchronization. The outputs of the counter are carried through all the columns. When the stop signal arrives, the current state of the outputs is recorded at the relevant column.

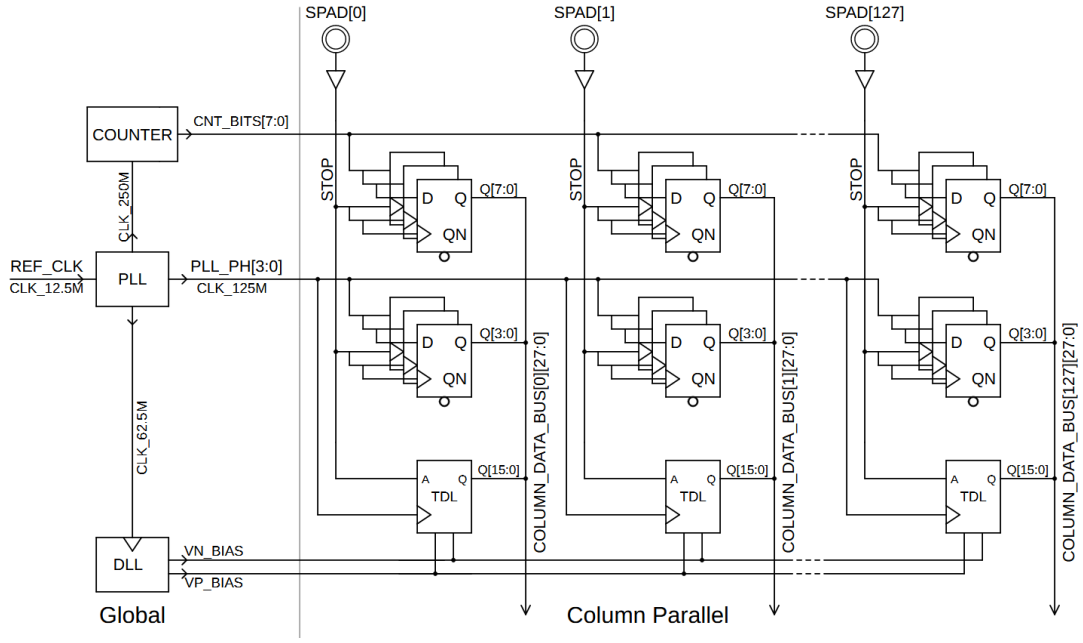



Figure 2.1. Top-level block diagram of the proposed column-parallel TDC.

## 2.2 Phase-Locked Loop (PLL)

Phase-locked loop (PLL) frequency synthesizers are used in a wide variety of applications. It decreases the phase noise and allows to work with high-frequency signals in high precision.

A PLL is a negative feedback system. It is a combination of a voltage-controlled oscillator (VCO), a frequency divider, and a phase detector. The VCO signal's frequency is divided by a frequency divider, and it maintains a phase – lock with the reference signal. In this thesis, PLL is used to generate low noise and a high-frequency clock signal from a fixed low-frequency clock signal. The PLL can be analyzed in general as a negative-feedback system with a forward gain term and a feedback term. A simple block diagram for such a system is given in Figure 2.2.

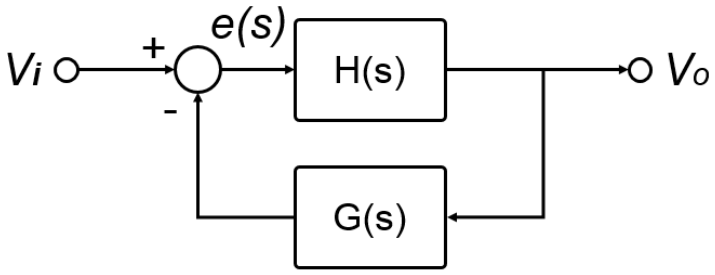



Figure 2.2. Negative-feedback control system model.

$$Closed - Loop\ Gain = \frac{H(s)}{1 + G(s)H(s)} \tag{2.1}$$

### 2.2.1 PLL Building Blocks

The schematic of the charge-pump integer-N PLL is given in Figure 2.3. The PLL has five main blocks; a phase-frequency detector (PFD), a charge-pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO), and a frequency divider [22].

The operation of each block can be summarized as follows:

- The PFD detects the phase and frequency differences and drives the CP.
- The CP injects or drains the charge to the LF and determines the control voltage ($V_{CTRL}$).
- The LF eliminates the high-frequency component that is coming from the loop and the CP. The output voltage of the loop filter $V_{CTRL}$ drives the VCO.
- VCO creates the output signal.
- The frequency divider divides the output signal's frequency into the range of input frequency [24].

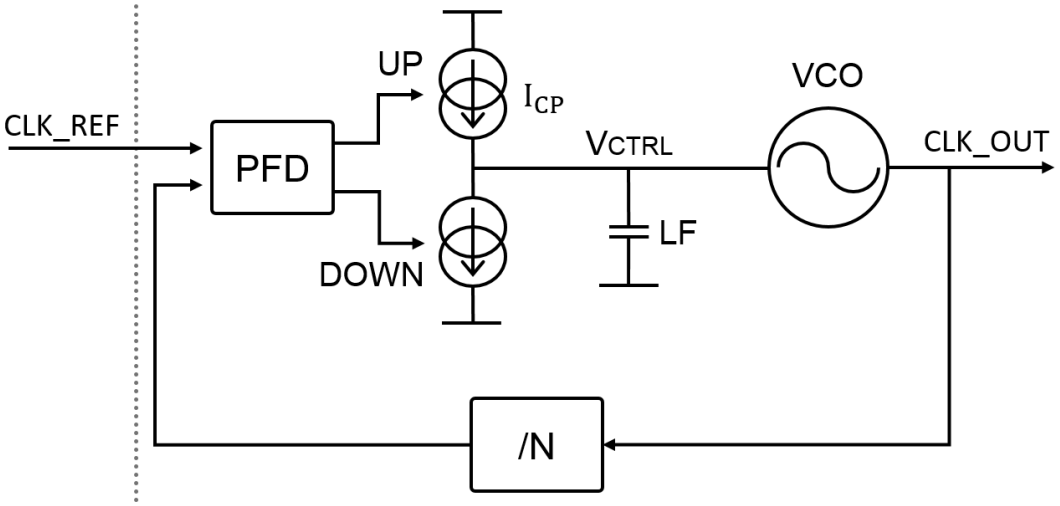



Figure 2.3. Block diagram of charge-pump integer-N PLL.

**Phase - Frequency Detector**

The phase-frequency detector can detect both phase and frequency differences. In Figure 2.4 REF signal and CLK signal has different frequency and phase. DC content of the PFD output UP and DOWN provide information about phase and frequency difference.

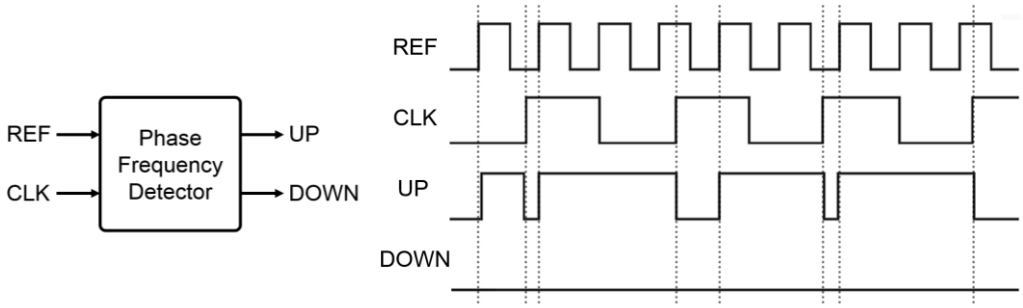



Figure 2.4. Phase-Frequency Detector (PFD) and response to phase and frequency error.

**Charge Pump**

The charge pump injects or drains the charge to the loop filter. The phase-frequency detector generates UP and DOWN according to the phase and frequency difference between REF and CLK signals. UP signal injects charge into the loop filter, and DOWN signal drains charge from it.

In Figure 2.5 schematic of the charge-pump is given. Two independent current sources are connected in cascode. The average charge is injected through the output node.

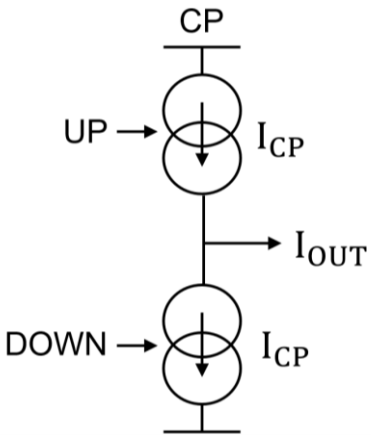


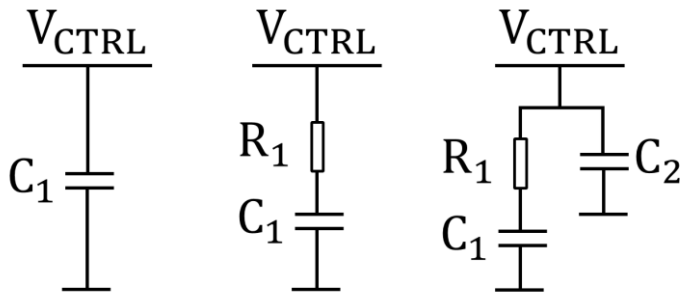

Figure 2.5. Block diagram of charge-pump.

**Loop Filter**

The loop filter is a low pass filter. It converges the current coming from the charge pump into a voltage. The loop filters voltage, $V_{CTRL}$, drives the voltage-controlled oscillator (VCO).

The phase detector produces repetitive pulses at its output, modulating the VCO frequency and generating large sidebands. Therefore low pass characteristic loop filter needs to be introduced between the PFD and the VCO to suppress high-frequency sidebands [22].

The simple loop filter is given in Figure 2.6 (a). It performs an integration operation. But the loop has another perfect integrator, the VCO. So the additional perfect integrator in the loop makes the system unstable and leads to oscillatory behaviors. A resistor is placed in series with an integrator capacitor, in Figure 2.6 (b), to prevent such behavior. This adds a zero to the loop filter's trans-impedance function and stabilizes the system [23]. This arrangement is called a type-II PLL because its open-loop transfer function contains two poles at the origin (i.e., two ideal integrators) [22].




(a) (b) (c)

Figure 2.6. . (a) Simple loop filter (b) resistor added to stabilize the system (c) additional capacitance added to reduce ripple.

The loop filter consisting of $R_1$ and $C_1$ in Figure 2.6 (b) does not suppress the ripple sufficiently. Due to the propagation mismatches within the PFD, small positive and

negative pulses are generated. Since the $I_{CP}R_1$ voltage is large, an additional mechanism to reduce the ripple becomes necessary. A simple approach is to connect an additional capacitor between control and ground lines in Figure 2.6 (c). It provides a low-impedance path for the ripple outputs. A small current pulse is generated by CP initially flows through $C_2$. After the CP turns off, $C_2$ begins to share its charge with $C_1$ through $R_1$ [22].

**Voltage Controlled Oscillator (VCO)**

An oscillator generates a periodic output. As such, the circuit must involve a self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal [22].

In Figure 2.7 ideal characteristic of a VCO is shown. The output frequency changes between $w_1$ to $w_2$ according to $V_{CTRL}$ in a certain tuning range. The slope characteristic is called the gain of the VCO and is represented as $K_{VCO}$. It is desired that $K_{VCO}$ does not change significantly in the tuning range [22].

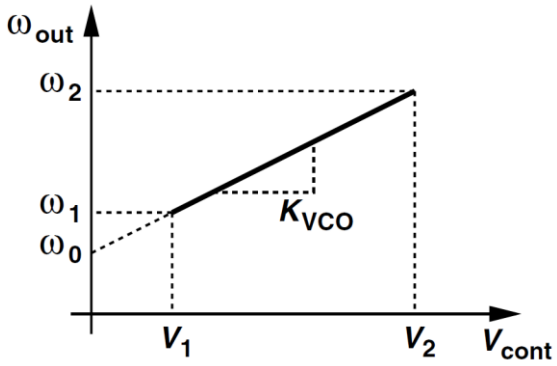



Figure 2.7. Ideal VCO characteristics [22].

$$K_{VCO} = dw_{VCO}/dV_{CTRL} \tag{2.2}$$

$K_{VCO}$ is the derivative of $w_{out}$ respected to control voltage, $V_{CTRL}$. Since the phase is the integral of the frequency, the output phase of the VCO can be represented as (2.3):

$$\emptyset_{VCO} = \int K_{VCO}.V_{CTRL}.dt \qquad [24]\ (2.3)$$

The VCO in the frequency domain (s-domain) is modeled as (2.4):

$$\frac{\emptyset_{VCO}}{V_{CTRL}}(s) = \frac{K_{VCO}}{s} \qquad [24]\ (2.4)$$

A CMOS ring oscillator is shown in Figure 2.7. It is an example of voltage controlled oscillator. A VCO is a self-oscillatory system; it has no input. VCO oscillation is controlled by the bias voltage/current of the inverters. VCO determines the phase and the frequency of the PLL. So that, phase and the frequency of the PLL are adjustable.

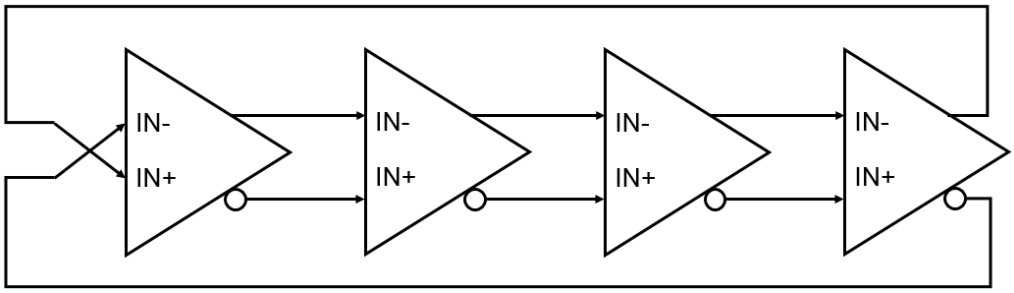



Figure 2.8. Ring oscillator. Barkhausen criteria result in oscillatory behavior.

In ring-oscillators, loop gain is higher than unity, and the phase difference is 180 degrees. Barkhausen criteria result in oscillatory behavior. The output voltage grows exponentially and saturates at a certain level. Consider the three CMOS inverters connected in cascade in Figure 2.8. The phase difference of the loop is 180 degrees. Each stage is identical and contributes 45 degrees of phase shift. Inverters work as an amplifier in this system; oscillation amplitude grows rapidly until the transistors enter a triode region. That decreases the gain of each stage, and the system oscillates between VDD and GND [26]. Output waveforms of the ring oscillator stages are given in Figure 2.9.

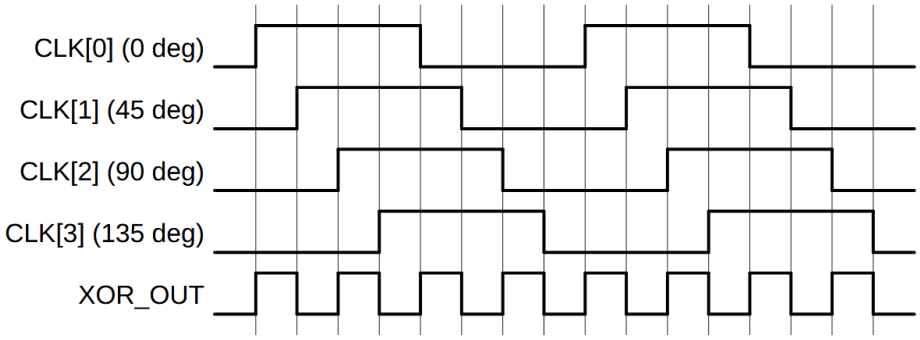



Figure 2.9. Output waveforms of the ring oscillator stages.

**Frequency Divider**

The reference clock of the PLL is generated by a crystal oscillator. The operation frequency of the crystal oscillator typically less than the VCO frequency. For proper phase and frequency detection, VCO frequency needs to be divided in the order of the crystal oscillator operation frequency range. The VCO frequency is divided by the frequency divider.

### 2.2.2 PLL Loop Characteristics

The open-loop transfer function of the charge-pump PLL is given in (2.5). It can be written as a combination of each component. The explicit version of the function is given in (2.6).

$$H_{open}(s) = F_{pfd}(s) * F_{cp}(s) * F_{lf}(s) * F_{vco}(s) \tag{2.5}$$

$$H_{open}(s) = \frac{I_{cp}(s)}{2\pi} * \left(\frac{1}{C_1 s} + R_1\right) * \frac{K_{vco}}{s} \tag{2.6}$$

The PLL is a negative-feedback control system. Its model is given in Figure 2.2. The open-loop transfer function, H(s), of the system is given in (2.6), and the feedback transfer function of the system, G(s), is 1/M. Put them into (2.1) and get the system's overall closed-loop transfer function in (2.7).

Note that a second capacitor, $C_2$, is introduced in the loop filter section. But it is not mentioned in (2.7). This because of simplicity. Introducing another capacitor to the system adds an additional pole to the system. Additional pole frequency is chosen high enough not to disturb the loop characteristics and only filter the charge pump's ripple outputs. It will further mention in the "PLL Design Procedure" section.

$$H_{closed}(s) = \frac{\frac{I_p K_{VCO}}{2\pi C_1}\,(R_1 C_1 s + 1)}{s^2 + \frac{I_p}{2\pi}\frac{K_{VCO}}{M} + \frac{I_p}{2\pi C_1}\frac{K_{VCO}}{M}} \qquad [22]\ (2.7)$$

The loop transfer function can be studied as follows. The denominator of (2.7) can be written as $s^2 + 2\zeta\omega_n + \omega_n^2$ where $\zeta$ is the damping ratio. Chose the damping ratio $1/\sqrt{2} < \zeta \leq 1$ for critically-damped response and $1 \ll \zeta$ for an overdamped response. The damping ratio is given in (2.8).

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p C_1 K_{VCO}}{2\pi M}} \qquad [22]\ (2.8)$$

The natural frequency, $\omega_n$, is given in (2.9). It determines the bandwidth of the system.

$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1 M}} \qquad [22]\ (2.9)$$

The poles of the closed-loop transfer function of the system are given in (2.10).

$$\omega_{p1,2} = \left[-\zeta \pm \sqrt{\zeta^2 - 1}\right]\omega_n \qquad [22]\ (2.10)$$

The closed-loop zero of the system is given in (2.11).

$$\omega_{zero} = \frac{\omega_n}{2\zeta} \qquad [22]\ (2.11)$$

Let us chose the $\zeta = 1$, where it will perform a critically damped response. In that case, closed-loop zero will be located at $\omega_{zero} = \omega_n/2$ and both poles

at $\omega_{p1,2} = \omega_n$. The transfer function of such a system is given in Figure 2.10. Note that in that case, "zero" of the system is located before the "poles." In fact, it is true all the time when the system is critically or overly damped. The system gain starts increasing when it encounters the zero, and it will keep constant after the first pole. Then it will start to decrease after the second pole. The system has some gain in low frequencies, and the gain decreases dramatically after the second pole, which is the very familiar low-pass characteristic.

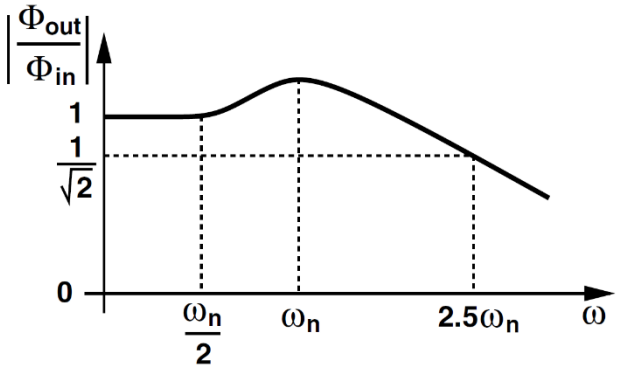



Figure 2.10. The closed-loop frequency response of the charge pump PLL (damping ratio is ζ=1) [22].

### 2.2.3 PLL Phase Noise

In the previous chapter, it is found that the closed-loop frequency response of the charge pump PLL has low pass characteristics. A typical crystal oscillator has a flat noise profile. The overall behavior is shown in Figure 2.11[22].

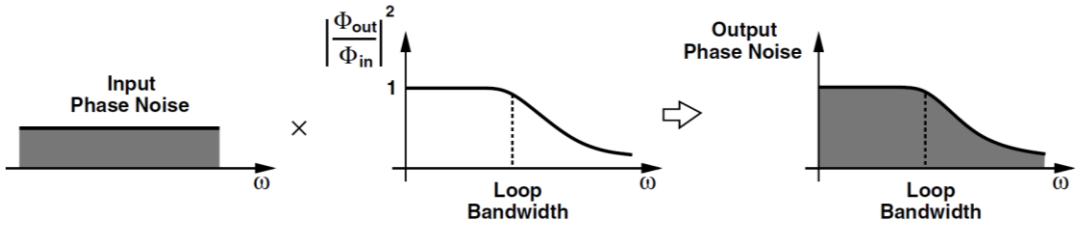



Figure 2.11. Effect of reference phase noise in a PLL.

Let’s assume that the input phase noise is equal to zero and only has the VCO phase noise. In this case, the phase-model can be written as in Figure 2.12 [22].

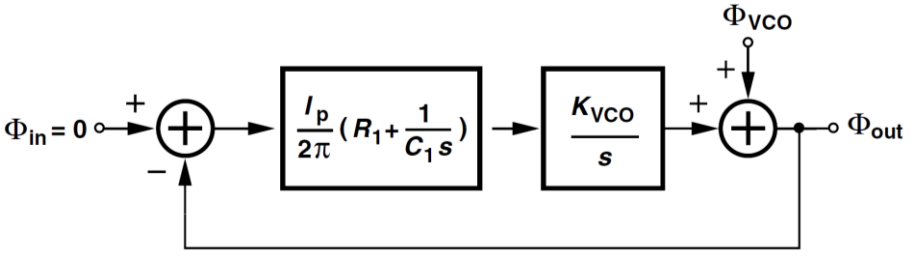



Figure 2.12. Phase-domain model for VCO phase noise.

The transfer function of the system given in the figure can be written as in (2.12).

$$\frac{\emptyset_{out}}{\emptyset_{VCO}} = \frac{s^2}{s^2 + 2\zeta\omega_n + \omega_n^2} \quad [22] \ (2.12)$$

The closed-loop response of the model has two zero at the origin and two poles, same with (2.7). The frequency response of the phase model of VCO is shown in Figure 2.13 [22]. It is resulting in a high pass response.

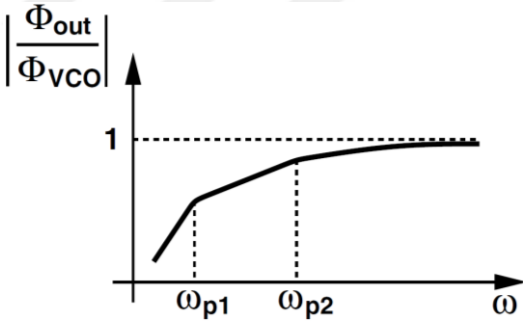



Figure 2.13. Frequency response for the phase model of VCO.

The phase noise of the free-running VCO is given in Figure 2.14. For the closed-loop noise contribution of the VCO, the transfer function given in (2.12) shapes the VCO phase noise as in Figure 2.14.

The reference noise contribution increases with increasing loop bandwidth. On the contrary, the phase noise contribution of VCO increases with decreasing loop bandwidth. So while choosing the bandwidth, there is a trade-off between reference and VCO phase noise contribution.

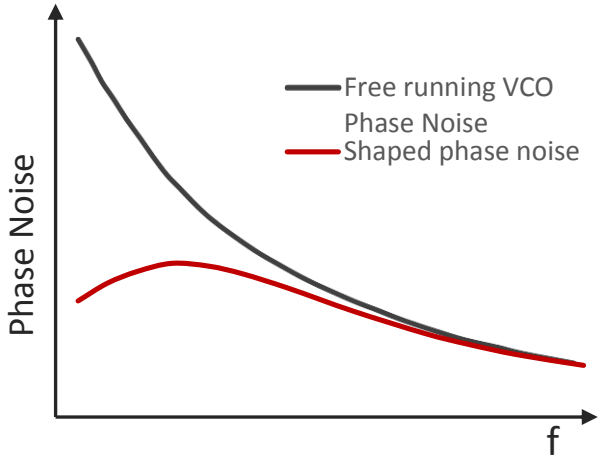



Figure 2.14. Reference and shaped VCO phase noise in a PLL.

The minimum overall noise contribution is achieved by critically damping $\zeta = 1$. In that case, both poles will be equal to $\omega_n$, and loop bandwidth at $2.5\omega_n$ . The phase noise contribution of reference and VCO is given separately in Figure 2.15. The reference noise has low pass characteristics, and the VCO noise has high pass characteristics [23].

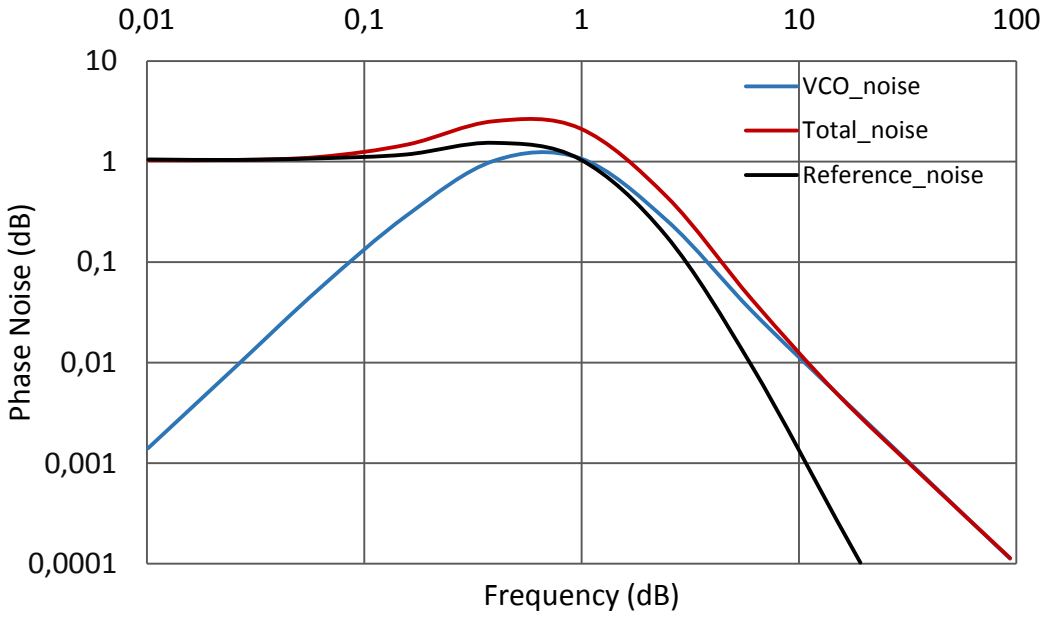



Figure 2.15. The noise sources of the PLL. The reference noise has low pass characteristics, and the VCO noise has high pass characteristics.

### 2.2.4 PLL Loop Bandwidth

Charge-pump PLLs are discrete-time (DT) systems. Because the charge pump turns off for part of the period and breaks the loop. For that reason, the previous observations hold only if the internal states do not change rapidly.

The time constant of the loop should be much less than the input signal period. If it is not, the loop can show underdamped behavior or may not lock.

To be able to make the continuous-time approximation, set the loop bandwidth to approximately one-tenth of $\omega_{in}$[27]. In (2.13), the loop bandwidth is given for critically damped response and in (2.14) overdamped response [22].

$$2.5\omega_n \ll \omega_{in}, \qquad \zeta = 1 \tag{2.13}$$

$$2\zeta\omega_n \ll \omega_{in}, \qquad \zeta^2 \gg 1 \tag{2.14}$$

### 2.2.5 PLL Design Procedure

In the previous chapter, it is proven that the loop should be critically damped for minimum phase noise. The damping ratio, $\zeta$ is equal to 1; it is given in (2.15).

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p C_1 K_{VCO}}{2\pi M}} \qquad [22] \tag{2.15}$$

The bandwidth is equal to $2.5\omega_n$ for critically damped, the $\omega_n$ is given in (2.16).

$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1 M}} \qquad [22] \tag{2.16}$$

The $K_{VCO}$ is known, and $I_P$, $R_1$, and $C_1$ have to be found. But there are two equations and three unknowns, so the equation is not unique. The parameters should be chosen according to the footprint and power consumption. In general, the $I_P$ is in the order

of few tens microamperes; after selecting $I_P$, $C_1$ and $R_1$ can be found. Lastly, the second capacitor $C_2$, is chosen according to $C_1$ as in (2.17).

$$C_2 = 0.2 * C_1 \quad [22] \quad (2.17)$$

## 2.3 Delay Locked Loop (DLL)

A delay-locked loop (DLL) is a phase-locked timing circuitry that is similar to a phase-locked loop (PLL). The main difference is that the voltage-controlled oscillator (VCO) is replaced with a voltage-controlled delay line.

A DLL has a series of delay blocks. Each block identical to the others and has the same amount of delay. There are N numbers of copies of the input signal, which has an equal phase difference between them. The input reference signal is delayed N times, and the total delay time is equal to the input signal period.

A DLL is generally used for fine timing purposes. The input signal is delayed N times by DLL, and fine timing resolution is achieved. In some applications carrying the high-frequency clock signal is not practical. The capacitive load of the bus will be very high. The signal strength will decrease through the bus. It needs to be repeated for a couple of 100um's. In that case, power consumption will be very high due to high frequency and repeaters. Instead of increasing the frequency, copies of a signal with the same phase differences can be used.

In this study, carrying the DLL outputs could give good timing resolution. But it is unpractical because of the routing of the output signals. It requires a large layout area. Instead, a TDL is used for the fine timing resolution. The TDL's delay cell is the same as the DLL's delay cell. Instead of carrying the DLL outputs, the bias voltage for the delay cell is carried. A TDL line is located at every column. It simplifies the layout and decreases the required silicon area.

### 2.3.1 DLL Building Blocks

The schematic of the charge-pump DLL is given in Figure 2.16. It has 5 main blocks; a phase-frequency detector (PFD), a charge-pump (CP), a loop filter (LF), and a voltage-controlled delay line (VCDL).

The reference signal and the $N^{th}$ output of the DLL have the same phase. PFD checks the phase difference between these two signals and drives the CP. CP injects or drains charge to the LF. The LF's output voltage, $V_{CTRL}$, controls the delay time of the VCDL.

DLL and PLL have very similar blocks. PFDs have very similar architecture, and CPs are the same. LFs are different because the VCDL does not introduce any pole to the transfer function; there is no need for a complicated filter. The schematic of the system is given in Figure 2.13[28].

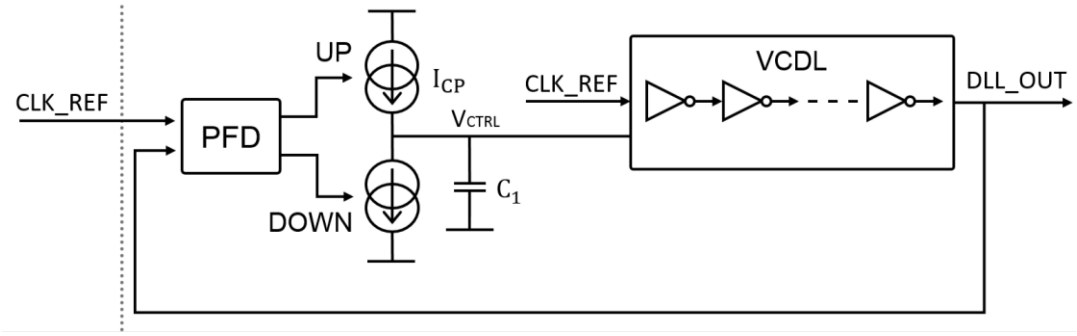



Figure 2.16. Block diagram of charge-pump DLL.

**Phase - Frequency Detector (PFD)**

The PFD of the DLL has the same architecture as the one in the PLL. In the previous chapter, it is mentioned that PFD can detect both phase and frequency. In DLL, the output signal has exactly the same frequency as the input frequency; only the change is the phase. In DLL, PFD is only used as a phase detector.

The phase-frequency detector can detect both phase and frequency differences. In Figure 2.17, REF signal and CLK signals have the same frequency and different phases. DC content of the PFD output UP and DOWN provide information about phase difference.

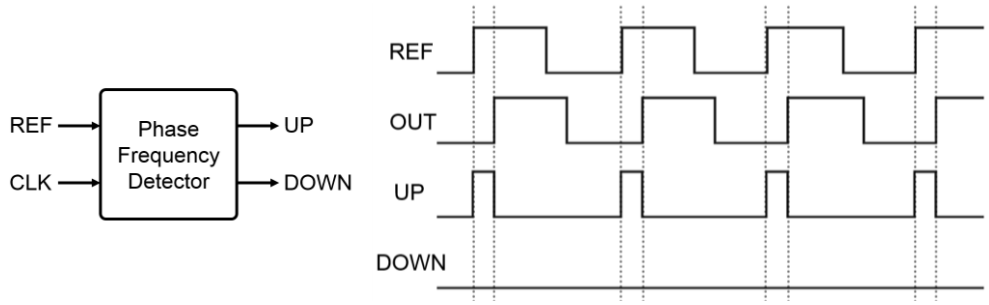



Figure 2.17. PFD phase difference response.

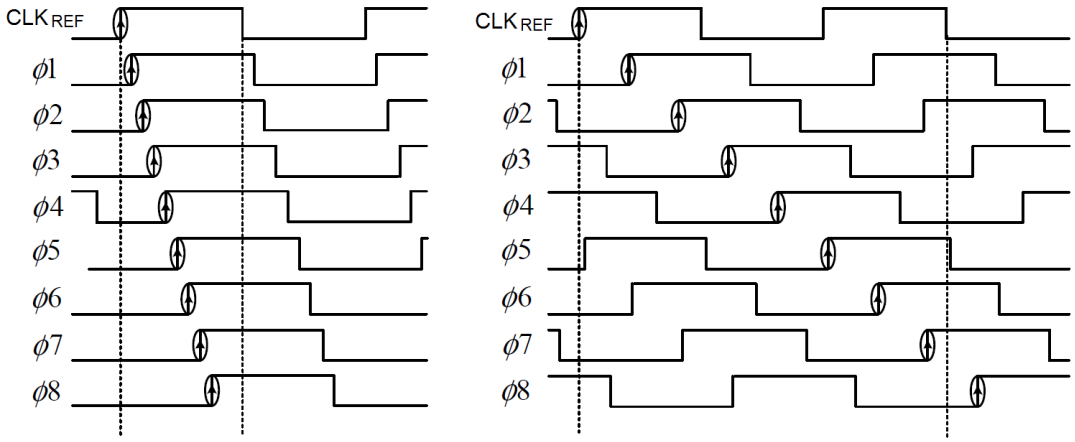



Figure 2.18. The lock failure cases (a) when TD is smaller than 0.5TCLK and (b) TD is greater than 1.5TCLK.

The frequency does not change in DLL. $CLK_{REF}$ and $CLK_{DLL}$ signals have exactly the same frequency all the time. $CLK_{DLL}$ is one period delayed copy of $CLK_{REF}$. They have a 360-degree phase difference. The PFD keeps the phase at $2\pi$. But DLL fails to lock if $T_{DELAY}$ is less than 0.5 $T_{CLK\_REF}$ or $T_{DELAY}$ is higher than 1.5 $T_{CLK\_REF}$. In the first case, the delay time is very short so that the $CLK_{REF}$ appears before the $CLK_{DLL}$, so that the loop tries to decrease the delay time furthermore. The DLL tries to lock at 0 phase difference. As a result, the loop fails to lock. In the second case opposite of the first case occurs. The delay time is so large that the $CLK_{DLL}$ appears

before the CLKREF. The loop tries to increase the delay time and locks the second or higher period of the $CLK_{REF}$ [29].

**Charge Pump (CP)**

The charge pump injects or drains the charge to the loop filter. The charge pump of the DLL is exactly the same as the one in the PLL. Please refer to Chapter 2.2.1 for further information.

**Loop Filter (LF)**

The loop filter of the DLL has a similar characteristic to the one in the PLL. It is a low pass filter. It integrates the charge coming from the charge pump. The loop filter's output voltage, $V_{CTRL}$, controls the voltage-controlled delay line (VCDL).

The PFD produces repetitive pulses at its output, modulating the VCDL phase and generating phase noise. Therefore, a low pass characteristic loop filter needs to introduce between the PFD and the VCDL to suppress high-frequency sidebands, which is a similar case with PLL.

DLL only has one integrator, the loop filter. It has one pole, and it is coming from the loop filter. So that DLL does not suffer from oscillatory behavior, which is a critical design concern for PLL. The loop filter of the DLL is given in Figure 2.18. It is the most basic low pass filter. Just shunt capacitance to $V_{CTRL}$ [30].

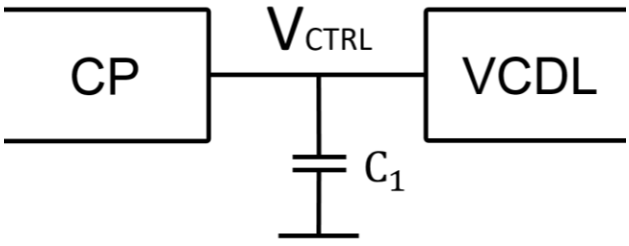



Figure 2.18. DLL loop filter, located between CP and VCDL. It filters the high-frequency sidebands of CP.

**Voltage Controlled Delay Line (VCDL)**

The voltage-controlled delay line has an N-number of series delay cells. Every cell is equal to each other, and all have the same amount of delay. The input reference clock is propagated by each cell, and the total delay is equal to one reference clock period. The delay of each cell is voltage controlled.

The delay cell is a current-controlled inverter. The output current is controlled by the $I_{BIAS}$ node. When the output current increases, the charge time of the output load capacitance decreases. Stages are connected in cascade, and each stage has the same output load. The schematic of the VCDL is given in Figure 2.19.

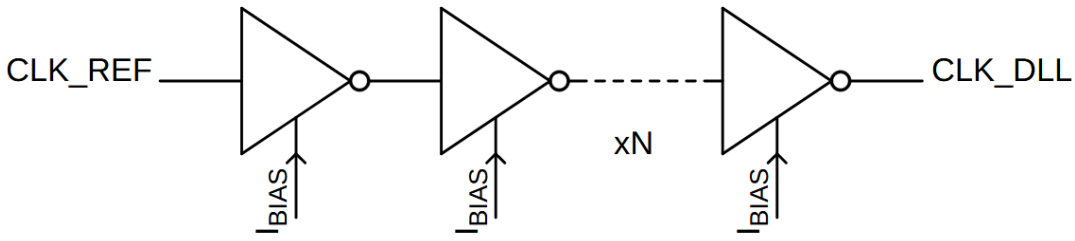



Figure 2.19. Schematic of voltage-controlled delay line (VCDL).

The open-loop transfer function of the charge-pump DLL is similar to the charge-pump PLL, but it is simpler. It is the combination of each component's transfer function (2.17). The explicit version is given in (2.18).

$$H_{open}(s) = F_{PFD}(s) * F_{CP}(s) * F_{LF}(s) * F_{VCDL}(s) \tag{2.17}$$

$$H_{open}(s) = \frac{I_{cp}(s)}{2\pi} * \left(\frac{1}{C_1 s}\right) * K_{VCDL} \tag{2.18}$$

The DLL is a negative-feedback control system. It is modeled as in Figure 2.2, the same as the PLL. The open-loop transfer function, H(s), of the system is given in (2.18), and the feedback transfer function of the system, G(s), is 1. Put them into (2.1) and get the overall closed-loop transfer function of the system in (2.19).

$$H_{closed}(s) = \frac{\frac{I_p K_{VCDL}}{2\pi C_1}}{s + \frac{I_p K_{VCDL}}{2\pi C_1}} \tag{2.19}$$

$$\omega_p = \frac{I_p K_{VCDL}}{2\pi C_1} \tag{2.20}$$

The loop has only one pole, given in (2.20), and does not have a zero. Because it is one pole system, it does not suffer from oscillatory behavior. The pole directly determines the bandwidth. The loop has low pass characteristics. The input noise is multiplied by the transfer function. The closed-loop frequency response of the charge pump DLL is given in Figure 2.20.

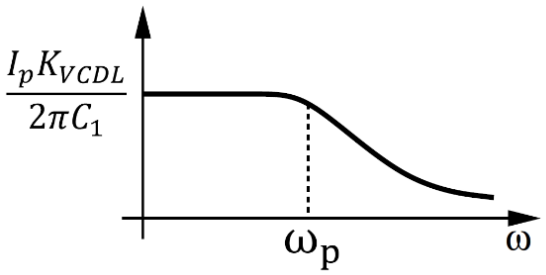



Figure 2.20. The closed-loop frequency response of the charge pump DLL.

In this study, PLL output is the input of the DLL. If the bandwidth of the DLL is much smaller than the PLL, the noise contribution of the PLL will decrease.

### 2.3.2 DLL Phase Noise

The closed-loop transfer function of the DLL is similar to the charge pump PLL. The DLL has low pass characteristics. The input noise is filtered, and the higher frequency noises will be filtered through the output as in Figure 2.11.

The VCDL phase noise does not filter by the loop. It will be dominant at a high frequency. Let's find the VCDL phase noise contribution to the output phase noise. Assume that the input phase noise is equal to zero and only has the VCDL phase noise. In this case, the phase-model can be written as in Figure 2.21.

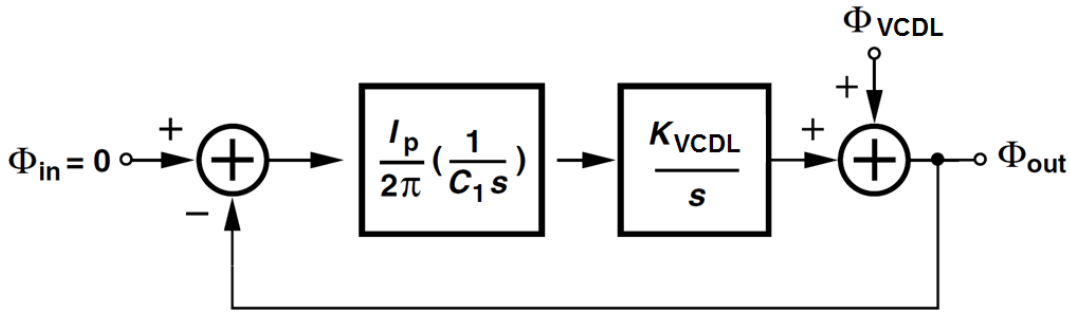



Figure 2.21. Phase-domain model for VCDL phase noise.

The transfer function of the system given in the figure can be written as in (2.21).

$$\frac{\emptyset_{out}}{\emptyset_{VCO}} = \frac{s}{s + \omega_p} \tag{2.21}$$

The closed-loop response of the model has one zero at the origin and one pole same with (2.20). The frequency response of the phase model of VCDL is shown in Figure 2.22. It is resulting in a high pass response [30].

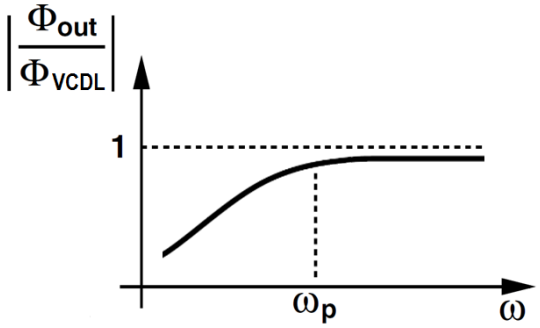



Figure 2.22. Frequency response for the phase model of VCDL.

The VCDL phase noise contribution increases with increasing loop bandwidth; on the contrary, the reference noise contribution increases with increasing loop bandwidth. So while choosing the bandwidth, there is a trade-off between reference and VCDL phase noise contribution.

### 2.3.3 DLL Loop Bandwidth

Charge-pump DLLs are discrete-time (DT) systems because the charge pump turns off for part of the period and breaks the loop. For that reason, the previous observations hold only if the internal states do not change rapidly.

The time constant of the loop should be much less than the input signal period. If it is not, the loop can show underdamped behavior or may simply not lock.

To be able to make the continuous-time approximation, set the loop bandwidth to approximately one-tenth of $\omega_{in}$. The bandwidth of the system is equal to the pole position (2.22). So that $\omega_p$ must be much smaller than $\omega_{in}$(2.23).

$$BW = \omega_p \tag{2.22}$$

$$\omega_p \ll \omega_{in} \tag{2.23}$$

### 2.3.4 DLL Design Procedure

The design procedure for the charge-pump DLL is much simpler compared to the charge-pump PLL. The DLL has only one pole and no zero so that the system is always stable. The only consideration is that the continuous-time approximation that is mentioned in the previous section. The pole location and input frequency are given in (2.24).

$$0.1\omega_{in} = \omega_p = \frac{I_p K_{VCDL}}{2\pi C_1} \tag{2.24}$$

The $K_{VCDL}$ is known. In general, the $I_P$ is in the order of few tens microamperes; after selecting $I_P$, $C_1$ can be found.

## 2.4 Tapped Delay Line (TDL)

The tapped delay line is similar to the VCDL line in DLL. It contains a number of cells with well-defined delay times. It has “START” and “STOP” inputs. The start signal is propagated through the delay cells. When the stop signal arrives, D-flip-flops records the current state of the delay cells [31]. The block diagram and the input and output waveforms of a simple TDL are given in Figure 2.23.

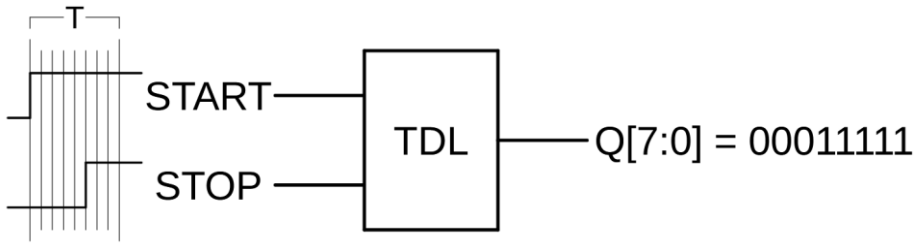



Figure 2.23. Simple tapped delay line (TDL) with input and output waveform.

The TDL has a series of inverters as delay cells. The gate delay time defines the resolution of the TDL. The inverters are the current starved inverters. They have a very precise delay time. The delay is controlled by a DLL. It will not suffer from PVT variations.

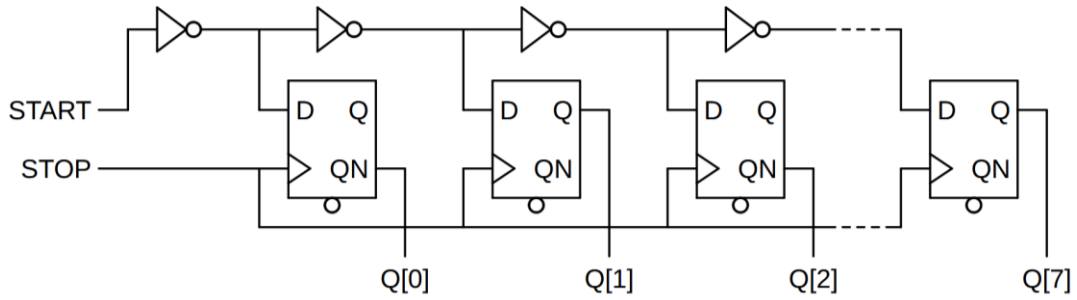



Figure 2.24. The tapped delay line (TDL) schematic.

The schematic of the tapped delay line is given in Figure 2.24. It has two inputs, “START” and “STOP.” Initially, these two signals are connected to “0” logic. Even inputs of the D flip-flops have logic “1” inputs (D[0], D[2], D[4], D[6]) and the odd inputs have logic “0” inputs (D[1], D[3], D[5], D[7]). When the start signal turns to

logic “1”. The even inputs of the D flip-flops turn to logic “0” and the odd inputs of the D flip-flops turn to logic “1”. The even-numbered outputs are connected to the inverted output (QN[N]), and the odd-numbered outputs are connected to the non-inverted outputs (Q[N]) of the D-flip-flops.

The tapped delay line consists of series inverters and D-flip-flops. The architecture is easy to implement at the column level.

# CHAPTER 3

# IMPLEMENTATION OF THE COLUMN PARALLEL TDC

In this chapter, the implementation of the column-parallel TDC is explained. The simulation results and the layout of each sub-block are given in the chapter. The operation and design specifications are verified.

The first subsection explains the top-level schematic of the design. It explains the connectivity between the blocks. The next subsections explain the three major sub-blocks; PLL, DLL, and column-parallel TDC.

## 3.1 Introduction

The top schematic of the proposed column-parallel TDC is given in Figure 3.1. The top-level is investigated under three main sub-blocks; phase-locked loop (PLL), delay-locked loop (DLL), and column-parallel TDC.

The reference clock frequency is 12.5MHz. PLL multiplies the reference clock signal by 10. At the output, PLL generates a 125MHz system clock. The PLL has a ring oscillator as a VCO. It has four stages. Outputs of the stages are used as a DLL. They carried through all the columns.

The counter LSB has the same frequency as the system clock, 125MHz. It is necessary for synchronization with the PLL. The 250MHz clock signal frequency is needed for the counter. The first and the third output of the PLL are multiplied with an XOR gate, and a 250MHz clock is generated for the counter.

The TDL contains a number of current starved inverted, which have well-defined delay time. The delay time is controlled by the DLL. A fast clock is needed for TDL. A faster clock signal decreases the number of stages in the TDL. The PLL outputs are multiplied with a 4-input XOR gate, and a 500MHz clock is generated.

The DLL suffers from the high-frequency input signal. It cannot perform well with the system clock frequency. At the input of the DLL, system clock frequency is divided by 2. The DLL works with a 62.5MHz clock signal. The DLL has the same current starved inverter as the TDL. The current starved inverter is biased in a DLL's closed loop. So the inverter does not suffer from process, voltage, and temperature (PVT) variations. The bias voltage is copied to the TDL's current starved inverters at the columns.

The outputs of the counter and the PLL are carried through all the columns. When the stop signal arrives, the outputs' current state is recorded with D-flop-flops at the relevant column.

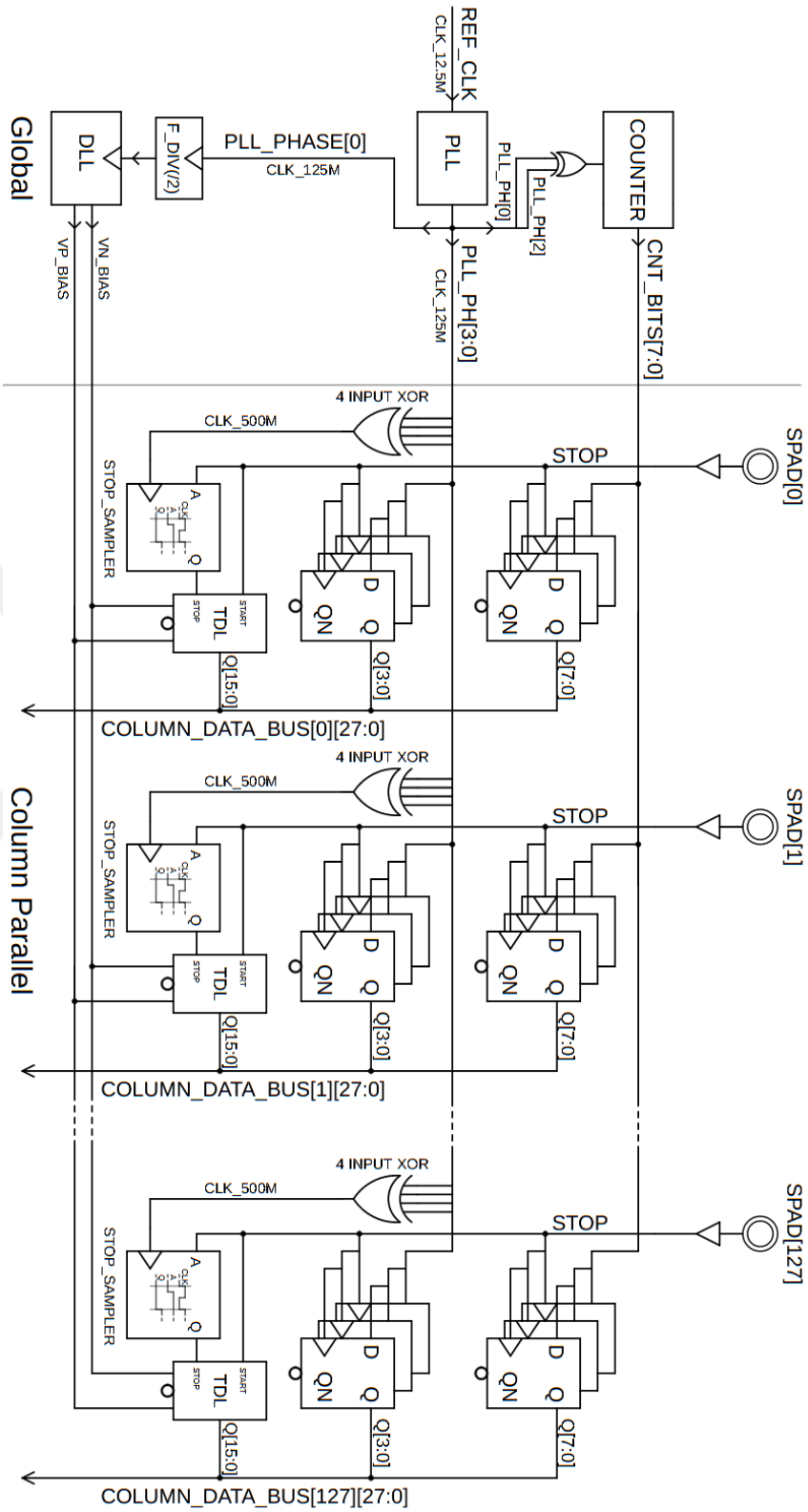



Figure 3.1. Top-level block diagram of the proposed column-parallel TDC.

### 3.2 Phase-Locked Loop (PLL)

The block diagram of the PLL is given in Figure 3.2. In Chapter 2.2.5 the design procedure of the charge-pump PLL is explained. Let us recall it briefly.

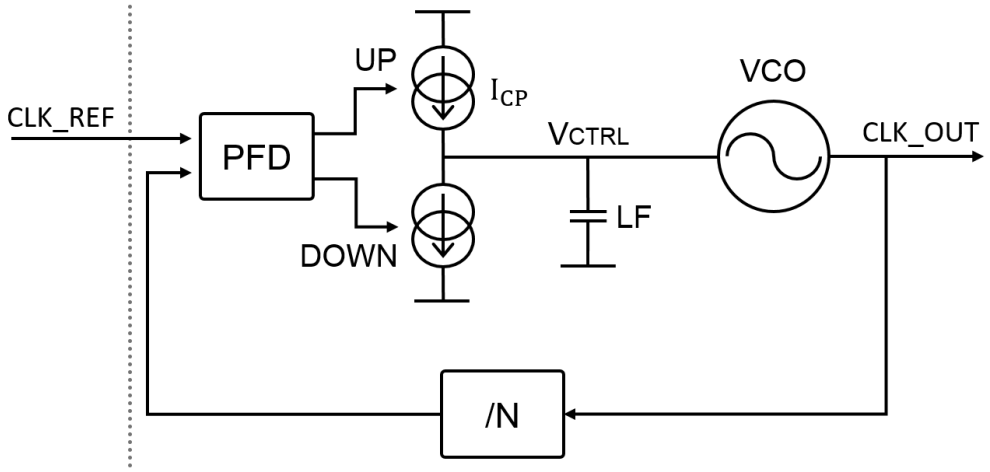



Figure 3.2. The block diagram for the PLL.

The best noise performance is achieved with the critically damped response. The damping ratio, $\zeta$ is equal to 1, the bandwidth results to $2.5\omega_n$ for the critically damped response. In equation (3.1), the damping ratio $\zeta$ and in (3.2) the natural frequency $\omega_n$ is given explicitly.

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p C_1 K_{VCO}}{2\pi M}} \qquad [22]\ (3.1)$$

The bandwidth is equal to $2.5\omega_n$ for the critically damped response, and the bandwidth is one-tenth of the input frequency.

$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1 M}} \qquad [22]\ (3.2)$$

Before going into calculation first, the $K_{VCO}$ needs to be found. After that, the $I_P$, $R_1$, and $C_1$ have to be calculated. There are three unknown but two equations for this calculation so that the parameters are not unique.

### 3.2.1 PLL Building Blocks

The charge-pump integer-N PLL has five main sub-block; a phase-frequency detector (PFD), a charge-pump (CP), a loop filter (LF), voltage-controlled oscillator (VCO), N frequency divider [22]. Each block is explained separately in the following.

**Voltage Controlled Oscillator (VCO)**

The VCO is a ring oscillator. Every stage is a differential amplifier. Each stage has a finite gain. At the last stage, the negative output node is connected to the positive input node, and the positive output node is connected to the negative input. That keeps the phase difference constant at 180 degrees. The gain at every stage is higher than 1. Barkhausen Criteria results in oscillatory behavior for the loop. The block diagram of a ring oscillator is given in Figure 3.3.

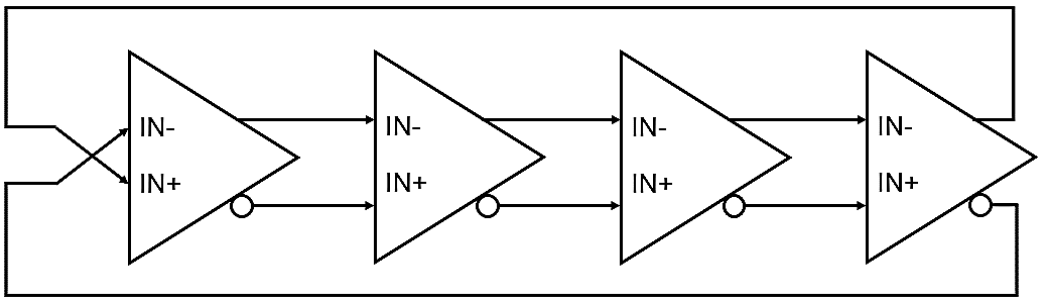



Figure 3.3. Block diagram of a 4 stage ring oscillator.

The transistor-level schematic of the differential amplifier is given in Figure 3.4. The differential amplifier has a large gain. The small voltage differences at the input are amplified and send to the output. The ring oscillator has four stages. The total gain of the ring is given in (3.3).

$$\mathrm{A_{ring}} = A_{one\ stage}{}^{\#number\ of\ stage} \tag{3.3}$$

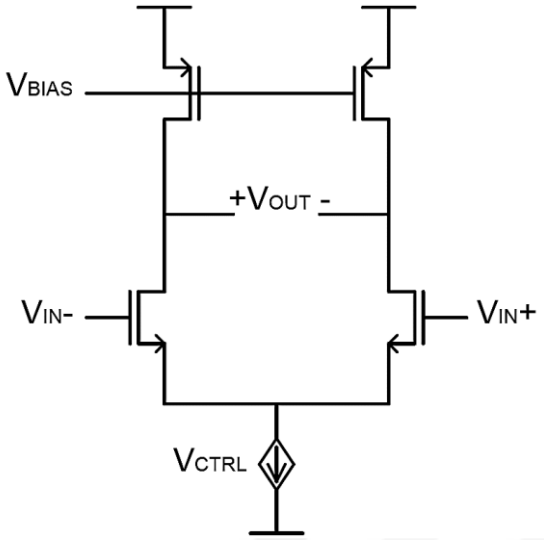



Figure 3.4. Schematic of a differential amplifier.

In the beginning, all the transistors are in the saturation region, and each stage has a large gain. After a certain time, small voltage differences at the input are magnified by each stage. The voltage swing at the output increases and the transistors go into the linear region. The gain of the amplifiers decreases and saturates at one. The loop has unity gain, and the phase difference is 180 degrees, Barkhausen Criteria holds, and the system oscillates.

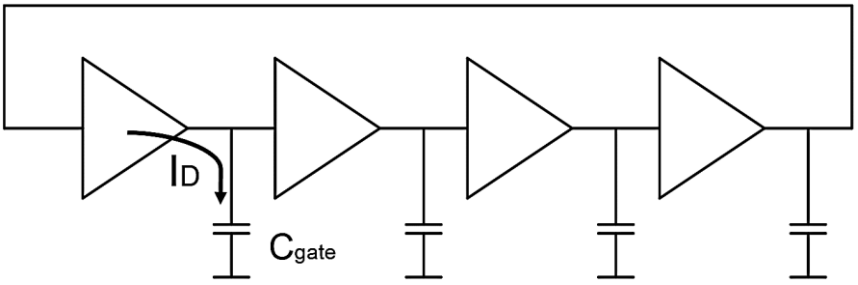



Figure 3.5. Simplified ring oscillator with gate capacitances.

The gain of the amplifier is one. The oscillation frequency is approximated in (3.4). It is defined by the drain current, swing voltage, and gate capacitances. The simplified version of the VCO and the gate capacitances is given in Figure 3.5.

$$f_{\text{oscillation}} = \frac{I_D}{C_{gate}(V^+ - V^-)} \tag{3.4}$$

The gate capacitance is defined by the process specifications and the gate area. The gate area is kept minimum to decrease dynamic power dissipation. The swing voltage does not change considerably in the operation frequency region. The only parameter that can be adjusted is the drain current of the amplifier. In this design, drain current is controlled via a voltage-controlled current source. The control voltage is the output of the loop filter output voltage, $V_{CTRL}$. The control voltage range is GND to VDD. But the current source is responsive after 1V. If the control voltage increase further by 3V, the gain of the VCO, $K_{VCO}$, decreases. So that the actual control voltage range is 1V to 3V, the operation frequency is 125MHz. At that frequency, the $V_{CTRL}$ is at the center of the control voltage range equal to 2V. The VCO oscillation frequency versus control voltage is given in Figure 3.6.

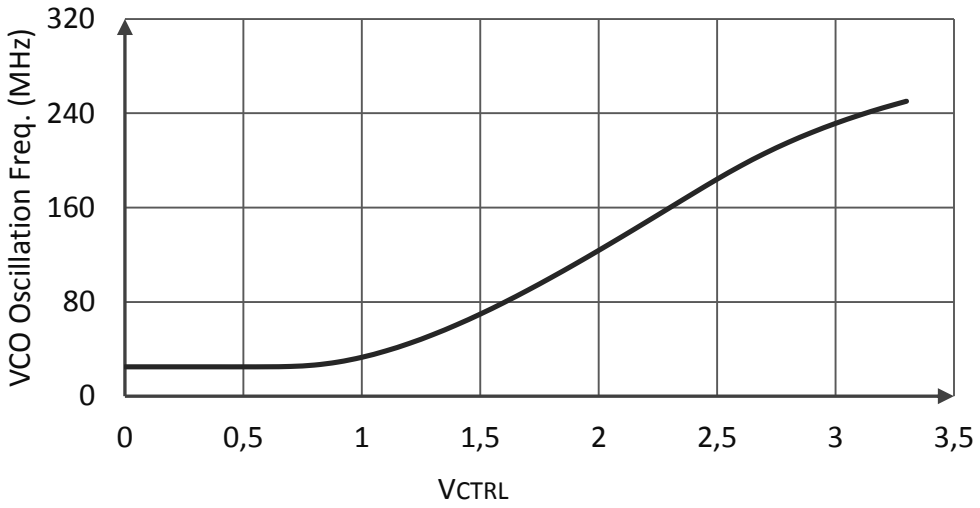



Figure 3.6. Simulation result for the VCO oscillation frequency versus control voltage, VCTRL. Oscillation frequency does not respond until 1V. The $V_{CTRL}$ is around 2V at operation frequency, 125MHz.

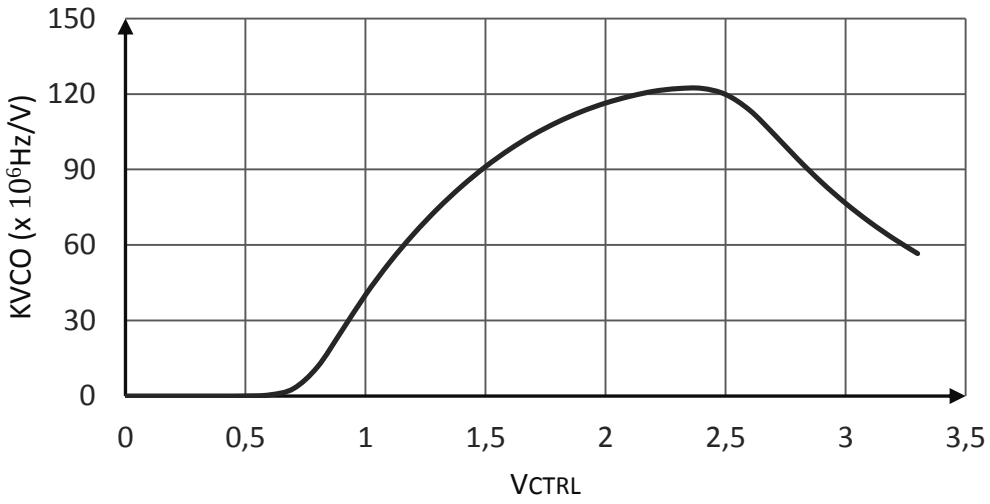



Figure 3.7. Simulation result for the $K_{VCO}$ versus control voltage. The gain of the VCO depends on the applied control voltage.

The slope of the oscillation frequency versus control voltage gives the gain of the VCO, $K_{VCO}$. By taking the derivative of it with respect to control voltage, $K_{VCO}$ can be plotted as in Figure 3.7. $K_{VCO}$ is not constant, and it changes over control voltage. For the sake of simplicity of the calculation, only the operation frequency point is taken into account. At that point, the $V_{CTRL}$ is 2V, and the $K_{VCO}$ is equal to 1.16 x $10^8$Hz/V.

**Loop Filter (LF)**

As mentioned above, the solution is not unique. One of the three parameters, the $I_P$, $R_1$, and $C_1$, needs to be set. $I_P$ is set to 64μA. The input frequency of the system is equal to 12.5MHz. The bandwidth of the system should be less than one-tenth of the input frequency. By using equation (3.2), $C_1$ can be found. The division factor, M, is equal to 125MHz/12.5MHz = 10.

$$\omega_{\text{in}} = 2\pi * f_{in} = 7.85 * 10^7\ rad/sec \quad (3.5)$$

$$\omega_{\text{BW}} < 7.85 * 10^6\ rad/sec \quad (3.6)$$

$$\omega_{BW} = 2.5 * \omega_n \tag{3.7}$$

$$\omega_n < 3.14 * 10^6\ rad/sec \tag{3.8}$$

Combining equation (3.2) with equation (3.8) and get the following expression (3.9).

$$C_1 > 38.3\ pF \tag{3.9}$$

The $C_1$ is chosen as 47pF. The main advantage of using a large $C_1$ capacitance is that it leads to smaller $R_1$ resistance. It improves the phase noise performance of the system. It is mentioned in Chapter 2.2.5, $C_2$ should be equal to $0.2C_1$ for the 45degree phase margin. To further increase phase margin, $C_2$ is chosen 3.3pF to be around one-tenth of the $C_1$. After setting the $I_P$ and $C_1$, $R_1$ can be found by using equation 3.1. It results in 10.6kΩ. The schematic of the loop filter is given in Figure 3.8.

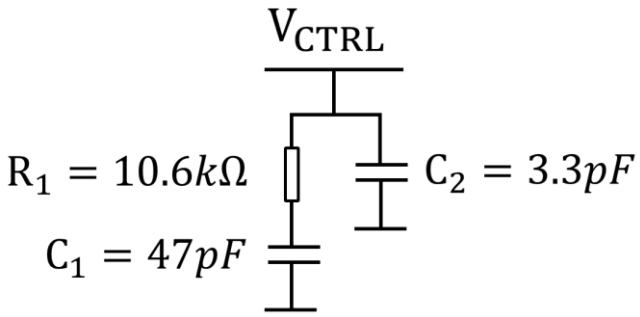



Figure 3.8. Schematic of the loop filter with optimized parameters.

**Phase Frequency Detector (PFD)**

In Figure 3.9, a sequential phase-frequency detector is given. The upper D flip-flop is clocked by the reference clock, and the lower D flip-flop is clocked by the PLL clock. The NAND gate monitors the up and down signals and generates the reset signal when both signals become active. The up and down signals control the current sources in the charge pump [23].

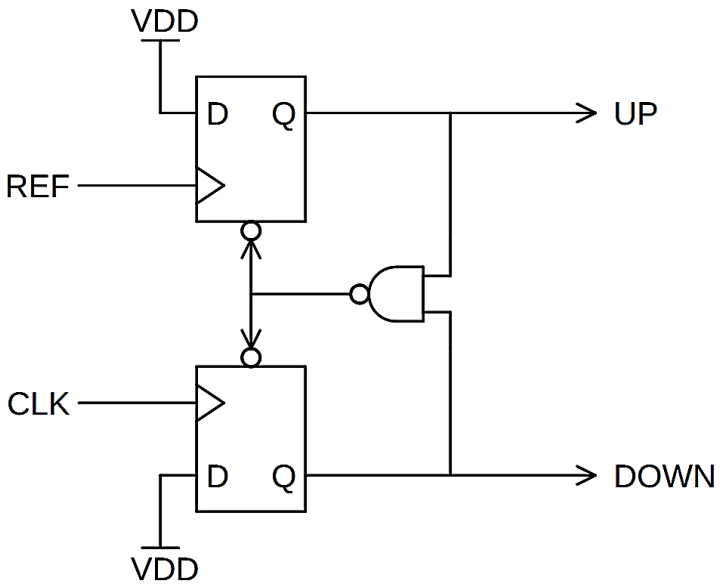



Figure 3.9. Sequential phase frequency detector.

**Charge Pump (CP)**

When up is active, a current with magnitude $I_{CP}$ is sourced by the charge-pump; conversely, when down is active, the current is sink into the charge-pump. When both up and down are inactive, no current flows into or out from the output node of the charge-pump. The output is a high impedance node under all circumstances [23].

In Figure 3.10, the schematic of the charge pump is given. The $M_3$ and $M_4$ transistors are the current sources of the charge pump. The current $I_{CP}$ is copied to $M_3$ and $M_4$ via $M_0$ and $M_2$ transistors. In the lock condition, the net output current is zero. In that case, the current has to be sourced and sink the same amount of current to the output. That means the matching is critical for $M_0$, $M_1$, $M_2$, $M_3$, and $M_4$ transistors. They are chosen large with dimensions to decrease process variations [25].

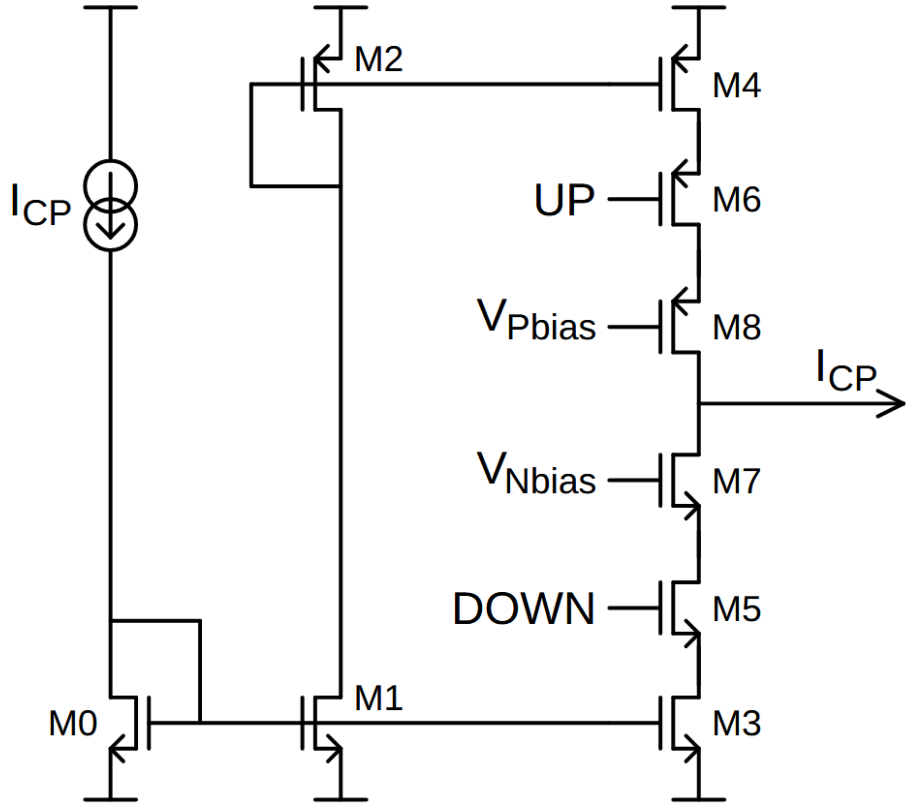



Figure 3.10. Schematic of the charge-pump.

**Frequency Divider**

The frequency divider is a synchronous frequency divider. It can divide the input frequency by an integer number in the range of 0 to 15. The schematic of the divider is given in Figure 3.11. It has a synchronous counter. When the count number is equal to the reference REF [3:0], the output signal is generated, and the counter is restarted.

The reference clock signal frequency is 12.5MHz, and the PLL output frequency is 125MHz. The division factor results in 10. The input and output waveforms of the operation are given in Figure 3.12. Note that the pulse width is not half of the period. But, it is not the problem for phase detection. The PFD only checks the posedge of the divided signal.

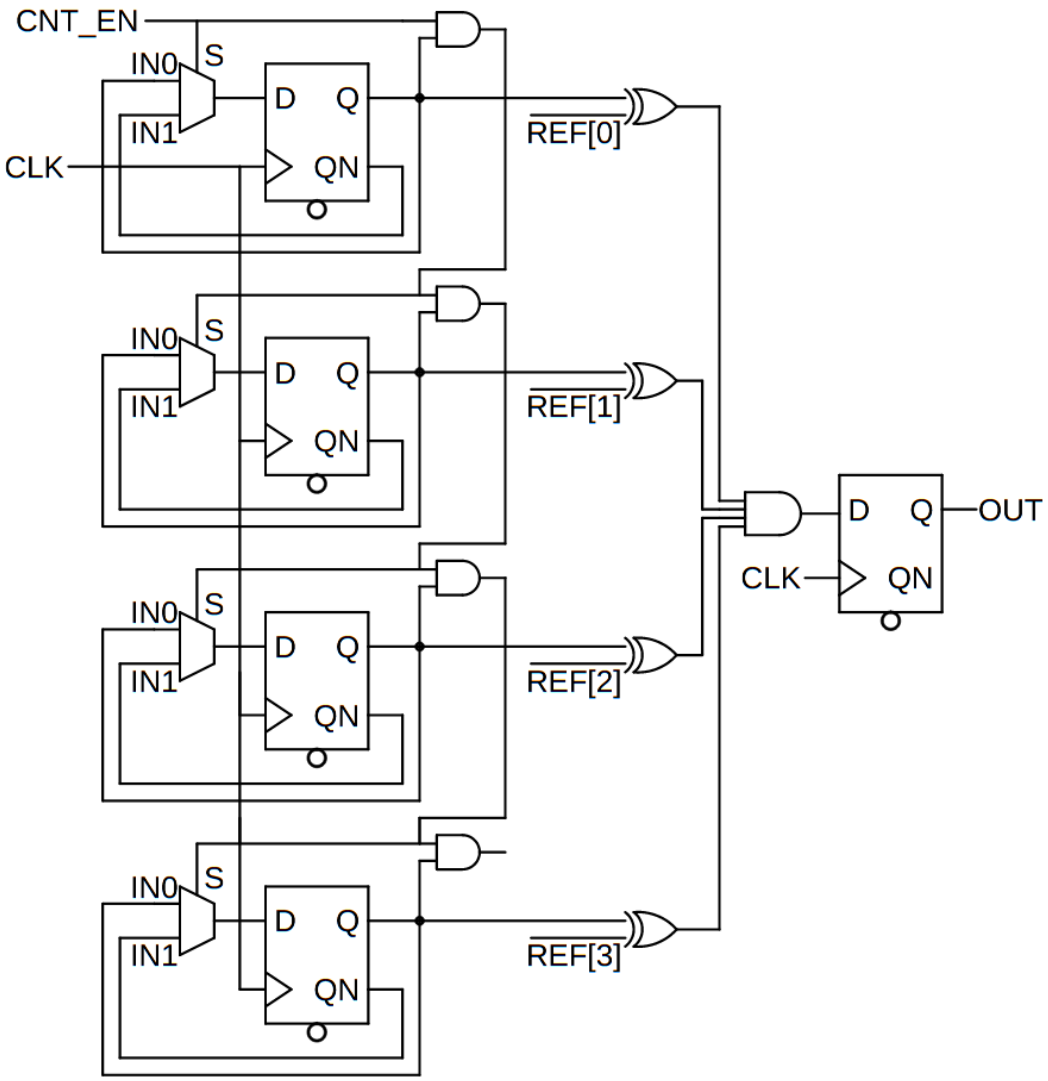



Figure 3.11. Synchronous frequency divider.

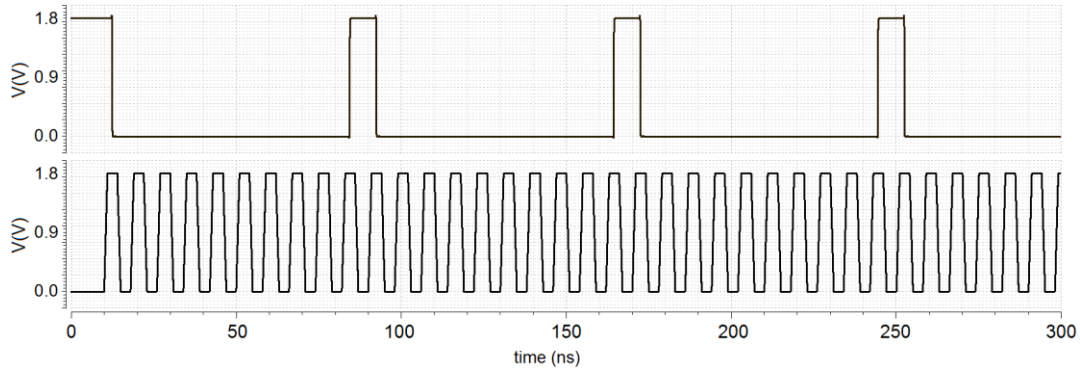



Figure 3.12. The input and output waveforms of the frequency divider.

### 3.2.2 PLL Simulation Results

The phase-locked loop (PLL) is investigated in three parts. First, the transient response is simulated. Then loop dynamics are analyzed with AC simulation. The gain and phase of the loop are found. At last, the phase noise and jitter performance are given.

**Transient Response**

The reference clock is 12.5MHz. It is multiplied by 10 by the PLL. The PLL locks at 124.91MHz. One period results in 8.006ps. The VCO is a ring oscillator. It has four stages. Every stage has a differential output. In result, there is eight 125MHz clock signal with 45-degree phase difference with each other. The transient simulated result is given in Figure 3.13. The PLL consumes 7.161mW power on average.

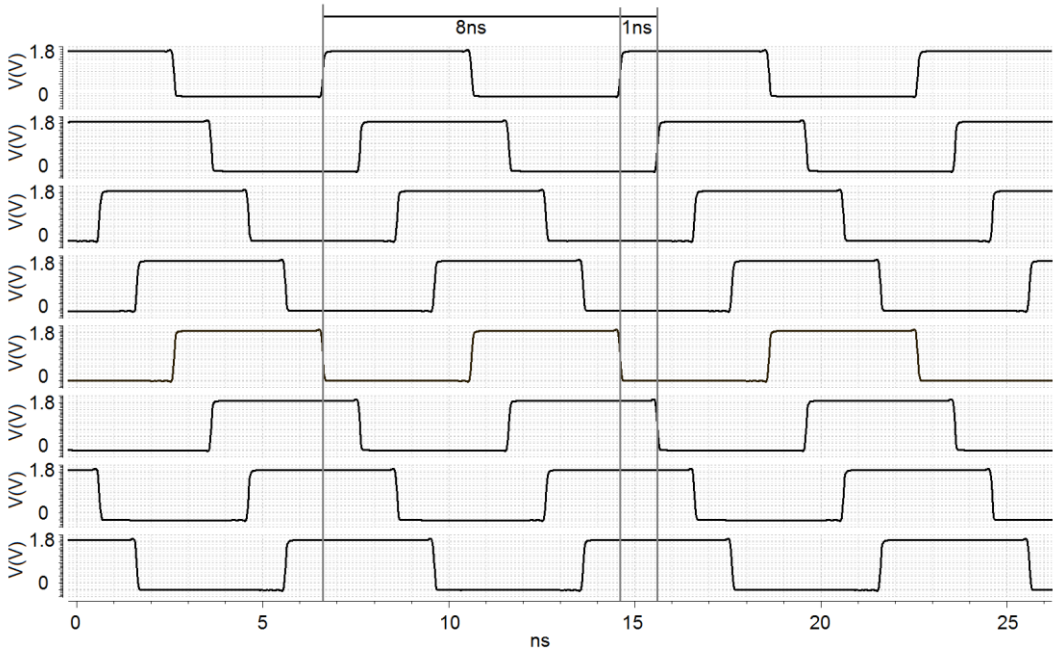



Figure 3.13. The transient simulation results of the PLL. It has eight 125MHz clock signals. Every signal has a 45degree phase difference.

**Stability Simulation**

The gain and phase of the PLL are given in Figure 3.14. The system is very stable. The phase margin peaks at the unity gain frequency point. It results in 60.17 degrees at 324.6 kHz. More information about the loop dynamics is given in Chapter 2.1.2.

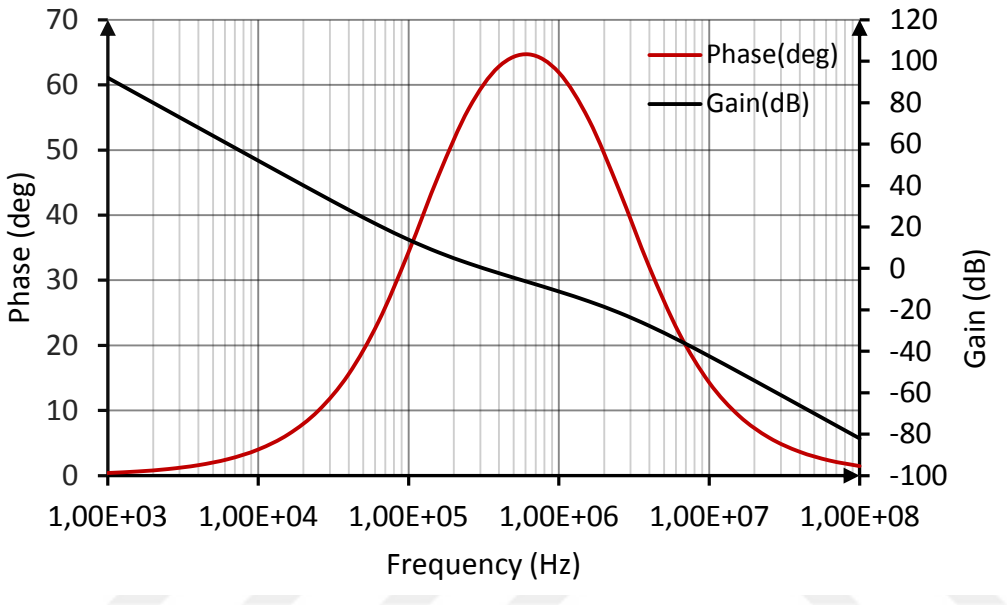



Figure 3.14. The stability simulation results of the PLL.

**Phase Noise**

The phase noise performance of the PLL is given in Figure 3.15. The high pass component is due to the VCO. The low pass noise component is due to CP, PFD, and frequency divider, and it is represented with "Loop." The combined phase noise is represented with "Output" in Figure 3.15.

The phase noise is -94dB at its maximum. It is better to convert the phase noise into jitter in timing circuitries. It can be achieved by integrating the phase noise in the relevant interval. The jitter results in 12.78ps for 125MHz carrier frequency.

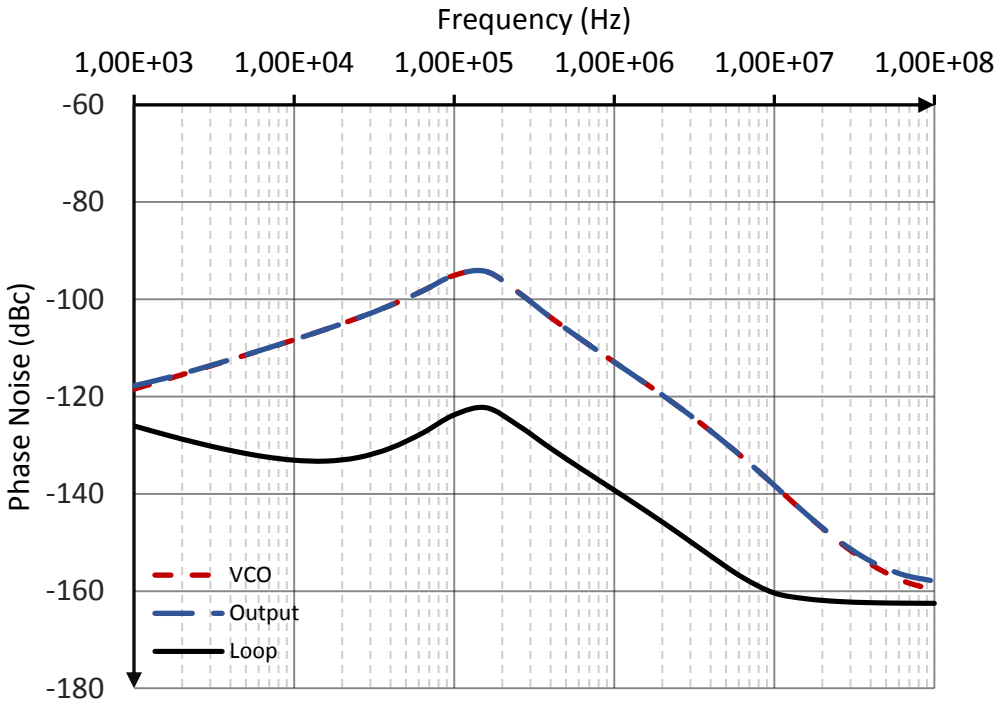



Figure 3.15. The phase noise simulation result of the PLL.

The phase noise is dominated by VCO noise. This is because of the ring oscillator. It is an RC oscillator and results in very high thermal noise. Sub-picosecond jitter performance can be achieved by LC oscillators. But in this application, the 12.78ps jitter is much less than 0.5LSB (62.5ps). The PLL noise is insignificant in this study.

### 3.2.3 Layout of PLL

The top layout of PLL is given in Figure 3.16. Each sub-block is highlighted in the figure. The dimensions are 500µm on X-axis and 350µm on Y-axis. It covers a 0.175mm$^2$ silicon area.

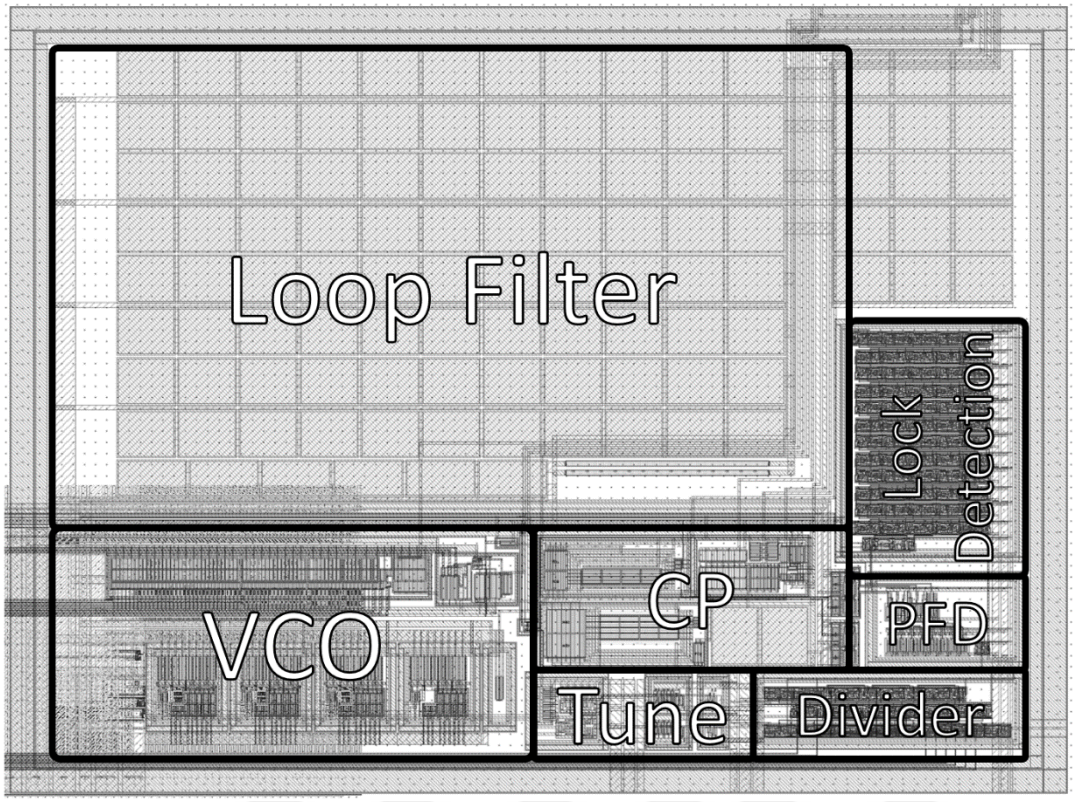



Figure 3.16. The PLL top layout. The dimensions are 500µm on X-axis and 350µm on Y-axis. It covers a 0.175mm$^2$ silicon area

### 3.3 Delay Locked Loop (DLL)

The block diagram of the charge-pump DLL is given in Figure 3.17. The sub-block and loop dynamics are explained in Chapter 2.3.

In this study, the DLL is used to bias the TDL delay cells. DLL and TDL have the same current starved inverters as a delay cell. Each cell has a 125ps delay time.

The DLL suffers from the high-frequency input signal. It cannot lock properly at the system clock frequency. The system clock is divided by two by a simple binary divider. The DLL reference clock frequency is 62.5MHz. DLL has 128 stages. The total delay is 16ns which is equal to the reference clock frequency.

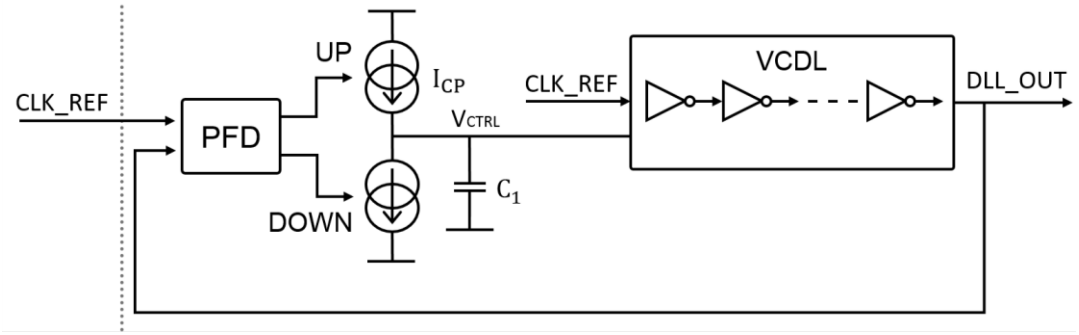



Figure 3.17. Block diagram of charge-pump DLL.

### 3.3.1 DLL Sub-blocks

The charge-pump DLL has five main blocks; a phase-frequency detector (PFD), a charge pump (CP), a loop filter (LF), and a voltage-controlled delay line (VCDL). Each block is explained separately in the following.

**Voltage Controlled Delay Line (VCDL)**

The input frequency of the DLL is 62.5MHz. The period of the input signal is 16ns. The VCDL has 128 identical delay cells. Each cell introduces a 125ps delay time. The total delay is equal to one reference clock period time, 16ns. In lock condition, $CLK_{REF}$ and $CLK_{DLL}$ signals are in phase.

The delay cell is a current starved inverter, in Figure 3.18. By controlling the current on the NMOS and PMOS transistors, the delay time can be adjusted. The current starved inverters are connected in series. The output of one inverter is the input of another inverter. The output load is the next cell's gate capacitance. It is charged by NMOS and PMOS drain current; by adjusting the $VN_{BIAS}$ and $VP_{BIAS}$ bias voltages, the currents can be controlled so that delay time [32].

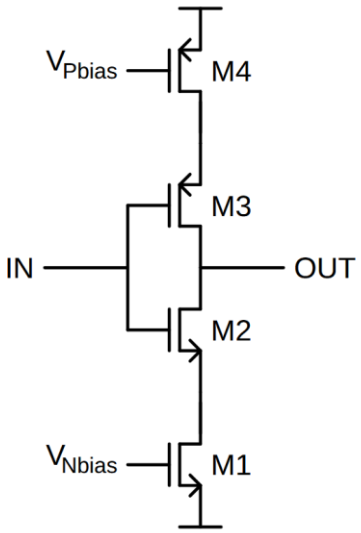



Figure 3.18. Schematic of the current starved inverter.

The output of the loop filter is $V_{CTRL}$, and it controls the $VN_{BIAS}$ and $VP_{BIAS}$ bias voltages. $V_{CTRL}$ cannot connect directly to $VN_{BIAS}$ or $VP_{BIAS}$. There has to be a conversion circuit. In Figure 3.19, the $V_{CTRL}$ drives a current source, $M_0$ is a self-biased, and $I_{BIAS}$ current flows through it. The $M_0$, $M_1$, and $M_{3\#}$ transistors are current mirrors, and the same $I_{BIAS}$ current flow through them. The $M_1$ and $M_2$ are on the same branch, and the drain currents are equal. $M_2$ and $M_{4\#}$ transistors are the current mirrors. As a result, the current of $I_{BIAS}$ is copied to $VN_{BIAS}$ and $VP_{BIAS}$ branches [33].

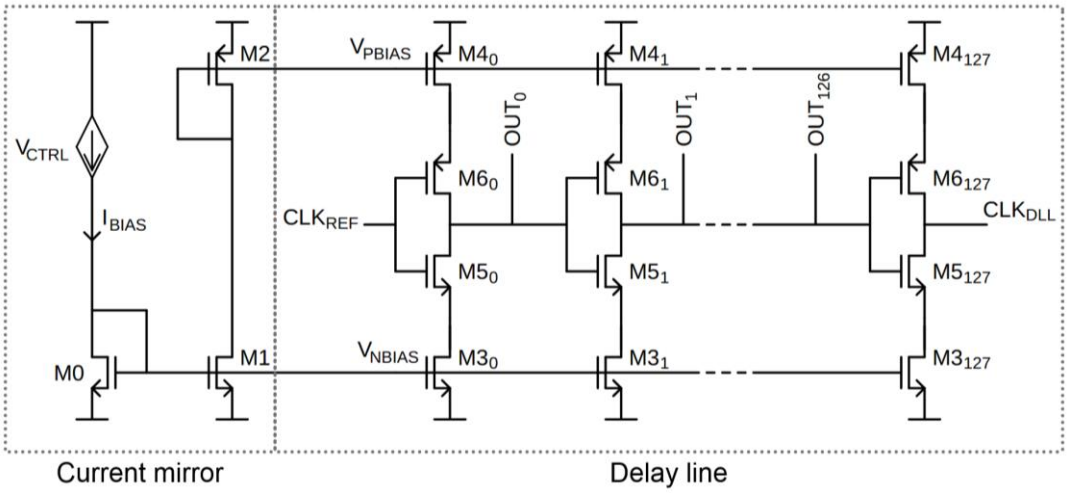



Figure 3.19. Schematic of the VCDL. The $V_{CTRL}$ drives the voltage-controlled current source, the current copied to $VN_{BIAS}$ and $VP_{BIAS}$ branches.

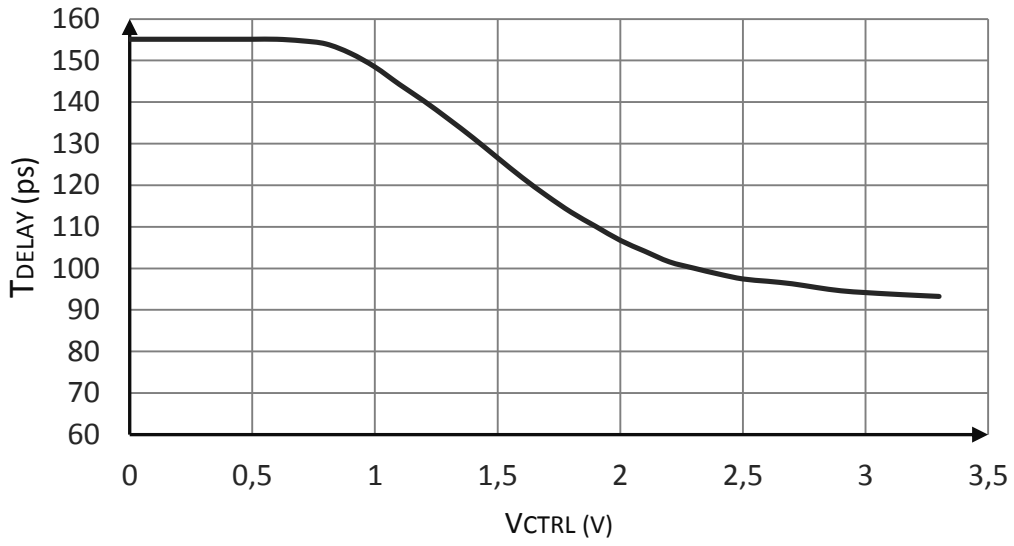



Figure 3.20. Simulation result for the inverter delay time with respect to $V_{CTRL}$. It is swept VDD to GND. As a result, $T_{DELAY}$ is equal to 125ps, and $V_{CTRL}$ is 1.5V in the lock condition.

The single inverter delay time with applied bias voltage is given in Figure 3.20. When 0 voltage is applied to the current source in Figure 3.19, the delay time of the inverter is 155ps, and it does not change much until 0.8V. After a further increase of the $V_{CTRL,}$ the current on the $M_0$ branch increases, and so that the drain currents of $M_{3\#}$ and $M_{4\#}$ transistors increases. An increase in drain currents decreases the charge time at the gates of $M_{5\#}$ and $M_{6\#}$ transistors. The transition takes less time. As a result, the delay time of the inverter decreases. The delay time does not change much after 2.5V. It is equal to 93ps when $V_{CTRL}$ is at maximum.

The gain of the VCDL, $K_{VCDL}$, is given in Figure 3.21. The gain is zero until 0.8V. After it increases rapidly and peaks at 1.5V, then it steadily decreases. The delay time is equal to 125ps at lock condition. In Figure 3.20, the delay time is equal to 125ps when $V_{CTRL}$ is equal to 1.5V. The $K_{VCDL}$ is equal to -0.384rad/V at that point.

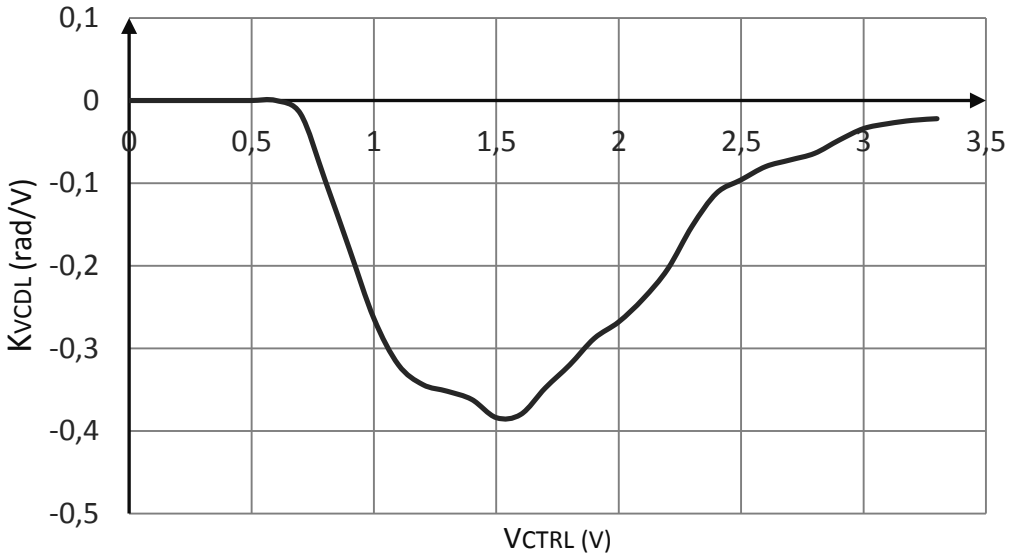



Figure 3.21. Simulation results for the gain of the VCDL, $K_{VCDL}$, with respect to control voltage, $V_{CTRL}$.

**Loop Filter (LF)**

The loop filter is a single capacitor in Figure 3.22. The design methodology is given in Chapter 2.3.4. The input frequency is 62.5MHz which results in $3.93\times10^8$rad/sec. The $K_{VCDL}$ is equal -0.38rad around the lock condition. There are two unknown $I_P$ and $C_1$ and one equation. The solution is not unique, $I_P$ is set to 32μA and put into (3.1). As a result, $C_1 \geq 48$fF.

$$0.1\omega_{in} \geq \omega_p = \frac{I_p K_{VCDL}}{2\pi C_1} \tag{3.10}$$

The $C_1$ capacitance can be selected in the range of few tens of femtofarads. When the DLL loop filter is compared with the PLL loop filter, it is concluded that $C_1$ capacitance is very large in PLL. This is because the $K_{VCO}$ is greater than $K_{VCDL}$. Another reason is that the input frequency is 12.5MHz for the PLL and 62.5MHz for the DLL.

It is not ideal to choose the loop filter in the order of femtofarads. It is the range of gate capacitances of the transistors. They can introduce poles and zeros. If they are close with the loop pole, that will disturb the loop dynamics and could lead to oscillatory behaviors. $C_1$ is found with iteration. In the simulation best value for the $C_1$ capacitance results 3.2pF.

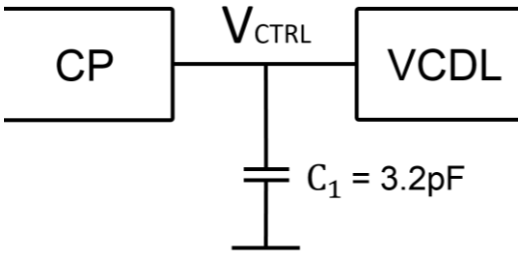



Figure 3.22. DLL loop filter. $C_1$ is chosen largely to have a more stable operation.

**Phase Frequency Detector (PFD) and Charge Pump (CP)**

The PFD and the CP of the DLL are the same as the ones in PLL. In Chapter 2.3.1, it is mentioned that the total delay of the DLL, $T_{DLL}$ should be in the range of $0.5T_{CLK}$ and $1.5T_{CLK}$. If it is not, the false lock condition will occur. It is good to have a lock correction circuit in that case. But in Figure 3.20, the delay time of one inverter is given. To find the $T_{CLK}$ multiply the one inverter delay time by 128. The $T_{CLK}$ is between 19.84ns and 11.9ns. It is in the range of $0.5T_{CLK}$ (8ns) and $1.5T_{CLK}$ (24ns). The DLL is safe for false lock conditions.

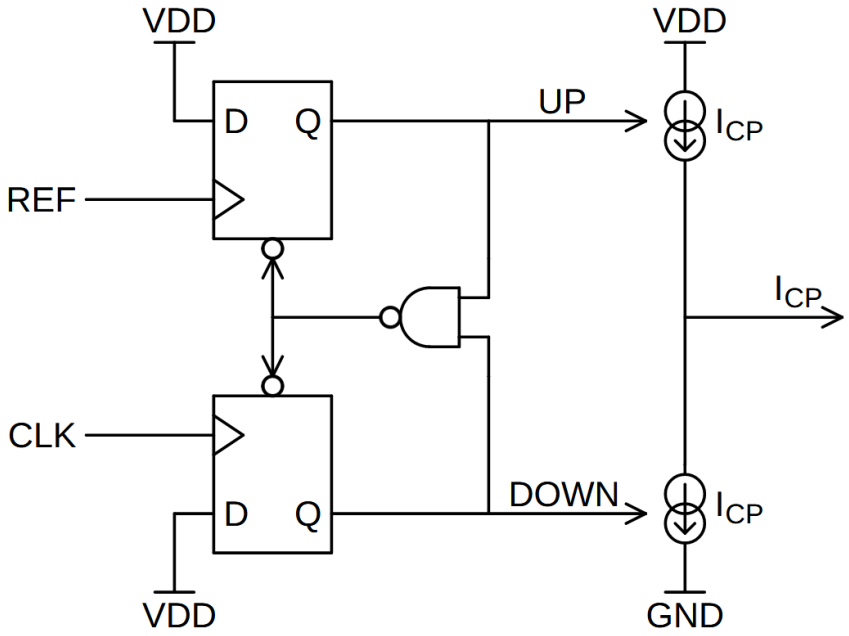



Figure 3.23. The phase-frequency detector and charge - pump of the DLL.

### 3.3.2 DLL Simulation Results

The delay-locked loop (DLL) is investigated in three parts. First, the transient response is simulated. Then loop dynamics are found in AC simulation. At last, the phase noise and the jitter performance of the DLL are calculated together with the PLL jitter.

**Transient Response**

The input of the DLL is a 62.5MHz clock signal. It is generated by PLL. The clock signal is divided by two, and the DLL clock is generated. It is delayed 128 times by the VCDL.

In Figure 3.24, the even-numbered outputs of the DLL are given with the DLL clock. It is in lock condition with the 128$^{th}$ output of the DLL. The delay time targeted 250ps for every even-numbered output. Transient simulation results in a 253.2ps

time difference. The phase error is 4.6 degrees. The DLL power consumption is 3.375mW on average.

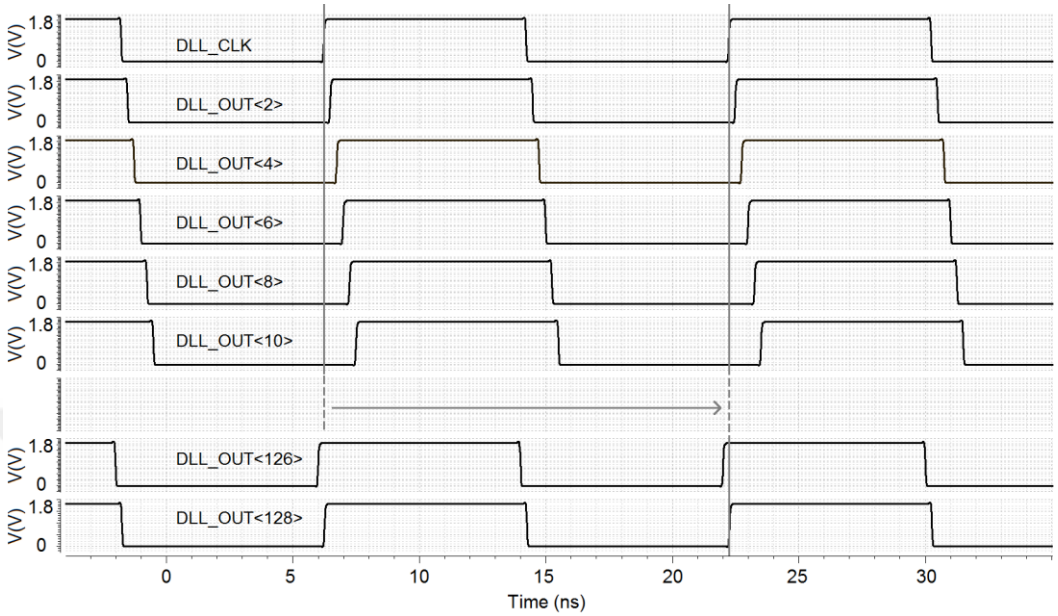



Figure 3.24. The transient simulation result of the DLL. The even outputs of DLL are given. Every even output has a 250ps difference.

**Stability Simulation**

The gain and phase of the DLL are given in Figure 3.25. The loop has only one zero at the origin. Loop is always stable. The phase margin is constant at 90-degree, and the gain decreases with 20dB/Dec.

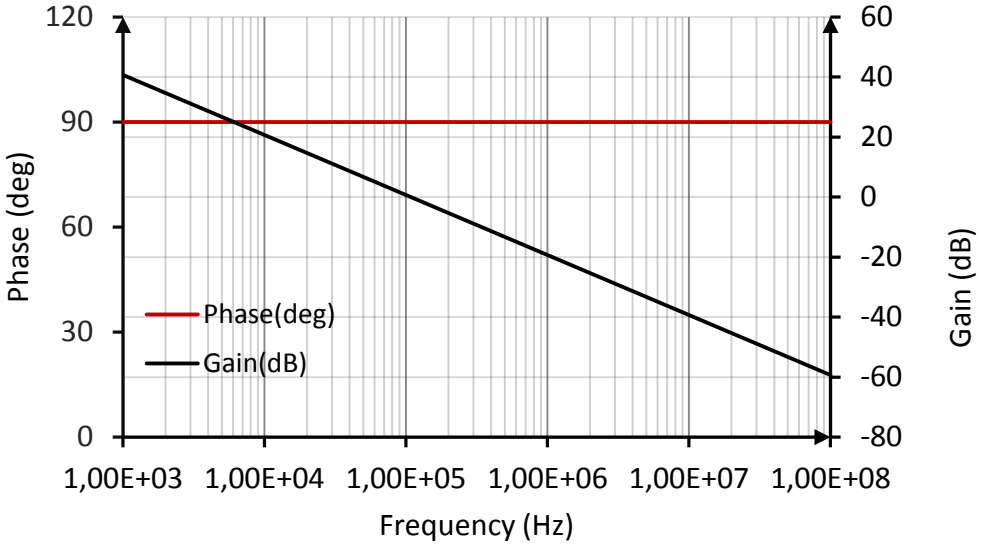



Figure 3.25. The stability simulation results of the DLL.

**Phase Noise**

The phase noise performance of the DLL and PLL is given in Figure 3.26. DLL noise is given with “red,” PLL noise is given with “blue,” and the combination of both noise sources given with “black.”

The DLL noise has low pass characteristics, and PLL noise has bandpass characteristics. The output of the PLL is the input of the DLL. As a result, at low frequencies, DLL noise is dominating. At mid frequencies, the PLL noise becomes more dominant. At high frequencies, the DLL becomes more dominant again. It is important to note that the PLL noise is suppressed by the DLL; as a result, the overall noise performance is better than the PLL noise performance.

The PLL has a 12.78ps jitter. The PLL noise is suppressed by the DLL. The PLL and DLL together have an 8.403ps jitter. The phase noise performance is improved.

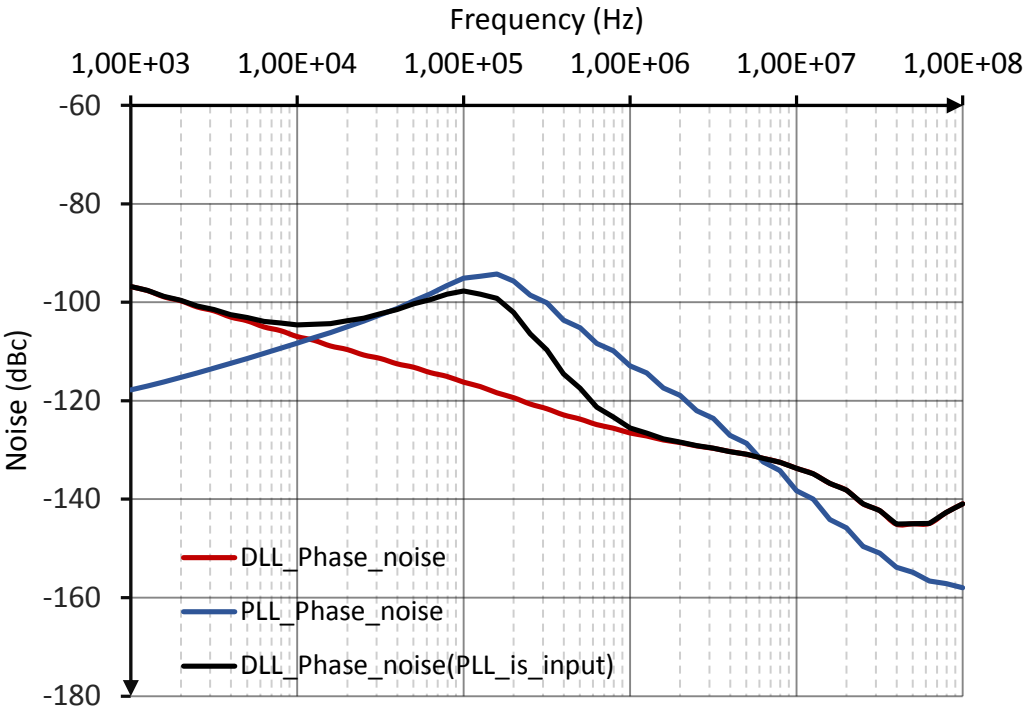



Figure 3.26. The phase noise simulation result of the DLL.

### 3.3.3 Layout of DLL

The top layout of DLL is given in Figure 3.27. Each sub-block is highlighted in the figure. The dimensions are 500µm on X-axis and 570µm on Y-axis. It covers a 0.285mm$^2$ layout area.

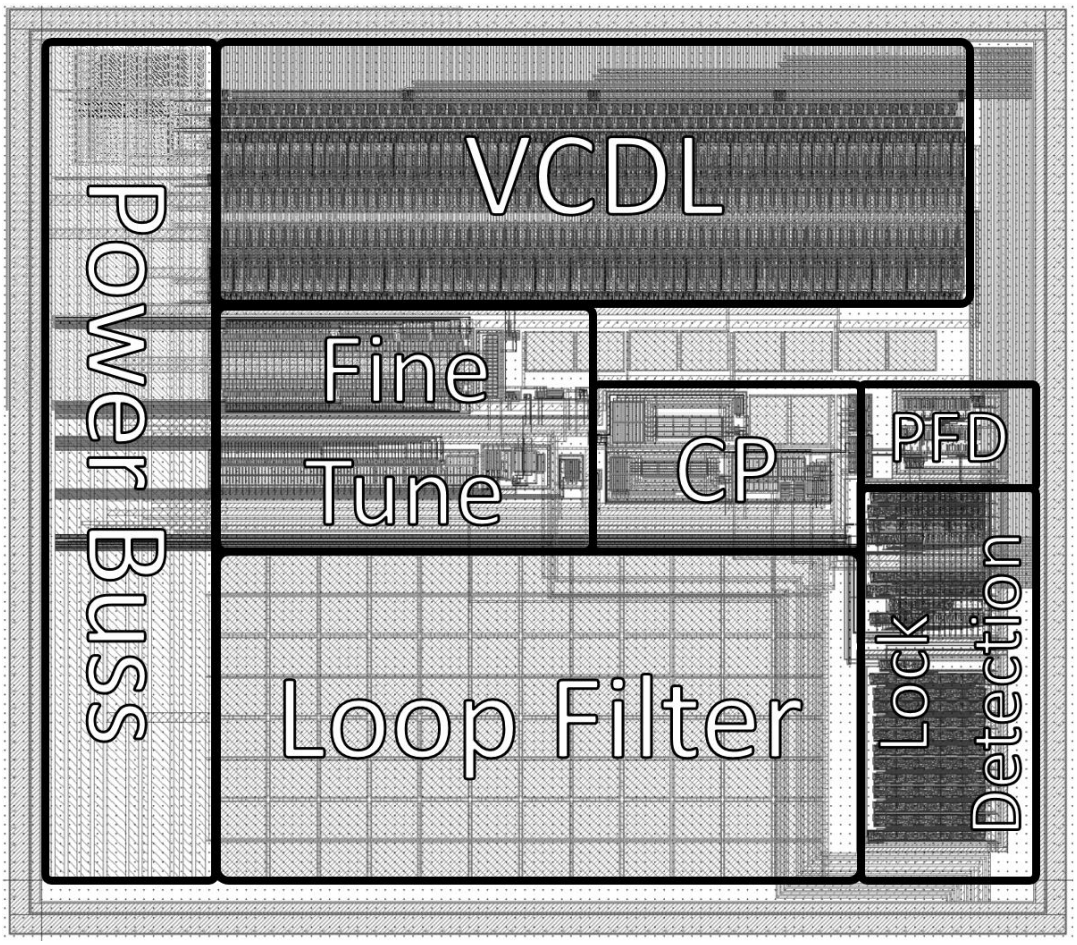



Figure 3.27. The DLL top layout. The dimensions are 500µm on X-axis and 570µm on Y-axis. It covers a 0.285mm$^2$ layout area.

### 3.4 Synchronous Counter

The 8 most significant bits (MSB) are generated by the counter. The counter is synchronous. It prevents ripple and possible pulse width losses.

The external clock signal is connected to every individual D flip flop's clock input. They are clocked together simultaneously at the same time. The output is "synchronous" with the clock signal [34].

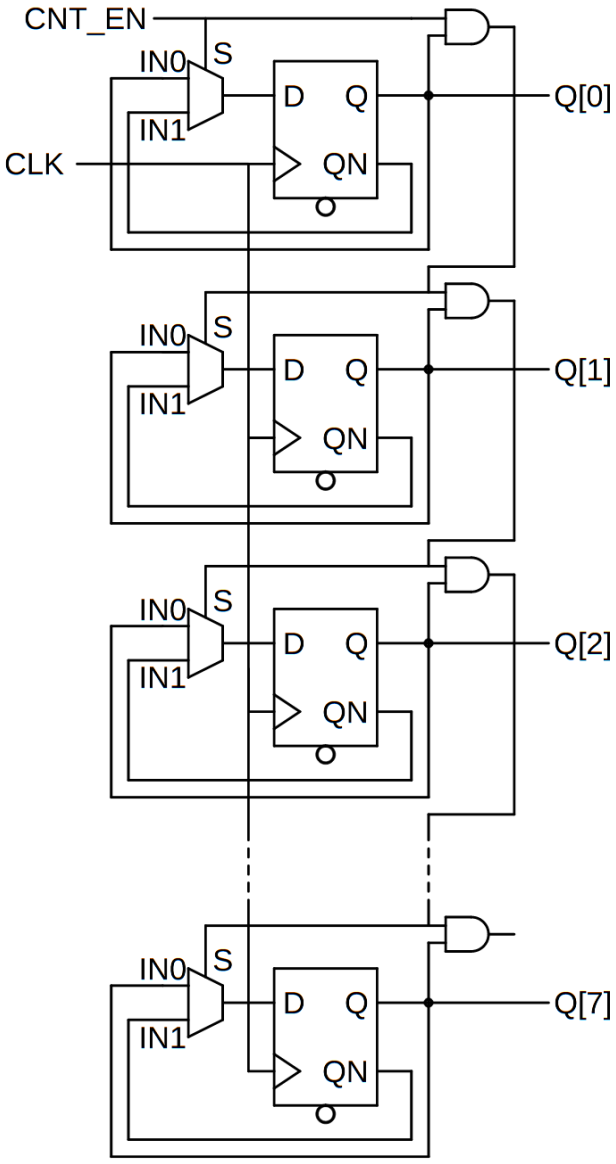



Figure 3.28. Synchronous counter schematic.

The schematic of the synchronous counter is given in Figure 3.28. It has eight stages. Every stage is one bit counter. They can be connected in cascade to build an 8 bit counter.

The one-bit counter has a count enable, “CNT_EN” signal. If the control signal is high, counter start counting. If not, the counter keeps the current state. Every stage output controls the next stage count enable signal. In that way, the frequency is divided at every stage.

The simulation result of the counter is given in Figure 3.29. The simulation is performed for 1024ns. It is the full range of the column-parallel TDC. In the figure, the clock signals are given at the bottom, and the MSB signals are given at the top. The clock signal is divided at every stage. The counter and the drivers consume 5.3mW power.

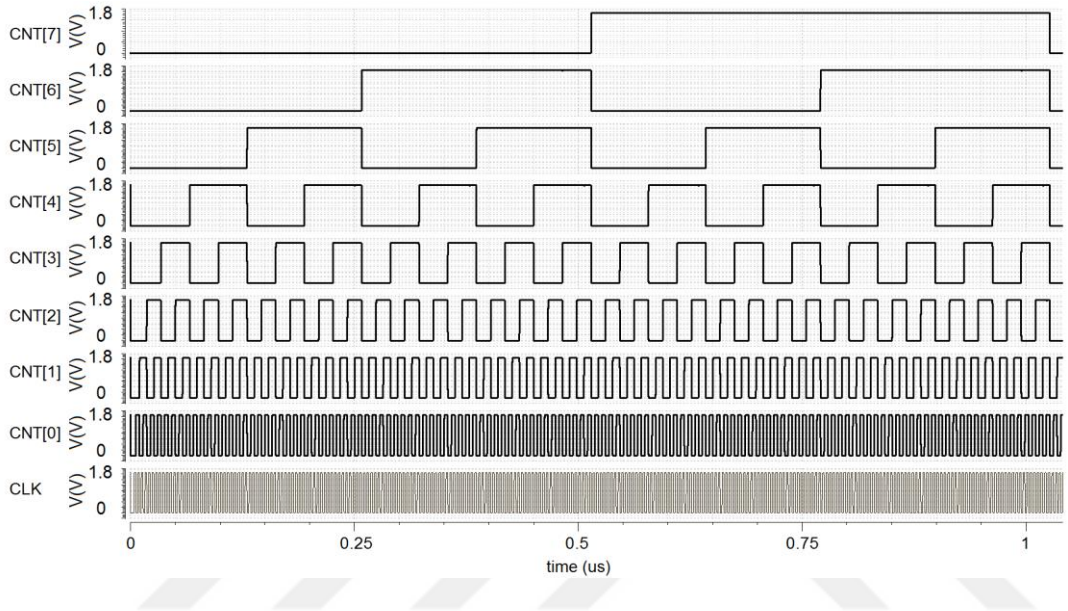



Figure 3.29. The transient simulation result of the synchronous counter.

## 3.5 Column Parallel TDC

The TDC in this design has column parallel architecture. At every column, there is TDC circuitry, and it is connected to a SPAD. When the SPAD is triggered, it records and sends the timing data to the digital controller. The block diagram is given in Figure 3.30.

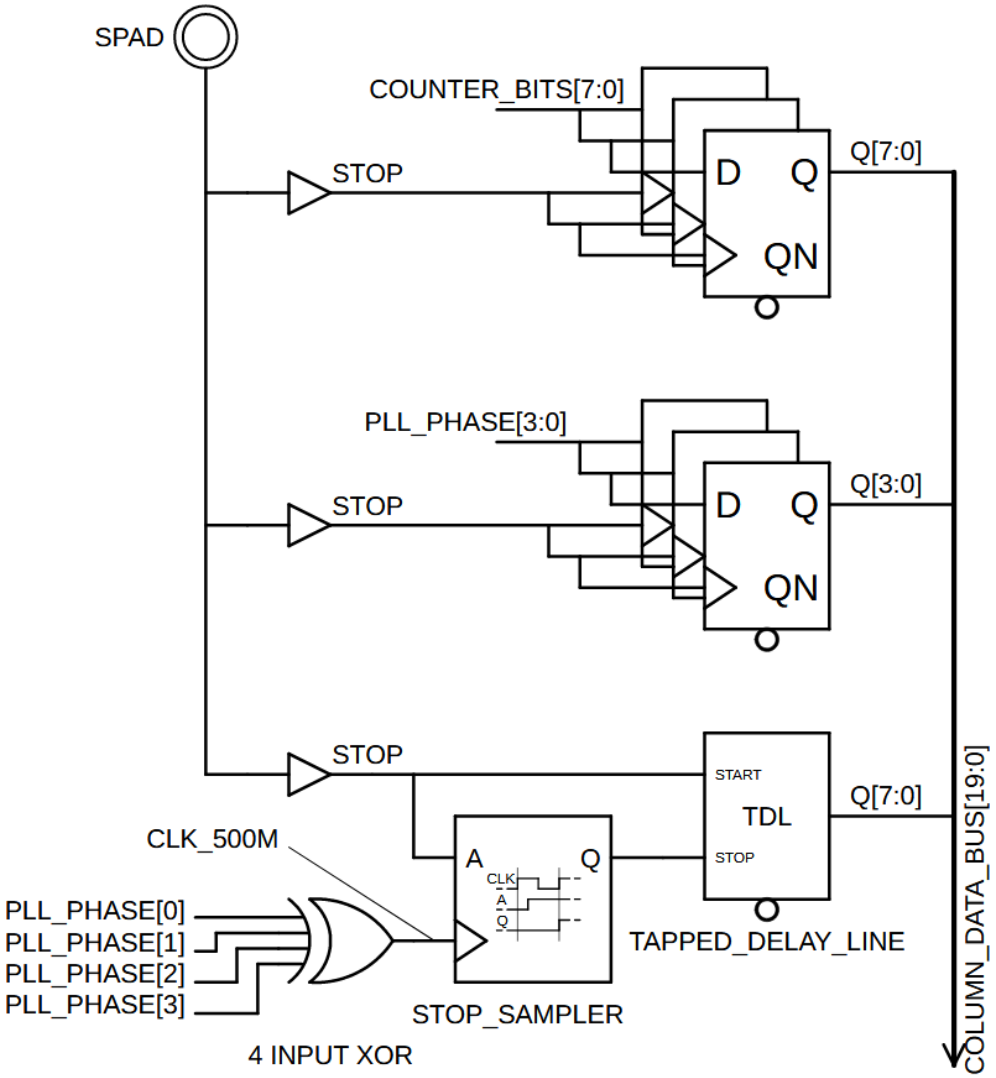



Figure 3.30. The column-parallel TDC.

The count bits are generated at the global side of the chip and carried through all the columns. It is a relatively slow bus. The LSB is working at 125MHz, and MSB is at 977kHz. There is 8bit memory at every column. When the STOP signal is triggered, it records the phases of the count bits. The data is binary coded.

The PLL has a ring VCO. It has four identical stages oscillating at 125MHz. Each stage has a 45-degree phase difference. By recording the PLL output phases, the resolution is increased from 8ns to 2ns. There is 4bit memory at every column to record PLL phases.

The PLL outputs are multiplied with an XOR gate. The 500MHz clock is generated at every column. It drives the "Stop Sampler." It samples the STOP signal at the next posedge of the 500MHz clock. The tapped delay line (TDL) records the time difference between the STOP signal and the next 500MHz clock posedge. It has 16 delay stages, and each stage has one-bit memory. The data is thermometer coded.

The counter has 8-bit output, the PLL has 4 bit, and the TDL has 16-bit output. The total data size 28-bit. It is carried to the digital controller via DATA BUS. It needs to be decoded to have meaningful data. This conversion should be executed in FPGA.

The START signal is generated by the digital controller. The digital-controller checks the PLL output phases. The START signal is generated when all the PLL output is low.

### 3.5.1 Multiplying Clock Signal

The 500MHz clock signal is needed to drive TDL. The system clock is 125MHz. It is generated by the PLL. In the PLL, the ring VCO is used. The VCO has four equal stages. At every stage clock signal is propagated by 45-degree. The stages are multiplied with the four input XOR gates. At the output, a 500MHz clock is generated.

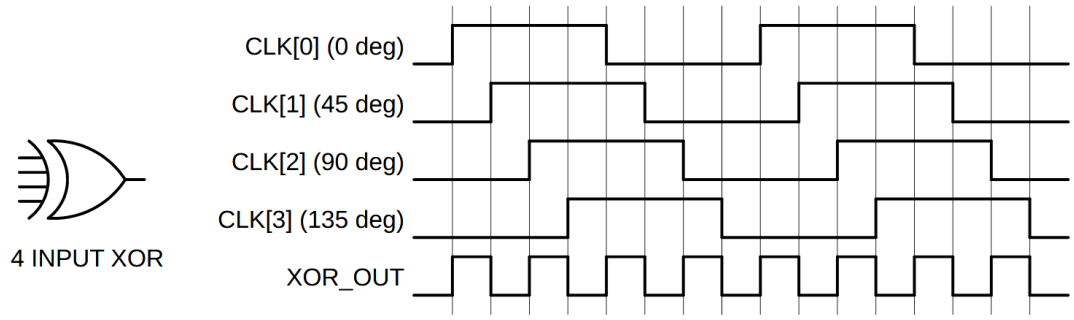



Figure 3.31. 4-input XOR gate (left), the inputs, and the output signals waveform (right).

### 3.5.2 Tapped Delay Line (TDL)

The tapped delay line (TDL) records the time difference between the “START” and the “STOP” signals. The full well is 2ns, and the resolution is 125ps.

The single inverter’s delay time defines the resolution of the tapped delay line. Each inverter has a 125ps delay time, and it is controlled and corrected by the DLL. The TDL has a 16 series inverter. In total, it has a 2ns delay.

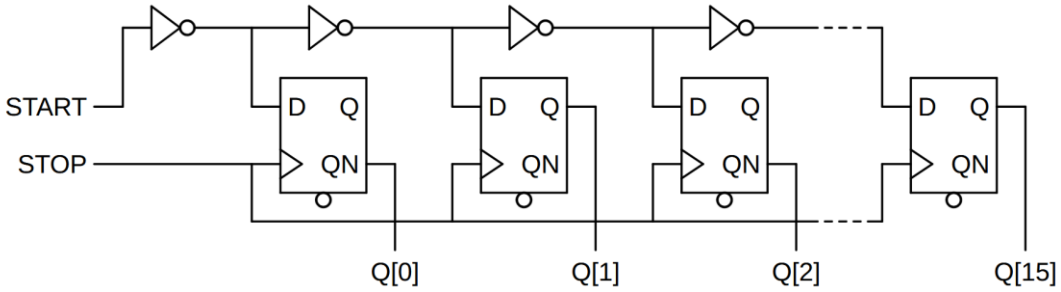



Figure 3.32. The schematic of the tapped delay line (TDL).

The schematic of the TDL is given in Figure 3.32. It has two inputs, “START” and “STOP”. Initially, these two signals are connected to “0” logic. Even inputs of the D flip-flops have logic “1” inputs (D[0], D[2], … D[14]) and the odd inputs have logic “0” inputs (D[1], D[3], … D[15]). When the start signal turns to logic “1”. The even inputs of the D flip-flops turn to logic “0,” and the odd inputs of the D flip-flops turn to logic “1”. But this transition takes time. Exactly the 125ps. While this transition, the stop signal arrives. When it arrives, D flip-flops record the input logic values. Some of the inputs made the transition, but there is not enough time for all of them.

It is crucial to have a very precise delay time. The controlled delay time is achieved by the current starved inverter in Figure 3.33. The current inverter is introduced for the DLL in Chapter 3.3.1. The identical inverter is used for the TDL. The delay time is controlled via $V_{NBIAS}$ and $V_{PBIAS}$ nodes. The bias voltages are generated at the DLL, and it is carried out through all the columns.

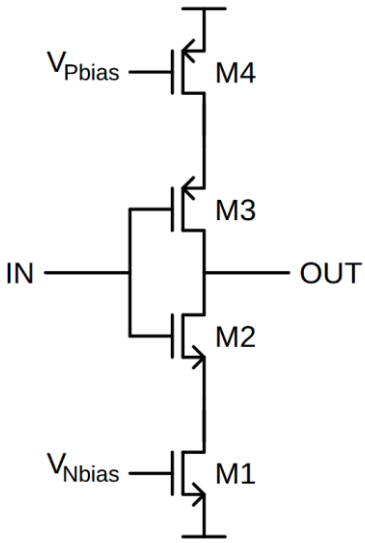



Figure 3.33. Current starved inverter.

At this point, someone may wonder why the DLL outputs do not carry out through the column. This is because of layout concerns. The DLL phases are working at 62.5MHz, and it has 128 outputs. Carrying high-frequency signals over long distances requires decent shielding to avoid crosstalk. It is simply not practical.

Instead, $V_{NBIAS}$ and $V_{PBIAS}$ signals are carried. They are DC signals and can be easily carried with simple shielding. Using TDL requires 16 inverters for each column. Comparing it with carrying all 128 outputs of the DLL, it requires considerably less silicon area.

Another reason is that the high-frequency signal will lose its phase and magnitude info over long distances. Powerful repeaters are required to avoid this problem. That will increase the layout footprint and power consumption.

The TDL is event-driven. The inverters make only one transition in one sampling cycle. That decreases the power consumption in the order of magnitude.

### 3.5.3 Stop sampler

The event-driven architecture is achieved by the Stop Sampler. It has CLK and STOP inputs. The STOP signal is sampled at the next positive edge of the CLK signal. The waveform of the inputs and output is given in Figure 3.34.

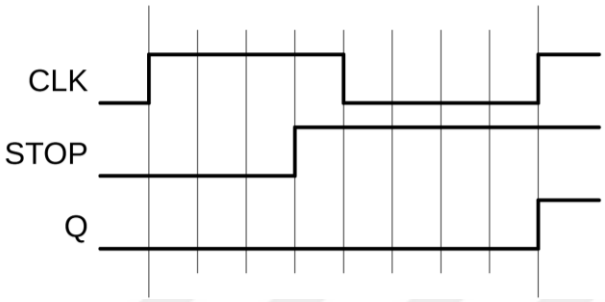



Figure 3.34. Stop sampler input and output waveforms.

The proposed architecture for the stop sampler is given in Figure 3.35. It consists of two series D flip-flops. They are positive edge triggered. Initially, they are in RESET state, “0”. Once the STOP signal makes a transition, the first D flip-flops output turns to “1”. Then at the next posedge of the CLK signal second flip-flop turns to “1”. One should be careful about the D flip-flops gate delay. It adds up to the time difference. While decoding, it should be excluded.

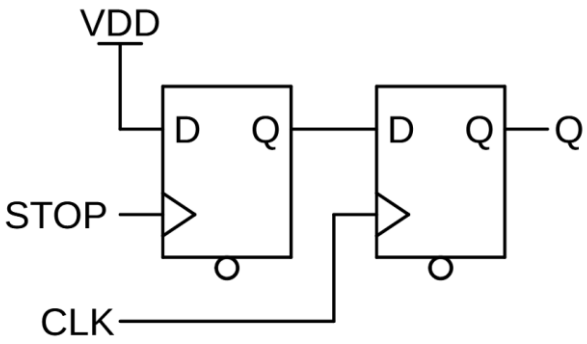



Figure 3.35. Stop sampler schematic.

### 3.5.4 Data bus and memory

The counter and PLL phases are driven through all the columns. They are sampled at every column individually when STOP signal arrives. The DATA BUS has 28 bits. The most significant 8 bits for the counter, the next 4 bits for the PLL phases, and the least significant 16 bits are for the TDL.

The counter bits are binary coded. 4 bit is phase code, and the last 16 bit is in thermometer code. 4-bit phase code can be represented with 3-bit binary code, and 16-bit thermometer code can be represented with 4-bit binary code. The extra bits are used for the synchronization between different domains. When all the outputs are converted into binary, it results in 13-bit binary code.

The TDC has a 13-bit resolution. The LSB is 125ps. It results in 1048ns full-well when it is multiplied by the speed of light; the range is will results in 150m in the distance. The range can be increased by simply increasing the counter bits. But in the larger distances, the returning laser power will be very low, and more advanced optical systems would be needed so that the system becomes unpractical.

**Counter Sampling**

The counter is a binary counter. It is sampled at posedge of the STOP signal in Figure 3.36. The D flip-flops are positive edge triggered. The STOP signal is generated by the SPAD. The code is binary, and it is the first 8 bit of the data bus.

The count signals have relatively low frequencies compared to the PLL phase signals. The fastest bit (CNT[0]) is in 125MHz, and the slowest signal (CNT[7]) is in 1MHz. Fast signals are shielded more carefully.

In Figure 3.36, the waveforms of the first 6 bits and the STOP signal are given. The sampled code is CNT[5:0] is 010110 in this particular case.

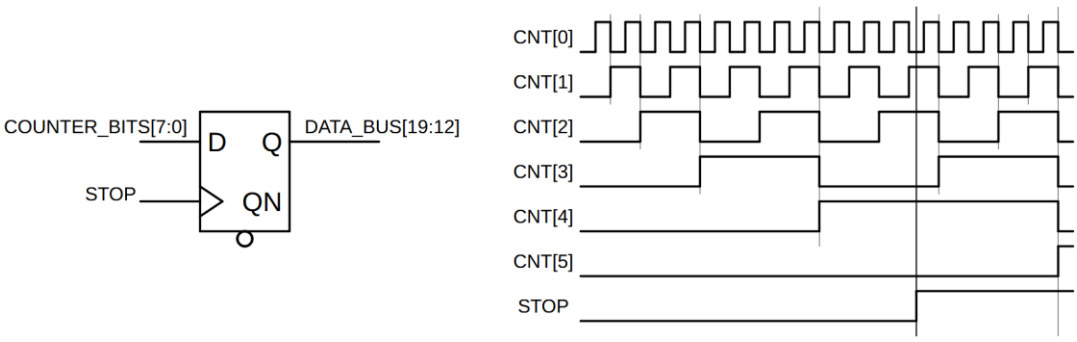



Figure 3.36. Counter data sampling and waveforms.

**PLL Phases Sampling**

The PLL has a ring oscillator for VCO. It has four equal phases. Each signal has a 45-degree difference. The waveform of the PLL phases is given in Figure 3.37. The PLL outputs are used as DLL.

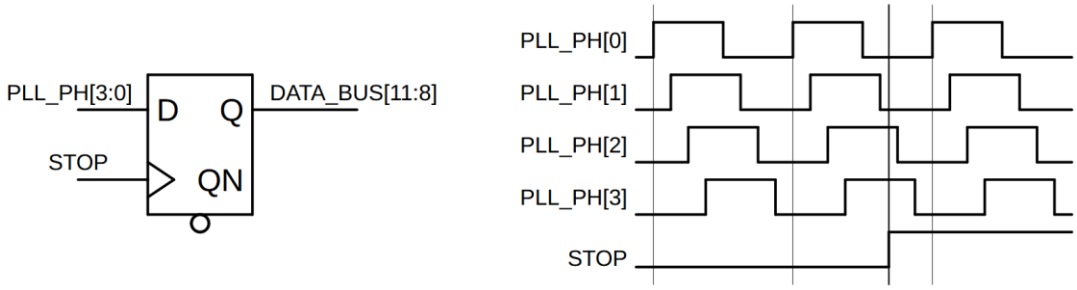



Figure 3.37. PLL phases sampling and waveforms.

Before sending the START signal, the digital controller checks the PLL output phases. The START signal is generated at the PLL_PH [3:0] = 0000 cases. The PLL_PH [3:0] code and encoded 3bit binary code are given in Table 3-1. In the table, the generated code is given in bold for the particular case given in Figure 3.37.

Table 3-1. The PLL phases and encoded binary codes.

| PLL_PH [3:0] | In Binary Code |
|---|---|
| 0001 | 001 |
| 0011 | 010 |
| 0111 | 011 |
| 1111 | 100 |
| 1110 | 101 |
| **1100** | **110** |
| 1000 | 111 |
| 0000 | 000 |

**Tapped Delay Line Decoding**

The Tapped Delay Line (TDL) has a 16-bit thermometer code at the output. It is the last 16 bits of the data bus. The data can be encoded in the digital controller or FPGA. The thermometer-coded data and encoded binary codes are given in Table 3-2 for the first 8 bits.

Table 3-2. The TDL thermometer code and encoded binary codes.

| PLL_PH [7:0] | In Binary Code |
|---|---|
| 00000001 | 000 |
| 00000011 | 001 |
| 00000111 | 010 |
| 00001111 | 011 |
| 00011111 | 100 |
| 00111111 | 101 |
| 01111111 | 110 |
| 11111111 | 111 |

### 3.5.5 Column Simulation Results

The system clock frequency is 125MHz. The column-parallel architecture is simulated over one clock period. At every column, the 500MHz clock signal is generated with the replicas of the system clock. The TDL measures the time differences between the STOP signal and the next 500MHz clock posedge.

The TDL parametric simulation result is given in Figure 3.38. The time difference at the input is swept over one clock period with 125ps steps.

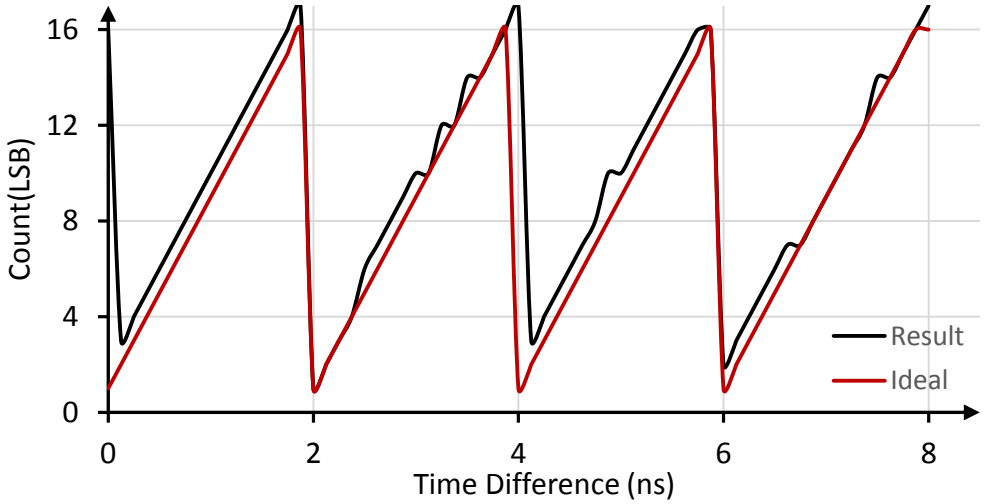



Figure 3.38. The TDL parametric simulation result. The time difference at the input is swept over one clock period with 125ps steps.

The first 4 bits of TDC are generated by TDL. The next 2 bits are generated by PLL outputs phase sampling. The sampling result of the PLL phases is given in Figure 3.39. Note that the TDL samples over a 2ns period and sampling of the PLL gives 1ns resolution. There is one-bit extra information. TDL and PLL phases are two different domains. The offset occurs between these two different domains, and it will change due to PVT variations. The one-bit extra information is used to cancel the offset between TDL and PLL domains.

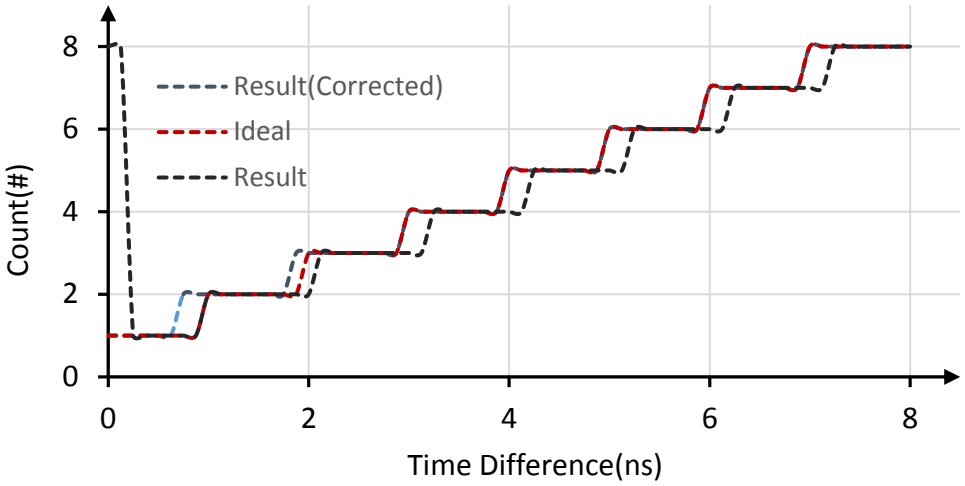



Figure 3.39. PLL phases sampling simulation results.

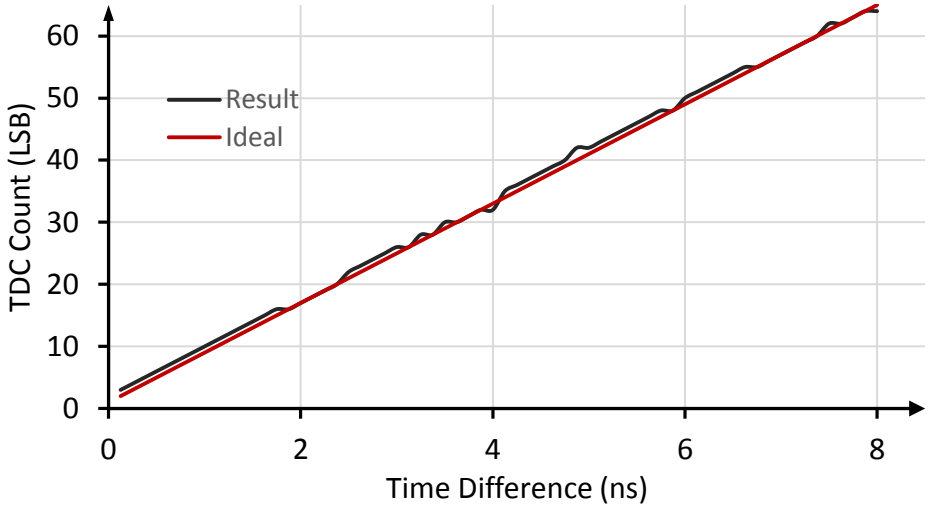



Figure 3.40. TDC sampling simulation result over one system-clock period.

The TDC sampling over one system clock period is given in Figure 3.40. It counts up to 64. TDC has a very linear response. The INL is given in Figure 3.41. It is 2 LSB in at worst case. The DNL is given in Figure 3.42. It has periodic over 2ns. The DNL is 2LSB at most.

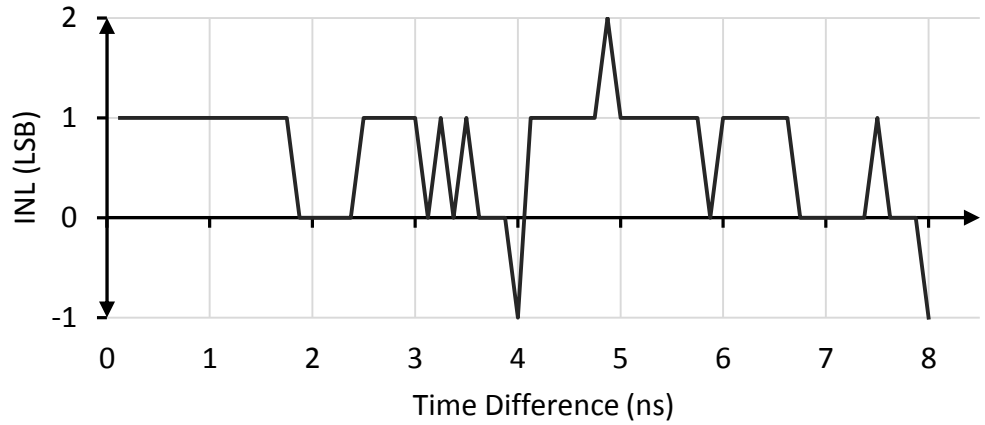



Figure 3.41. The INL simulation result for one clock period.

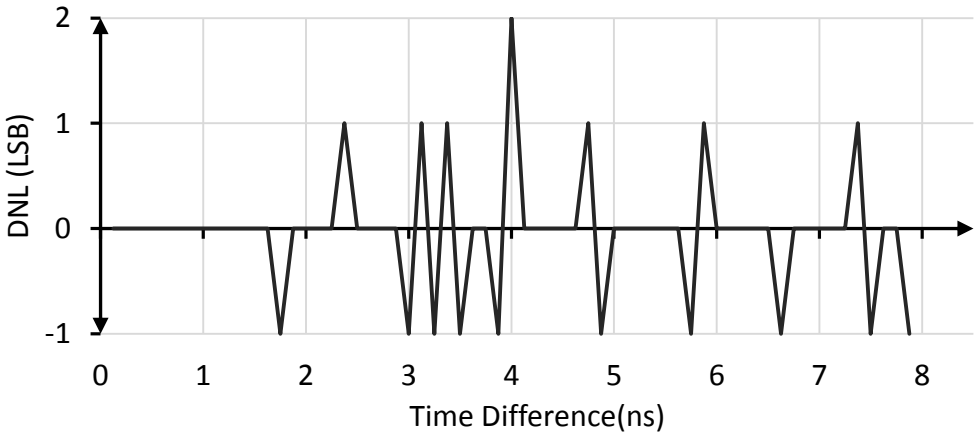



Figure 3.42. The DNL simulation result for one clock period.

The TDL consumes 4.61mW on average. At worst power case, all the column is sampled at the same time. In that case, power consumption is 33.12mW.

### 3.5.6 Column – Parallel Layout

The single TDC layout is given in Figure 3.43. A single delay cell is magnified in the figure. The column-parallel TDC is 52μm wide and 206μm in height. Even-numbered pixels are connected to the bottom TDCs, and the odd-numbered pixels are connected to the upper TDCs. The counter signals and the PLL outputs are carried through all the columns. They are shielded carefully.

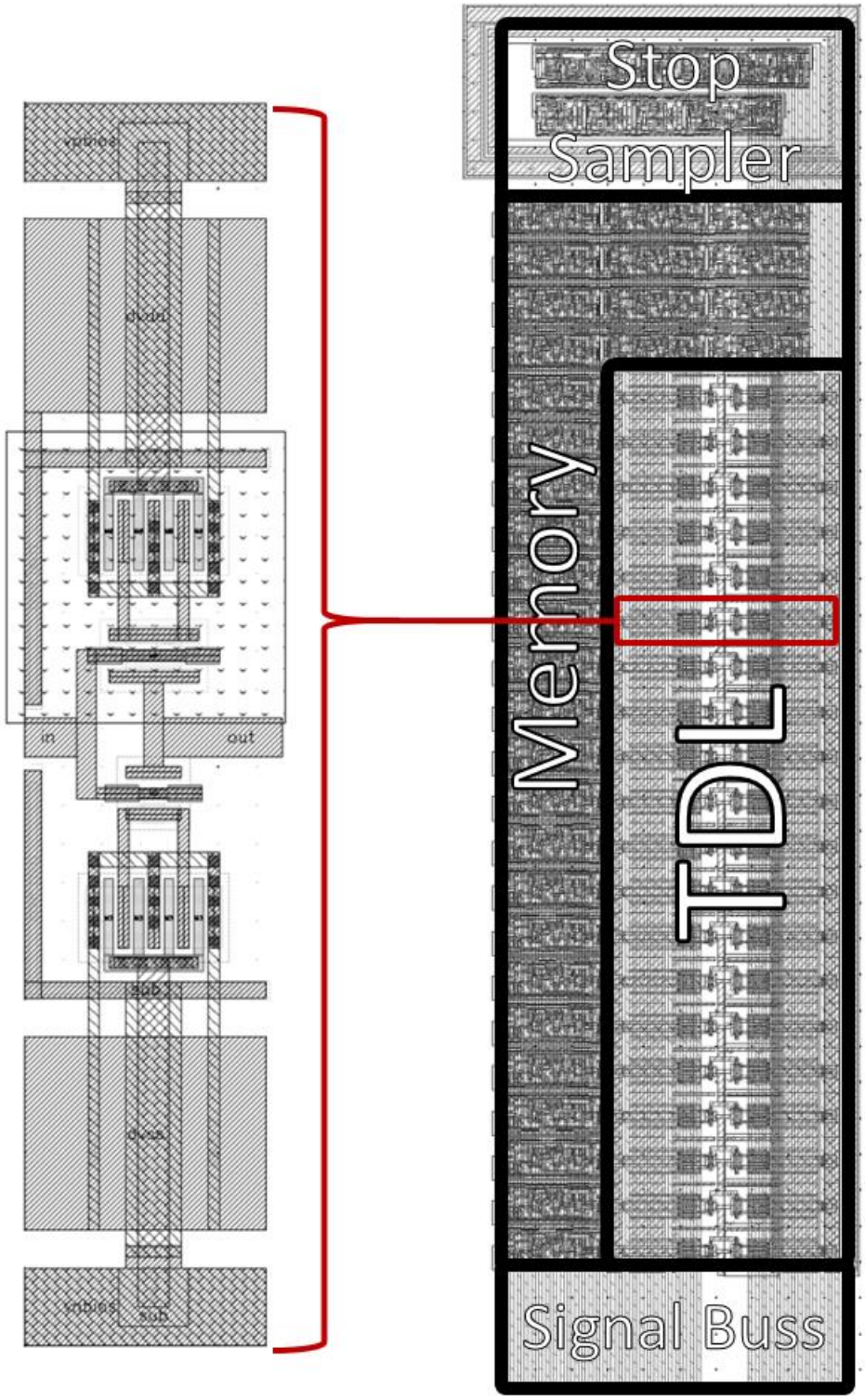



Figure 3.43. Column-parallel TDC layout, a current starved inverter is magnified. The column-parallel TDC is 52μm wide and 206μm in height.

## 3.6 Top Level Integration

### 3.6.1 Simulation Results

The column-parallel TDC has a 13-bit resolution. The LSB is 125ps, and the full range is 1024ns. The range can be further increased by simply increasing the counter resolution. But the system becomes unpractical due to the requirement of the large optic power.

The 4 LSB is generated by the TDL, the next 2 bit is generated by the PLL, and the most 7 bit is generated by the counter. The LSB of the counter runs at 125MHz. The simulation has run up to 40ns time difference. It is enough to observe the offset effects of the three different domains on the decoded code.

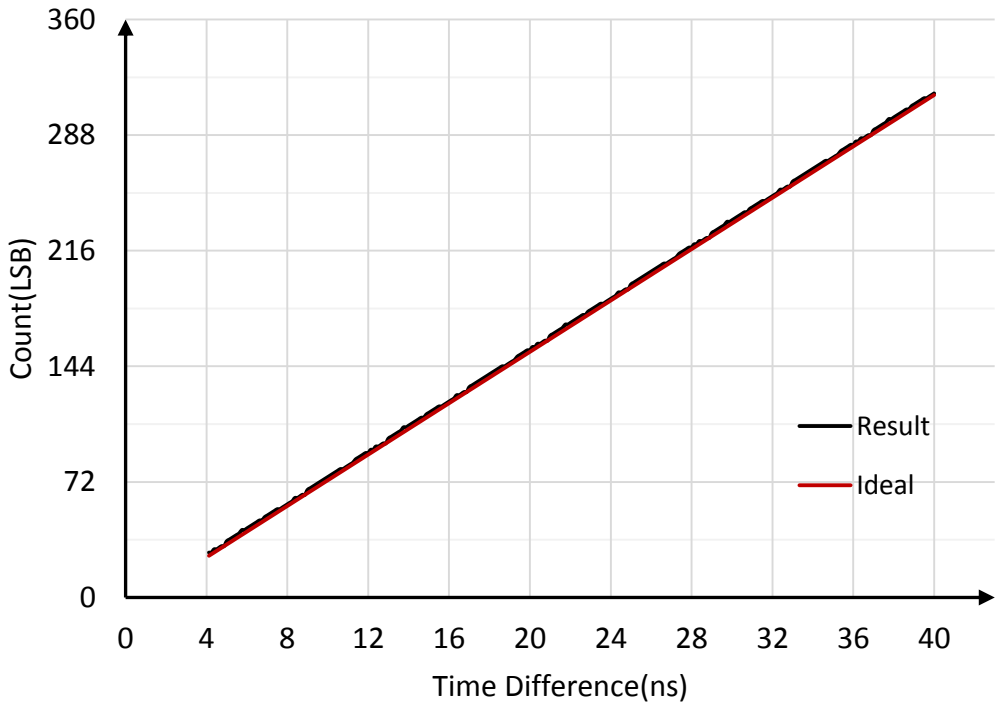



Figure 3.44. The top-level time difference conversion simulation result.

The time difference starts from 4ns, and it increased 125ps at every step up to 40ns. The result is given in Figure 3.44.

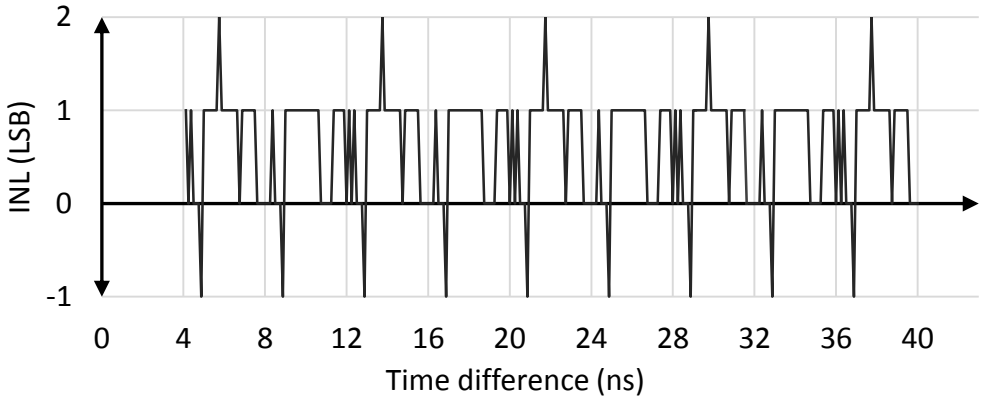



Figure 3.45. The INL simulation result of the top-level TDC.

The conversion is very linear. The INL is given in Figure 3.45, and the DNL is given in Figure 3.46. They are both 2LSB in at worst case. The TDL samples over 2ns, and the system clock has an 8ns period. The INL and DNL errors are periodic with harmonics of these two signals.

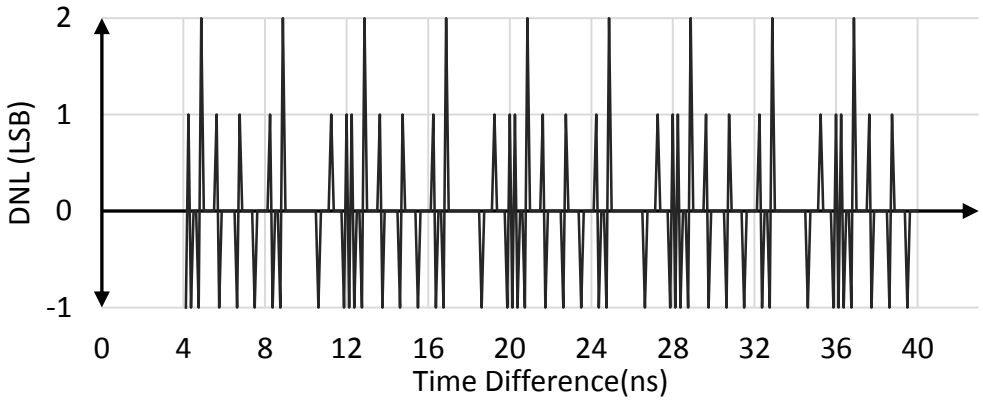



Figure 3.46. The DNL simulation result of the top-level TDC.

### 3.6.2 Top Level Floor Plan

The top-level floor plan of recommended LIDAR is given in Figure 3.47. It is a recommended design. It has 128 pixels horizontally and 96 pixels vertically. The pixel pitch is 26µm. The dimensions are 4400µm on X-axis and 3800µm on Y-axis. It covers a 16.72mm$^2$ silicon area.

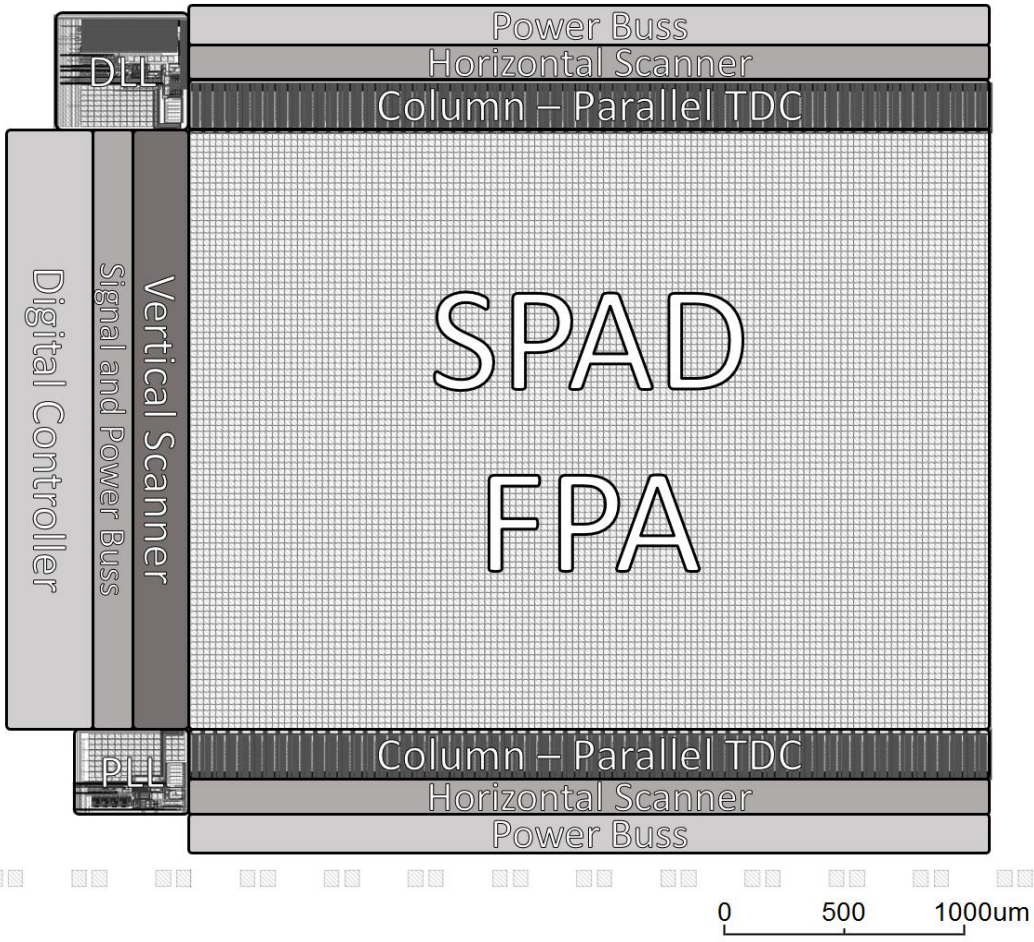



Figure 3.47. The recommended LIDAR floor planning. The dimensions are 4400µm on X-axis and 3800µm on Y-axis. It covers a 16.72mm$^2$ silicon area.

### 3.6.3 Literature Comparison and Summary

The design is implemented in 180nm CMOS technology. The pixel size is optimized to 26µm. The resolution of the designed column-parallel TDC is 125ps. The depth of the TDC is 13bit. It counts up to 1024ns, the range results in 150 meters. The jitter noise of the system is 8.4 ps which is well below half of the LSB. The INL and DNL error is +2/-1. The total power dissipation of the TDC – combined with PLL, DLL, and the column-parallel TDC – is 20.5mW in nominal, 49mW at worst case. The

TDC sampling period is 1024ns. The TDC sampling rate is 1MS/s. The limitation is determined by the data accusation rate of the digital controller.

The design can be used with monolithic CMOS SPAD arrays [2]. It is also suitable for flip-chip bonded InGaAs/InP SPAD arrays. The array size is recommended as 128x96. The TDC design has 128 columns. The sizes can be adjusted according to application specifications. It is fully scalable. The recommended design has a 16.72mm$^2$ silicon area.

The performance comparison of the design with the state-of-the-art TDC architectures available in the literature is given in Table 3-3. This work offers a small pixel pitch with high time precision. The image resolution is relatively high, and it is adjustable.

Table 3-3. The performance comparison with the state-of-the-art TDC available in the literature.

| Work | [11] | [12] | [35] | [36] | [37] | **This work** |
|---|---|---|---|---|---|---|
| Tech node (nm) | 45/65 | 150 | 180 | 350 | 350 | **180** |
| Pixel size (um) | 19.8 | 60 | 21 | 30 | 25 | **26** |
| LSB (ps) | 60 - 320 | 250 - 20000 | 208 | 312 | 97 | **125** |
| INL (LSB) | +3.4/-0.8 | +4.8/-3.2 | +0.32/-0.56 | +0.22/-0.22 | +1.6/-1.9 | **+2/-1** |
| DNL (LSB) | +0.8/-0.7 | +1.2/-1 | +0.15/-0.17 | +0.06/-0.06 | +0.1/-0.1 | **+2/-1** |
| TDC Depth (bits) | 14 | 16/15 | 12 | 10 | 10 | **13** |
| Array size | 16x8 | 64x64 | 16x1 | 32x32 | 32x1 | **128x1*** |
| Image resolution | 256x256 | 64x64 | 202x96 | 32x32 | 128x128 | **128x96*** |
| Number of TDC | 1 | 4096 | 64 | 1024 | 32 | **128** |
| Imaging Type | Scanning | Flash | Mechanically Scanning | Flash | Scanning | **Scanning** |

* It is the recommended size, and it is fully scalable.

# CHAPTER 4

## CONCLUSION AND FUTURE WORK

The main objective of this thesis is to design and implement a column-parallel time to digital converter (TDC) for the LIDAR applications. For this purpose, three different architecture is used. The first one is the Phase-Locked Loop, the second is the Delay Locked Loop and the last one is the Tapped Delay Line. The TDC is designed and implemented in 180nm CMOS technology. In order to verify the functionality of the architecture transient simulation, noise simulation and stability simulations are performed. The outputs are observed according to different time differences. The performance parameters are analyzed in detail. The implementation will continue with the digital controller, vertical and horizontal scanners. The main achievements of this work can be summarized as follows;

1. Different LIDAR types and TDC techniques are investigated. The pulse-based (dToF) LIDAR is decided.
2. The system architectures of the PLLs are investigated based on the required silicon area, jitter, and power consumptions. The charge-pump PLL with ring oscillator architecture is chosen. The VCO outputs are used as 125MHz DLL.
3. The system architectures of the TDCs are investigated. It is seen that the TDL requires a small silicon area, offers a fast sampling rate and good timing resolution. The TDL requires a well-defined gate delay time. A DLL is used to control the delay time of the TDL delay gates. The TDL is an event-driven architecture that decreases power consumption significantly.
4. A basic counter is used together with the TDL. The counter generates the MSB codes, and the TDL generates LSB codes. In that way, the TDC has a very high resolution and a high range.

5. Each block is verified individually. The stability and phase noise simulations are performed for the DLL and PLL. The total jitter is much less than 0.5LSB.
6. The first 4 PLL output phases are sampled at the column. The sampling of the phases increases the resolution of the TDC. Also, they are multiplied to have a fast clock signal at the columns.
7. The power consumption of the Column – Parallel TDC is 20.5mW at nominal and 48.9mW at worst case.
8. The linearity parameters INL and DNL of the TDC are both +2/-1LSB.
9. The dimensions of the recommended LIDAR SoC dimensions are 4.4mm on X-axis and 3.8mm on Y-axis. It covers a 16.72mm$^2$ silicon area.

Besides the achievements, some items should be carried out as future work.

1. The TDC will be implemented together with a SPAD array.
2. The linearity of the TDC should be improved further. INL and DNL should be less than 0.5LSB.
3. There is flexibility in the PLL and DLL. After verifying the operation, the power consumption and silicon area will be optimized by removing the flexibilities.

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