JUNE 2021 Ph.D. in Electrical and Electronics Engineering OMAR KANAAN NOORI ALBASRI

REPUBLIC OF TURKEY

GAZIANTEP UNIVERSITY

GRADUATE SCHOOL OF NATURAL & APPLIED SCIENCES

DEVELOPMENT OF MULTI-LEVEL INVERTER FOR POWER QUALITY ENHANCEMENT

Ph.D. THESIS

IN

ELECTRICAL AND ELECTRONICS ENGINEERING

BY

OMAR KANAAN NOORI ALBASRI

JUNE 2021

DEVELOPMENT OF MULTI-LEVEL INVERTER FOR POWER QUALITY ENHANCEMENT

Ph.D. Thesis

in

Electrical and Electronics Engineering

Gaziantep University

Supervisor

Prof. Dr. Ergun ERÇELEBİ

by

Omar Kanaan Noori ALBASRI

June 2021

DEVELOPMENT OF MULTI-LEVEL INVERTER FOR POWER QUALITY ENHANCEMENT

submitted by **Omar ALBASRI** in partial fulfillment of the requirements for the degree of Doctor of Philosophy in **Electrical and Electronics Engineering, Gaziantep University** is approved by,

Assoc. Prof. Dr. Mehmet İshak YÜCE
Director of the Graduate School of Natural and Applied Sciences …….....

Prof. Dr. Ergun ERÇELEBİ
Head of the Department of Electrical and Electronics Engineering …….....

Prof. Dr. Ergun ERÇELEBİ …….....
Supervisor, Department of Electrical and Electronics Engineering
Gaziantep University

Exam Date: 8 June 2021

Examining Committee Members:

Prof. Dr. Ergun ERÇELEBİ …….....
Thesis Supervisor, Department of Electrical and Electronics Engineering
Gaziantep University

Prof. Dr. İlyas EKER …….....
Department of Electrical and Electronics Engineering
Çukurova University

Assoc.Prof.Dr Mete VURAL …….....
Department of Electrical and Electronics Engineering
Gaziantep University

Asst.Prof.Dr Serkan ÖZBAY …….....
Department of Electrical and Electronics Engineering
Gaziantep University

Asst.Prof.Dr Emrah IRMAK …….....
Department of Electrical and Electronics Engineering
Alanya Alaaddin Keykubat University

I hereby declare that all information in this document have been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Omar Kanaan Noori ALBASRI

ABSTRACT

DEVELOPMENT OF MULTI-LEVEL INVERTER FOR POWER QUALITY ENHANCEMENT

ALBASRI, Omar Kanaan Noori
Ph.D. in Electrical and Electronics Engineering
Supervisor: Prof. Dr. Ergun ERÇELEBİ
June 2021
112 Pages

The objective of this thesis is to develop and improve the performance of the multi-level inverter. Two paths have been followed in the development and improvement works. The first one represents the off grid connected multi-level inverter. The trend is focused to increase the number of the level at the output of the inverter while the inverter represents the main energy source. In the second path followed in the studies, the grid-connected multi-level inverter has been considered. Power quality enhancement has been done by developing the control unit of grid connected multi-level inverter in such a way to ensure the stability of the system against the system voltage sag. The multilevel inverters designed in the thesis are both simulated using a computer software program and implemented in hardware. The developed inverters are multilevel and hybrid inverters. Conventional inverters give five levels in the output waveform. These inverters contain two H-bridge circuits to generate different levels at the output while the hybrid inverter developed in the thesis includes three H-bridge circuits to form different levels at the output. Moreover, developed hybrid inverter can also operate in conventional mode when it is supplied with equal sources. The output of each H-bridge has been connected in a cascaded form. The sum of the individual H bridges voltages represents the final inverter voltage. Experimental results on the developed circuits gave satisfactory results and confirmed the accuracy of the design.

Key Words: Low Voltage Ride Through (LVRT), Photovoltaic Panel (PV), Multi Level Inverter, Maximum Power Point Tracking (MPPT), Active And Reactive Power Control.

ÖZET

GÜÇ KALİTESİNİ ARTIRMAK İÇİN ÇOK SEVİYELİ EVİRİCİNİN GELİŞTİRİLMESİ

ALBASRI, Omar Kanaan Noori
Doktora Tezi,Elektrik ve Elektronik Mühendisliği
Danışman: Prof. Dr. Ergun ERÇELEBİ
Haziran 2021
112 sayfa

Bu tezin amacı, çok seviyeli eviricinin performansını geliştirmek ve iyileştirmektir. Geliştirme ve iyileştirme çalışmalarında iki yol izlenmiştir. İlki, şebekeye bağlı olmayan çok seviyeli eviriciyi temsil etmektedir. Eğilim, evirici ana enerji kaynağını temsil ederken, evirici çıkışındaki seviye sayısını artırmaya odaklanmıştır. Çalışmalarda izlenen ikinci yolda ise şebeke bağlantılı çok seviyeli evirici ele alınmıştır. Şebeke bağlantılı çok seviyeli evirici kontrol ünitesi, sistemin sistem gerilim düşmesine karşı kararlılığını sağlayacak şekilde geliştirilerek güç kalitesi iyileştirmesi yapılmıştır. Tezde tasarlanan çok seviyeli eviriciler, bilgisayar yazılım programı kullanılarak hem simüle edilmiş hem de donanımsal olarak gerçekleştirilmiştir. Geliştirilen eviriciler, kademeli çok seviyeli ve hibrit eviricilerdir. Geleneksel eviriciler, çıkış dalga biçiminde beş seviye vermektedirler. Bu eviriciler, çıkışta farklı seviyeler oluşturmak için iki adet H-köprü devresi içerirken, tezde geliştirilen hibrit evirici, çıkışta farklı seviyeler oluşturmak için üç adet H-köprü devresi içermektedir. Ayrıca geliştirilen hibrit evirici, eşit kaynaklarla beslendiğinde konvansiyonel modda da çalışabilmektedir. Her bir H köprüsünün çıkışı kademeli bir biçimde bağlanmıştır. Bireysel H köprü gerilimlerinin toplamı, son evirici gerilimini temsil etmektedir. Geliştirilen devreler üzerinde yapılan deneysel sonuçlar tatmin edici sonuçlar vermiştir ve tasarımın doğruluğunu onaylamıştır.

Anahtar Kelimeler: Alçak Gerilim Geçişi (AGG), Fotovoltaik Panel (FP),Çok Seviyeli Evirici,Maksimum Güç Noktası Takibi (MGMT), Aktif ve Reaktif Güç Kontrolü.

"Dedicated to my family"

ACKNOWLEDGEMENTS

In the name of Allah, the most Merciful, the most Gracious. I would like to present my great thanks to my supervisor Prof.Dr.Ergun Ercelebi for his guidance and support along the path of my current process. Thanks a lot, to my father & mother who never stop inspiring me with love& care to go on.

TABLE OF CONTENTS

Page

LIST OF TABLES

Page

LIST OF FIGURES

Page

LIST OF SYMBOLS

T	Time
D	Duty cycle
C	Capacitor
L	Inductance
VA	Volt Amper
F	Fahrad
H	Henry
P	Active Power
Q	Reactive Power
V	Voltage
I	Current
W	Watt
VAR	Volt-Amper reactive
S	Second
HZ	Hertz
D	Duty Cycle

LIST OF ABBREVIATIONS

AC	Alternating Current
CHB	Cascaded H Bridge
STATCOM	Static Synchronous Compensator
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
VSC	Voltage Source Converter
SPWM	Sinusoidal Pulse Width Modulation
EMI	Electromagnetic Interference
PV Panel	Photovoltaic panel
MPPT	Maximum Power Point Tracking
MLI	Multilevel inverter
PWM	Pulse Width Modulation
CCM	Conduction Current Mode
DCM	Discontinuous Current Mode
FFCM	Fundamental Frequency Control Method
FWCBCM	Full wave Charge Balance Control Method
LVRT	Low Voltage Ride Through

CHAPTER I

INTRODUCTION AND BACKGROUND

1.1 Introduction

The thesis work is briefly listed in this chapter and the work problem is clarified. The functionality of this thesis is composed of many software simulations of multi-level inverter connected with power system to achieve stable active and reactive power compensations with unbanded load disturbances. The simulations work also presents many topologies of a multi-level inverter. The performance analyses of the proposed inverters in stand-alone operation or on-grid operation are studied. The modified inverter unit is utilized also in static synchronous compensators (STATCOM) to keep the system voltage stable and fixed against the load variations by compensating or absorbing reactive power to or from the grid.

Concerning the hardware, the conventional and hybrid inverter modules have been designed. The output of these modules can analyze the benefits of the proposed hybrid inverter over the classical topology inverters.

1.2 Background

Over the past decades, the increase of crude oil price triggered alternative power supply such as solar power, wind, and wave energy [1,2]. The solar system is particularly the most attractive renewable source of energy due to its advantages such as quiet operation, relatively small size, reliability, and positive impact on the environment [3,5], etc.

Many developing countries encourage and fund renewable energy integration. They see that it is necessary to use the considerable sunlight intensity. So today, solar power plants are being built to use this infinite energy. The lack of light and the partial shading are its most drawbacks because energy is absorbed only when there is light. Thus, procedures have been followed to make use of such energy in light absence. In this case, we need a battery and various maximum power tracking techniques have

been modified to obtain constant maximum power output from solar energy. Many algorithms are emerged to fix the partial shading of the PV field or the imbalanced voltage sag. Inverters are used to convert the DC energy of the PV panels to AC current where most industry and home appliances and grid standards need this kind of energy. The increasing trend of a large-scale grid with solar power generation (PV) requires converter optimization in this combination. The objective of the optimized inverter is to maximize the transmitted power into the grid with minimum harmonics and losses profile in such a way that maintains the grid standard connection such as frequency, phase angle and amplitude value [6].

As a comparison between conventional two-level and multilevel inverters,it is possible to get higher efficiency with multi-level inverters and that comes behind these types of inverters using low voltage drop switches. The prompting for multi-level inverter installment is increased while these inverters decrease the voltage stress on the switches without the output filter, mitigate the electromagnetic interface and evolve the power quality.

The multi-level inverter can be classified into three main types: diode clamped or natural point clamped (NPC), flying capacitor (FC) and cascade H bridge inverter(CHB). These three types of inverters are considered the main classical types of multi-level inverters. It is also possible to combine the classical topologies to generate more output levels. This type of inverter is called a hybrid inverter. It is recognized that cascaded multi-level inverter has fetched better concern for its capability on medium /high power operations and other benefits for instance: superior power quality, lower order harmonics, less switching losses and the mitigation of electromagnetic interference (EMI) [7]. These aforementioned advantages are capable of generating a required stepped AC voltage waveform from DC voltage sources as inputs. Other inverters are good too, although they have the following drawbacks:

In term of efficiency, it is high with diode clamped inverters but if there is a concern to increase the number of output levels there would arise with their diode number and then there are boosting in cost and control complexity.

Flying capacitor multilevel inverters are similar to diode clamped inverter in their operation principles only in that it uses a capacitor to reserve voltage level. The advantages of flying capacitor multi-level inverter can be summarized in their ability to control the active power and reactive power flowing. However, this topology has a complex and an inefficient voltage control.

1.3 Problem Explanation

According to what was mentioned in the background above, industrial growth and urban demand have led to energy shortages around the world during all past periods. These solar panels use sunlight density. However, there are some issues when using this feature. The intensity of the sun changes throughout the day. The temperature also changes, which affects the efficiency of the photovoltaic panel. And as there is no sunlight at night, therefore, we need an algorithm that can draw maximum power from the PV array and a process that can charge the battery to use that energy in the absence of sunlight. Therefore, a DC-DC converter is required to charge the battery stably.

In power electronics, the conversion unit is called the inverter, the inverter output must be stable and it has low harmonic output, so it is necessary to utilize an inverter that ensures an ideal total harmonic distortion (THD) and excellent efficiency. Multi-level inverters have become more publicly known because of their best consequences compared to traditional two-level inverters.

The thesis is divided into two parts: a computer program simulation and hardware implementation of the multi-level inverter. By using the Simulink libraries, the simulations have been achieved in the program of the computer simulation. Simulations performed in Simulink include charging the battery using PV panel, perturb and observe algorithm (MPPT) [7]. Different topologies of the multi-level inverter are implemented in the simulation work. Concerning the second part which represents the hardware modules, a cascaded multilevel inverter and the hybrid inverter have been designed. The cascade conventional inverter gives a five-level output while the hybrid inverter supplies fifteen levels of semi sin waveform. To attain various levels of voltage, an excellent switching method should be used.

1.4 Thesis Target

The simulation of modified multilevel inverter and the problem solving of the voltage sag problems with the grid-connected multilevel inverter represent the main target of this thesis. The conventional and the modified cascaded inverters will be implemented in the hardware module to verify the theoretical results.

1.5 Thesis Methodology

The methodology used is as follows:

- Collect information related to the simulation of a photovoltaic system.
- Develop models with computer simulation programs using Simulink.
- Charging using a buck-boost converter and battery model.
- Maximum power point tracking implemented using perturb and observe algorithms.
- Simulation model validation and testing.
- Implementation of multi-level inverters technology for hardware set up.
- Obtain results and evaluate hardware modules.

1.6 Outlines Of The Thesis

Chapter 1: mentions the generic introduction of the problem explanation and the target of the thesis.

Chapter 2: presents the previous studies concerning thesis work.

Chapter 3: represents the background of the detailed components for this thesis.

Chapter 4: Analyzes simulations and results.

Chapter 5: contains the hardware modules analysis and implementation results.

Chapter 6: concludes the thesis work.

CHAPTER II

LITERATURE AND PREVIOUS WORK SURVEY

2.1 Related Work In The Literature

A new method for mitigation the inter-harmonics of a PV system is proposed in [8]. The inter-harmonic is considered as an emerging power quality challenge in grid-connected photovoltaic (PV) systems. The sampling rate of the MPPT algorithm has a great impact on the inter-harmonic characteristic of the PV system. A higher sampling rate increases the power efficiency while increasing the harmonic contains. The proposed procedure optimizes the MPPT algorithm in such a way that specifies the sampling rate between the fast and the slow values which effectively reduces the inter-harmonic in the output current waveform. The proposed method has been validated experimentally on a single-phase PV-connected system.

Karanayil et al. [9] worked on a central three-level PV converter under partial shading conditions. A maximum power point tracking loses its functionality when used with two or more PV panels to gain higher DC link voltage. So, a new configuration is proposed when multiple arrays are used in a cascaded manner with each other. This method used an auxiliary converter that feeds the central diode clamped inverter. In this method, the PV panels will operate at their maximum values which guarantee higher power production for all PV units. Simulation and hardware work implementation verified the proposed method.

Carrasco et al. [10] proposed an analog multiplication method for maximum power point tracking. Basic multiplayer can be used for harvesting the peak power that the PV cell produces, however, this basic multiplayer causes discrepancy between the actual power and the PV voltage. It may be shown that its maximum follows the maximum of the power curve of the panel. The proposed multiplier allows complete analog coincide of actual power with PV power.

The novel maximum power point tracking algorithm presented by Hu et al. [11], the developed MPPT strategy work for dual active bridge three-phase converter integrates with large scale PV energy source by medium DC link voltage. This converter kit

could boost the DC link voltage and extract the peak power point of the PV in a synchronization manner. High average power efficiency is achieved by optimizing the stray inductance and transformers turn ratio to specify the maximum power point of PV despite the environmental conditions. The proposed control method has been verified in both simulation and scale-down hardware prototypes.

Pachaivannan et al. [12] presented a plant height optimization algorithm (PHOA) for crowded PV plants to gain the maximum power point. The tuning process for this algorithm was developed to calculate the accurate duty cycle (D) for the DC converter with pi controller assistant to ensure maximum power extraction. PHOA found the most stable height for the PV farm as a numerical value and considered it as the optimal for the farm. This optimal high value will convert to duty ratio fed to the converter. Despite the weather conditions (D) was continuously adjusted which ensures DC output stabilization. The comparison between the proposed method and the perturb and observe method is done with simulation software program /Simulink frame work confirms the robustness and accuracy of the optimization method.

Selvakumar et al. [13], presented a high-speed maximum power point tracking algorithm. The proposed algorithm works with DC boost converter integration to optimize global power point under partial shading condition with minimum tracking time. As a comparison between the proposed MPPT method and other methods like perturb and observe the proposed process ensures high speed, high efficiency, and super performance under different weather conditions. The proposed high-speed MPPT controller beats both duty sweep and particle swarm optimization based on MPPTs. Validation is done for this method in both simulation and scale-down hardware modules.

Nami et al. [14] designed a novel H bridge multi-level pulse with modulation topology which joined in a cascade connection the high voltage diode clamped inverter with a traditional converter (low voltage). In this method, arrangement for DC link voltage is done by keeping the neighboring switching vector between voltage levels to maximize the produced output levels with minimum solid-state requirements. The proposed configuration has a very low total harmonic distortion of voltage and currents waveforms, thus the filter can be minimized. Simulation and hardware implementation outcomes under different modulation indexes are listed to confirm the validation of the proposed method in power quality improvement.

Batschauer et al. [15] submitted a novel hybrid multi-level inverter for medium voltage application. This inverter is composed of a conventional two-level inverter connected in series with a half-bridge module for each phase. According to this configuration, the major portion of the produced energy can be gained through VSI by utilization of a unique multi- pulse rectifier. The residual amount of energy is processed within the half-bridge modules so that a reduction in the galvanically insulated requirement for the DC source occurs. Modularity is born naturally. The modulation method for four levels is proposed and analyzed in detail. This scheme is to allow uni-directional power flow on all DC power supplies to make the diode bridge available for the rectification input stage for uni-directional applications.

Gautam et al. [16] studied two new structures of hybrid multi-level inverter based on the symmetrical and asymmetrical framework and appealable for renewable energy, machine, and drives. Employing the proposed methods leads to a reduction in the required component number, DC sources, and less installation area when compared with conventional topologies. The problem of the capacitor voltage balancing is mitigated in this method which represents an essential advantage especially since the balancing process occurs regardless to the load type, load unbalancing, and modulation index. For switching control the multi-carrier pulse with modulation method is used in this work, both simulation and experimental work are used to verify the validation of this study.

Manyuan Ye et al. [17] presented a hybrid modulation technique for the cascaded hybrid multi-level inverter. The cascade hybrid inverter could extend to a higher number of output levels when compared with the conventional inverters. When the general hybrid pulse width modulation is used, uneven distribution for the output power between the high-voltage and low-voltage H-bridge occurred and a power transfer between the high-voltage cell and the low voltage cell appeared causing voltage boost in the low-voltage cell capacitor. A modified hybrid pulse with a modulation method based on power balance is developed to solve this problem. With the hybrid modulation method, the power balancing among the H-bridge cells is avoided with improved performance of the inverter. The simulation and experimental implementation of the proposed method prove their robustness and accuracy.

Apurv Kumar Yadav et al. [18] presented a single DC link hybrid multi-level inverter using low voltage devices. The proposed topology is composed of a five-level diode

clamped inverter and three-level type inverters. Low voltage switches are used in this method with three floating capacitors. The balancing process for these capacitors is done by the pulse width modulation (PWM) switching duration using switching-state redundancies for each pole-voltage level. The voltage control algorithm is proposed for floating capacitors and the DC link stack capacitor is independent of load power factor and modulation index. Field-oriented close loop control, open-loop V/f, and steady and transient states are proposed to verify the above claims.

Lei Wang et al. [19] proposed a hybrid static synchronous compensator that has a higher compensation range with low DC link voltage. Firstly, the circuit for this hybrid STATCOM is discussed and then the I/V characteristics have been analyzed. A comparison between the proposed STATCOM and C-STATCOM is done in this work to verify the performance and advantages of the studied topology. A new control method for hybrid STATCOM is designed to ensure the operation of this method under different types of disturbances like unbalanced current, voltage dip, and voltage fault. The wide compensation range for the hybrid STATCOM has been verified in simulation and experimental works.

Saleh Ziaeinejad et al. [20] studied a new method for selecting DC side voltages distribution static synchronous compensator (D-STATCOM). This compensator is installed in a distribution system to inject reactive power in case of voltage dip. The controller of a D-STATCOM regulates its DC-side voltage and provides the required reactive power. The new method proposed in this work is used for choosing the trade-off reference value of the DC-side voltage of STATCOM to reduce switching loss and the total harmonic distortion for the output current without affecting the responsibility of the d-STATCOM. The estimation method for determining the parameter requirement for this DC voltage estimation method is also presented. The effectiveness of the proposed method is examined through experimental results.

Rajiv K. Varma et al. [21] presented a novel smart inverter PV-STATCOM where a photovoltaic inverter can be controlled as a dynamic reactive power compensator STATCOM. The proposed study provides complete voltage control during system disturbances. At night, the capacity of the inverter is used for STATCOM operation. In system disturbances during the day, the smart inverter temporarily stops the actual power generation function (about a few seconds) and frees its full inverter capacity used for STATCOM operations. After removing the interference responding to grid voltage control needs, solar farms are back to actual power generation before

disturbance. Performance of the PV-STATCOM is evaluated through both EMTDC/PSCAD simulations and laboratory hardware implementation using d-SPACE control.

Hesamaldin Maleki et al. [22] introduced a novel control approach for photovoltaic (PV) system as static synchronous compensator (STATCOM) which is called a PV-STATCOM system. The proposed STATCOM unit can immediately mitigate oscillations in the transmission system. When disturbances cause power oscillation, the proposed control strategy cuts solar power generation for the same period which the disturbance takes and changes the functionality of STATCOM to oscillation damping in this period. When power oscillation is suppressed, the solar power plant returns the active power before the disturbed state and activates the damping mode. The simulation results show a significant increase in power transfer capability during both internal and interarea oscillation modes. As a comparison between the proposed method and the conventional STATCOM control method, the proposed method can significantly reduce the cost of the utility providing oscillation mitigation.

Ghazal Falahi et al. [23] studied and analyzed modular multilevel converter (MMC) performance as VSC based on HVDC systems during disturbances conditions like voltage dip and fault. A new control strategy to improve the low voltage ride-through performance is proposed also in this work, this control method allows the system to generate the necessary active and reactive power by a mathematical calculation based on the capability of the MMC-HVDC system and LVRT requirements. The injected active and reactive power values follow the LVRT guidelines are identical to different grid codes. Simulation works by EMTDC/PSCAD verified the performance of the proposed method.

Nayan Kumar et al. [24] presented a new robust and adaptable sliding mode (SM) control of grid-connected photovoltaic (PV) system based on the cascaded two-level inverter (CTLI). Modeling and design of control schemes for grid-connected photovoltaic systems based on CTLI were developed to provide effective reactive power and variable solar radiation. A vector controller was developed in consideration of the maximum output of PV. Two different switching methods are used in the designing of the SM controller. The study was conducted under similar operating conditions. Instead of using space vector pulse width modulation (SVPWM) technology, simple PWM modulation technology is used to perform SM controller.

A. Ghafouri et al. [25] presented a static synchronous compensator system (STATCOM) with a fuzzy logic control unit instead of conventional controllers like PID control [25]. Fuzzy controller can contribute effectively to utility power enhancement due to the nonlinear capability that makes it more robustness and reliable against many system disturbances. Neural network techniques are used in this work for adjusting the parameters of the proposed controllers which lead to improve performance of the system. A single machine infinite bus system is implemented to verify the accuracy of the proposed techniques.

Umesh Kumar Rathod et al.[26] studied a new generation static synchronous compensator (STATCOM) which used modular multi-level inverter occupied the conventional converter.This presented combination could increase the power transfer limits and dynamically improve the power quality. The above-mentioned advantages come due to the scalable technology for the modular multi-level converter (MMC) which can increase current and voltage.The new generation STATCOM with MMC has been discussed with different configurations in this work. The series-parallel configuration gives the best performance than series or parallel configuration. The work implemented in simulation software program Simulink is to confirm the results.

Prashant M. [27] presented a hybrid power system connected to the grid through the STATCOM unit which maximizes the dependency of the hybrid energy sources like wind energy and photovoltaic power while these sources cannot maintain their power delivery at all time. This article has improved power quality at the coupling point. The daily load is a continuous variable. Customers want high-quality electricity that is continuous and reliable power. This means that customer demand can continuously increase. This condition affects both source and power quality.

Young-Tae Jeon et al. [28] presented a low capacitance static synchronous compensator (LC-STATCOM) with a new method for active shaping of the capacitor voltage. Conventional LC -STATCOM can be operated with a high voltage ripple capacitor during rated current while reducing the current beyond the standard limit which removes the advantages of LC-STATCOM such as high current quality and low switches losses. The method of active shaving of the capacitor voltage aims to maintain a large voltage ripple across the capacitor by using a simple boost converter to ensure continuous functionality of the LC-STATCOM. Simulation work preformation accentuated the high performance of the method.

CHAPTER III

BACKGROUND OF PV SYSTEM THROUGH MULTILEVEL INVERTER

In this chapter, the comprehensive study of all the components used in the work is explained in detail such as DC-DC converters, PV panel control system, and multilevel inverters. The battery charging process is done through a DC-DC converter with the proper maximum power point tracking algorithm with the PV panel at the first stage.

3.1 DC-DC Converter

Many industrial applications require different levels of DC voltage. So, to generate the demanded levels of DC voltages to meet the requirements of the appliance, a DC-DC converter must be used. The conversion process is based on one of the two modes: linear mode or switched mode. If the current flow doesn't reach the zero point, the converter works in a continuous conduction mode (CCM) while in a discontinuous conduction mode (DCM) the current reaches zero.

DC-DC converters can also be classified into isolated converters and non-isolated (switch mode) converters. Buck-Boost converter has been used in this work and it is enrolled under (switch mode) non-isolated topology. This converter is able to operate in buck or boost mode so that the output voltage will either step up or step down. Dual operation of this mood guarantees the right tracking of maximum power point of PV panels. The duty cycle value must be increased or decreased to achieve the expected result of the operation [29].

3.2 Switch Mode DC-DC Converter Types

Switch-mode DC-DC converter has a DC path between its input and output. Switch-mode DC-DC converter designs mainly employed by ICs are specifically intended for that purpose. The switch mode DC-DC converters have the following divisions:

- Boost Converter

- Buck Converter
- Buck-Boost Converter
- Cuk Converter

An inductor,a capacitor, and a diode are components of the switch-mode converter. The input voltage and the duty cycle that the switch supplied specify the output voltage.

3.2.1 Boost Converter

Stepping up the voltage is done by the boost converter to equip the load demand. It is known that power is fixed in the electrical system and thus increasing the voltage while decreasing the current to meet the same power ratings. At least two semiconductor switches are used in the circuit of this type, which are a diode and a transistor. The inductor is used as an energy storage element. The ripple removing process is done by connecting a capacitor on the output or input side.

The operation principles are given as:

1. The inductor current is continuous and this is made possible by selecting an appropriate value of L.
2. The inductor current in a steady-state rises from a value with a positive slope to a maximum value during the ON state and then drops back down to the initial value with a negative slope. Therefore, the net change of the inductor current over any complete cycle is zero [30].

On and Off states operations are the basic keys for the operation of the boost converter: The ON state means that the inductor is charged while the OFF state means that stored energy in the inductor is freed as current passes through the diodes. A boost converter topology is shown in figure 3.1.

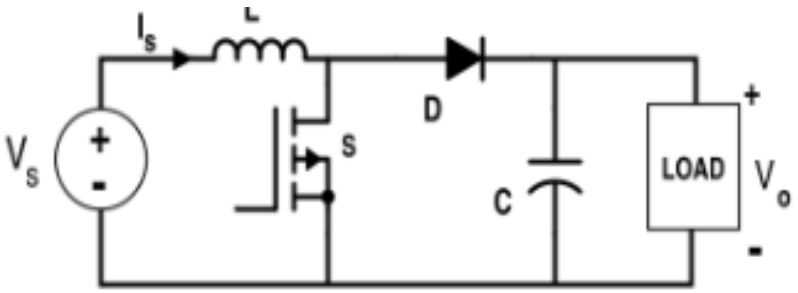


Figure 3.1 Circuit for the boost converter

3.2.2 Buck Converter

These kinds of converters are also named Choppers. Step Down Chopper or Buck converter reduces the input DC voltage to a specified DC output voltage. Buck converters are basically used in power supplies that split the main power supply into smaller ones. The computer system power supply uses a buck converter to step down the voltage to other components.

The input voltage source is joined with a controllable solid-state device which acts as a switch. The switch can be a power MOSFET or IGBT. Thyristors are not typically used in DC-DC converters. To turn a Thyristor a DC-DC circuit another commutation circuit is required. By simply making the voltage between the gate and the source terminals of a power MOSFET, or, the voltage between gate and collector terminals of the IGBT goes to zero power MOSFET and IGBT can be turned off.

The diode is the second switch. To reduce the ripple contains in voltage and current, a low pass filter LC filter is designed [31]. A buck converter topology is given in Figure 3.2.

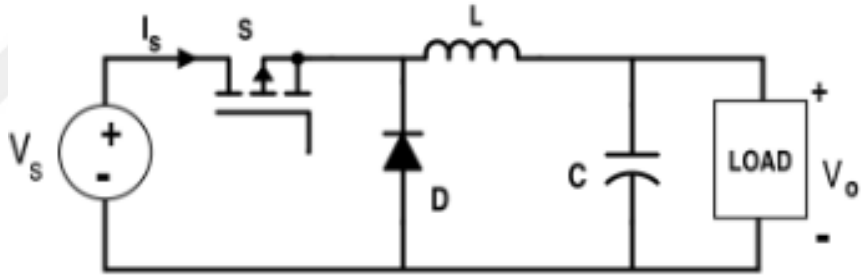


Figure 3.2 Circuit for the buck converter

3.2.3 Buck-Boost Converter

Depending upon the duty cycle which feeds the semiconductor switch, a buck-boost can operate in step-up or step-down modes. Typically, a buck-boost converter contains the same component as a boost converter but the arrangement is made differently. The output voltage of this converter type is given by 3.1 equation:

$$VOUT = -VIN.D/(1-D) \quad (3.1)$$

Where D is the duty cycle of the controlled switch.

The minus symbol indicates that the output voltage of this type has an inverse polarity related to its input [32]. Figure 3.3 shows the circuit for the buck-boost converter.

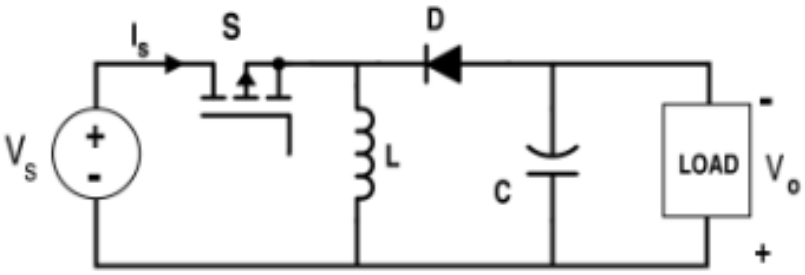


Figure 3.3 Buck-boost converter circuit

3.2.4 Cuk Converter

Cuk converter is another type of DC-DC converter, it performs the functionality of buck-boost converter so that it can work as boost and buck converter. A buck converter is installed on the right side while the boost converter is to the source side. For energy storage purposes a capacitor is used[33].

Cuk converter is similar to other converters in that it works in continuous and discontinuous modes. The Cuk converter consists of dual capacitors, dual inductors, and a single switch with a diode as shown in Figure 3.4.

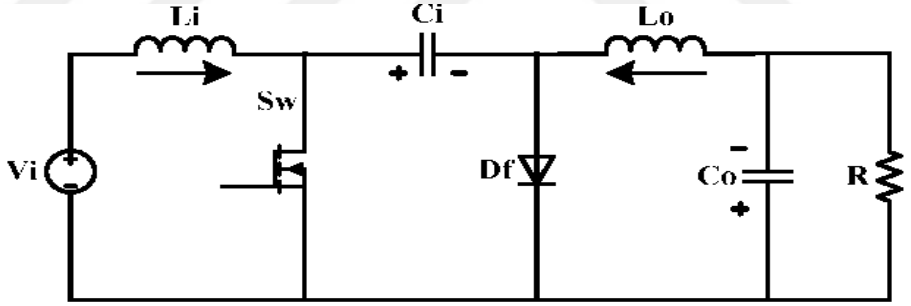


Figure 3.4 Cuk converter circuit

3.3 Maximum Power Point Tracking Algorithm (MPPT)

Photovoltaic panels have some constraints such as temperature and irradiation limits. To operate it with the maximum available power, an algorithm should be inserted with the charge control unit. This algorithm is called the maximum power point tracking algorithm (MPPT). The maximum power from these panels lies in the region where the PV panels support their maximum voltage and it is known by the maximum power point of the panel. Changing the solar density and ambient temperature are the most active parameters which can affect the available power of the PV panels. Extracting

the maximum power from the PV panels is considered an essential duty of MPPT algorithms

3.4 Operation Of Maximum Power Point Tracking

The chief operating basis of the maximum power point tracking algorithm is the maximum available power got from the solar panel. Tracking the peak power point of the panel is the best means to achieve that. MPPT ensures the required current and voltage for the battery to track the maximum power point of the PV.

Voltage and current are the most important parameters in power tracks. As more current is drawn, the voltage goes down, and vice versa. MPPT algorithm acts best under the following states:

- In cold temperatures, PV panels can work better.
- In deeply discharged or less charged cases MPPT can supply the required charge to keep the battery charge.

MPPTs are widely used nowadays due to some more advantages than other controllers like PWM charge controllers.

MPPT is commonly used in high power systems to provide more efficient voltage and current capacity. Higher voltage can be obtained at a low temperature to keep the battery charge. It is easier than other controllers for providing better voltage when the battery is low besides operating very efficiently.

One of the cons of this controller is that its being expensive when compared with the PWM controller and its requirement for the proper tune. Many topologies can perform the maximum power point tracking algorithms but we use to perturb and observe method due to its simplicity and cost-effectiveness. It is also considered as the most applicable method for hardware setup [34].

3.5 Perturb And Observe Algorithm

The main problem of the MPPT method is automatically finding the voltage VMPP or current IMPP, and at a certain temperature and irradiance, the solar array can provide maximum power at this voltage. In the P & O method, the MPPT algorithm is based on sampling PV array current and voltage to calculate PV output power and power variation. The tracker works by periodically increasing or decreasing the voltage on the solar array. If the PV output power increases/decreases due to a specific

disturbance, the subsequent disturbance is generated in the same/opposite direction. Changing the DC chopper duty cycle and repeating the process result in maximum power point. In fact, the system vibrates around the MPP. Reducing the perturbation step minimizes vibration. However, reducing the step size will reduce the MPPT speed. Figure 3.5 shows IV and PV characteristics of the PV system[35].

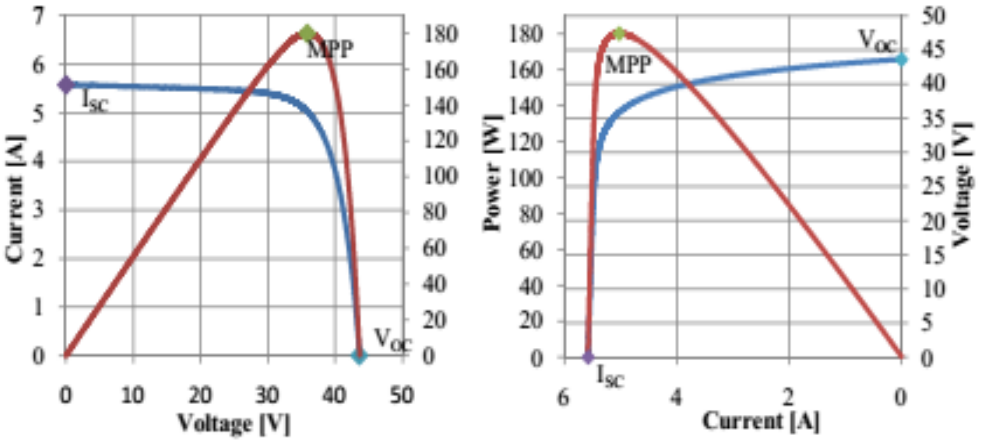
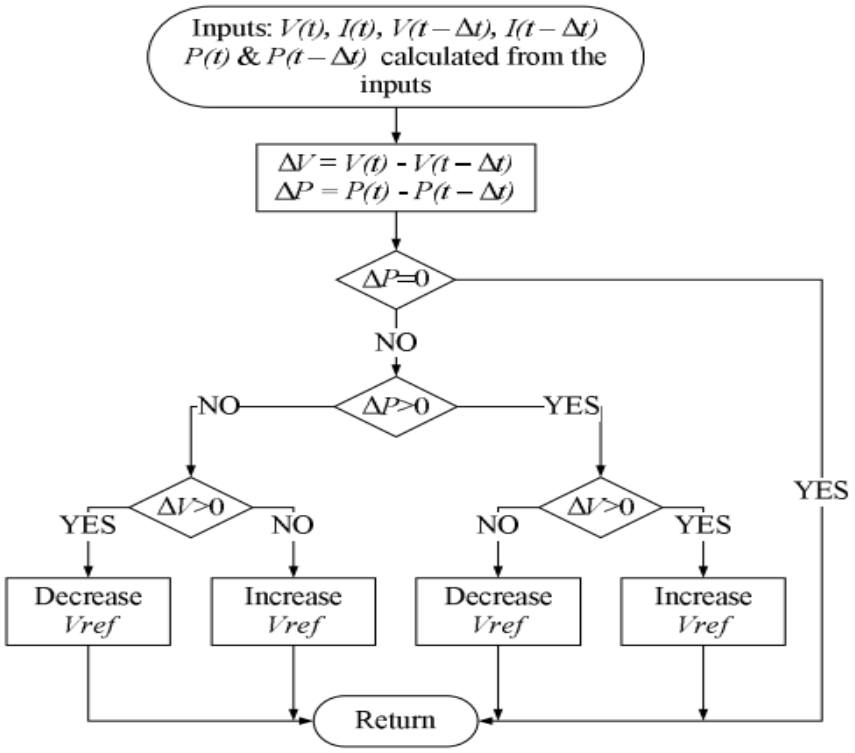


Figure 3.5 Characteristics curve of a pv panel

Figure 3.6 shows the flow chart for perturb and observe method.



.

Figure 3.6 Flow chart for perturb and observe method

3.6 Multilevel Inverters

An inverter is an electrical device or a circuit that performs the function of converting the direct current into an alternating current while a rectifier does the inverse duty. Conventional inverters output contains two levels only (+VDC, -VDC) and that is why it is suffering from a high harmonic distortion profile. The term multilevel inverter refers to the construction of inverters to gain the multi-levels of voltage at the output and harvesting a high-power quality that approximating to pure AC sin wave. The modified outputs waveform makes it possible for us to use multilevel inverters with high power rated sites.

3.7 Types Of Multilevel Inverters

The configuration circuit of each multilevel inverter has a different application. Some of the most common applicable kinds of multilevel inverters are discussed below as follows:

3.7.1 Diode Clamped Multilevel Inverter

Diode clamped multilevel inverter is considered the first emerged topology for multi-level inverters. The circuit here consists of diodes and series DC bank capacitors. Diodes are used for voltage blocking purposes to minimize voltage stress on the power devices. (2n-2) switches and (n-1) sources are necessary for an n-level diode clamping inverter. The low capacitance usage in this type makes it suitable for back-to-back converters. The main disadvantages of this type occur when a higher number of levels are required and consequently the number of the utilized diodes increases. Hence, there is a limitation for this type with higher-level usage [36]. Figure 3.7 shows the five-level diode clamped inverter.

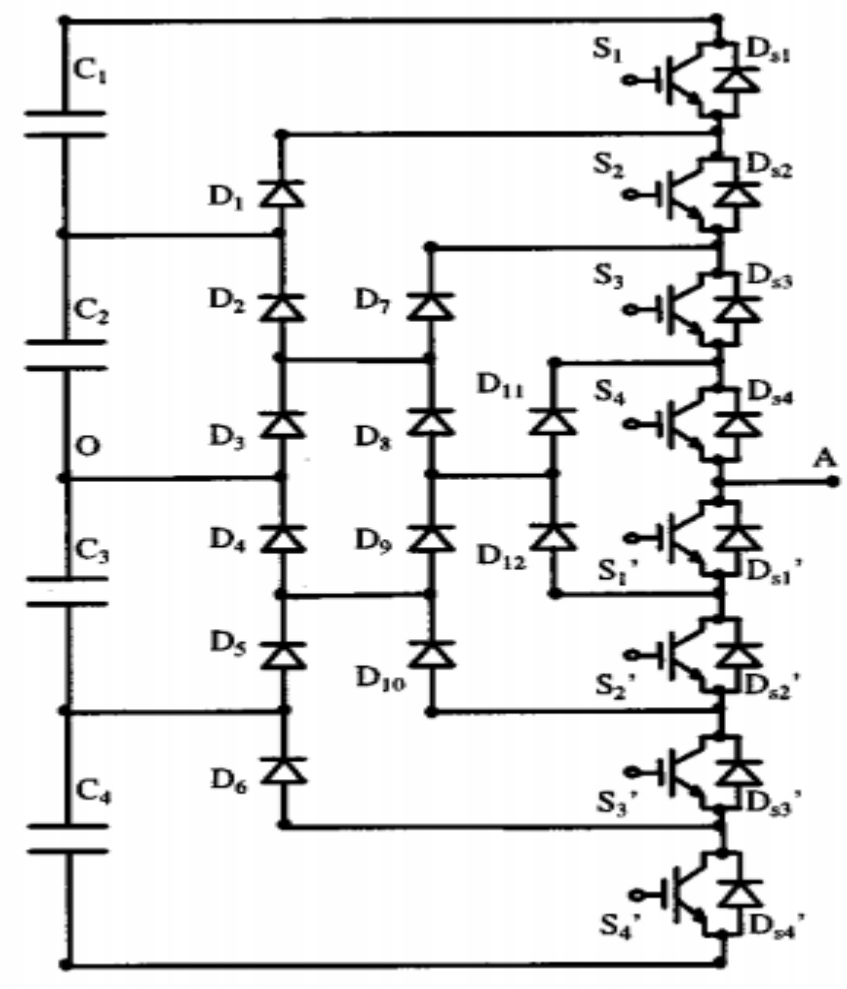


Figure 3.7 Circuit for the five-level diode clamped inverter

Table 3.1 shows the switching for a five-level diode clamped inverter.

Table 3.1 Diode clamped inverter switching table

Voltage Vector	Switch Table							
	S1	S2	S3	S4	S5	S6	S7	S8
VDC/2	1	1	1	1	0	0	0	0
VDC/4	0	1	1	1	1	0	0	0
0	0	1	1	1	1	1	1	0
-VDC/2	0	0	0	0	1	1	1	1
-VDC/4	0	0	0	1	1	1	1	0

3.7.2 Flying Capacitor Multilevel Inverter

Flying capacitor multilevel inverter includes the same operational principles for diode clamped inverters but there is only one difference in that flying capacitor multi-level inverter uses capacitors for voltage restrain. The input DC voltages are divided by the capacitors in this topology. This inverter also utilizes the same equipment's number used for an N-level diode clamped multilevel inverter. The main disadvantages related to this type of inverters are complex voltage control and the lack of efficiency [37]. Figure 3.8 shows the circuit diagram of the five-level flying capacitor inverter.

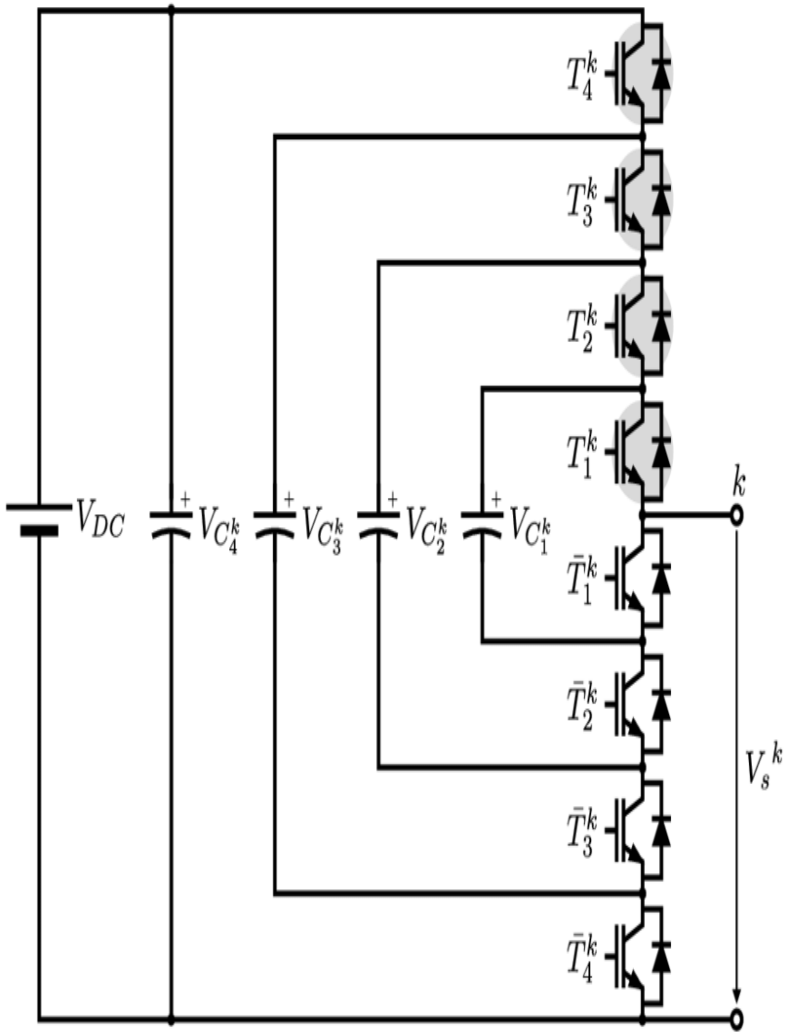


Figure 3.8 Flying capacitor inverter circuit

The inverter switching state for the flying capacitor multilevel inverter is listed as follows in Table 3.2.

Table 3.2 Switching table for flying capacitor inverter

Switching states	Output voltages	DS1	DS2	DS3	DS4	DS5	DS6	DS7	DS8
+1	Vdc/2	1	1	1	1	0	0	0	0
+2	Vdc/4	1	1	1	0	1	0	0	0
0	0	1	1	0	0	1	1	0	0
-2	-Vdc/4	1	0	0	0	1	1	1	0
-1	-Vdc/2	0	0	0	0	1	1	1	1

3.7.3 Modular Multilevel Inverters

Modular multilevel inverters represent the modified version of cascade H bridge inverter since it works under the cascaded staircase with reduced harmonics principles. The necessity for this type arose when the conventional two or three-level inverters could feed only low or medium voltage application while most industry nowadays demands high-level inverters. Figure 3.9 shows the circuit diagram for the modular inverter.

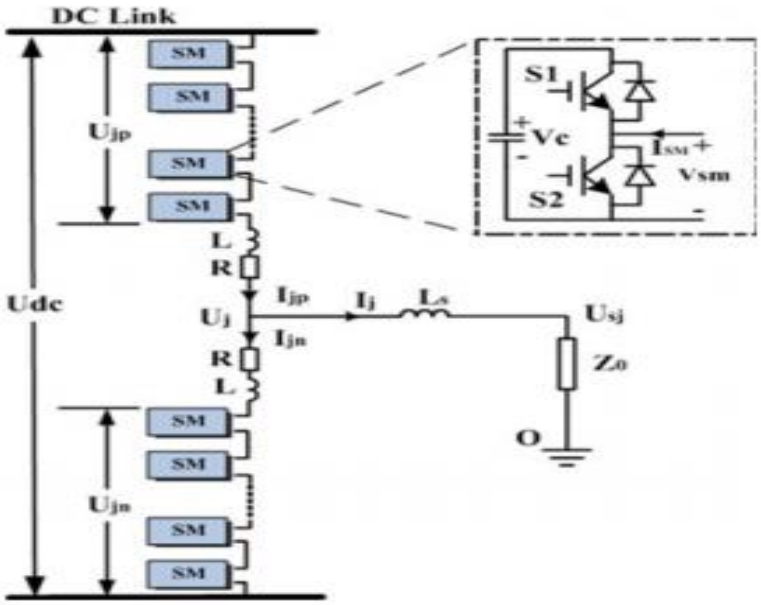


Figure 3.9 Single-phase five-level modular inverter

Half bridges or sub-modules are connected in a specific manner to produce the requested voltages. Complexity with voltage balancing of the upper and lower arms results in the difficult hardware implementation of these multilevel inverters [38]

Table 3.3 shows the switching status for the modular inverter.

Table 3.3 Modular MLI switching table

Vload	Sm1	Sm2	Sm3	Sm4	Sm5	Sm6	Sm7	Sm8
VDC/2	0	0	0	0	1	1	1	1
VDC/4	1	0	0	0	0	1	1	1
0	1	1	0	0	0	0	1	1
_VDC/4	1	1	1	0	0	0	0	1
_VDC/2	1	1	1	1	0	0	0	0

3.7.4 Cascaded H Bridge Multilevel Inverter

The cascade H bridge multi-level inverter is considered one of the most vital types of multi-level topologies. The distortion is a problem caused by a simple four-switch inverter that produces a square. A square wave combined from multiple frequencies and affects the power efficiency. That's why this simple four-switch inverter is not applicable for high power efficiency applications. Therefore, when a multi-level inverter is used, a square wave is close to a sin wave type. The higher number of the voltage level, the higher sin wave similarity that contains more fundamental harmonics and more power efficiency.

There are several benefits of the cascaded H bridge multilevel inverter such as it needs fewer components than NPC and FC converters, it is cheaper and lighter than NPC and FC converters, and possible soft switching by using the switching technique. This configuration provides better efficiency and less THD [39].

3.7.4.1 Symmetric Cascade H Bridge Multilevel Inverter

Cascaded H bridge inverter can be divided into symmetric and asymmetric inverters. When all the DC input sources are the same, then they are called symmetric multilevel inverters. Most applications use this symmetrical configuration of inverters while it requires a unique input voltage. Therefore, using them at various voltage levels (such as PV panel systems) is not a very effective technique. Maintenance costs also increase because the charging process of such systems is different [40].

3.7.4.2 Asymmetrical Cascaded H-Bridge Multilevel Inverter

The asymmetric multilevel inverter has unequal input DC voltages that are not similar to each other. Maximum output amplitude, higher voltage level, and reduction of semiconductor devices,unlike the symmetrical ones, can be achieved. Such technology is suitable for photovoltaic systems where different voltage levels can be obtained. A cost-effective inverter with few components is essential for operation[14].

3.7.5 Hybrid Multi-Level Inverter

Hybrid multi-level inverter usually uses hybrid configuration, hybrid DC sources, or hybrid devices in a specific way to generate the output with reduced DC sources. High conversion efficiency with a smaller number of switches and low switching frequency mean low switching losses in such a manner that it is flexible to enhance various topologies for different applications. The circuit configuration and pulse control method are the most important parameters to classify the hybrid multi-level inverters [41].

Several methods and approaches have been found and adopted for these multilevel inverters modulation and control. The switching modulation techniques are mainly divided into two types: fundamental switching frequency schemes and a high switching frequency PWM scheme.

3.8 Control Techniques

The inverter switches are driven ON or OFF by the control technique and so the inverter can draw the objective output. The discussion of some of these control techniques is below.

3.8.1 Sinusoidal Pulse Width Modulation Technique

This method is considered one of the most applicable techniques to control the multi-level inverter. This method can eliminate the low frequency harmonics for the inverter output waveform so it is very popular and dependent in many industrial applications. Carrier signal which represents a high-frequency triangular wave is used, and it is compared with a reference copy of the desired sinusoidal waveform as a modulating wave. Distortion and the switching losses are reduced when using this method [42].

Figure 3.10 shows the flow chart for generating the SPWM.

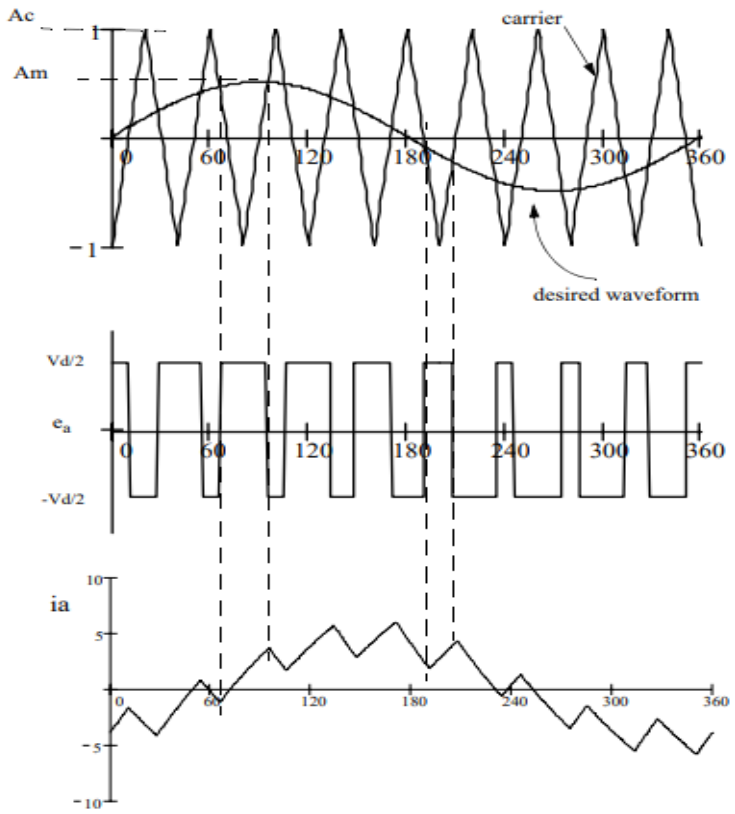


Figure 3.10 Flow chart for generating the SPWM

3.8.2 Space Vector Pulse Width Modulation (SVPWM)

Space vector pulse width modulation technique is one of the real-time modulation techniques which is widely used in digital control or voltage source converter. Equation (3.2) shows the duty cycle for the individual vector to obtain the required output from the inverter.

$$V^* = \frac{(T_j V_j + T_{j+1} V_{j+1} + T_{j+2} V_{j+2})}{T} \tag{3.2}$$

This technique ensures less ripple and total harmonic distortion in the output current with easy implementation on hardware as well as makes it suitable to use for high power applications. When there is an increase in the number of levels that the inverter supplies, there will be an increase in the complexity of the switching state, thereby decomposing the number of space vectors into smaller numbers makes it easier to calculate the duty cycle [43]. The following Figure 3.11 shows the three-level inverter with eight space vectors using the technique of space vector modulation.

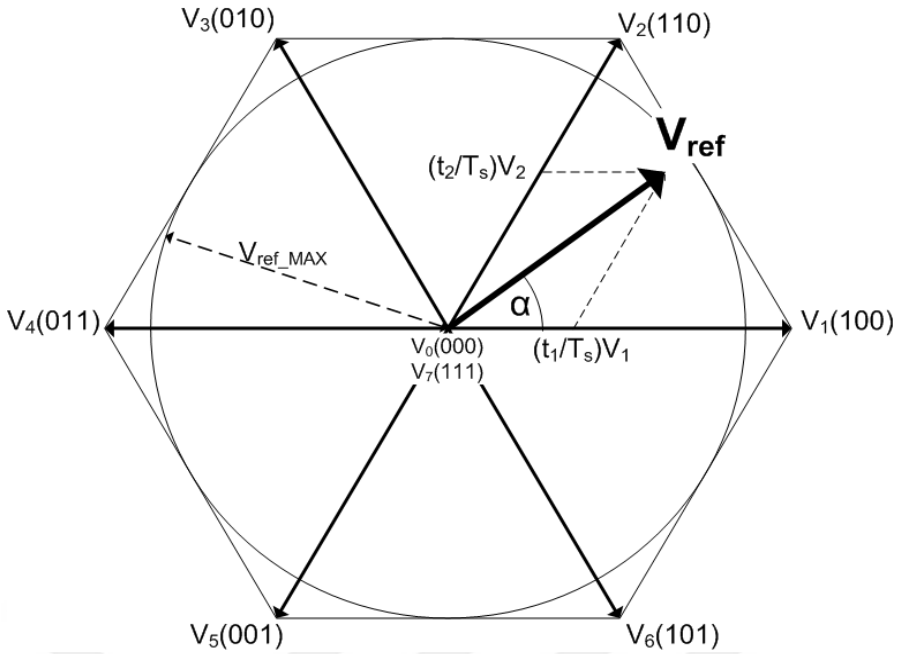


Figure 3.11 The three-level inverter with eight possible space vectors

3.8.3 Fundamental Frequency Control Method (FFCM)

Fundamental frequency control method is another control method. It operates with a low switching frequency with less switching losses and high quality. The different charge conditions of the used DC sources represent the essential drawbacks of this method which increase the inverter maintenance cost [44]. To overcome the impact of charge changing, the charge balance control technique is used to ensure equal charge status with all the DC sources.

CHAPTER IV

SIMULATION RESULTS

4.1 Introduction

All the simulation results related to this thesis are shown here in this chapter. These experiments can be classified into two main parts: off-grid simulation and on-grid simulation. Robust conditions are used to examine the simulation performance.

4.2 Results Of Off-Grid System

4.2.1 Off-Grid System With Asymmetrical Cascade H Bridge Inverter

In this simulation work, a cascade H-bridge multilevel inverter model designed with a conventional H-bridge unit is used. By increasing the number of output voltage levels, the inverter can give a better sinusoidal waveform. Using asymmetric voltage distribution between the H bridge cells instead of the symmetric method and by using the charge balance control method lead to the cardinal modification of this work. Moreover, the power drawn from each H-bridge will be equalized. This process results in increasing the battery life of the inverter.

To make a comparison between the mentioned conventional topologies and this new topology, we find that the new one has a reduction in the component count with 42 %. The next section introduces the control techniques and simulation results besides the operation principles of the proposed inverter [45].

Each full-bridge inverter can produce three different voltage output levels. The basic duty of the multilevel inverter is to synthesize the objective voltage by summing the separate voltages obtained from batteries, fuel cells, or ultra-capacitors.

Figure 4.1 shows V_o the output voltage of the cascaded inverter and it can be evaluated by adding the following voltages of V_{o1}, V_{o2} and V_{o3}.

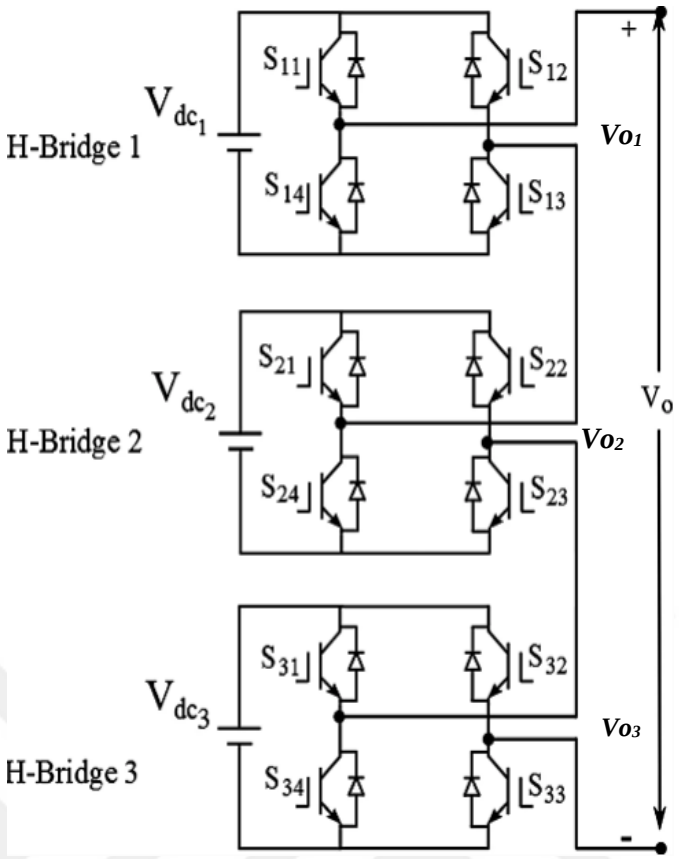


Figure 4.1 Conventional cascade H-bridge inverter

In symmetrical voltage distribution, the produced numbers of voltage levels N_{LEVEL} from this inverter are directly related to the number of the connected H bridge N, according to Equation 4.1.

$$N_{LEVEL} = 1 + 2N \tag{4.1}$$

The maximum output voltage V_{max} can also be given as DC sources used with the following equation:

$$V_{max} = NV_{dc} \tag{4.2}$$

From chapter two of the literature review mentioned above, it is quite clear that the main interests of improving the produced voltage quality of the inverter are to be the same as international standards. That is done by increasing the levels of the produced output which causes a decrease of the harmonics content. From the symmetrical distribution of DC voltages and according to equation 4.1, it is noticed that producing more levels at the output voltage needs to use more number of DC sources and H-bridges, therefore, there will be an increase in the number of the power electronic

switches, cost, and the inverter size. These things together are considered the most constraints of the symmetrical inverter [46].

To remedy this weakness of symmetric distributions of voltages, asymmetrical topology was depended on in this work. So, the distributions of voltage between the bridge cells will not be equal: for example, if VDC is given to the first H-bridge, the second cell bridge will be 2VDC. By this binary progress, an increment in the number of the produced levels will be gained in the output voltage while the number of DC sources and switches will still the same as in the symmetric method. Equation 4.3 shows the connection between the produced output levels and the utilized H-bridge cells in binary distribution for the dc sources.

$$N_{LEVEL}=4N-1 \tag{4.3}$$

And here another example of using the ternary process distribution of voltages between the bridges: if the first cell is supplied with VDC the second cell will be fed with 3VDC and so on. The output levels number is given as a function with the number of DC sources in Equation 4.4.

$$N_{LEVEL} = 3N+6 \tag{4.4}$$

By comparing the equations (4.3),(4.4) with (4.1), it is clear that the output levels increase in the asymmetrical topology when it is compared with the symmetric method. The values of DC sources in this simulation are based on asymmetrical configurations and sources will be settled according to the binary progress manner.

The charge balance control method is used as a control technique to make the amount of power that is drawn from different batteries equal. Thus, battery life is increased and the meantness cost is reduced. The charge balance control method is implemented due to the possible use of several modulation patterns. After one cycle, the angle will rotate continuously in a full-wave pattern while the angle will rotate after half cycle in the half-wave pattern. If either of these two patterns is used, all the DC sources get charged and balanced except the battery which is used in the first H bridges. The following equation shows the amount of power as :

$$\boldsymbol{P_{Dc}} = \frac{1}{\mathrm{T}}\int_0^{\mathrm{t}} V_o . I_o \ \mathrm{dt} \tag{4.5}$$

Figure 4.2 below shows a schematic of fundamental frequency and the charge balance control methods. This figure has three patterns labeled from up as follows: the fundamental frequency control method is shown in the first pattern and the difference

between the duty cycles of each H-bridge cell is clear here. Such difference indicates this method's drawback. To overcome this drawback, the charge balance control method should occur as appeared in the second and third patterns. Focusing on these patterns, we will see that the duty cycle is the same for each H-bridge cell by using the charge balance method. As a result, every switch will conduct with equal time and so avoiding excessive heat of switches which conduct long time switches. Pattern three represents a charge balance control method but with half-wave swap and that's why it is so named as half-wave charge balance control method [47].

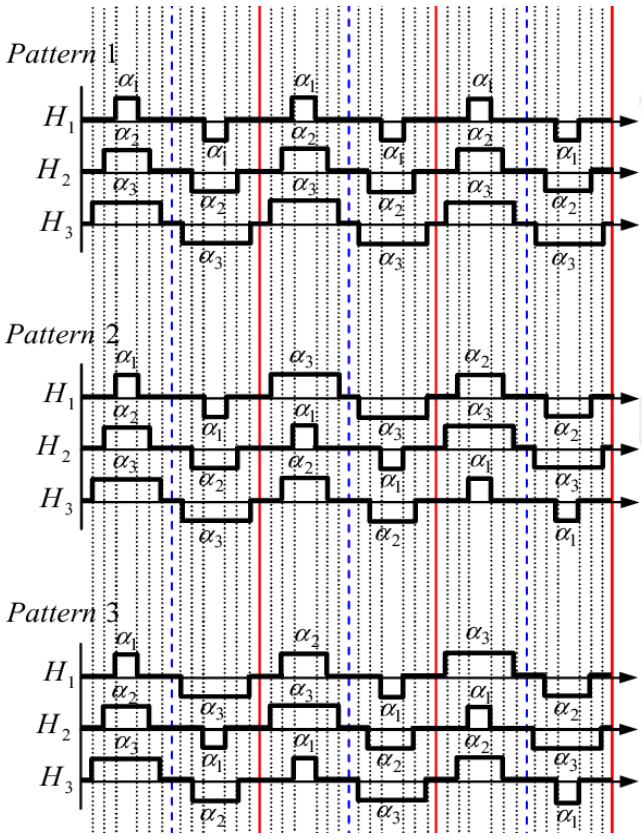


Figure 4.2 Patterns of the fundamental frequency control

The implementation of asymmetric inverter and using charge balance control method are done. In this work, only the first cell will be expected from the implementation of the charge-balanced. The distribution of voltages will be according to binary distribution manner. According to equation 4.3, fifteen levels will be earned by using four H-bridge cells at the output terminals of the inverter instead of nine levels related to the standard symmetrical topology.

The two experiments below prove the operation of the proposed inverter. The first experiment depends on using the fundamental frequency control method while the second one depends on the charge balance control method. These two experiments aim at showing clearly the difference between the two methods and verifying the advantage of the proposed method. The following subsection shows the results of the inverter by using these methods.

4.2.1.1 Results By Using Fundamental Frequency Control Method(FFCM)

The proposed inverter is formed from four H-bridge cells. The following figures show the output of each cell and we can achieve more number of levels by using this method of control. Yet the duty cycle of each bridge is different from each other. That means a different amount of power drawn from each cell is different from that of the adjacent cell.

Figures (4.3),(4.4),(4.5) and (4.6) show the first, second, third, and fourth H bridge outputs waveforms.

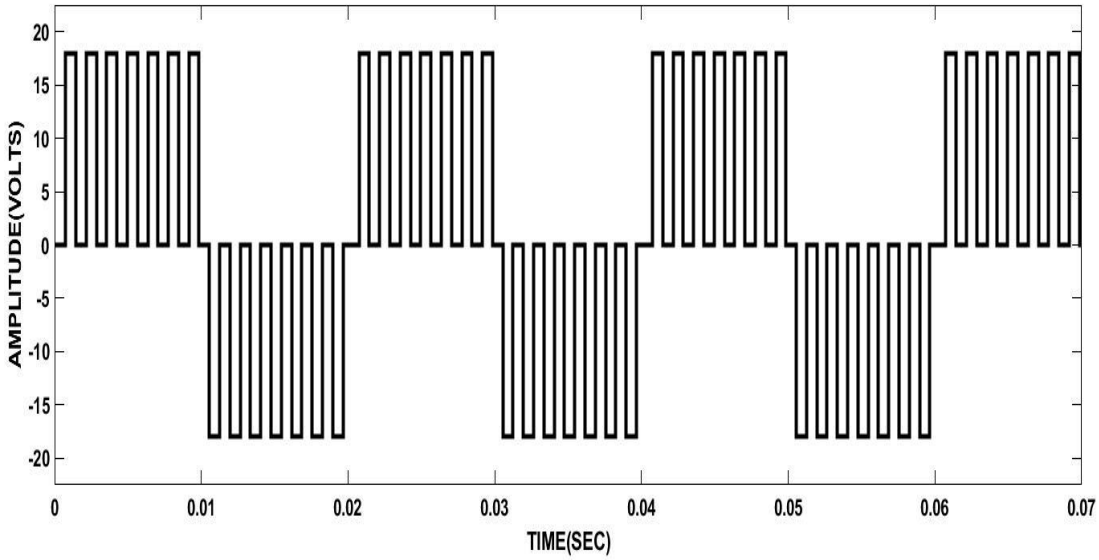


Figure 4.3 Output waveform of first H-bridge based (FFCM)

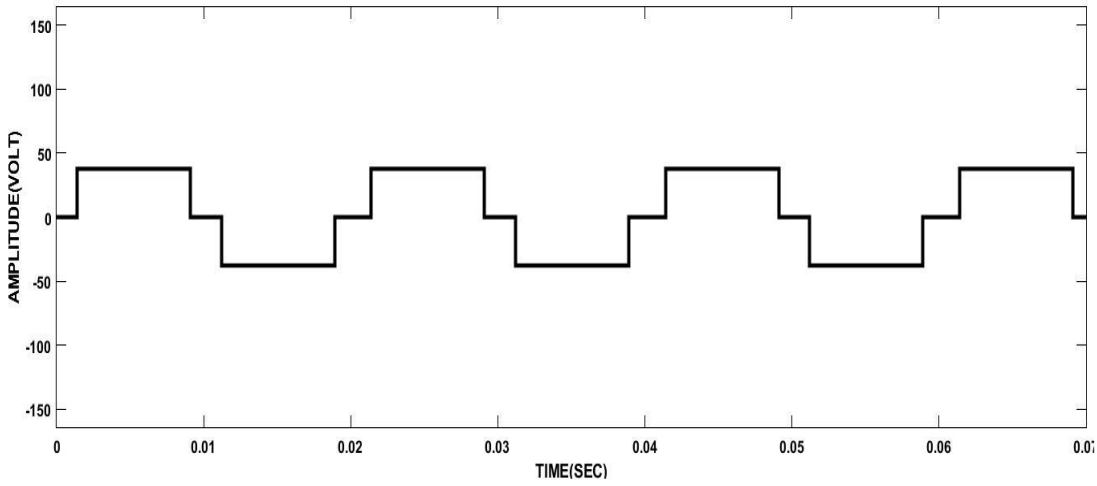


Figure 4.4 Output waveform of second H-bridge based (FFCM)

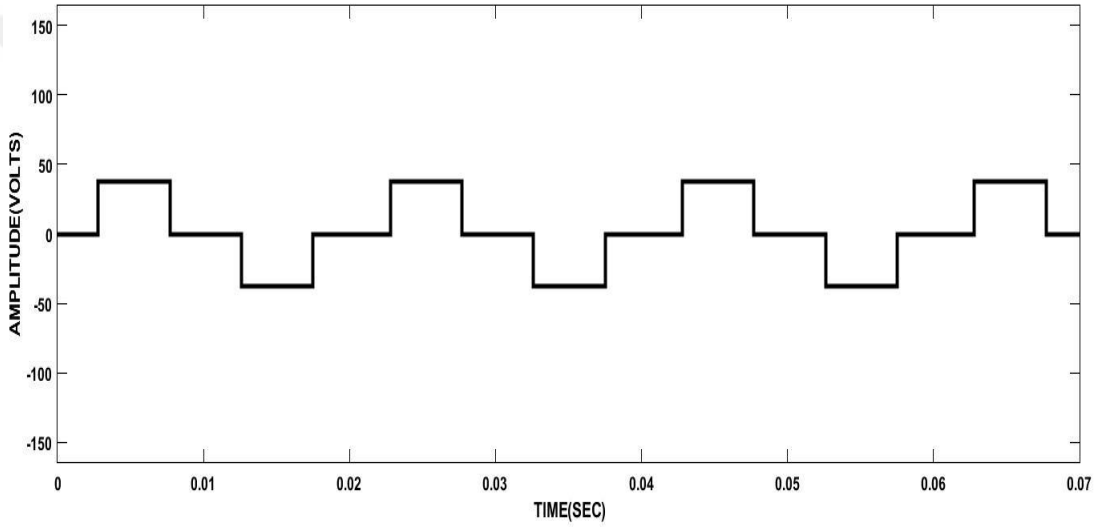


Figure 4.5 Output waveform of third H-bridge based (FFCM)

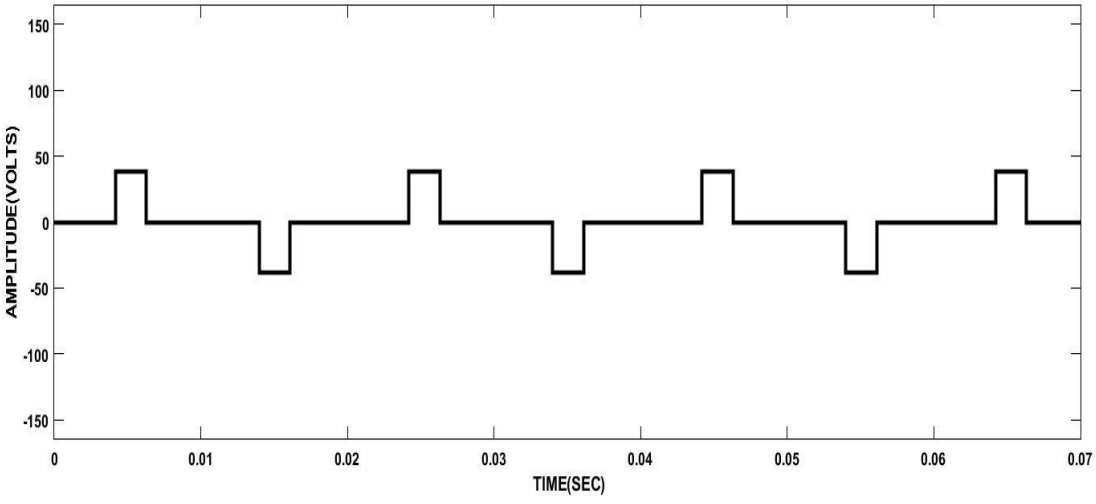


Figure 4.6 Output waveform of fourth H-bridge based (FFCM)

4.2.1.2 Results By Using Charge Balance Control Method(CBCM)

This module utilizes the full-wave charge balance control method. The output of each H-bridge is shown in the following figures. Obviously, by using this method, each H-bridge has an equal on-period or duty cycle.Figures (4.7),(4.8),(4.9) and (4.10) show the first, second, third, and fourth H bridge outputs waveforms.

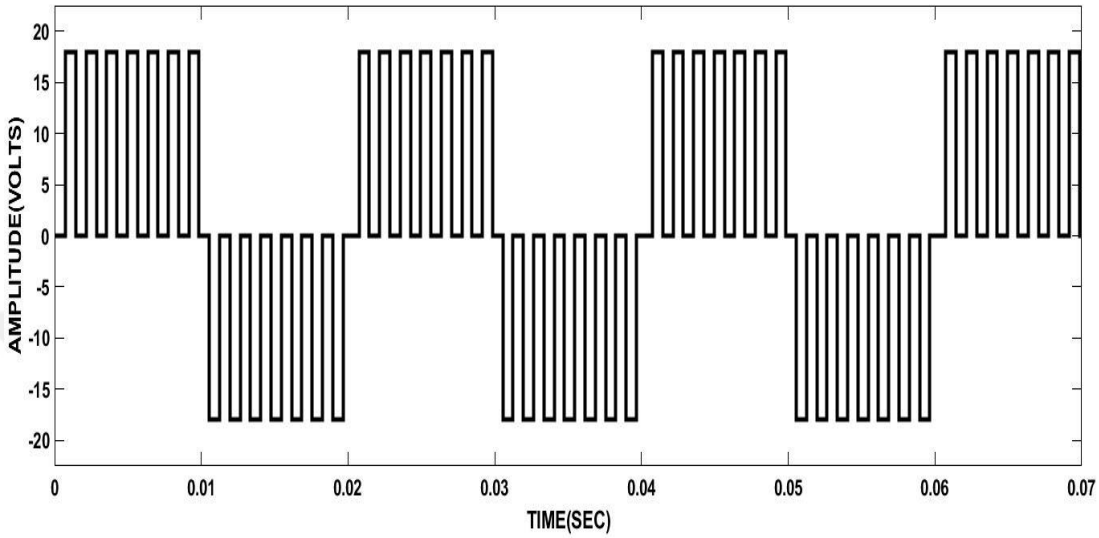


Figure 4.7 Output waveform of the first H-bridge based (FWCB)

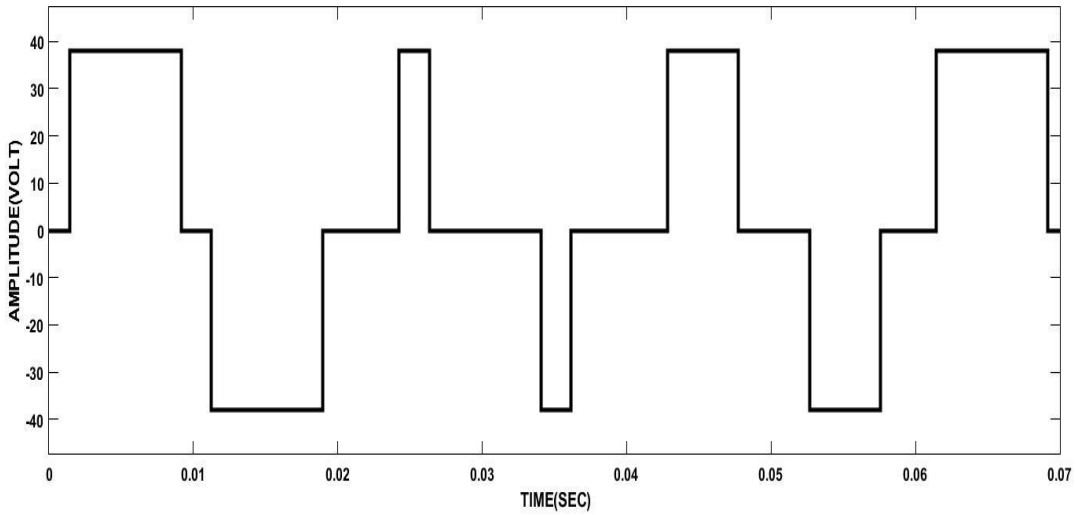


Figure 4.8 Output waveform of the second H-bridge based (FWCB)

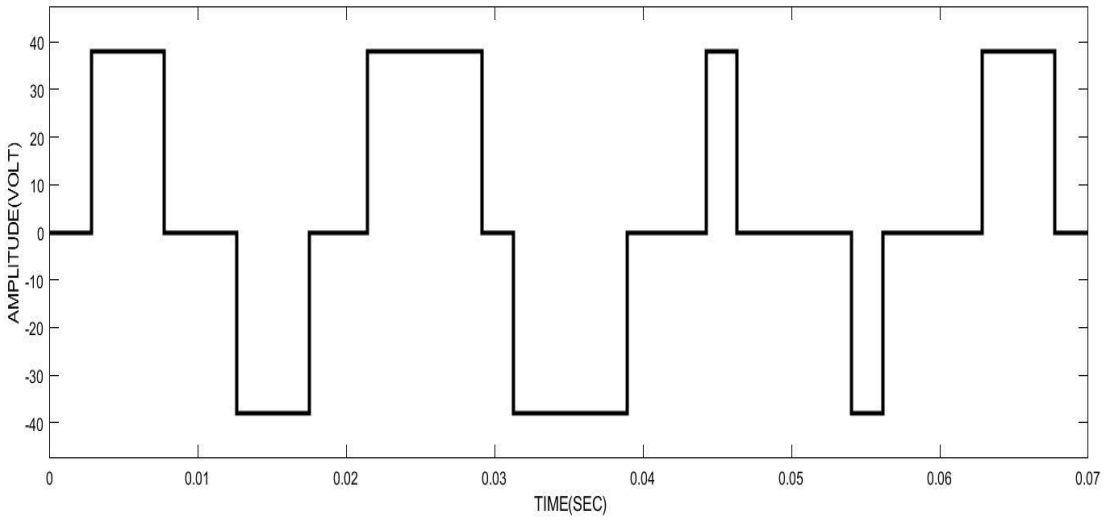


Figure 4.9 Output waveform of the third H-bridge based (FWCB)

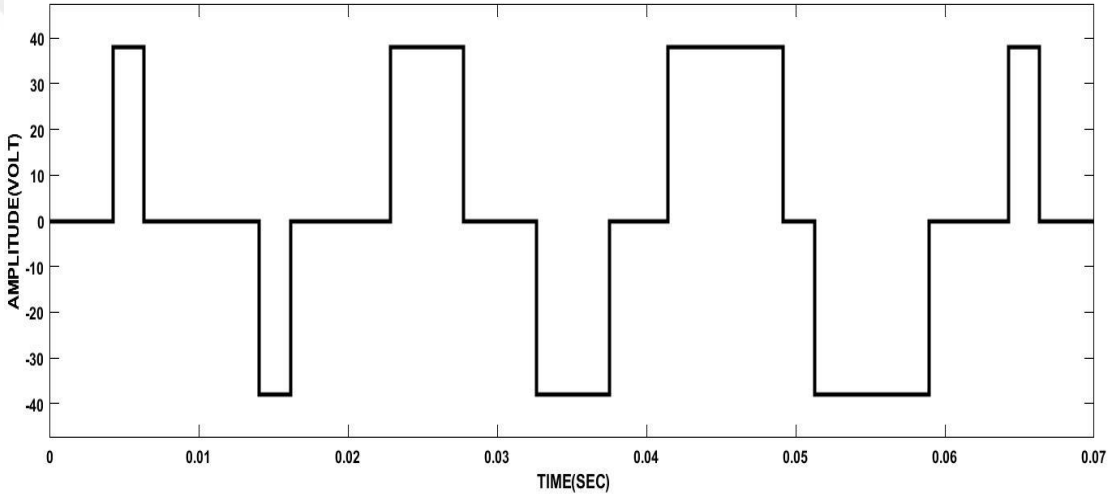


Figure 4.10 Output waveform of the fourth H-bridge based (FWCB)

Figure 4.11 shows the current of the inverter due to the connected RL load of 10-ohm resistance and 200mH inductance.

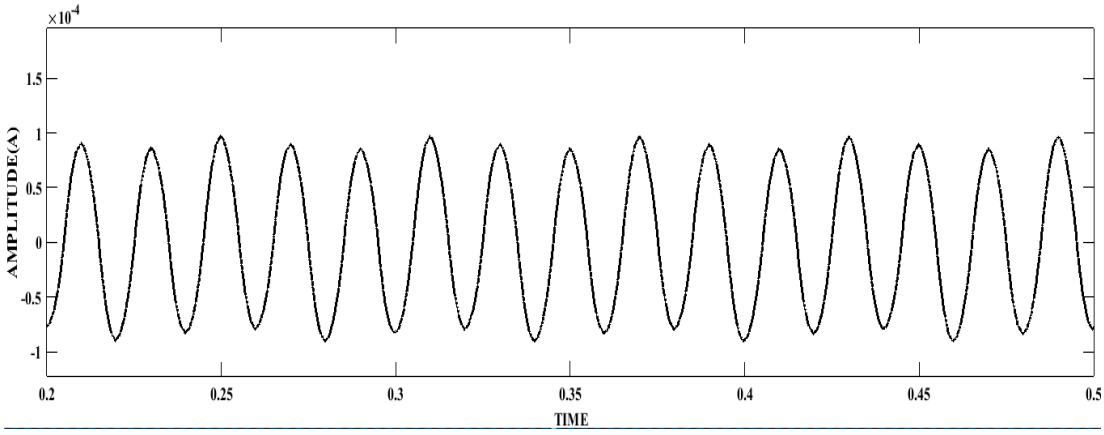


Figure 4.11 Inverter output current

Figure 4.12 shows the fifteen-level output waveform generated from the asymmetrical cascade inverter.

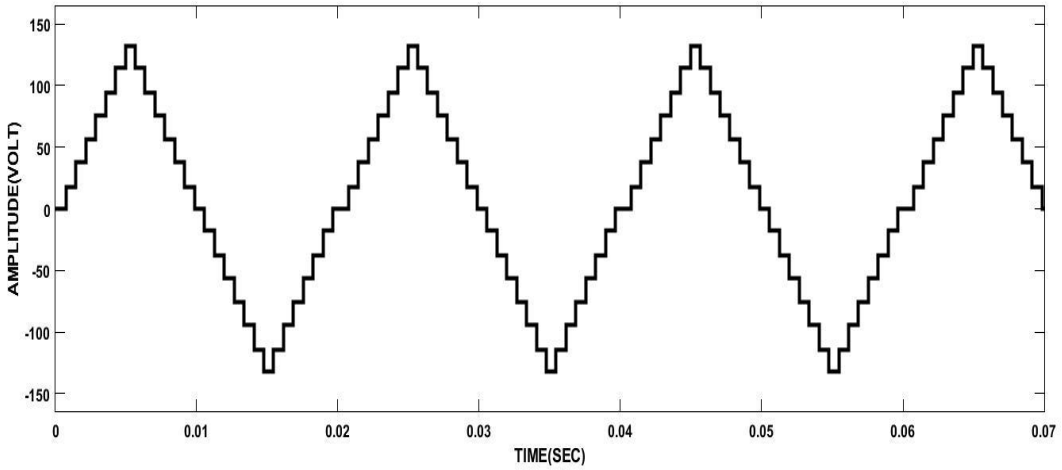


Figure 4.12 Final inverter output waveform

While the harmonic spectrum for the voltage wave is given in figure 4.13.

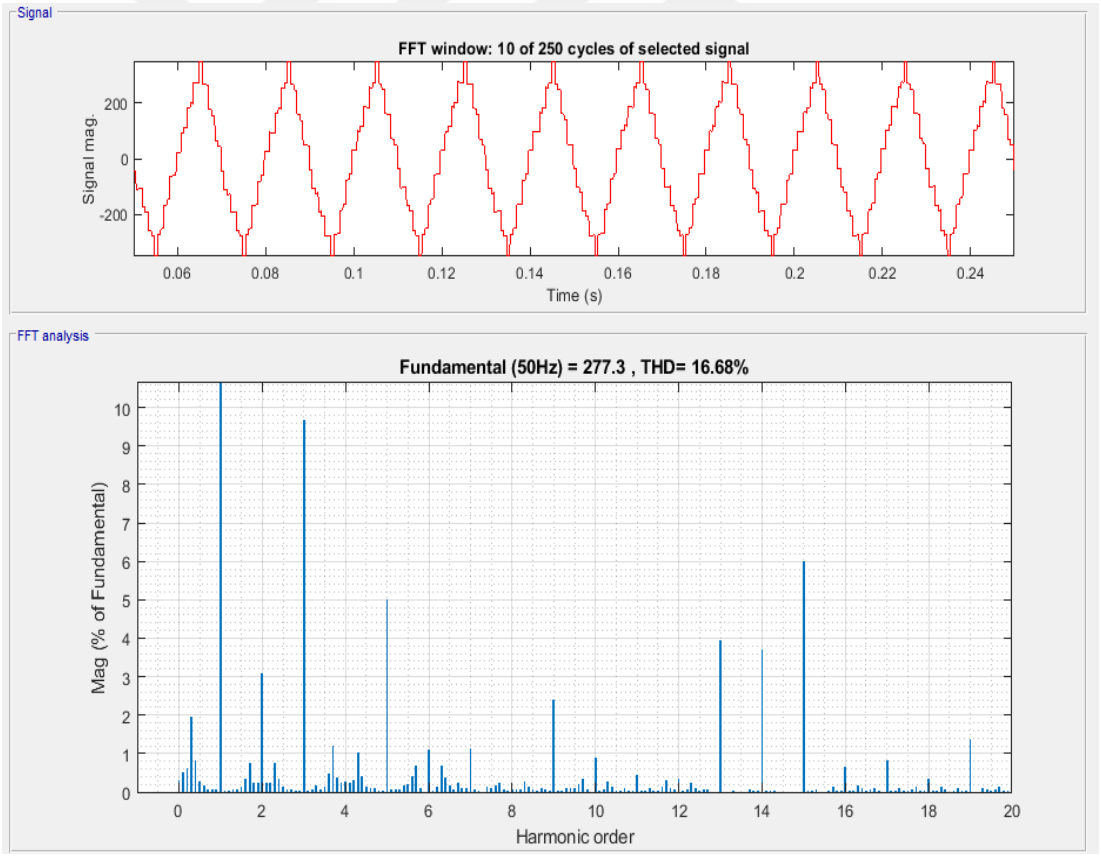


Figure 4.13 Total harmonic distortion for the voltage signal

An improvement in the cascade inverter is done in the two simulations mentioned above. This improvement is related to two points: the first one is the increasing number of the output levels due to the use of asymmetrical topology with a minimum number

of DC sources and semiconductor switches. The second one is equalizing the amount of power from each DC source (except the first source) due to the use of the charge balance control method. The simulation result proves that this inverter is working perfectly.

4.2.2 Off Grid System with Hybrid Multilevel Inverter

The study and simulation of a three-phase nine-level hybrid inverter are presented here. This inverter with its modern circuit used only twelve switches and fed by photovoltaic panels. To pick the maximum PV power, a DC-DC converter with an MPPT algorithm is implemented in this simulation. This study also presents a control technique for this hybrid inverter topology.

This topology requires a fewer number of components and it is more efficient than that of the conventional topology because the inverter operates at line frequency. There is no need for all switches to work in high frequency. So, it results in the simpler and more reliable control of the inverter. To get the output voltage from the hybrid multi-level inverter, two separated generations are there:

level generation and polarity generation. In the level generation, high-frequency switches are essential to produce the required levels. The polarity generator operates at line frequency. Thus, this topology merges the low frequency and high frequency to produce the multi-level voltage output.

The level generator (high-frequency part) generates the positive levels to produce a complete multilevel output. The level generation output feeds the polarity generator (full-bridge inverter) which will provide the output with the polarity it needs. Consequently, a reduction in the number of semiconductor switches will occur.

Figure (4.14) below shows the proposed nine-level twelve switches inverter which consists of eight switches on the left and four on the right [41].

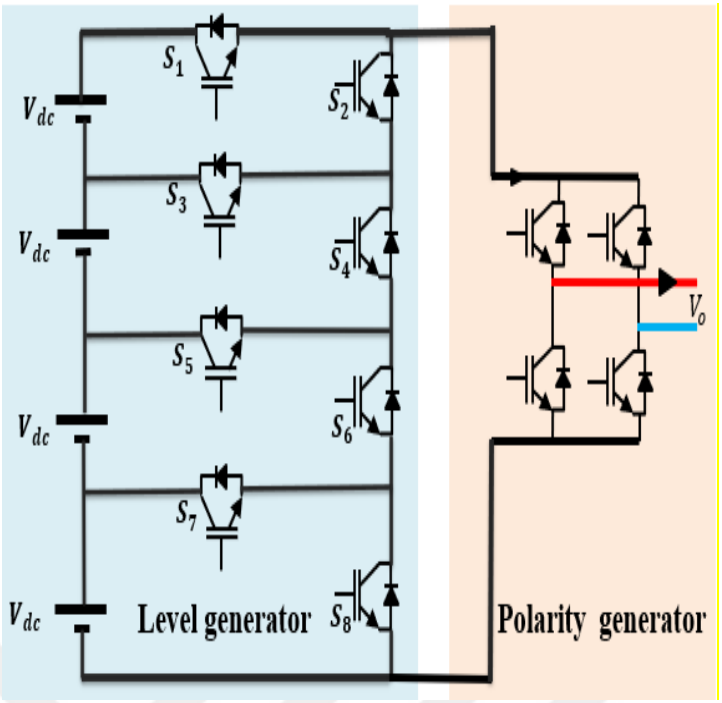


Figure 4.14 Nine level twelve switch hybrid inverter

Hence the solar panel sources will replace the DC sources. The polarity generator is on the right side of the figure, it occupies its position which includes a conventional H bridge unit. The level generator output will be the polarity generator input. Not only this, the isolation component between the polarity and level part is no more in use. Table 4.1 reveals the switching status for the positive cycle of the level generator.

Table 4.1 Switching status for the positive cycle of the level generator

Switching status								Output voltage	Number of sources
S1	S2	S3	S4	S5	S6	S7	S8		
OFF	ON	OFF	ON	OFF	ON	OFF	ON	0 VDC	-
OFF	ON	OFF	ON	OFF	ON	ON	OFF	1VDC	1
OFF	ON	OFF	ON	ON	OFF	OFF	OFF	2VDC	2
OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	3VDC	3
ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	4VDC	4

The modulation technique which is used to generate nine-level output is based on sinusoidal pulse with modulation method (SPWM).

The reference signals of this technique provide the same amplitude and frequency to line frequency. The value of the offset of the magnitude of the reference signal is equal. To produce the required pulses for the inverter switches, these references signal will be compared with the carrier signal. The modulation index for the inverter can be defined as the ratio of the amplitude of the reference signal to the amplitude of the carrier signal. Figure 4.15 displays both the reference signal as well as the carrier signal.

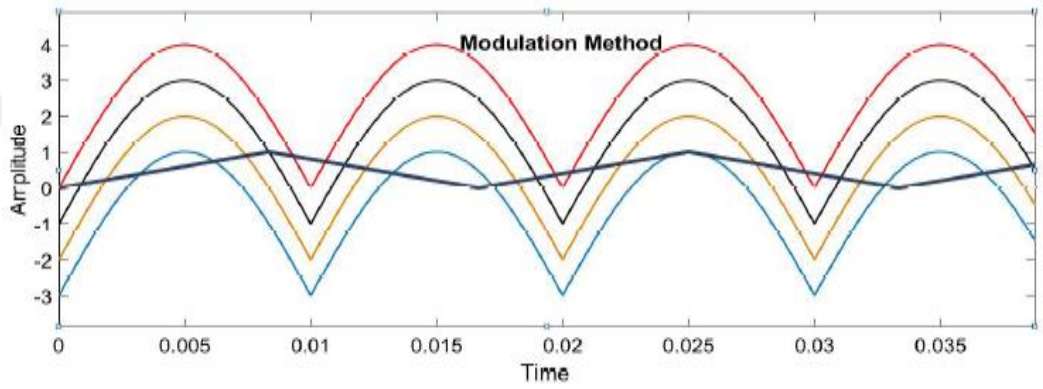


Figure 4.15 Hybrid inverter modulation method

As a whole, solar cells are made up of silicon cells. Solar cells generate potential from solar energy through photovoltaic modules. The output of these cells is commonly low and that's why a photovoltaic array is formed to rise the potential output. Solar cells of the array are connected either in series or in parallel so that voltage or current generated by the module will increase. The position of the array is determined to supply a maximum output power at a specific point. This is so-called the maximum power point. Because of external effect, the photovoltaic module does not operate at the maximum. Thus, one tracking algorithm of the maximum power point must be utilized. MPPT should be used with the DC-DC converter to maintain the panel work near the maximum point. The constant voltage MPPT algorithm, the perturbation and observation (P & O) MPPT algorithm, and the incremental conductance (INC) MPPT algorithm are all considered as types of these techniques [34]. This simulation work utilizes the components below:

1-buck-boost DC-DC converter

2-perturb and observe algorithm

4.2.2.1 Hybrid Multilevel Inverter Simulation Results

Simulation outputs indicate the operation of the implemented inverter with the PV module which is responsible for a continuous battery charge. The PV type is BPSX150, this panel generates its maximum power at VMPP = 34.5v and Imax = 4.35 A. According to the symmetric distribution of the voltages related to this inverter, all PV panels must provide the same voltages 54 volts. As a result, the DC-DC converter will work in boost mode (D> 0.5) [32]. Figure 4.16 displays the PV module duty cycle.

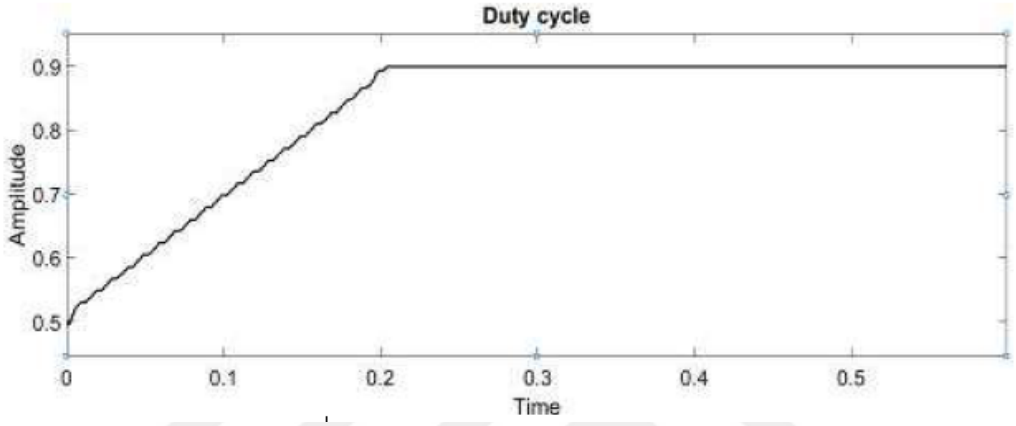


Figure 4.16 Buck-boost converter duty cycle

Table 4.2 mentions the characteristic of the PV module.

Table 4.2 Characteristic of the PV module

Characteristics	The value
Maximum Power (Pmax)	150W
Voltage at Pmax (Vmp)	34.5V
Current at Pmax (Imp)	4.35A
Warranted minimum Pmax	140W
Short Circuit Current (Isc)	4.75A
Open Circuit Voltage (Voc)	43.5V

Figure 4.17 shows the battery voltage while it is charged through the photovoltaic panel.

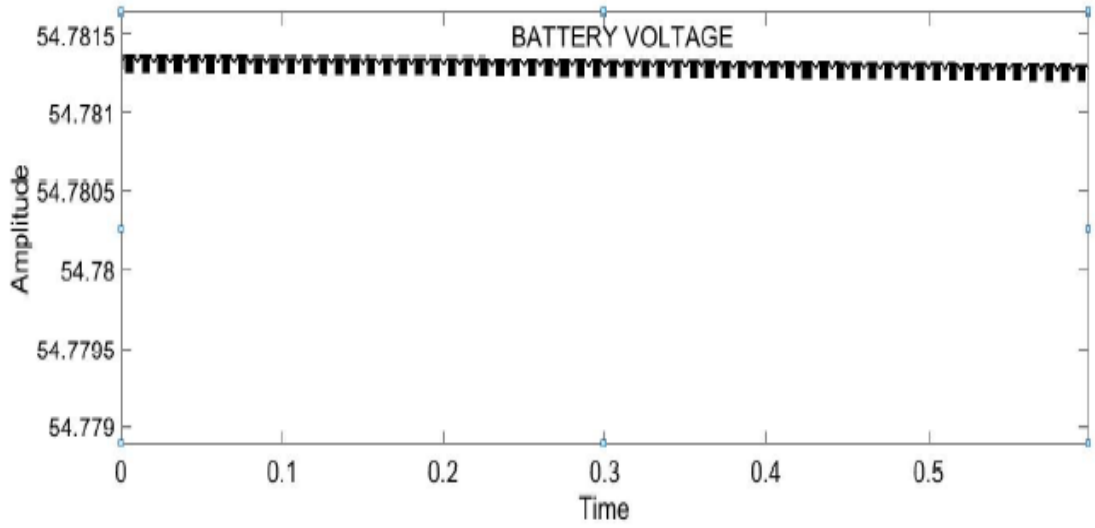


Figure 4.17 Battery output voltage

In figure (4.18) the final output waveform (nine levels) is displayed.

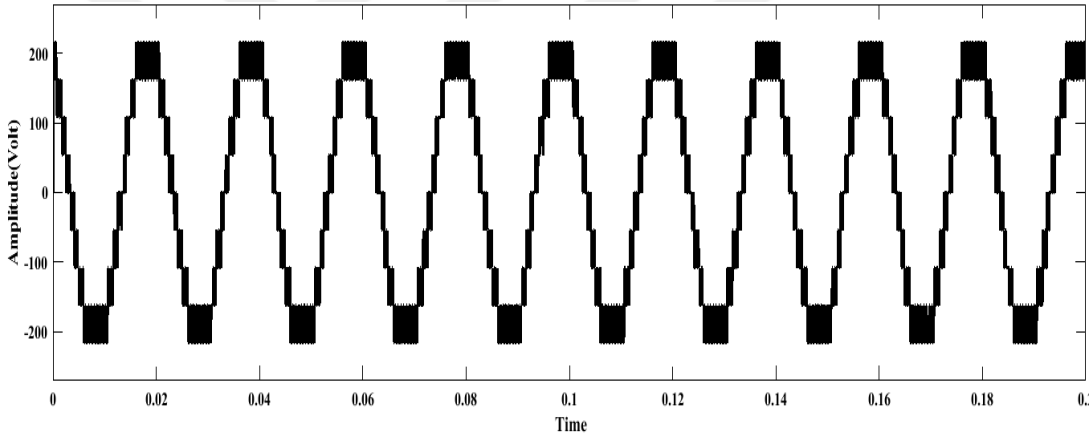


Figure 4.18 Nine level output voltage of the hybrid inverter

Figure 4.19 shows the current of the inverter when it connected to RL load with a resistance of 10 ohm and 20mH inductance..

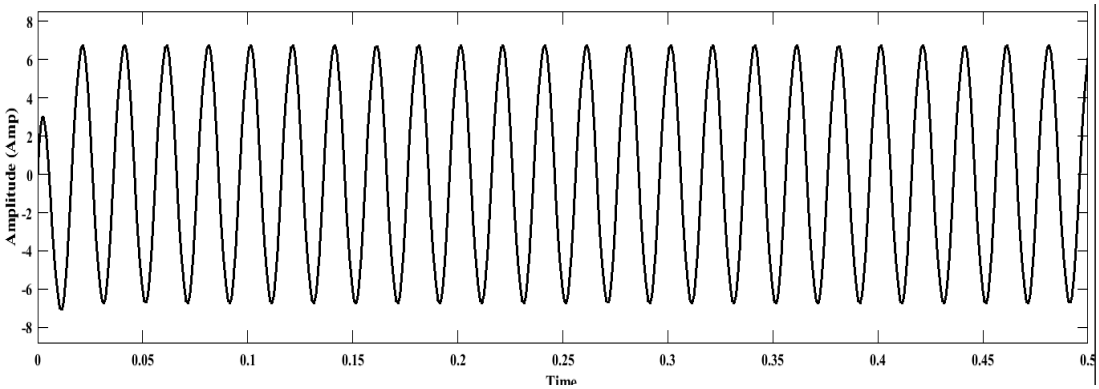


Figure 4.19 Output current for the hybrid inverter

Figures 4.20 and 4.21 show the analysis of the total harmonic distortion(THD) related to the current and voltage signals of the hybrid inverter respectively when it is connected to RL load with a resistance of 10 ohm and 20mH inductance.

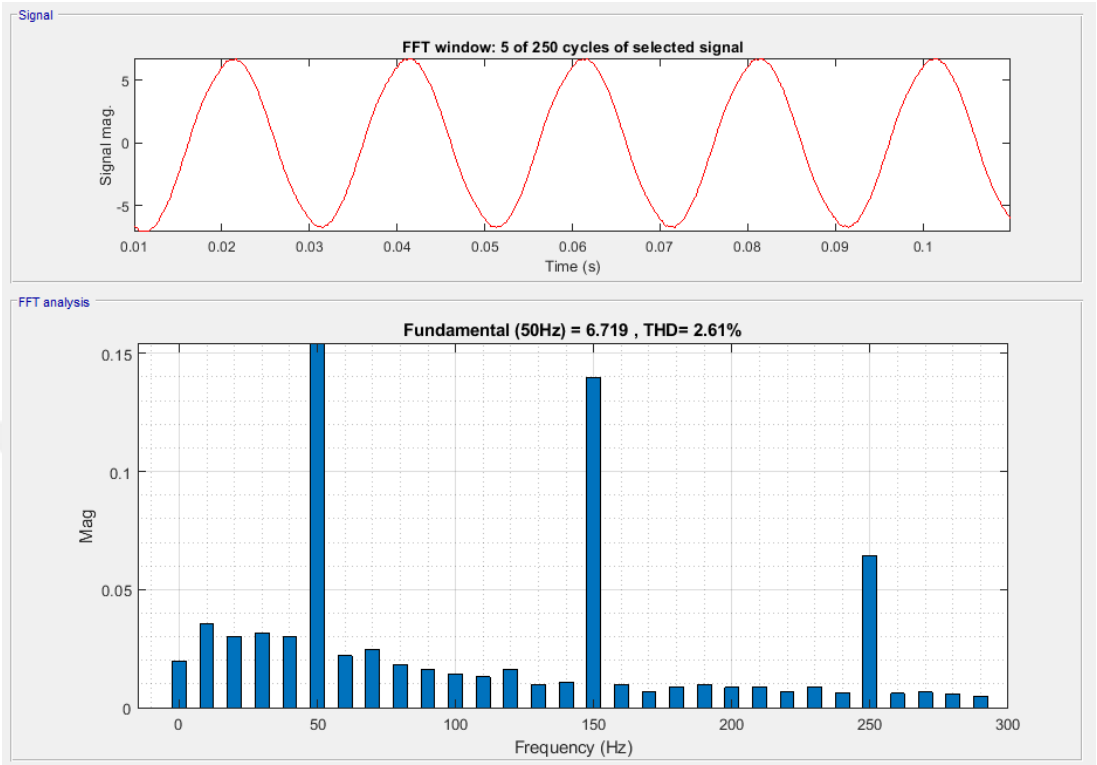


Figure 4.20 Hybrid inverter current total harmonic distortion signal

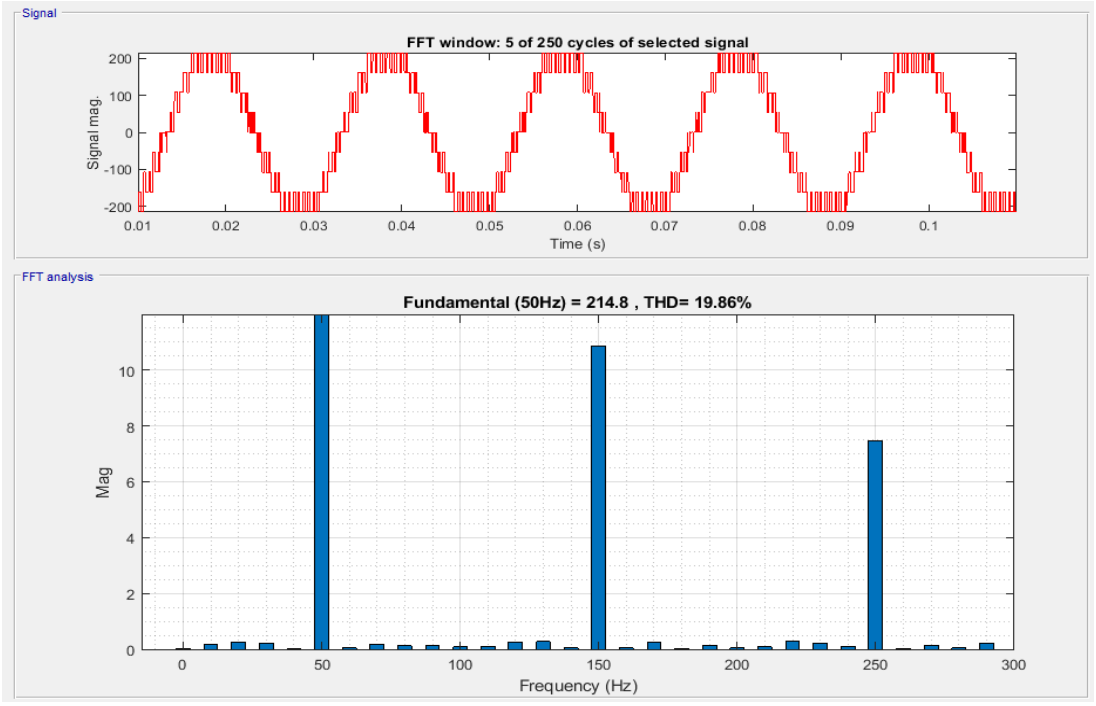


Figure 4.21 Hybrid inverter voltage total harmonic distortion signal

4.3 Cascaded Three Phase Inverter With Low Voltage Ride Through

A potential solution for medium and large-scale solar power plants connected to a grid is the multilevel cascade H-bridge (CHB) inverter. Nevertheless, it has not been thoroughly studied how it operates during voltage sags. An easy strategy for controlling the operation of solar grid-connected CHB inverters in periods of unstable voltage sags is presented here. The main contribution of this study is the fact that the proposed strategy is capable of infusing reactive powers which represents the so-called low-voltage ride-through capability (LVRT), and active power into the grid as well as maintaining voltage balance of all DC-link capacitors. To obtain gate signals, the phase-shifted sinusoidal pulse width modulation (PWM) technique is applied. Under various unbalanced voltage sags, the performance of the proposed strategy for the operation of a grid-connected CHB converter was illustrated and validated through a computer simulation platform[48]. Figure 4.22 shows the three-phase cascaded H-bridge five-level inverter which is connected to the grid through the filtering inductor.

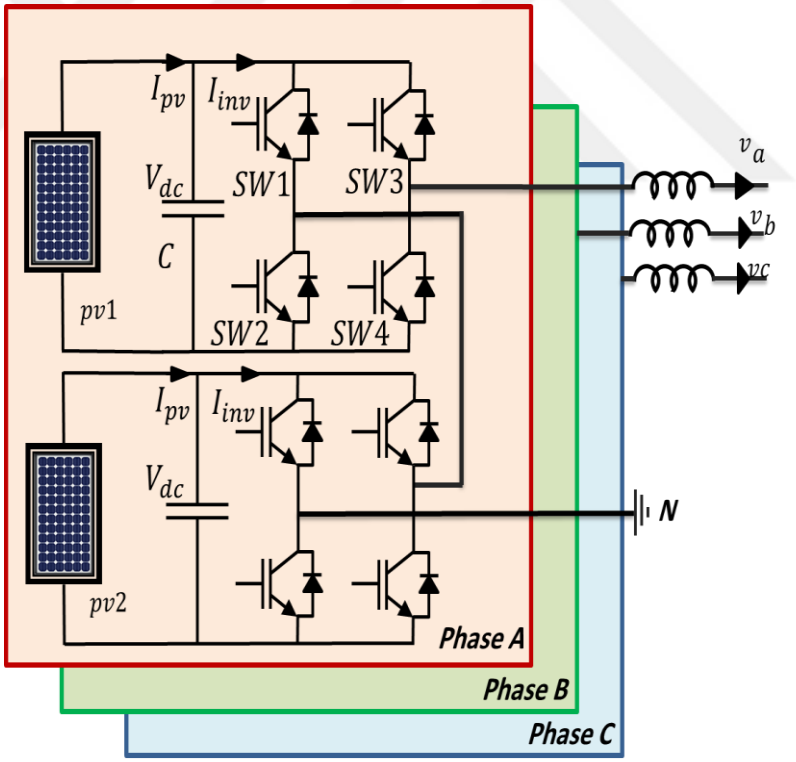


Figure 4.22 Cascaded H-bridge five-level inverter

Due to partial shading or unbalanced load, each phase of the CHB inverter may generate a different amount of power and experience the phase imbalance issue [49]. These imbalances can lead to:

- drop in the voltage quality.
- deviation from one of the DC-link voltage values, which may lead to the activation of the over-voltage protection relay or the loss of MPPT in the case of the single-stage power conversion system.

Considering the data in the literature that asymmetric voltage dips occur more frequently than symmetric voltage dips and concerning the foregoing discussion, this study proffers a flexible strategy for controlling the operation of the grid-connected PV CHB inverter during voltage drops[50]. The developed strategy can balance DC-link voltages as well as the voltage at the point of common coupling (PCC) by deploying LVRT capability during the disturbances of the load[51].

Simulations involving the grid-connected five-level-CHB inverter have been used to evaluate and validate the capability and performance of the proposed control strategy on the operation of the grid-connected CHB inverter during voltage drops. Balanced voltage drops are less common than unbalanced voltage drops, and it is also easier to manage the operation of the PV CHB inverter under balanced voltage drops[52]. Hence, while all the case studies being examined in this work, focus on voltage drops while the proffered control mechanism can also be applied during stable voltage sags or normal grid operation. Although it is not the primary objective of this study, MPPT can be used consistently for those operations. The developed simulations were tested under severe and light unbalanced conditions and the results of the case studies show that this system can handle a voltage sag.

4.3.1. Controlling Technique For PV CHB Inverters Connected To The Grid

Figure 4.22 illustrates the grid-connected PV system configuration with the five-level CHB inverter. A PV power plant equipped with a grid-connected CHB inverter is comprehensively described in [53]. This section focuses on the N-level CHB in an attempt to generalize the proposed technique. The following sections present the structure of the proposed control technique.

4.3.2 Synchronous Reference Frame-Based Theory (SRF)

According to this method, symmetrical three-phase voltages or currents are transformed into direct, quadrature, and zero-sequence components by using the power invariant transformation in a synchronously rotating frame and by the agency of

transformation matrix T given in (4.6), which also known as Park Transformation Matrix. The rotating frame is used to synchronize the phase angle of the AC utility voltage with the support of a phase-locked loop. The direct and quadrature components are symbolized by active and reactive components of the system. Although the main aim is to obtain DC quantities in a rotating frame, higher-order harmonics will remain if there are harmonics in the phase voltage or current. This transformation is first determined by using the transformation matrix C (Clark transformation) given in (4.7) to find alpha, beta, and zero components, and then by synchronizing the phase angle $\boldsymbol{\theta}$ of the AC utility voltage, DQ, and zero components are calculated[54].

$$T = \begin{bmatrix} cos(\Theta) & sin(\Theta) & 0 \\ -sin(\Theta) & cos(\Theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{4.6}$$

$$C = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{\sqrt{2}} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{4.7}$$

The reference currents are calculated as shown in Figure 4.23.

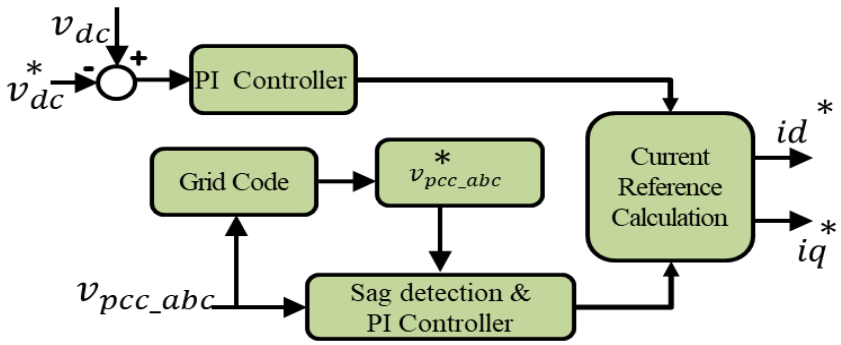


Figure 4.23 Current reference calculation

Figure 4.24 shows the transformation from the ABC frame to DQ coordinates.

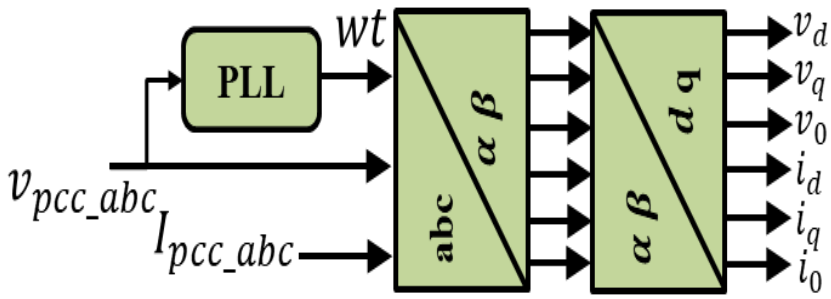


Figure 4.24 Converting the measured current and voltage to dq frame

Here, $v_{0\,is}$ the voltage zero component of the two-axis system in the stationary reference frame, v_α the x-axis voltage in the stationary reference frame, and v_β the y-axis voltage in the stationary reference frame.

4.3.3 Pulse Width Modulation Generation

To calculate the *d*-axis current reference (i^*_d), the error between bridge DC voltage reference v^*_d and vdc^- is fed into a *PI* controller, as shown in Figure 4.23. A sag detection based on an orthogonal system is applied in this study for the calculation of the amplitude of phase voltages and determination of the minimum phase voltage amplitude. The current reference of the q-axis (i^*_q) is determined from the grid codes based on the voltage sag amplitude.

Basing on the grid codes, the reactive current reference is determined by including the grid voltages at the PCC $v_{pcc-abc}$ in the calculation algorithm of the current reference, while the active current reference is calculated by measuring the DC-link voltage. The output of the current reference calculation block is the active power reference current i^*_d and the reactive power reference current $i^*_{q,}$ which are used for LVRT capability[55]. The current regulator and the reference signal generator are shown in Figure 4.25.

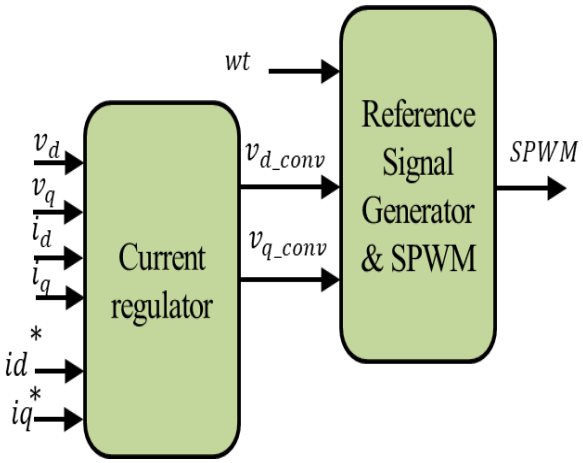


Figure 4.25 Current regulator and SPWM.

The voltage at PCC $v_{pcc-abc}$ and the current at PCC $I_{pcc-abc}$ are measured and converted to the stationary reference frame ($\alpha\beta$ frame). After that, Park transformation is used to generate the rotational reference dq frame v_d, v_q, i_d and i_q. From the active power reference current, $^{i*}{}_d$, reactive power reference current $^{i*}{}_q$, v_d, v_q, i_d and i_q the required SPWM is generated.

Controlling of id leads to regulate the active power. By controlling the active power injected from the CHB inverter, the average DC-link voltage is maintained. The equation (4.8) is used for calculating the average DC-link voltage.

$$\bar{v}_{\mathrm{dc}} = \frac{\sum_{x=a}^{c} \sum_{j=1}^{N} vdc_{xj}}{N*3} \tag{4.8}$$

Where x in the first summation represents the phase arrangements (a,b, and c) while the term j denotes the individual capacitor voltage in such x phase. Several frame transformations are usually required for implementing the conventional PI controller for injecting balance currents, which often reduces the dynamic performance in contrast with controllers that apply the ABC framework. Nevertheless, the conventional PI controller is still simpler to implement compared with other types of controllers. The sinusoidal structure of the output voltage reference is preserved by the controlling loops. Moreover, the computational complexity increases due to the need to calculate both negative and positive-sequence voltages in the *DQ* frame to obtain the precise current injection under voltage sags[49].

4.3.4 Feedback Voltage Compensation Impacts

To improve the operation of the controller, voltage sags need to be quickly detected [51]. At the start of voltage sags, there is a high transient current due to the algorithm's delay in detecting voltage sags. This is because the grid keeps receiving maximum power from the controller in the period from the occurrence of the voltage sag until it is detected. As a result, reducing the transient current during such periods requires the implementation of a feedback voltage compensator. In the absence of this feedback compensator, it is necessary to stress that the current controller, which is unable to immediately react to the voltage sag, is completely responsible for regulating the voltage references[50]. Figure 4.26 shows the diagram of the system connected to the grid.

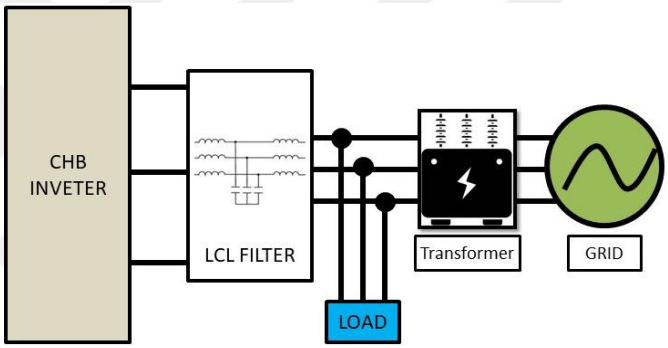


Figure 4.26 Overall grid model

During a voltage sag, utility voltage must remain stable because the five-level CHB inverter must inject an amount of reactive power into the grid to increase the voltage level at the PCC. It means that the power factor correction and voltage regulation cannot be achieved together. For this reason, the three-phase five-level CHB inverter will work in the voltage regulation mode. The first stage of this regulation as a very important procedure is the detection of the voltage sag. A voltage sag has to be detected and references current produced to prevent a voltage sag.

4.3.5 Strategy For Inter-Phase And Inter-Bridge Stability

The addition of the voltage references ($v^*_{a-1,}$ v^*_{b-1}, and v^*_{c-1}) to a zero-sequence voltage (v_{zero}) is used as an inter-phase balancing technique. To get high-quality output voltages, all the DC-link voltages of the various phases must be equal. If the power of

the bridges of each phase is different, it means that their voltages are different since their currents are equal. To calculate the voltage reference associated with each bridge, the desired deviation of the voltage reference of each bridge for inter-bridge balancing (Δv_{xj}) is added to the value obtained when the voltage reference of the phase (v^*_{x-2}) is divided by N [55]. Figure 4.27 shows the implementation of the interphase and inter-bridge voltage balancing algorithm.

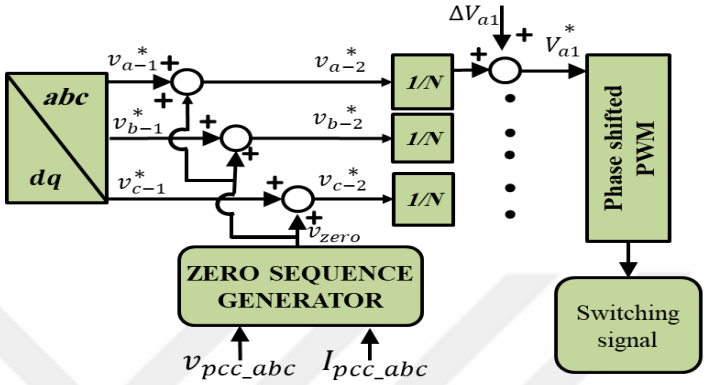


Figure 4.27 Interphase and inter-bridge voltage regulation

4.3.6 Simulation Setup And Result

A model was developed by using a computer simulation platform. The circuit includes a five-level inverter, a controller, a local load, a transformer, and a grid as illustrated in Figure 4.26. Figure 4.28 shows the inverter line to ground and line to line voltages.

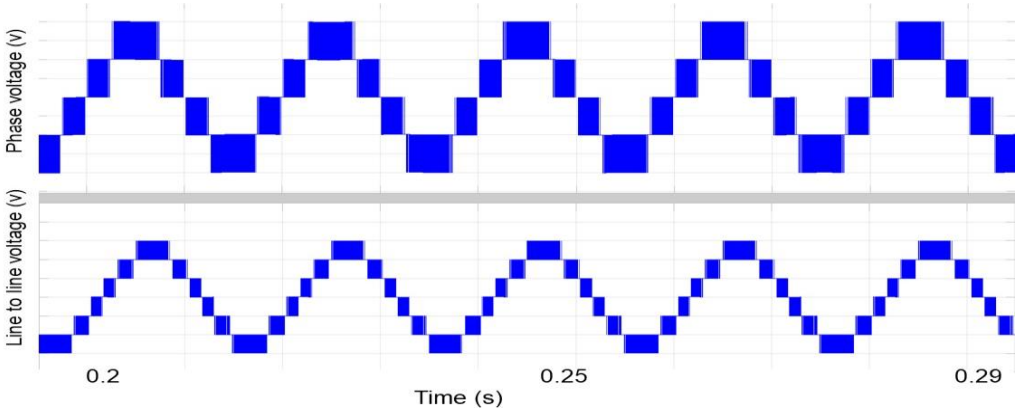


Figure 4.28 Inverter's line-to-ground output voltage and line-to-line voltages

In the simulated cases below, the inverter controller fixed the DC $V_{ref.}$ To Achieve the robust LVRT strategy, the reactive power dispatched to PCC from the inverter has to be calculated carefully. The equation (4.9) used to calculate the desired amount of reactive power to regulate the voltage is shown below[56].

$$Q = V_{alcl} \frac{V_{alcl} - V_{blcl}}{\Delta x} \quad (4.9)$$

where Q is the possible injected reactive power during a voltage sag, V_{alcl} RMS line-to-neutral voltage after using the *LCL* filter, V_{blcl} RMS line-to-neutral voltage before using the *LCL* filter, and X_{Δ} the reactance between V_{blcl} and $V_{alcl.}$ According to Eq. (4.9), if V_{blcl} is equal to V_{alcl}, reactive power generation is zero. To get the desired V_{blcl} at the terminals of the inverter, the DC voltage V_{DC} was calculated based on Eq. (4.10)

$$v_{\mathrm{dc}} = \sqrt{2} \frac{V_{blcl}}{\sqrt{3}} \quad (4.10)$$

Figure 4.29 shown below depicts the measured and reference voltages of the simulated system.

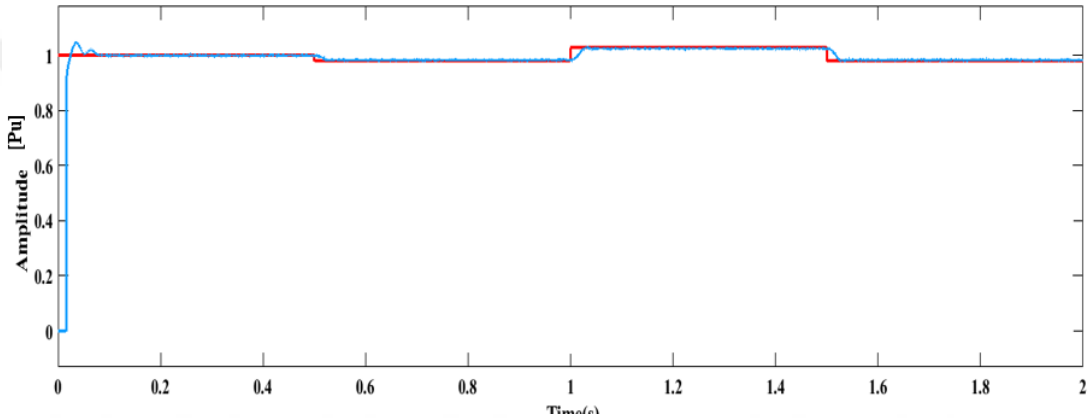


Figure 4.29 voltage sags condition

Figure 4.30 shows the single-phase capacitors' voltages.

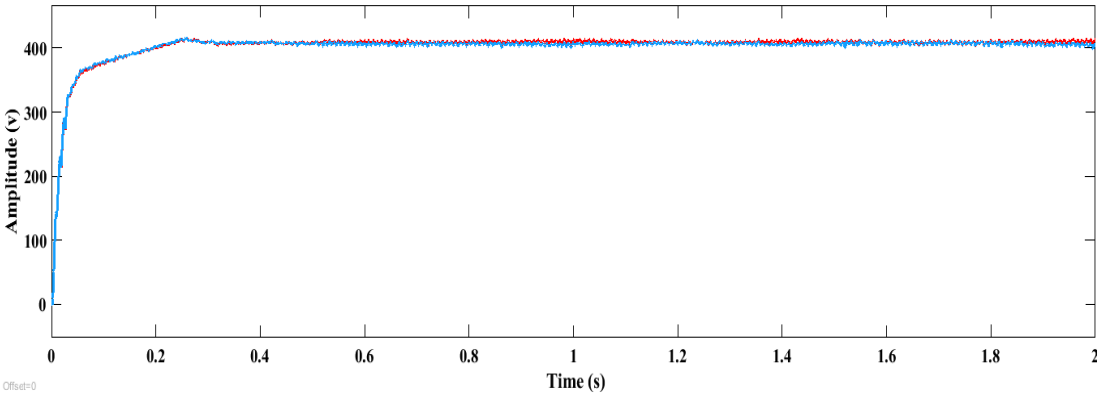


Figure 4.30 Single-phase capacitors' voltages

Figure 4.31 shows the three-phase average voltages.

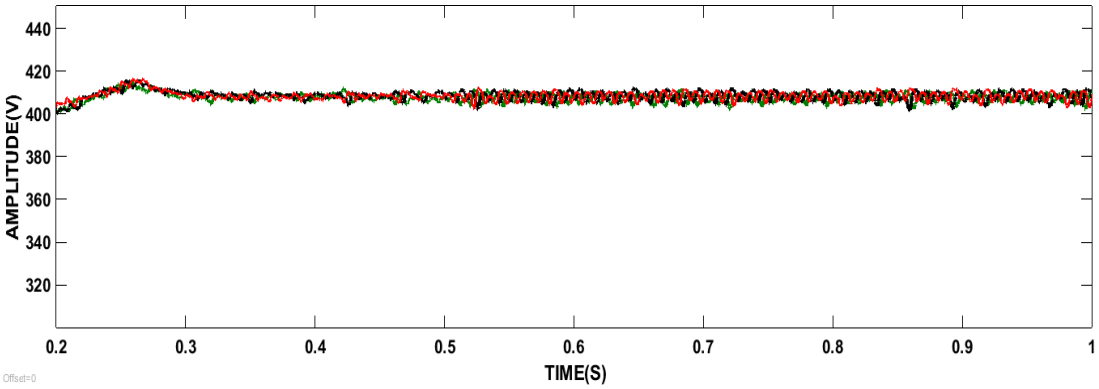


Figure 4.31 Three-phase capacitors average voltages

Figure 4.32 shows the measured direct current and the reference direct current of the system.

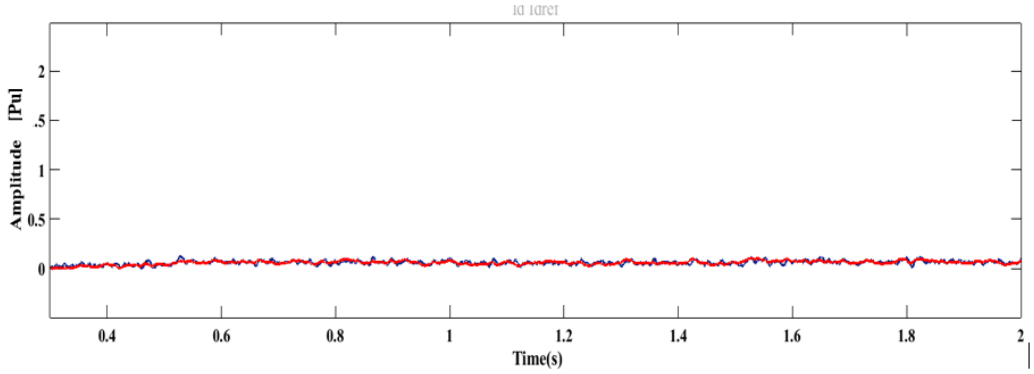


Figure 4.32 Measured (black)and the reference(red) direct currents

Figure 4.33 shows the measured and the reference quadrature current component of the system.

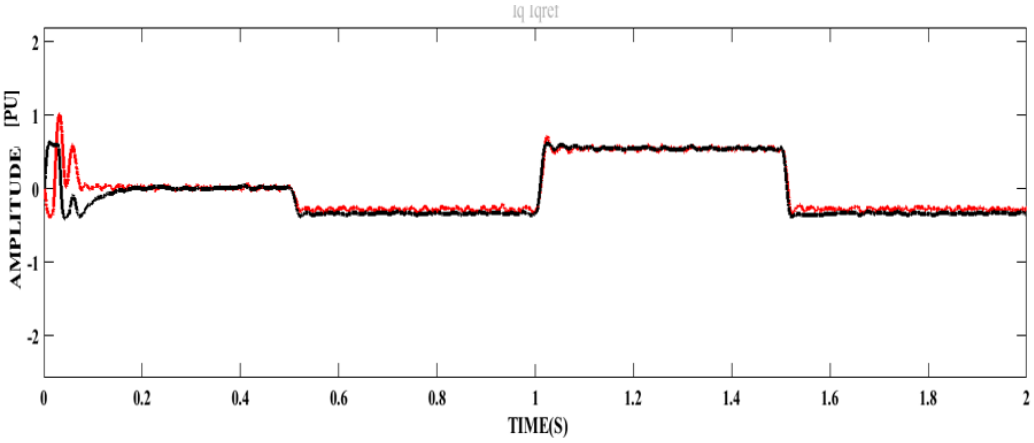


Figure 4.33 Measured(black) and the reference quadrature(red) current

Figure 4.34 shows the active and reactive power transferred between the grid and the inverter.

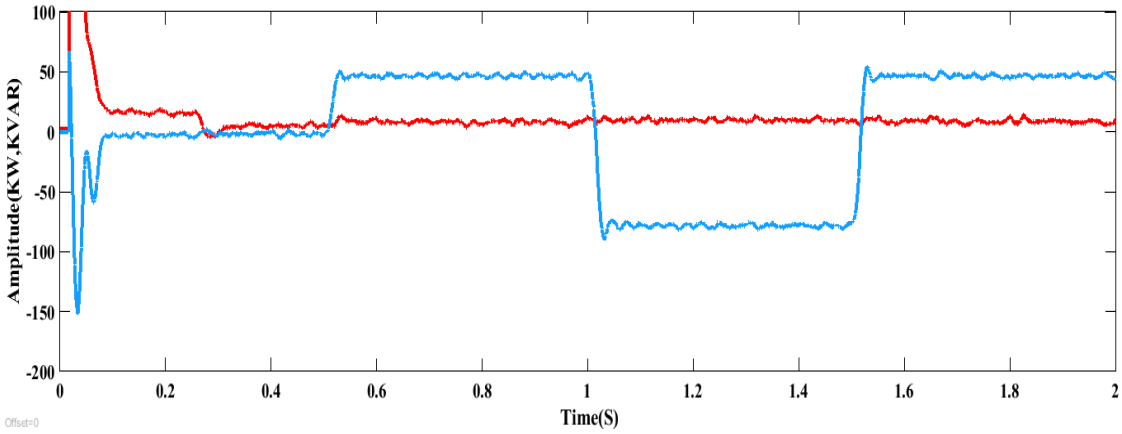


Figure 4.34 Active(red) and reactive power(blue)

4.4 Control Parameter Optimization To STATCOM Based On Hybrid Inverter

This simulation work aims to improve the classical Static Synchronous Compensator (STATCOM) unit by utilizing hybrid multilevel inverter instead of conventional inverters type which reduces the number of semiconductor switches used in inverter design. The dynamic performance of the STATCOM unit is investigated by finding the optimal gains for PI controller using PSO and GA optimization methods. Simulation results from each optimization technique are studied and verified by realizing the effect of finding the optimal gains for the STATCOM PI-controllers. Furthermore, the comparison is conducted to find the best-utilized optimization methods.

As the complexity of medium and high transmission lines increase, the size and number of loads are continuing to be enlarged due to additional new tunnels, roads, and buildings. As a result, it becomes much difficult to control the grid voltages in the demand-sides from the side of the generator only. The typical contemporary technology used for regulating the voltages level on the power system grids is called static synchronous compensator (STATCOM). The STATCOM usually works as a voltage controller and power quality improvement when setup near to loads. The performance of the STATCOM controller depends on the reference value of reactive power or standard gird voltages [56]. The controller must be rapidly tracking such a one reference signal or multiple reference signals to achieve efficient STATCOM operation and more stability in the output of VSI. The conventional structure of STATCOM includes a voltage source inverter (VSI) that is comprised of the three-level inverter. In the DC side of the inverter, selecting an optimum value for the DC-

link voltage is a crucial matter. At the same time, the small voltage is favorite for its achieving lower switching losses and eliminating the injected current harmonics from STACOM to the grid [57,58]. In many previous works, the proportional-integral (PI) is widely used as automatic controllers for STATCOM. The PI controller is forced to linearize the system operation points which makes the error between the desired signal and the measured signal approach to zero. Furthermore, the simplicity of PI control makes it the most attractive control method. On the other hand, the PI controller can give an acceptable performance with load varying conditions. The weak aspect in the performance of the PI controller is the change in the eigenvalues positions when the system experiences load changing[59,60]. Similarly,because of having easy construction and fine-tuning of PI controller, it becomes a traditional controller for STATCOM based on the multilevel inverter. The tuning of PI controller gains for the loop controller is a critical aspect, especially for a non-linear system that includes many variables. The approach based on trial and error is considered in many studies as an optimal approach to tune the PI controller. However, it is not clear from the drawbacks such as time-consuming and suffering from a change in system operating conditions [61,62]. On the other hand, many control schemes were used as a controller unit for STATCOM, in [63] the linear quadric regular (LQR) controller for the current source converter CSC-STATCOM was discussed although they utilized genetic optimization in determining the controller gain values, the best gain values of the controller were obtained using trial and error method. The simulation of cascaded H-bridge multilevel converter based on STATCOM has been discussed with the model predictive controller (MPC), and further details are given in [64]. The STATCOM based on H-bridge multilevel converter with fast MPC was presented in [65].In other words, the genetic optimization method has been used to find LQR controller coefficients. This method has been utilized to find coefficients for LQR controller, the Q and R coefficients are determined for STATCOM based on the LQR controller. Not only this, there are numerous optimization methods to find the optimum gains for PI-controller, such as PSO and GA etc. The PSO and GA algorithms are used for classification of power quality disturbance and detection the location of disturbance source based on different signals features, the extracted features were clustered by fuzzy C-means algorithm [66]. The PSO algorithm was used for the tuning PI-controller gains; the results were considered under different loading conditions which increase the natural dynamic of the PI controller [67]. In addition to that PSO did not

need prior training as the same as artificial neural network (ANN) and this meant the minimum convergence time which leads to system velocity increasing.

There are other views which state that optimization methods operating under the objective function criteria that have to be defined precisely focus on the optimal available solution. It is worth mounting the performance of STATCOM unit associated trustily with converter topology which is used like a voltage source converter (VSC) fed by a capacitor in DC-link. In recent studies various converter structures based on STATCOM have been addressed, the first generation of STATCOM utilizes a conventional three-phase six switches inverter which is rejoiced as a simple structure and easy control unit implementation. At the same time, the output voltage quality suffered from high harmonic content which affects the injected current at PCC. Massive attention has been paid to improve the power quality at PCC through modified inverters topologies [68]. The modern topologies for inverters are known as a multilevel inverter, that topologies play a critical role in harmonics mitigation and provide superior harmonic profile at their output. Different topologies for multilevel inverters were presented and classified under hybrid structures [69,70]. The increase in the number of diodes and capacitor makes the process control further complicated and increase the size of the inverter circuit which leads to the limited application of these types of inverters. In cascade multicell inverters structure, phase voltage is gained by adding the voltages of each sub converter model in the same phase inside the sub converter units. A specific leg converter is joined with others to generate the objective voltage. The design of these inverters expresses more functionality and simplicity than other structures such as diode and capacitor-clamped inverter circuits. Generally, N-level multilevel cells are put next to each other. In this structure, every level of voltage is controlled and balanced by itself independently to load features which means that, this topology ensures a multilevel inverter frame that can balance the DC voltage by technical control method utilization. In hybrid combined-level multilevel inverter cells, the multilevel circuits of diode-clamped inverter and capacitor-clamped inverter occupy the position of the full-bridge cell in the cascaded multicell inverter design. In this way, the number of sources is diminished. This type of inverter expresses benefit-able characteristics when it is used in high power and high-voltage utilities. However, diode-clamped and capacitor-clamped inverters increase the sophisticates of inverter control algorithms. In an asymmetric hybrid multilevel inverter structure, the amplitude of the DC voltage in one cell is different

from the other according to DC levels distribution manner, each inverter suffers different stress, which increases the cost and control complexity[71]. These methods generate more levels with the same number of switches concerning symmetric schemes inverters. According to the previous review related to the hybrid multilevel inverter, it could be observed that the hybrid combined level suffers from control complexity and most of the presented inverters are designated for high voltage applications due to feeding by multiple sources. In this work, STATCOM based on novel hybrid nine-level inverter topology is implemented and different optimization methods are used to determine the system controller parameters. The proposed STATCOM structure with a hybrid inverter provides an effective stability operation even with different grid voltage conditions. Furthermore, the tuning methods of PI-controller gains have significant advantages as compared with the conventional tuning method.

According to IEEE standardization, "a static synchronous generator worked as a shunt coupled VAR compensator device with its an independently on capacitive or inductive currents that can dynamically control the AC system voltage", STATCOM can control both the capacitive and the inductive output current separately of the AC system voltage. Basing on the application requirement, STATCOM could be utilized as a voltage or current source converter[72]. The representation block diagram for STATCOM based on a hybrid inverter is depicted in Figure 4.35.

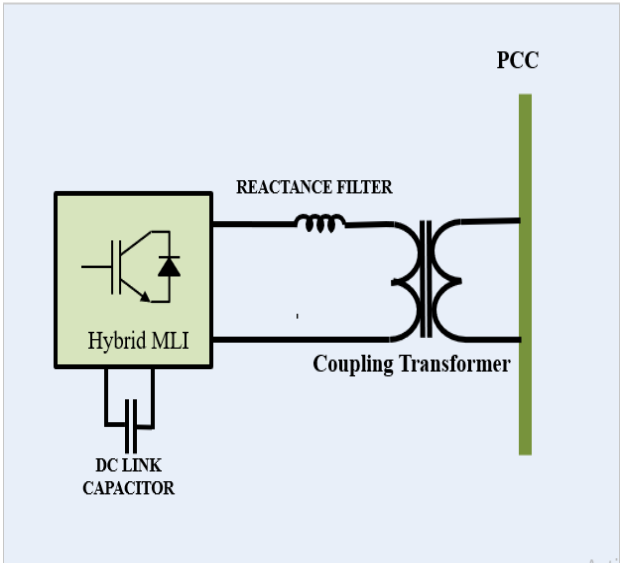


Figure 4.35 Block diagram for STATCOM based hybrid multilevel inverter

STATCOM is formed by a voltage source converter (VSC) which stands for hybrid nine-level inverter, and a coupling reactance usually acts as a filter and a coupling transformer that connects the multilevel inverter side with the point of common coupling (PCC). This connection allows STATCOM to supply the required controllable reactive current into PCC. The other side of the inverter is the DC side, which includes the DC-link capacitors bank or energy source that is responsible for the four-quadrant operation modes of STATCOM. The bidirectional switches in the inverter allow transferring real power into two directions between DC-link and grid. In VSC, the DC-link can be represented by capacitors bank illustrated in Figure 4.36. A harmonic filter is usually used to eliminate harmonics at the AC side (PCC), the harmonics injection in the AC side happens due to the non-linearity characteristics of the semiconductor switches. The control techniques for turn-on and -off semiconductor switches also cooperate in reducing harmonics injection in AC-grid. Many switching control topologies can be utilized to implement VSCs which imperceptibly contribute to eliminate harmonics. The modulation technique typically applies the pulse width modulation (PWM) method to control the status of the semiconductor switches in such a way that the sinusoidal waveform is generated with variable amplitude and phase angle. The generated waveform is compared with the triangular waveform to produce a train of pulses[73]. The detailed scheme for nine-level hybrid inverters for the three-phase system is illustrated in Figure 4.36.

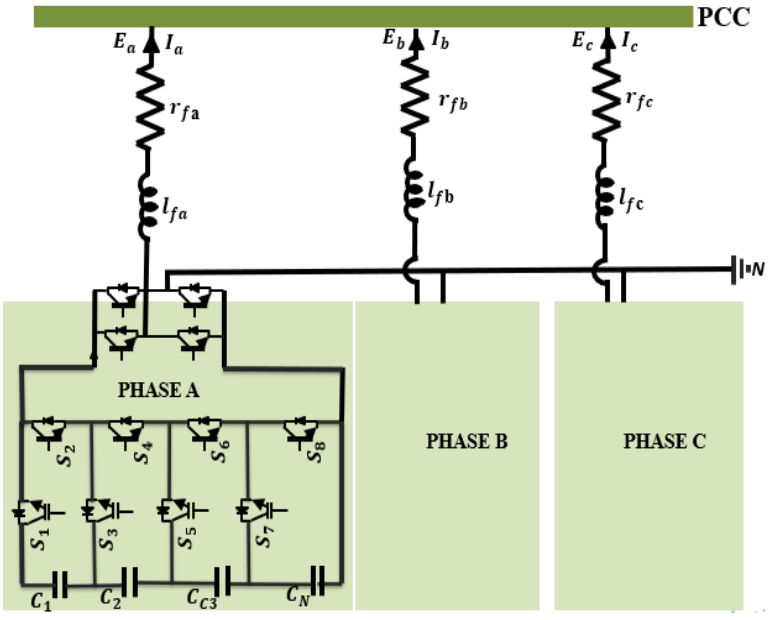


Figure 4.36 Three-phase hybrid multilevel inverter based statcom

$$-n_a v_{DC} + \frac{L\, dI_a}{dt} + I_a r_{fa} + Ea = 0 \tag{4.11}$$

$$-n_b v_{DC} + \frac{L\, dI_b}{dt} + I_b r_{fb} + Eb = 0 \tag{4.12}$$

$$-n_c v_{DC} + \frac{L\, dI_c}{dt} + I_c r_{fc} + Ec = 0 \tag{4.13}$$

Depending on these three Equations I_a, I_b and I_c represent the three-phase current, while the three-phase voltages are E_a, E_b and E_c .The harmonic filter consists of inductance and resistance which are L and r_f respectively, n_x represents the number of capacitors in DC-link. The active power flow for single-phase can be represented by Equation (4.14), while similarly, procedures can be applied for other phases.

$$P_1 = \frac{dW}{dt} = \frac{P_a - \frac{r_f |I_a|^2}{2}}{n} - \frac{{V_{DC}}^2}{r_{DC}} \tag{4.14}$$

In the real power flow equation, the active power flow in each cell of the phase -a is defined P_a. P_1 is the single-phase real power flow to the grid, while W is the energy stored in the DC-link capacitor C, and r_{DC} is auxiliary shunt resistance which represents the overall losses in the DC-link, V_{DC} represents an average DC-voltages that come from the total of the capacitor sources[74,75].

The rotating frame transformations matrix is expressed in Equation (4.15)

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos(\omega t) & cos(\omega t - \frac{2\pi}{3}) & cos(\omega t + \frac{2\pi}{3}) \\ -sin(\omega t) & -sin(\omega t + \frac{2\pi}{3}) & -sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{4.15}$$

By using stationary frame Clark's transformation, the Equations (4.11) can be simplified and expressed as follows:

$$-nm\, v_{DC} + \frac{L\, dI_{dq}}{dt} + I_{dq} r_{fa} + Ea = 0 \tag{4.16}$$

Where m is the modulation index.

4.4.1 Pi-Controller For The Statcom Based On Hybrid Multilevel Inverter

The control system of the STATCOM that is generally integrated from two sub-controllers are usually called an internal control or current controller and outer control. The inner controller adjusts the STATCOM current while the external controller is responsible for capacitor voltage regulation. The outer controller determines the real power P transferor to DC-link capacitors which indicates the charging and discharging process of the capacitor voltage. At the same time, the outer controller is used to

directly control the DC voltage magnitude and sensing the reference current called $I_{d\,ref}$. The amount of reactive power supplied or absorbed into PCC, can be implemented in two different ways based on operation modes for STATCOM[76].

In voltage operation mode, the reference voltage or the required voltage is compared with the measured voltage, and then the error of comparison is applied to the PI controller to produce the generated $I_{q\,ref}$ which is responsible indirectly for regulating the reactive power flow. On the reactive power regulation mode, the target reactive power is compared with the measured reactive power from the grid, and then the difference between these readings passes within a PI controller resulting in $I_{q\,ref}$ generation. In this work, the voltage mode regulator STATCOM is implemented. Thus, the reactive current reference is taken from PI controller output while the difference between the measured and reference voltages lies in the controller inputs. The overall control block of the STATCOM system is illustrated in Figure 4.37.

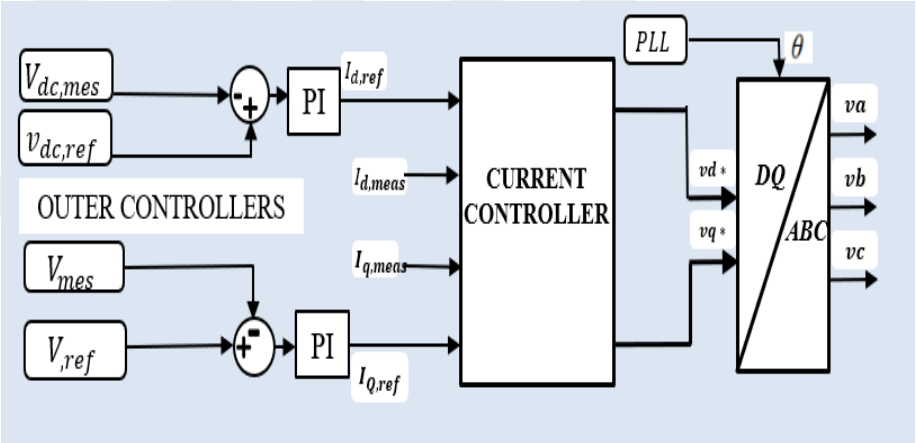


Figure 4.37 The comprehensive control unit of STATCOM

The block diagram of the STATCOM control unit is comprised of Clarke's transformation for DQ component calculations and grid-voltage angle θ . Since the DQ controller will be performed, a constant sample time will be used for current and voltage sampling. This sampling time specifies no less than twice of switching frequency.

The internal controller loop is responsible for the measured difference between the targets currents measured from outer controllers $i_{d\,ref}$ and $i_{q\,ref}$ compared with the measured grid currents id and Iq respectively and after proceeding with the PI controller, the two reference voltages are generated and mentioned as $V_d$and V_q in DQ

rotating bases. The block diagram for the internal control loop is depicted in Figure 4.38.

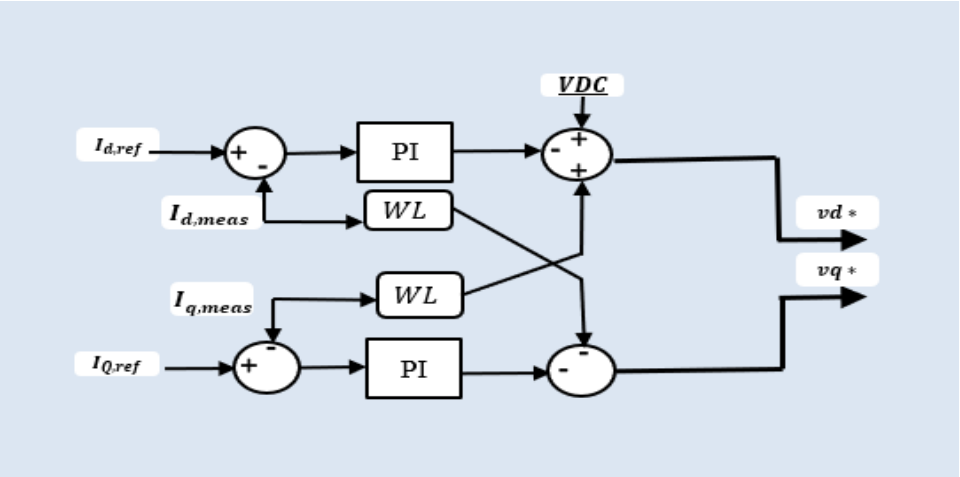


Figure 4.38 The internal controller scheme

To evaluate the current control based on the Laplace domain, Equation 4.16 is modified to Equation 4.17.

$$I_{dq}Lf\ s + r_f I_{dq} + V_{dq} + j\omega Lf I_{dq} = nm\, V_{DC} \tag{4.17}$$

The Equation (4.17) after passing through PI controller unit, the output can be written as:

$$(K_p + \frac{K_i}{s})(i_{dq}{}^* - i_{dq}) + v_{dq} + j\omega Lf\, i_{dq} = nm\, V_{DC} \tag{4.18}$$

The controller gains K_p and K_I involve all constant values, the K_p and K_I represent the proportional and integral gains for PI-controller, respectively. The output current of STATCOM is decomposed into real current i_d and reactive current i_q components[77]. The active power for AC and DC to phase "a" with system loss neglection can be written as follows:

$$P_{DC} = \frac{c\ d\ ({V_{DC1}}^a + {V_{DC2}}^a + {V_{DC3}}^a + {V_{DC4}}^a)}{2ndt} \tag{4.19}$$

The overall three-phase average DC voltages V_{DC} which represents the measured DC voltage for the DC-link capacitor is given as :

$$V_{DC} = \frac{\sum_{x=a}^{c} \sum_{k=1}^{n} v_{DC-xj}}{N*3} \tag{4.20}$$

Where x in the first summation represents the phase arrangements (a,b, and c) while the term j denotes the individual capacitor voltage in such x phase[78].

Kennedy and the electrical engineer Russell Eberhart in 1995, developed an optimization algorithm based on the behavior of the bird flocking in search of their food in a multi-dimensional space which depends on the experience of class members.

The proposed algorithm by Kennedy and Eberhart has been called Particle Swarm Optimization (PSO).

Due to structure simplicity for the PSO and quickly converges, the optimized solution with high efficiency, simple implementation, fewer parameters, and high effectiveness will be obtained. Therefore, it has become widespread in recent years for tuning PID controllers. However, getting the optimal values of proportional and integral constants (Kp, Ki) is still obscure. Figure 4.39 shows the PID-based PSO control.

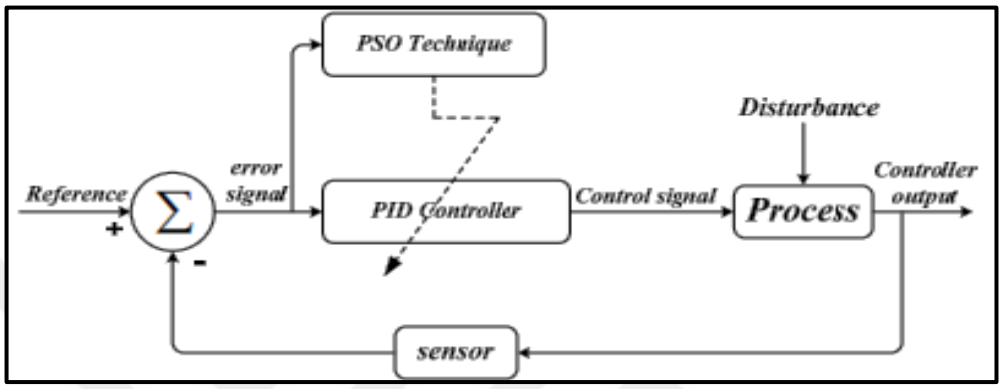


Figure 4.39 Block diagram of the PID controller based PSO method

In PSO each particle in the entire swarm searches to update its local present position and velocity to a new global position and velocity [79]. The procedures of the particle's velocity updated with its new position is shown in Figure 4.40.

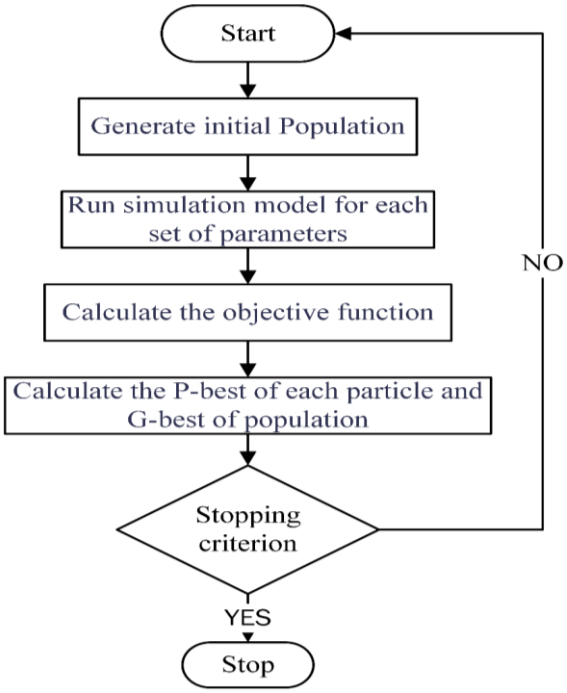


Figure 4.40 Flow chart for the PSO algorithm

The particles are updated their velocity (v) and their new position (w), based on the following equations.

$$V_i^d(t+1) = W(t)V_i^d(t) + C_1 S_{b1} S\left(Pbest_i^d - S_i^d(t)\right) + C_2 S_{b2} S\left(gbest_i^d - S_i^d(t)\right) \quad (4.21)$$

$$W(t) = randX\frac{t}{t_{max}}X(W_{max} - W_{min}) + W_{min} \quad (4.22)$$

Where $V_i^d(t)$ and $V_i^d(t+1)$ represent the current and new particle of i^{th} velocity at t^{th} iteration, and d^{th} demission, respectively. C_1 and C_2 represent adjustable acceleration coefficients. b_1 and b_2 represent random numbers between [0,1]. The general formula for the PSO algorithm can be summarized in Figure. 4.40. The PSO algorithm can be adopted by the following steps:

1) Identify the number of particles and give initial values for speed and position to each particle.
2) Compute the cost function of each particle.
3) For each particle, compare the past calculated cost function with its present best cost function. In the case that the previous is better, replace its current best cost function with the previous, and replace its best position with the current position.
4) For each particle, compare its cost function with the swarm's global best cost function. In the case of earlier is better, replace global best cost function by the earlier, and replace the global best position by the best position of the compared particles.
5) The equations (4.21) and (4.22) are applied for update position and speed for each particle.
6) Return to step 2 and repeat until termination conditions are satisfied.

Unlike PSO, the genetic algorithms are stochastic seeking methods depend on the fundamental concept of natural selection and fittest survival. Moreover, the GA consolidates objective function with a randomized or well-structured swap of information between solutions continues until approaching a global optimum. Three stages describe GA implementation architecture; initial population generation, objective function evaluation, and genetic operations. Figure 4.41 shows the flow chart for the genetic algorithm.

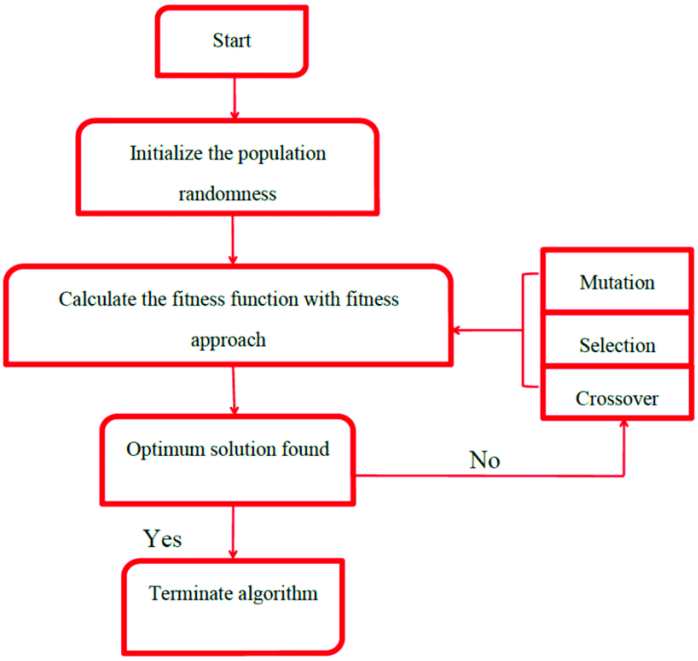


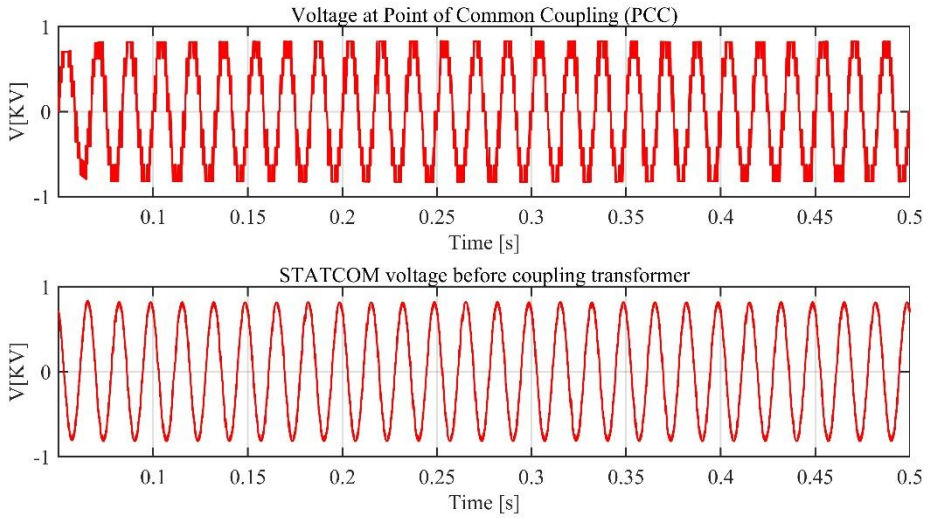
Figure 4.41 Flow chart for the GA algorithm

The GA control variables are initially defined, and an initial population of binary strings of restricted length is arbitrarily created. After addressing the initial population, GA works in cycles namely generations[80,81].

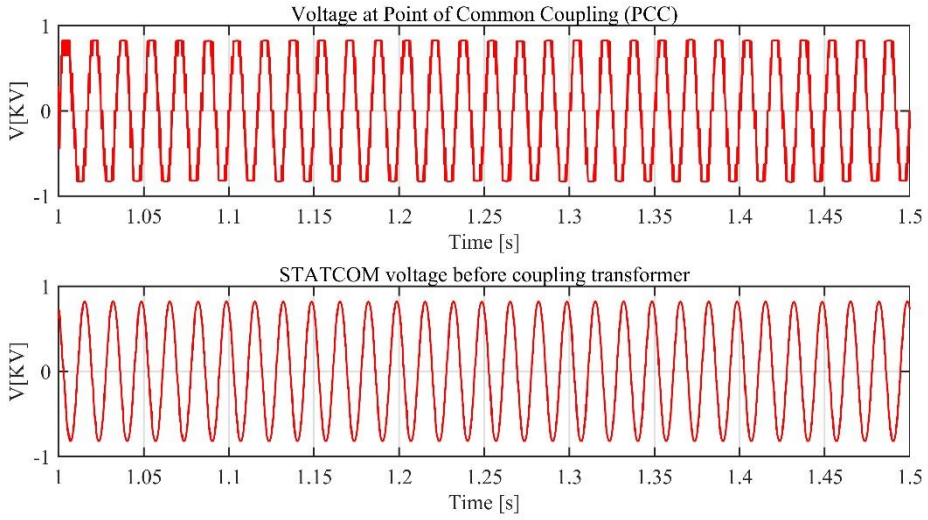
4.4.2 Results Of The Statcom Based Hybrid Inverter

In this section, the proposed STATCOM based on a hybrid nine-level inverter is modeled and discussed. Furthermore, STATCOM performances based on the hybrid inverter with parameters of the PI controller are optimized by PSO and GA, and various unbalanced voltage sag cases are simulated. The specifications of STATCOM with optimization algorithms codes are listed in (Appendix A), (Appendix B) and (Appendix C).

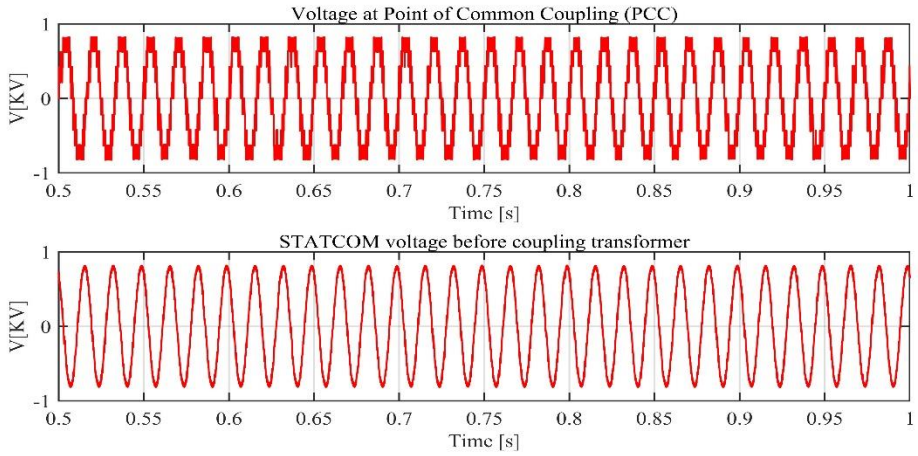
The output phase voltages of STATCOM with controller parameters optimized by PSO are shown in Figure 4.42.



a.STATCOM off-state mode.



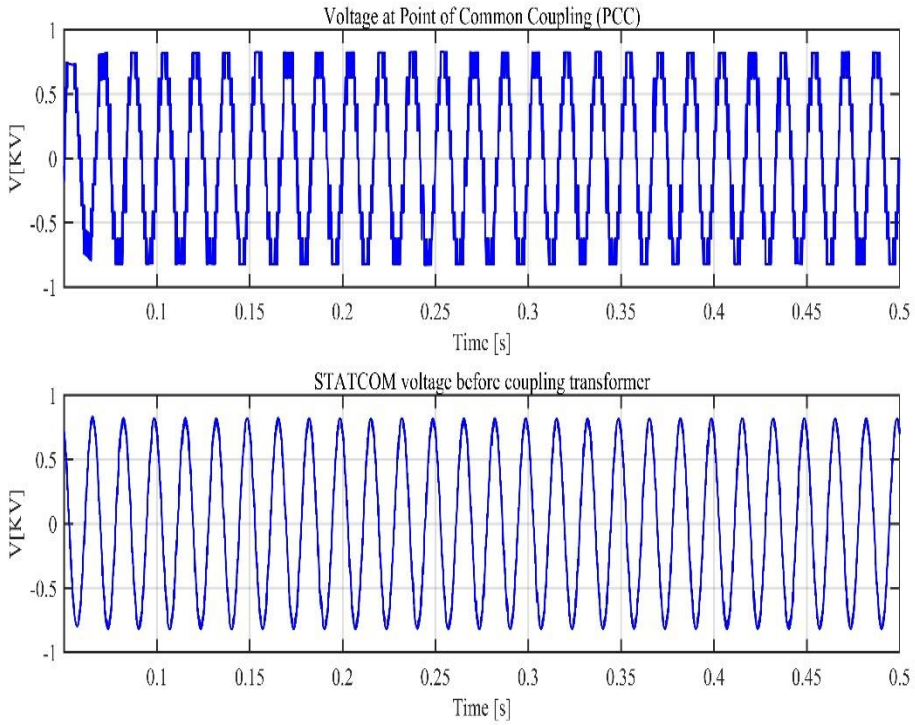
b. STATCOM in inductive – mode.



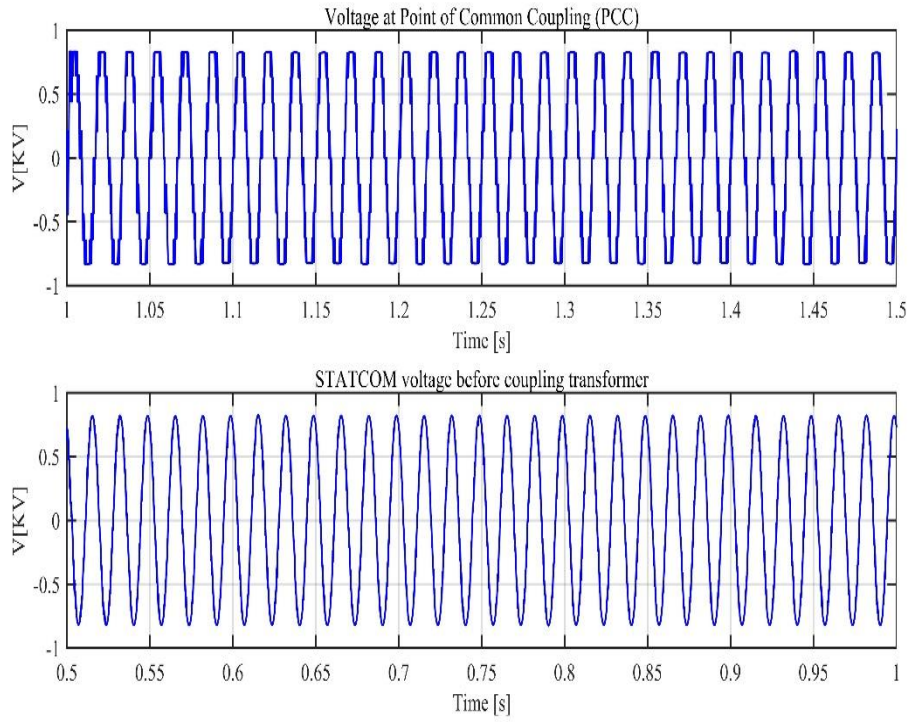
c. STATCOM in capacitive mode – mode.

Figure 4.42 STATCOM output voltages with PI controller based PSO.

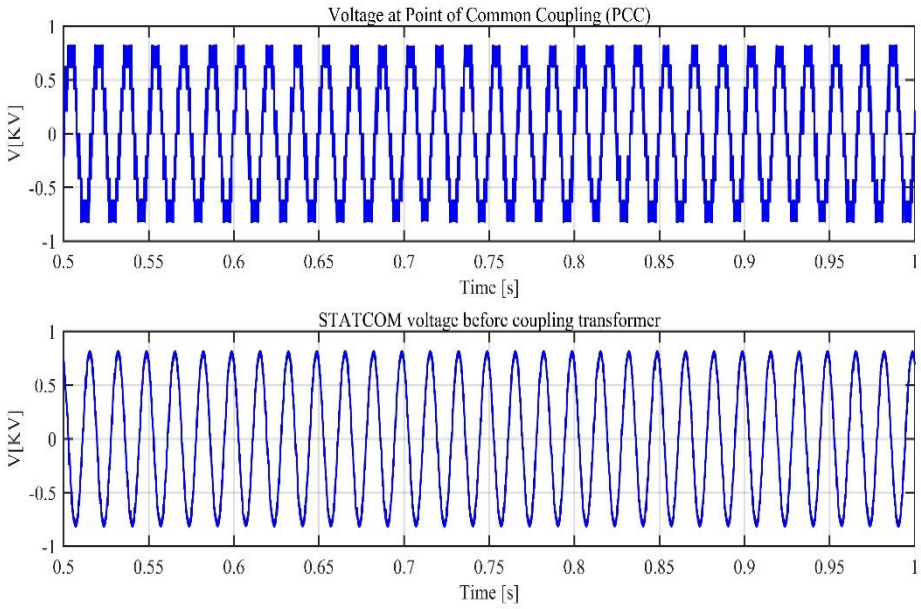
The controller parameters are optimized by using GA, and the output voltage is shown in Figure 4.43.



a.STATCOM off-state mode.



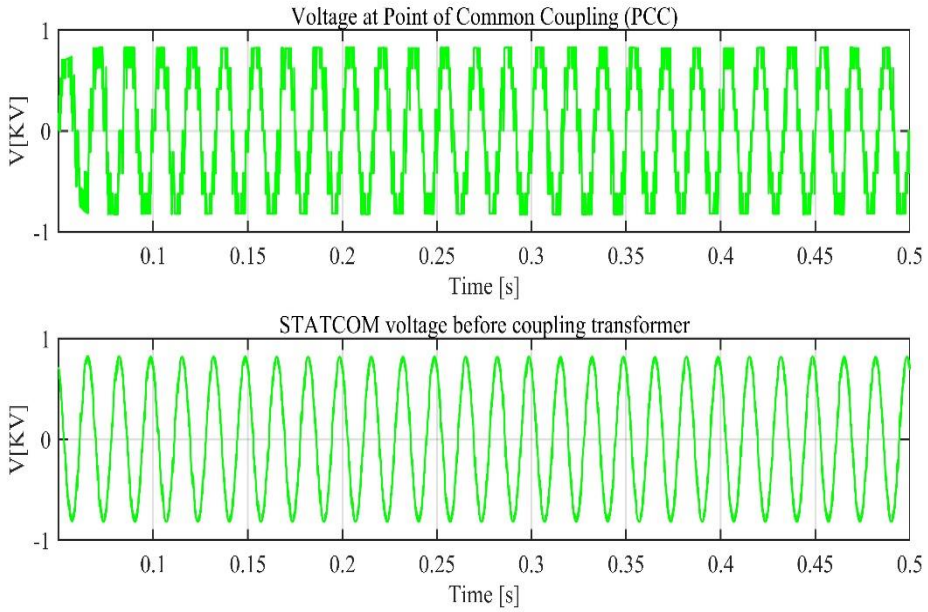
b. STATCOM in inductive – mode.



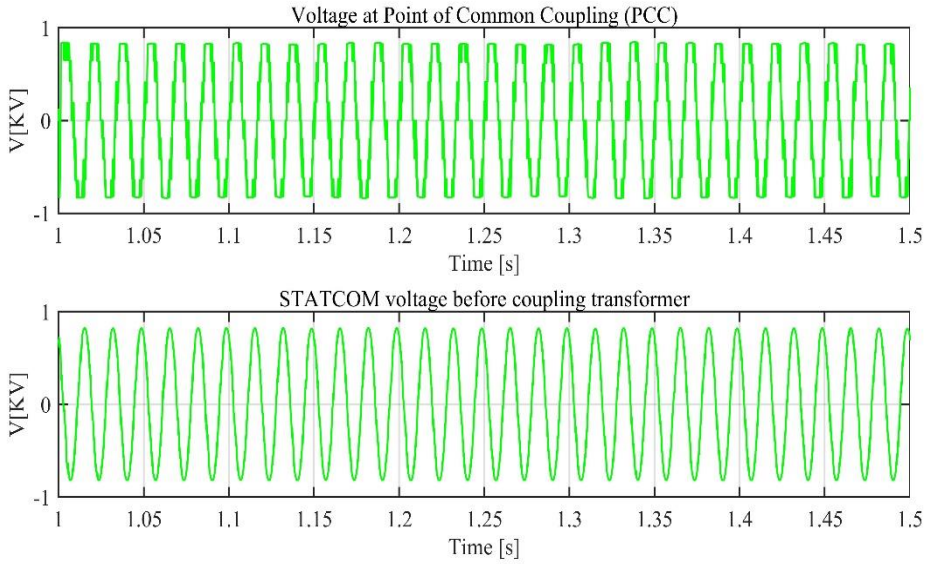
c. STATCOM in capacitive – mode.

Figure 4.43 STATCOM output voltages with PI controller based GA.

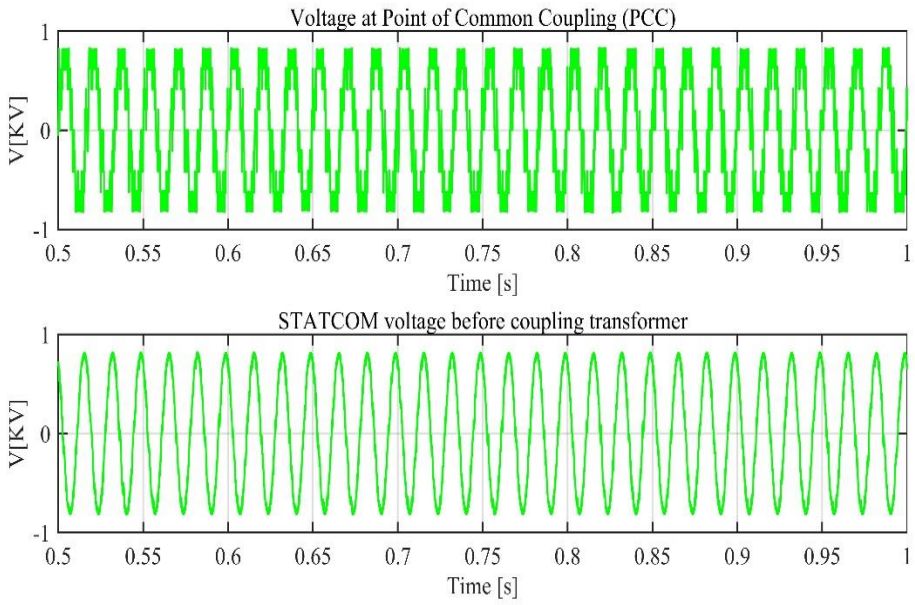
Figure 4.44 shows the output voltages for the nine-level inverter and the STATCOM after harmonics elimination filter, and the PI-controller is tuned by the trial-and-error method.



a.STATCOMoff-state mode.



b. STATCOM in inductive – mode.



c. STATCOM in capacitive – mode.

Figure 4.44 STATCOM voltages with PI controller based on trial and error

It can be observed from Figures 4.42, 4.43, and 4.44 that the inverter voltages are more stable for PSO followed by GA and trial and error method. The curves in Figure 4.45 show the grid voltage for STATCOM and reference grid voltage with controller parameters optimization by PSO, GA, and trial and error.

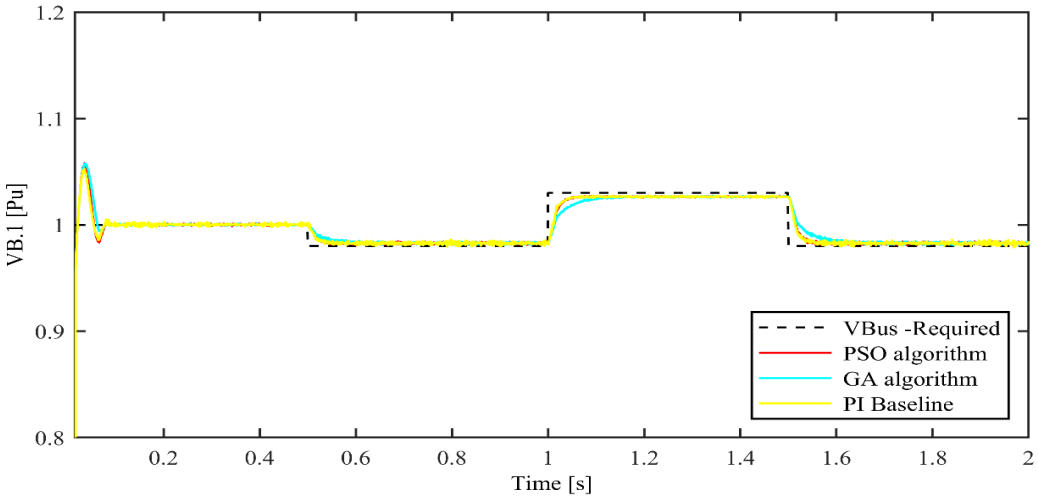


Figure 4.45 Grid voltages with PI-based PSO, GA, and trial and error

The STATCOM DC capacitor voltage with controller parameters optimized by using PSO, GA, and trial and error method appears in Figure 4.46.

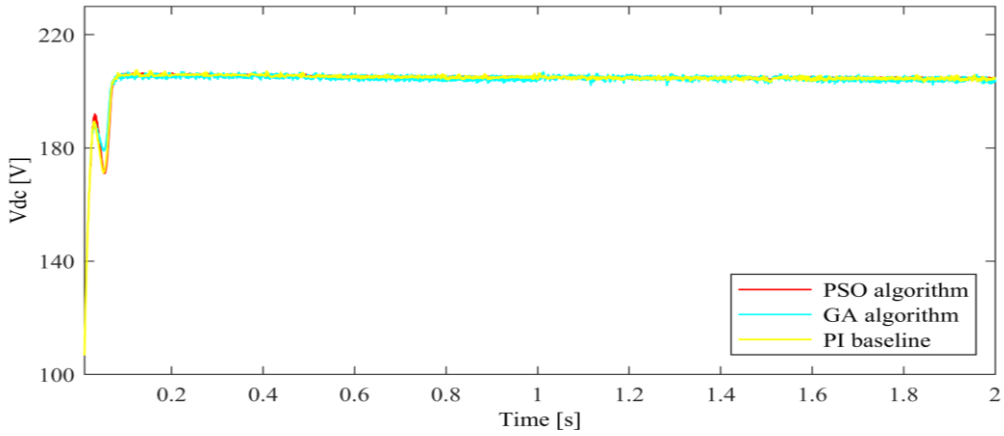


Figure 4.46 DC-link voltages by PI-based PSO, GA, and trial and error

The active power for STATCOM on-grid is shown in Figure 4.47.

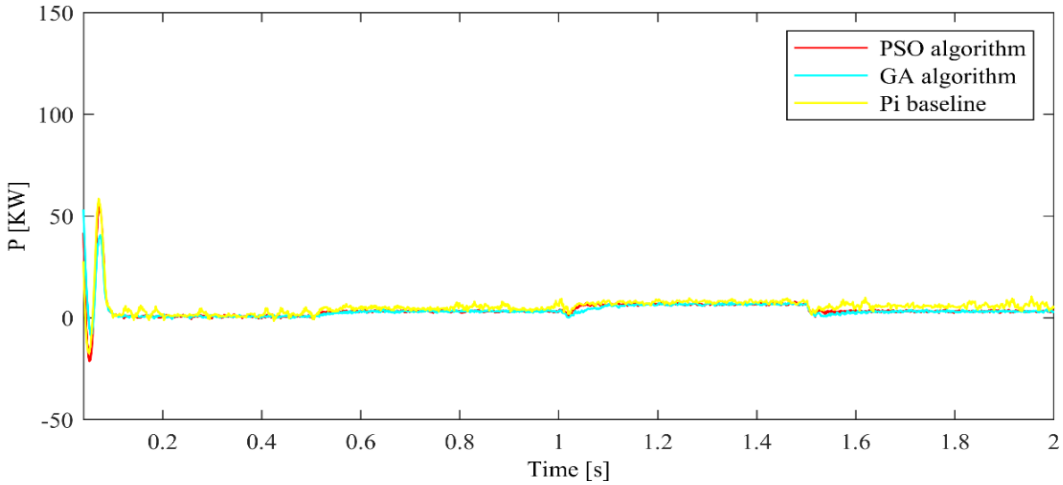


Figure 4.47 Real power with PI-based PSO, GA, and trial and error

The reactive power for STATCOM on-grid is shown in Figure 4.48.

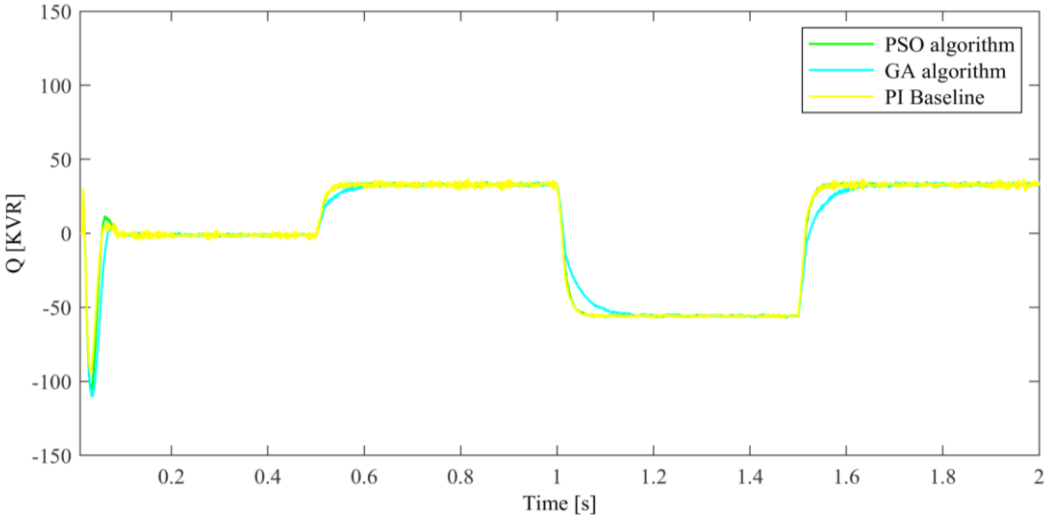


Figure 4.48 Reactive power with PI-based PSO, GA, and trial and error

The three-phase voltages for the STATCOM are shown in Figure 4.49.

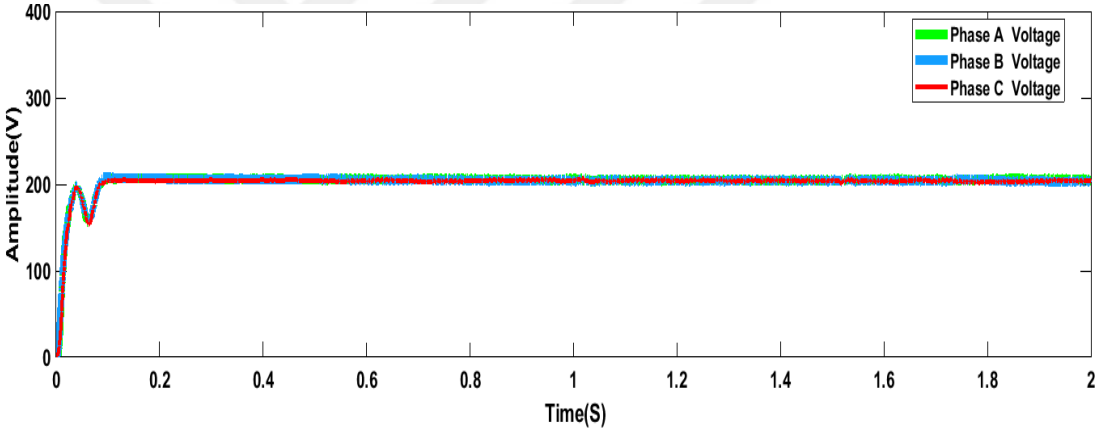


Figure 4.49 Three-phase system voltage

The measured and reference reactive currents for STATCOM are shown in Figure 4.50.

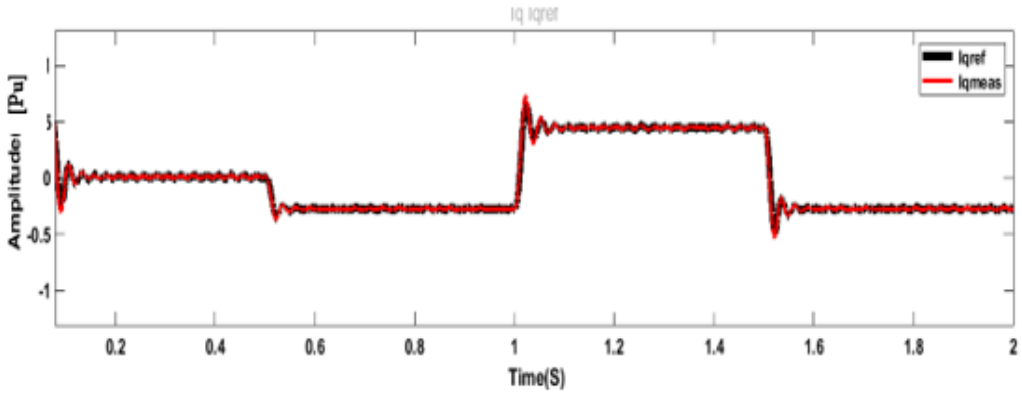


Figure 4.50 Measured (red)and reference(black) reactive currents

The Measured and reference direct currents for STATCOM on-grid are shown in Figure 4.51.

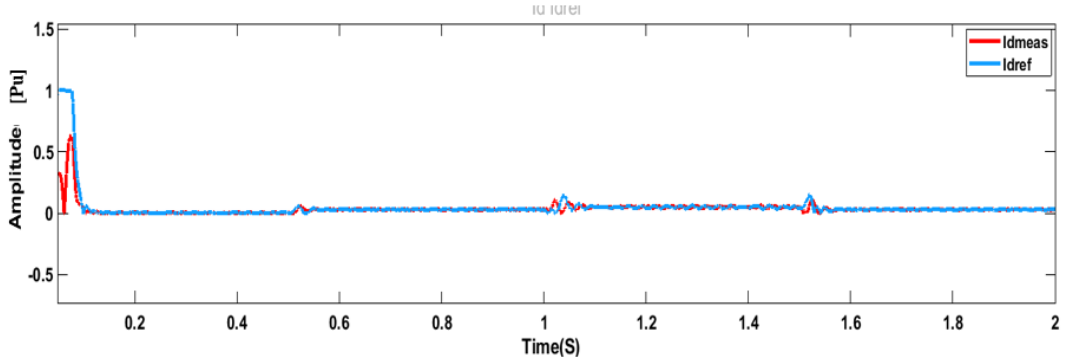


Figure 4.51 Measured(red) and reference(blue) direct currents

4.4.3 Objective Function

The fitness or objective function describes the mathematical relationship between optimized parameters that utilize the optimization parameters as inputs. in this problem, the objective function is responsible for demoralizing out the oscillations of the STATCOM controller. The different indices are considered in the literature for evaluation optimization performance [83,85]. Such indices are Integral absolute error (IAE), Integral square error (ISE), and Integral square time error (ISTE). However, IAE is extensively used with digital simulation for such a system that is employed since ISE is deemed controllers' error only without attention to simulation time.

Meanwhile, in the power system stability problems, time is a critical aspect in dying out the system oscillations, furthermore limitation the duration of the settling time for the system[86].

Therefore, performance evaluation parameters ITSE and ITAE have additional time coefficient which is multiplied by the error function that indicates long-duration errors. Not only this, this criterion is very suitable for systems demanding a fast settling time. In other words, the evaluation index ITAE has the advantage of providing smaller overshoots and oscillations as compared with the ISE or ISE performance index ,and besides, its common sense against all performance indices. Thereby, the ITAE performance index is defined as the objective function for tuning the controller parameters of STATCOM with particle swarm optimization (PSO) and genetic algorithms (GA) optimization methods. The performance index with consideration coefficient of time can be expressed as follows:

$$\mathrm{ITAE} = \int_0^{\infty} t.|\mathrm{V_t(t)}|\mathrm{dt} \quad (4.23)$$

$$\mathrm{ITSE} = \int_0^{\infty} t.\mathrm{V_t(t)}^2\mathrm{dt} \quad (4.24)$$

where $\mathrm{V_t(t)}$ and t represent error value on voltage signal and simulation time, respectively.

Generally, numerous optimization algorithms are available for tuning the PI-controllers gains. However, in this work, the PSO is used as a baseline algorithm to determine the optimum PI controller parameters and compared with the performance of the GA[84]. In both presented methods; the objective function has been defined as the integral time square error (ITSE) and integral time absolute error as illustrated in Table 5.1. The errors are minimum for PSO as compared with GA.

Table 4.3 Optimal parameters of a different system

Controller conflagration	AC voltage regulator		DC voltage regulator		ITAE	ITSE
	K_p	K_i	K_p	K_i		
PI controller with (PSO)	10.00	1716.85	0.08	0.05	0.01	2.315e-5
PI controller with (GA)	10.00	872.24	0.08	0.05	0.011	0.001
PI controller	16	1900	0.08	0.05	0.08	0.005

The comparison between the PSO and GA optimizations methods to tune PI-controller is conducted in table 4.3 above. The results confirmed the efficiency of PSO among GA and conventional methods for tuning the PI controller while the PSO method has the minimum ITSE. It is found that the PSO-PID tuned optimal controller parameters for the proposed STATCOM with a hybrid nine-level inverter.

4.4.4 Discussion

The proposed topology of hybrid multilevel inverter -STATCOM ± 38 KVAR has appeared in Figure 4.28. The presented system consists of four symmetric DC sources connected in series that form the DC link part of the voltage source inverter. At the same time, the AC side of the nine-level inverter is connected as a three-phase star

form. The voltage control mode is implemented for grid voltage control and reactive power injection balancing. Basing on the grid reference voltage waveform, the reactive power can be injected/absorbed from the system according to the reference waveform variation. The simulation time is two seconds, the STATCOM worked in the off-state mode from 0 to 0.5 seconds, and there is no reactive power transfer in this mode where the reference waveform is set to one. The STATCOM worked in a capacitive mode during the simulation time interval 0.5 to 1 second, and the reference waveform becomes less than one. In that simulation interval, the STATCOM begins to compensate reactive power to the grid. While in the simulation time from 1 to 1.5 seconds, the STATCOM works in inductive mode and the reference waveform is above one. Thus, the STATCOM begins to absorb reactive power from the grid and acts as an inductive load to balance the grid voltage. The STATCOM based on the hybrid nine-level inverter was presented and the two optimization methods were used for tuning the PI- controller gains. The numerical results confirmed that the PSO tuning method has notable stability in obtaining the controller gains as compared with the GA algorithm and the classical trail and error tuning . The STATCOM based on hybrid multilevel converter consists of 12 switches per phase for generating nine-level, while in literature the cascaded H- bridge multilevel converter consists of 16 switches per phase to generate nine levels per phase. And by Basing on this bases, it can be observed that the proposed hybrid inverter provides a notable reduction in the number of switches required to create levels.This means it establishes its effectiveness in the ship power system.

CHAPTER V

HARDWARE IMPLEMENTATION

5.1 Cascaded Multilevel Inverter

The hardware module implemented here is a cascaded H-bridge multilevel. This experimental setup is developed to reveal the effectiveness of the controller. For developing the hardware setup, an electronic design automation software for printed circuit boards (PCB) is used. There are four switches for each bridge, the voltage at the terminal of each switch is 12V, and there are three DC-DC converters to supply each bridge. Since the two low-side switches of the circuit have the common grounding, three DC-DC converters are sufficient for this circuit and thus the two switches below are supplied from the same DC-DC converter.

The hardware setup is sampled by the internal 12-bit ADC of the DSP C2000 device. The reason behind selecting this controller is due to its high number of PWM ports. Thus, It can be used to control the 24 switches of the three-phase inverter while in other hardware module implementations the Arduino Nano controller is suffecient to drive the utilized switches. Moreover, using Arduino Nano in these implementations leads to reduce the footprint of the whole module.

A Hall sensor was used to transfer the current signal into the voltage range of approximately 0 to 5V with a 0.25V offset. Then the sensor continued transferring the voltage range of approximately 0 to 3V with offset using the resistor divider and external filter and lastly inputting to the micro-controller unit analog digital converter. In order to develop the hardware switching circuit, an ePWM module was used. One ePWM module can output two PWM signals with dead-time implementation: EPWMxA and EPWMxB. Six ePWM modules were used to generate 12 PWM signals and then an external NOT gate circuit was developed to generate the opposite signals as shown in the following figure. Figure. 5.1 illustrated the hardware setup for the conventional cascaded inverter.

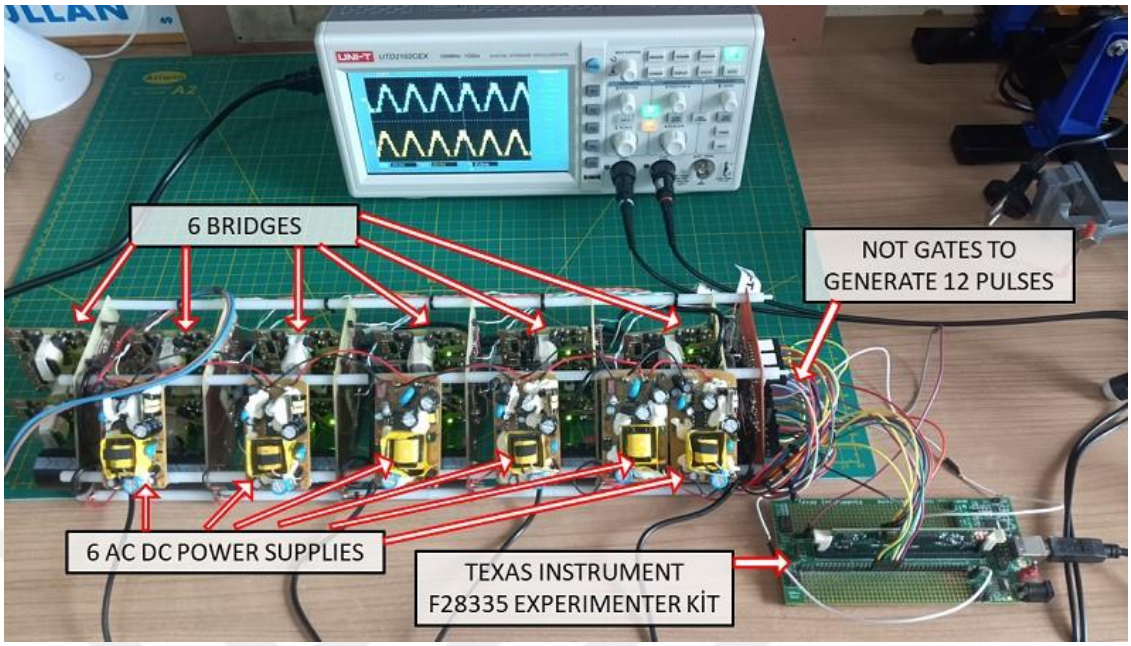


Figure 5.1 Hardware setup for the conventional cascaded inverter.

A total of 24 signals was generated from both the C2000 MCU and the NOT gates circuit to drive the three-phase five-level CHB MLI, by switching the 24 MOSFET switches. Each drive has its own insulated DC-DC power circuit, as illustrated in Figure 5.1 above. PWM pulses were obtained by using a regulating pulse-width modulator, an internal soft-start, and latching. This experimenter kit is highly programmable, extremely flexible, and simple to use while having the capacity of producing complex pulse width waveforms with reduced CPU overhead or intervention. Each ePWM module has two PWM outputs: ePWMxA and ePWMxB. All ePWM modules in the C2000 device are identical, and one module can be used simultaneously to generate synchronized pulses. This module has a high resolution which reaches 159 picoseconds. A built-in dead-band sub-module was used to protect the two switches (e.g. SW1 and SW2) from being switched on simultaneously and creating a short circuit case. A general block diagram of the hardware module is demonstrated in Figure 5.2.

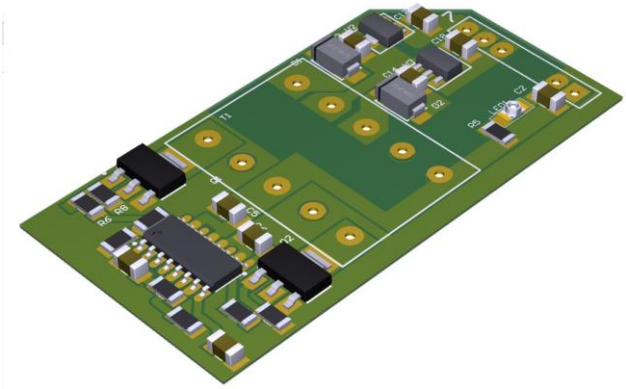


Figure 5.2 A general block diagram of the hardware module

Figure 5.3 demonstrates the developed circuit for each bridge after mounting the components on the surface of PCB. Each component is chosen carefully to fit properly in the exact location in the circuit. It is apparent that there are four switches with three DC-DC converters.

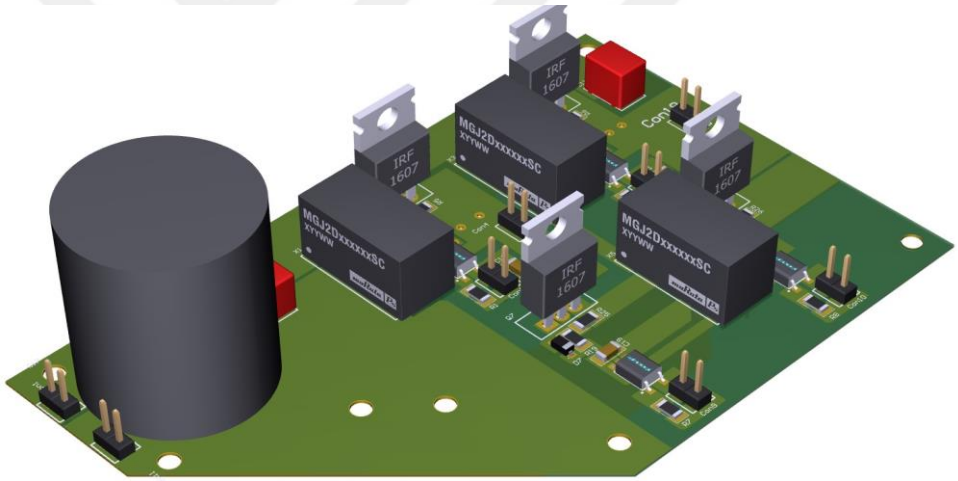


Figure 5.3 Circuit diagram after mounting the electronic circuit

The hardware setup was provided with 6 bridges, two for each phase, and each bridge has 4 MOSFET switches. There are also six AC DC power supplies for supplying the 6 bridges. Moreover, the TEXAS INSTRUMENT F28335 EXPERIMENTER KIT was used to generate PWM for the 24 switches. An illustration of SPWM is provided in Figure 5.4.

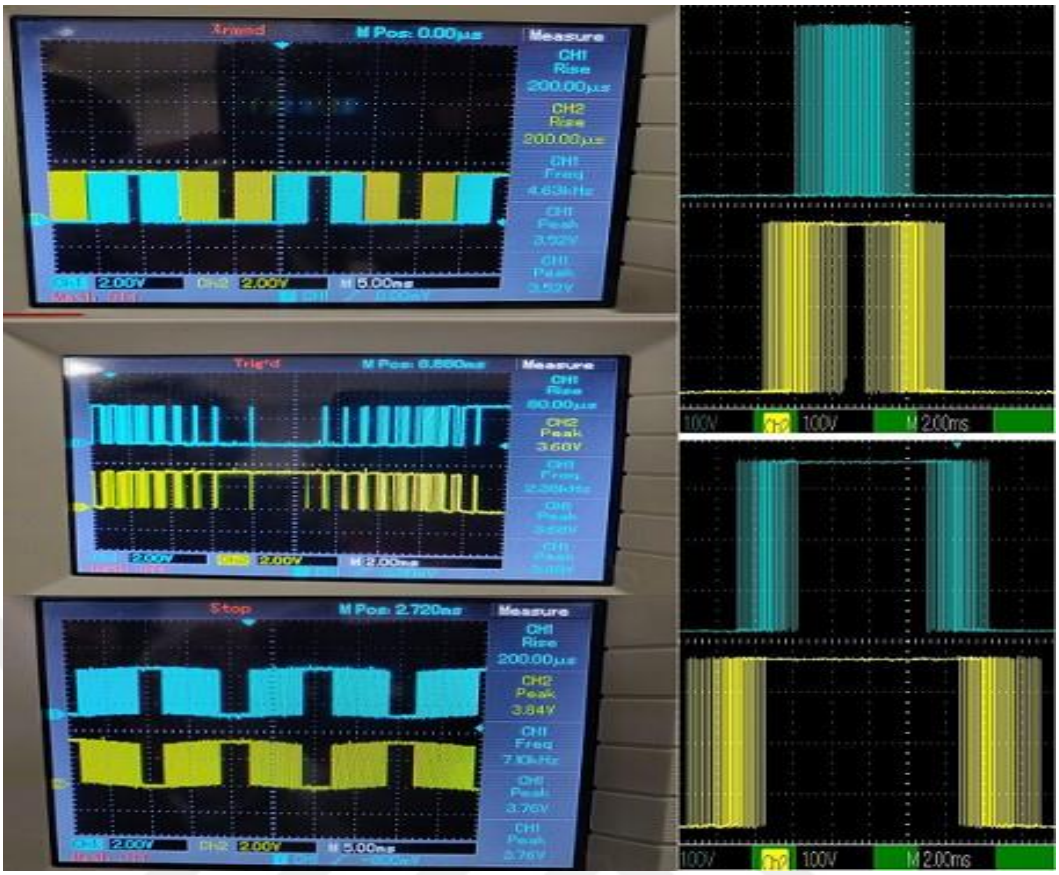


Figure 5.4 Sin pulse width modulation of the inverter

It can be seen that at the beginning of each pulse it had a short duty cycle, then it was increasing gradually and decreasing again. This creates a smooth sin wave without bulky filter components being required. For any of the two switches above each other, it is very important to avoid having both of them switched on simultaneously as this will create a short circuit situation. Due to this restriction, the width of the pulses has to be the opposite of each other as shown by blue and yellow pulses in Figure 5.4. The developed design for the gate drive generates two voltage levels +15 v and -5 v which makes the MOSFET switches accurate and rapid. The footprint of each part has to be chosen properly. In this study, the datasheet of a component was studied and the dimensions were calculated to generate the final shape of the PCB. The generated magnetic field from each component was considered during the mounting to avoid any interference effect between the components. Also, in the practical circuits, proper isolation between high voltage and low voltage regions has to be implemented (DC and AC power circuits and the gate drive circuit). Different separated circuits were used in this research. Besides, the gate drive circuit was placed as close as possible to the MOSFET to avoid gate ringing, parasitic inductance and to keep the frequency

distortion as low as possible. The circuit diagram of the gate drive circuit generated by electronic design automation software is shown in Figure 5.5.

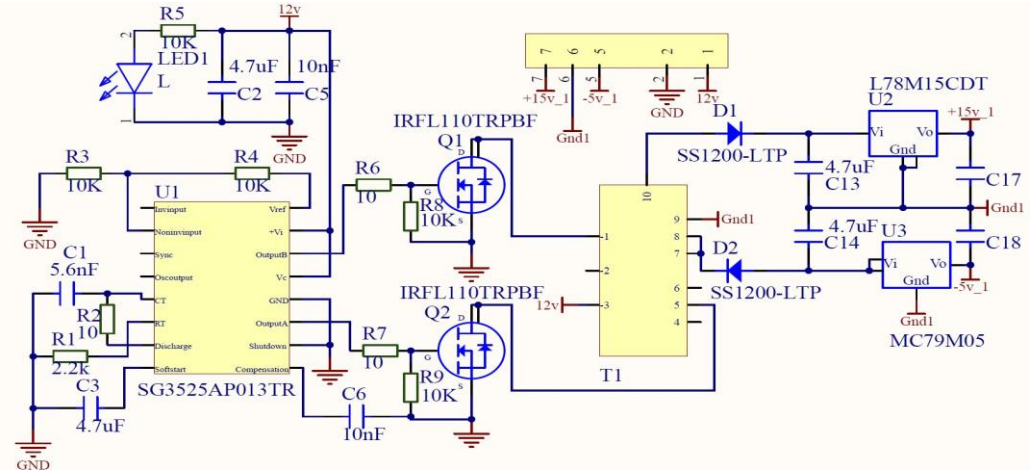


Figure 5.5 Circuit diagram of the gate drive circuit

The output voltage generated from the hardware setup is presented in Figure 5.6. The -phase-to-ground voltage shows the five levels. The generated PWM was effective and produced the correct voltage at the output of the inverter.

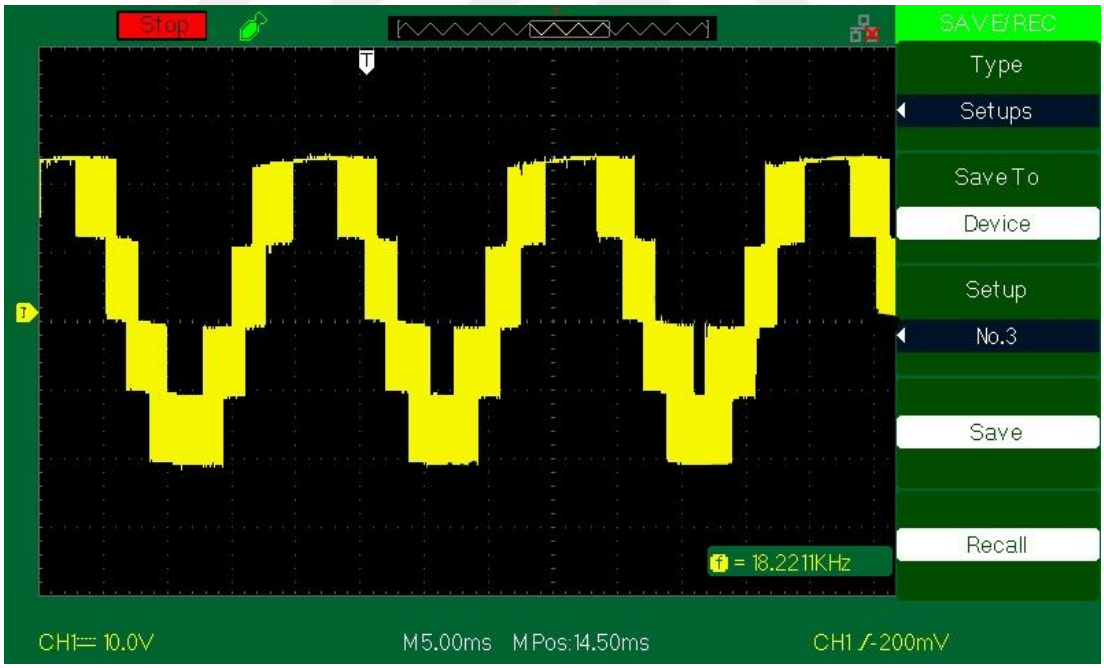


Figure 5.6 The generated voltage at phase-A

The output current generated from the inverter when connected to a resistive load of 110Ω is presented in Figure 5.7. The current sensor signal is connected to an RC low pass filter with a cutoff frequency of 2 KHZ to improve the sensor accuracy by mitigating electromagnetic interference(EMI).

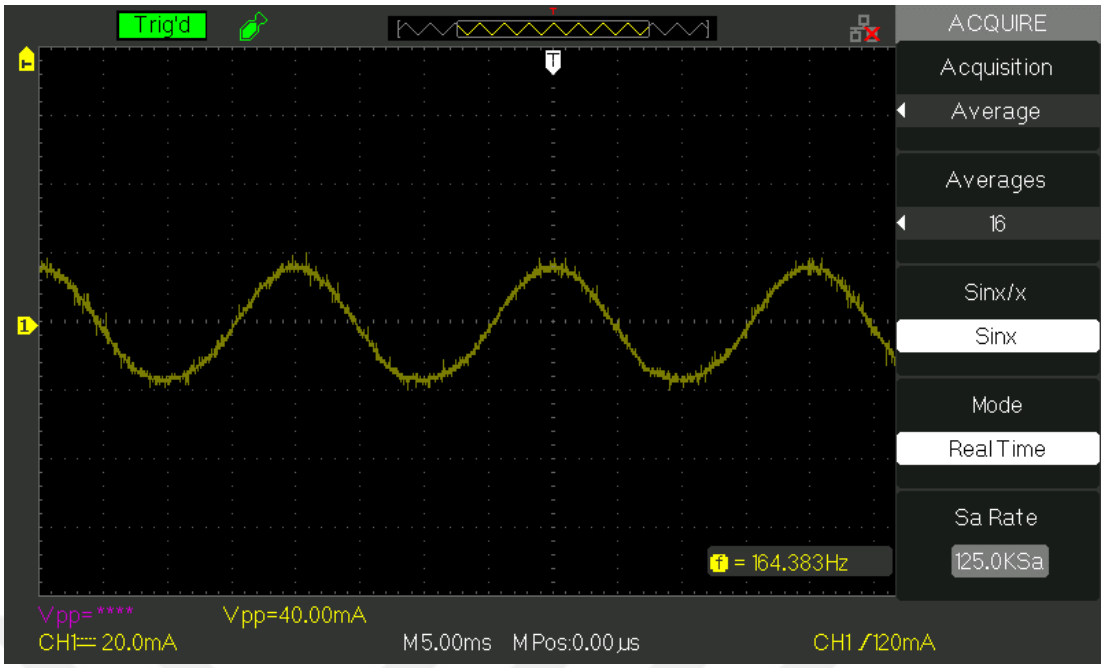


Figure 5.7 The generated current at phase-A

5.2 Asymmetrical Cascade H Bridge Inverter Hardware Implementation

In this hardware implementation, the asymmetrical and symmetric inverters are performed. The designed inverter can operate as an asymmetrical inverter if it is fed by different DC sources. At the same time, it ensures the symmetric operation when it is supplied with equal inputs. So this module represents two modules in the same experiment kit. The reason behind the flexibility of operation is the dynamic and accuracy of the implemented code. The inverter circuit is composed of three H- bridge. The MOSFETs used here are IRFZ44N while the microcontroller is the Arduino Nano which is responsible for gate signal generation according to the injected software code. Figure5.8 shows the overall module of the implemented inverter.

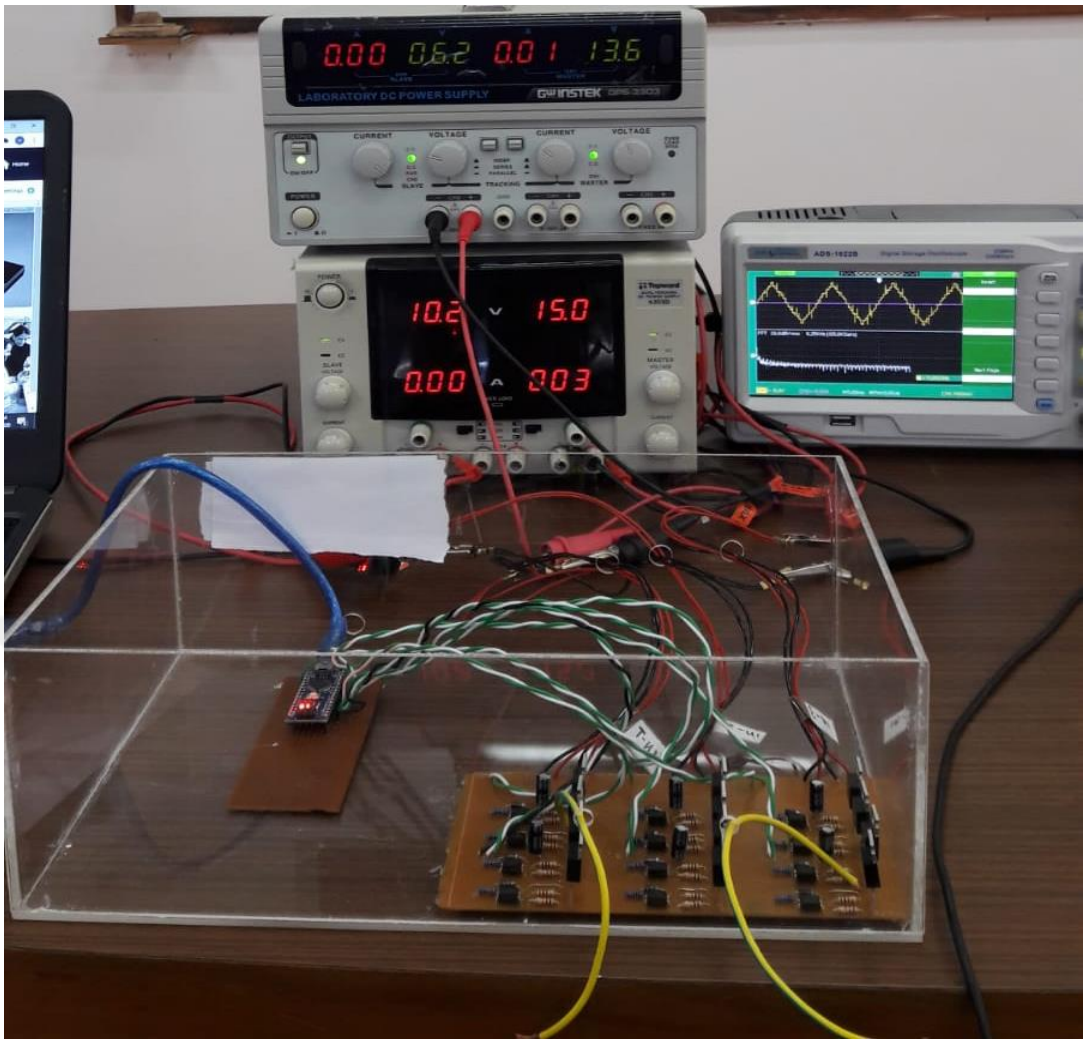


Figure5.8 Hardware setup for symmetric/asymmetric cascaded inverter.

5.2.1 Symmetrical Mode Cascade H Bridge Implementation.

In this mode, as it is also clear from its name, all the three sources will be equal to all the three H bridges. The produced AC signal will be composed of seven levels in its output. Figures(5.9-5.10-5.11)shown below show the first, second, and third output H-bridge signals. All the DC sources are equal in this implementation and they are set to 10 volts.

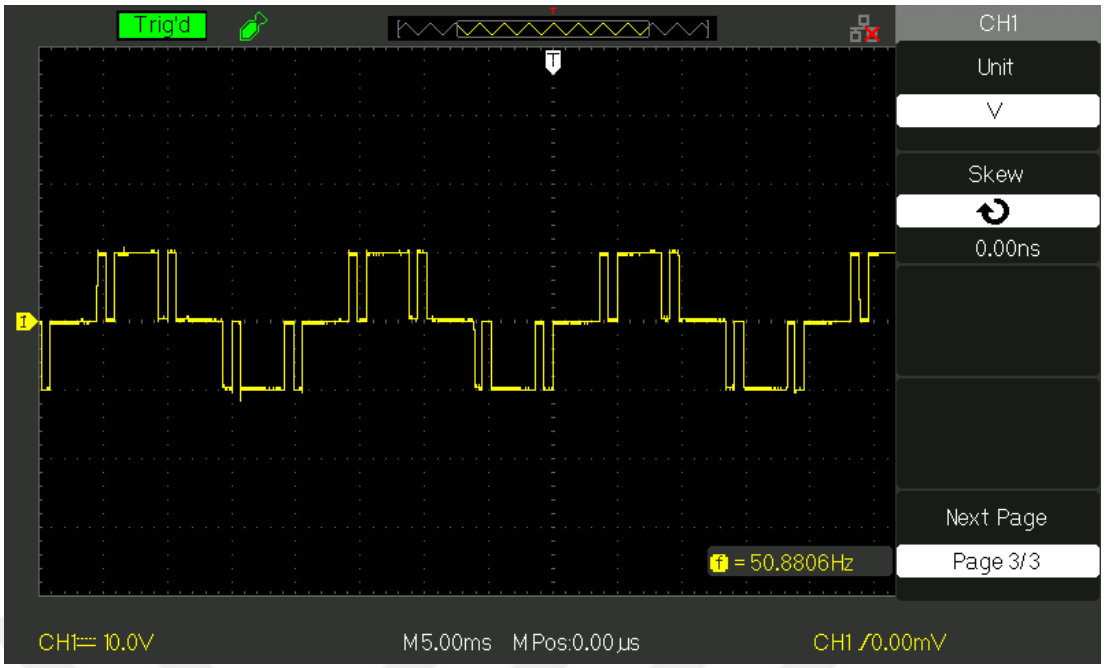


Figure 5.9 First H bridge output.

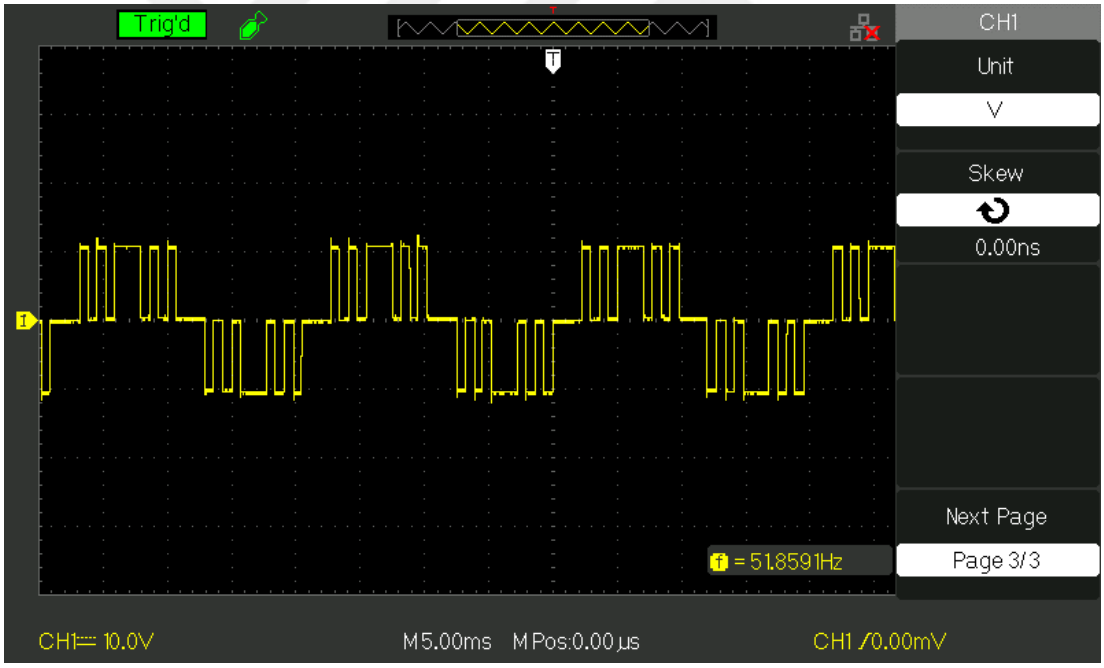


Figure 5.10 Second H bridge output.

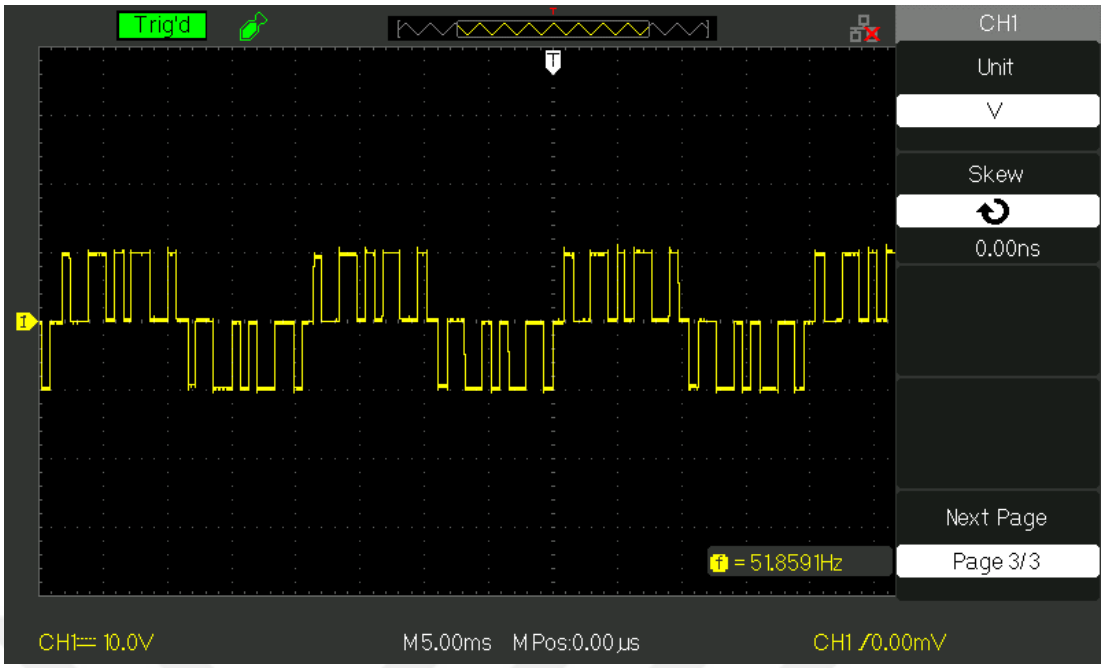


Figure 5.11 Third H bridge output.

The final seven levels output inverter is shown in figure 5.12.

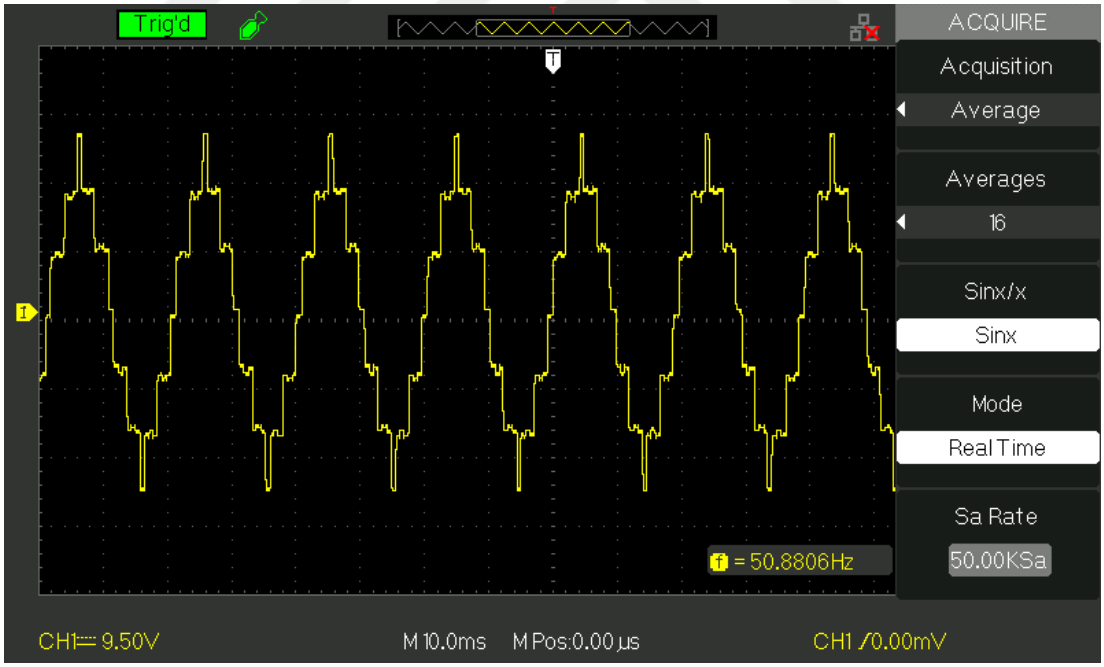


Figure 5.12 Seven levels symmetric inverter output

5.2.2 Asymmetrical mode Cascade H Bridge implementation.

In this mode, the three DC sources of the inverter are different from each other. The produced inverter AC output signal is composed of 15 levels. The first DC source is

set to 5 volts, the second is set to 10 volts and the third is set to 15 volts. The figures(5.13-5.14-5.15) shown below show the pulse signals for the first, second, and third bridges.

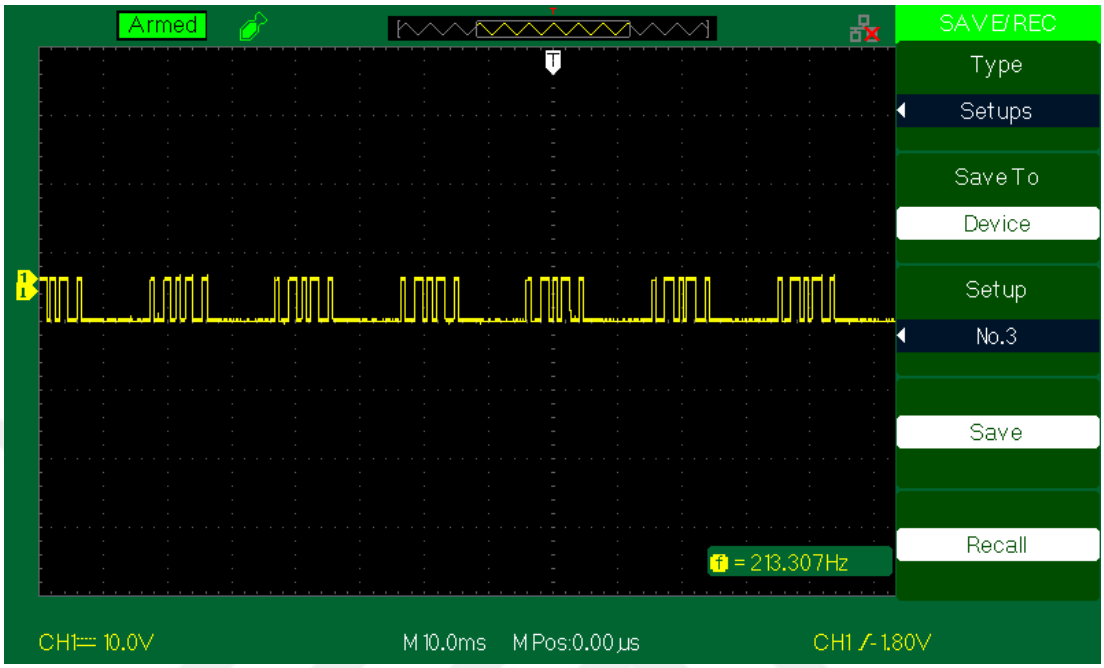


Figure 5.13 First H bridge pulse signal

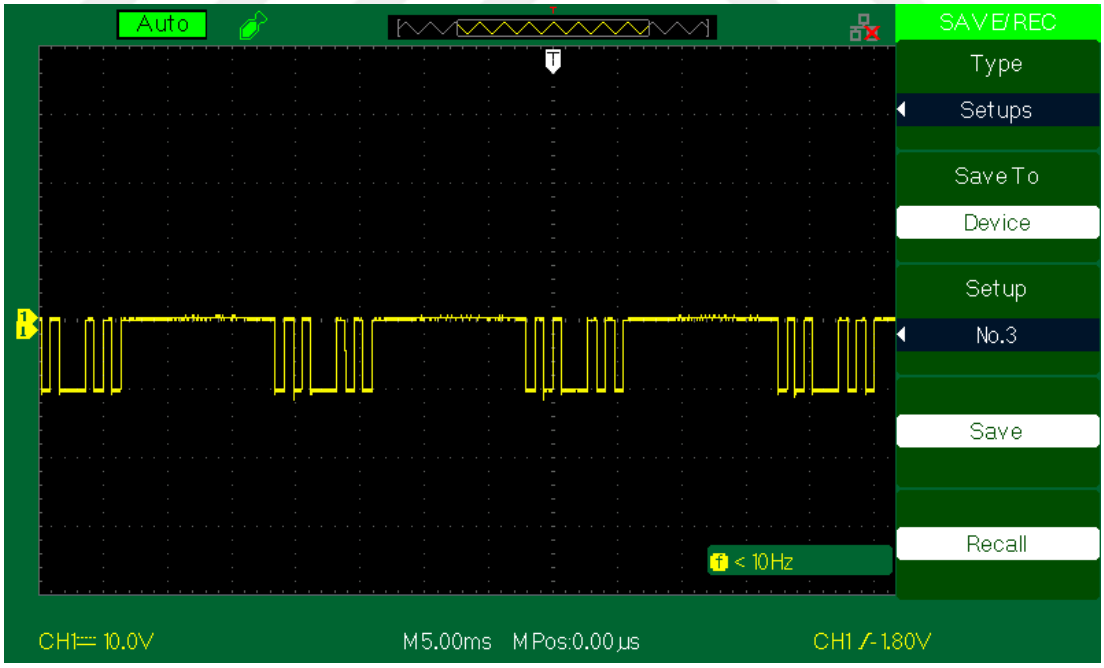


Figure 5.14 Second H bridge pulse signal

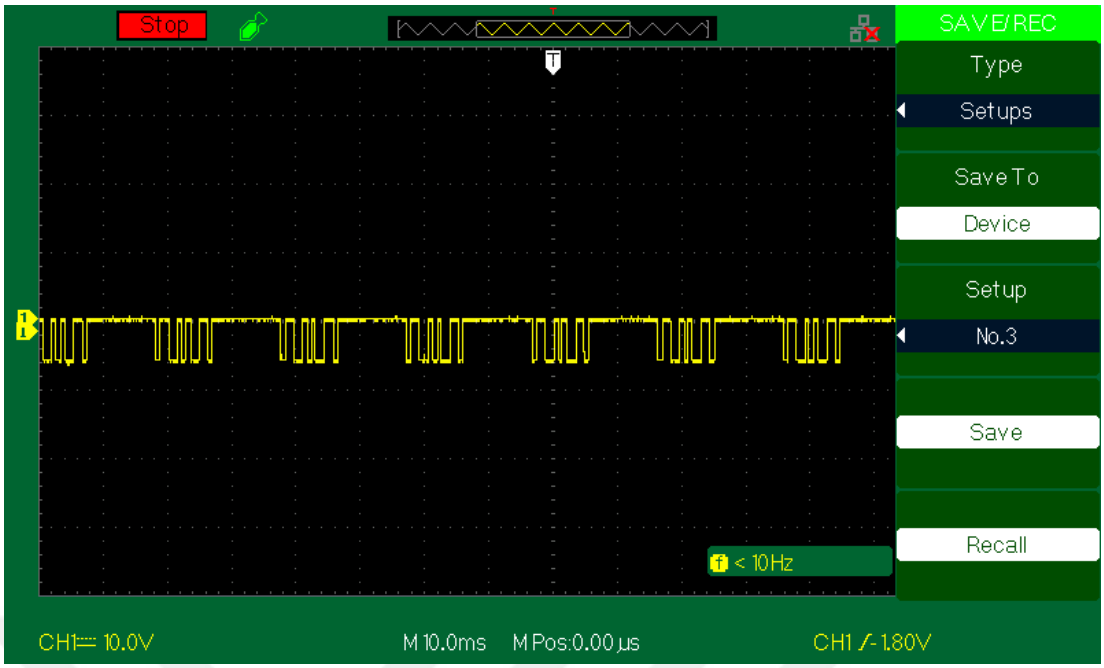


Figure 5.15 Third H bridge pulse signal

The figures (5.16-5.17-5.18) shown below show the signals for the first, second and third bridges.

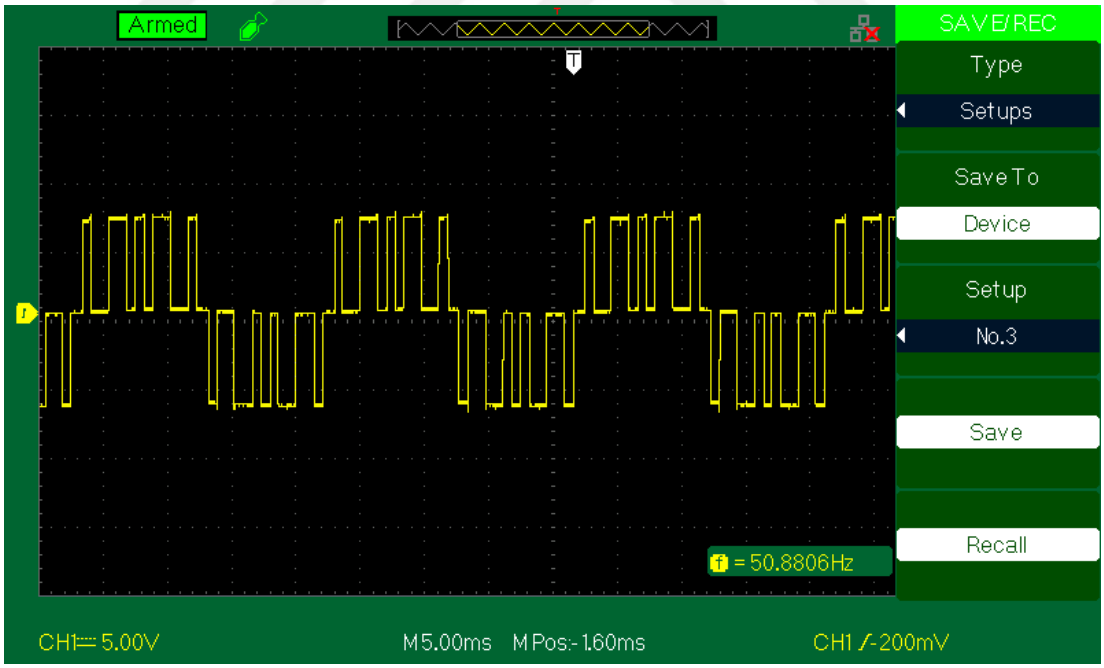


Figure 5.16 First H bridge output signal

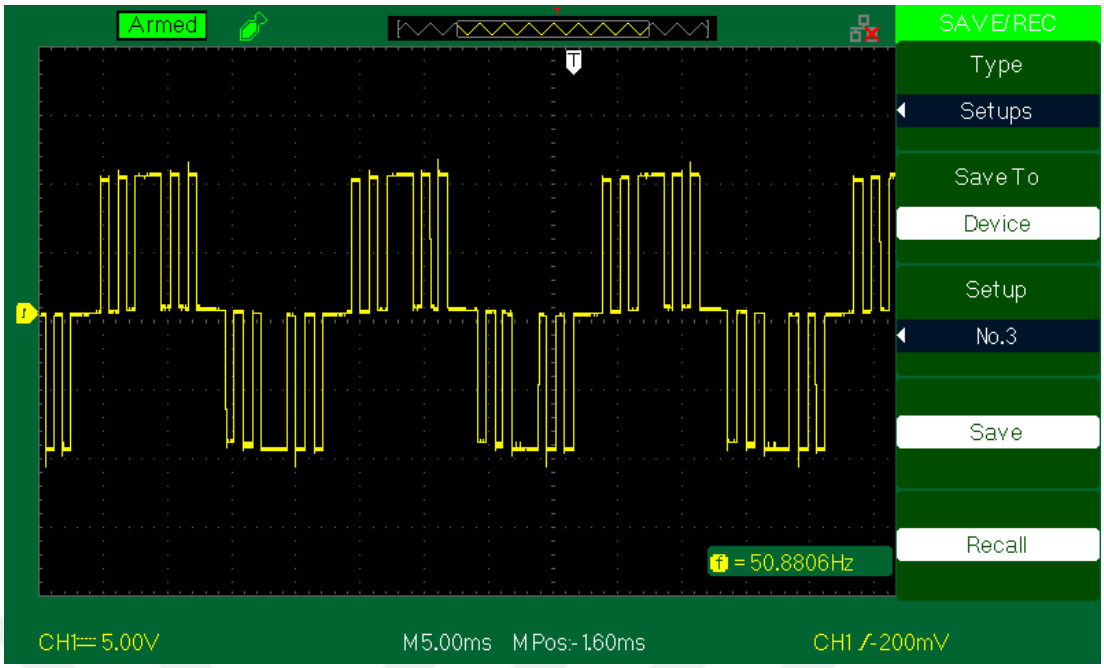


Figure 5.17 Second H bridge output signal

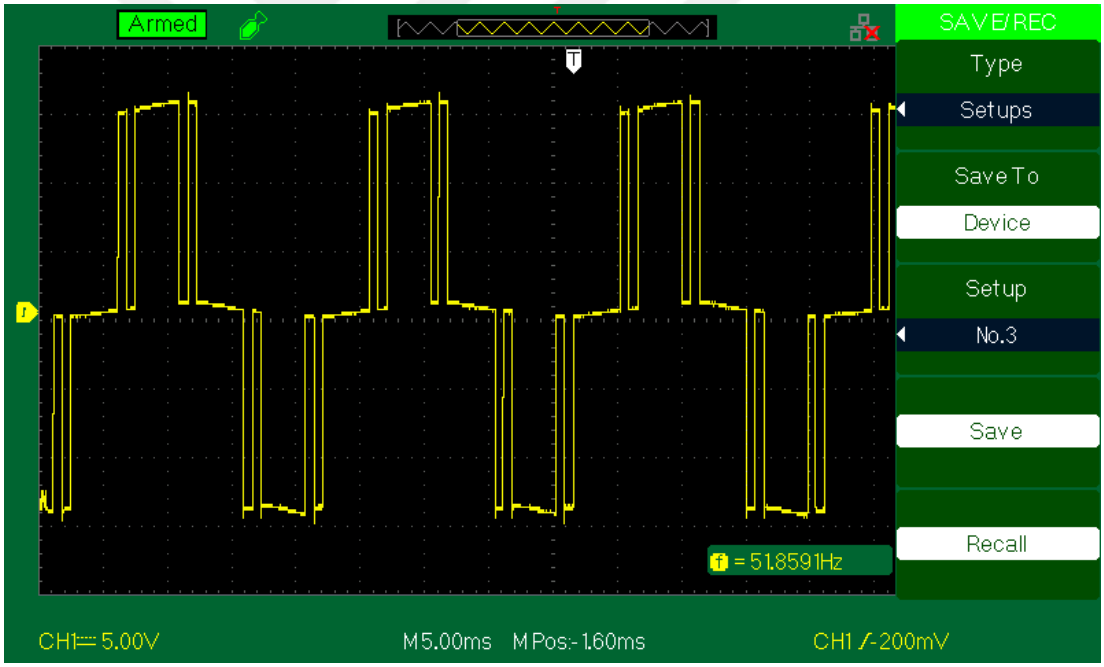


Figure 5.18 Third H bridge output signal

The final fifteen levels output signal produced by the summation of the individual bridges voltages is shown in Figure 5.19 below.

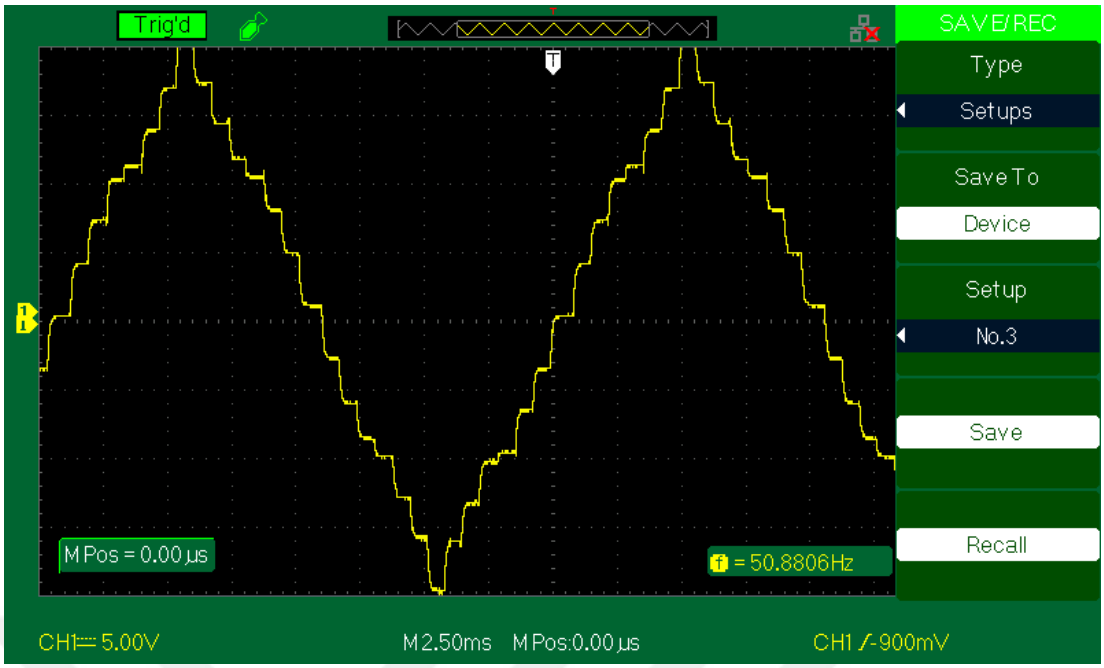


Figure 5.19 Final fifteen level output signal

The output current generated from the hardware setup when connected to load of 110Ω is presented in Figure 5.20. The current sensor signal is connected to an RC low pass filter with a cutoff frequency of 2 KHZ to improve the sensor accuracy by mitigating electromagnetic interference(EMI).

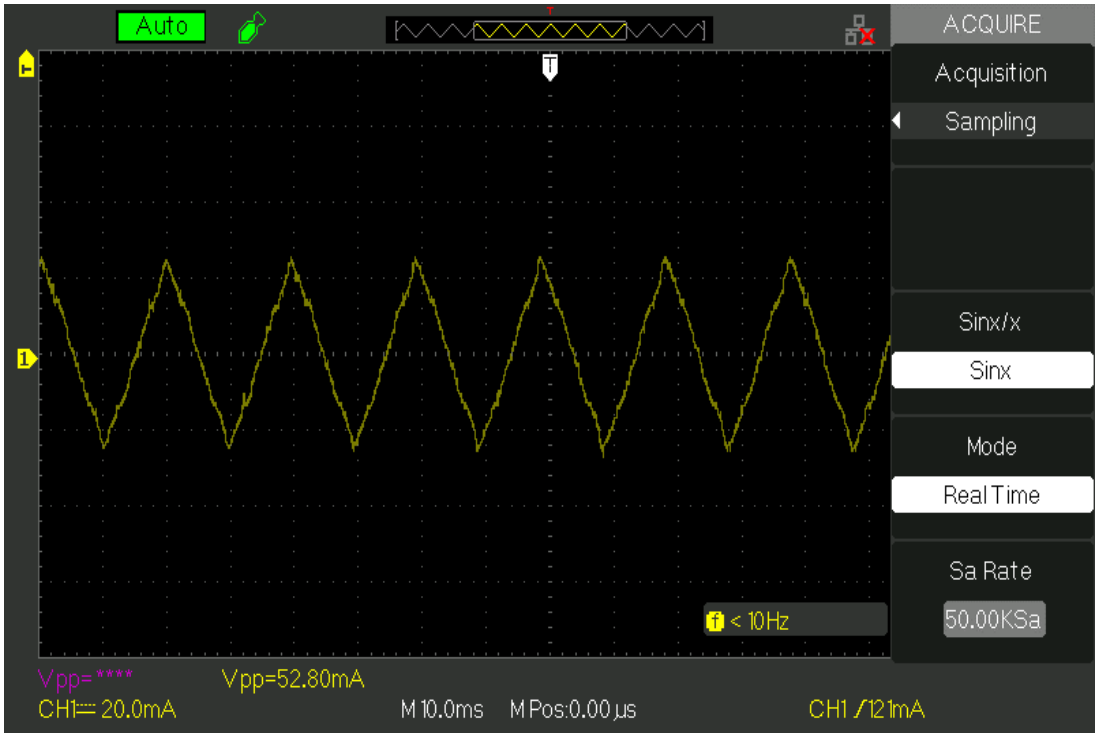


Figure 5.20 Output current for the asymmetrical inverter

5.3 Hybrid Multi-Level Inverter Hardware Implementation

The implementation of the nine-level hybrid inverter which depicted in Figure 4.14 is presented here. This inverter with its modern circuit used only twelve switches. The MOSFETs used here are NCEP0178AF while the gate drive is the TLP350 which is responsible for producing the proper gate signal to the twelve utilized switches. The microcontroller used here is the Arduino which leads to reduce the overall footprint of the inverter all the codes are given in Appendix E. Figure 5.21 demonstrates the designed printed circuit board PCB for the hybrid inverter. Each component is chosen carefully to be fit properly in the exact location in the circuit. It is apparent that the inverter contains twelve switches:eight for the level generator part and four for the polarity generator part. Each switch uses its own DC-DC converter and its gain drive.

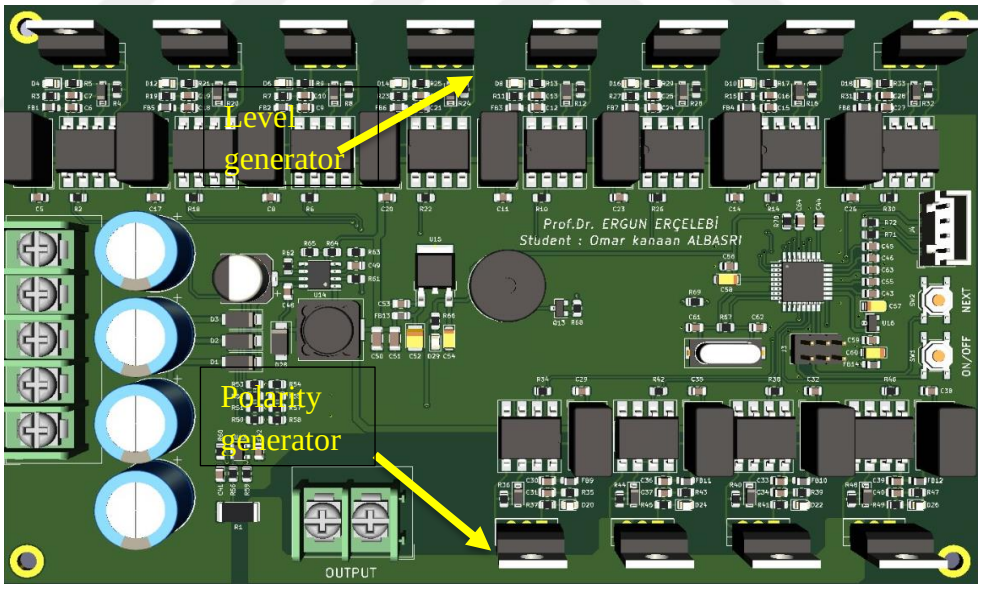


Figure 5.21 Designed printed circuit board (pcb)

The pin configration for TLP350 gate drive is shown below in Figure 5.22.

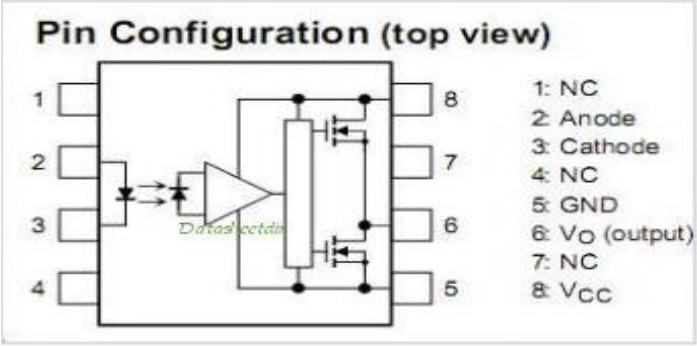


Figure 5.22 Pin configration for TLP350 gate drive

The schematic circuit for the gate drive is shown in Figure 5.23.

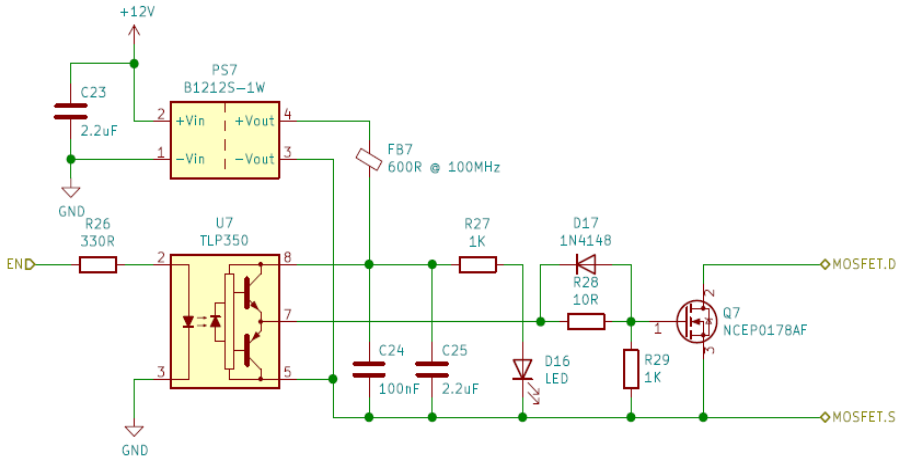


Figure 5.23 schematic circuit for TLP350 gate drive

Figure 5.24 demonstrates the developed circuit after mounting the components on the surface of PCB.

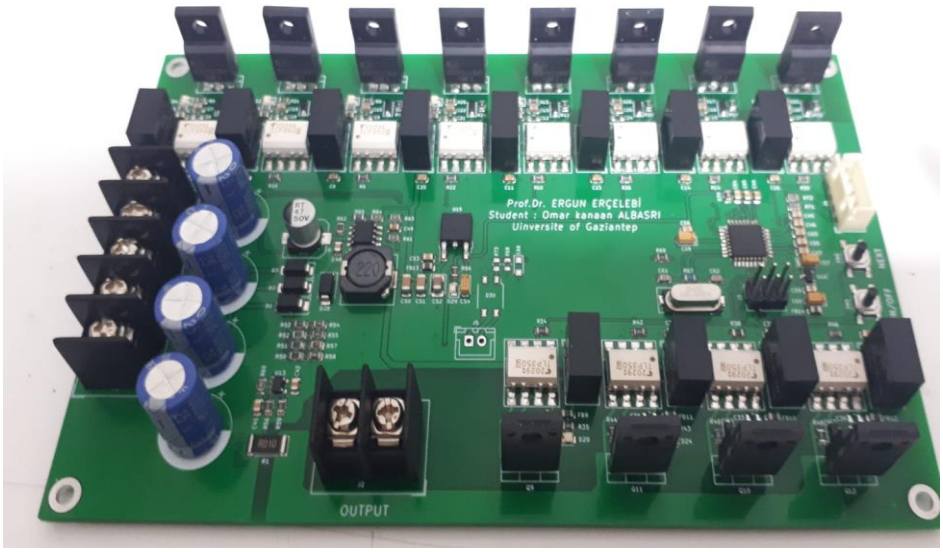


Figure 5.24 Final circuit with components mounting

The final nine levels output signal produced at the output of the polarity generator is shown in Figure 5.25 below.

Figure 5.25 Final nine level output signal

The output current and the output nine level voltage generated from the hardware setup when connected to load of 110Ω are presented in Figure 5.26. The current sensor

signal is connected to an RC low pass filter with a cutoff frequency of 2 KHZ to improve the sensor accuracy by mitigating electromagnetic interference(EMI).

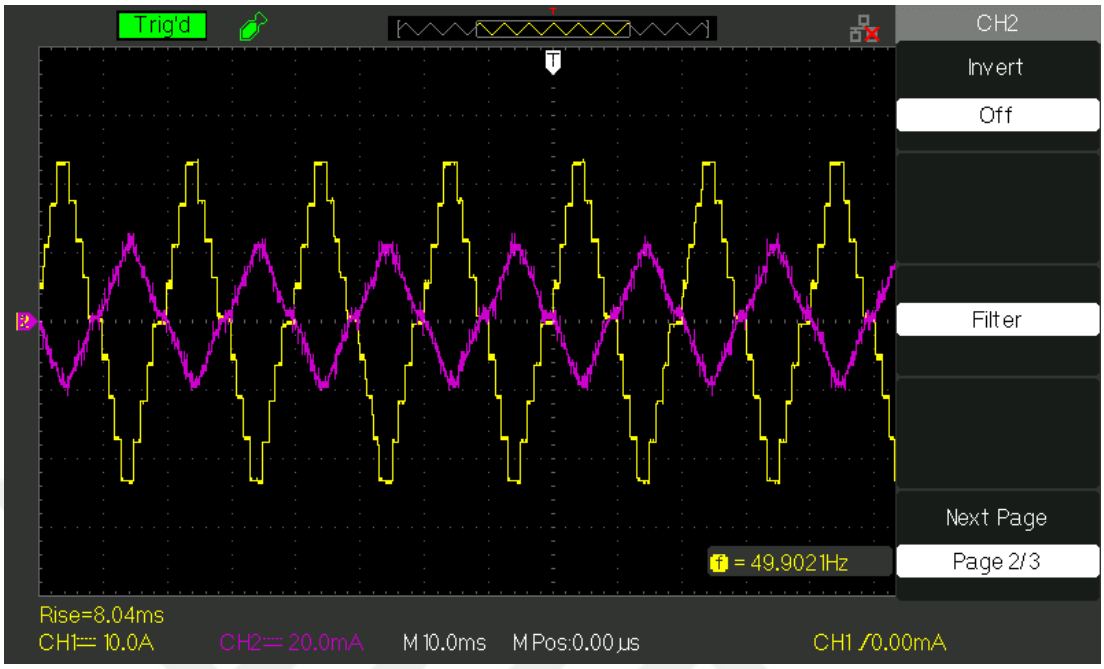


Figure 5.26 Output current and voltage for the hybrid inverter

The schematic circuit of the power supply unit for the microcontroller and the gate drive is shown in figure 5.27.

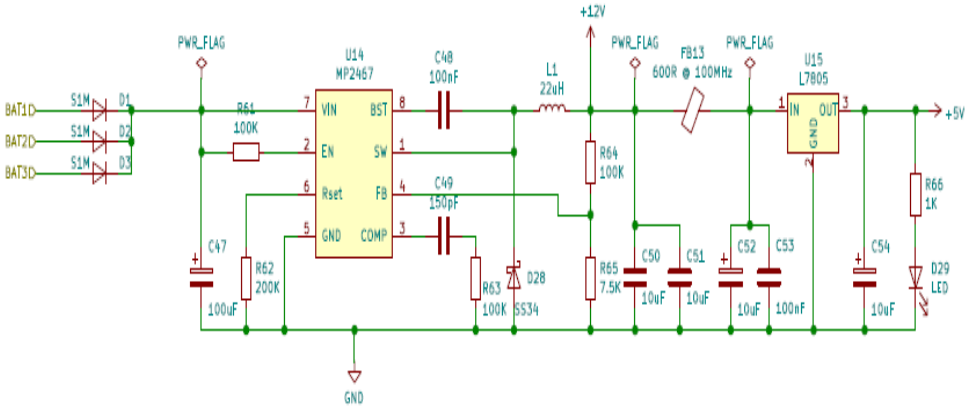


Figure 5.27 Schematic circuit of the power supply unit

CHAPTER VI

CONCLUSION AND SUGGESTIONS FOR FUTURE WORK

6.1 Conclusion

The thesis work involves many approaches to improve the performance of the multi-level inverter. The work process is accomplished into two parts: simulation and hardware. The simulation work is expanded into the off-grid and on-grid systems. The off-grid system is depicted in two experiments: the first one is the implementation of asymmetrical cascaded H-bridge inverter with charge balance control method as a control technique. The second experiment is the nine-level-twelve switch hybird inverter. The inverter is simulated in Simulink software using sinusoidal pulse with modulation technique. This inverter topology has superior performance, offering improved output waveforms over conventional topology in terms of the number of switches required, control system, and reliability. In the above topology, the switching operation is separated into high and low-frequency parts. This adds up to the efficiency of the converter as well as reducing the size and cost of the Inverter.

In addition, this simulation work also implements the charging system through a maximum power point tracking algorithm using a buck-boost converter. The results are promising as shown in the figures proving that the operating point is at the maximum for the PV panel. The battery is uninterruptedly charged as it can be seen from the charge state.

In the on-grid system, the work is done through two experiments: The first one deals with the operation of cascaded inverter within low voltage ride-through capability. Whereas during voltage drops, medium and large-scale grid-connected PV power plants require reactive or active power injection. However, no detailed studies have been carried out on the performance of grid-attached CHB inverters which serve as potential candidates for such type of grid-connected PV power plants.

Thus, this work has introduced a simple strategy for controlling the performance of the grid-attached CHB inverter during a voltage drop.

As an attempt to balance the inter-phase voltages, the injection of a zero-sequence voltage was applied while the voltage references of the bridges were modified to obtain the inter-bridge balancing. A feedback voltage compensator was used to significantly reduce the inverter's transient currents at the start of the voltage drop. Under various unbalanced voltage sag circumstances, a grid-connected PV power plant was used to conduct simulations and experiments to determine the effectiveness of the proposed control strategies. Based on the grid codes, the CHB inverter can supply the grid with the right amount of reactive and active power as well as achieve low voltage ride through. The suitability of the proposed control technique for medium and large-scale grid-connected PV power plants in periods of voltage drops was verified by the evaluation results.

In the second grid work, the STATCOM based on a hybrid nine-level inverter has been proposed, and the two optimization methods for tuning of the STATCOM PI-controller are studied. The comparison between PI-controller tuning methods based on optimizations and conventional tuning is also conducted. The simulation results confirmed the efficiency of PSO among GA and conventional methods for tuning the PI controller. It is found that the PSO-PID tuned optimal controller based on the proposed STATCOM with a hybrid nine-level inverter is performed satisfactorily and establishes its effectiveness in the ship power system. The results of the tuning method based on PSO have illustrated the capability of the controller for tracking the required grid voltages under different load conditions. In this way, relying on simulation results, it could be concluded that the proposed STATCOM based on a hybrid nine-level inverter is efficient and very suitable for real-time implementation.

The second part of the thesis work consisted of the hardware implementation. A conventional cascaded multilevel inverter has been implemented with the TEXAS INSTRUMENT F28335 EXPERIMENTER KIT for PWM generation. The operation of the inverter is done in such a way that only two switches are closed at any given time diagonally. To save the circuit from short-circuiting switching, technique is carefully worked out. More details on operation are provided in chapter five above.

In the second hardware implementation, the asymmetrical and symmetric inverters are performed. The designed inverter can operate as an asymmetrical inverter if it is fed by different DC sources at the same time. This inverter ensures the symmetric operation when it is supplied with equal inputs. So it represents two modules in the

same experiment kit. The reason behind the flexibility of operation comes from the dynamic and accuracy of the implemented code. The inverter circuit is composed of three H- bridges. The MOSFETs used here are IRFZ44N while the microcontroller is the Arduino Nano which is responsible for gate signal generation according to the injected software code.

The hardware implementation chapter discussed in detail the operation of the proposed multi-level inverters, the hardware results and the simulation indicate the achievement of the required outputs. A successful switching technique implementation as well as achieving a five-level output of the inverter are accomplished. Not only this, but standard equipment during the process of testing and assessment is also conducted. Moreover, the multiple levels of the output voltage stand behind enhancing the overall power efficiency.

6.2 Suggestions For Future Work

Concerning this thesis, suggestions and future work can be listed in the following points :

1-Relating to asymmetrical cascaded H-bridge inverter,anothor control technique can be used or anothor asymmetrical voltage distributions can be implemented.

2- Implementation of other hybrid inverters topologies which increase the output levels while decresing the inverter requirements.

3- Implementation of photovoltaic based STATCOM system (PV-STATCOM) so that the module is capable of injecting both active and reactive powers to the system through PCC.

4-Use the Neural Network (N.N) method to control the photovoltaic based STATCOM system (PV-STATCOM).

REFERENCES

[1] Islam, M., Mekhilef, S., Hasan M. (2015). Single Phase Transformer Less Inverter Topologies for Grid-Tied Photovoltaic System: A review, *Renewable and Sustainable Energy Reviews*.**45**, 69 – 86.

[2] Kadam, A., Shukla, A. (2017). A Multilevel Transformer Less Inverter Employing Ground Connection Between PV Negative Terminal and Grid Neutral Point, *IEEE Transactions on Industrial Electronics*. **64,**8897–8907.

[3] E. Romero-Cadaval, G. Spagnuolo, L. G. Franquelo, C. A. Ramos-Paja, T. (2013). Grid-Connected Photovoltaic Generation Plants: Components And Operation, *IEEE Industrial Electronics Magazine*.**7**, 6–20.

[4] Li, W., Gu, Y., Luo, H., Cui, W. (2015) Topology Review and Derivation Methodology of Single-Phase Transformer Less Photovoltaic Inverters for Leakage Current Suppression, *IEEE Transactions on Industrial Electronic*. **62**,4537–4551.

[5] Freddy, T. K. S., Rahim, N. A., Hew, Che, W. H. S. (2014). Comparison And Analysis Of Single-Phase Transformer Less Grid-Connected PV Inverters, *IEEE Transactions on Power Electronics*. **29**, 5358– 5369.

[6] Ramani, K., Krishnan, A.(2010). New Hybrid Multilevel Inverter Fed Induction Motor Drive-A Diagnostic Study, *International Review of Electrica Engineering*. **5(6)**,2562-2569.

[7] Patel, U., Sahu, M. D., Tirkey, D.(2013). Maximum Power Point Tracking Using Perturb & Observe Algorithm And Compare With Another Algorithm, *International Journal of Digital Application & Contemporary Research Conference*. **2**

[8] Sangwongwanich, A., Blaabjerg, F. (2019). Mitigation of Inter-harmonics in PV Systems With Maximum Power Point Tracking Modification, *IEEE Transactions On Power Electronics*. **34**,8279–8282.

[9] Karanayil, B., Ceballos, S., Pou, J. (2019). Maximum Power Point Controller for Large-Scale Photovoltaic Power Plants Using Central Inverters Under Partial Shading Conditions, *IEEE Transactions on Power Electronics*. **34.**

[10] Carrasco, J., de Quiros, F., Alaves, H., Navalon, M. (2019). An Analog Maximum Power Point Tracker with Pulse width Modulator Multiplication for a Solar Array Regulator, *IEEE Transactions on Power Electronics*. **34**, 8808-8815

[11] Hu, J., Joebgesn, P., Pasupuleti, G., Averous, N., De Doncker, R. (2019). A Maximum-Output-Power-Point-Tracking-Controlled Dual-Active Bridge Converter for Photovoltaic Energy Integration into MVDC Grids, *IEEE Transactions On Energy Conversion*. **34**, 170-180.

[12] Pachaivannan, N., Subburam, R., Ramkumar, U., Kasinathan, P. (2019). Crowded Plant Height Optimization Algorithm Tuned Maximum Power Point Tracking For Grid Integrated Solar Power Conditioning System, *IET Renewable Power Generation*. **13(12)**, 2137-2147.

[13] Selvakumar, S., Madhusmita, M., Koodalsamy, C., Simon, S., Sood, Y. (2019). High-Speed Maximum Power Point Tracking Module for PV Systems, *IEEE Transactions on Industrial Electronics*. **66**, 1119-1129.

[14] Nami, A., Zare, F., Ghosh, A., Blaabjerg, F. (2011). A Hybrid Cascade Converter Topology with Series-Connected Symmetrical and Asymmetrical Diode-Clamped H-Bridge Cells, *IEEE Transactions on Power Electronics*. ***26*(1)**, 51-65.

[15] Batschauer, A., Mussa, S., Heldwein, M. (2012). Three-Phase Hybrid Multilevel Inverter Based on Half-Bridge Modules, *IEEE Transactions on Industrial Electronics*. **59(2),** 668-678 2012.

[16] Gautam, S., Kumar, L., Gupta, S. (2018). Single-Phase Multilevel Inverter Topologies with Self-Voltage Balancing Capabilities, *IET Power Electronics*. **11(5)**, 844-855.

[17] Ye, M., Kang, L., Xiao, Y., Song, P., Li, S. (2018). Modified Hybrid Modulation Strategy with Power Balance Control For H-Bridge Hybrid Cascaded Seven-Level Inverter, *IET Power Electronics*. **11(6)**, 1046-1054.

[18] Yadav, A., Gopakumar, K. R. K., Umanand, L., Bhattacharya, S., Jarzyna, W. (2019). A Hybrid 7-Level Inverter Using Low-Voltage Devices and Operation with Single DC-Link, *IEEE Transactions on Power Electronics*. **34(10)**, 9844-9853.

[19] Wang, L., Lam, C., Wong, M. (2016). A Hybrid-STATCOM With Wide Compensation Range and Low DC-Link Voltage, *IEEE Transactions on Industrial Electronics*. **63(6),** 3333-3343.

[20] Zibanejad, S., Mehrizi-Sani, A. (2018). Design Tradeoffs in Selection of the DC-Side Voltage for a D-STATCOM, *IEEE Transactions On Power Delivery*. **33(6)**, 3230-3232.

[21] Varma, R., Siavashi, E. (2018). PV-STATCOM –A New Smart Inverter For Voltage Control In Distribution Systems, *IEEE Power & Energy Society General Meeting (PESGM*).

[22] Varma, R., Maleki, H. (2019). PV Solar System Control as STATCOM (PV-STATCOM) for Power Oscillation Damping, *IEEE Transactions on Sustainable Energy*. ***10*(4),** 1793-1803.

[23] Falahi, G., Huang, A. (2014). Low Voltage Ride Through Control of Modular Multilevel Converter Based HVDC Systems, *IECON 2014 – 40th Annual Conference of the IEEE Industrial Electronics Society*.

[24] Kumar, N., Saha, T. K., Dey, J. (2016). Sliding-Mode Control of PWM Dual Inverter-Based Grid-Connected PV System: Modeling and performance analysis, *IEEE Journal of Emerging and Selected Topics in Power Electronics.***4(2)**.

[25] Ghafouri, A., Zolghadri, M., Ehsan, M. (2007). Power System Stability Improvement Using Self-Tuning Fuzzy Logic Controlled STATCOM, *EUROCON 2007–The International Conference on Computer as a Tool*.4400598.

[26] Rathod, U. K., Modi, B. (2017). Simulation and Analysis of Various Configuration of MMC For New Generation STATCOM, *8th International Conference on Computing, Communication and Networking Technologies (ICCCNT)*.8203944.

[27] Chavan, P. M., Chavan, G. P. (2017). Interfacing of Hybrid Power System to Grid Using STATCOM & Power Quality Improvement, *2017 International Conference on Information, Communication, Instrumentation and Control (ICICIC)*.8279079.

[28] Jeon, Y., Farivar, G., Townsend, C. D., Park, J., Pou, J. (2018). Capacitor Voltage Shaper for Cascaded H-Bridge STATCOM, *2018 IEEE 4th Southern Power Electronics Conference (SPEC)*.8635915.

[29] Dusmez, S., Li, X., Akin, B. (2016). A New Multi-Input Three-Level DC/DC Converter, *IEEE Transactions on Power Electronics*. **31(2),** 1230-1240.

[30] Faraj, K. S., Hussein, J. F. (2020). Analysis and Comparison of DC-DC Boost Converter and Interleaved DC-DC Boost Converter, *Engineering and Technology Journal*.**38(5A)**, 622–635.

[31] Lee, J.Y. (2014). Low-area Dual mode DC-DC Buck Converter with IC Protection Circuit, *Journal of IKEEE*.***18*(4),** 586–592.

[32] Banaei, M. R., Ajdar, F. B. (2017). High-Efficiency Transformerless Buck-Boost DC-DC Converter, *International Journal of Circuit Theory and Applications*.***45*(8),** 1129–1150.

[33] Almalaq, Y., Alateeq, A., Matin, M. (2017). Non-Isolated High Gain Switched Inductor DC-DC Multilevel Cuk Converter For Photovoltaic Applications, *2017 North American Power Symposium (NAPS)*.

[34] Belkaid, A., Gaubert, J. P., Gherbi, A., Rahmani, L. (2014). Maximum Power Point Tracking For Photovoltaic Systems With Boost Converter Sliding Mode Control, *IEEE 23rd International Symposium on Industrial Electronics*. 556-561.

[35] Nedumgatt, J. J., Jayakrishnan, K. B., Umashankar, S., Vijayakumar, D., Kothari, D. P. (2011). Perturb And Observe MPPT Algorithm For Solar PV Systems-Modeling And Simulation, *2011 Annual IEEE India Conference*.

[36] Lakshmi, G. S. (2018). Performance Analysis of Multi-Level Diode-Clamped Inverter Fed IPMSM Drive for Electric Vehicles, *2018 IEEE Innovative Smart Grid Technologies – Asia (ISGT Asia*. 54-61, 84678202018.

[37] Pawar, N., Kumar Tayal, V., Choudekar, P. (2020). Design of Flying Capacitor Multilevel Inverter for Solar Energy Applications. *E3S Web of Conferences*. *184*, 01035.

[38] Bhattacharya, S., Mascarella, D., Joos, G. (2013). Modular Multilevel Inverter: A Study For Automotive Applications, *2013 26th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE).*

[39] Babaei, E., Laali, S., Alilu, S. (2014). Cascaded Multilevel Inverter With Series Connection of Novel H-Bridge Basic Units, *IEEE Transactions on Industrial Electronics*. **61(12),** 6664-6671.

[40] Ding, K., Cheng, K. W. E., Zou, Y. P. (2012). Analysis of An Asymmetric Modulation Method For Cascaded Multilevel Inverters, *IET Power Electronics*. **5(1)**, 74-85.

[41] Vijayarajan, P., Shunmugalatha, A., Sathik, M. A. (2017). A New Hybrid Multilevel Inverter Topology for Medium and High Voltage Applications, *Applied Mathematics & Information Sciences*. **11(2)**, 497-508.

[42] D.Mohan, D. M., B.Kurub, S. (2012). A Comparative Analysis of Multi Carrier SPWM Control Strategies using Fifteen Level Cascaded H bridge Multilevel Inverter, *International Journal of Computer Applications*.***41*(21),**7–11.

[43] Kouzou, A., Mahmoudi, M.O., Boucherit, M.S. (2011). The Space Vector Modulation PWM Control Methods Applied On Four Leg Inverters, *Electric Machines and Drives*.

[44] Du, Z., Tolbert, L. M., Ozpineci, B., Chiasson, J. N. (2009). Fundamental Frequency Switching Strategies of a Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter, *IEEE Transactions on Power Electronics*. ***24*(1)**, 25-33.

[45] Babaei, E. (2011). Charge Balance Control Methods for a Class of Fundamental Frequency Modulated Asymmetric Cascaded Multilevel Inverters, *Journal of Power Electronics*. **11(6)**, 811-818.

[46] Yu, Y., Konstantinou, G., Hredzak, B., Agelidis, V. G. (2015). Power Balance Optimization of Cascaded H-Bridge Multilevel Converters for Large-Scale Photovoltaic Integration, *IEEE Trans. Power Electron.* **31(2)**, 1108–1120.

[47] Augusto, C., Kommers, T., Brunelli, A. Ruiz-Caballero, D., Astudillo, R., Martinez, L., Ahmad Mussa, S. (2019). Asymetrical Multilevel Hybrid Inverter - Analysis And Experimentation, *Eletrônica de Potência*. **24(3),** 296–305.

[48] Hossain, M. K., Ali, M. H. (2014). Low Voltage Ride Through Capability Enhancement Of Grid Connected PV System By SDBR, *IEEE PES T&D Conference and Exposition*.

[49] Kouro, S., Leon, J. I., Vinnikov, D., Franquelo, L. G. (2015). Grid-Connected Photovoltaic Systems: An Overview of Recent Research and Emerging PV Converter Technology, *IEEE Industrial Electronics Magazine*. ***9*(1),** 47-61.

[50] Agelidis, V., Baker, D., Lawrance, W., Nayar, C. (1997). A Multilevel PWM Inverter Topology For Photovoltaic Applications, *ISIE '97 Proceeding of the IEEE International Symposium on Industrial Electronics*. **2**, 589-594.

[51] Eid, B. M., Rahim, N. A., Selvaraj, J., Williams, B. W. (2016). Electronically Coupled Distributed Generation Modeling and Control Strategies for Microgrid Applications, *Appl. Math. Inf. Sci.* **10**(4), 1343–1353.

[52] Jaalam, N., Rahim, N., Bakar, A., Eid, B. (2017) Strategy to Enhance the Low-Voltage Ride-Through in Photovoltaic System During Multi-Mode Transition, *Sol. Energy*. **153**, 744–754.

[53] Tafti, H. D., Maswood, A. I., Konstantinou, G., Pou, J., Acuna, P. (2018). Active/Reactive Power Control of Photovoltaic Grid Tied Inverters With Peak Current Limitation And Zero Active Power Oscillation During Unbalanced Voltage Sags, *IET Power Electron.***11(6)**, 1066–1073.

[54] Antoniadou-Plytaria, K.E. (2017). Distributed and Decentralized Voltage Control of Smart Distribution Networks: Models, Methods, And Future Research, *IEEE Trans. Smart Grid*. **8 (6),** 2999–3008.

[55] Mehrizi-Sani, A. (2017). Distributed Control Techniques in Microgrids, *Microgrid Adv. Control Methods Renew. Energy Syst. Integr.*, **5 (6)**, 43–62.

[56] Alskran, F.A., Simoes, M. (2020). Multilevel Current Source Converter-Based STATCOM Suitable For Medium-Voltage Applications, *IEEE Trans. Power Deliv.* 89**77**,1–1.

[57] Lam, C.S. (2012). Adaptive DC-Link Voltage-Controlled Hybrid Active Power Filters For Reactive Power Compensation, *IEEE Trans. Power Electron*. **27(4),**1758– 1772.

[58] Tripathi, A., Narayanan, G. (2017). Investigations On Optimal Pulse Width Modulation To Minimize Total Harmonic Distortion In The Line Current, *IEEE Trans. Ind. Appl*. **53 (1**), 212–221.

[59] Joos, G. (1991). Performance Analysis of a PWM Inverter VA Compensator, *IEEE Trans. Power Electron.* **6(3)**,380–391.

[60] Chen, B.S., Hsu, Y.Y.(2008). A Minimal Harmonic Controller For A STATCOM, *IEEE Trans. Ind. Electron*. **55 (2),**655–664.

[61] Behrouzian, E. (2016). Impact of Switching Harmonics on Capacitor Cells Balancing in Phase-Shifted PWM-Based Cascaded H-Bridge STATCOM, *IEEE Trans. Power Electron*. **32 (1),**815–824.

[62] Graydon, I. (2006). Adaptive Controller For Statcom To Enhance Voltage Stability, *United States Patent*.**1**,24.

[63] Gupta, S., Tripathi, R.K.(2014). Improved Performance Of LQR Controller In CSC Based STATCOM Using Genetic Optimization, Proc. *6th IEEE Power India Int. Conf. PIICON*,**1**–6.

[64] Comparatore, L.(2017). Model Based Predictive Control With Switcher Of Redundant Vectors For A Cascade H-Bridge Multilevel STATCOM, *Proc. 2016 IEEE ANDESCON, ANDESCON*.16–19.

[65] Yonglei, Z., Xiaojie, Wu., Xibo, Yuan., Yingjie, W., Peng D. (2016). Fast Model Predictive Control for Multilevel Cascaded H-Bridge STATCOM With Polynomial Computation Time, *IEEE Trans. Ind. Electron.* **63** (8), 5231–5240.

[66] Biswal, B. (2009). Power Quality Disturbance Classification Using Fuzzy C-Means Algorithm and Adaptive Particle Swarm Optimization, *IEEE Trans. Ind. Electron.* **56 (1),** 212–220.

[67] Liu, C. (2010). Design of a Self-Tuning PI Controller for a STATCOM Using Particle Swarm Optimization,**57(2),**702–715.

[68] Jerez, J.L. (2014). Embedded Online Optimization for Model Predictive Control at Megahertz Rates, *IEEE Trans. Automat. Contr*.**59(12),**3238–3251.

[69] Song, B.M. (2001). A Multilevel Soft-Switching Inverter With Inductor Coupling, *IEEE Trans. Ind. Appl*. **37(2)**,628–636.

[70] Naik, B.S. (2017). Design And Implementation Of A Symmetrical Multilevel InverterTopology ,Proc. Int. Conf. Inven. Syst. *Control. ICISC 2017*. **59 (11),** 4148–4154.

[71] Esa, M., Moiz, S.A.(2019). Study and Simulation of Seven Level-Ten Switch Inverter Topology, *Int. J. Res*. **111 (1),**798–803.

[72] Camargo, R.S. (2020). A Novel Cascaded Multilevel Converter Topology Based on Three-Phase Cells with Model Predictive Control, *IEEE Int. Symp. Ind. Electron.*1161–1166.

[73] Shyaa, S.S., Hassan, P.R.F.(2020). STATCOM Based on Diode Clamped Multilevel Converter Using Phase Shift PWM Control Strategy,**62(03),**785-795.

[74] Felix, S., amp, I. Jacob, D. (2018). Voltage Regulation Using STATCOM with PI and Adaptive PI Controls. *International Journal of Engineering & Technology*, **7(3.1)**, 178.

[75] Maurya, D.S. (2020). A Detailed Comparative Analysis of Different Multipulse and Multilevel Topologies for STATCOM, (*Icesc*).1112–1117.

[76] Kadu, A. (2020). Reduced Switch Multilevel Inverter based STATCOM. *International Journal for Modern Trends in Science and Technology*, ***6*(5)**, 117–121.

[77] Manjrekar, M., Lipo, T. (1998). Hybrid Multilevel Inverter Topology For Drive Applications, *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. APEC*. **2**,523–529.

[78] Paital, S.R. (2017). Bacterial Foraging Optimized STATCOM For Stability Assessment In Power System, *2016 IEEE Students' Technol. Symp. TechSy, (TechSym)*. 85–89.

[79] Farokhnia, N. (2010). Optimization Of PI Controller Gains In Nonlinear Controller Of STATCOM Using PSO And GA, *Renew. Energy Power Qual.* **1(8),** 180–185.

[80] Daryabeigi, E.(2014). Electrical Power and Energy Systems Calculation of optimal induction heater capacitance based on the smart bacterial foraging algorithm, *Int. J. Electr. Power Energy Syst*.**61**,326–334.

[81] Coley, D.A.(1999). An Introduction to Genetic Algorithms for Scientists and Engineers.

[82] Golkar, M.A., Zarringhalami, M. (2009). Coordinated Design of PSS and STATCOM Parameters for Power System Stability Improvement Using Genetic Algorithm, *Iran. J. Electr. Comput. Eng*. **8 (2),**80–88.

[83] Hasanien, H.M. (2013). Design Optimization Of PID Controller In Automatic Voltage Regulator System Using Taguchi Combined Genetic Algorithm Method, *IEEE Syst. J.*, **7 (4)**, p. 825–831.

[84] Kamel, O.M. et al. (2020). A Novel Hybrid Ant Colony-Particle Swarm Optimization Techniques Based Tuning STATCOM for Grid Code Compliance. *IEEE Access*, **8**, p. 41566–41587.

[85] Paital, S.R. et al. (2017). Bacterial Foraging Optimized STATCOM For Stability Assessment In Power System, *2016 IEEE Students' Technol. Symp. TechSym 2016*, (TechSym). 85–89.

[86] Farokhnia, N. et al. (2010). Optimization Of PI Controller Gains In Nonlinear Controller Of STATCOM Using PSO And GA, *Renew. Energy Power Qual. J.*, **1** (8), p. 180–185.

APPENDIX A

Parameter	Value
PCC voltage (L-L)	15 Kv
System frequency	60 Hz
DC capacitor value	11μf
capacitor voltage value	204 V
Filter inductance L *f*	4mH
Filter resistor R *f*	2 Ω
Number of switches per phase	12
Active power (P)	5 Kw

APPENDIX B

```
clear all;
close all;
clc;
% Define the details of the table design problem
ub = [1000 2000 ];
lb =[10  200];
fun = @(x)myobjfunc(x);
noP = 20;
maxIter=50;
nvars = 2;
options =
optimoptions('particleswarm','SwarmSize',noP,'HybridFcn',@fmincon,'MaxIterations
',maxIter,'PlotFcn','pswplotbestf','Display','iter');
[xbest,fval,exitflag,output] = particleswarm(fun,nvars,lb,ub,options);
xbest
output
sim('my_statcom.slx');
```

APPENDIX C

```
clc;clear;close all;

n_variables=2;

LB=[10  200];% The lower bound of the chromosomes

UB=[2000 2000 ]; % The upper bound of the chromosomes

fobj = @(x)myobjfunc(x);

generation=15;  % Maximum Number of Iterations

population_size= 30; % Population size

population=zeros(population_size,n_variables); % Initializing the size of the
population

temp_population=zeros(population_size,n_variables); % Intializing the size of the
temporary population

mu=0.1; % muitation rate

S_population= zeros (population_size,n_variables+1);% Initializing the size of the
sorted population using the problem objective function

F= zeros(population_size,1);% initializing the size of the objective function based on
the population size

crossover_times=4;% number of crossovers

mutation_times=5; % number of mutations

for i=1:1:population_size

    for n=1:1:n_variables

    population(i,n)= unifrnd(LB(1,n),UB(1,n));

    end

 F(i)= fobj(population(i,:));

 end
```

```
% sorting of the population
 S_population(:,1:n_variables)= population(:,:);
 S_population(:,n_variables+1)=F;
 S_population= sortrows(S_population,n_variables+1);

% Generation
for ii=1:1:generation
    k=1;% This is used to initialize the location of the temp_population;

%Elitism
temp_population(k,1:n_variables)=S_population(1,1:n_variables);
k=k+1;
% Selection and Crossover
for j=1:1:crossover_times
% parent selection
    y1(j) = geornd(0.1)+1;
    while   y1(j)> population_size
            y1(j) = geornd(0.1)+1;
    end
    y2(j) = geornd(0.1)+1;
    while   y2(j)> population_size
            y2(j) = geornd(0.1)+1;
    end
end
for u=1:1:crossover_times
parent1= S_population(y1(u),1:n_variables);
parent2= S_population(y2(u),1:n_variables);
```

```
% arithmetic crossover
[Children]= arithmetic_crossover (parent1, parent2);
temp_population(k,1:n_variables)=Children(1,:);

temp_population(k,1:n_variables)=max(temp_population(k,1:n_variables),LB);
temp_population(k,1:n_variables)=min(temp_population(k,1:n_variables),UB);
k=k+1;
temp_population(k,1:n_variables)=Children(2,:);
temp_population(k,1:n_variables)=max(temp_population(k,1:n_variables),LB);
temp_population(k,1:n_variables)=min(temp_population(k,1:n_variables),UB);
k=k+1;
end
% Mutation
for e=1:1:mutation_times
   parent=S_population(unidrnd(population_size),1:n_variables);
   [child]= gene_mutation (parent,mu,LB,UB);
   temp_population(k,1:n_variables)=child;
   temp_population(k,1:n_variables)=max(temp_population(k,1:n_variables),LB);
   temp_population(k,1:n_variables)=min(temp_population(k,1:n_variables),UB
   k=k+1;
end
% Replication
for k=k:1:population_size
replicated_child=S_population(randi([1 population_size]),1:n_variables);
temp_population(k,1:n_variables)=replicated_child;
k=k+1;
end
```

```
% Calculating the temporary population objective function values
for iii=1:1:population_size
F(iii)= fobj(temp_population(iii,:));
end
% sorting for the next generation and selection of the population best
S_population(:,1:n_variables)= temp_population;
S_population(:,n_variables+1)=F(:,:);
S_population= sortrows(S_population,n_variables+1);

Best_F(ii)= S_population(1,n_variables+1);
end
figure(1)
plot(Best_F,'b');
pause(0.1)
xlabel('Generation')
ylabel('Best Value')
grid on
Xmin=S_population(1,1:n_variables)
Fval=Best_F(1,generation)
sim('my_statcom.slx');
```

APPENDIX D

```
float f=50;
float t=(1/f)*1000000;
float a1=10;
float a2=30;
float a3=60;
float alp1=a1*t/360;
float alp2=a2*t/360;
float alp3=a3*t/360;
float d=5+15;
int pin1=2;
int pin2=3;
int pin3=4;
int pin4=5;
int pin5=6;
int pin6=7;
int pin7=8;
int pin8=9;
int pin9=10;
int pin10=11;
int pin11=12;
int pin12=13;
14
void setup() {
```

```
 pinMode(pin1, OUTPUT);
 pinMode(pin2, OUTPUT);
 pinMode(pin3, OUTPUT);
 pinMode(pin4, OUTPUT);
 pinMode(pin5, OUTPUT);
 pinMode(pin6, OUTPUT);
 pinMode(pin7, OUTPUT);
 pinMode(pin8, OUTPUT);
 pinMode(pin9, OUTPUT);
 pinMode(pin10, OUTPUT);
 pinMode(pin11, OUTPUT);
 pinMode(pin12, OUTPUT);
}
void loop() {
 digitalWrite(pin1,HIGH);
 digitalWrite(pin2,HIGH);
 digitalWrite(pin5,HIGH);
 digitalWrite(pin6,HIGH);
 digitalWrite(pin9,HIGH);
 digitalWrite(pin10,HIGH);
 delayMicroseconds(alp1-d);
15
 digitalWrite(pin2,LOW);
 delayMicroseconds(d);
 digitalWrite(pin4,HIGH);
 delayMicroseconds(alp2-alp1-d);
```

```
digitalWrite(pin6,LOW);
delayMicroseconds(d);
digitalWrite(pin8,HIGH);
delayMicroseconds(alp3-alp2-d);
digitalWrite(pin10,LOW);
delayMicroseconds(d);
digitalWrite(pin12,HIGH);
delayMicroseconds(t/2-(2*alp3)-d);
digitalWrite(pin9,LOW);
delayMicroseconds(d);
digitalWrite(pin11,HIGH);
delayMicroseconds(alp3-alp2-d);
digitalWrite(pin5,LOW);
delayMicroseconds(d);
digitalWrite(pin7,HIGH);
delayMicroseconds(alp2-alp1-d);
16
digitalWrite(pin1,LOW);
delayMicroseconds(d);
digitalWrite(pin3,HIGH);
delayMicroseconds((2*alp1)-d);
digitalWrite(pin4,LOW);
delayMicroseconds(d);
digitalWrite(pin2,HIGH);
delayMicroseconds(alp2-alp1-d);
digitalWrite(pin8,LOW);
delayMicroseconds(d);
```

```
 digitalWrite(pin2,HIGH);
 delayMicroseconds(alp2-alp1-d);
//--
 digitalWrite(pin8,LOW);
 delayMicroseconds(d);
 digitalWrite(pin6,HIGH);
 delayMicroseconds(alp3-alp2-d);
 digitalWrite(pin12,LOW);
 delayMicroseconds(d);
 digitalWrite(pin10,HIGH);
 delayMicroseconds(t/2-(2*alp3-d));
17
 digitalWrite(pin11,LOW);
 delayMicroseconds(d);
 digitalWrite(pin9,HIGH);
 delayMicroseconds(alp3-alp2-d);
 digitalWrite(pin7,LOW);
 delayMicroseconds(d);
 digitalWrite(pin5,HIGH);
 delayMicroseconds(alp2-alp1-d);
 digitalWrite(pin3,LOW);
 delayMicroseconds(d);
 digitalWrite(pin1,HIGH);
 delayMicroseconds(alp1);
}
```

APPENDIX E

```
volatile uint8_t LevelIndex = 0;
volatile uint8_t HBridgeIndex = 0;
const uint8_t LevelArr[10] = {
  0B10101010, // 0 VDC
  0B01101010, // 1 VDC
  0B00011010, // 2 VDC
  0B00000110, // 3 VDC
  0B00000001, // 4 VDC
  0B00000001, // 4 VDC
  0B00000110, // 3 VDC
  0B00011010, // 2 VDC
  0B01101010, // 1 VDC
  0B10101010, // 0 VDC
};
const uint8_t HBridgeArr[] = {
  0B00111001,
  0B00110110
};

void setup() {
  LevelCtr_PORT = 0x00; // all OFF
  LevelCtr_DDR  = 0xFF; // all Output
  HBridge_PORT  = 0x30; // Pull-up Enable Btn 1 & 2
```

```
  HBridge_DDR   = 0x0F; // Output 0..3
  // turn ADC on
  ADCSRA = (1 << ADEN) | (1 << ADIE) | (1 << ADIF) | (1 << ADPS0) | (1 << ADPS1) | (1 << ADPS2);  // Prescaler of 128, Interrupt Enable
  //    ADCSRB = (1 << ADTS1); // ADC Auto Trigger (Timer 1 overflow)
  ADMUX  = ADC_Channels_MapReg[ADC_Channel];
  SetTimer();
}
void loop() {
}
void SetTimer() {
  cli(); // disable global interrupts
  TCNT1  = 0x00;
  TCCR1A = 0x00;
  TCCR1B = (1 << WGM12) | (1 << CS11) | (1 << CS10); // clock on, Prescaler 64 & CTC Mode
  OCR1A  = 250;
  TIMSK |= (1 << OCIE1A);
  sei();// enable global interrupts
}
ISR(TIMER1_COMPA_vect) {
  if (powerFlag) {
    LevelCtr_PORT = 0x00;
    delayMicroseconds(2); // 2uS delay
    LevelCtr_PORT = LevelArr[LevelIndex];

    //OCR1A = LevelTimeArr[LevelIndex];
    if (++LevelIndex >= 10) {
```

```
      LevelIndex = 0;
      HBridge_PORT = 0B00110000;
      delayMicroseconds(2); // 2uS delay
      HBridge_PORT = HBridgeArr[HBridgeIndex];
      ++HBridgeIndex &= 0x01;
    }
  }
  ADCSRA |= (1 << ADSC); // ADC Start Conversion
}
```

CURRICULUM VITAE

PERSONAL INFORMATION

Name and Surname: OMAR KANAAN NOORI ALBASRI

Foreign Language **:**English//Turkish

EDUCATION

	Graduate School	Year
Master	Electric and electronic Engineering Department, College of Engineering, Gaziantep University–Turkey	2017
Bachelor	Electric and electronic Engineering, College of Engineering, Al-Mustansiriya University – IRAQ	2006

PUBLICATIONS

1. Development of Cascade H-Bridge Multi-level Inverter for photovoltaic Panels. (2016).
2. New Topology Of Asymmetrical Cascade H-Bridge Multi-Level INVERTER(2018).
3. Hybrid Multi-Level Inverter Based Photovoltaic Application (2019).
4. Multilevel Cascaded Three Phase Inverter With Low Voltage Ride Through Flexible Control Capability For Photovoltaic Systems (2020)