

**A TWO STAGE X-BAND LOW NOISE
AMPLIFIER OPTIMIZED FOR MINIMUM
NOISE APPLICATION**

A THESIS

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MASTER OF SCIENCE

By

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ABSTRACT

A TWO STAGE X-BAND LOW NOISE AMPLIFIER OPTIMIZED FOR MINIMUM NOISE APPLICATION

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Low Noise Amplifiers (LNA) are used as the first stage of any radio frequency receiver or any sensitive application requiring detection of very small signals with the minimum possible additional noise in order to get maximum signal-to-noise ratio at the output which also provide large enough gain to supersede the noise added by the following stages.

An X-Band two stage low noise amplifier operating in the 8.2-8.4 GHz frequency band with active bias network by using microstrip technology is studied. The first stage of the LNA is designed to minimize the noise figure and the second stage of the amplifier is designed to obtain the necessary gain. The input match is optimized for better noise figure and to obtain reasonable input coupling. Total gain is kept above a certain value in order not to degrade the total noise figure of the whole cascaded system. Stability is obtained without sacrificing the in-band gain. Agilent's ADS tool is used to simulate and Altium Designer tool is used for PCB design. The measurement results are compared with simulation results and the comparison shows good agreement.

Keywords: Low Noise Amplifier, LNA, Noise Figure.

ÖZET

MİNİMUM GÜRÜLTÜ UYGULAMALARI İÇİN OPTİMİZE EDİLMİŞ İKİ KATLI X-BANT DÜŞÜK GÜRÜLTÜLÜ GÜÇ YÜKSELTECİ UYGULAMASI

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Düşük gürültülü güç yükselteç genellikle radyo frekans alıcılarının antenden sonraki ilk kısımları olur. Bu yükselteçlerin amacı antenden gelen sinyalin gürültü seviyesine olabildiğince az gürültü ekleyerek alıcıların bir sonraki kısmına sinyalin güç seviyesini yükselterek vermektir.

İki katlı düşük gürültülü güç yükselteç, 8.2 -8.4 GHz frekans bandında mikrostrip teknoloji kullanılarak tasarlanmıştır. Tasarımın ilk katı gürültü figürü en düşük olacak şekilde tasarlanırken, ikinci katı ise kazancı arttırmak için tasarlanmıştır. Simülasyonlar Agilent'in ADS programı ile tasarlanırken, PCB tasarımı ise Altium Designer programında yapılmıştır.

Anahtar sözcükler: Düşük Gürültülü Yükselteç, Gürültü Figürü.

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Chapter 1

Introduction

A Low Noise Amplifier (LNA) is a crucial component of any radio frequency receiver to effectively amplify weak signals received and to maximize the signal-to-noise ratio. In cascaded systems, as the noise figure of the first stage dominates the noise figure of a properly designed amplifier, low noise amplifier has a crucial role in RF receivers. Also, power gain can be defined as the small signal amplification capability of LNA. As the maximum power gain and the minimum noise figure cannot be obtained simultaneously, a trade-off between the two parameters is needed. [1] To reach optimal values and to satisfy the requirements, gain and noise circles on Smith chart should be used. While designing the input and output matchings in the trade-off between minimum noise figure and maximum gain, the choice of source and load impedances, the location of the input and output stability circles should also be considered. [2]

Low Noise Amplifier (LNA) design considerations are low noise figure, good input and output matching, high gain, stability and linearity. Although these considerations are crucial, they are interdependent and to find a common optimum solution is not easy. To satisfy these considerations, transistor selection is one of the most important step in LNA design.

X-Band covers the frequency range of electromagnetic waves between approximately 8 GHz and 12 GHz. In this thesis, an X-Band LNA operating in the

frequency band 8.2-8.4 GHz is studied. Most known applications in these frequencies are satellite communications, radar, motion detectors and aerospace communications.

The basic component of the LNA is the transistor that can work in desired frequency. GaAs HEMTs transistors are especially suitable for low noise amplifiers because of their lower noise figure. One of such amplifier transistors is the Gallium-arsenide high electron mobility transistor (GaAs HEMT) which is a hetero junction FET. It is constructed with several layers of compound semiconductor materials. [2]

In this thesis, an X-Band low noise amplifier is designed at 8.2-8.4 GHz frequency band. The transistor used is X to Ku band super low noise transistor which is an HJ-FET transistor (NE3511S02) manufactured by NEC Technologies. Substrate used is RO4003 Rogers material with $\epsilon_r = 3.38$, substrate thickness $H=0.508$ mm, and metal thickness $t=0.035$ mm. The design contains matching networks and standard lumped elements for the active bias network based on SMBT2907A and Panasonic thick film chip resistors. The two stage LNA achieves a noise figure of 1.42 dB and a power gain of 22.20 dB.

Chapter 2

Background

2.1 Low Noise Amplifier Definition

Low Noise Amplifiers (LNA) are the RF front-end devices of a radio receiver circuit which are located close to the antenna. The main purpose of a low noise amplifier is to amplify the signal with minimum additional noise. Low Noise Amplifier (LNA) design considerations are low noise figure, good input and output matching, high gain, stability and linearity. The crucial criteria are operating bandwidth, a low NF, a large enough gain, gain flatness, stability, VSWR and large enough intermodulation and compression points.

2.1.1 LNA Topologies

There are three well known topology structures found in the literature. They are common-source, common-gate and cascode topologies. Below, they are briefly explained.

2.1.1.1 Common-Source Amplifier

Common-source amplifiers are the most widely used as good voltage and transconductance amplifiers. They have large voltage gain, high input resistance and medium / high output resistance. The signal enters the gate and leaves the drain in this type of amplifier in Figure 2.1. Due to Miller effect, the bandwidth of the amplifier tends to be low. [3]

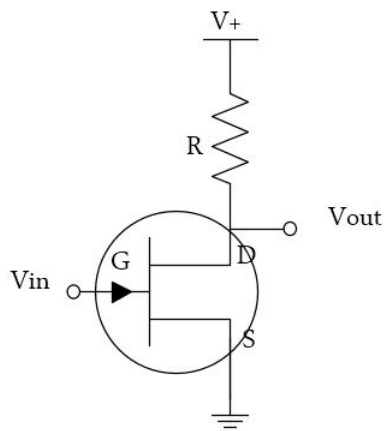


Figure 2.1: Common source amplifier

2.1.1.2 Common-Gate Amplifier

In common-gate amplifier topology, input signal is applied to the source and output is taken from the drain as shown in Figure 2.2. Common-gate amplifier is a good voltage amplifier and transconductance amplifier. It has large voltage gain and medium / high output resistance. Common-gate low noise amplifiers achieve a broadband impedance match, superior reverse isolation and stability due to the absence of the Miller effect, and a high linearity. Common gate feedback amplifiers aim at decoupling the noise and power (input) match trade-off without degrading other relevant LNA parameters. [3]

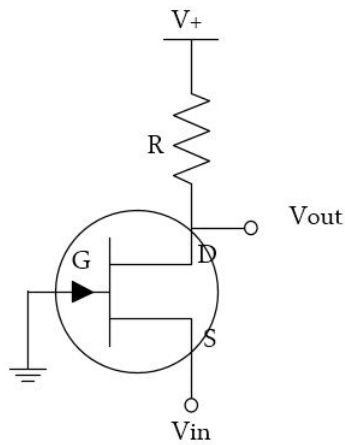


Figure 2.2: Common gate amplifier

2.1.1.3 Cascode Amplifier

This topology which is shown in Figure 2.3 improves the voltage gain of the LNA and the output impedance while providing shielding as well, input and output isolation. When designing low noise amplifier, cascode stage is added to decrease the variation in the capacitance seen by the transmission lines which is caused by Miller effect. [4] Also, because the Miller effect is eliminated, much higher bandwidth can be contributed. This type amplifier has higher input-output isolation from the signal obtained on the drain line coupling back to the gate, higher input impedance, high output impedance, higher gain and higher bandwidth. [3]

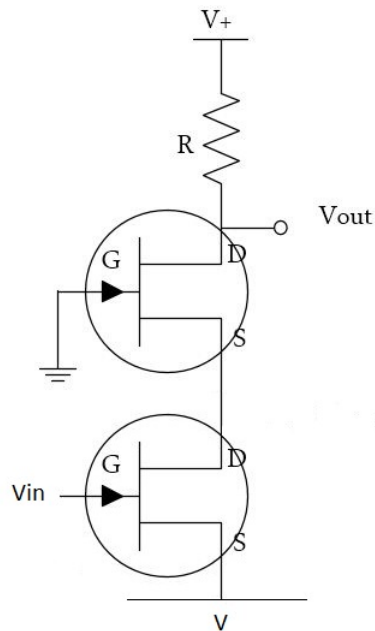


Figure 2.3: Cascode amplifier

2.2 Requirements of the LNA Design

An LNA design is changeable with respect to design objective because of its simultaneous requirement for low noise figure, high gain, good input and output matching, unconditional stability, linearity etc. Even though all are equally important, they are interdependent and LNA design has performance trade-offs as any other design process. These considerations and parameters are introduced in this part of the thesis.

In this thesis, the goal is to obtain the minimum noise figure. Minimum noise figure can be obtained from a given device by using the optimum source impedance. The source impedance that minimizes the noise figure generally differs, perhaps considerably, from that which maximizes the power gain. Hence, it is possible for poor gain and a bad input match to accompany a good noise figure. [5]

2.2.1 Noise Figure and Noise Considerations

At high frequencies, the noise input is dominated by the thermal noise. In equation 2.1, the available noise power to the matched load is illustrated. [1]

$$P_N = kTB \quad (2.1)$$

where, k is the Boltzmann's constant, T is the resistor's physical temperature in Kelvin and B is the two-port network's noise bandwidth.

Noise factor, F , which is defined in equation 2.2 is a measure of the reduction in the signal to noise ratio between the input and the output of the component. [2] The noise figure, NF , which is defined in equation 2.3 is one of the most important challenges of the LNA design. By increasing the signal or reducing noise of the system, overall signal-to-noise ratio (SNR) of the system can be optimized. Because the output noise is larger than input noise of the system multiplied by the gain, input SNR is larger than output SNR; therefore, F is always bigger than one or NF being greater than 0 dB.

$$F = \frac{P_{Si}/P_{Ni}}{P_{So}/P_{No}} \quad (2.2)$$

$$\text{Noise Figure} = 10 \log_{10} F = NF(\text{dB}) \quad (2.3)$$

$$P_{Ni} = kT_0B \quad (2.4)$$

where,

P_{Si} = available signal power at the input

P_{So} = available signal power at the output

P_{Ni} = input noise power

P_{No} = output noise power

Any type of noise has a power spectrum, if the noise power spectrum is not a strong function of a frequency, it can be modelled as an equivalent thermal noise temperature, T_e . [1]

$$T_e = \frac{P_n}{G_A k B} \quad (2.5)$$

where T_e is the equivalent noise temperature of the amplifier, P_n is amplifier's generated noise power and G_A is the available power gain of the amplifier. Both amplifier and source resistor creates the combined equivalent noise temperature, T'_e .

$$T'_e = T_e + T_S \quad (2.6)$$

$$P_{No} = G_A P_{Ni} + P_n = G_A k B (T_S + T_e) = G_A k B T'_e \quad (2.7)$$

In equation 2.7, P_{Ni} is the noise power at the input terminals of the amplifier and P_{No} is the total output noise power. [1]

$$P_{No} = F P_{Ni} = F k T_0 B = k B (T_e + T_0) \Rightarrow F T_0 = T_e + T_0 \Rightarrow T_e = (F - 1) T_0 \quad (2.8)$$

From equation 2.2;

$$P_{No} = P_{Ni} F G = k T_0 B F G = \underbrace{(F - 1) k T_0 B G}_{\text{added noise}} + \underbrace{k T_0 B G}_{\text{input noise}} \quad (2.9)$$

In a cascaded system, if noise figure of each stages is known, noise figure of the whole system can be determined. Generally, the first stage of the system is the crucial one for the noise performance of the total system.

Noise factor, F , which is expressed as equation 2.2 is a measure of the reduction in the signal to noise ratio between input and output of the component. [2] The noise figure (NF) is the one of the most important challenges of the LNA design.

$$P_{No1} = G_{A1} k B (T_0 + T_{e1}) \quad (2.10)$$

$$P_{No2} = G_{A2} P_{No1} + G_{A2} k T_{e2} B = G_{A1} G_{A2} k B (T_0 + T_{e1} + T_{e2}/G_{A1}) \quad (2.11)$$

$$P_{No} = G_A k B (T_0 + T_e) \quad (2.12)$$

$$F = 1 + T_e/T_0 = 1 + (T_{e1} + T_{e2}/G_{A1})/T_0 \quad (2.13)$$

For the n-stage cascaded system, from the Friis Formula,

$$T_{e,cas} = T_{e1} + \frac{T_{e2}}{G_{A1}} + \frac{T_{e3}}{G_{A1} G_{A2}} + \dots + \frac{T_{en}}{G_{A1} G_{A2} \dots G_{An-1}} \quad (2.14)$$

where, $T_{e,cas}$ is the equivalent temperature of the cascaded system, T_{e1} , T_{e2} until T_{en} and G_{A1} , G_{A2} until G_{An-1} are the equivalent temperature and the gains of the respective stages of the system.

2.2.2 Stability

One of the crucial considerations of the amplifier design is the stability which is the ability of an amplifier to maintain effectiveness in its nominal operating characteristics despite any large changes in the any conditions. [1]

In terms of the reflection coefficients, in a two port network, if one of the input reflection coefficient, Γ_{IN} , or output reflection coefficient, Γ_{OUT} , are less than unity then it does not oscillate for some values of source or load impedance. [6]

$$|\Gamma_{IN}| = |S_{11} + \frac{S_{12} \cdot S_{21} \cdot \Gamma_L}{1 - \Gamma_L \cdot S_{22}}| < 1 \quad (2.15)$$

$$|\Gamma_{OUT}| = |S_{22} + \frac{S_{12} \cdot S_{21} \cdot \Gamma_S}{1 - \Gamma_S \cdot S_{11}}| < 1 \quad (2.16)$$

$$|\Gamma_S| < 1$$

$$|\Gamma_L| < 1 \quad (2.17)$$

In terms of the scattering parameters of the two port, if an amplifier is unconditionally stable these two equations should hold for any frequencies:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad (2.18)$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (2.19)$$

Unconditional stability is one of the goal of the LNA design. It means that any load presented to the input or the output of the device, the circuit will not oscillate for the complete range of the frequencies where the transistor has substantial gain.

There are three phenomena that cause instabilities. One of them is internal feedback of the transistor, another is external feedback around the transistor caused by the external circuit and excess of gain at frequencies outside of the band of operation.

2.2.3 Linearity

One of the important factor is the linearity to achieve optimum performance from the LNA. Linearity is an ability of amplifier to handle signals of varying level, without compressing the peak values of the modulated signal. [1] If the input signal power is small enough, the circuit will operate in linearity; however, when the input signal power increases, the amplifier's dynamic operation point will be changed due to nonlinearity. [7] Signal distortion is a direct result of the nonlinear behaviour of the devices in the circuit. [8] There are many measures of linearity, the most common measures are the third-order intercept (IP3) and the 1-dB compression point (P-1dB).

IP3 and P-1dB are summarized at the following statements: "As the input power level is increased, the circuit become saturated and the fundamental output fails to respond linearly to the input. Because of nonlinearity of the device, the gain compression causes the power gain to deviate from its idealized curve. The point at which the power gain drops 1 dB from ideal curve is referred to as the 1-dB compression point. [8] When two signals at different frequencies are applied to the nonlinear circuit, the output signals appear at applied signal frequencies and intermodulation (IM) product frequencies. [8] The third order intercept point (IP3) is the point at which the extrapolated third order intermodulation level (IM3) is equal to the signal levels in the output of a two-tone test when the extrapolation is made from a point below which the third order intermodulation follows the third order law." [9]

One of the trade-offs in designing LNA is the linearity and the current drain. To improve IP3 performance of the LNA for a given frequency, the current draw of the LNA should be increased. If the current draw is less important than IP3, it

can be increased slightly to increase the gain. While the lowest NF is obtained with a lower current draw, to improve IP3, higher current draw is required. Also P1dB match at the output different from conjugate gain match and it is an important factor to obtain higher IP3. Therefore, to improve linearity, a trade off will occur between current draw, NF and gain. [10]

A two tone linearity test, f_1 and f_2 frequencies are applied to the input of the LNA to determine IP3 products. The amplitudes of two IP3 products at $(2f_1 - f_2)$ and $(2f_2 - f_1)$ frequencies appearing close to f_1 and f_2 can then be measured. Third-order two-tone intermodulation products $(2f_1 - f_2)$ and $(2f_2 - f_1)$ have a crucial role on the upper limit on the dynamic range of the amplifier. [1]

2.2.4 Input and Output Matching

An important step in LNA design is the input and output matching. The dilemma in choosing the input match in LNA is summarized at the statement below: "A typical approach in LNA design is to design an input matching circuit that terminates the transistor with a Γ_{opt} , which represents the terminating impedance of the transistor for the best noise match. In many cases this means that the input return loss of LNA will be sacrificed. The optimal input return loss can be achieved only when the input matching network terminates the device with a conjugate of S_{11} , which in many cases is different from conjugate of Γ_{opt} ." [11] Same argument is given also in [12].

As for the output matching, there is a trade-off between linearity and output return loss. For narrow band LNA, conjugate matching is used to maximize the gain of the device. However, depending on the application, additional IP3 requirements can change the output matching of the circuit. Because the optimal gain impedance does not match with IP3 point, there will be trade-offs between linearity and gain. [13] This is not a constraint for this thesis and conjugate match is used for output matching to obtain high gain.

The goal of this thesis is to achieve the minimum noise figure. Therefore,

the optimum source reflection coefficient, Γ_{opt} , is selected for source reflection coefficient, Γ_S . Then conjugate matching is selected at the output to set load reflection coefficient, Γ_L . [14], [15]

2.2.5 Transistor Selection

A critical aspect while designing a Low Noise Amplifier is the selection of the transistor that will be used in the circuit. Because the LNA design has many trade-offs, transistor should be suitable to satisfy the requirements of high gain and low noise figure. [11], [12] In this thesis, X to Ku band super low noise transistor, HJ-FET transistor NE3511S02, manufactured by NEC Technologies was chosen. Datasheet values of the transistor seems to satisfy the prestated conditions to a reasonable extent.

2.3 Noise Figure Measurement Techniques

There are two main techniques for measuring noise figure; Y-Factor method and cold source method. The Y-factor or hot/cold-source method is the most commonly used and is generally implemented with noise-figure analyzers and spectrum analyzer-based solutions. In contrast, the cold-source method is usually performed using vector network analyzers (VNAs), which provide magnitude and phase information. Commonly, the cold-source technique makes it possible to achieve better accuracy in low noise figure measurements. [16]

2.3.1 Y-Factor Method

The Y-Factor method is a common method for noise figure measurement. The Y-factor method uses a calibrated noise source. [16] A calibrated noise source consists of a specially designed noise diode that can be turned on or off. If the diode is turned off, it means that the noise source is in its cold state and the

noise source presents a room temperature termination to the amplifier. If the diode is turned on, it means that the noise source is in its hot state and the noise source presents an electrical noise that is higher than the cold state noise. The hot state is characterized by the excess noise ratio (ENR) which is calibrated against frequency. [17] From two measurements, cold state and hot state, and knowing ENR values of the noise source, the scalar gain and the noise figure of the amplifier can be calculated.

Y-factor is a ratio of two noise power levels, one measured with the noise source on and the other with the noise source off as in equation 2.20. Also noise power is proportional to noise temperature as in equation 2.21. Therefore, Y is measured several times for sampling and an averaged value of Y can be computed. [18]

$$Y = N_{ON}/N_{OFF} \quad (2.20)$$

$$Y = T_{ON}/T_{OFF} \quad (2.21)$$

ENR is calculated as in equation 2.22 where T_{SON} and T_{SOFF} are noise temperature of the noise source in its on or off states. T_0 is the reference temperature of 290 K. [18]

$$ENR_{dB} = 10 \log((T_{SON} - T_{SOFF})/T_0) \quad (2.22)$$

ENR value is commonly given for each specific noise source with respect to frequency. In Y-Factor method noise source is connected to input of the device under test (DUT) and output of the DUT is connected to a spectrum analyzer. DUT is turned on during the measurement. Noise source is turned off which means that it is in cold state and noise level measured in spectrum analyzer is N_{OFF} , then noise source is turned on which means that it is in hot state and noise level measured in spectrum analyzer is N_{ON} . Given the noise levels Y is calculated according to equation 2.20. If the ENR of the noise source is known, noise figure (F) can be calculated with equation 2.20. Some spectrum analyzers has this function to carry out the calculation automatically to measure the noise figure.

$$F_{dB} = ENR_{dB} - 10 \log(Y - 1) \quad (2.23)$$

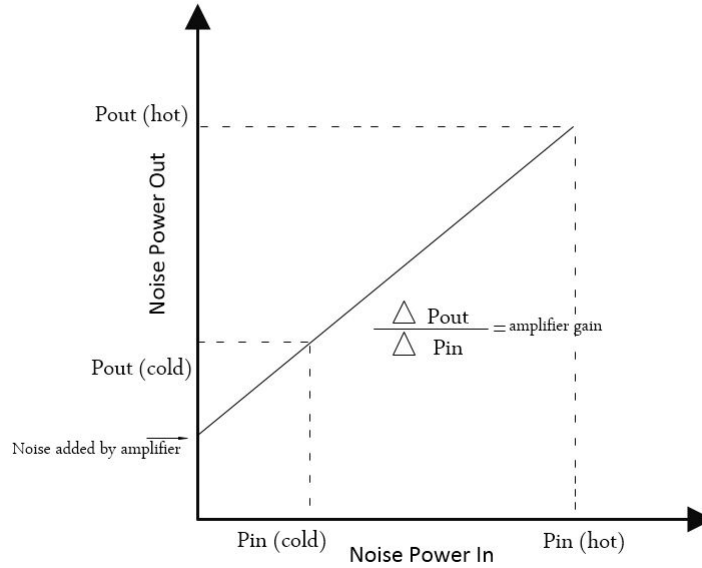


Figure 2.4: Graphical representation of Y-Factor method

While measuring noise figure, there are assumptions and uncertainties of Y-Factor method. The first assumption is the output impedance of the noise source matching of amplifier. It is commonly expected to be exactly 50Ω . However, for the most of the cases, it is not. Because, main element of the noise source is a diode and usually diodes' impedance is not controlled and the impedance of the diode changes with applied voltage (on and off state). Furthermore, as explained in Section 2.2.4, input impedance of a LNA can be mismatched because of noise matching. This mismatch between amplifier and noise source causes an uncertainty in Y-factor method.

Another cause of error in Y-factor method is excessive input noise used when measuring very low noise amplifiers. ENR level of the noise source should be as small as possible in low noise DUT measurements. In such measurements, numerical errors can create large uncertainties.

2.3.2 Cold Source Method

Cold source method is often used with vector network analyzers and it relies on good measurement of gain. Similar to Y-factor method, the noise power injected to DUT is known; however, for a single power level. Typically a 50Ω termination is used as noise source. On the other hand, the gain of the DUT is very well known because a VNA is used for this measurement. In contrast to Figure 2.4 instead of knowing two point of same graph, a point and slope of the graph is known in cold source method in Figure 2.5. In other words, gain represents slope and input/output noise levels represent a point.

Figure 2.5 defines the slope of the line from an independent gain measurement of the amplifier. Only one power measurement is needed to establish Y-intercept point which allows derivation of the noise figure of the circuit. [19]

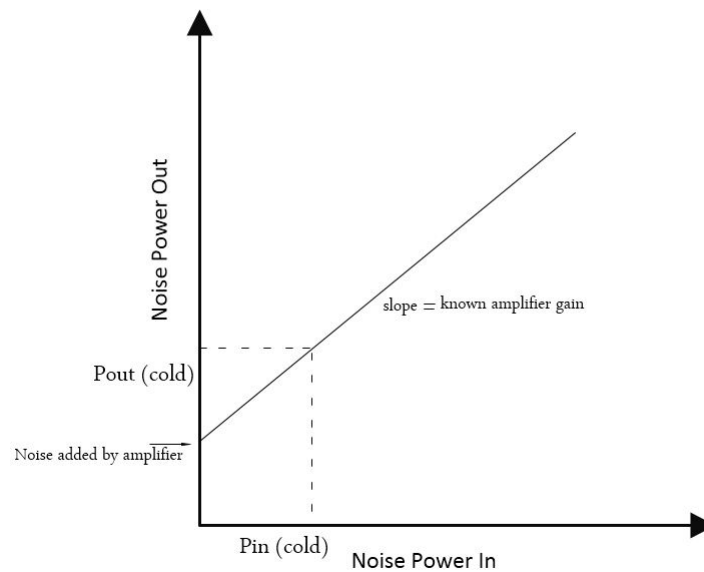


Figure 2.5: Graphical representation of cold-source method

Noise Figure measurement with cold source method presents more smooth and nicely centered results than Y-factor method. Although noise source is directly connected to the input of the amplifier in Y-Factor method, the PNA-X measurement results have lower uncertainty than the Y-factor method (0.2 dB for the PNA-X versus about 0.5 dB for Y-factor). [16] Because of uncertainties,

especially when measuring sub-1 dB noise figures, vector calibration of the measurement reference plane and mismatch correction between the noise source and amplifier become critical to measure precision. [20]. For low and medium noise figure devices, the PNA-X measurement results are quite significant.[16]

2.4 Simulation Techniques Used

The LNA design is simulated and optimized using the Advanced Design System (ADS) software of Agilent Technologies Inc. with using ADS, the design is tuned to get the optimum value for noise figure, gain, stability and input and output reflection coefficients.

2.4.1 Small Signal S-Parameters Simulations

By using S-Parameters simulation controller in ADS which is a type of small signal AC simulation, the scattering parameters of the design is obtained with respect to swept frequency. Also, the noise figure of the system is obtained using S-Parameter simulation. Each company provide S-parameters for their products such as transistors, capacitors, resistors. S-parameters have a file extension .s2p. which contains S-Parameters and noise parameters. The LNA is designed using this .s2p. file; therefore, S-Parameters and gain of the entire LNA are obtained. By enabling noise tab, all noise calculations could also be obtained.

2.4.2 DC Simulations

If the design contains a non-linear device, a DC simulation which verifies the proper DC operating characteristics of the design should be performed. By using DC simulation and adding relevant current probe, active bias circuit is arranged using Spice model of the transistor to obtain the required drain voltage and drain current of the transistor.

2.4.3 Momentum Simulations

Momentum electromagnetic simulator which is based on the Method of Moments (MoM) is very helpful in achieving the optimal design goals and in optimizing the structure of the design based on electromagnetic simulation. By using Momentum, as the schematic circuit is converted to the physical layout, simulation of the circuit including microstrip topology is carried out.

2.5 Microstrip Technology

Microstrip is a popular microwave transmission-line technology. Microstrip transmission line circuits are operating in a quasi transverse electromagnetic (TEM) mode which has non-zero electric and magnetic fields in the propagation direction. [21] Because it is an open conduit for wave transmission not all of the electric and magnetic fields will be confined in the structure. This fact, along with the existence of a small axial E-field, leads not to purely TEM wave propagation, but to a quasi-TEM mode of propagation. [1] Field configuration of the microstrip transmission line is shown in Figure 2.6. Also, in Figure 2.7, it is illustrated that a microstrip transmission line consists a signal conductor on the top and a ground plane on the bottom of the substrate and ground plane separated by a dielectric medium of thickness (d).

In high frequency circuit designs, loss budgets, propagation mode issues, radiation losses and electromagnetic interference (EMI), and even the printed-circuit-board (PCB) assembly logistics and the relative difficulty of adding components to a PCB are considered. All simulations are done by using both ADS tool Schematics and Momentum Simulator in order to achieve results that are close to real measurements. Also, the physical dimensions of the microstrip stubs and lines are calculated with LineCalc tool available in ADS, which is based on the properties of the substrate and the operating frequency.

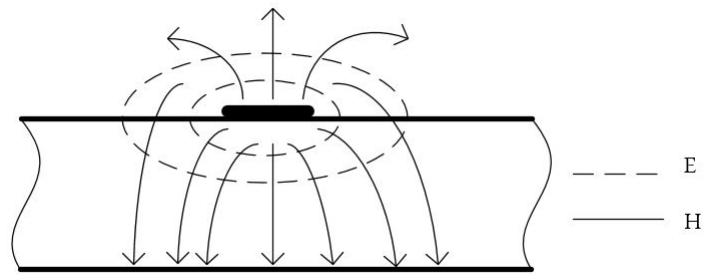


Figure 2.6: A microstrip transmission line field configuration

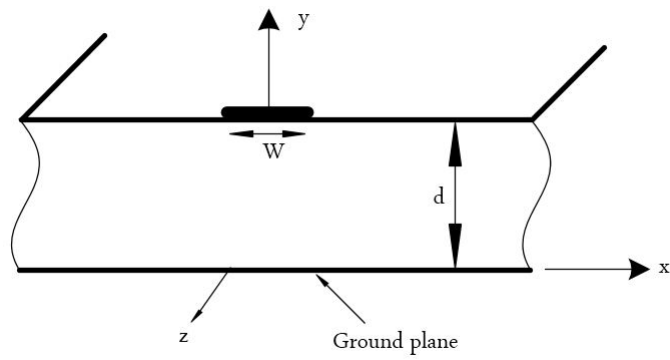


Figure 2.7: A microstrip transmission line geometry

Chapter 3

Design and Simulation Results

The design of two stage cascaded X-Band LNA in microstrip technology using active bias networks for minimum noise application is studied in this thesis. The operating frequency band is 8.2 - 8.4 GHz. The objective of the thesis is to get good gain with minimum noise figure for the entire bandwidth. The design procedure is simulated and optimized using Advanced Design System (ADS) software of Agilent Technologies Inc. All simulations and optimizations are done by using both schematic and momentum simulation tools. RO4003 Rogers material with $\epsilon_r = 3.38$, substrate thickness $t = 0.508$ mm substrate is used. The design contains X to Ku band super low noise N-Channel HJ-FET transistor NE3511S02 manufactured by NEC Technologies, microstrip lines for matching networks, MMBT2907A PNP transistor and standard 0402 package lumped elements for active bias circuit.

At first, one stage LNA is simulated, fabricated and optimized, then two stage LNA is designed, simulated and fabricated. One stage X-band LNA achieves a noise figure of 1.2 dB, a power gain of 12 dB with respectively -4.5 dB input and -25.8 dB output return losses at a frequency range of 8.2 - 8.4 GHz. Two stage X-Band LNA achieves a noise figure of 1.4 dB, a power gain of 22 dB with respectively -3,2 dB input and -12,6 dB output return losses. In this section of the thesis, the simulation results are reported.

3.1 Design of Active Bias Circuit

An active bias circuit is widely used for biasing of the transistor. In the active bias circuit, while an op-amp which requires an extra power supply could be used, PNP transistor is a simpler approach and frequently used. In this thesis, PNP transistor is used for the active bias circuit.

To obtain a good performance from the RF transistor, datasheet supplied by the manufacturer of the transistor is a good starting point for LNA design. Active bias circuit represents the first step in LNA design. S-parameters and Spice model of the transistor is supplied by the manufacturer. Drain current, I_d , 10 mA and gate to source voltage, V_{gs} , -500 mV for drain to source voltage, V_{ds} , 2V is a good starting point as suggested by the NE3511S02 datasheet. Therefore, active bias circuit with PNP type transistor is arranged to obtain these parameters. To bias the transistor at the values suggested above, the active bias circuit proposed in Figure 3.1 and Figure 3.2 shows result of DC simulation.

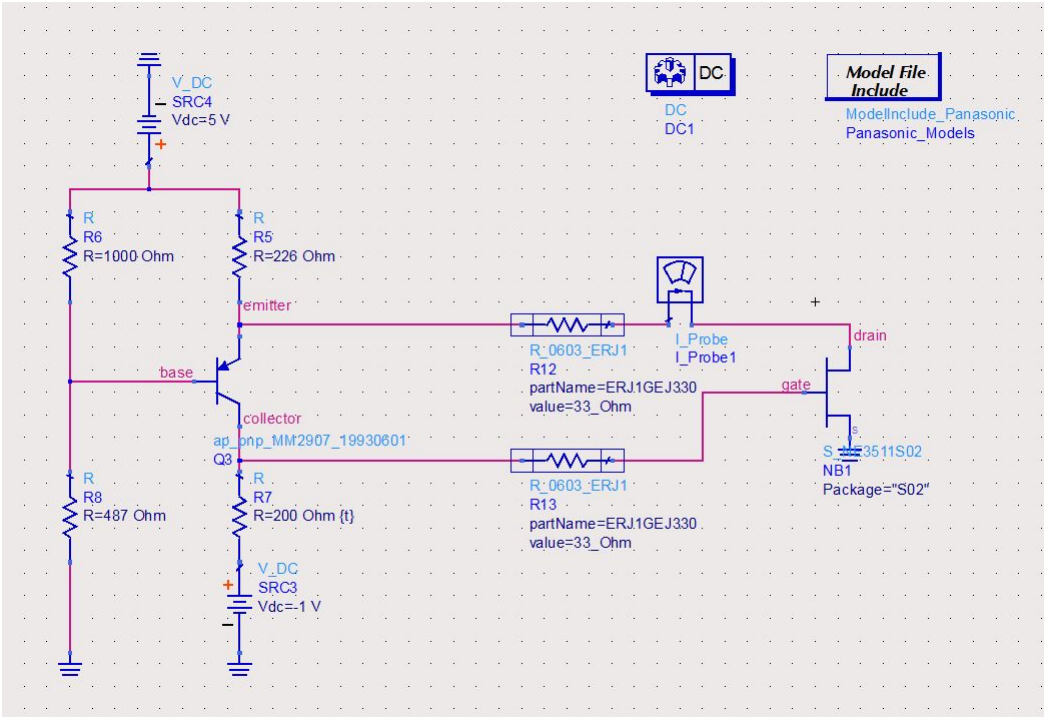


Figure 3.1: Proposed active bias circuit

freq	drain	gate	I_Probe1.i	base	emitter	collector
0.0000 Hz	1.986 V	-507.8 mV	9.479 mA	1.643 V	2.298 V	-507.8 mV

Figure 3.2: The result of DC simulation

Bias network contains also RF-Chokes. Transmission lines and radial stubs, TL1, TL16, Stub1 and Stub2 that transform AC short circuit to AC open circuit in Figure 3.3 are $\lambda/4$. With straight transmission line, radial stubs are also used for providing a clean broadband short circuit. These RF chokes should be ensure good isolation of the active bias source from the RF input and output.

The lengths and widths of the microstrip transmission lines and radial stubs are calculated with LineCalc tool available in ADS which is based on the properties of substrate used and operating frequency. For both one stage and two stage LNA design, same active bias circuit and bias network which includes RF chokes is used. After making sure that active bias circuit and bias network in one stage LNA design, they are used in two stage LNA design in the same way.

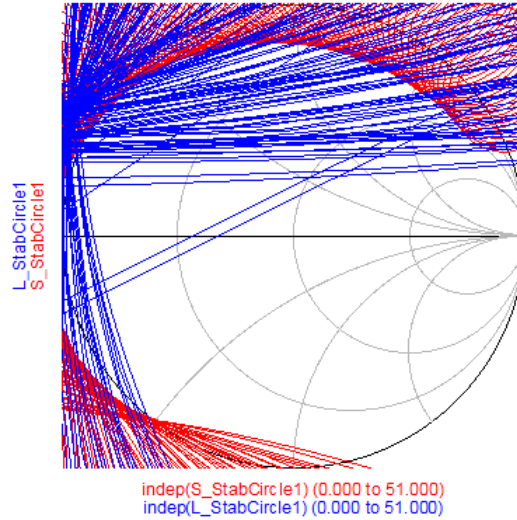


Figure 3.4: Source and load stability circles of transistor

Two methods are applied for stabilization. Firstly, series resistor, 33 ohm is added in the output port of the transistor to stabilize circuit in all frequencies. Even though this method is capable of improving the stability of the circuit, it also decreases the gain of the amplifier. Since there is a trade-off with stability and gain, the value of the resistor should not be high too much.

Secondly, series resistors, 33 ohm are added in the gate and drain of the NE3511S02 transistor in the active bias circuit after RF choke transmission lines to stabilize in low frequencies. Also the advantage of these series resistors in the drain and gate of the transistor does not reduce gain as much as. Same methods are used both one stage and two stage LNA designs as illustrated in Figure 3.5.

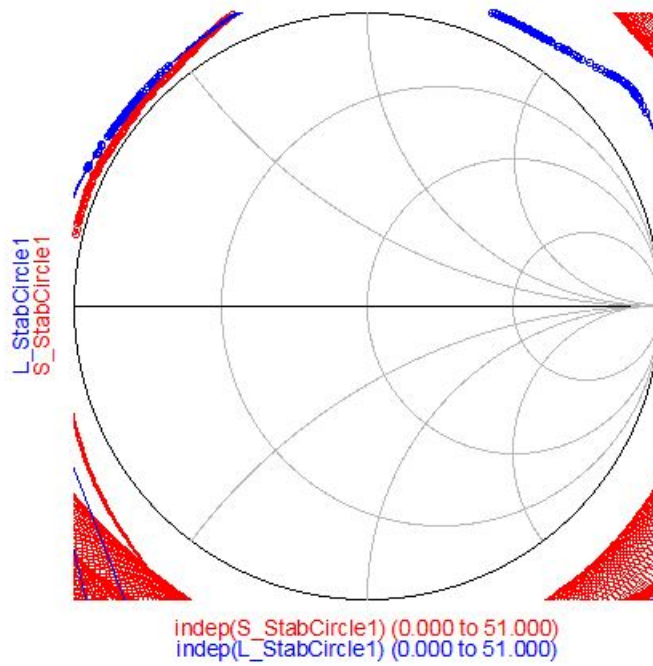
with respect to S_{opt} . To achieve minimum noise figure, the optimal source reflection coefficient is selected to source reflection coefficient, Γ_S . As Γ_S approaches Γ_{opt} , the transistor noise factor approaches its minimum. As Γ_S departs from Γ_{opt} , the noise factor increases. [22] For input matching series transmission line and single open stub matching technique is used on smith chart tool.

For output matching, conjugate matching method is used to match the output to 50Ω . For output matching series transmission line and single open stub matching technique is used on Smith Chart tool in ADS for both one stage and two stage LNA designs.

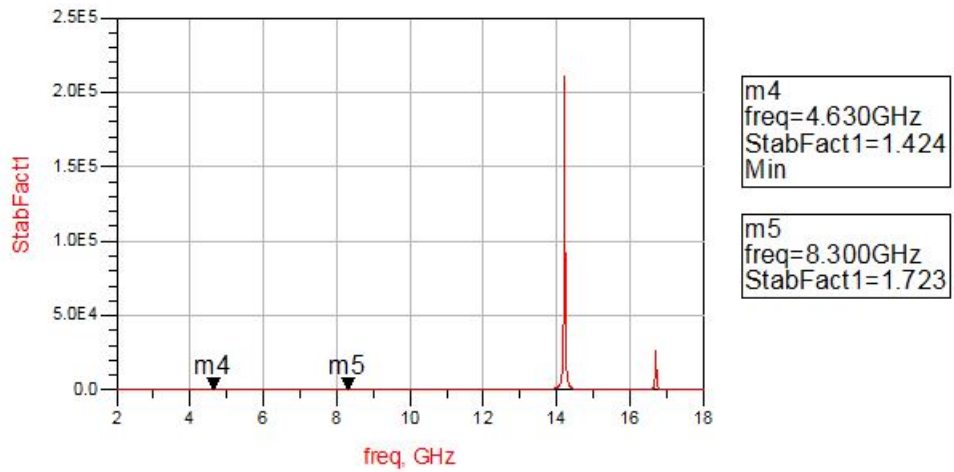
3.4 One Stage LNA Design

3.4.1 Stability

One stage LNA satisfies the unconditional stability. The following figures illustrate stability factor and input output stability circles. When K-factor is greater than unity, the circuit will be unstable for any load. After stabilizing the circuit with series resistors illustrated in Figure 3.5, schematic and momentum simulation results at frequency range of 2-18 GHz are given in Figure 3.6 and Figure 3.7. As seen from the figures, all stability factors are greater than one and all stability circles are out of smith chart which means that one stage LNA circuit is unconditionally stable in frequency range of 2-18 GHz.

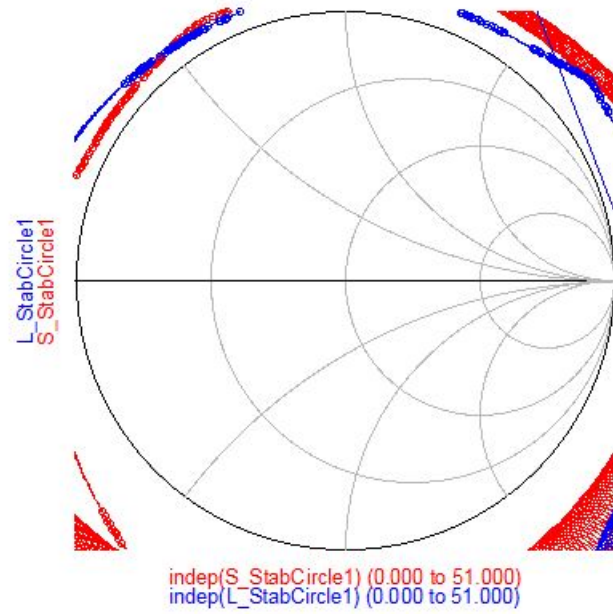


(a) Stability circle

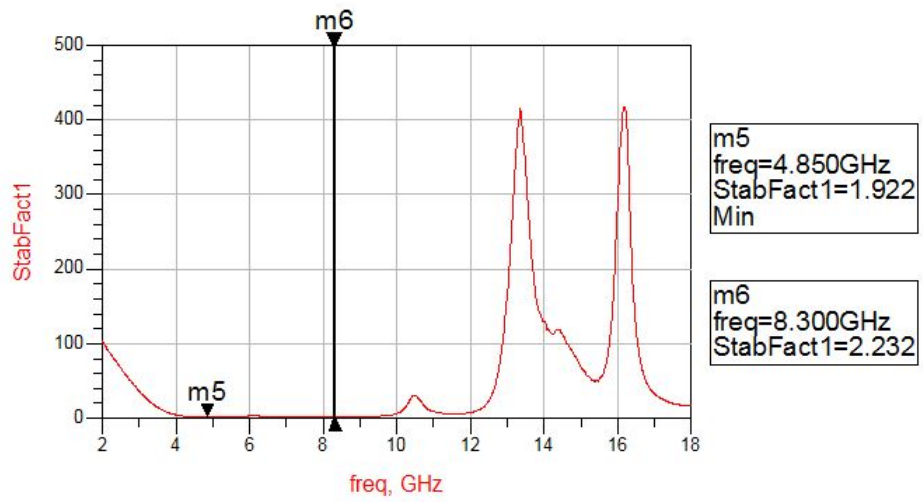


(b) Stability factor

Figure 3.6: Schematic simulation results



(a) Stability circle



(b) Stability factor

Figure 3.7: Momentum simulation results

3.4.2 Input Matching

Noise matching achieved by using Smith Chart tool available in ADS consists series transmission line and open stub, TL5 and TL7 as seen in Figure 3.8.

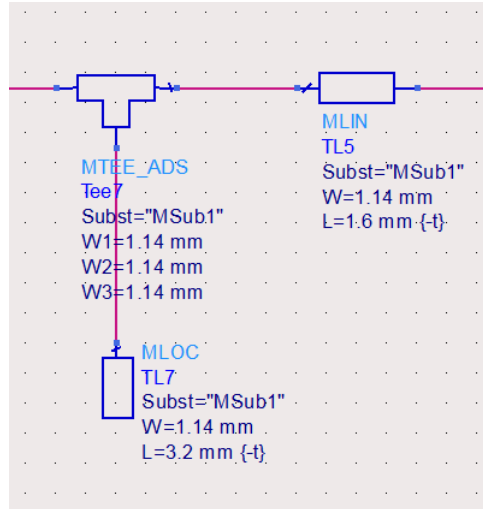
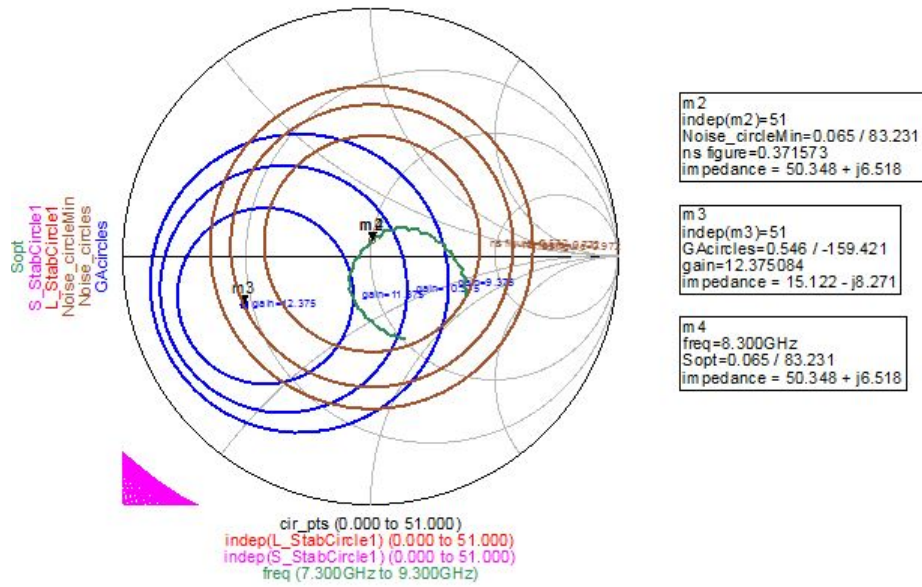
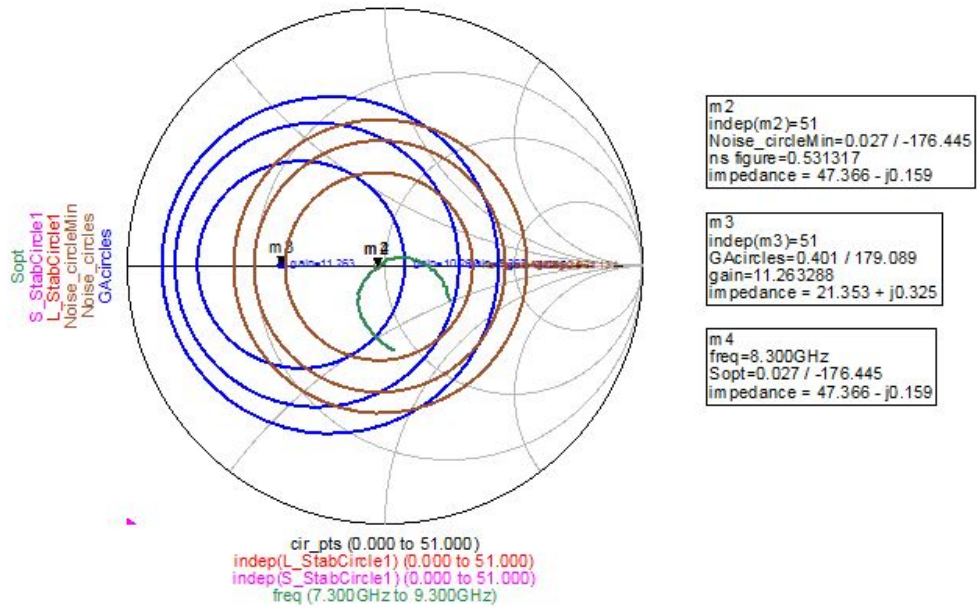


Figure 3.8: Input matching

After optimizing the input match circuit with both schematic and momentum simulations, noise and gain circles are obtained as in Figure 3.9. Optimum reflection coefficient is also illustrated in Figure 3.10.

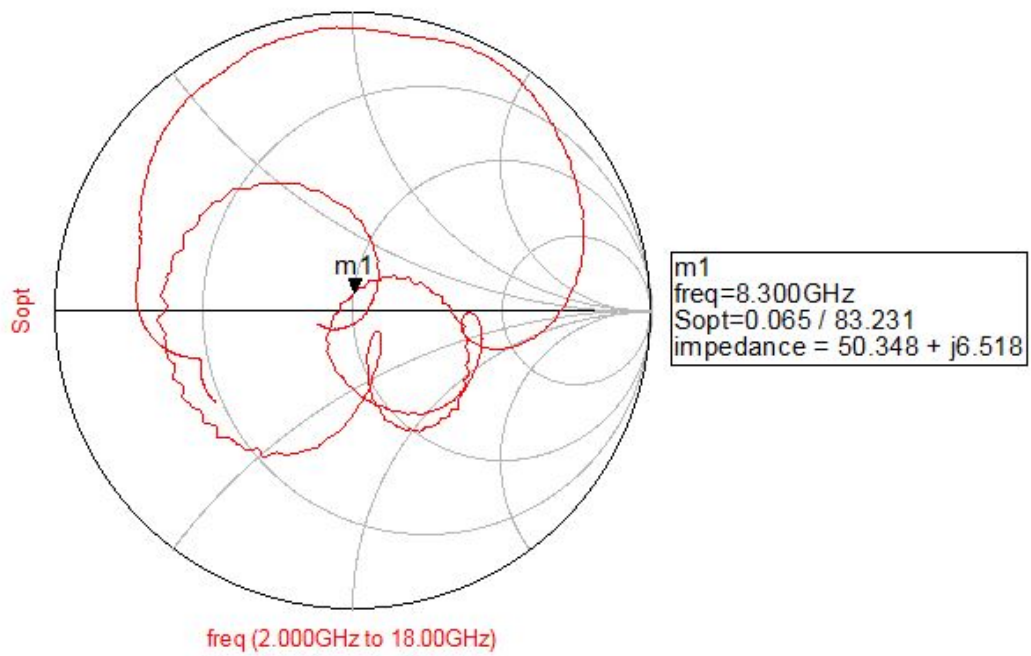


(a) Noise and gain circles with schematic simulation

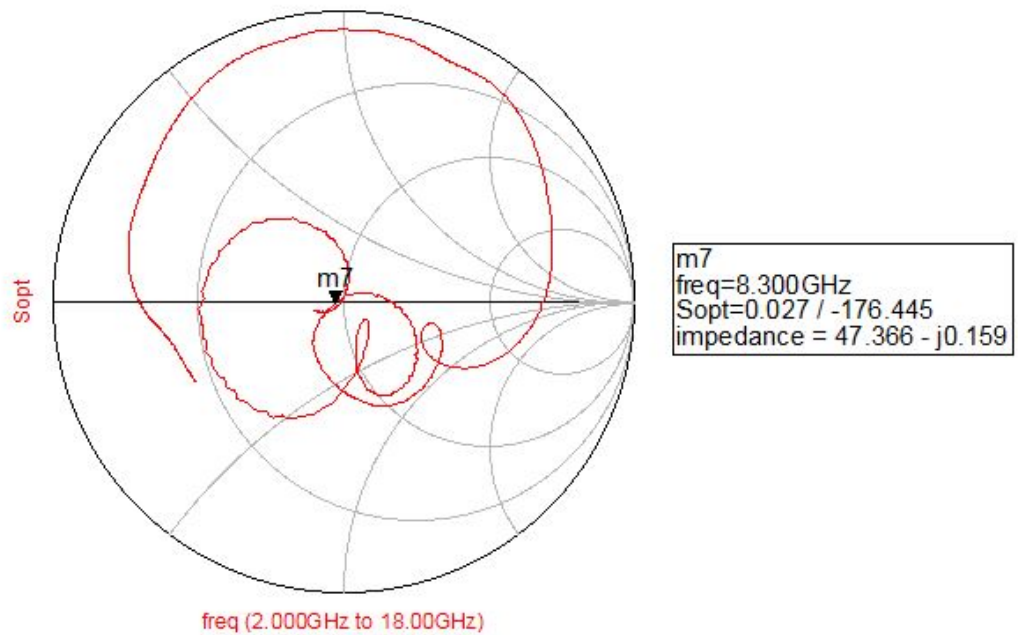


(b) Noise and gain circles with momentum simulation

Figure 3.9: Noise and gain circles



(a) Γ_{opt} with schematic simulation

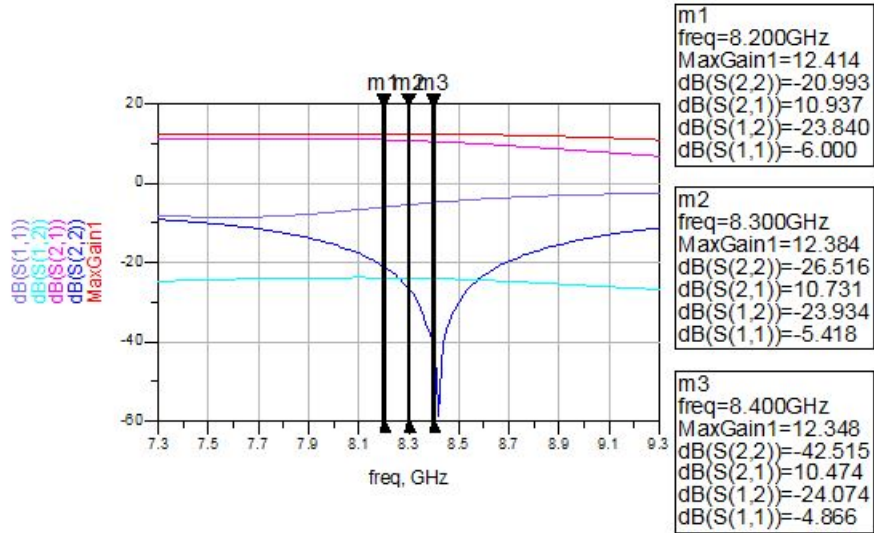


(b) Γ_{opt} with momentum simulation

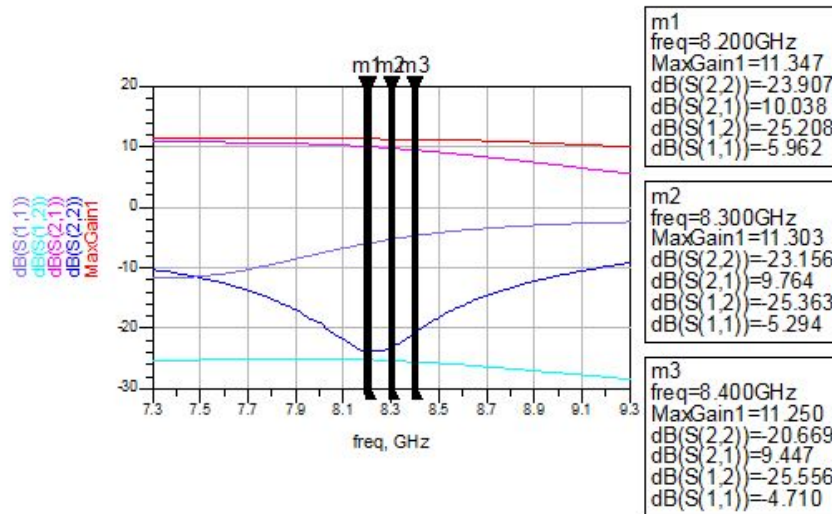
Figure 3.10: Γ_{opt}

At the results of optimization of input matching with respect to get minimum

noise figure, S-Parameters and Noise Figure schematic and momentum simulation results are given in Figure 3.11 and Figure 3.12

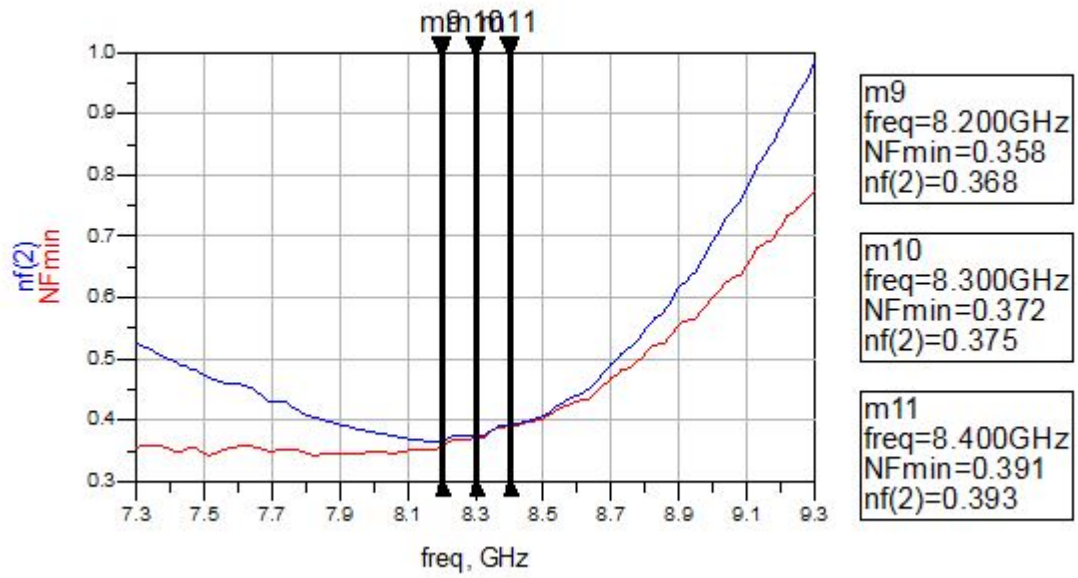


(a) S-Parameters with schematic simulation

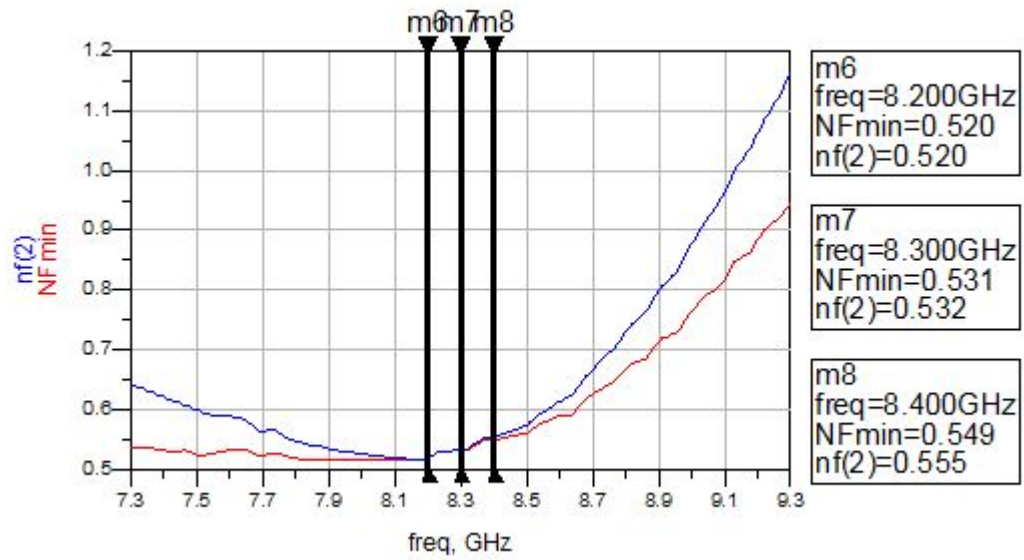


(b) S-Parameters with momentum simulation

Figure 3.11: S-Parameters



(a) Noise figure with schematic simulation



(b) Noise figure with momentum simulation

Figure 3.12: Noise figure

3.4.3 Output Matching

Conjugate matching which consists series transmission line and open stub, TL and TL as illustrated in Figure 3.13 is designed using Smith Chart tool.

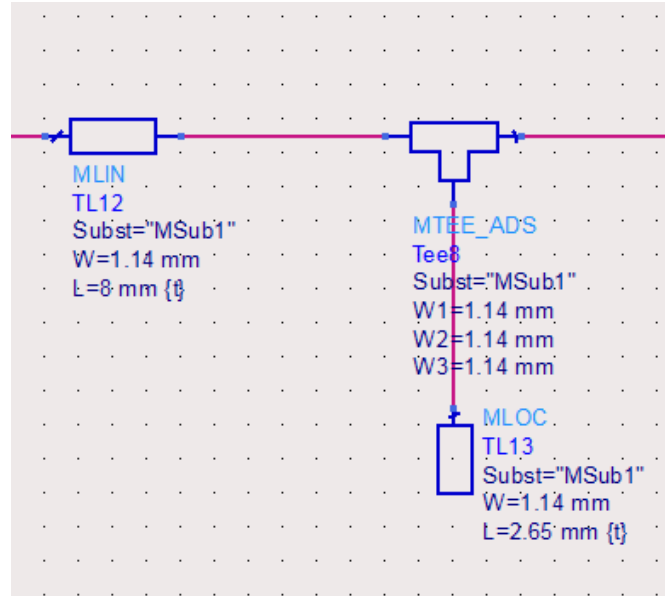
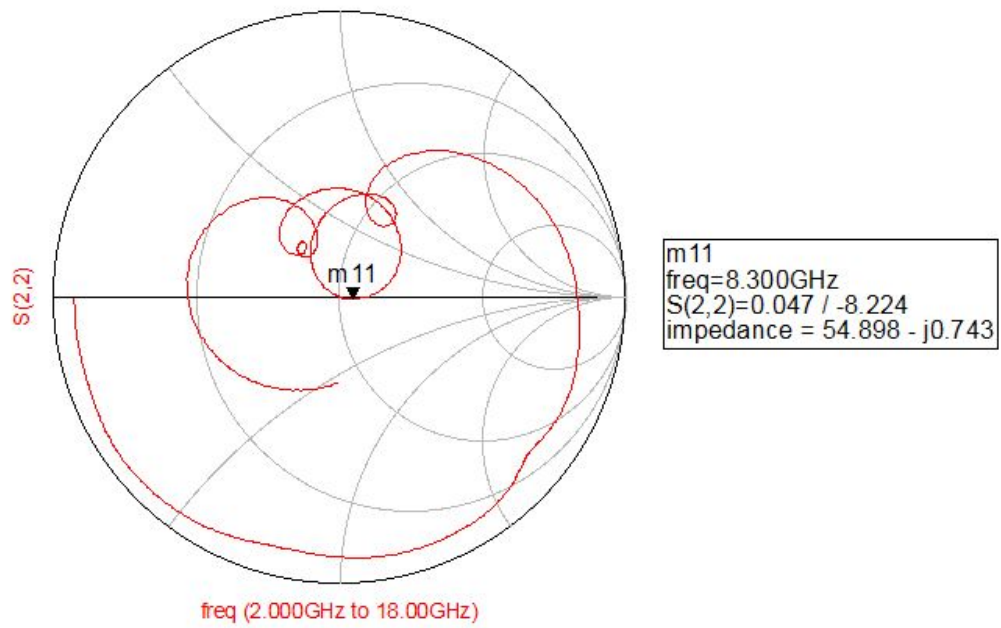
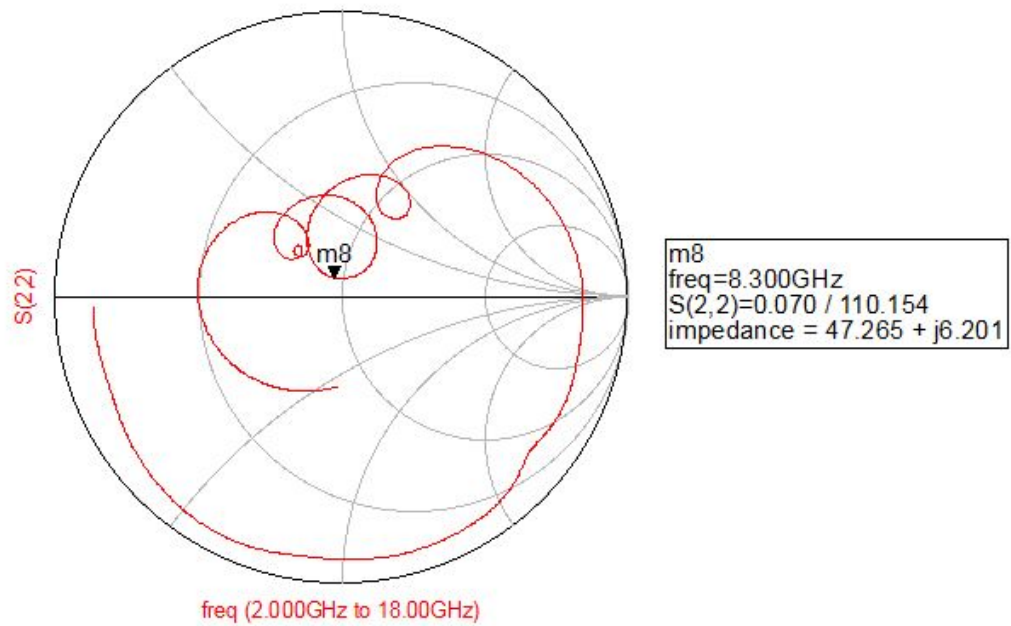


Figure 3.13: Conjugate matching

After optimization for conjugate match $S(2,2)$ of schematic and momentum simulation results are illustrated in Figure 3.14.



(a) $S(2,2)$ with schematic simulation



(b) $S(2,2)$ with momentum simulation

Figure 3.14: $S(2,2)$

3.4.4 Final Design and Printed Circuit Board Layout

One stage LNA design is simulated both schematic and momentum simulation tools in ADS. Figure 3.15 is design of schematic simulation, whereas Figure 3.16 and Figure 3.17 are design of momentum simulations in ADS. The PCB is designed in Altium PCB Designer. Source of the transistor is filled with vias to do ground this part of the transistor. PCB Layout is as shown in Figure 3.18.

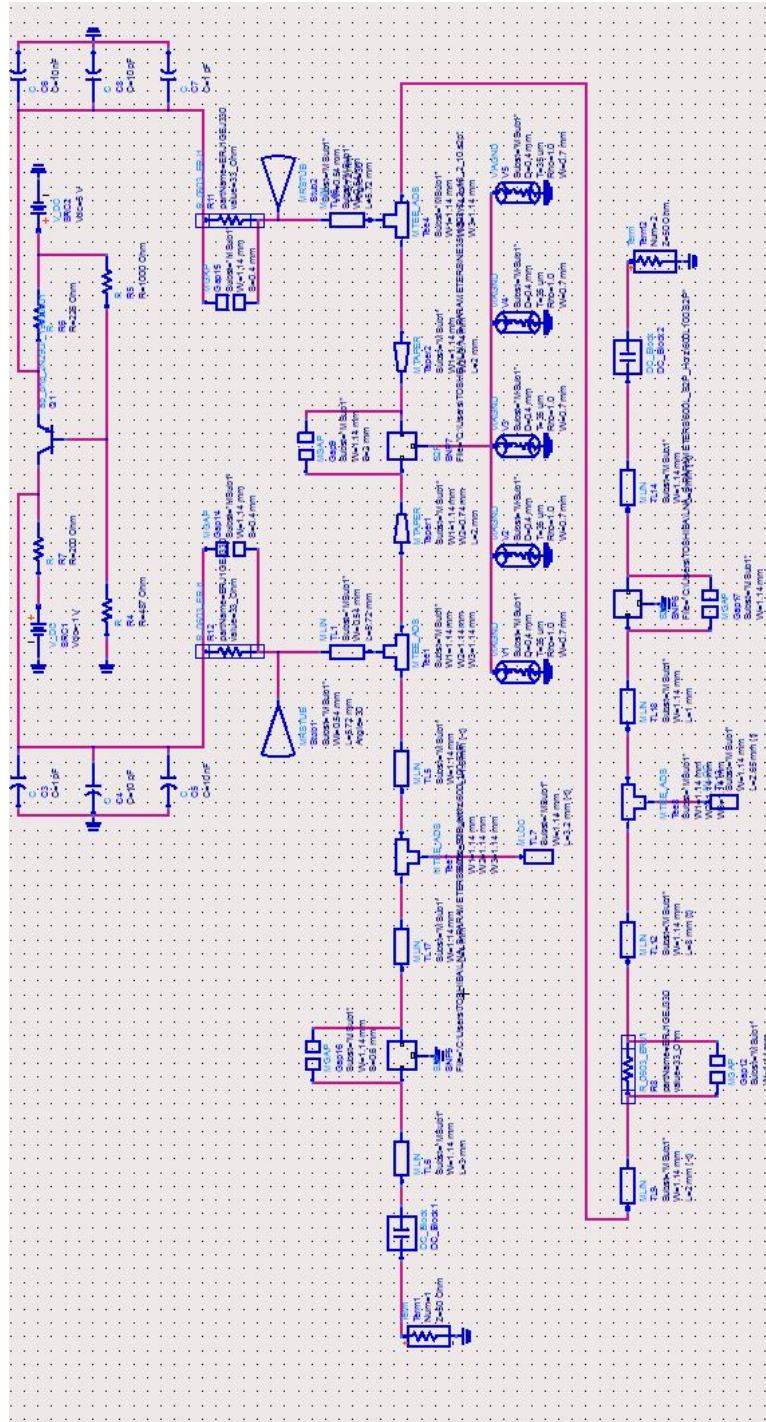


Figure 3.15: One stage final design of schematic simulation

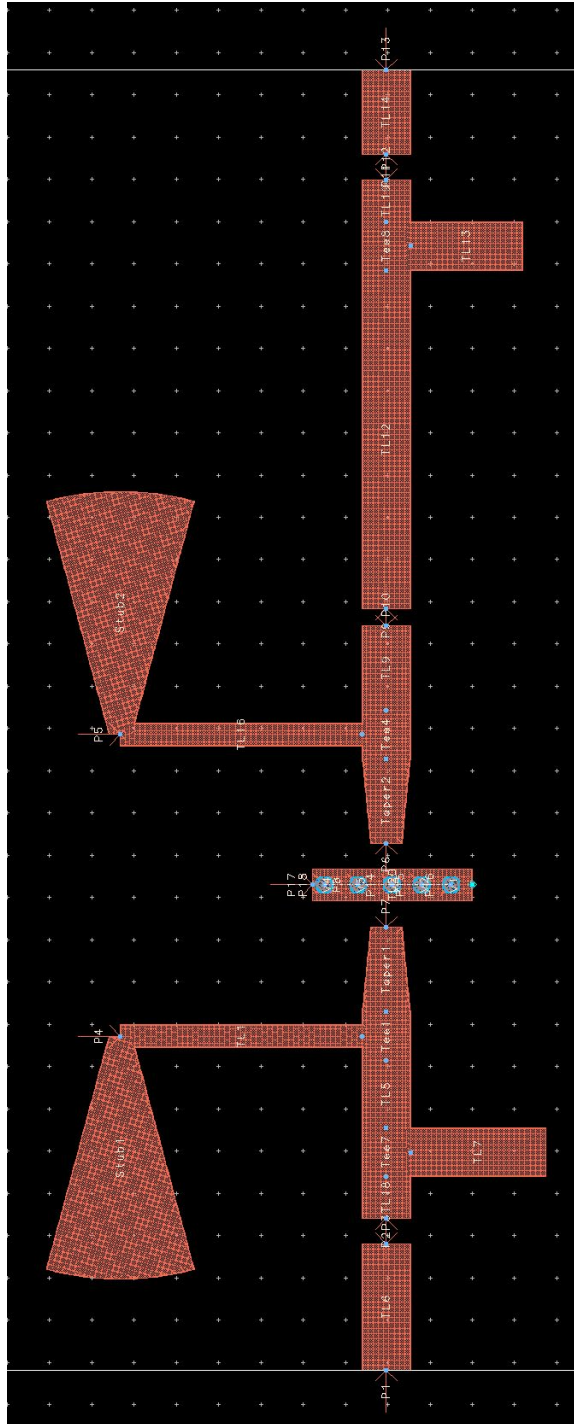


Figure 3.16: One stage layout in momentum simulation

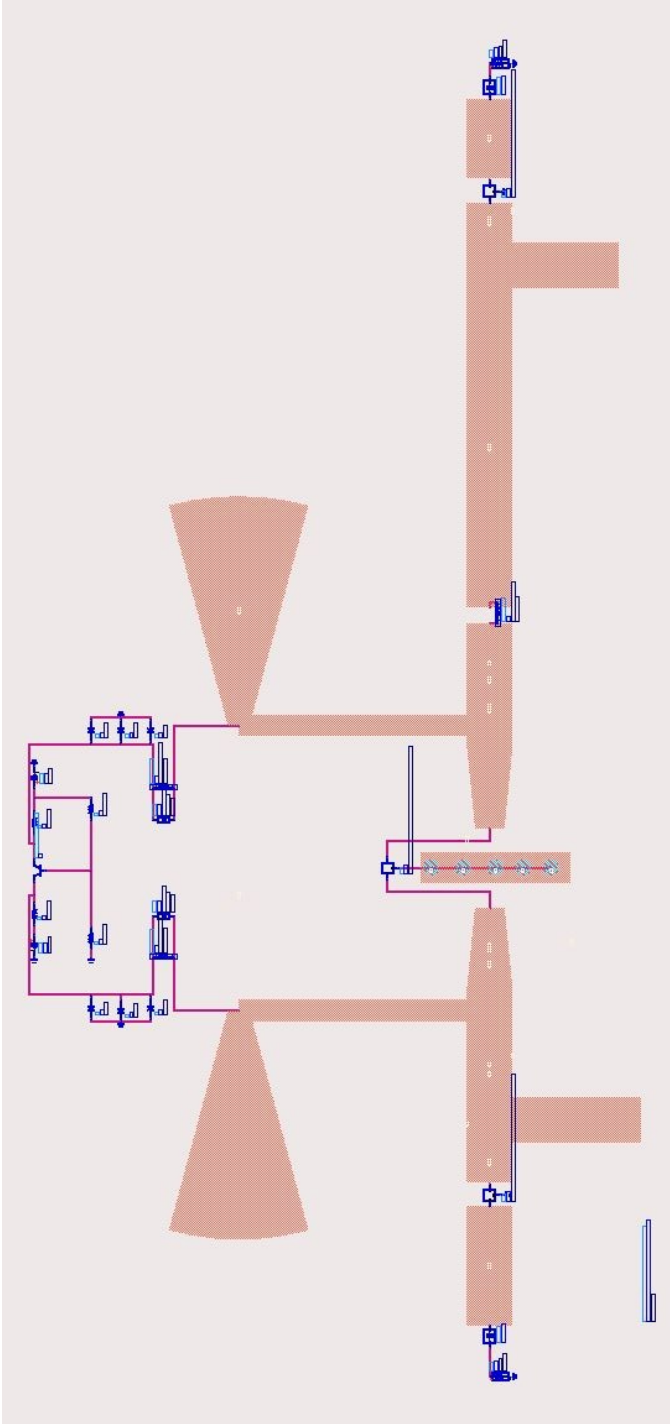


Figure 3.17: One stage final design of momentum simulation

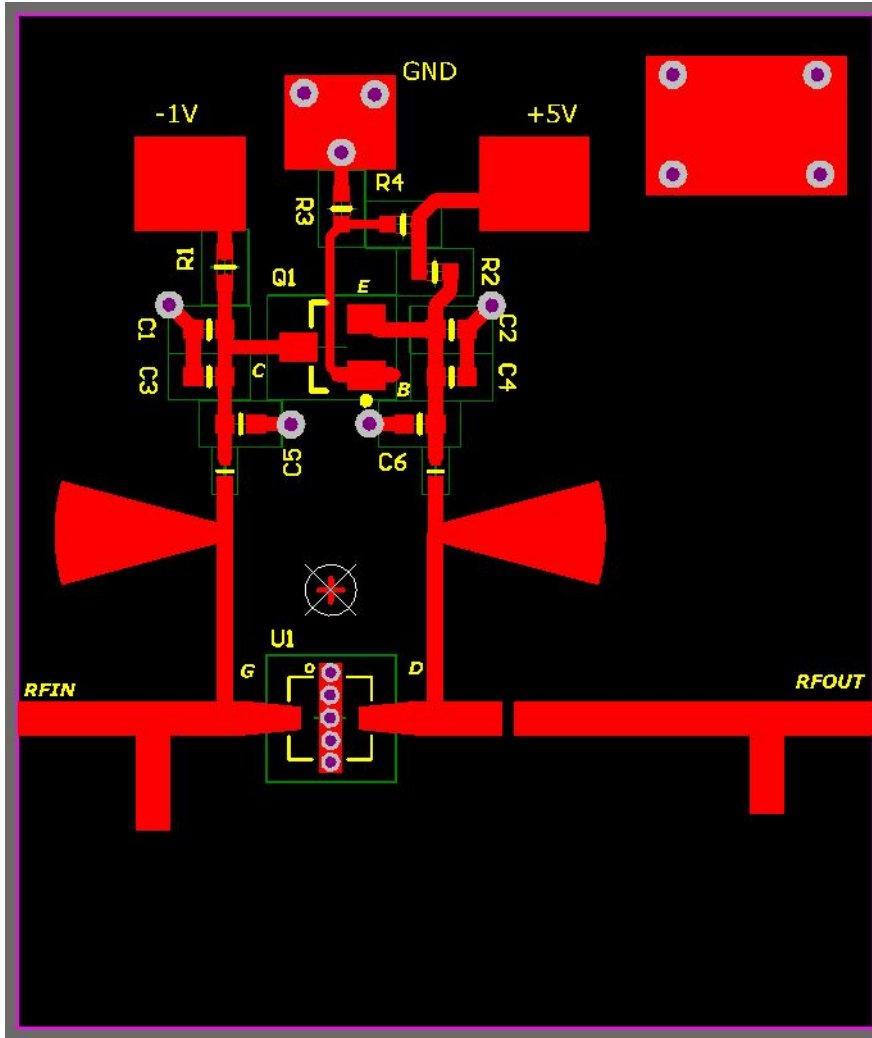
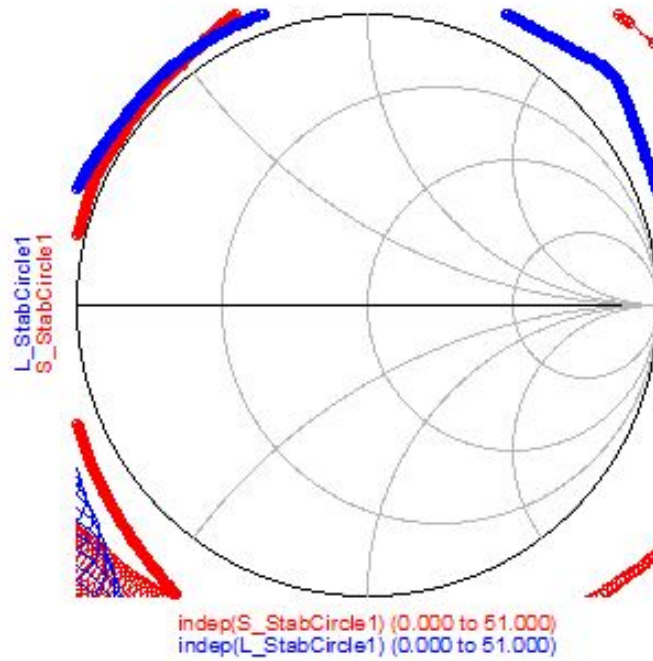


Figure 3.18: One stage PCB design

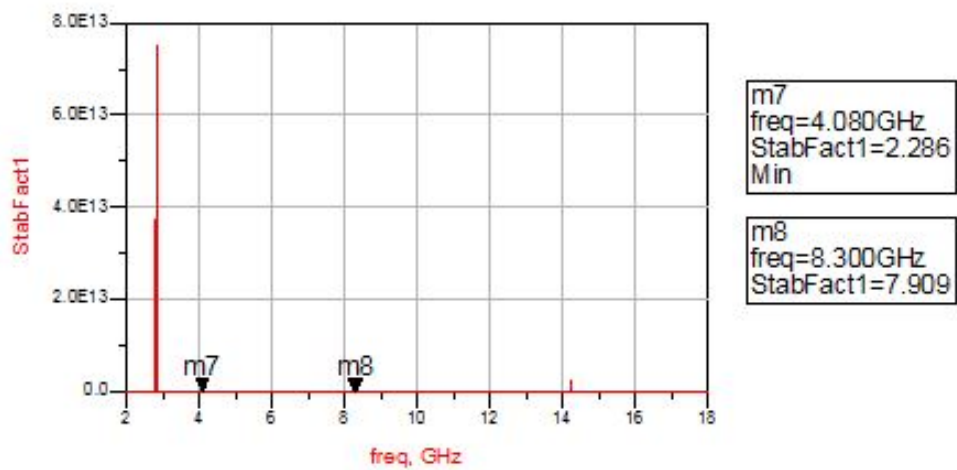
3.5 Two Stage LNA Design

3.5.1 Stability

Schematic and momentum simulation results at frequency range of 2-18 GHz are given in Figure 3.19 and Figure 3.20. As seen from the figures, all stability factor are greater than one and all stability circles are out of Smith Chart which means that one stage LNA circuit is unconditionally stable in frequency range of 2-18 GHz.

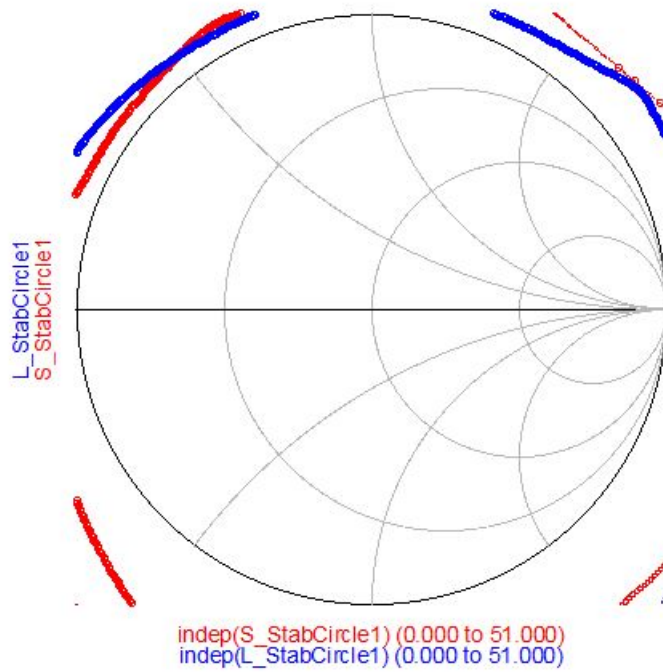


(a) Stability circle

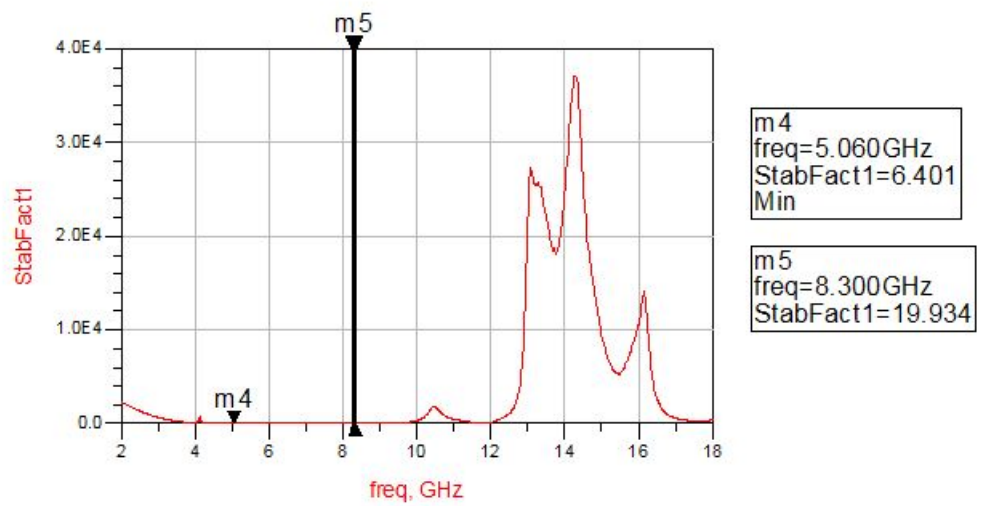


(b) Stability factor

Figure 3.19: Schematic simulation results



(a) Stability circle

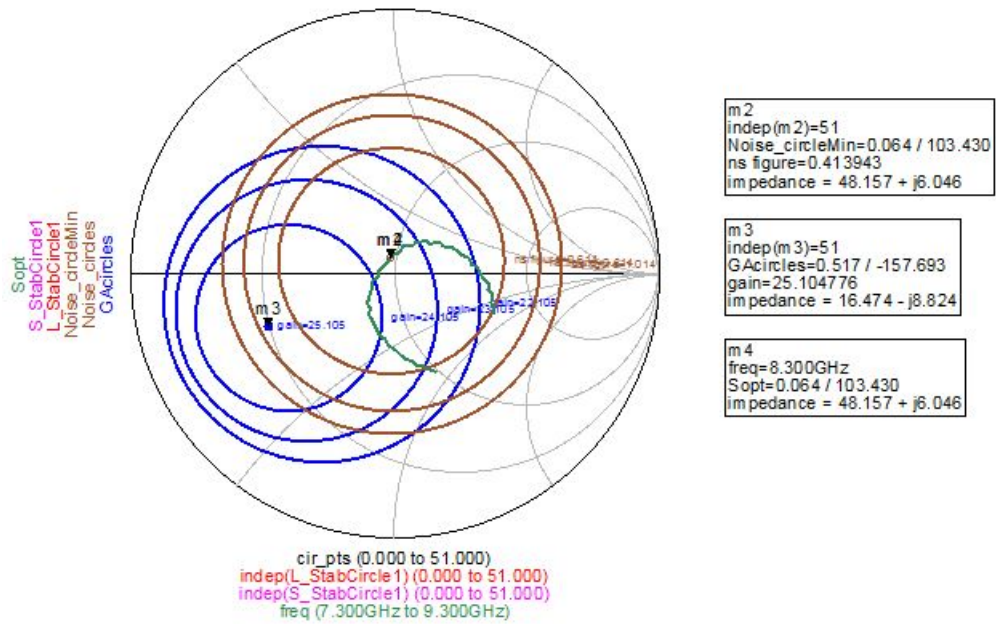


(b) Stability factor

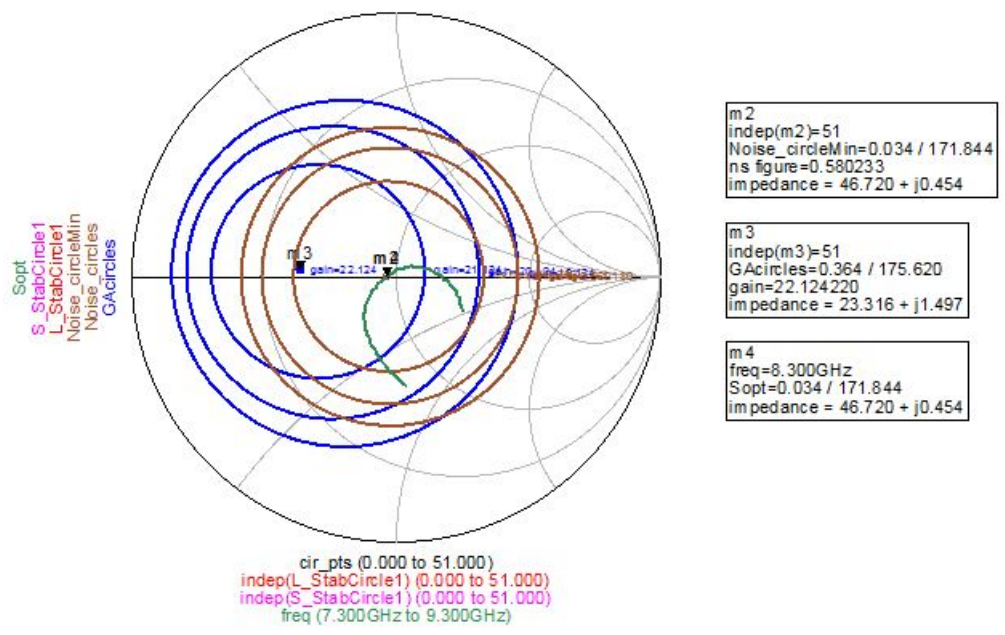
Figure 3.20: Momentum simulation results

3.5.2 Input Matching

Without changing input matching, two stage LNA design is achieved by adding intermediate matching as conjugate matching. Both schematic and momentum simulations, noise and gain circles are obtained as in Figure 3.21. Optimum reflection coefficient is also illustrated in Figure 3.22.

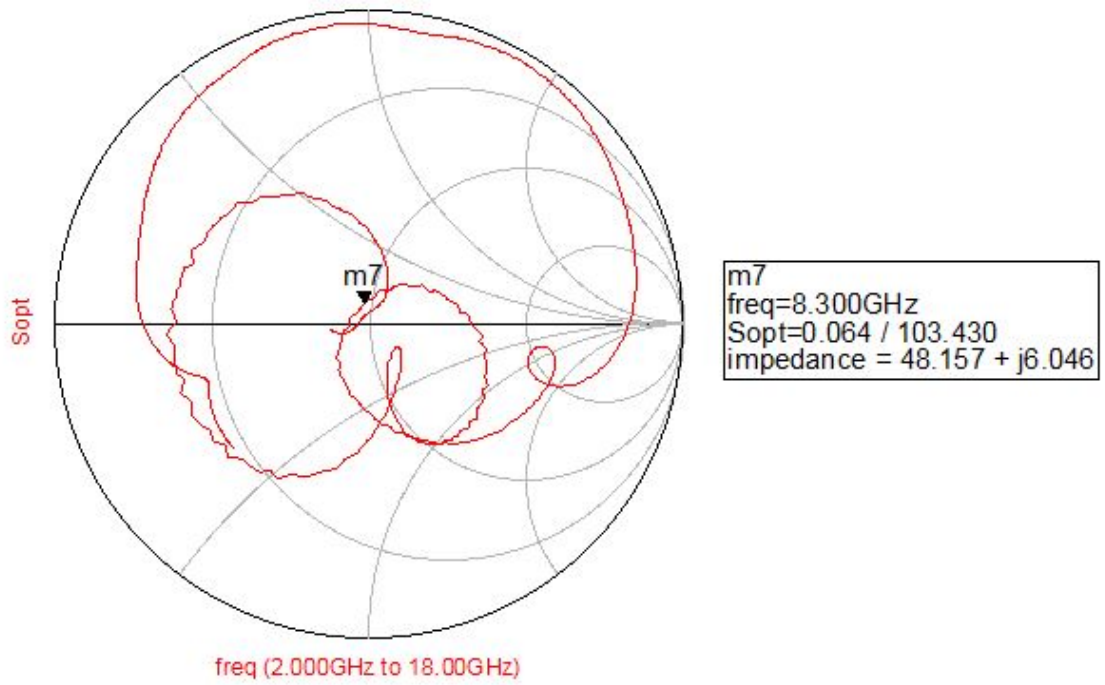


(a) Noise and gain circles with schematic simulation

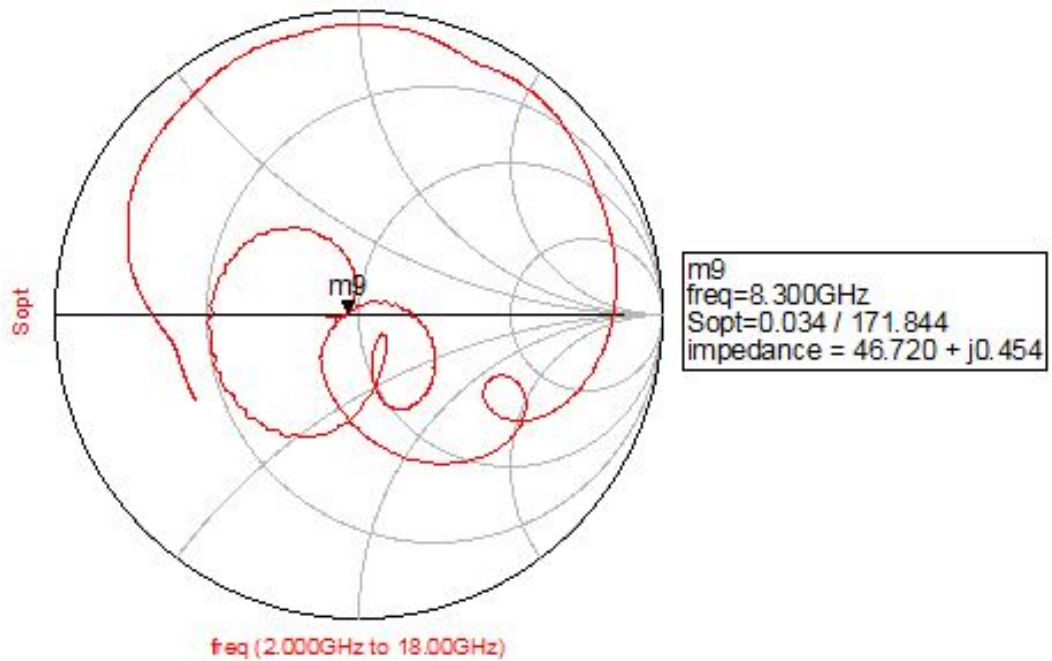


(b) Noise and gain circles with momentum simulation

Figure 3.21: Noise and gain circles



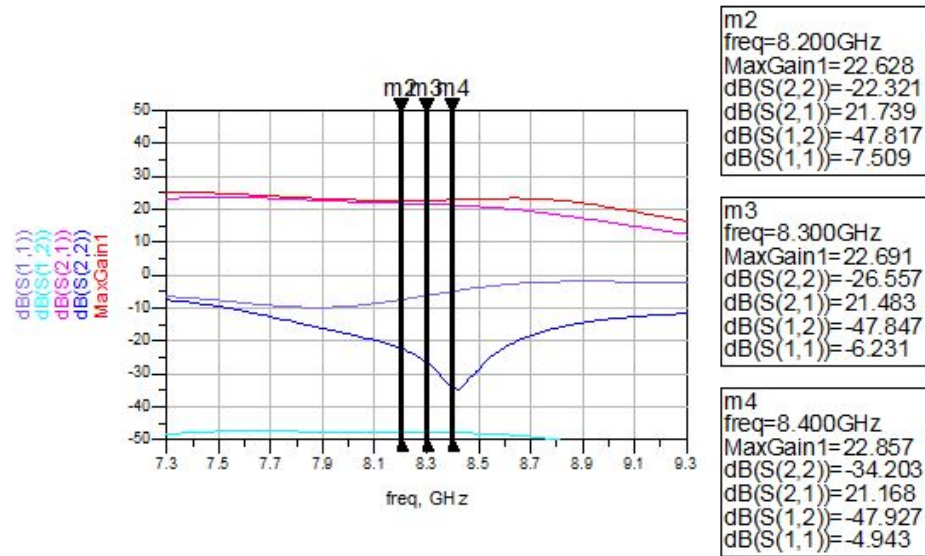
(a) Γ_{opt} with schematic simulation



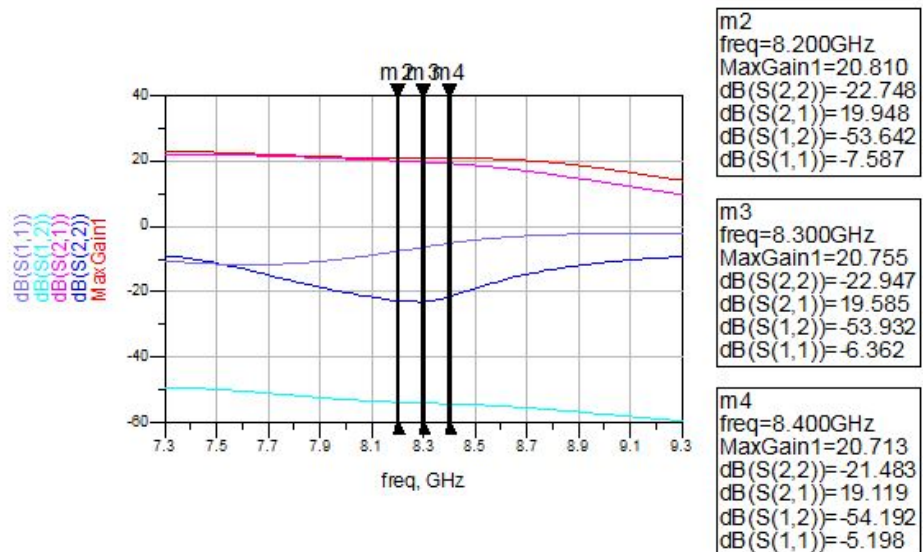
(b) Γ_{opt} with momentum simulation

Figure 3.22: Γ_{opt}

S-Parameters and Noise Figure schematic and momentum simulation results are given in Figure 3.23 and Figure 3.24

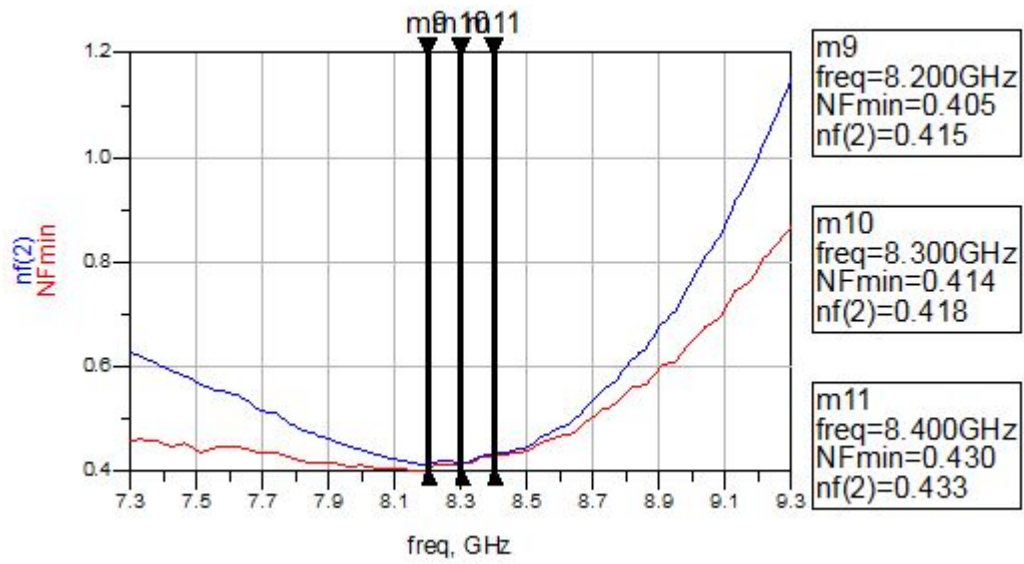


(a) S-Parameters with schematic simulation

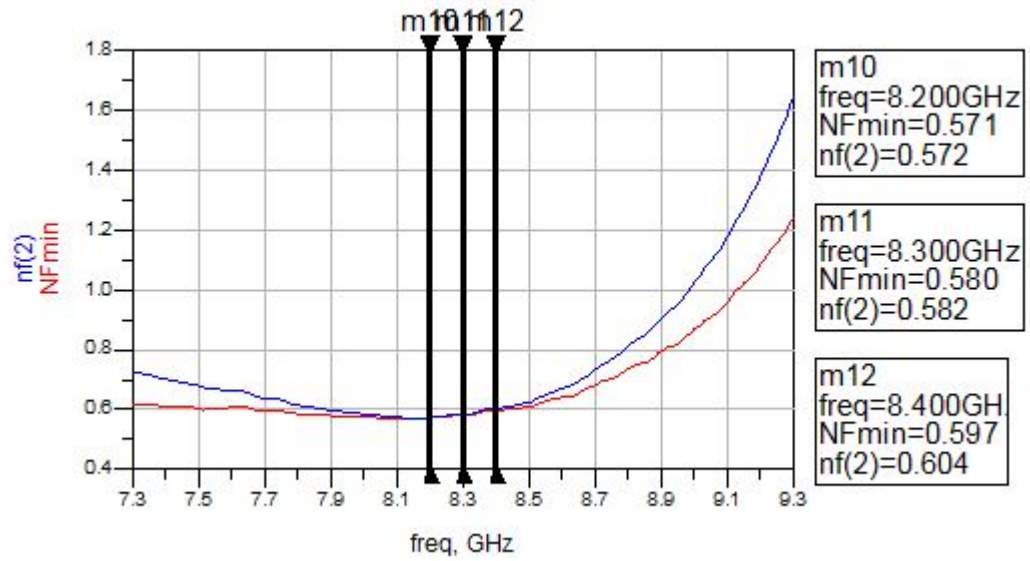


(b) S-Parameters with momentum simulation

Figure 3.23: S-Parameters



(a) Noise figure with schematic simulation



(b) Noise figure with momentum simulation

Figure 3.24: Noise figure

3.5.3 Intermediate Stage Matching

For intermediate stage matching, conjugate matching is used. Firstly, S_{22} of the one stage LNA is found by simulation and is shown in Figure 3.25. S_{11} of the second stage for two stage LNA is designed as the conjugate of the S_{22} of the one stage LNA which can be seen at Figure 3.26. There is capacitor, 10 pF in series, between two stages because of isolation bias between two stages.

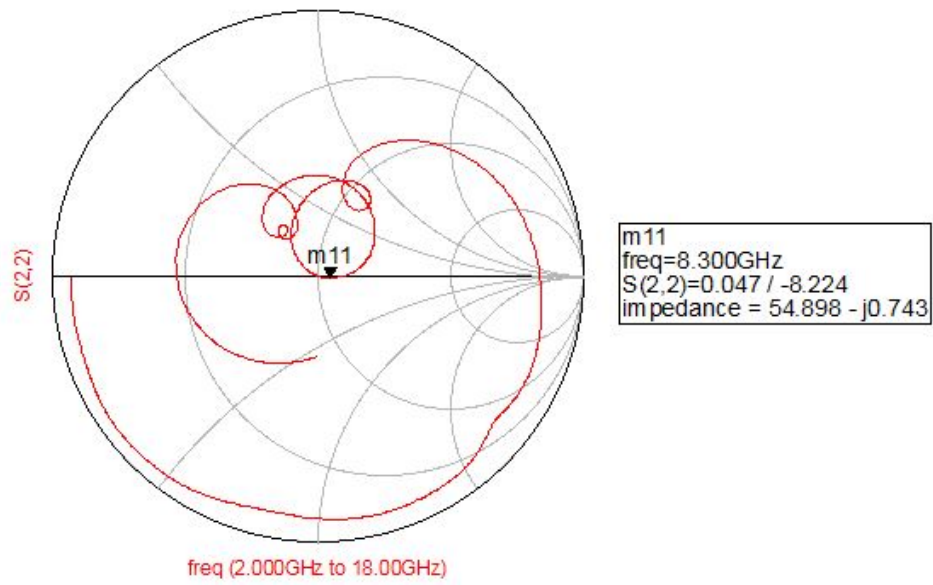


Figure 3.25: S22 of the one stage LNA

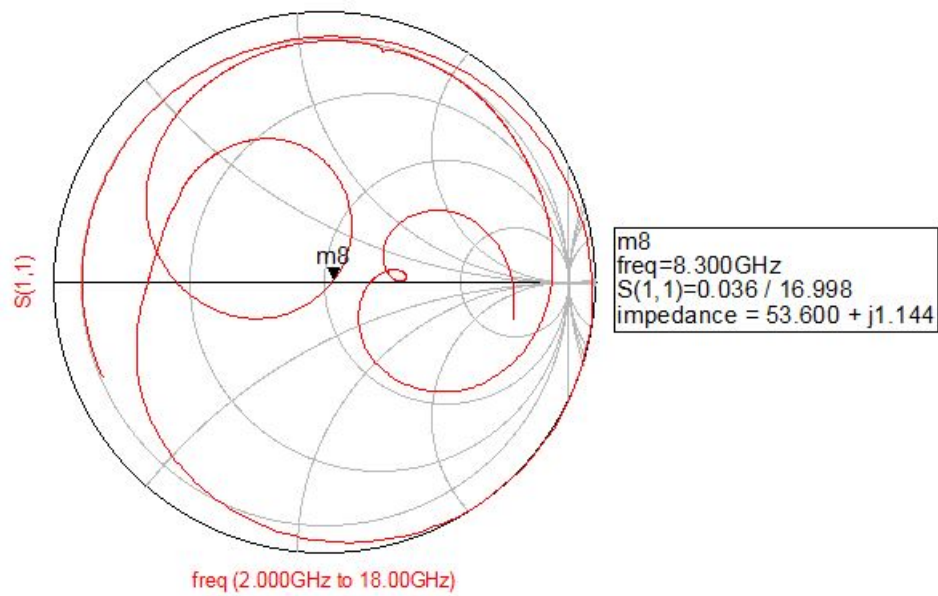
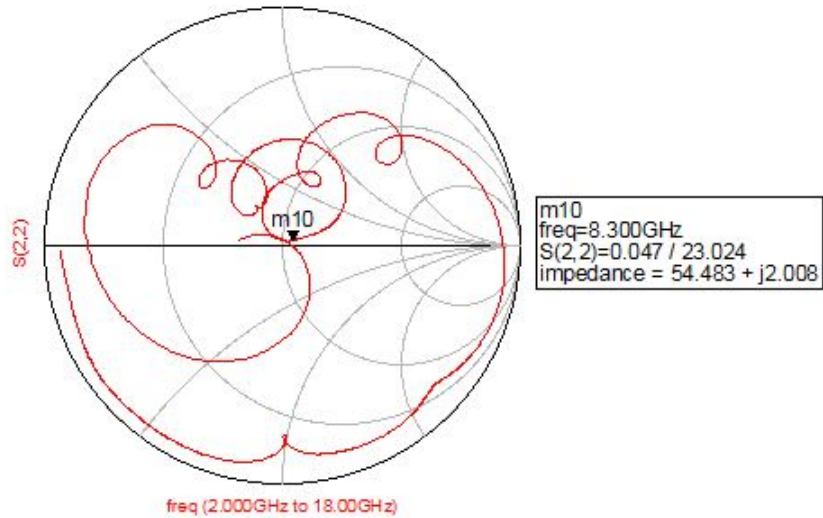


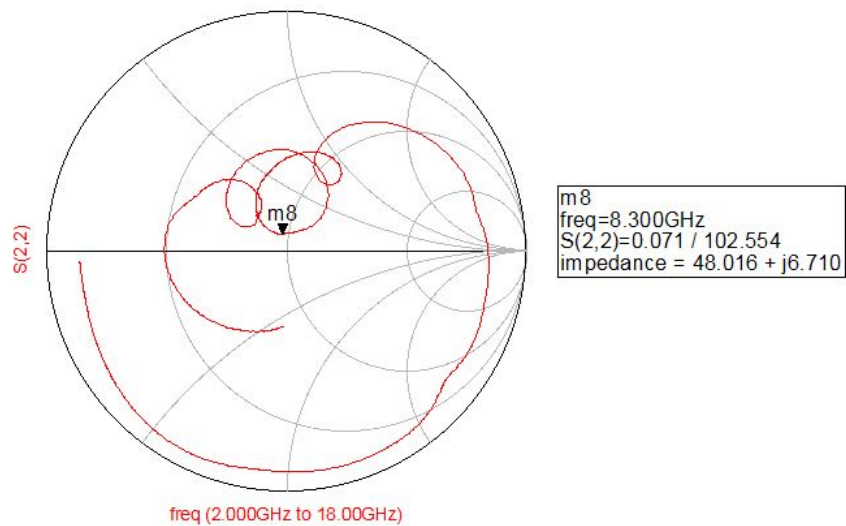
Figure 3.26: S11 of the second stage of the two stage LNA

3.5.4 Output Matching

The output match of the second stage is designed as conjugate match. In Figure 3.27, $S(2,2)$ of two stage LNA design simulations are given.



(a) $S(2,2)$ with schematic simulation

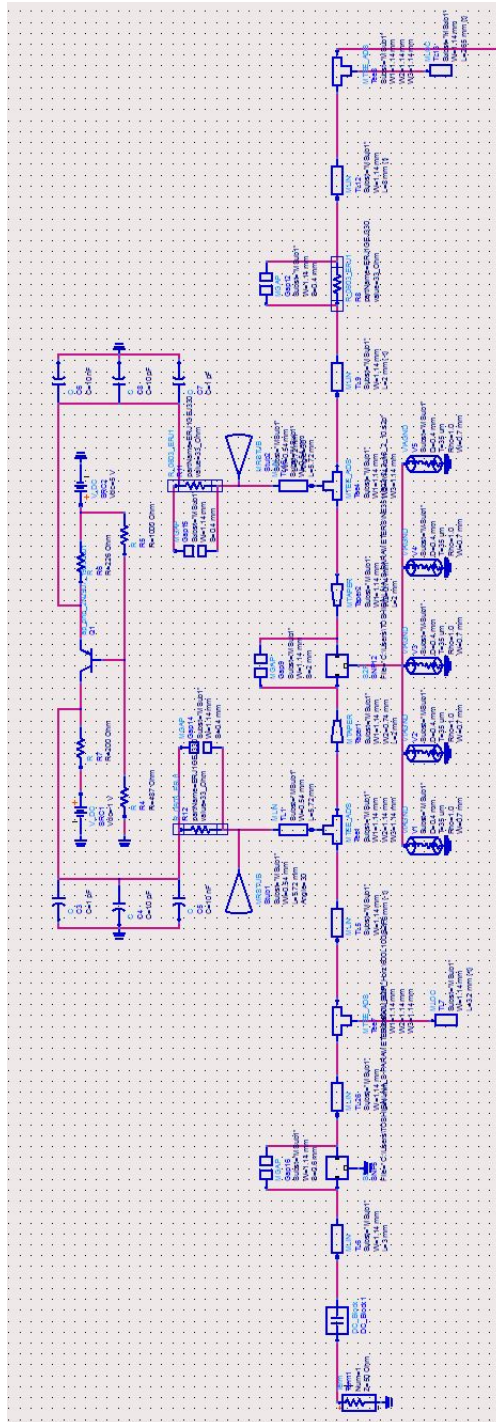


(b) $S(2,2)$ with momentum simulation

Figure 3.27: $S(2,2)$

3.5.5 Final Design and Printed Circuit Board Layout

Figure 3.28 are design of schematic simulation tool, Figure 3.29 and Figure 3.30 are design of momentum simulation tool in ADS. PCB Layout is as shown in Figure 3.31.



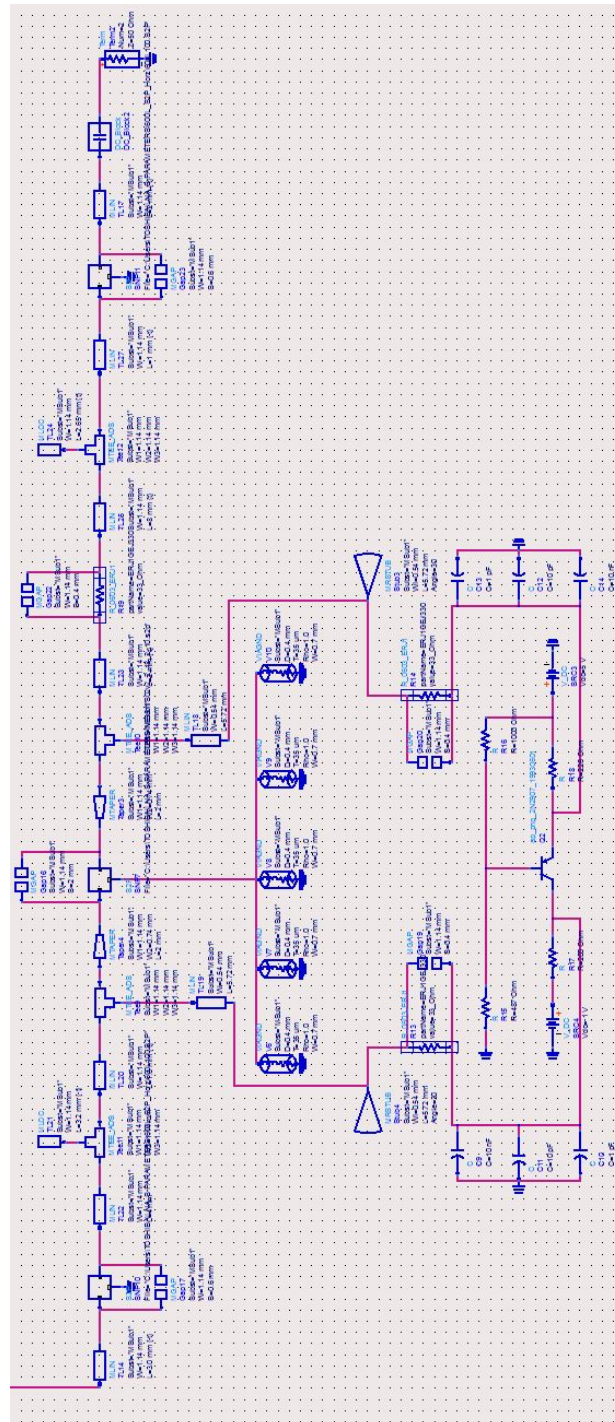


Figure 3.28: Two stage final design of schematic simulation

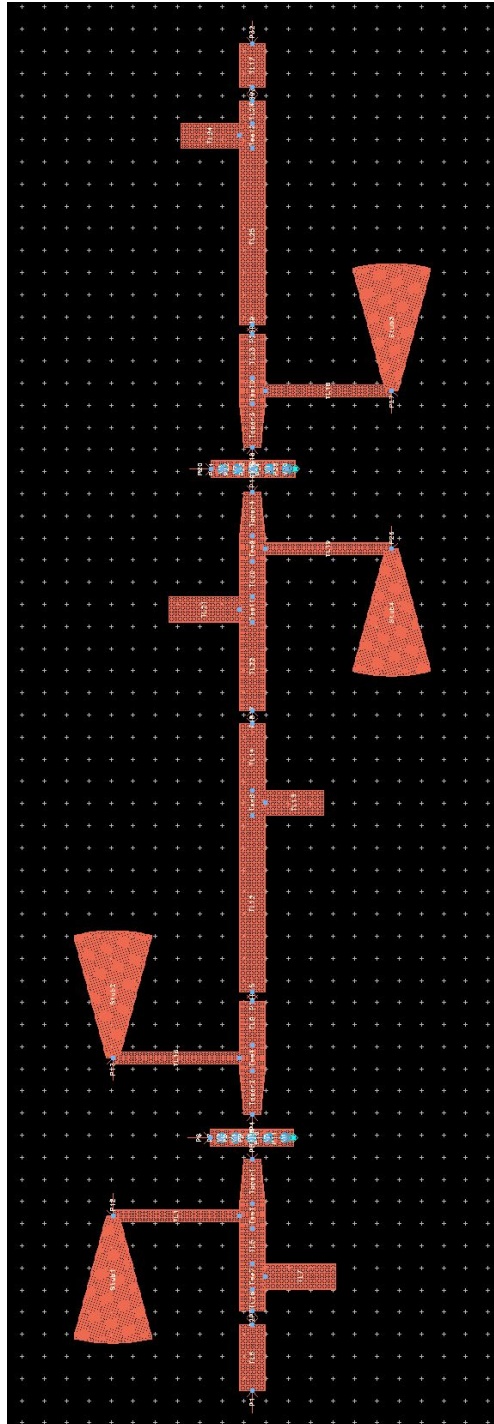


Figure 3.29: Two stage layout in momentum simulation

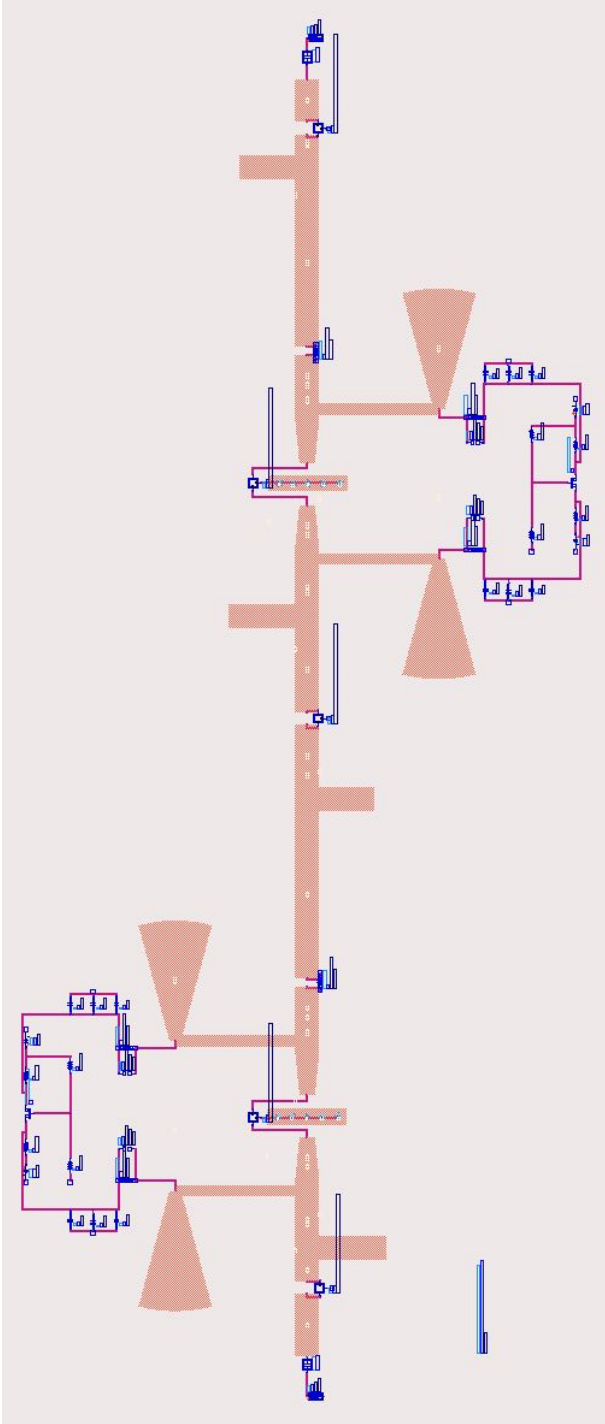


Figure 3.30: Two stage final design of momentum simulation

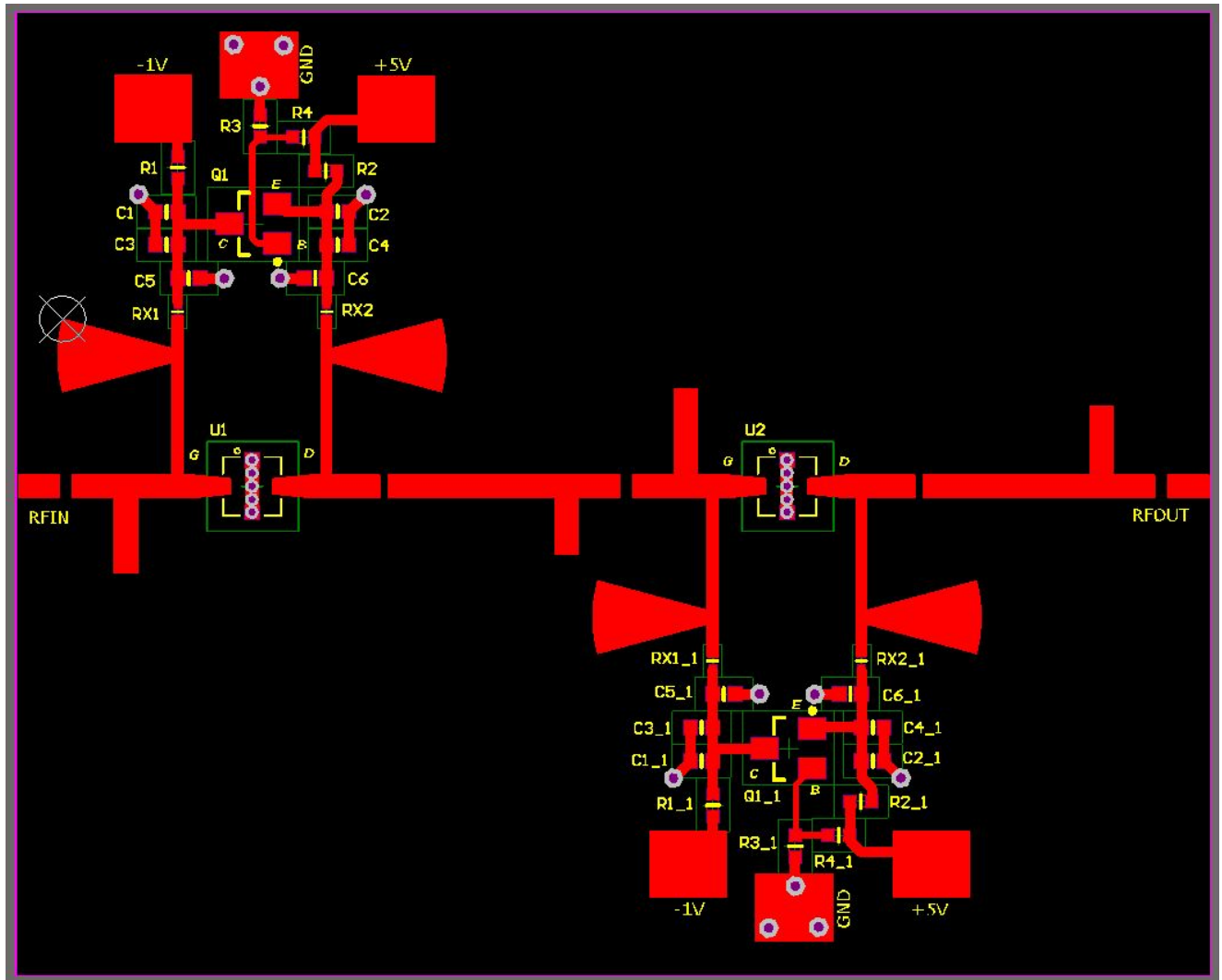


Figure 3.31: Two stage PCB design

Chapter 4

Measurement Results and Comparison with Simulation Results

One stage and two stage X-Band LNA designs are fabricated as shown in Figure 4.1 and Figure 4.2. Because the substrates are too thin, to avoid bending the PCB and also to measure noise figures more reliably, circuits are packaged in RF tight boxes.

Both one stage and two stage LNA's are biased using 5 V positive and -1 V negative supply voltages. The active bias circuits are based the transistors to approximately 10 mA with gate voltages nearly -0.5 V.

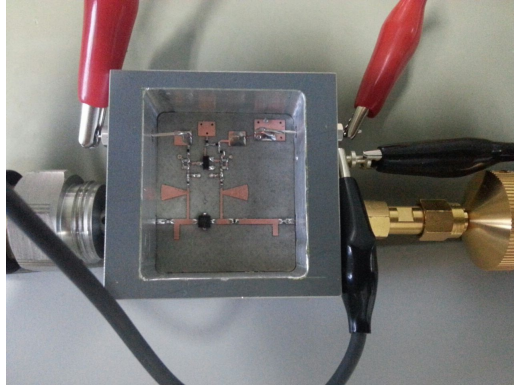


Figure 4.1: One stage LNA design

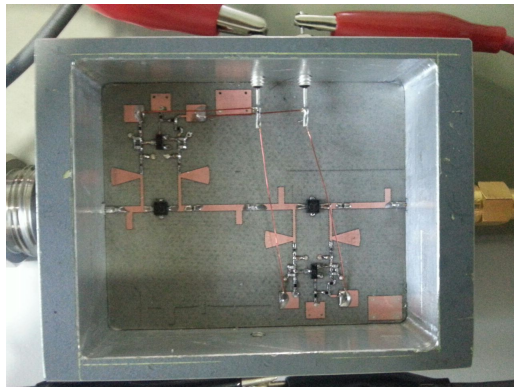


Figure 4.2: Two stage LNA design

4.1 S-Parameter Measurements and Simulation Comparison

S-Parameter measurement is done with Agilent PNA N5222A Network Analyzer. Because the amplifier is a low noise amplifier, the stimulus power is given as -50 dBm at first; however, although the calibration is done with respect to -50 dBm, the results have a lot of noise on them. Then the stimulus power is increased to -30 dBm; therefore, the results had much lower noise and the amplifier was still working in the linear region.

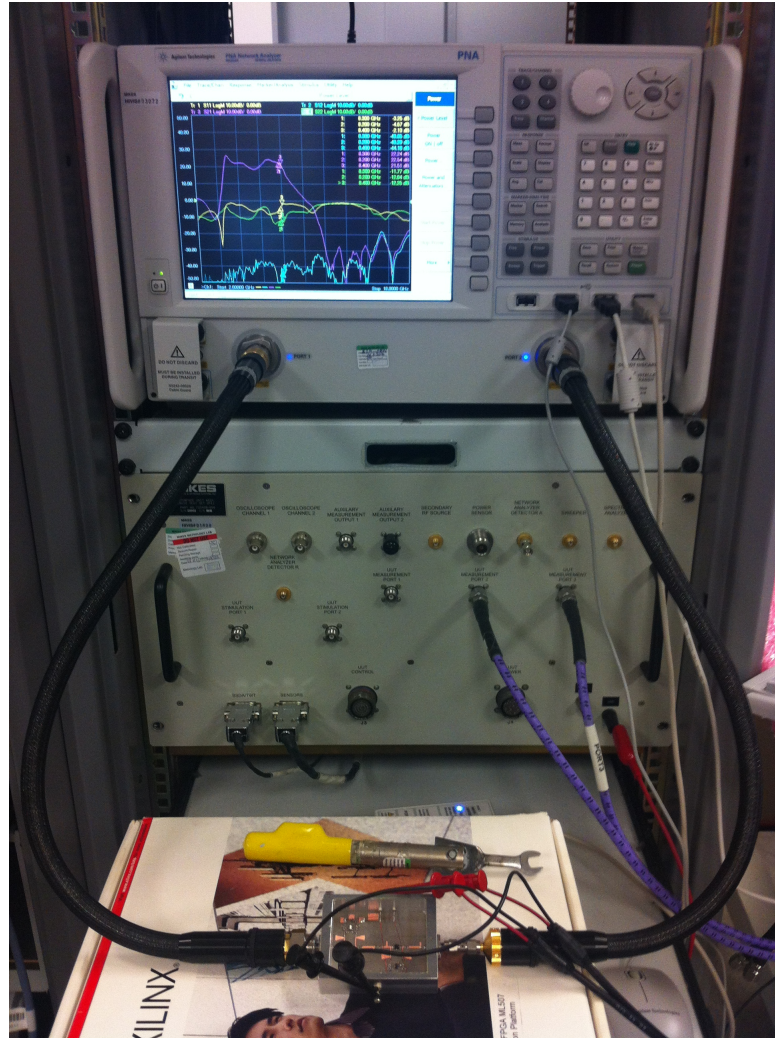
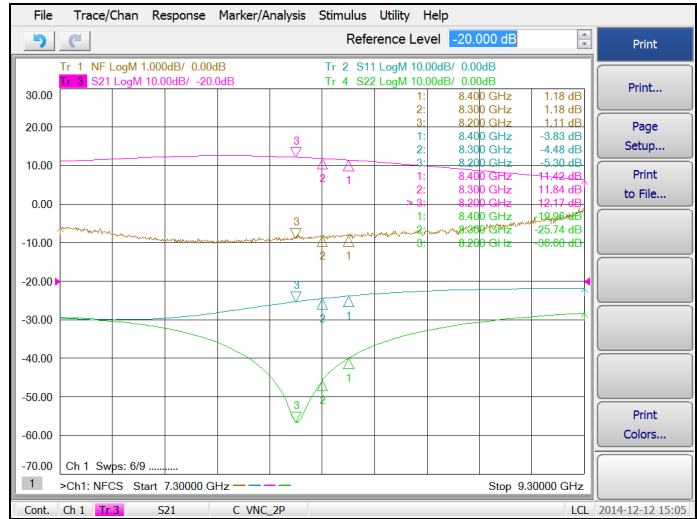


Figure 4.3: S-Parameter measurement setup

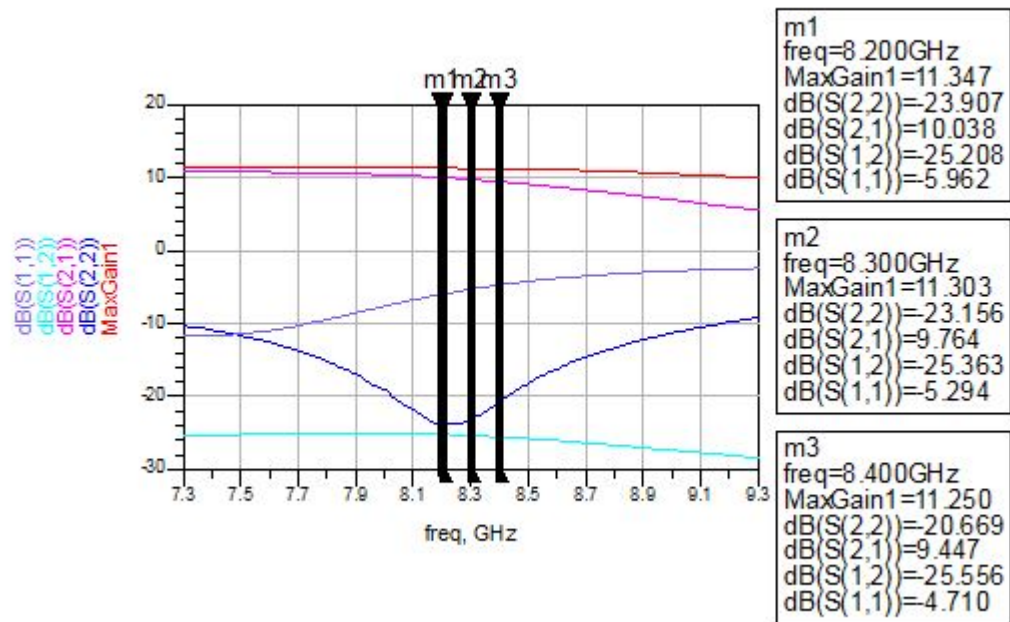
In Figure 4.4 and Figure 4.5, S_{11} , S_{12} , S_{21} and S_{22} are shown with color codes in frequency band. Measured and simulated S-Parameters are similar. Of course the results are not exactly same because in fabricated board realization of PCB, connectors and packaging affect the result of measurements.

4.1.1 One Stage LNA Design

S-Parameters measurement with simulation data is compared in Figure 4.4.



(a) Measured S-Parameters

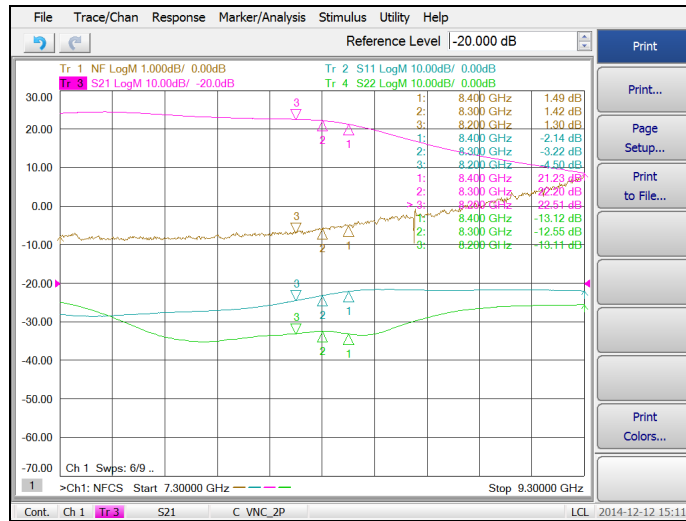


(b) Simulated S-Parameters

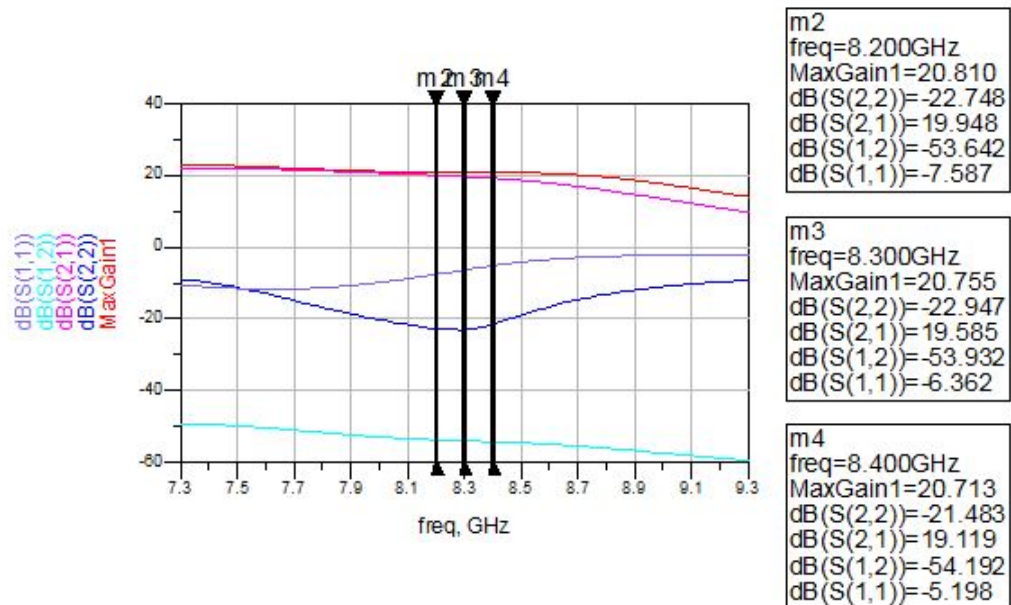
Figure 4.4: Comparisons of simulated and measured S-Parameters of one stage LNA

4.1.2 Two Stage LNA Design

For two stage of circuit design, S-Parameters measurement and simulation data are compared in Figure 4.5.



(a) Measured S-Parameters



(b) Simulated S-Parameters

Figure 4.5: Comparisons of simulated and measured S-Parameters of two stage LNA

4.2 Noise Figure Measurements and Simulation Comparison

To measure noise figure of the circuits, both Y-Factor Method and Cold Source Method need calibration before measurements. As mentioned in Chapter3, the cold source method is more precise than the Y-Factor method. As seen from the measured results, the noise figure measured with cold source method is lower than the one measured with the Y-factor method.

4.2.1 Cold Source Method

Noise Figure measurement with Cold Source Method is done with Keysight PNA-X N5242A Network Analyzer. The frequency range is set to 7.3 GHz - 9.3 GHz. Figure 4.6 illustrates cold source method NF setup.

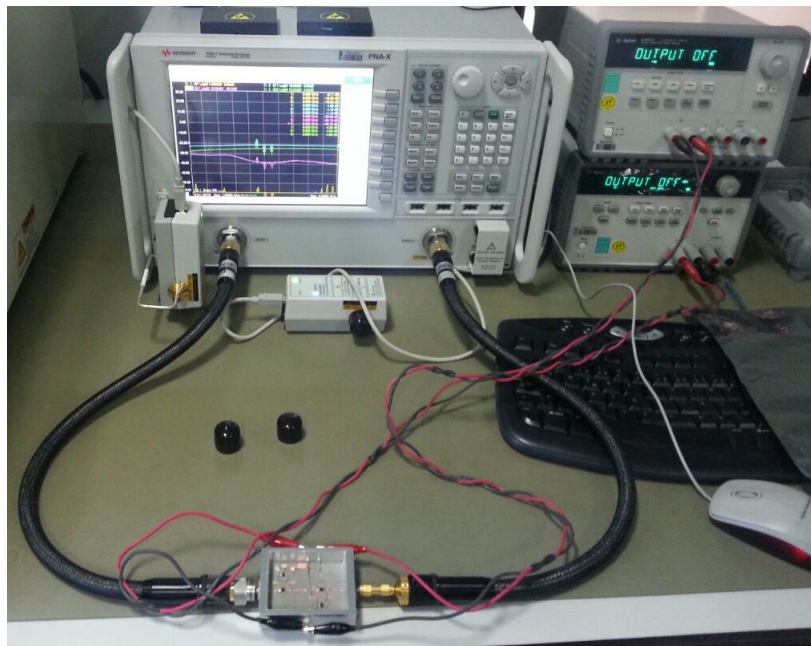
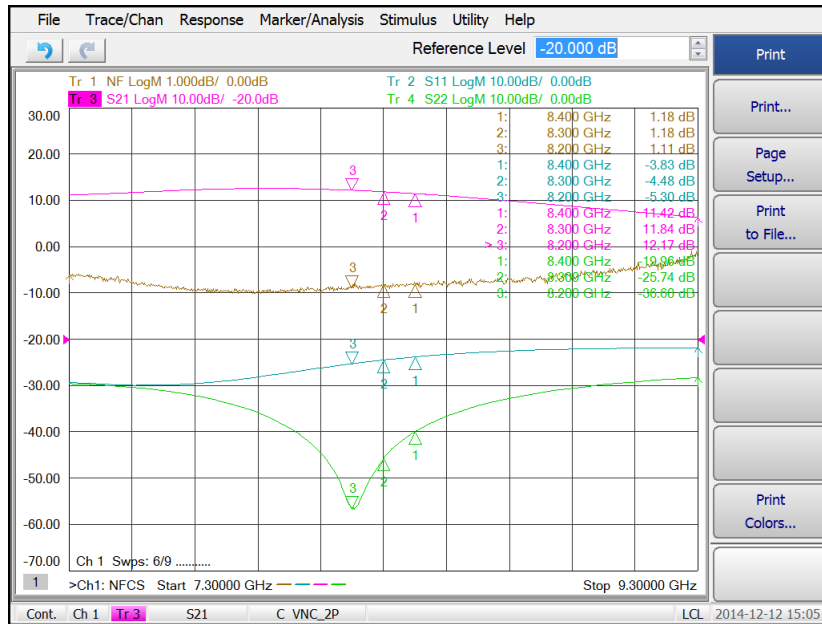


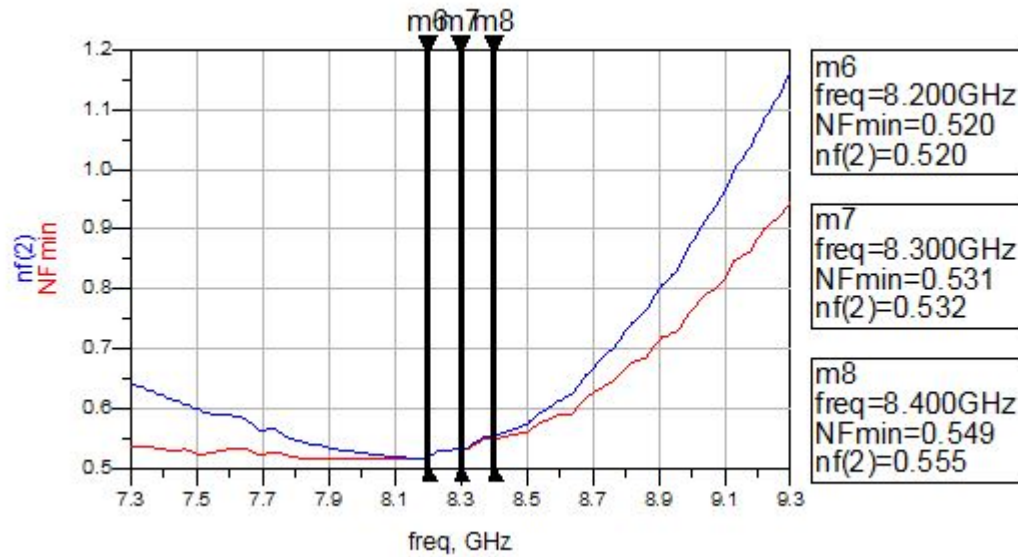
Figure 4.6: NF measurement setup with cold source method

The measurement and simulated results are slightly different from each other for both one stage and two stage LNA designs, probably due to the adapter between output connector of the circuit and output port cable. Also input connector increase the noise figure because of attenuation. In Figure 4.7 and Figure 4.8 illustrates the simulated and measured results.

4.2.1.1 One Stage LNA Design



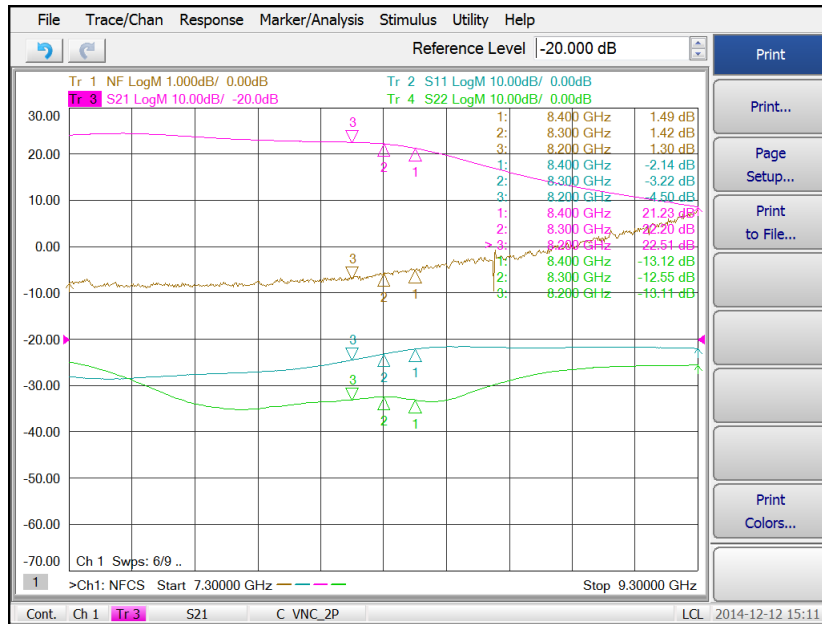
(a) Measured noise figure



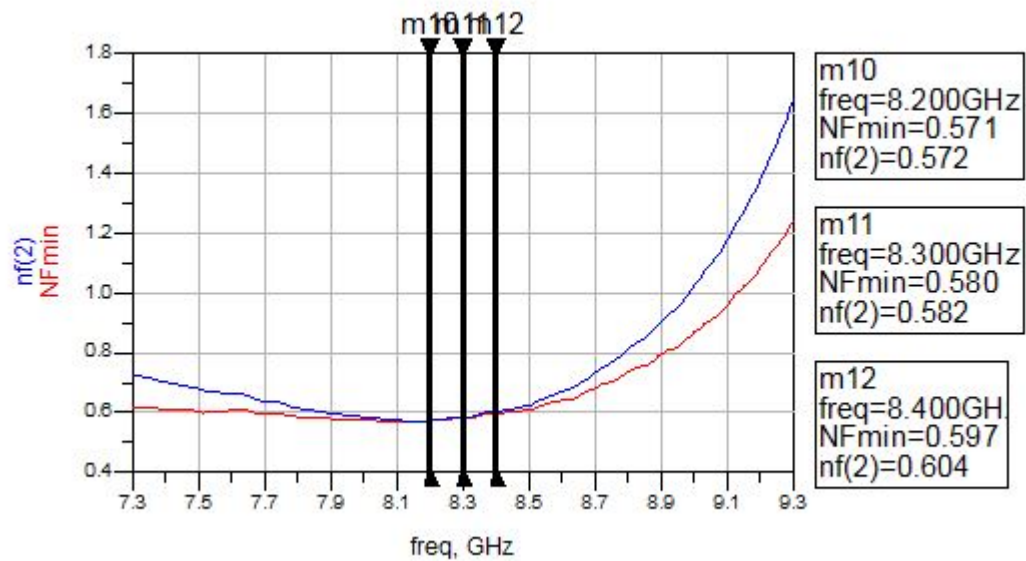
(b) Simulated noise figure

Figure 4.7: Comparisons of simulated and measured NF of one stage LNA

4.2.1.2 Two Stage LNA Design



(a) Measured noise figure



(b) Simulated noise figure

Figure 4.8: Comparisons of simulated and measured NF of two stage LNA

4.2.2 Y-Factor Method

Noise Figure measurement with Y-Factor Method is done with Agilent E4446A spectrum analyzer and noise source. Measurement is done in frequency range 7.3 GHz - 9.3 GHz to see obviously. Figure 4.9 illustrates noise figure measurement setup with Y-Factor method.

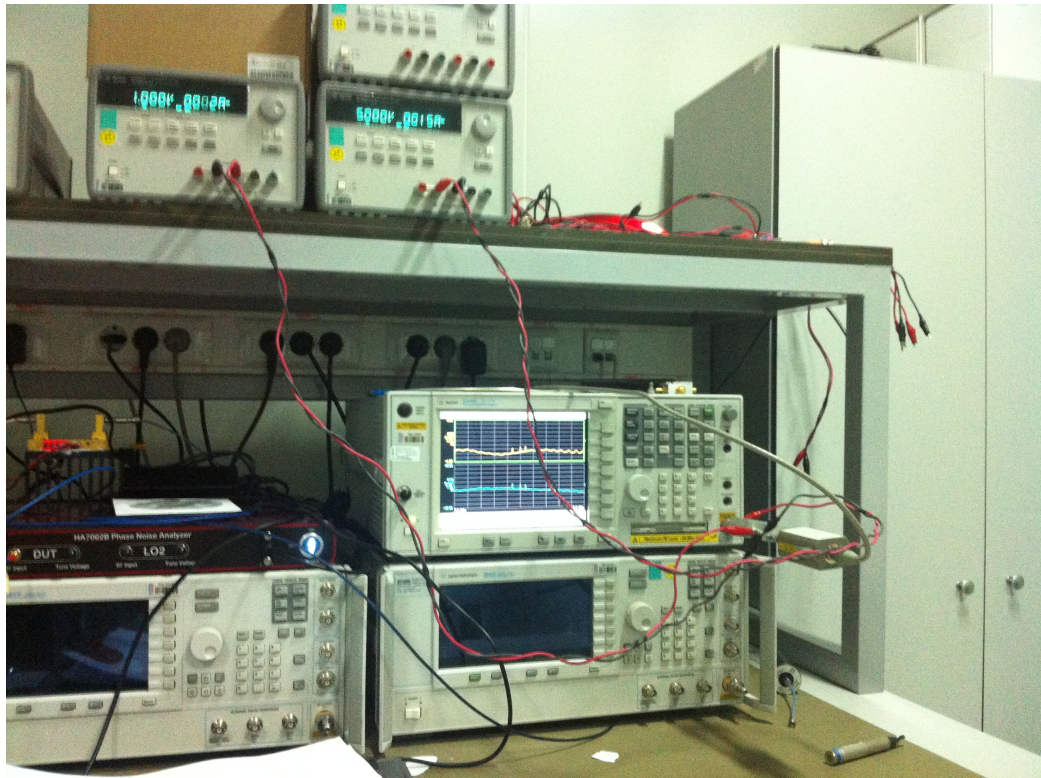


Figure 4.9: NF measurement setup with Y-Factor method

After entering ENR values of the noise source which is shown in Figure 4.10 to the spectrum analyzer, the noise source is connected to the spectrum analyzer as through to calibrate. The calibrated noise figure data is given in Figure 4.11.

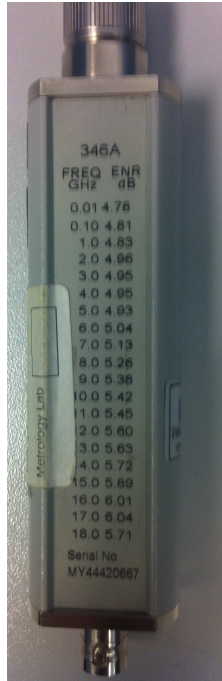


Figure 4.10: ENR values of noise source

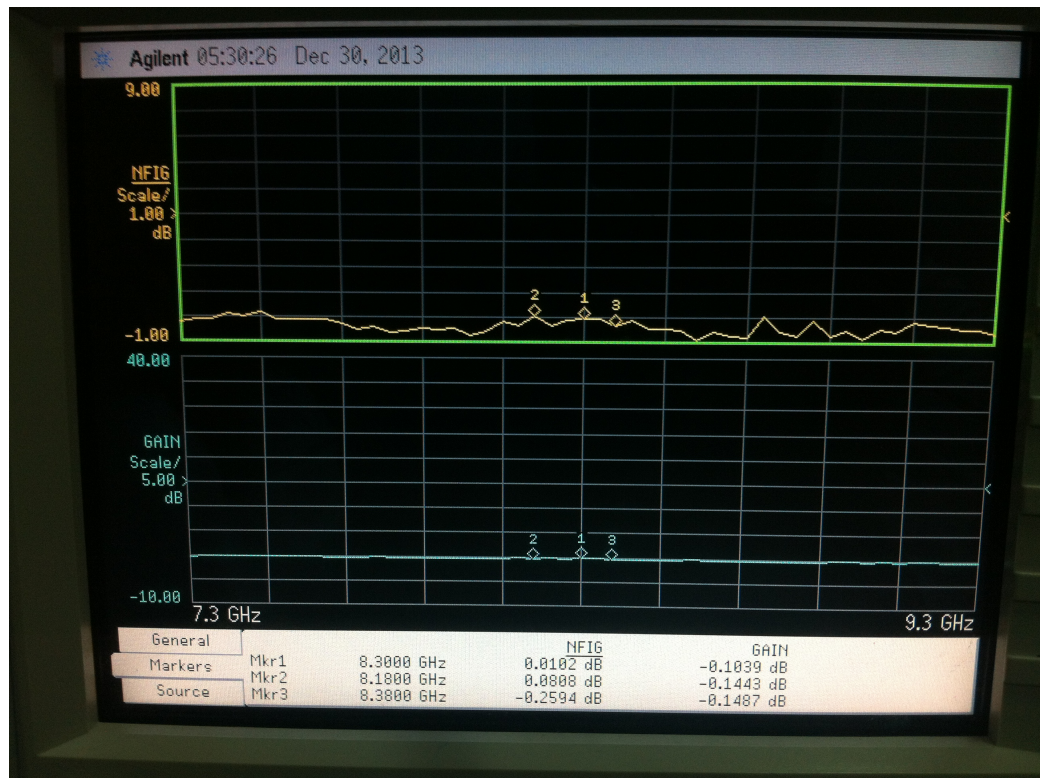
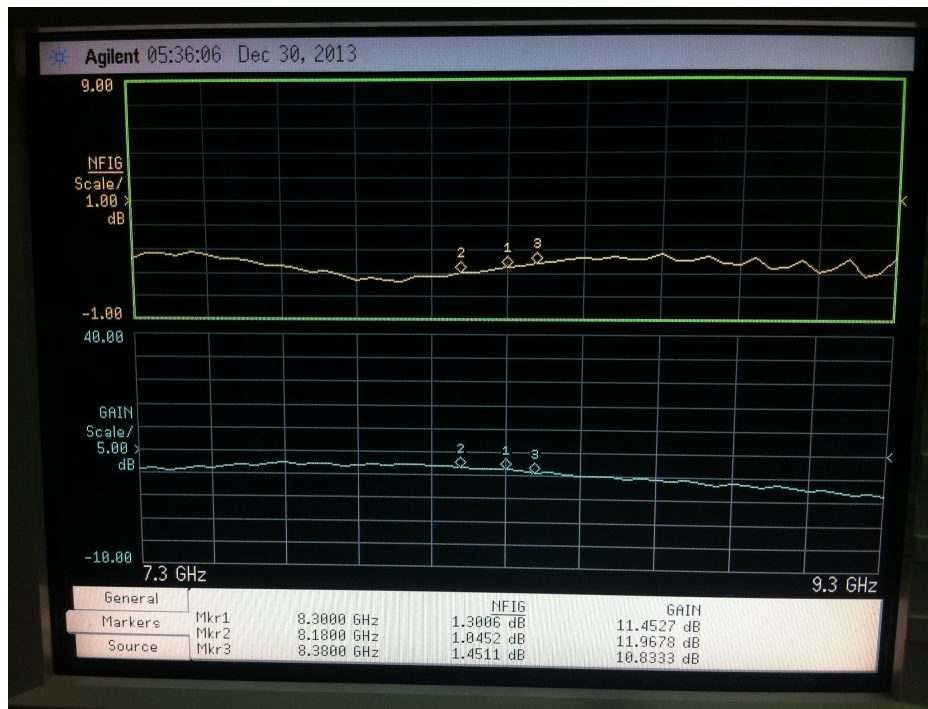


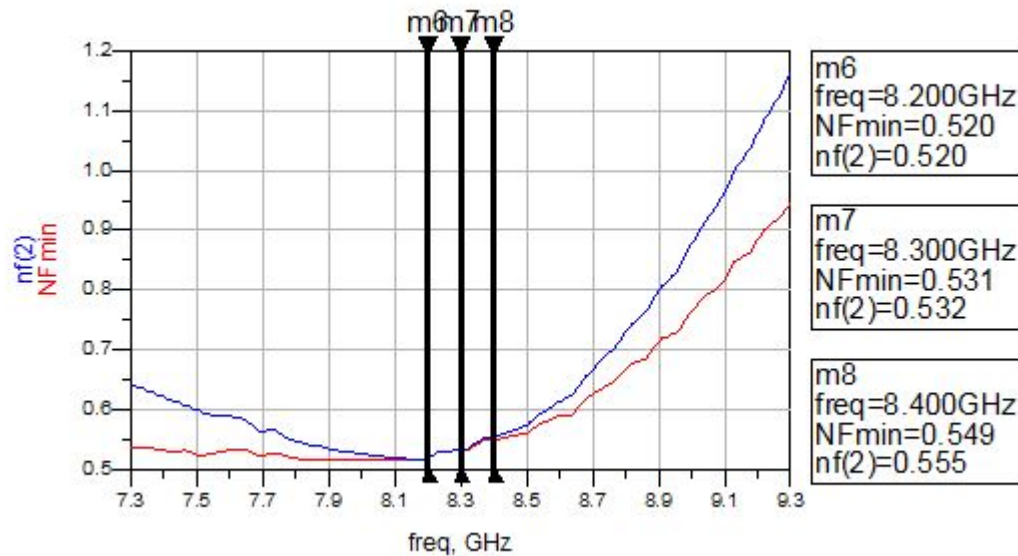
Figure 4.11: Calibrated noise figure data

4.2.2.1 One Stage LNA Design

As seen from Figure 4.12, the results are slightly different from each other. Adaptors between noise source and input of the amplifier are added measured result. Also, input connector of the amplifier is added as a noise in this measurement. Measurements are done also with lid closed as in Figure 4.13.



(a) Measured noise figure



(b) Simulated noise figure

Figure 4.12: Comparisons of simulated and measured NF of one stage LNA

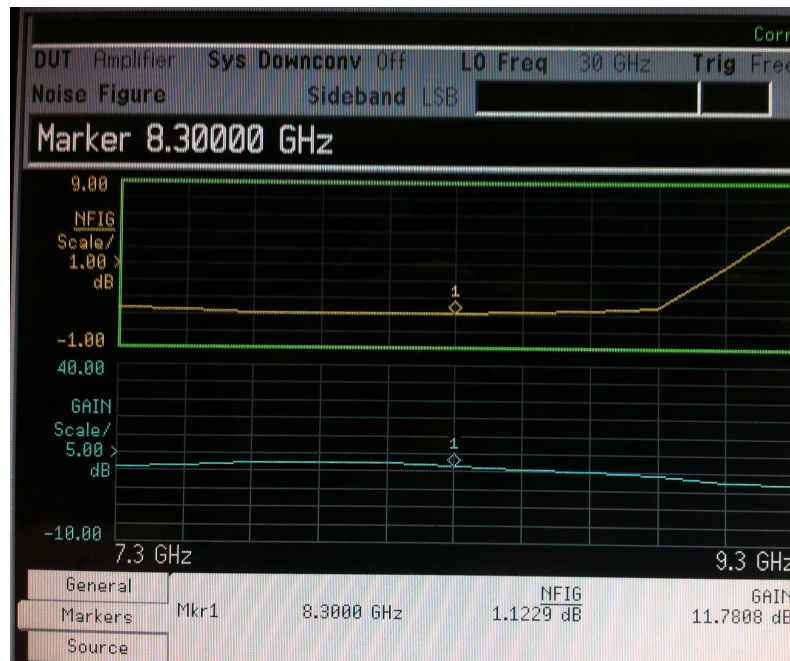
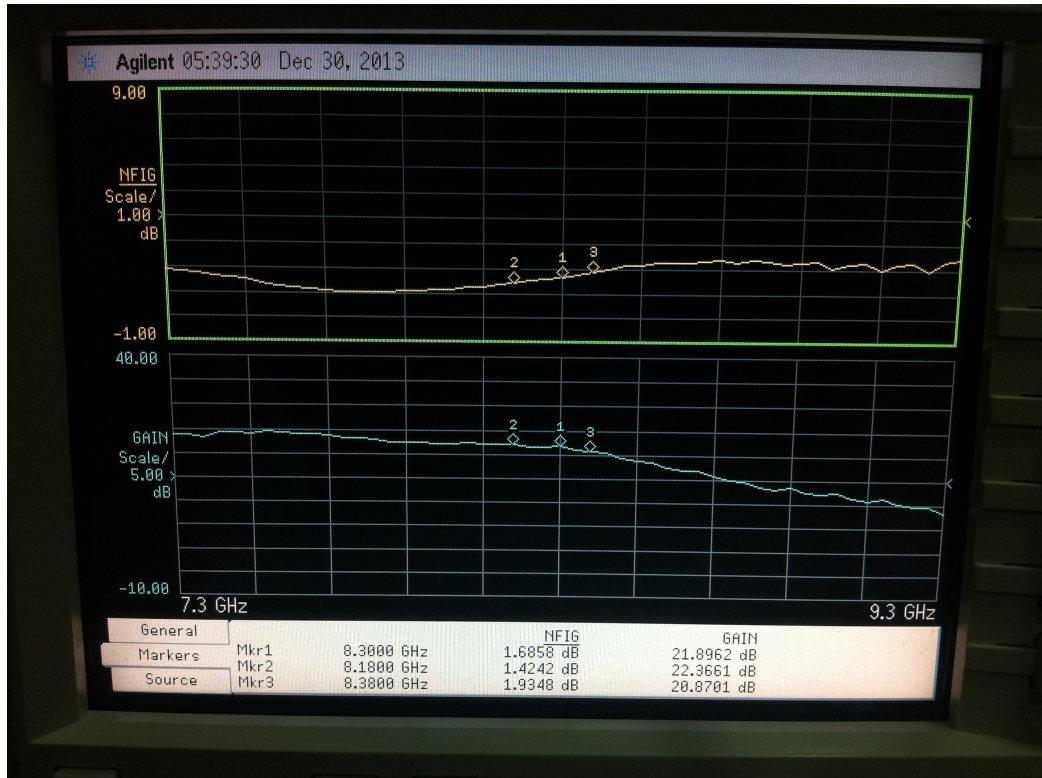


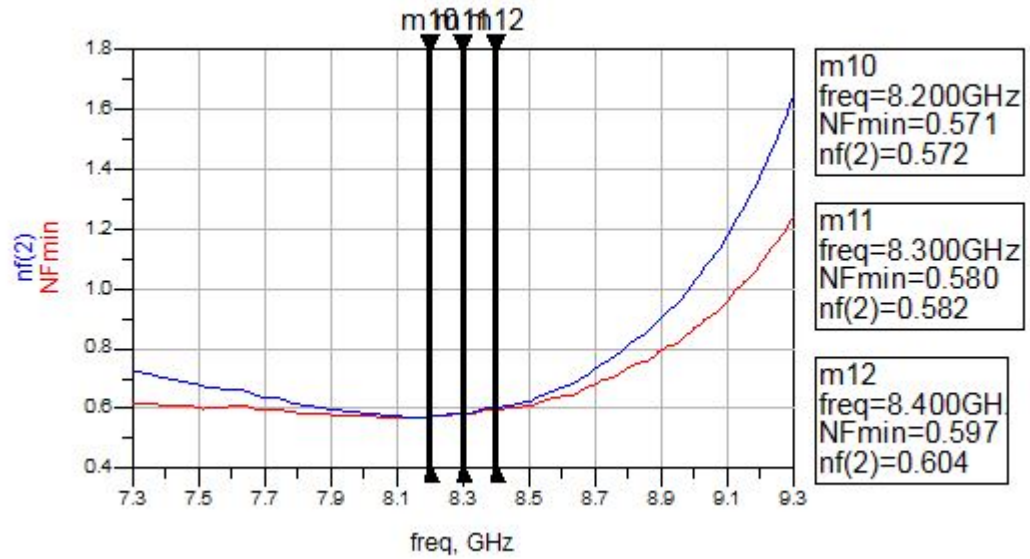
Figure 4.13: NF measurement with lid closed

4.2.2.2 Two Stage LNA Design

As seen from Figure 4.14, the results are quiet different from each other. Adaptors between noise source and input of the amplifier are added measured result. The input connector also contributes the overall noise of the amplifier as it also attenuates the signal. Measurements are done also with lid closed as in Figure 4.15.



(a) Measured noise figure



(b) Simulated noise figure

Figure 4.14: Comparisons of simulated and measured NF of two stage LNA



Figure 4.15: NF measurement with lid closed

4.3 IP3 Measurements

A two tone linearity test was done for intermodulation measurement. For this measurement, two signal generators, Agilent E8257D and Hewlett Packard 83731B and one spectrum analyzer E4446A, and one combiner are used. Two input signal in $f_1 = 8.275$ GHz and $f_2 = 8.325$ GHz frequencies are applied to the input of the amplifier using combiner. The cable losses and loss of combiner are normalized when applying the input power levels. The input power level of the circuit is -20 dBm when doing normalizations for one stage LNA. However, the input power level of the circuit is -30 dBm when doing normalizations for two stage LNA. Because the gain of the two stage LNA is greater than one stage LNA, to see intermodulation products exactly, the input power level of one stage LNA is greater. The amplitudes of two-tone intermodulation products at $(2f_1 - f_2) = 8.225$ GHz and $(2f_2 - f_1) = 8.325$ GHz frequencies appear closest to f_1 and f_2 . Because the transistor do not have non-linear model, simulations could not be done, only measured.

4.3.0.3 One Stage LNA Design

The signal generators are set to the same level and the output levels at the output end of the cables are calibrated. -14.10 dBm and -15.18 dBm are applied to input of the circuit. By combining these two signal, -20 dBm input power level is given from the input of the circuit as shown Figure 4.16 and Figure 4.17.



Figure 4.16: Input power level of first signal generator

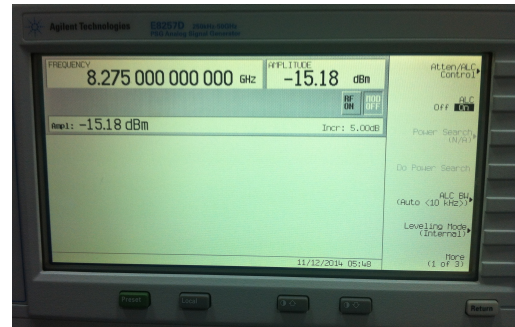


Figure 4.17: Input power level of second signal generator

The test set-up is shown in Figure 4.18.

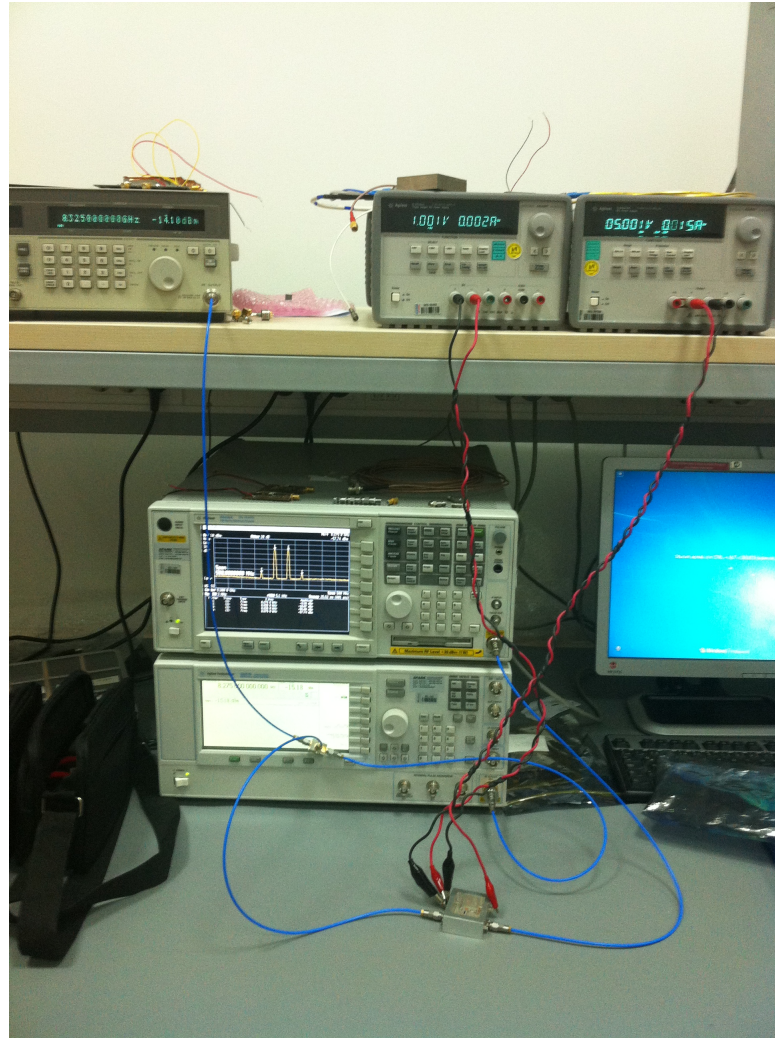


Figure 4.18: Setup of 2-Tone measurement of one stage LNA design

Two input signal levels in $f_1 = 8.275$ GHz and $f_2 = 8.325$ GHz frequencies and the amplitudes of two-tone intermodulation products at $(2f_1 - f_2) = 8.225$ GHz and $(2f_2 - f_1) = 8.375$ GHz frequencies are shown in Figure 4.19.

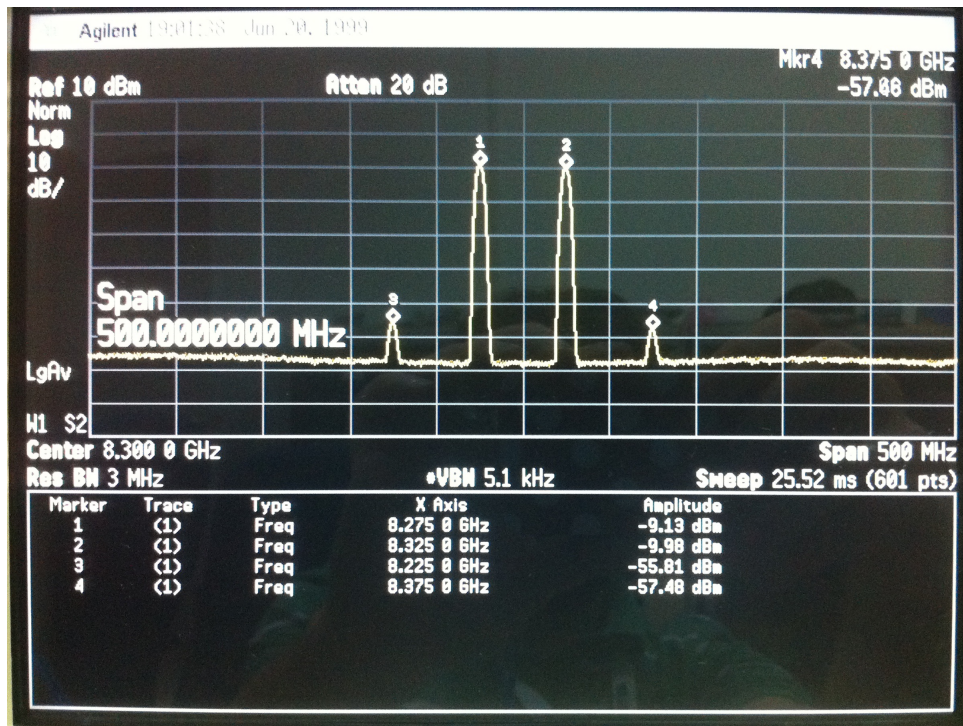


Figure 4.19: Two tone test of one stage LNA design

4.3.0.4 Two Stage LNA Design

The signal generators are set to the same level and the output levels at the output end of the cables are calibrated. -24.10 dBm and -25.18 dBm are applied to input of the circuit which is enough to see intermodulation products is given from the input of the circuit as shown Figure 4.20 and Figure 4.21.



Figure 4.20: Input power level of first signal generator

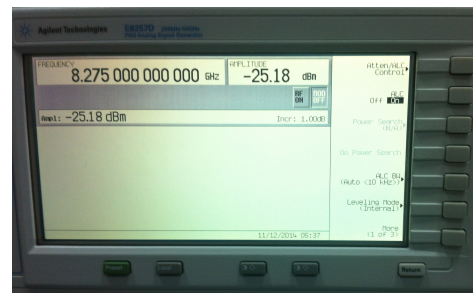


Figure 4.21: Input power level of second signal generator

The test set-up is shown in Figure 4.22.

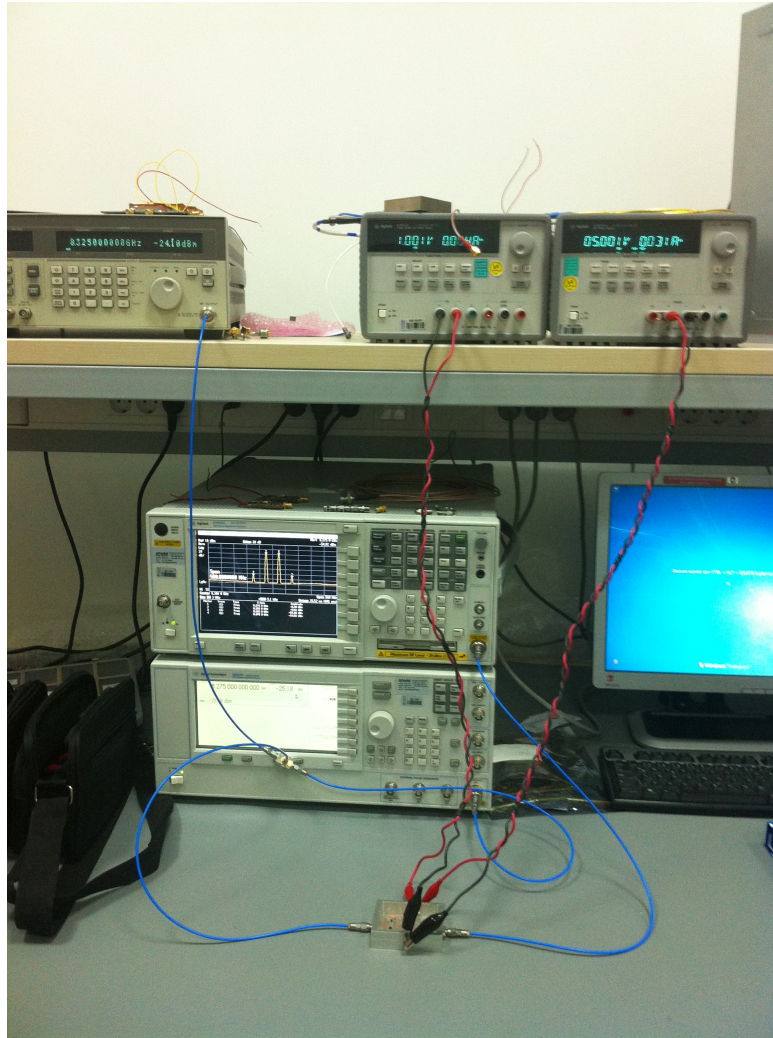


Figure 4.22: Setup of 2-Tone Measurement of two stage LNA design

When in $f_1 = 8.275$ GHz and $f_2 = 8.325$ GHz frequencies, these power levels are applied, the amplitudes of two-tone intermodulation products at $(2f_1 - f_2) = 8.225$ GHz and $(2f_2 - f_1) = 8.375$ GHz frequencies are shown in Figure 4.23.

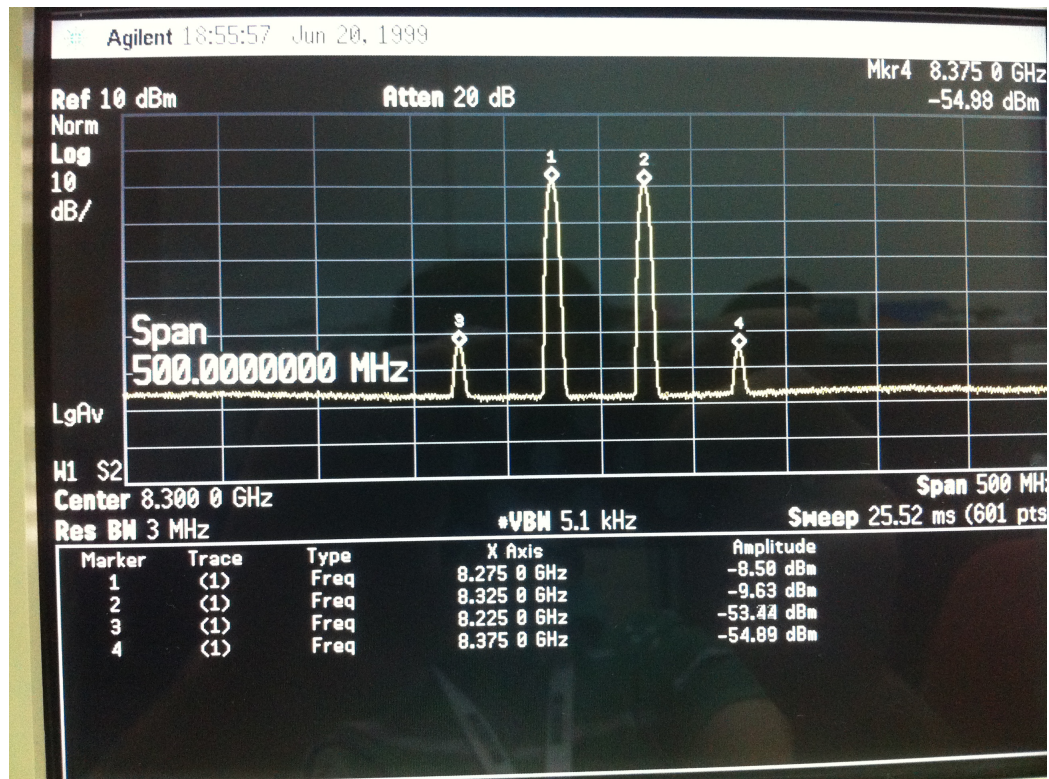


Figure 4.23: Two tone test of two stage LNA design

4.4 P1dB Measurements

To characterize large signal response of the amplifier, non-linear measurements are done. These measurement aims to find P1dB of the amplifier at center frequency, 8.3 GHz. Agilent E8257D signal generator and Agilent E4440A spectrum analyzer are used as equipment for this measurement. In Figure 4.24 and Figure 4.25 are shown by entering measured data in Matlab.

Input of the amplifiers is connected to the signal generator directly via an adaptor which has 0.5 dB loss. However, output of the amplifier is connected to the spectrum analyzer via cable with -2.3 dB cable loss in frequency band. Because the manufacturer of the transistor does not supply non-linear model, simulations could not be done, the circuit was only measured.

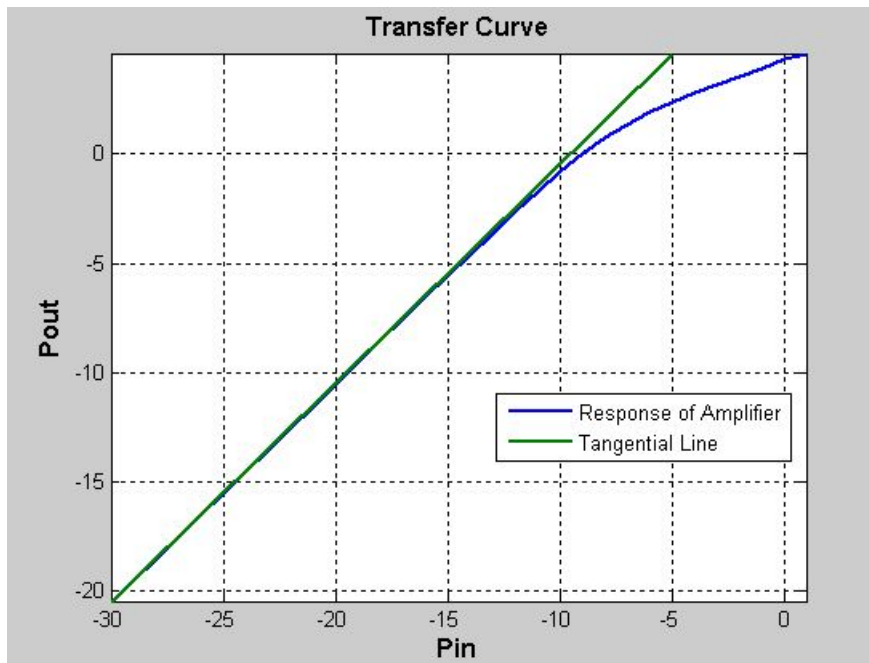


Figure 4.24: Transfer curve for one stage LNA

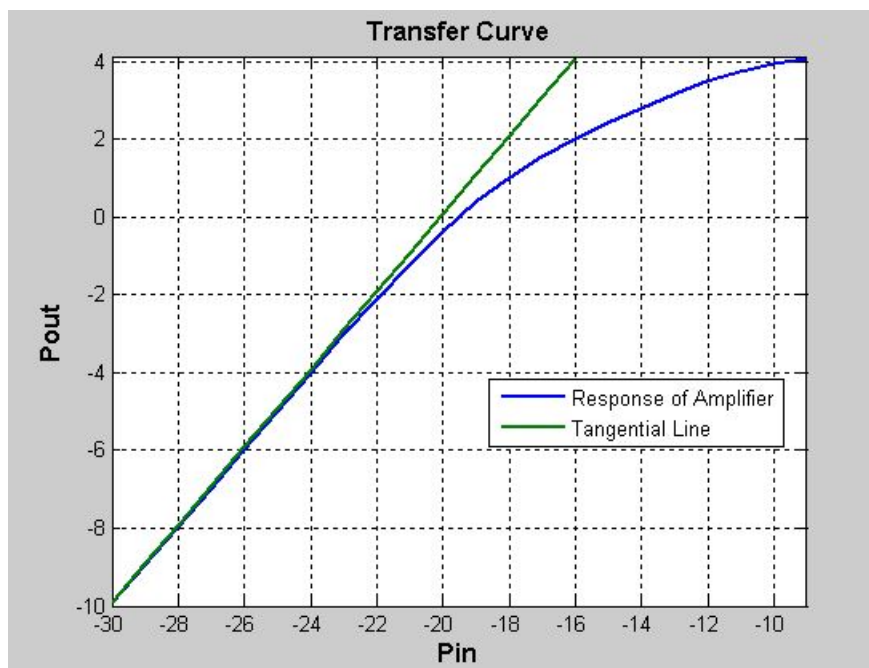


Figure 4.25: Transfer curve for two stage LNA

As seen from figures, for one stage amplifier, when input power level is -7 dBm, output power level is 1.37 where the output power level decrease 1 dB. Therefore, output P1dB point is 1.37 dB and cable loss at the output of the amplifier. It means that output P1dB is $OP1dB = 1.37dBm + 2.3dB = 3.67dBm$.

For two stage amplifier, when input power level is -18 dBm, output power level is 1.03 where the output power level decrease 1 dB. Therefore, output P1dB is $OP1dB = 1.03dBm + 2.3dB = 3.33dBm$.

4.5 Harmonics Measurements

In harmonic measurements, input signal is given as -30 dBm, to see more obviously harmonics of both one stage and two stage LNA. Agilent E8257D signal generator and Agilent E4440A spectrum analyzer are used as equipment for this measurement. Input signal is given in center frequency, 8.3 GHz as -30 dBm. Therefore, fundamental signal appears in 8.3 GHz, second harmonic signal appears in 16.6 GHz frequency. In Figure 4.26, frequency and amplitude setup is shown. As the manufacturer of NE3511S02 does not supply non-linear model of the transistor, simulations could not be done, the circuit was only measured.

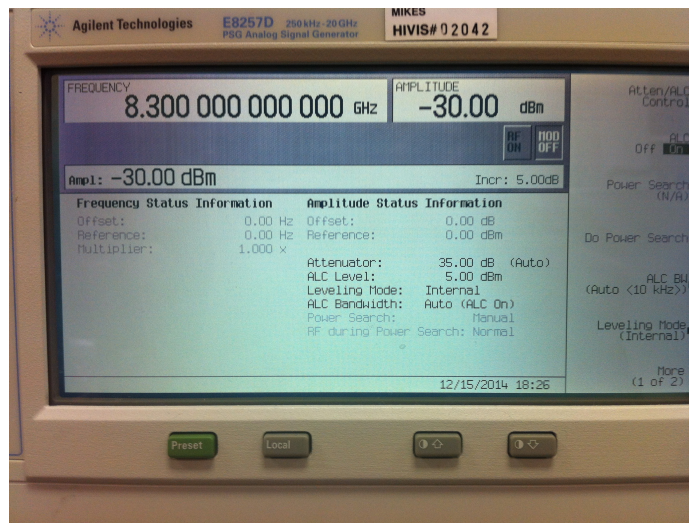
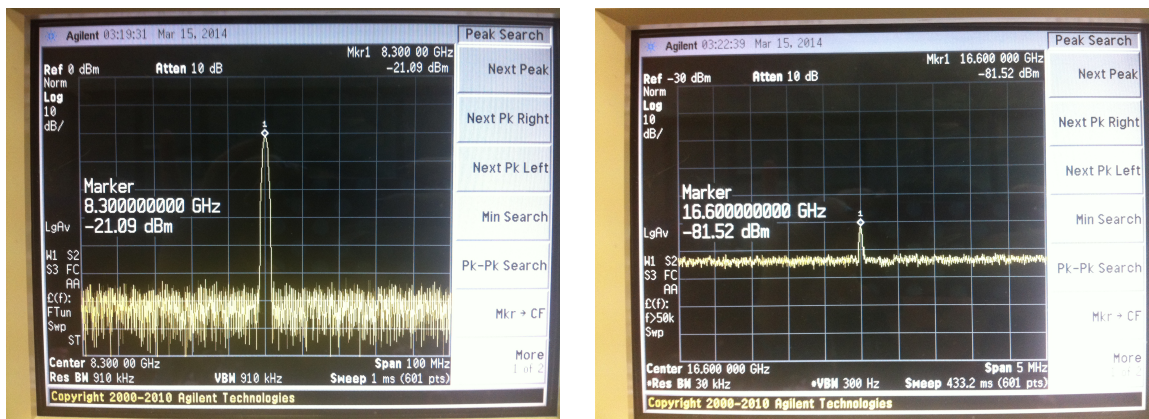


Figure 4.26: Input signal power for harmonic test

4.5.0.5 One Stage LNA Design

As the gain of the one stage amplifier is not much high as, -30 dBm is applied as the input signal level. If the input signal level was given less than -30 dBm, second harmonic could not have seen clearly because of noise floor. Therefore, to see more clearly second harmonic level, -30 dBm input power is applied to the circuit. In Figure 4.27 is illustrates fundamental signal and its second harmonic for one stage LNA.



(a) Fundamental signal

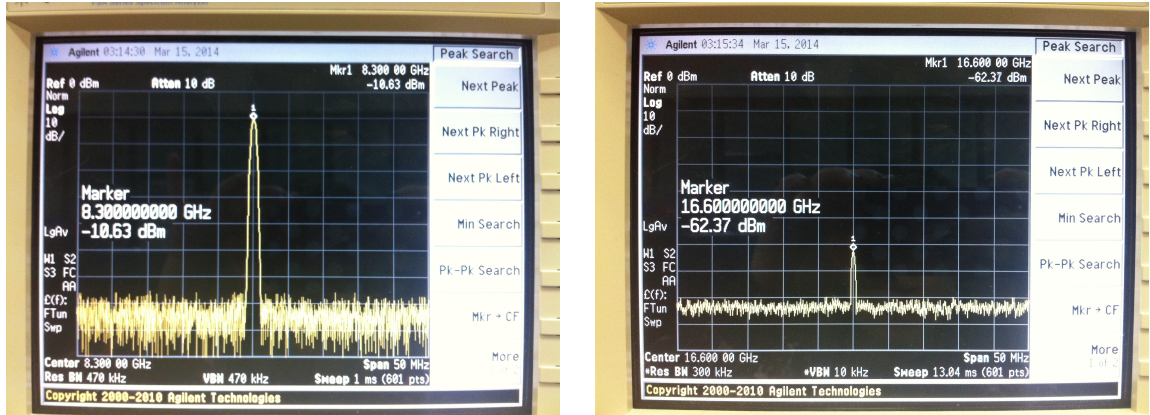
(b) Second harmonics

Figure 4.27: Harmonics measurement of one stage LNA

As seen above figures when input power is -30 dBm, fundamental signal power level is -21.09 dBm and second harmonics of the signal power is -81.52 dBm.

4.5.0.6 Two Stage LNA Design

In Figure 4.28 is illustrates fundamental signal and its second harmonic for one stage LNA.



(a) Fundamental signal

(b) Second harmonics

Figure 4.28: Harmonics measurement of two stage LNA

As seen above figures while input power is -30 dBm, fundamental signal power level is -10.63 dBm and second harmonics of the signal power is -62.37 dBm.

4.6 Summary

Table 4.1 and Table 4.2 show the summary of the LNA designs. The results at 8.3 GHz center frequency in 8.2-8.4 GHz frequency band are given in these tables.

@8.3 GHz	One Stage LNA Design	
Quantity	Simulated (dB)	Measurement (dB)
S_{11}	-5,3	-4,5
S_{21}	9,8	12
S_{12}	-25,4	-22,5
S_{22}	-23	-26
<i>Noise Figure</i>	0.532	Cold Source Method = 1,18 Y-Factor Method = 1.3

Table 4.1: Comparisons of simulated and measured results for one stage LNA

@8.3 GHz	Two Stage LNA Design	
Quantity	Simulated (dB)	Measurement (dB)
<i>S11</i>	-6,4	-3,2
<i>S21</i>	19,6	22,2
<i>S12</i>	-54	-45
<i>S22</i>	-23	-13
<i>Noise Figure</i>	0.582	Cold Source Method = 1,42 Y-Factor Method = 1.68

Table 4.2: Comparisons of simulated and measured results for two stage LNA

Table 4.3 shows examples of other LNA's and work in the literature. Some examples from literature or company products are classified with respect to their frequency, noise figure and gain. The table shows that in this work, an LNA was obtained with comparable results with the literature and existing competitors, although there are still some very good outliers. A discussion about the table is included in the conclusions.

Name of Company/ Literature	Frequency Band	Noise Figure	Gain
<i>Low Noise Factory [23]</i>	1-15 GHz	0.7 dB (typical)	37 dB
<i>NORSAT [24]</i>	7.25-7.75 GHz	0.8 dB	50 dB
<i>M/A-COM Technology Solutions [25]</i>	8-12 GHz	1.6 dB	20 dB
<i>Literature [26]</i>	7-11 GHz	1.85 dB	18 dB
<i>Literature [27]</i>	X-band	2.3 dB	16 dB

Table 4.3: Examples of other LNA's

Chapter 5

Conclusion

Low noise amplifiers (LNAs) play a crucial role in the radio receivers as the first stage of the system by dominating the noise figure of the system. In this thesis, the aim was to design, simulate and implement an LNA with the minimum noise figure and sufficient gain. The work started with a one stage LNA and to have sufficient gain another stage is added later. Both one stage and two stage LNAs were designed using micro-strip technology in 8.2 - 8.4 GHz frequency band and with active bias networks in order to have stable bias and to minimize passive components in the signal path. In these designs, common-source LNA topology is used, but inductive degeneration effects were also taken into account by simulation. Both one stage and two stage amplifiers are designed using NE3511S02 transistor, simulated and tuned to get the minimum noise figure. The designed one stage amplifier which cover the frequency band 8.2 - 8.4 GHz has a gain of 12 dB and noise figure of 1.2 dB at 8.3 GHz. The two stage amplifier has a gain of 22 dB and noise figure of 1.4 dB at 8.3 GHz. Both noise figure measurements were done using cold source method and Y-factor method in order to check the error margin in measurements. The simulated and measured results are compared and they showed good agreement in general. The noise turned out to be rather higher than the simulated results. These differences can be attributed to errors in measurements and simulations, but also input coupling losses.

Both one stage and two stage amplifiers are designed to obtain minimum

noise figure and the input reflection coefficient S_{11} was not taken into account as a parameter in the designs. The input match was designed to show Γ_{opt} to the input of the transistor for minimum noise figure. As seen from both simulations and measurements, input return losses of the amplifiers are not good enough. For one stage LNA design, it is clearly seen in Section 4.1.1, simulated and measured data are slightly close to each other. However, for the two-stage LNA design which is mentioned in Section 4.1.2, although noise matching is done at 8.3 GHz frequency as seen from simulation results, at the measured results it is clearly seen that matching has shifted by approximately 600 MHz to a lower frequency. At 7.7 GHz, noise figure, gain and input rejection coefficient are more consistent with simulated results of 8.3 GHz. The reason of the error could be packaging, PCB implementation, simulation errors or deviations in the transistor parameters. It is a well-known fact that transistor parameters can change appreciably from lot to lot.

It must also be stated that the design works better at lower frequencies although the results in the frequency band 8.2 - 8.4 GHz are also quite good. In future work the design must be shifted to higher frequencies.

In Section 4.6, the work carried out here is compared with the examples from the literature and the industry. This comparison does not claim to be comprehensive as this is a well-studied subject. In this thesis, an attempt was made to equal the existing technology and it is largely accomplished as seen in the table in Section 4.6. An industry standard LNA is designed and fabricated. There are some outlier amplifiers with very good noise figure in the industry, but a lot of effort must be spent in order to reach the best.

In future work, the first thing to be done is to find the reason behind the frequency shift and try to correct it. Along with this further study, other topics can also be studied. The input coupling of the circuit can be studied more extensively and losses of the input connector can be included in the simulation. The length of the transmission line between the connector and the input of the transistor can be made shorter to improve the noise figure. In addition, in this work, gain and noise figure were sacrificed to provide unconditional stability of

the circuit. In future work, an optimization between stabilization and noise figure can also be studied.

Another critical point in the design of LNAs with exceptionally good noise figures at the order of 1 dB is the measurement accuracy. In the literature, cold source method is quoted as having less error margin, but both the method and its application must be studied in more detail in order to make sure that the noise figure is measured correctly as error margin increases as the noise figure measured decreases.

Bibliography

- [1] M. Radmanesh, *Radio Frequency and Microwave Electronics Illustrated*. Prentice Hall PTR, 2001.
- [2] D. M. Pozar, *Microwave Engineering*. Wiley-IEEE Press, 2011.
- [3] S. Z. Sunny Gyamlani and J. C. Jigisa Sureja, “Comparative study of various lna topologies used for cmos lna design,” *International Journal of Computer Science and Emerging Technologies*, vol. 3, no. 1, pp. 41 – 49, 2012.
- [4] S. Arekapudi, “Analysis and design of cmos wide-band low noise amplifiers,” Master’s thesis, Stanford University, 2004.
- [5] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 1998.
- [6] J. Kucera and U. Lott, *The RF and Microwave Handbook*. CRC Press, 2001.
- [7] J. Adhyaru, “Design and analysis of ultra wide band cmos,” Master’s thesis, San Jose State University, 2007.
- [8] T. T. T. Nga, “Ultra low-power low-noise amplifier designs for 2.4 ghz ism band applications,” Master’s thesis, Nanyang Technological University, 2012.
- [9] D. Cherukumudi, “Ultra-low noise and highly linear two-stage low noise amplifier (lna),” Master’s thesis, Linkoping Institute of Technology, 2011.
- [10] T. Baker, “Successful lna design involves performance trade-offs,” *RF Design*, p. 68, 2006.

- [11] A. A. M. Challal and D. V. Janvier, “K-band two stages low noise amplifier design in microstrip technology,” *Eighth International Multi-Conference on Systems, Signals and Devices*, 2011.
- [12] J. Lucek and R. Damen, “Lna design for cdma front-end,” *RF Design*, 1999.
- [13] M. Edwall, “Low-noise amplifier design and optimization,” Master’s thesis, Lulea University of Technology, 2008.
- [14] X. S. a. L. Jingshi Yao, “Ultra low-noise highly linear integrated 1.5 to 2.7 ghz lna,” *TriQuint Semiconductor*, 2013.
- [15] J. L. Mayberry, “6 ghz low-noise amplifier design,” *IEEE*, 2012.
- [16] *Agilent Technologies, Optimizing On-wafer Noise Figure Measurements up to 67 GHz.*
- [17] *Agilent Technologies, High Accuracy Noise figure Measurements Using PNA-X Series Network Analyzer.*
- [18] *Agilent Technologies, Noise Figure Measurement Accuracy - The Y-Factor Method.*
- [19] *Agilent Technologies, PNA-X Series Microwave Network analyzers.*
- [20] T. Das, “Practical considerations for low noise amplifier design,” *Freescale Semiconductor White Paper*, 2013.
- [21] J. Coonrod and B. Rautio, “Comparing microstrip and cpw performance,” *Microwave Journal*, vol. 55, no. 7, pp. 74–82, 2012.
- [22] *Agilent Technologies, S-Parameter Simulations.*
- [23] *Low Noise Factor, LNF-LNR1-15A.*
- [24] *NORSAT, X1000S X-BAND LNA.*
- [25] *M/A-COM Technology Solutions Inc., MAAL-010528 X-Band Low Noise Amplifier.*

- [26] S. T. Janesch and K. H. G. Duh, "0.25 um pHEMT x band multifunction LNA mmic with t/r switch and attenuator achieves 1.85 dB noise figure," *IEEE MTT-S Digest*, 1992.
- [27] J. P. B. Janssen and M. van Heijningen, "X-band robust AlGaIn/GaN receiver mmics with over 41 dBm power handling," *Compound Semiconductor Integrated Circuits Symposium*, 2008.

Appendix A

Datasheet



HETERO JUNCTION FIELD EFFECT TRANSISTOR

NE3511S02

X TO Ku BAND SUPER LOW NOISE AMPLIFIER

N-CHANNEL HJ-FET

FEATURES

- Super low noise figure and high associated gain
NF = 0.30 dB TYP., $G_a = 13.5$ dB TYP. @ $f = 12$ GHz
- Micro-X plastic (S02) package

APPLICATIONS

- X to Ku-band DBS LNB
- Other X to Ku-band communication systems

ORDERING INFORMATION

Part Number	Order Number	Package	Quantity	Marking	Supplying Form
NE3511S02-T1C	NE3511S02-T1C-A	S02 (Pb-Free)	2 kpcs/reel	B	• 8 mm wide embossed taping • Pin 4 (Gate) faces the perforation side of the tape
NE3511S02-T1D	NE3511S02-T1D-A		10 kpcs/reel		

Remark To order evaluation samples, contact your nearby sales office.
Part number for sample order: NE3511S02-A

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$)

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	4	V
Gate to Source Voltage	V_{GS}	-3	V
Drain Current	I_D	I_{DSS}	mA
Gate Current	I_G	100	μA
Total Power Dissipation	P_{tot} ^{Note}	165	mW
Channel Temperature	T_{ch}	+125	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65 to +125	$^\circ\text{C}$

Note Mounted on $1.08 \text{ cm}^2 \times 1.0 \text{ mm}$ (t) glass epoxy PCB

Caution Observe precautions when handling because these devices are sensitive to electrostatic discharge.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

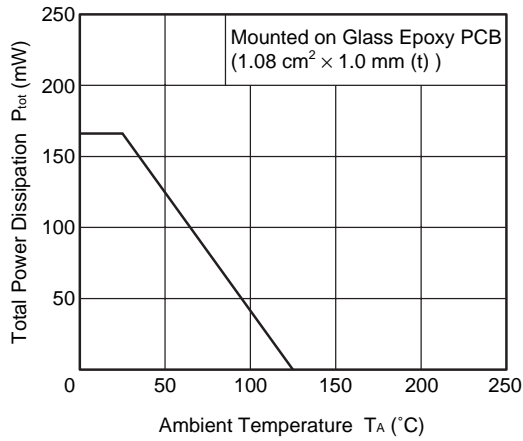
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Drain to Source Voltage	V _{DS}	1	2	3	V
Drain Current	I _D	5	10	20	mA
Input Power	P _{in}	–	–	0	dBm

ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise specified)

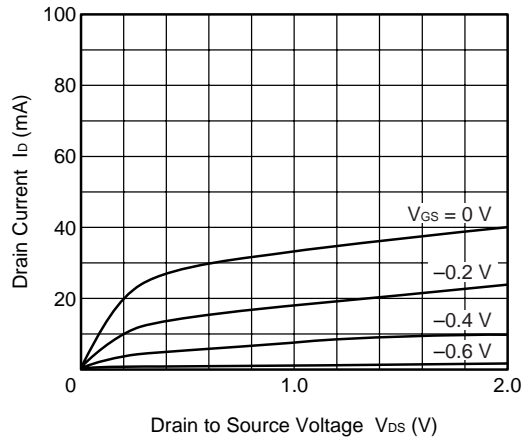
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source Leak Current	I _{GSO}	V _{GS} = –3 V	–	0.5	10	μA
Saturated Drain Current	I _{DSS}	V _{DS} = 2 V, V _{GS} = 0 V	20	40	70	mA
Gate to Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 2 V, I _D = 100 μA	–0.2	–0.7	–1.7	V
Transconductance	g _m	V _{DS} = 2 V, I _D = 10 mA	50	65	–	mS
Noise Figure	NF	V _{DS} = 2 V, I _D = 10 mA, f = 12 GHz	–	0.30	0.45	dB
Associated Gain	G _a		12.5	13.5	–	dB

TYPICAL CHARACTERISTICS (T_A = +25°C, unless otherwise specified)

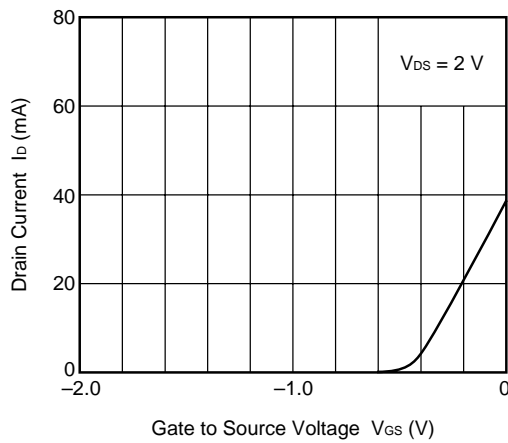
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



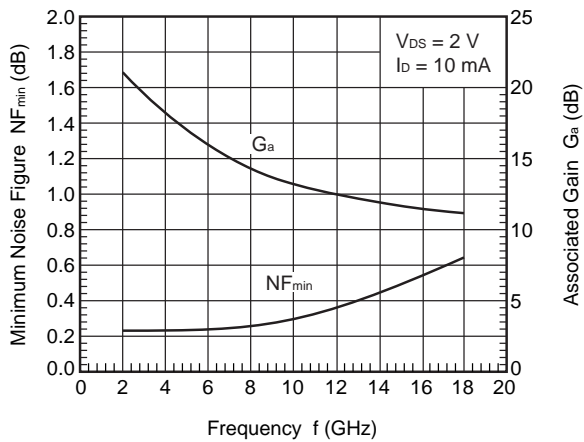
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



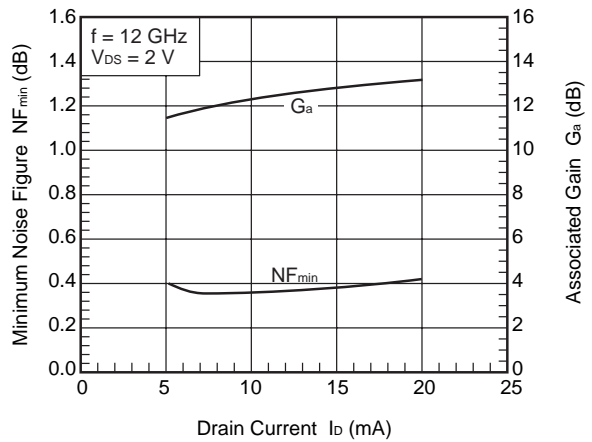
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



MINIMUM NOISE FIGURE, ASSOCIATED GAIN vs. FREQUENCY



MINIMUM NOISE FIGURE, ASSOCIATED GAIN vs. DRAIN CURRENT



Remark The graphs indicate nominal characteristics.

S-PARAMETERS

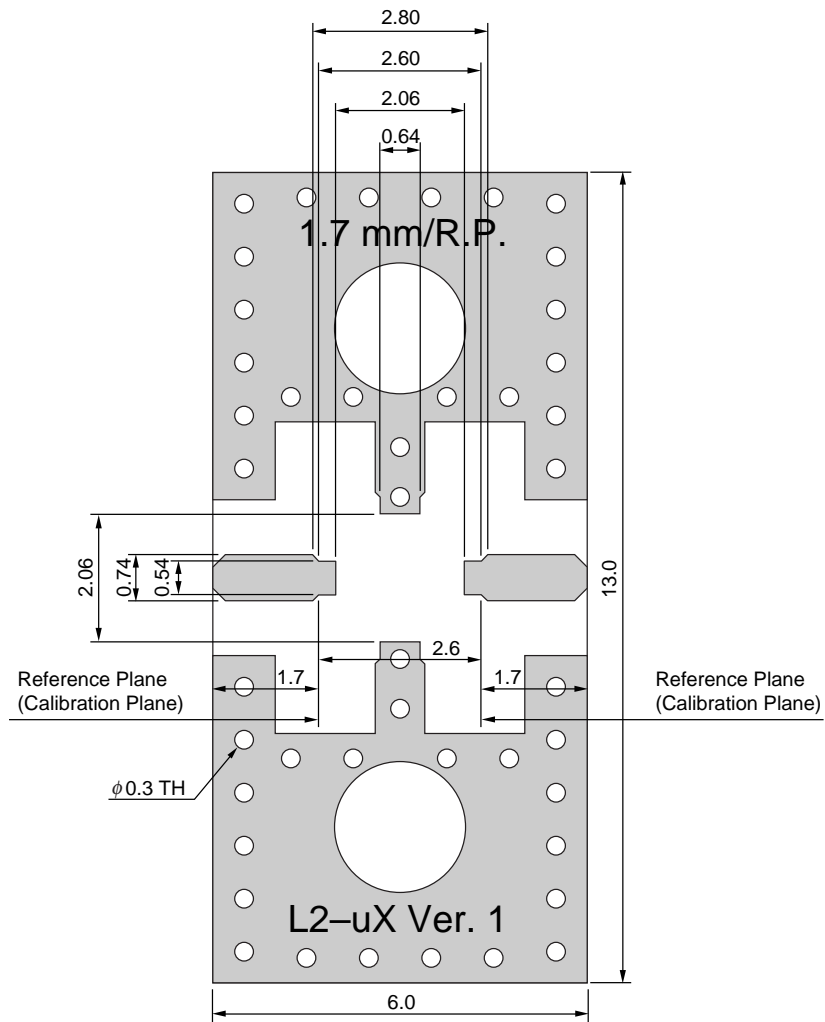
S-parameters/Noise parameters are provided on our web site in a form (S2P) that enables direct import to a microwave circuit simulator without keyboard input.

Click here to download S-parameters.

[RF and Microwave] → [Device Parameters]

URL <http://www.ncsd.necel.com/microwave/index.html>

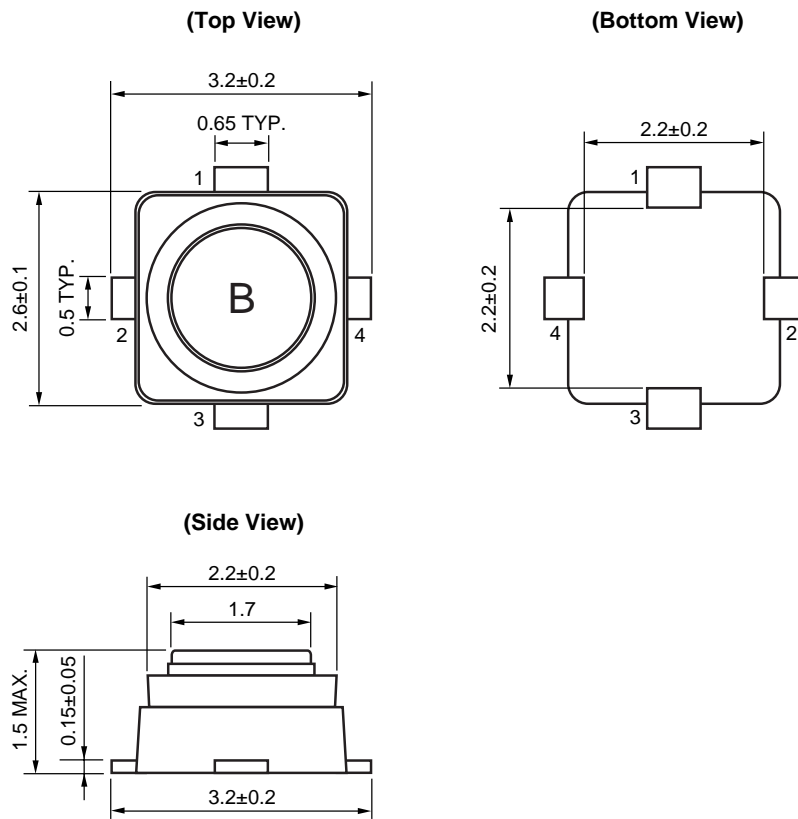
RF MEASURING LAYOUT PATTERN (REFERENCE ONLY) (UNIT: mm)



RT/duroid 5880/ROGERS
 t = 0.254 mm
 $\epsilon_r = 2.20$
 tan delta = 0.0009 @10 GHz

PACKAGE DIMENSIONS

S02 (UNIT: mm)



PIN CONNECTIONS

1. Source
2. Drain
3. Source
4. Gate

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions	Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature)	: 260°C or below
	Time at peak temperature	: 10 seconds or less
	Time at temperature of 220°C or higher	: 60 seconds or less
	Preheating time at 120 to 180°C	: 120±30 seconds
	Maximum number of reflow processes	: 3 times
	Maximum chlorine content of rosin flux (% mass)	: 0.2%(Wt.) or below
Partial Heating	Peak temperature (terminal temperature)	: 350°C or below
	Soldering time (per side of device)	: 3 seconds or less
	Maximum chlorine content of rosin flux (% mass)	: 0.2%(Wt.) or below

Caution Do not use different soldering methods together (except for partial heating).

• **The information in this document is current as of October, 2006. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**

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(Note)

(1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.

(2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).

Caution	GaAs Products	<p>This product uses gallium arsenide (GaAs). GaAs vapor and powder are hazardous to human health if inhaled or ingested, so please observe the following points.</p> <ul style="list-style-type: none"> • Follow related laws and ordinances when disposing of the product. If there are no applicable laws and/or ordinances, dispose of the product as recommended below. <ol style="list-style-type: none"> 1. Commission a disposal company able to (with a license to) collect, transport and dispose of materials that contain arsenic and other such industrial waste materials. 2. Exclude the product from general industrial waste and household garbage, and ensure that the product is controlled (as industrial waste subject to special control) up until final disposal. • Do not burn, destroy, cut, crush, or chemically dissolve the product. • Do not lick the product or in any way allow it to enter the mouth.
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► For further information, please contact

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Compound Semiconductor Devices Division

NEC Electronics Corporation

URL: <http://www.ncsd.necel.com/>

Subject: Compliance with EU Directives

CEL certifies, to its knowledge, that semiconductor and laser products detailed below are compliant with the requirements of European Union (EU) Directive 2002/95/EC Restriction on Use of Hazardous Substances in electrical and electronic equipment (RoHS) and the requirements of EU Directive 2003/11/EC Restriction on Penta and Octa BDE.

CEL Pb-free products have the same base part number with a suffix added. The suffix –A indicates that the device is Pb-free. The –AZ suffix is used to designate devices containing Pb which are exempted from the requirement of RoHS directive (*). In all cases the devices have Pb-free terminals. All devices with these suffixes meet the requirements of the RoHS directive.

This status is based on CEL's understanding of the EU Directives and knowledge of the materials that go into its products as of the date of disclosure of this information.

Restricted Substance per RoHS	Concentration Limit per RoHS (values are not yet fixed)	Concentration contained in CEL devices	
		-A	-AZ
Lead (Pb)	< 1000 PPM	Not Detected	(*)
Mercury	< 1000 PPM	Not Detected	
Cadmium	< 100 PPM	Not Detected	
Hexavalent Chromium	< 1000 PPM	Not Detected	
PBB	< 1000 PPM	Not Detected	
PBDE	< 1000 PPM	Not Detected	

If you should have any additional questions regarding our devices and compliance to environmental standards, please do not hesitate to contact your local representative.

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