DESIGN OF THE ANALOG BLOCKS USED IN A FIELD PROGRAMMABLE MIXED ARRAY (FPMA) IN 90-NM CMOS TECHNOLOGY

by

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ABSTRACT

DESIGN OF THE ANALOG BLOCKS USED IN A FIELD PROGRAMMABLE MIXED ARRAY (FPMA) IN 90-NM CMOS TECHNOLOGY

The miniaturization trend in electronic circuits enforces integrating analog and digital circuits in a System On a Chip (SOC) solution, reviving a renewed interest in Field Programmable Mixed Arrays (FPMA). This approach has an advantage of implementing both analog and digital circuits in one chip. In this thesis we present the analog building blocks used in the analog core of a Field Programmable Mixed Array (FPMA). The analog array contains CABs (Configurable analog block) with both configurable and fixed analog blocks such as OTAs with tunable transconductances, wide common-mode range OPAMP, comparator, linear voltage to current converter, current to voltage converter and capacitors bank. Filter application such as low and bandpass G_m-C filters in a frequency range from 10Hz to 120MHz has been implemented using the designed components. The circuit blocks were designed and layouts of proposed analog blocks were implemented in TSMC 90-nm CMOS process single poly nine-metal with single 1.2 V power supply.

ÖZET

BİR ALANDA PROGRAMLANABİLİR KARMA DİZİDE (FPMA) KULLANILAN ANALOG BLOKLARIN 90nm CMOS TEKNOLOJİSİNDE TASARIMI

Elektronik devreleri giderek küçültme eğiliminin analog ve sayısal devreleri tümleşik olarak tek bir sistem yongası (SOC) üzerinde birleştirmeye yöneltmesi, alanda programlanabilir karma dizilere (FPMA) olan ilginin yeniden canlanmasına neden olmuştur. Bu yaklaşım, hem analog hem de sayısal devreleri tek bir tümdevrede gerçekleştirebilme avantajı sağlamaktadır. Bu tezde FPMA tümdevresinin analog kısmında yer alan temel devre katlarının tasarımları sunulmaktadır. Analog diziler ayarlanabilir işlemsel geçiş iletkenliği kuvvetlendiricisi (OTA), geniş giriş aralıklı işlem--sel kuvvetlendirici (OPAMP), karşılaştırıcı, sığaç öbeği, doğrusal gerilim-akım ve akım-gerilim dönüştürücüleri gibi gerek yapılandırılabilir, gerekse sabit analog katlardan oluşan yapılandırılabilir analog katlardan (CAB) oluşmaktadır. Tasarlanan yapılar ile örnek uygulamalar olarak 10 Hz ile 120 MHz aralığında çalışan çeşitli alçak geçiren ve bant geçiren G_m-C süzgeçlerin benzetimi yapılmıştır. Önerilen analog katların devre ve serim tasarımları TSMC 90nm CMOS tek poly dokuz metal 1.2V besleme gerilimi teknolojisi ile yapılmıştır.

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LIST OF SYMBOLS

C	Capacitance
C_L	Load Capacitance
C_c	Compensation Capacitance
C_{ox}	Capacitance of the oxide layer
$\overline{(eto)^2}$	Output noise voltage spectral density
$\overline{(eni)^2}$	Input noise voltage spectral density
G_m	Transconductance
L	Channel length of a transistor
μ	Carrier Mobility
r_{ds}	Drain-source resistance
R_o	Output resistance
W	Channel width of a transistor
V_{cm}	Common-mode voltage
V_{dd}	Supply voltage
V_{ds}	Drain to source voltage
V_{gs}	Gate to source voltage
V_{ov}	Effective gate to source voltage (overdrive voltage)
V_t	Threshold voltage
T	Temperature

LIST OF ACRONYMS/ABBREVIATIONS

ADC	Analog-to-Digital Converter
ASIC	Application-specific integrated circuit
CAB	Configurable Analog Block
CLB	Configurable Logic Block
DAC	Digital-to-Analog Converter
FG	Floating Gate
FPAA	Field Programmable Analog Array
FPGA	Field Programmable Gate Array
FPMA	Field Programmable Mixed Array
HD3	Third Harmonic Distortion
IC	Integrated Circuit
IM3	Intermodulation distortion
IRN	Input Referred Noise
LI	Local interconnect
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LUT	Look-up Table
MITE	Multiple-Input Translinear Element
MOS	Metal Oxide Semiconductor
NMOS	Negative-Channel Metal Oxide Semiconductor
OPAMP	Operational Amplifiers
OTA	Operational Tranconductance Amplifier
PLD	Programmable Logic Device
PLL	Phase-Locked-Loop
Pmax	Maximum Power Consumption
PMOS	Positive-Channel Metal Oxide Semiconductor
SB	Switch Box
SC	Switched-Capacitor

SI	Switched Current
SOC	System-On-Chip
TIA	Transimpedance Amplifier

1. INTRODUCTION AND BACKGROUND

The market circumstances have made an important impact on electronic circuit design. Recently it is difficult to follow the market conditions since, technology is advancing in a fast rate. The most important issue is to responding the consumer demands and even some new upgrades might be required during first design such as performance improvements and additional enhancements. One of the practical solutions to these difficulties is reconfigurability. High fabrication costs and fierce time-to-market competition resulted in bringing huge success and popularity to the Field Programmable Gate Arrays (FPGA) for digital design in the last three decades [8], [9]. Despite the prevalence of digital circuits in integrated circuit (IC) industry, analog integrated circuits still have an unsubstitutable role in interfacing digital circuits to the real world; therefore, several Field Programmable Analog Array (FPAA) architectures [10–12] have also been proposed as analog counterparts for FPGAs. The miniaturization trend in electronic circuits enforces integrating analog and digital circuits in a System On a Chip (SOC) solution, reviving a renewed interest in Field Programmable Mixed Arrays (FPMA) that had not attracted much attention since the idea was first proposed in 1995 [13]. On the other hand, designing analog and digital reconfigurable circuits in the same IC brings new challenges especially for the analog arrays as the technology scales down to 100nm and below. While digital circuits benefit from the advantages of technology scaling, analog circuits usually suffer from the increasing non-ideal sub-micron effects. Recent studies on digitally assisted analog circuits suggest solutions for some of these problems. Compensation by either calibration of the analog circuit or digital error correction are the two solutions that are being suggested for solving systematic errors caused by non-ideal effects such as mismatch and non-linearity.

This thesis focuses on the design of basic analog circuit blocks to be used in the analog core of an FPMA IC in TSMC-90nm CMOS process. In Chapter 2, the proposed FPMA architecture is briefly described. The analog array and interconnect

architecture are presented in Chapter 3. This chapter mainly focuses on the design procedure and obtained schematic simulation results of both configurable and fixed analog blocks which are going to be used in the configurable analog blocks. In Chapter 3, some of the important layout techniques is introduced. The layout of the proposed analog circuits and post-layout simulation results is presented. Chapter 4 presents some circuit topologies such as I-V converters, multipliers and Gm-C filters which can be implemented with available analog blocks.

1.1. Digital Arrays (FPGA)

Field programmable gate arrays have been utilized for prototyping wide range of digital circuits over the last decades. Their architecture is the most significant purpose of their rise since, it provides a programmable logic functions and interconnect. FPGAs are programmable devices with high flexibility, they can be configured in a short time and most important, the fabrication cost is low comparing to Application Specific Integrated Circuit (ASIC) devices. For manufacturing a beneficial ASIC, long time and high cost is required. The high cost includes placement, routing, simulation, CAD tool, the mask of fully-fabricated device and etc. Therefore, avoiding these high costs and longtime fabrication, digital designers are prompted toward FPGA implementations. FPGAs have some drawbacks such as more power consumption, low speed and they require more area because of their programmable structure.

As depicted in Figure. 1.1 FPGAs are made up of an array of programmable logic blocks. According to their functionality these blocks are grouped into logic blocks, memory and multiplier cells. Configurable blocks can connect to each other through a programmable interconnect network which enclose all the available blocks in the array. The I/O blocks are also place around the array in order to provide a connection between FPGA and other devices. By programing these arrays and connect them in a desired configuration, it is possible to program a function into chip.

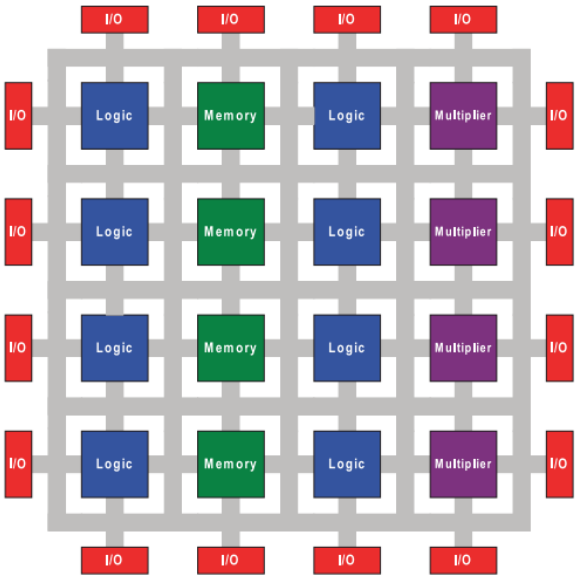

Figure 1.1. Basic FPGA architecture [1].

1.1.1. Configurable Logic Block (CLB)

Configurable Logic Blocks are the programmable cells which are placed in an array structure inside the FPGA in order to implement logic functions. The main tasks of these blocks are providing computations and storing data. For obtaining more functionality, especially in commercial FPGAs (Xilinx, Altera and etc.), simple basic elements are replaced with developed complex logic blocks which employ lookup tables (LUTs) as combinatorial function blocks Figure 1.2. lookup tables can implement Boolean functions corresponding to their number of input variables. Recent FPGAs such as Xilinx XC3000 [2] and Virtex 5 employ developed lookup tables to implement logic functions. The logic blocks include lookup tables (2 to 6 input variables), flip-flops, I/O selection units and etc.

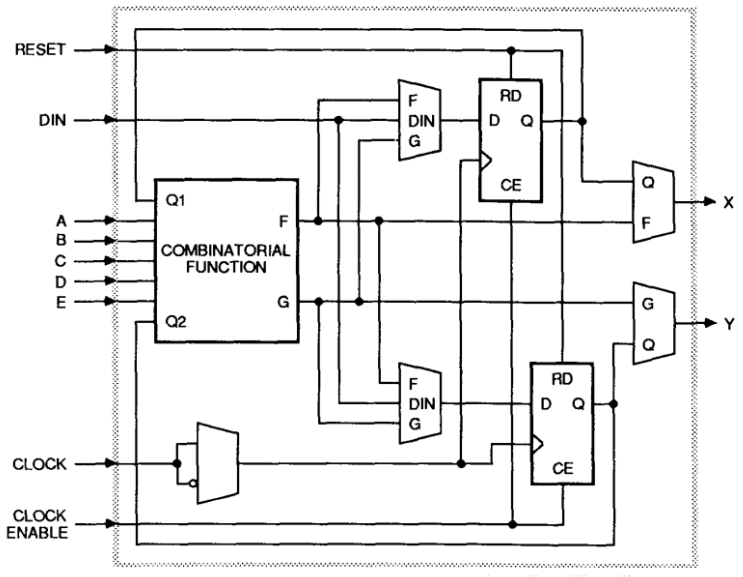

Figure 1.2. XC3000 Configurable Logic Block [2].

1.1.2. Routing Architecture

The routing architecture is a major issue of designing programmable arrays since, it defines the places and numbers of wires in channels, position of routing channels in respect to placement of logic blocks, length of wires and etc. There are several routing architecture categories such as hierarchical [14] and island-style [15].

- Hierarchical Routing Architectures

  As shown in Figure 1.3, in this routing architecture, logic blocks are partitioned into several different groups. The wire segments are divided into low and high level routing hierarchy. Segments with lower hierarchy level connect blocks in same group and segments with higher hierarchy level connect blocks in distant groups. This architecture has been used in several commercial FPGA devices such as Altera, Flex10K and Apex architectures.

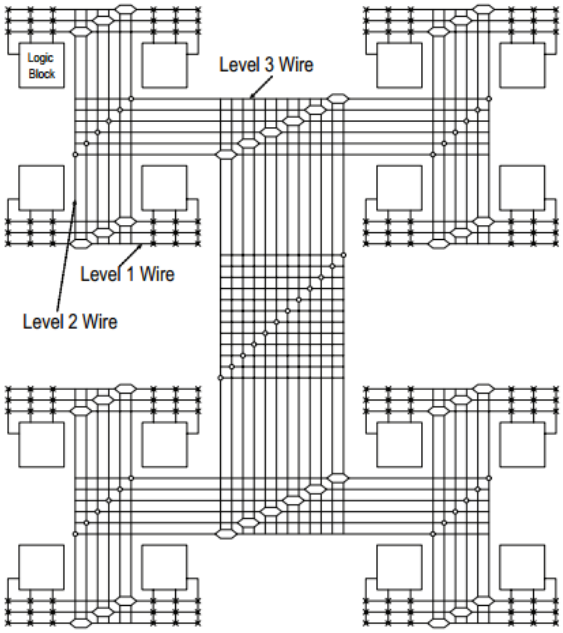

Figure 1.3. Example of Hierarchical Routing Architecture [1].

- Island-Style Routing Architecture

  As illustrated in Figure 1.4, in this routing architecture, logic blocks are placed in two dimensional network. The routing network is distributed throughout an array of logic blocks in a way that each block is surrounded by several wire segments. At a present time the SRAM-based FPGA devices are using this architectures.

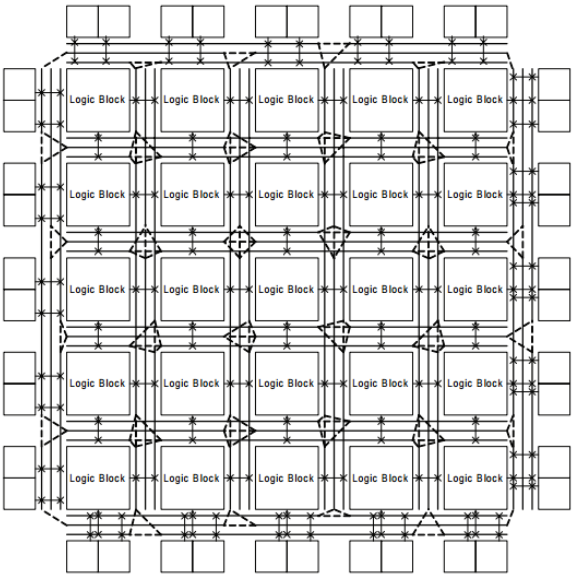

Figure 1.4. Example of Island-Style Routing Architecture [1].

1.1.3. Programming Technologies

There are large amount of switches used in FPGAs, which are the main elements for controlling the programming task. Several programming technologies such as EPROM, EEPROM, flash, static memory and anti-fuses are being used to control these switches and each one has an specific influence on configurable logic architecture.

Programming Methods have been used in FPGAs:

- Static Memory Programming Technology

  This approach is based on SRAM programming technology which are broadly used in FPGAs and it is observed in Xilinx, Lattice and Altera FPGA devices. A basic static memory cell is depicted in Figure 1.5. Reconfigurability is provided with static memory cells which are spread over wide area inside the chip. SRAMs are used for either switching lines to multiplexers that drive interconnect signals or storing data in lookup tables. The advantages of using SRAM technology are

higher speed and lower dynamic power consumption, as they do not require a specific circuit processing steps. SRAM-based programming technologies however have some drawbacks such as high area usage, volatility, insecurity and etc.

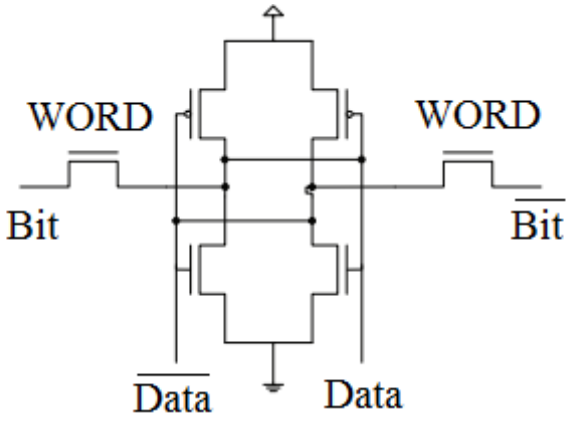

Figure 1.5. Static memory cells.

- Flash/EEPROM Programming Technology

Flash or EEPROM technology uses floating gate (FG) transistors for programming task. Modern technology provide a possibility to use floating gate transistors as individual switches. Figure 1.6 depicts a floating gate transistor schematic view. An additional small transistor is used for programming floating gate by injecting charge and erasing it as well. The most significant advantage of Flash Programming technology is non-volatility. The other advantages of this programming approach are high speed functionality and less area usage. Contrary to SRAM based programming technology, flashed-base devices cannot be programmed an indefinite number of times because of the charge accumulation in the oxide. Therefore their programming cycles are limited to few hundred times. For instance this rate is 500 for Actel ProASIC3 EEPROM based FPGA device.

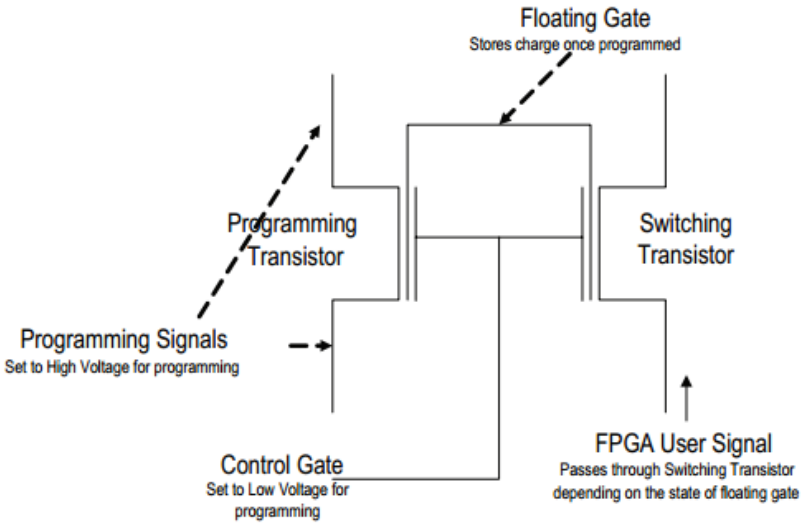

Figure 1.6. Floating gate transistor [1].

- Anti-fuse Programming Technology

  Anti-fuse Programming technology is based on resistive switches. These switches operate similar to a high-resistance in the path of signal when they are switched off. They can be programmed to become a low resistance to create a connection. There are two approaches available to implement anti-fuse switches. First is using a dielectric made of oxide-nitride-oxide which has a capability of breaking down in high voltages and conducting the signal with low resistance around few hundred ohms. The second one is using metal-to metal based anti-fuses which are made of fiercely pressed insulating materials such as silicon oxide between two metals. The second approach is used in Actel and QuickLogic FPGA devices. The advantages of anti-fuse programming approach low area, low on-resistance and parasitic capacitance. Anti-fuse programming approach is not re-programmable and this is the major drawback that makes it inappropriate for reconfigurable applications. Moreover, Anti-fuse cannot be implemented by standard CMOS technology.

1.2. Analog Arrays (FPAA)

Although the Digital circuits are most prevalent elements for the VLSI market, analog integrated circuits are still required for present electronics. Analog circuits is interfacing digital electronics to the real world in many applications such as analog signal processing, motion control, biomedical measurements and etc. [16].

Field-programmable gate arrays for testing digital circuits are now commercially available from several vendors [3]. Field programmable analog arrays (FPAAs) are quite practical in signal processing as analog front-end and are commonly used as sensor interfaces or be feasible element for analog/digital-converters in order to amplify or filter the signal before it is sampled. It is possible to implement adaptable filters using FPAA, when the signal-bandwidth of the input-signal is variable, e.g. in hard disk drives, wireless communication and biomedical applications. The significance of testability has increased with growing manufacturability and costs; however, testing of analog circuits is a difficult task since many factors are taken into account such as gain, bandwidth, noise, linearity, leakage, etc. The FPAA concept provides an stimulating approach to rapid prototyping of analog circuits since the circuits in configurable blocks are similar and the routing network provides accessibility to inputs and outputs of each block. The FPAA provides tunability and observability, such that each programmable analog function can be tested systematically. There are also several commercially available discrete and continuous time FPAAs in the market such as Anadigm "AN120E04" and "ispPAC30 In-System Programmable Analog Circuit". As discussed in previous section, generally, field-programmable gate arrays (FPGA) consists of configurable logic blocks (CLB's) that implement logic functions and a routing network to provide connections between CLB's. Similarly, The FPAA contains configurable Analog Blocks (CABs) and the interconnection network. It can be observed that, the circuit topologies for different functions are similar. Figure 1.7 shows a array architecture overview of an FPAA which contains a group of CABs and routing network.

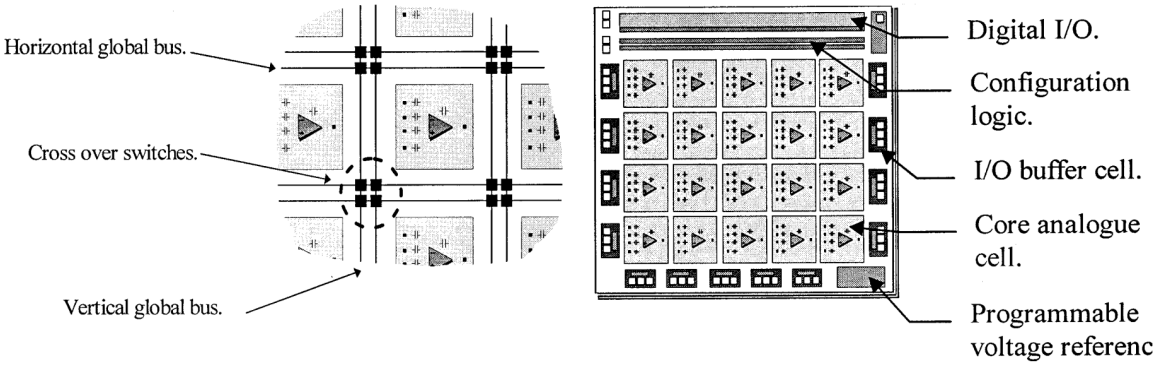

Figure 1.7. Archtecture overview of DPAD2 Field Programmable Analog Array which contains a group of CAB and routing network [3]

1.2.1. FPAA Design Issues

- Discrete-time vs Continuous-time

  (i) Discrete-time domain FPAA

  Discrete-time domain devices operate using a sample clock. Most of discrete-time FPAAs are based on switch-capacitor topologies [5] in which the analog blocks get a sampled input signal from sample and hold circuits which consist of multiple switches and capacitor banks. This approach requires more complex topologies. The Discrete-time FPAAs have better bandwidth, programmability and insensitivity to resistance in programming switches. However, these FPAAs consume more power comparing to continuous-time FPAA and their input voltage frequency is limited to clock speed. Anadigm (AN120E04) [17] and Lattice(ispPAC30) [18] are two commercially available discrete-time FPAAs.

  (ii) Continuous-time domain FPAAs

  A continuous-time domain devices consist of analog blocks such as transconductors and OPAMPs. These types of FPAAs have advantages in terms of less power

consumption and easier design. However their programming range is not as wide as discrete-time counterparts and they are mostly affected by degradation that is caused by parasitics. Cypress (PSoC) [19] and Zetex (TRAC) [20] are two commercially available discrete time FPAAs.

- Voltage-mode vs. Current-mode.

  (i) Current-mode FPAAs
  Current is chosen as a signal parameter in these types of FPAAs. These FPAAs have advantages in terms of low-power consumption, offering simple basic blocks and wide-band frequency responses. They consist of current mirrors and basic blocks for implementing variable gain OPAMPs and tunable transconductances [21].
  (ii) Voltage-mode FPAAs
  Voltage is chosen as a signal parameter in these types of FPAAs. The voltage-mode FPAA has low bandwidths comparing to current mode designs. The major drawback of voltage signals is having a high fanout. The voltage-mode design [22] has a low accuracy and high power comparing to current-mode design approach [23].

- CAB Design.

  Configurable analog blocks are the main components of FPAAs. In order to design CABs many factors should be taken into account such as functionality and performance of circuits which are going to be implemented using programmable cells. The supporting technology and area efficiency of routing network also effects designing CABs. The other factor is level of granularity. CABs are grouped into fine-grained and coarse-grained architectures.

  (i) Fine-grained architecture
  CABs are programmable at the transistor level. Although these architectures [4],

[24] needs more complex routing and large number of switches, they are more versatile and it is possible to implement wide range of circuits and applications. Signal degradation and non-linearity caused by many switches and connections are some drawbacks of using this architecture.

(ii) Coarse-grained architecture
CABs are programmable at the macro block level (tunable analog blocks) [6], [5]. Coarse-grained architectures are less versatile comparing to fine-grained ones and it is not possible to implement many various circuits on them. The coarse-grained architectures have less parasitics.

- In terms of reconfigurability different types of analog blocks to be used in coarse-grained CABs can be designed:

  (i) Tunable Analog Blocks
  CABs consist programmable components such as tunable transconductance, programmable resistors and programmable capacitor arrays. The programmable capacitors are commonly used in switch-capacitor topologies [16].

  (ii) Fixed Analog Blocks
  CABs include fixed circuits such as OPAMPs, comparators, voltage to current converter and etc. Hence, the programmability is provided with connecting these fixed analog blocks in a various configurations to implement analog applications.

- Connection Network Architectures
  One of the major factors in designing FPAAs is opting for an appropriate interconnection network, since the interconnect topology has an important influence on the performance of prototyped circuits. Different types of architectures either hierarchical or full crossbar interconnection architectures are used considering the problems that are more critical in analog design such as parasitics, noise and non-ideal effects which are introduced by switches in the signal path.

1.2.2. CAB Design Examples

Figure 1.8 depicts a CAB design example which is presented in [4]. This FPAA is based on current-mode design techniques; therefore, current mode cells are used in CABs Figure 1.8a. A cell can be connected to the other one using switches which are simple pass transistors Figure 1.8b. The schematic diagram of whole CAB is shown in 1.8c. A neural network and Gilbert multiplier circuit were implemented in this FPAA with available cells in the CAB.

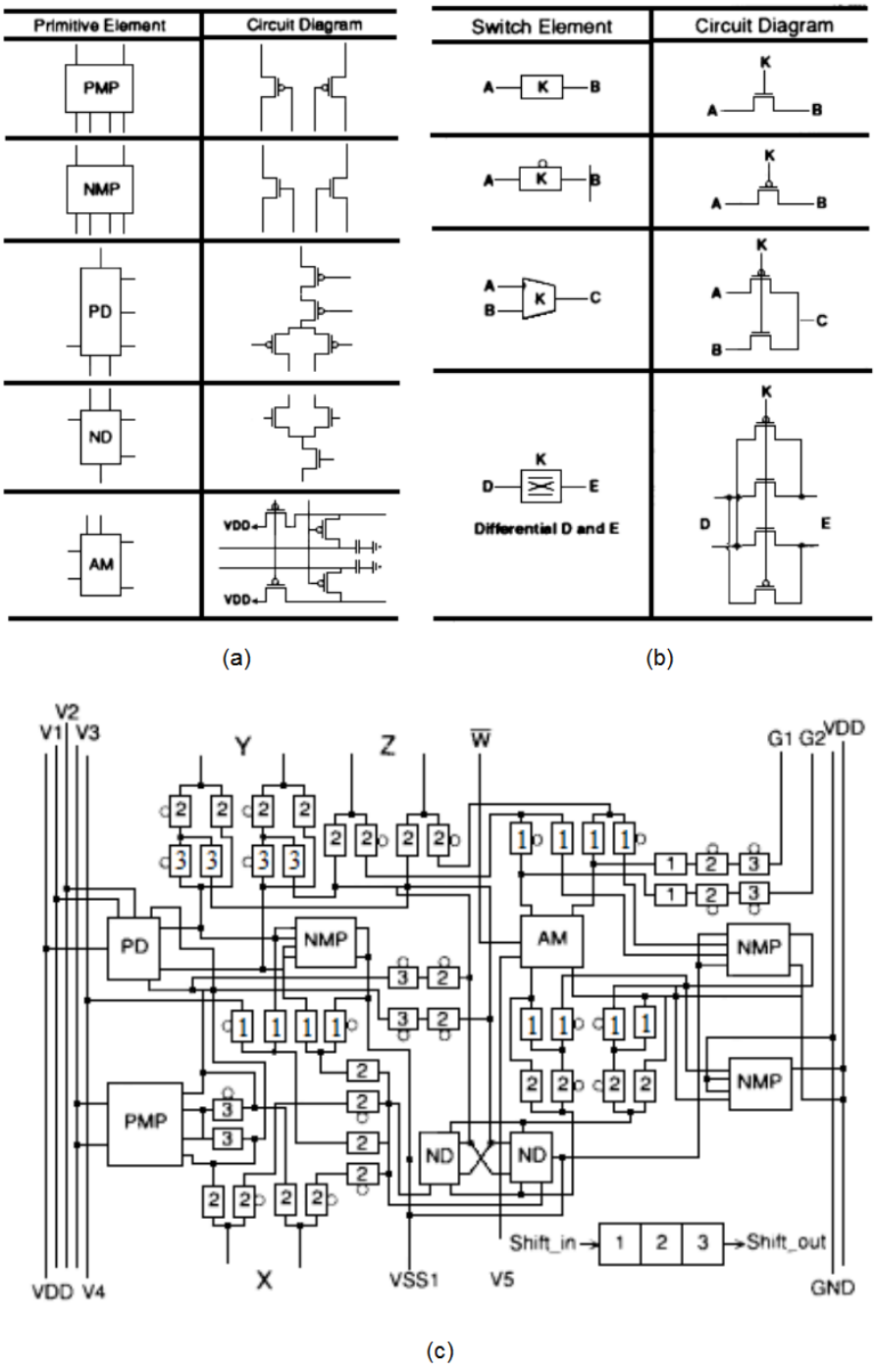

Figure 1.8. The CAB design example [4]. (a) current-mode cells used as elements of the CAB. (b) The switches (c) Overall schematic view of CAB.

A FPPA architecture based on switched-capacitor technique is proposed in [5]. As

shown in Figure 1.9 CABs contain switch capacitor elements and OPAMPs. The programmability of CABs is achieved by changing the clock frequency of switched-capacitors. Applications such as different types of filters from low to high orders, tunable amplifiers, modulators, demodulator and etc are implemented in this FPAA.

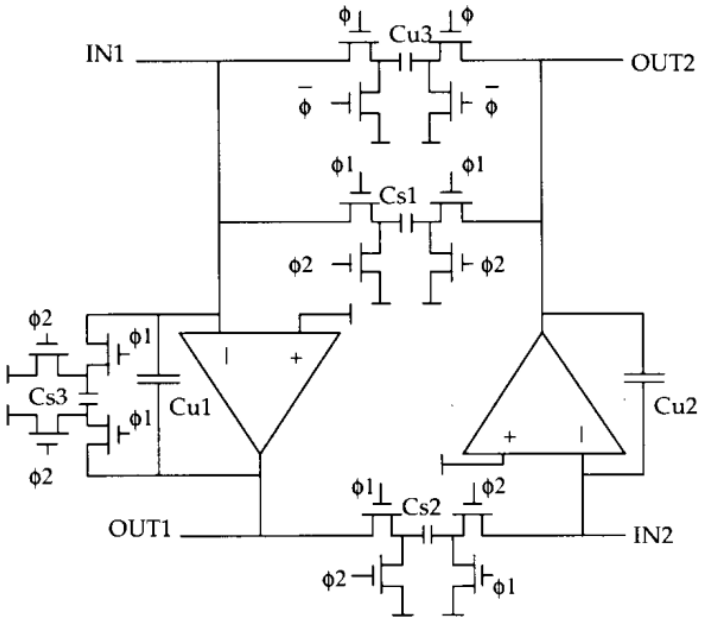

Figure 1.9. CAB structure based on switch-capacitor technique [5].

Another example of FPAA design is implemented in [6]. In this FPAA operational transconductance amplifiers known as Gm-cells are used as configurable analog blocks which are tuned digitally. As depicted in Figure 1.10 seven OTAs are placed in one CAB, where CABs are placed in a hexagonal lattice network. In this architecture each CAB is surrounded by six identical CABs. All CABs and OTAs are hardwired here and no switches are used. Therefore, each OTA can be switched off or on by controlling its bias current. High order Gm-C filters are implemented in using array of CABs.

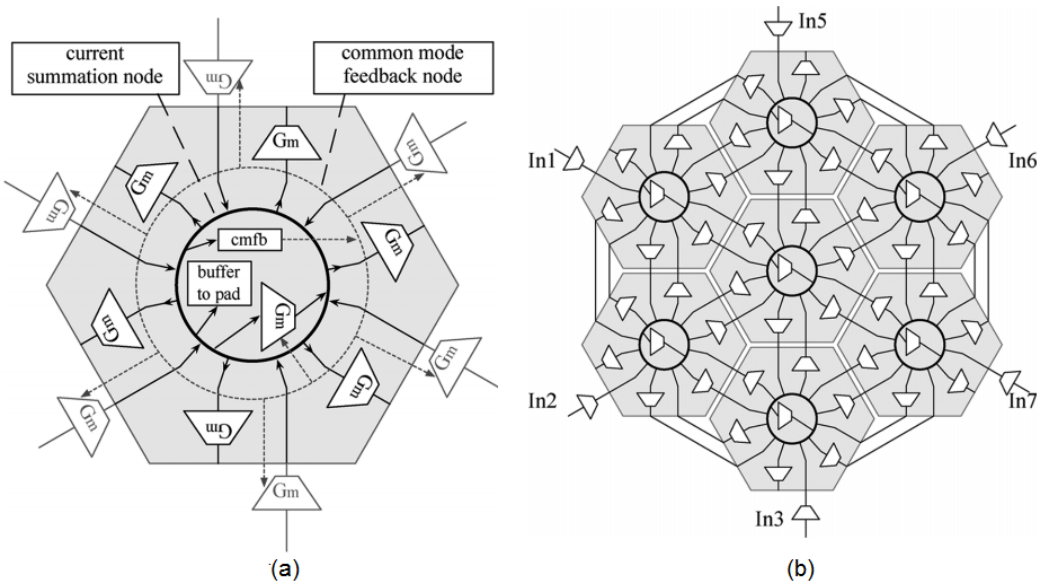

Figure 1.10. CAB design example with tunable OTAs [6]. (a) Array topology of implemented FPAA with CABs. (b) Schematic view of single CAB.

1.3. Field Programmable Mixed Arrays (FPMA)

The FPMA approach has an advantages of implementing both analog and digital circuits in one chip; therefore, it has less interconnection, area and most important less cost. There have been some attempts to use both digital and analog circuits on a single programmable chip to produce a single Field-Programmable Mixed-analog-digital Array (FPMA) [13]. FPMA has both FPGA and FPAA arrays and signal conversion interface in between. This mixed-signal interface consists of D/A and A/D for data conversion between analog and digital part. Two conceptual views of FPMA architecture are shown in Figure 1.11. The first concept is implementing the data converters with programmable components in analog and digital array Figure 1.11a. The second approach is an autonomous mixed-signal interface, which is constructed separately and connected to analog and digital part through interconnect network Figure 1.11b. Second concept has an advantages in terms of flexibility; However, more area usage and low speed, are the two major drawbacks.

Recently, a new approach of implementing a field programmable array of analog and

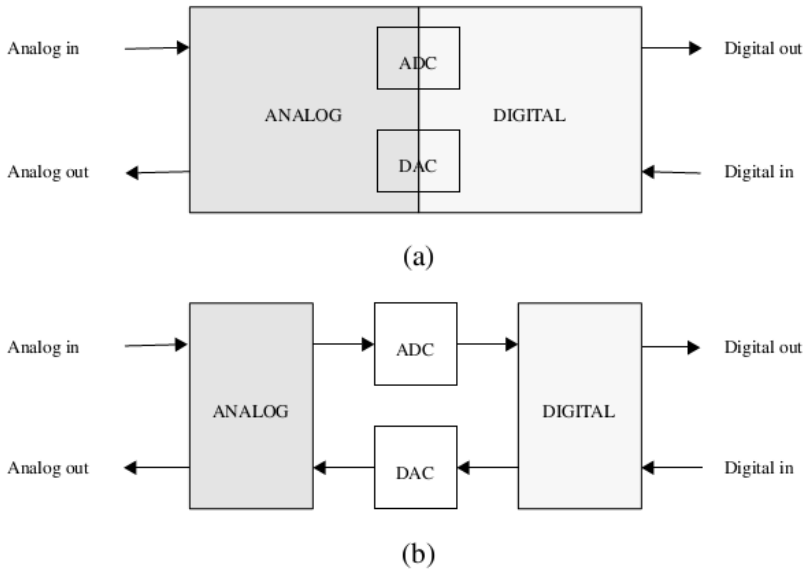

Figure 1.11. Conceptual views of mixed-signal architectures: (a) array architecture with field-programmable resources capable of constructing data converter as required; (b) array architecture with dedicated data converters [13].

digital devices (FPAADD) has been proposed [7]. The main concept of this trend is inserting the digital computational blocks in between the analog blocks, rather than separating the analog and digital parts. Therefore this method increases the flexibility. Similar to other architectures the digital configurable blocks are look-up tables (LUTs) and the analog tunable blocks consists either transistors or OPAMPs and multiple input trans linear elements (MITEs). The major difference between this approach and other designs is, using floating gate transistors (FG) for implementing a connection network. The floating gate transistors have many advantages in terms of detailed programmability, low sub-threshold leakage current and non-volatility. Figure 1.12 depicts the architecture overview of FPAADD.

In this topology floating gate transistors are used as switches. Moreover, FG transistors operate as non-volatile memory cells since they store states. Therefore, as discussed in Section 1.1.3 with such a topology, reprogramming is not required on power up. The FG transistors tasks are not limited to only switching, since they can be utilized as

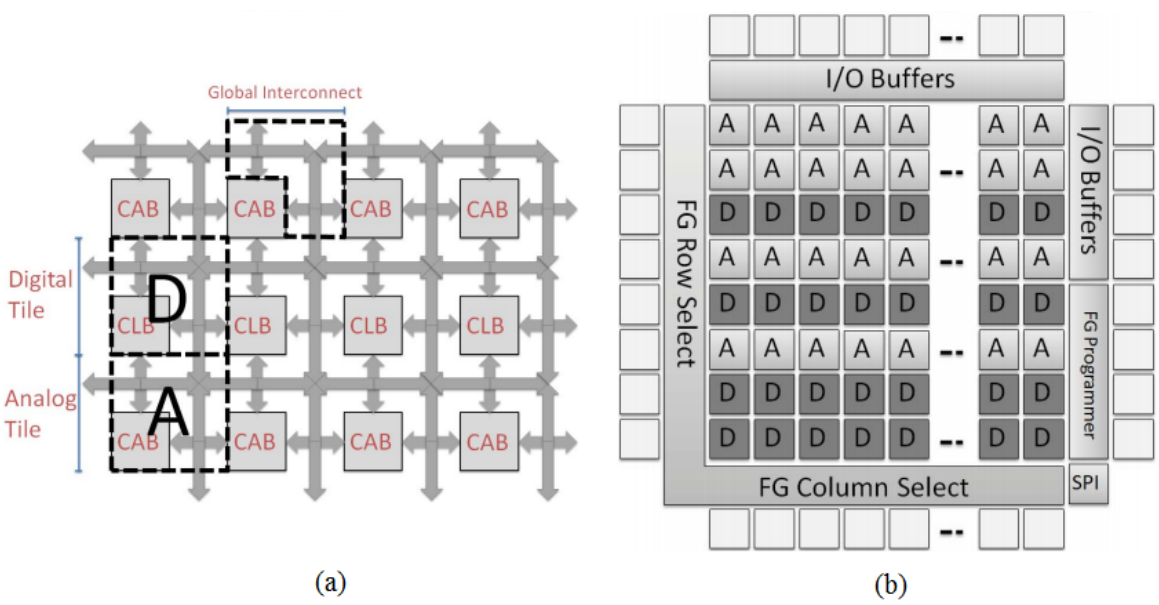

Figure 1.12. General architecture of the FPAADD. (a) Interchangeable digital and analog tiles are built from either a CLB or a CAB with reconfigurable routing that allows signals to propagate between tiles (global interconnect). (b) Top level. Blocks not to scale [7].

programmable delays, current biases and analog vector matrix multipliers. Fig. 1.13 depicts the FG transistor programming architecture.

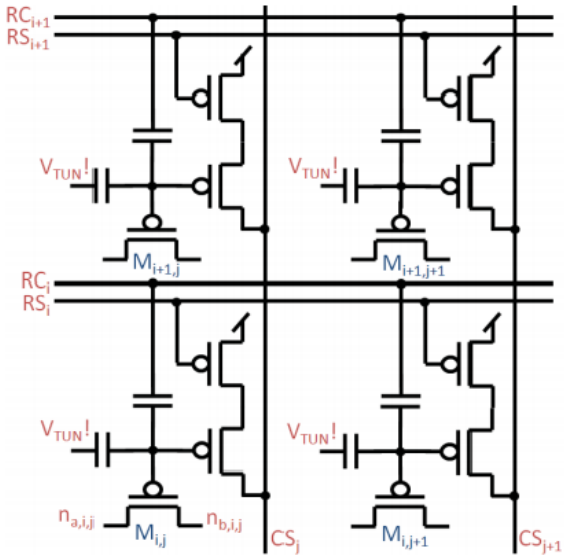

Figure 1.13. Programming is achieved by globally removing charge from the FG nodes through C_{TUN} via Fowler–Nordheim tunneling, and then selectively adding charge through $M_{i,j}$ with impact carrier hot channel electron injection. Injection of charge per row is controlled by the selection lines CS_i, and per column by the drain lines CS_i [7].

2. ANALOG PART OF FPMA

Some important development factors of FPAAs are discussed in Section 1.2. Design of analog circuits is more complex comparing to digital design since, analog design has many trade-offs as mentioned in previous sections. Despite of all these difficulties analog circuits are still required beside digital circuits in many applications. In order to overcome some of these difficulties, it is beneficial to use a circuit design which implements various analog functions. FPAAs are used for this purpose.

Design issues of FPAA are discussed in previous section. The FPAAs are grouped into continuous or discrete-time domain, voltage or current mode designs. A number of FPAA designs are introduced in previous sections. Some of these include discrete-time switch capacitor techniques [5], sub-threshold MOS operation [8]. Some of commercially available discrete and continuous time FPAA devices are mentioned such as Anadigm, Lattice, Cypress and Zetex. However some of these topologies have limited bandwidth and programming flexibility. One of the important design issues for FPPAs is granularity which defines the level of programmable units. Some topologies are based on fine-grained granularity which consist of CABs which are programmable at transistor level. In coarse-grained topologies, CABs contain macro level configurable blocks. For instance in switch capacitor designs, the main macro blocks are operational amplifier (OPAMPs). In coarse-grained topologies, CABs might contain macro blocks such as operational transconductance amplifier (OTAs), OPAMPs, resistors, capacitors banks, switches, transmission gates, etc. By connecting these blocks and tuning them it is possible to implement an analog function or a building block of an analog application such as gain stages, filters, summing and difference amplifiers, current to voltage, voltage to current conversion circuits, vector matrix multipliers, variable gain amplifiers (VGA), etc. Routing architecture is another design issue which is discussed briefly in previous sections. The routing task is much more important in design of analog arrays comparing to digital arrays since, switches and wires are used in interconnect have a great influence on analog signal. The noise, parasitic capacitances, resistances and nonlinearity are introduced by routing elements and degrade the both

programmability and functionality of analog circuits.

2.1. Analog Array Architecture

As illustrated in Figure 2.1a. the analog part of proposed FPMA consist of an arrays of configurable analog blocks (CAB). These programmable cells are placed in two dimensional network similar to Island-Style Routing Architecture which is discussed in Section 1.1.2. The routing network is distributed throughout an array of blocks in a way that each block is surrounded by several wire channels. The connections between CABs can be made via transistors that are used as switches between local wires for connecting to the nearby units, or global wires for connecting two units that are far from each other. Transmission gates are used in interconnect network in order to avoid voltage drops in the signal path and these gates are controlled by SRAM cells in the control circuit. Figure 2.1b. depicts the interconnections between CABs. It is possible to make a connection between inputs and outputs of each CAB either by itself or nearby CABs through switches that connect local wire segments. Also it is possible to form a connection between horizontal and vertical channels using switch boxes; therefore, this provides a possibility to make connections between two CABs that are far from each other. With such a routing network each analog block in one CAB can be connected to the other blocks either in the same or different CABs.

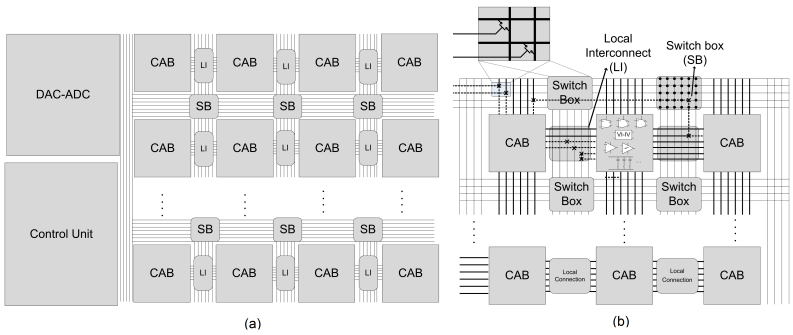

Figure 2.1. Analog part of proposed FPMA. (a) Analog core of FPMA consists of CABs and routing network. (b) Each CAB can be connected to nearby CABs with local interconnect (LI). Switch boxes (SB).

2.2. Analog Design Challenges In Sub-micron Technologies

Designing reconfigurable circuits brings new difficulties especially for the analog arrays as the technology scales down to 100nm and below. Digital circuits benefit from the advantages of technology scaling since, it is possible to achieve high performances for digital circuits with small geometry transistors. However, analog circuits usually suffer from the increasing non-ideal effects in sub-micron technologies. Some of these non-ideal effects are increased leakage current, gain reduction, poor matching, non-linearity and low voltage head-room. Some of non-ideal effects which are introduced by 90nm technology will be discussed in this section [25].

- Gain reduction in moderate inversion

  Generally the voltage gain of an analog circuit depends on the on-resistance of active load transistors at the output stage. The value of output resistance depends on either bias current and Early voltage (V_A). Transistors in TSMC-90nm suffers from low Early voltage; therefore, this cause a significant reduction in output resistance and consequently obtaining low voltage gain.

- Low supply voltage

  The supply voltage in sub-micron technologies has been decreased to 1.2V. However low supply voltage means low power consumption, it implies some limitations in performance of analog circuits. Biasing transistors in low supply voltage is a difficult task since, the voltage amount to be used by each transistor will be decreased. Especially in cascode and telescopic cascode structures, it is challenging to have all the transistors operate in saturation region, rendering such circuits unreliable. Moreover, low supply voltage implies low input common mode voltage range, and low input and output voltage swing.

- Gate leakage

  Sub-micron technologies suffer from high gate leakage since the gate oxide thickness shrinks nearly to level of atom diameter, the gate current increases one order of magnitude. Gate leakage mismatch dominates the long transistor mismatch. This phenomena limits the achievable maximum matching performance. This problem can be solved by either using more power or using active cancellation techniques [26].

- Velocity saturation and mobility degradation

  As high electric field is applied between source and drain, the carriers velocity reaches its maximum level. This phenomenon is known as velocity saturation [27]. In this state carriers velocity remains constant with increasing electric filed. Velocity saturation even becomes more dominant in small geometry devices. If a transistor operates in velocity saturation state, its current does not increase linearly with applied voltage; therefore, it introduces non-linearity and distortion. Mobility degradation is another phenomenon, which is more pronounced in sub-micron technologies [28]. The voltage applied to the gate of transistors creates a vertical electrical field and this field causes the carriers to scatter more frequently; therefore, it degrades the mobility of carriers. Mobility degradation causes drain current and DC transfer function of analog circuit to be non-linear.

2.3. Configurable Analog Blocks (CABs)

The main objective in developing reconfigurable analog devices such as FPAA and FPMA is to make analog design more practical for a wider range of designers, reduce the costs of prototyping analog systems, and make digital FPGAs whole by inclusion of an analog reconfigurable core, making reconfigurable System on a Chip

(SoC) solutions possible. There are two ways to establish reconfigurability in an analog system. First, various types of commonly used analog building blocks must be available for selectively connecting and disconnecting via their pins. Second, a mechanism to change the operating point of an analog building block should be available to satisfy different circuit specifications. The collection of reconfigurable analog blocks is called a CAB.

The trade-off between performance and functionality should be considered for designing configurable analog blocks. Hence, it is feasible to choose the most suitable and reliable circuits topologies with satisfying performance. In order to opt the most appropriate and commonly used analog blocks, a literature survey is conducted. Numerous papers presenting various analog designs and applications in last three years are reviewed within journals; IEEE Journal of Solid State Circuits (JSSC), IEEE Transactions on VLSI, Systems (TVLSI) and IEEE Transactions on Circuits and Systems (TCAS), and within the conference papers; IEEE International Symposium on Circuits and Systems (ISCAS), International Solid-State Circuits Conference (ISSCC), IEEE International System-on-Chip Conference (SOCC). Table 2.1 lists the mostly used analog blocks in analog circuit implementations in last three years.

As listed in Table 2.1, OPAMPs and OTAs are two mostly used analog blocks in many applications. Variable gain amplifiers are also one of the essential analog blocks for providing programmability. It is possible to construct VGAs using tunable OTAs. Low noise amplifiers (LNAs) are also needed for pre-amplification purposes since, it may require to amplify the input signal before the main analog blocks to prevent performance distortion caused by the circuit noises.

The CABs in the proposed FPMA IC contains common circuits such as amplifiers, converters to convert signals between voltage and current modes, and comparators as demonstrated in Figure 2.2. Amplifiers included are either programmable Output Transconductance Amplifiers (OTA) with tunable transconductance (g_m) to be used flexibly for a wide range of applications or fixed-bias OPAMP to be used for

Table 2.1. Most used analog blocks during last three years.

Block	Number of times appearing in an article
Amplifiers	30
OPAMP, OTA, etc	236
VGA	41
LNA	40
Power amplifier	13
Comparators	67
Oscillators	61
Filters / Integrators	60
ADC	57
DAC	57
Mixers / Multipliers	38
Biasing circuits	27
Charge pumps	24
Buffer circuits	15
PLL	15
V/I converters	11

certain tasks such as buffering. In addition to these basic circuits, capacitor banks are also available in CABs.

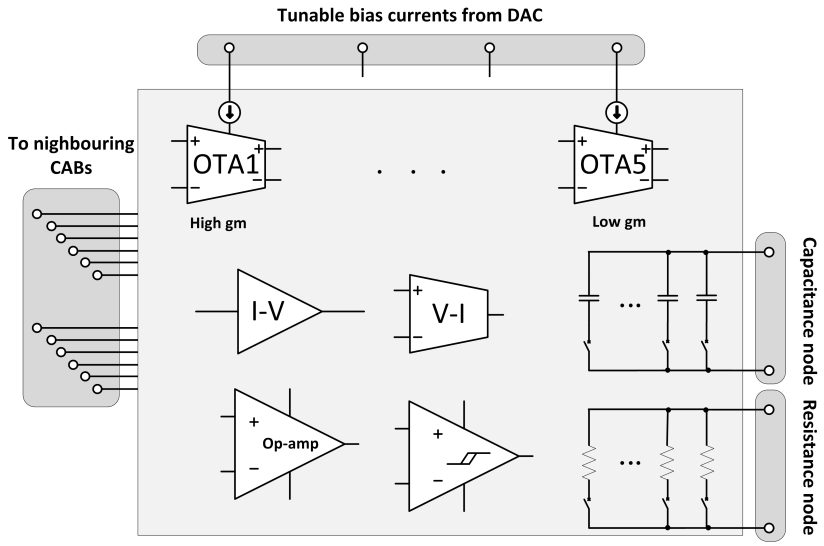

Figure 2.2. Configurable analog block (CAB) consists of programmable transconductance, capacitor and resistor arrays and fixed analog circuits including voltage to current, current to voltage converter, wide common-mode range OPAMP and comparator.

One should also not forget that there is also the cost of reconfigurability for the analog circuits used in FPAA or FPMA devices, which manifests itself as the overhead of the additional switches and excessive wire lengths between the different components on the signal path compared to a hardwired design. Analog circuits cannot tolerate excessive number of switches on the signal path; therefore, routing resources that connect the analog components must be planned and used carefully both when designing the FPMA routing topology and when implementing designs on FPMA later.

3. DESIGN AND LAYOUTS OF ANALOG BLOCKS WITHIN CABS

3.1. Tunable Operational Transconductance Amplifier (OTA)

Figure 3.1 depicts the topology of the programmable OTA, which is a single stage folded-cascode OTA with PMOS input transistors and differential output. $M_{1,2}$ comprise an input, PMOS differential pair with drain currents received by NMOS folded cascode devices $M_{7,8}$. The $M_{7,8}$ drains are connected directly to the OTA output. The NMOS devices $M_{3,4}$ are current sources which supplies the drains of input differential pair and source of $M_{7,8}$ folded-cascode devices. The biasing circuit (Figure 3.2) separated from signal path consisting of appropriately sized rail devices $M_{b1,b4}$ and cascode devices $M_{b1,b4}$, provides a reference voltages $V_{b1,b2}$ for $M_{7,8}$ and $M_{9,10}$ devices.

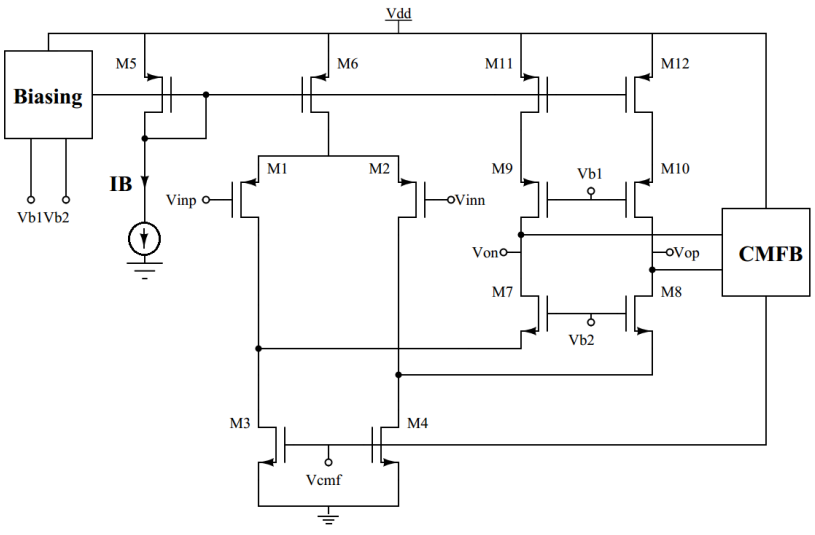

Figure 3.1. Fully differential cascode OTA with PMOS input pair transistors. This transconductance is biased using varying tail current that is provided by current DAC.

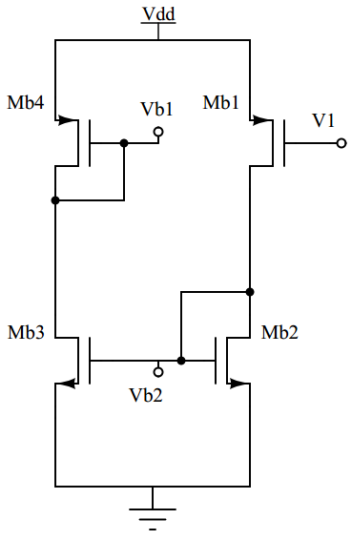

Figure 3.2. Biasing circuit for generating reference voltages $V_{b1,b2}$.

OTA transconductance (Gm) is equal to G_m of the input transistors $M_{1,2}$, and using PMOS transistors at the input is preferred for reducing the noise of the amplifier. OTA transconductance is approximated by the transconductance of the input transistors. The transconductance (G_m) of individual input pair devices is given by

$$G_m = g_{m1,2} = \frac{2I_b}{V_{ov}} = \sqrt{2K_{1,2}I_b} \tag{3.1}$$

Where the V_{ov} is effective gate-to-source voltage, I_b is tail current and $K = \mu C_{ox} W/L$. Then the voltage gain of proposed OTA can be written as

$$A_v = G_{m1,2} R_o \tag{3.2}$$

Where R_o is the output resistance and it can be written as

$$R_o = r_{up} \parallel r_{down} = (g_{m10} r_{o10} r_{o12}) \parallel [(g_{m8} r_{o8})(r_{o4} \parallel r_{o2})] \tag{3.3}$$

Equation 3.3 can be expressed using $r_{ds} = \frac{V_{AL}.L}{I_D}$ and this gives

$$R_o = r_{up} \parallel r_{down} = \frac{V_{AL8}.L_8}{V_{ov8}}[(\frac{V_{AL2}.L_2}{I_{D2}}) \parallel (\frac{V_{AL4}.L_4}{I_{D4}}) \parallel (\frac{V_{AL12}.L_{12}}{I_{D12}})] \tag{3.4}$$

Finally, the gain for the cascode OTA 3.2 is equal to the product of G_m from Equation 3.1 and R_o from Equation 3.4 as given by

$$A_v = G_{m1,2}R_o = \frac{2I_b}{V_{ov1,2}}\frac{V_{AL8}.L_8}{V_{ov8}}[(\frac{V_{AL2}.L_2}{I_{D2}}) \parallel (\frac{V_{AL4}.L_4}{I_{D4}}) \parallel (\frac{V_{AL12}.L_{12}}{I_{D12}})] \tag{3.5}$$

From Equation 3.1, it can observe that the transconductance of OTA can be tunned by altering the bias current; However, the overdrive voltage (V_{ov}) is also affected when I_b is varied, because of the fact that the transistor geometry cannot be altered once the IC is fabricated. Therefore, OTA Gm can be tuned by varying I_b alone only within a certain range before the transistors leave the active region. The effect of bias current on voltage gain in Equation 3.5 can be neglected since current terms in nominator and denominator cancel each other. The gain of proposed OTA depends on V_{ov}, lengths of transistors and early voltage values V_{AL2}. Therefore, the gain of OTA will changed few dBs by changing the tail current.

To stabilize the DC voltage level of the output, a common mode feedback (CMFB) circuit (Figure 3.3) that provides the bias voltage for transistors $M_{3,4}$ is designed. If the voltage of outputs ($V_{op,on}$) changes differentially the V_{CMF} remains constant but, if for instance the common mode voltage of both output nodes increases, the drain current of $M_{13,14}$ decrease and this leads to current rise in M_{20}; therefore, the V_{CMF} increases. If the gate voltage of $M_{3,4}$ increases, these pairs pull the output common voltage down; therefore, prevent increasing the common-mode level.

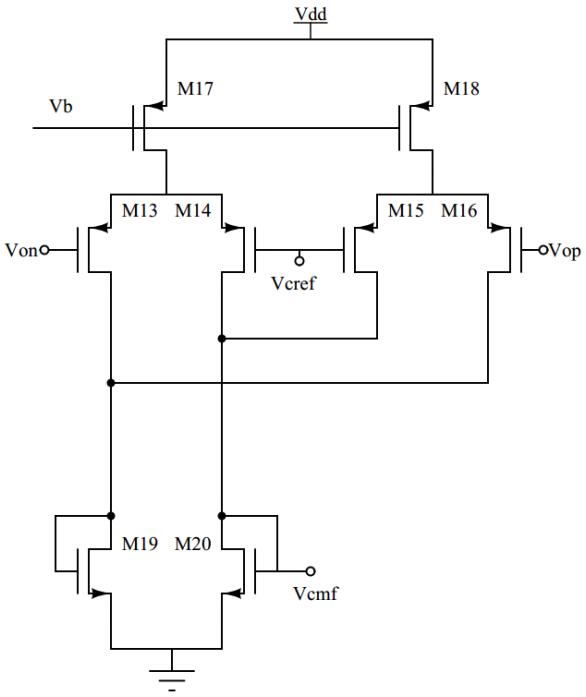

Figure 3.3. Common mode feedback circuit.

The proposed OTA is designed to be biased with varying tail current in a range over 10 to 100 μA. Figure 3.4 illustrates the simulated V-I curves and transconductance of OTA with different bias currents. Figure 3.5 depicts the simulated AC frequency response of Proposed OTA with different bias currents. It can be observed that the DC gain remains constant (around 54 db) with varying bias current as described in Equation 3.5. Table 3.1 summarizes some of the simulated results which are obtained from OTA.

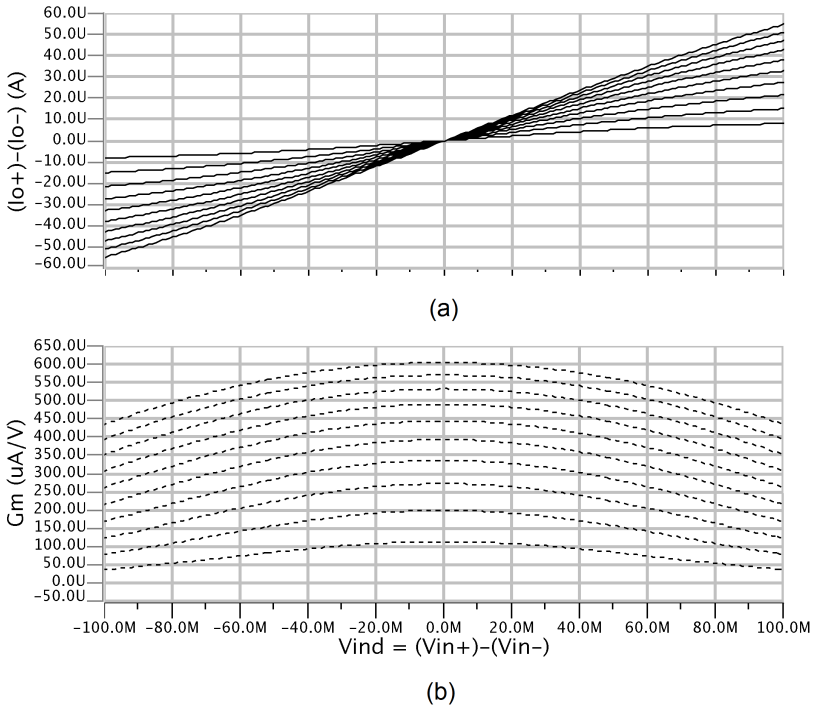

Figure 3.4. DC transfer curves of proposed OTA with different bias currents (10-100 μA). (a) Output current $i_o = i_{o+} - i_{o-}$ versus input differential voltage $v_{id} = v_{i+} - v_{i-}$ curves. (b) transconductance $G_m = i_o/v_{id}$ curves.

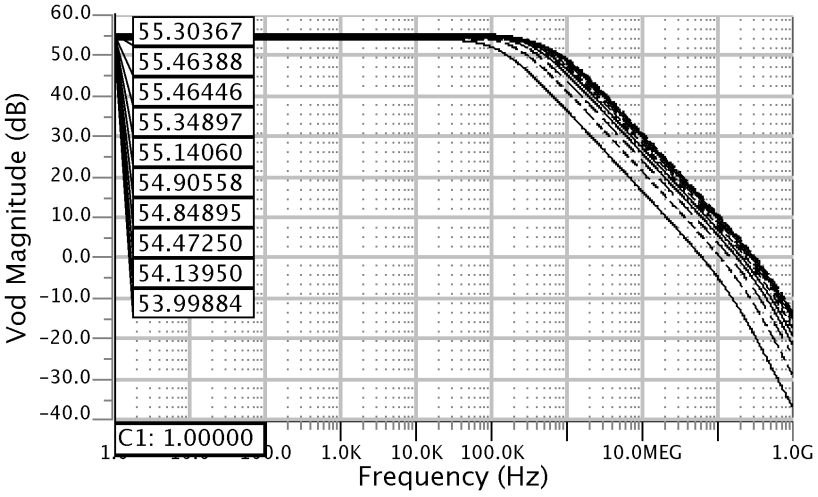

Figure 3.5. AC frequency response of proposed OTA with different bias currents (I_B = 10-100 μA).

Table 3.1. The summery of OTA performance (Schematic).

Technology	TSMC 90-nm
VDD	1.2v
Voltage Gain	>54 dB
Ibias	10-100 μA
UGB ($C_L = 500fF$)	70-320 MHz
Phase Margin	>67 dB
CMRR	85 dB
Max Power consumtion	54-457 μ W
G_m range	100-600 μ A/V
PSRR	>70 dB
Total area (Layout)	$\approx 36 \times 46\ (\mu m)^2$

As discussed previously, OTA Gm can be tuned by varying I_B alone only within a certain range before the transistors leave the saturation region. Therefore, to obtain wider range of Gm values with all transistors of the OTA operating in the saturation region four OTAs of the same topology but different transistor geometries are designed. As the fifth type, the topology of the OTA is slightly modified by including current division method [29,30] as depicted in Figure 3.6 to obtain very low Gm values. Using this configuration the total G_m will be reduced to

$$G_m = g_{m1,2} - g_{mCS1,2} - g_{mCS3,4} \tag{3.6}$$

However current devision approach has some disadvantages. Transistors $M_{CS3,CS4}$ are used for current stealing purpose and most of the bias current flows through these pairs; therefore this cause the remaining transistors biased with very low drain current and enter subthershod region. Obtaining a low voltage gain from OTA is another drawback of using this structure.

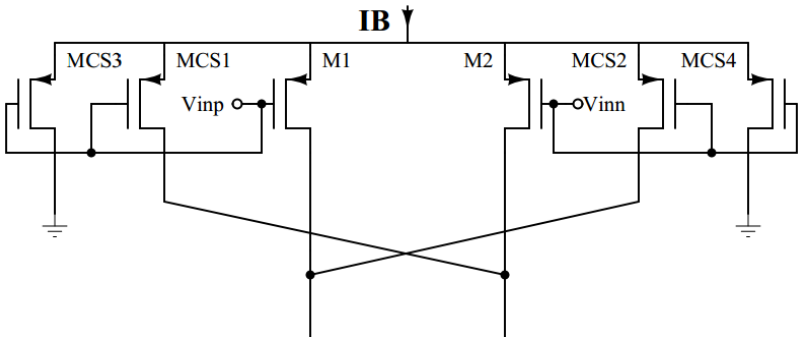

Figure 3.6. Current division configuration used at the input stage for minimizing the value of GM in OTA type 5.

Table 3.2. Characteristics for different types of OTAs.

OTA Type	**Gm Range**	**Gain**	P_{max}	**IRN**	**Area**
OTA t.1	100-600 μ A/V	>54 dB	457 uW	12 nV/Hz	1000 um^2
OTA t.2	80 - 10 μ A/V	>60 dB	53 uW	30 nV/Hz	200 um^2
OTA t.3	8 - 0.5 μ A/V	>51 dB	5.2 uW	100 nV/Hz	300 um^2
OTA t.4	300 - 45 nA/V	>46 dB	607 nW	300 nV/Hz	400 um^2
OTA t.5	4 n - 300 p A/V	>20 dB	300 nW	40 uV/Hz	500 um^2

Table 3.2 presents the metrics obtained from the five programmable OTAs, including Gm range, maximum power (P_{max}), input referred noise (IRN) and occupied area. Using the programmable interconnects, multiple OTAs of the same type or different types can be connected in conjunction with other circuit elements to build various circuits such as filters.

Figure 3.7 shows the Monte Carlo simulations results of OTA t.1. Output DC gain has been measured in 200 simulations in which all transistors vary in both sizes and parameters randomly in order to include the process variation after fabrication.

Among 200 simulation 92 of them are giving the desired voltage gain and operating in desired region. The rest can be fixed certainly by doing a precise layout design.

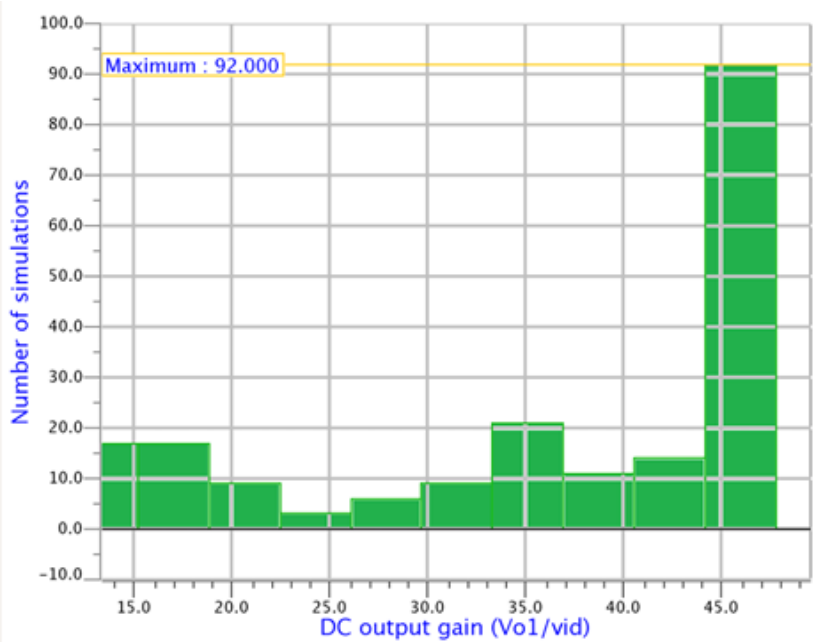

Figure 3.7. Monte Carlo simulation results in which the DC gain of OTA t.1 is measured in 200 simulations.

3.2. Wide Common-mode Range OPAMP

Although OTAs are sufficient for on-chip amplification purposes since the inputs of the subsequent stages are mostly capacitive, OPAMPs are still required for buffering, signal conversion, adding, summing signals and some other common tasks. One of the siginifacnt factors in designing op-amps is input common-mode voltage rage. As discussed in Section 2.2 using low supply voltage for designing analog circuits in advanced technologies, implies some performance limitations. One of these limitations is low common-mode input voltage range. Figure 3.8 shows the two configurations that are commonly used as input stage in designing OPAMPs and OTAs.

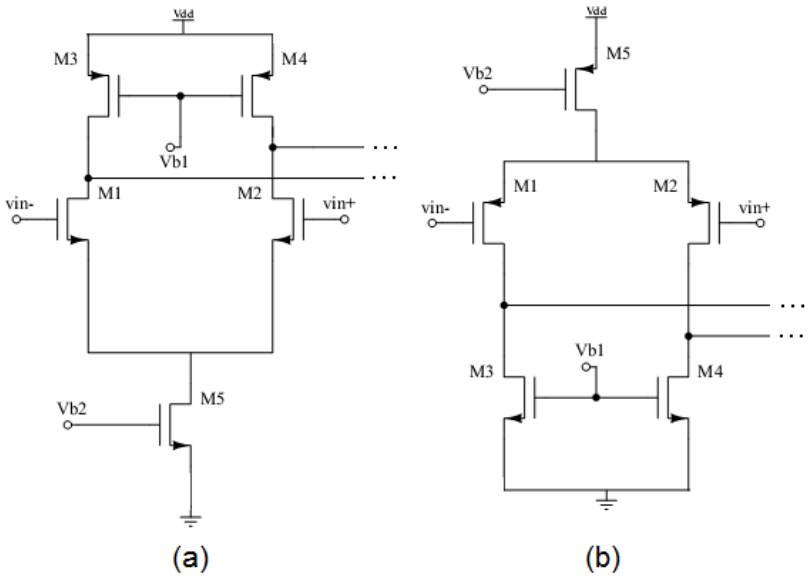

Figure 3.8. Two commonly used input stages configurations. (a) Input stage with NMOS input differential pair. (b) Input stage with PMOS input differential pair.

To find the input common-mode voltage range, both positive and negative differential input is connected to DC common-mode voltage (V_{cm}). The maximum and minimum value of V_{cm} is limited by the requirements that $M_{1,2}$ operate in saturation region. Assuming that the $M_{3,4}$ are operating at the edge of saturation, the input voltage common-mode range for NMOS input pair configuration can be written as

$$V_{ov5} + V_{ov1} + V_{tn} \leq V_{cmN} \leq V_{DD} - |V_{ov3}| + V_{tn} \tag{3.7}$$

And similarly for PMOS input pair is given by

$$V_{ov3} - |V_{tp}| \leq V_{cmP} \leq V_{DD} - |V_{ov1}| - |V_{ov5}| - |V_{tp}| \tag{3.8}$$

It is desirable to choose the value of overdrive voltages (V_{ov}) as low as possible since, V_{ov} subtract from the dc supply voltage and it leads to reduction in the input common-mode voltage. Therefor for NMOS input stage (Figure 3.8a.), while the upper limit on the input voltage common-mode range exceeds the supply voltage, the lower limit is

significantly higher than ground. The opposite situation occurs for the configuration depicted in Figure 3.8b. In this case the upper limit is significantly lower than supply voltage.

The threshold voltage of standard transistor models in TSMC-90nm is around 0.3 volt approximately. According to Equation 3.7, by choosing low overdrive voltage around 0.1 volts, the minimum input common mode voltage for NMOS input configuration is

$$Vmin_{cmN} = V_{ov5} + V_{ov1} + V_{tn} = 0.1 + 0.1 + 0.3 = 0.5 \tag{3.9}$$

It is obvious that the input common-mode voltage should be greater than 0.5v; however, this is a significant problem for designing an OPAMP with 1.2v supply voltage. The solution for this limitation is using PMOS and NMOS differential pair in parallel that provides wide common-mode range which is known as rail-to-rail input configuration. Figure 3.9 shows the proposed OPAMP.

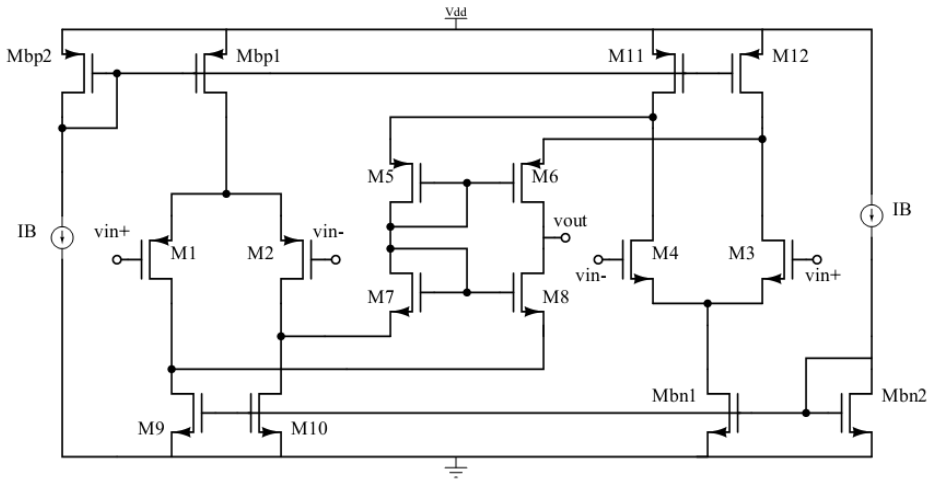

Figure 3.9. Proposed wide common-mode range OPAMP

Two possessive and negative input terminals are to be connected together. Transistors. Transistors $M_{5,6}$ are the cascode transistors for $M_{3,4}$ and transistors $M_{7,8}$ are cascode devices for $M_{1,2}$ input pair. Assuming $G_m = g_{m1} = g_{m2} = g_{m3} = g_{m4}$ the voltage gain

can be written as

$$A_v = 2G_m R_o \tag{3.10}$$

Where R_o is the output resistance. The circuit topology of proposed OPAMP is similar to cascode OTA which is discussed in previous section; therefor, typically the voltage gain of maximum 50dB may be obtained from this OPAMP. Moreover, the output resistance will be too high in this case. Hence, as illustrated in Figure 3.10, to increase the gain and reduce the output resistance, a basic common-source second stage is cascaded with OPAMP.

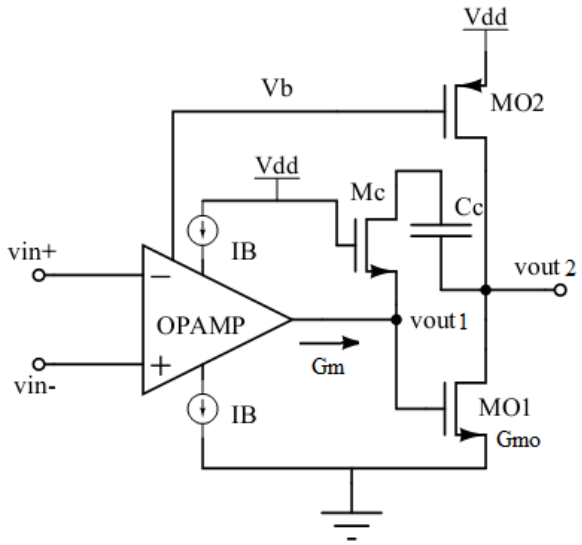

Figure 3.10. Proposed OPAMP is cascaded with second stage which is common source configuration

Adding a second stage has an advantages in terms of achieving high gain and low output resistance; however, it implies some draw backs such as bandwidth reduction and more area usage. Also second stage adds a second pole to the transfer function of system and therefore to assure suitable phase margin (PM), it requires to add a compensation circuit. For this purpose RC compensation technique is used at output terminal of OPAMP in order to achieve better phase margins. In this approach an

additional capacitor (Cc) and single transistor which operates in linear region (Mc) is used for compensation purpose. For obtaining reasonable phase margin the compensation capacitor (Cc) and the on resistance of Mc should be chosen as

$$C_c{>}0.3C_L, \qquad R_{onMC} = \frac{1}{G_{mo}} \tag{3.11}$$

where the C_L is a load capacitance and the transconductance of NMOS transistor M_{o1} is designed to be

$$G_{mo}{>}10G_m \tag{3.12}$$

In this case, the total voltage gain is given by

$$A_v = \frac{V_{out1}}{V_{ind}} \times \frac{V_{out2}}{V_{out2}} = (2G_m R_o) \times (G_{mo} R_{o2}) \tag{3.13}$$

Where $R_{o2} = R_{Mo1}||R_{Mo2}$ is the output resistance of second stage. Finally, the unity gain bandwidth (UGB), first pole and second pole of the transfer fucntion of whole system is given by

$$UGB \approx \frac{2G_m}{C_c}, \qquad p_1 \approx \frac{1}{R_o Cc}, \qquad p_2 \approx \frac{1}{R_{o2} CL} \tag{3.14}$$

Figure 3.11 and 3.12 depicts the AC frequency response of OPAMP and transient pulse response of unity gain buffer constructed using proposed OPAMP. Table summarizes the characteristics of the designed OPAMPs.

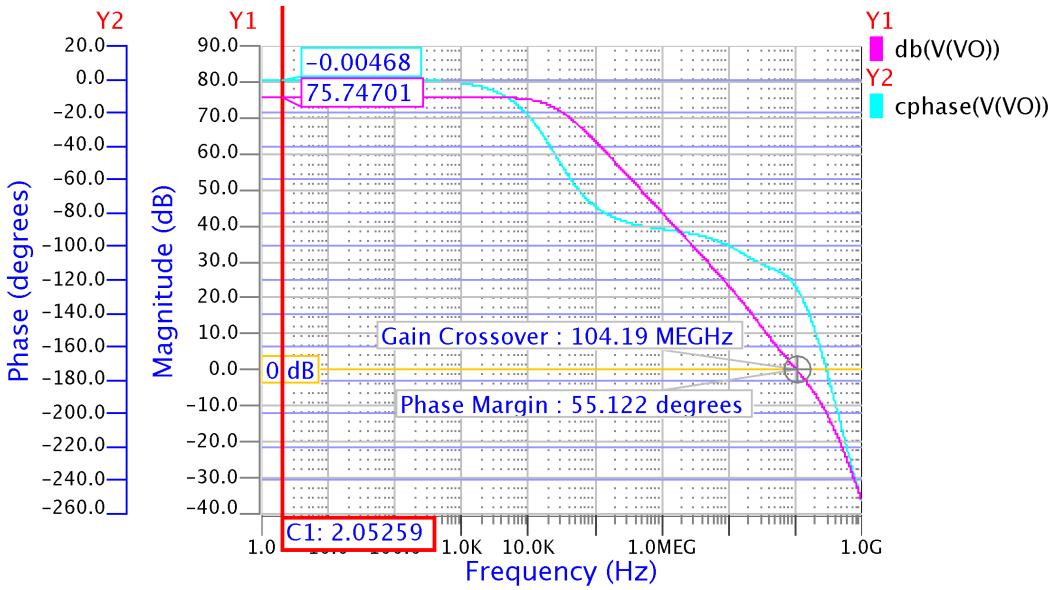

Figure 3.11. AC frequency response of OPAMP ($C_l = 1pf$)

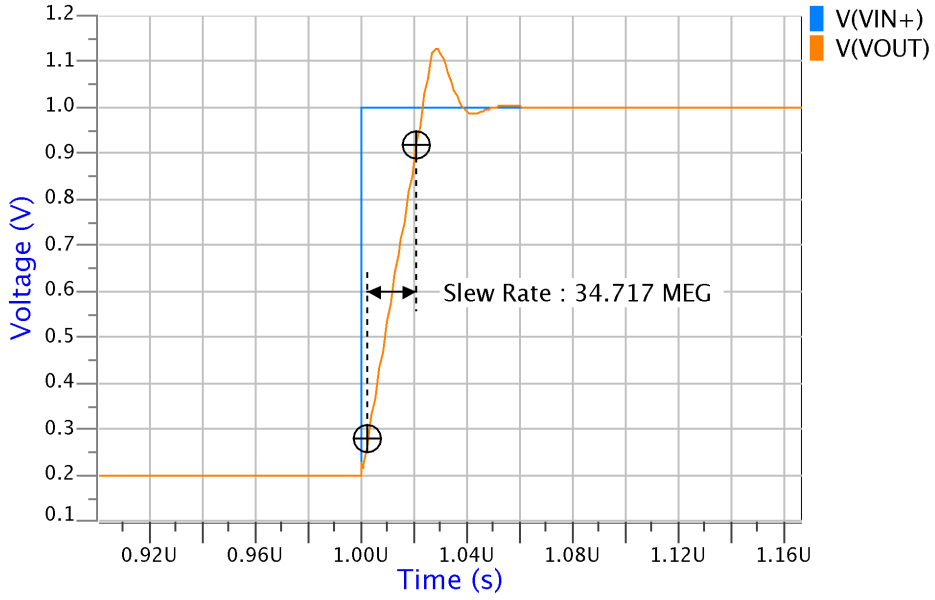

Figure 3.12. transient pulse response of unity gain buffer constructed using proposed OPAMP.

Table 3.3. The summery of OPAMP performance (Schematic).

Technology	TSMC 90-nm
VDD	1.2v
Voltage Gain	75.7 dB
IB	100u μA
C_c	1p F
UGB ($C_L = 500fF$)	104 MHz
Phase Margin	55 dB
Slew rate	35 Meg V/S
CMRR	70 dB
Max Power consumption	270 μ W
Total area (Layout)	2000 $(\mu m)^2$

3.3. Linear Voltage To Current Converter (Linear OTA)

In current-mode mixed signal systems, V-I and I-V converters can be used for interfacing voltage and current mode analog circuits. Wide linear range and bandwidth are the most important specifications for these converters. A combination of linearization techniques was used in some high performance designs reported earlier [31], [32]. OTAs are types of V-I converters as they operate similar to voltage-controlled current source. For some filter applications OTA should have high linearity and low-distortion. In Section 2.2 it is discussed that, as advanced VLSI technologies are scaled down to sub-micron level, many factors such as mobility degradation and velocity saturation become more dominant and impose nonlinear effects on devices. Moreover, low voltage headroom forces the signal swing become less. Therefore, achieving a high linearity with big input signal swings becomes a challenge. Especially in 90nm transistors suffer from low Early voltage and high non-linearities. The major disadvantages of V-I converter is signal distortion induced by the nonlinear behavior of transistors. Hence

to achieve a linear performance for V-I, numbers of various techniques of linearity improvement has been introduced. For voltage to current converter circuit, the cascode OTA topology which is discussed in Section 3.1 is modified. In Section 3.1 the DC transfer function of cascode OTA is presented in Equation 3.1; However, some terms has been ignored. If it is been written precisely, the relationship between input voltage, transconductance G_m and output current is given by

$$i_o = G_m v_{id} \sqrt{1 - (\frac{v_{id}}{2V_{ov}})^2} \tag{3.15}$$

However it might be ignored for high effective gate-to-source voltages, the second term under the square root will cause linearity defections. Specially for low-voltage applications it is a major problem. Hence, a combination of linearizion techniques are applied for attenuation and canceling the second term. The first approach is current division method which is used for canceling the third harmonic components. Second method is adding R for source degeneration. In previous conventional methods resistors are used as elements for source degeneration. In this work resistors are replaced by transistors operating in triode region.

Linearization Techniques:

- Current division method .

  The current division method is used in some implementations [33] for canceling the nonlinearity. This approach is implemented on proposed V-I converter using additional differential input pair as shown in Figure 3.13. In this work, current division technique is enhanced in order to avoid transconductance loss and high power consumption. Transistors are sized smaller relatively and no resistors are used for achieving less area usage. Assuming $v_{id} = v_{in+} - v_{in-}$ as input differential voltage and v_{ov} as an effective gate-to-source voltage with output current of $i_o = (i_{o1+} - i_{1o-}) - (i_{o2+} - i_{2o-})$, where the small signal transconductance for each pair is $G_{mi} = \sqrt{K_i I_{bi}}$, the Taylor series expansion of equation (3.15) (other

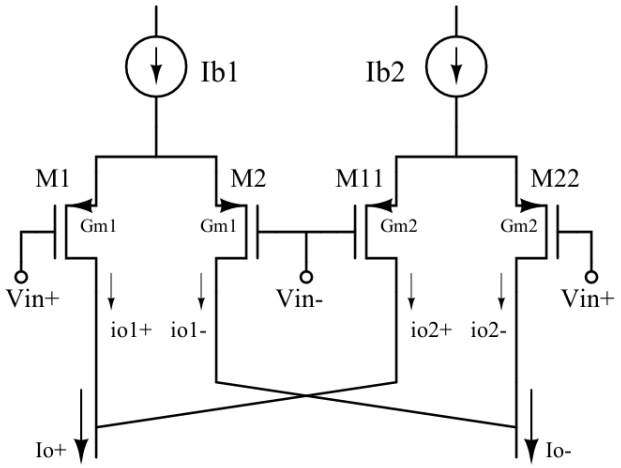

Figure 3.13. Configuration of current division transistors. Additional differential pair ($M_{11,22}$) are used to cancel the nonlinearity.

terms are neglected due to their minor contribution) can be written as

$$i_{oi} = G_{mi} v_{id} (1 - (\frac{1}{8(v_{ovi})^2}) v_{id}^2) \tag{3.16}$$

Where i=1 and 2 for $M_{1,2}$ and $M_{11,22}$ respectively. The third harmonic term will be canceled by choosing the optimum sizes for transistors $M_{1,2,11,22}$. In order to remove the third-harmonic term the following condition should be satisfied:

$$\frac{G_{m1}}{(v_{ov1})^2} = \frac{G_{m2}}{(v_{ov2})^2} \tag{3.17}$$

Where G_{m1} and G_{m2} are the trans conductances of transistors $M_{1,2}$ and $M_{11,22}$. Current division method improves the linearity; however it is not quite enough for total elimination of the third harmonic component due to non-ideal effects which are introduced in sub-micron technologies.

- Source Degeneration method

  One of the simple and prevalent techniques [34] to linearize the transfer charac-

teristic of V-I converter is source degeneration method using resistors; however it has some drawbacks such as high area consumption, extra thermal noise, tunability elimination, and the most significant the transconductance loss. Therefore in this work, resistors are replaced by MOS transistors which are operating in triode region. Source degeneration transistors ($M_{3,4,33,44}$) provides relatively high transconductance relatively if they are matched perfectly. Figure 3.14 depicts the addition of extra transistors to the source of transistors in previous topology. Combination of two techniques provides with better linearity since it attenuates the third harmonic term; moreover it increases the input voltage range. The transfer characteristics of this circuit can be written as

$$i_o = \frac{G_m v_{id}}{S}\sqrt{1 - 2(\frac{v_{id}}{SV_{ov}})^2} \tag{3.18}$$

where

$$S = 1 + \frac{\beta_{1,2}}{4\beta_{3,4}} \tag{3.19}$$

Adding a source degeneration transistors changes the equation (3.17) into

$$\frac{G_{m1}}{S_1^3(v_{ov1})^2} = \frac{G_{m2}}{S_2^3(v_{ov2})^2} \tag{3.20}$$

where S_1 and S_2 is for $M_{3,4}$ and $M_{33,44}$ respectively. It can be observed that the S parameter in the denominator suppress the component of third harmonic distortion. The disadvantage of this configuration is that according to 3.18 the S parameter also appears in main tone;therefore, the total trascondactance will be reduced into

$$G_{mtotal} = \frac{G_{m1}}{S_1} - \frac{G_{m2}}{S_2} \tag{3.21}$$

Contrary to implementation of source degeneration method with resistors, replacing them by MOS transistors prevent severe G_m loss.

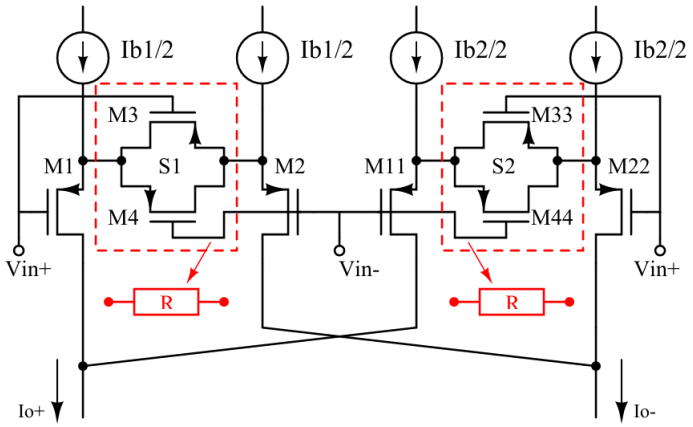

Figure 3.14. Configuration of current devision topology with source degeneration transistors $M_{3,4}$ and $M_{33,44}$.

Proposed OTA which was discussed in Section 3.1 (Figure. 3.1) is enhanced using mentioned techniques for achieving a linear transfer characteristics. The input transistors ($M_{1,2}$) are replaced with configuration in Fig. 3.14. The tail current is provided through mirror transistors which are connected to M_5. The cascode OTA is designed with $G_{m2} \simeq 8G_{m1}$, $I_{b2} \simeq 7I_{b1}$ and $S_2 \simeq 1.3S_1$ in order to satisfy the equation 3.20 which is obtained in Section 3.3. Figure 3.15 depicts the DC transfer curve and transconductance of V-I converter at bias current of 15μA and Figure 3.16 illustrates the DC transfer curves and transconductances of V-I converter while bias current changes over 1-15 μA. Output transconductance is constant for 400mV p-p input voltage; however, as bias current reduces the input range decreases because of the fact that, effective gate-source voltage decreases in low currents and this causes an increase in voltage gain. Higher gain causes higher output swings and consequently low linearity. The transconductance is still linear for $I_b = 1u$ at 200mv p-p input range.

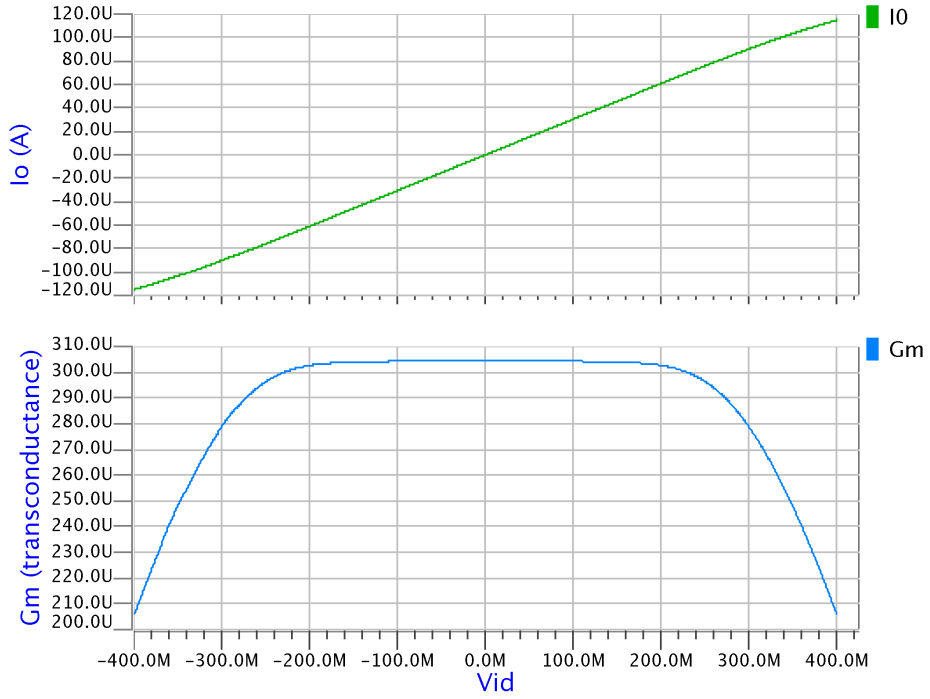

Figure 3.15. Simulated transconductance and DC transfer curves of linear V-I converter at bias current of 15μA.

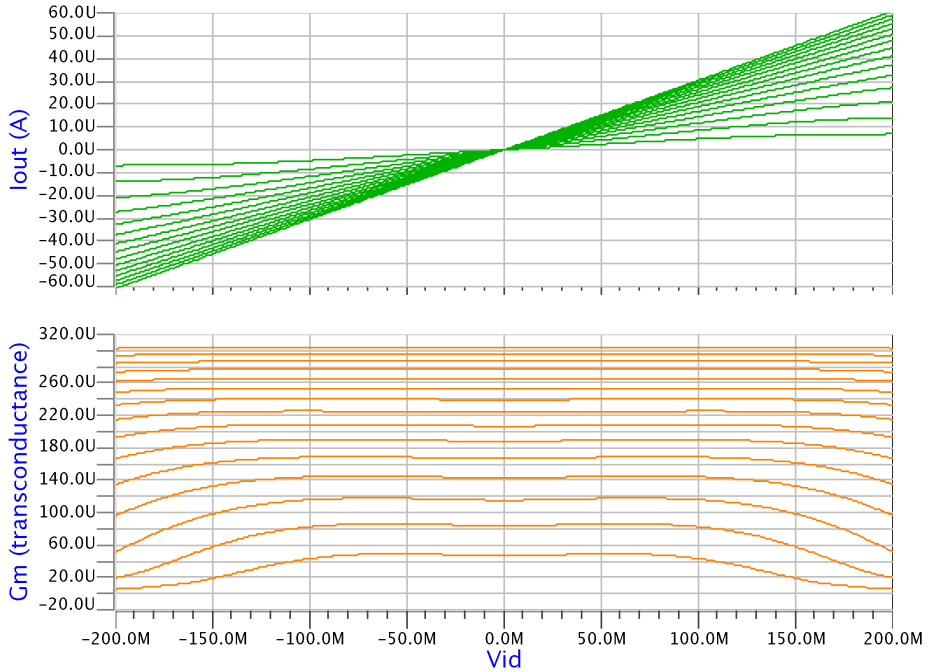

Figure 3.16. Simulated transconductances and DC transfer curves of linear V-I converter as bias current changes over range of 1-15μA.

In order to observe the linearity of output current power spectrum simulation is done using MATLAB. A signal at 1MHz frequency with amplitudes of 400mv and 200mv pp are applied to the input of proposed V-I converter. As shown in Figure 3.17 the HD3 of output current is -50dB and -54dB for 400mv and 200mv input pp voltage. Figure 3.18 depicts the comparison between the HD3 of the output current of linear OTA and non-linear OTA which is discussed in Section 3.1. As shown in the Figure the HD3 of the output current of linear OTA for 400mv input pp voltage is -31dB.

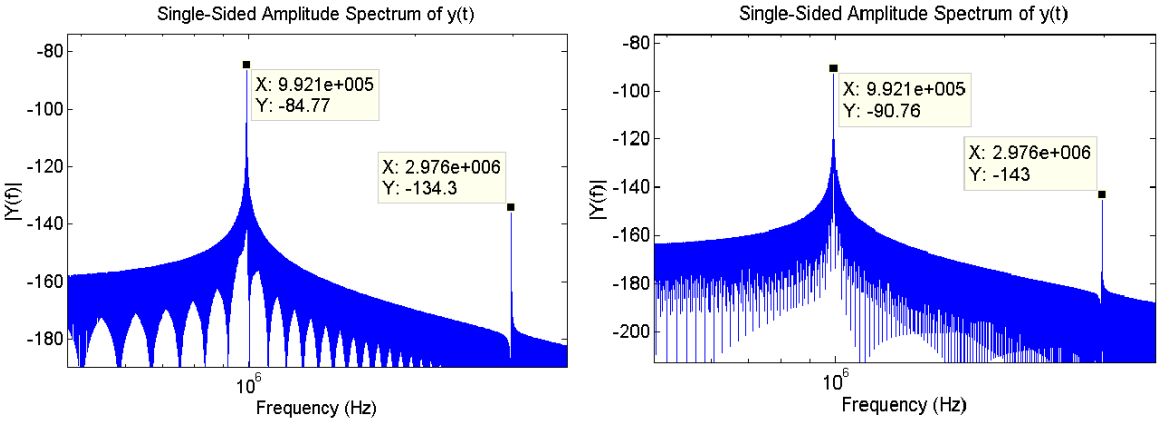

Figure 3.17. Power spectrum simulation of output currrent. (a) The original tone and third harmonic of output current with 400mv pp input voltage. (b) The original tone and third harmonic of output current with 400mv pp input voltage.

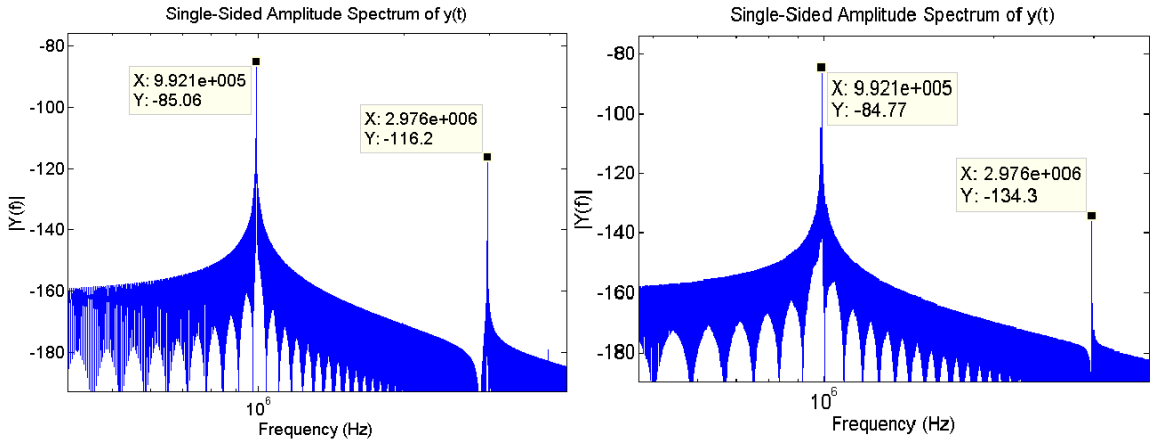

Figure 3.18. Power spectrum simulation of output currrent. (a) Power spectrum simulation of the output current of OTA with 400mv input pp voltage. (b) Power spectrum simulation of the output current of linear OTA with 400mv input pp voltage.

3.4. Dynamic Comparator

Comparator is another circuit type that can be used in various analog applications and data conversion as well as programming and calibrating the analog blocks of FPMA IC. Dynamic latched comparators are capable of sensing small input voltages in a very short time [35]; therefore, they are the preferred topology in this IC as well. Designed comparator has high input sensitivity, high speed and full-swing output. By optimizing transistor sizes at the input stage, the input referred latch offset voltage is minimized. Figure 3.19 illustrates the proposed dynamic comparator. The comparator circuit consist of two parts, first part is main comparator and second stage is a basic latch.

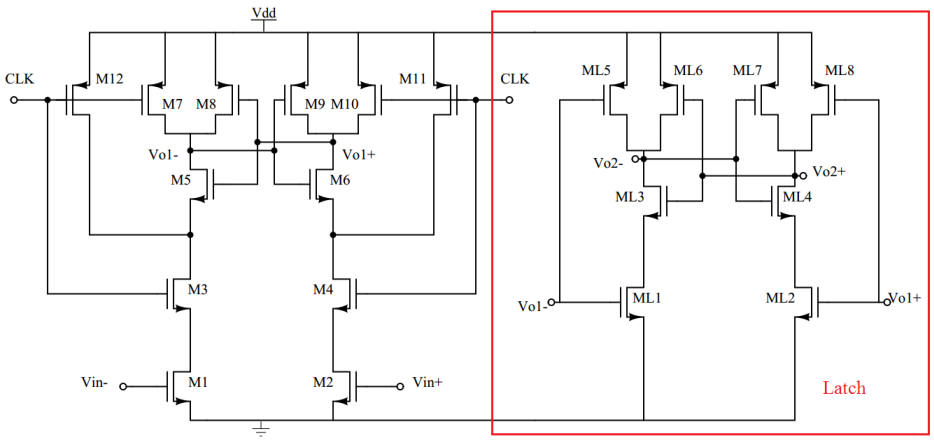

Figure 3.19. Schematic diagram of dynamic comparator with latch circuit in the second stage.

For main comparator operation, during the pre-charge, PMOS transistors are turned on (CLK=0) and the output is pulled to V_{DD} . The comparison begins when the clock is forced to V_{DD}. For instance, when the V_{in+} is higher than V_{in-} more current flows through $M_{2,4}$ and V_{o1+} is pulled to zero. Therefore, the gate of PMOS transistor M_8 will be sufficiently low to pull the V_{o1-} to V_{DD}. This also changes the outputs of latch circuit similarly and consequently the output voltages V_{o2+} and V_{o2-} will become V_{DD} and zero respectively. The latch circuit holds the previous output voltage values when the clock is forced to zero. The transient simulation wave forms obtained from proposed comparator are shown in Figure 3.21 and Figure 3.20.

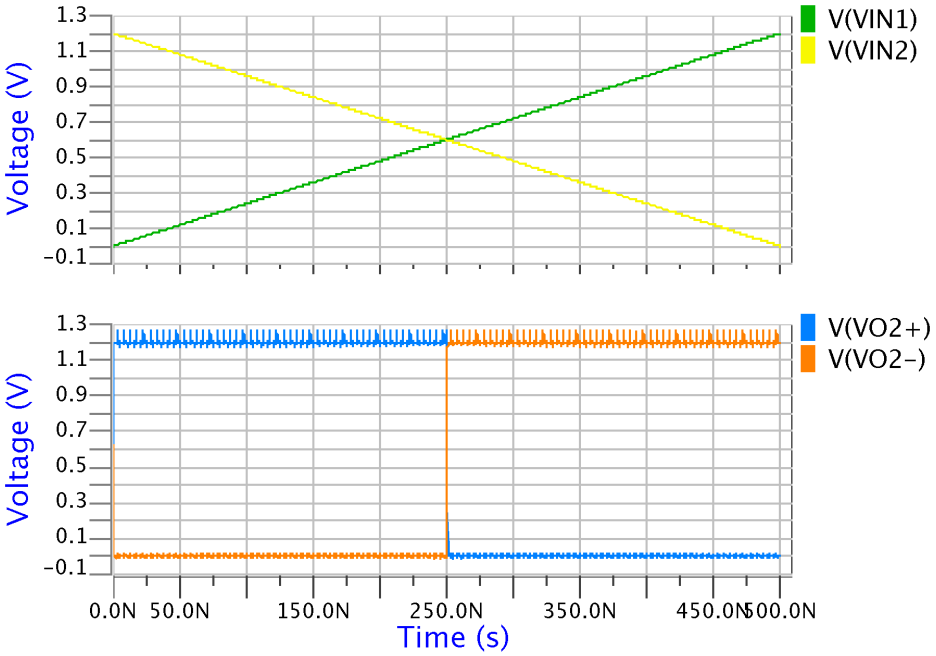

Figure 3.20. Transient simulation waveforms.

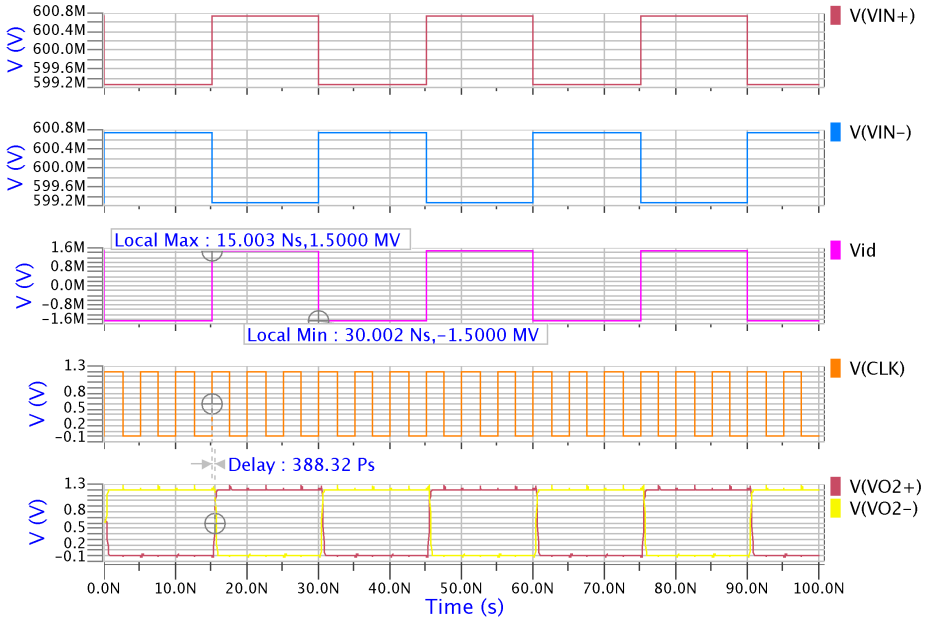

Figure 3.21. Transient simulation obtained under conditions of $V_{DD} = 1.2v$, (Max sensitivity)$V_{ind} = 1.5m$, $V_{com} = 0.6V$, $C_L = 10fF$, $f_{clk} = 200MHz$ and TT simulation corner.

3.5. Low Noise Amplifier (LNA)

LNA is the block where the signals with low amplitude captured from analog world via probes are amplified before filtration and the other blocks. In this amplification process, undesired noise signals are also amplified in addition to the desired signals. Moreover, this amplifier also adds some noise to the signal because of its structure. The block design is targeted to obtain a 40 dB gain and high bandwidth while minimizing the noise added to amplified signal.

There are some issues that should be considered in order to minimize the noise:

- Maximize the signal gain as close to the input as possible. (As a consequence, only the input stage will contribute to the noise of the op amp.)
- To minimize the 1/f noise: Use PMOS input transistors with appropriately selected dc currents and W/L ratios.

Proposed circuit

Our proposed circuit as shown in Figure 3.22 consists of PMOS and NMOS transistors. PMOS pair used as input transistors and they will be optimized for noise reduction in the following sections. This pre-amplifier is designed similar to the miller op-amp but its second stage has been removed since obtaining high gain is not the main goal of a typical pre-amplifier but bandwidth should be improved, also removing the second stage will omit the extra noise produced by output transistors.

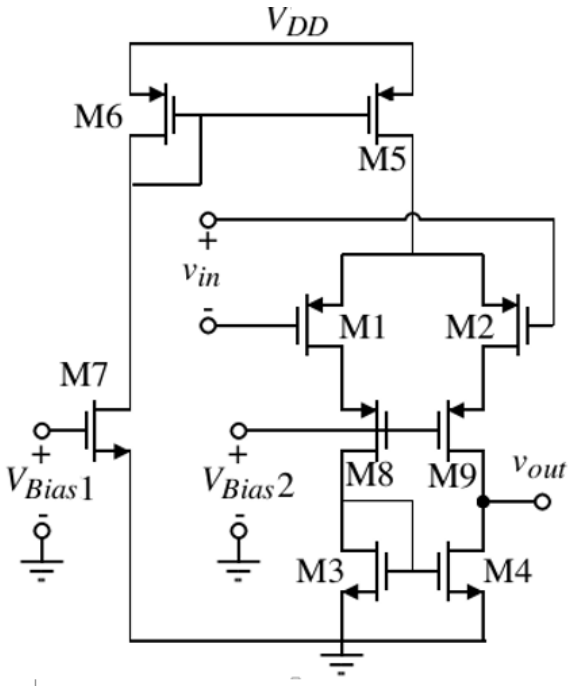

Figure 3.22. Schematic diagram for proposed LNA.

The voltage gain of a typical pre-amplifier should be around 35 – 40 dB but the significant point is to increase the bandwidth and at the same time to reduce the noise. Voltage gain of the proposed amplifier can be written as

$$A_v = G_{m1} R_o \tag{3.22}$$

Where Ro is the output resistance and it is given by

$$R_o = r_{o4} || (r_{o2} + g_{m9} r_{o9} r_{o2}) \tag{3.23}$$

By setting the overdrive voltage of input transistors to the minimum value we can increase the gm of circuit thus our voltage gain will be increased but we should choose the optimum value for the bias current to enhance bandwidth. First pole determines the bandwidth of amplifier. The circuits dominant pole is at output node because of high output resistance and capacitance values.

$$W_1 = (2(C_{gd} + C_{db)} + C_L) Ro) \tag{3.24}$$

Noise analysis

Analog signals processed by integrated circuits are corrupted by two different types of noise: Device electronic noise and "environmental" noise. We focus on device electronic noise here. Two kinds of noise can occur in electronic devices [36].

- Thermal noise

  The random motion of electrons in conductor introduces fluctuations in the voltage measured across the conductor.
- Flicker noise

  The interface between the gate oxide and the silicon substrate is a MOSFET entails a phenomenon. Since the silicon crystal reaches an end at this interface. Many lossy bonds appear, giving rise to the extra energy states. As charge carriers move at the interface, some are randomly trapped and later released by such energy states, introducing "flicker" noise in the drain current.

Input referred noise of Proposed Circuit

We can represent the effect of all noise sources in the circuit by a single source $\overline{(V_{in,n})^2}$, at the input of same circuit but the noiseless one such that the output noise equals that in the noisy circuit. We are going to extract the input referred noise of proposed amplifier. For the noise analyze, a noise generator for each transistor that contributes to the noise, is inserted. Then the output noise voltage across an open-circuit or output noise current into a short circuit is obtained and finally the reflect of the total output noise back to the input resulting in the equivalent input noise voltage, is extracted.
In the the noise modeling circuit as shown in Figure 3.23 noise generators inserted for each transistor at the gate. The total output noise voltage spectral density will be

extracted.

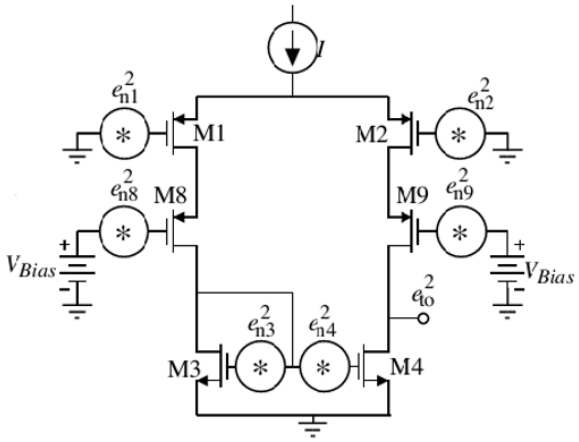

Figure 3.23. Noise modeling circuit for pre-amplifier.

The total output noise voltage spectral density $\overline{(eto)^2}$ is as follows

$$\overline{(eto)^2} = R_o^2(G_{m1}^2 e_{n1}^2 + G_{m2}^2 e_{n2}^2 + G_{m3}^2 e_{n3}^2 + G_{m4}^2 e_{n4}^2 + G_{m8}^2 e_{n8}^2 + G_{m9}^2 e_{n9}^2) \qquad (3.25)$$

Where G_{m8} and G_{m9} approximately equals $1/r_{ds1}$ and $1/r_{ds2}$. Therefor the output noise can be written as

$$\overline{(eto)^2} = R_o^2(G_{m1}^2 e_{n1}^2 + G_{m2}^2 e_{n2}^2 + G_{m3}^2 e_{n3}^2 + G_{m4}^2 e_{n4}^2 + (1/r_{ds1})^2 e_{n8}^2 + (1/r_{ds2})^2 e_{n9}^2) \quad (3.26)$$

In order to find the input-referred noise the output noise voltage should be divided by Av^2.

Finally the Input-noise voltage spectral density is given by

$$\overline{(eni)^2} = \frac{e_{to}^2}{G_{m1}^2 R_o^2} = 2e_{n1}^2[1 + (\frac{G_{m3}}{G_{m1}})^2(\frac{e_{n3}}{e_{n1}})^2 + \frac{e_{n8}^2}{G_{m1}^2 r_{ds1}^2 e_{n1}^2}] \approx 2e_{n1}^2[1 + (\frac{G_{m3}}{G_{m1}})^2(\frac{e_{n3}}{e_{n1}})^2] \qquad (3.27)$$

Noise optimization

By choosing the correct values of W and L we can reduce the total noise. Initially we

consider the 1/f flicker noise. Therefore the noise generators are replaced by,

$$\overline{(eni)^2} = \frac{B}{fW_iL_i} \tag{3.28}$$

Thus , the approximate eq. input noise voltage spectral density is

$$\overline{(eni)^2} = 2e_{n1}^2[1 + (\frac{K_NB_N}{K_PB_P})^2(\frac{L_1}{L_3})^2] \tag{3.29}$$

Therefore, by choosing the PMOS pair as input transistors and selecting the high value for W1.L1 and choosing $L_1 << L_3$ it is possible to minimize the input referred noise.

Similarly we focus on thermal noise, therefore the noise generators are replaced by

$$\overline{(eni)^2} = \frac{8KT}{3G_m} \tag{3.30}$$

Thus, the approximate eq. input noise voltage spectral density is

$$\overline{(eni)^2} = 2e_{n1}^2[1 + \sqrt{\frac{K_NW_3L_1}{K_PW_1L_3}}] \tag{3.31}$$

As we noticed in 3.29 the previous choices also satisfy this case.

The proposed pre-amplifier is designed in 90-nm technology. The design parameters are listed in Table 3.4.

The AC frequency response is depicted in Figure 3.24. We obtained 39.7 dB voltage gain with -3 dB cutt-off frequency of 10.6 MHz. The input referred noise simulation is shown in Figure 3.25.

Table 3.4. Design parameters of proposed LNA.

Technology	TSMC 90-nm
VDD	1.2v
W/L(1,2)	100u/1u
W/L(3,4)	60u/10u
W/L(8,9)	10u/0.3u
W/L 5	20u/0.3u
W/L 6	5u/0.3u
W/L 7	0.8u/0.3u
I	300uA

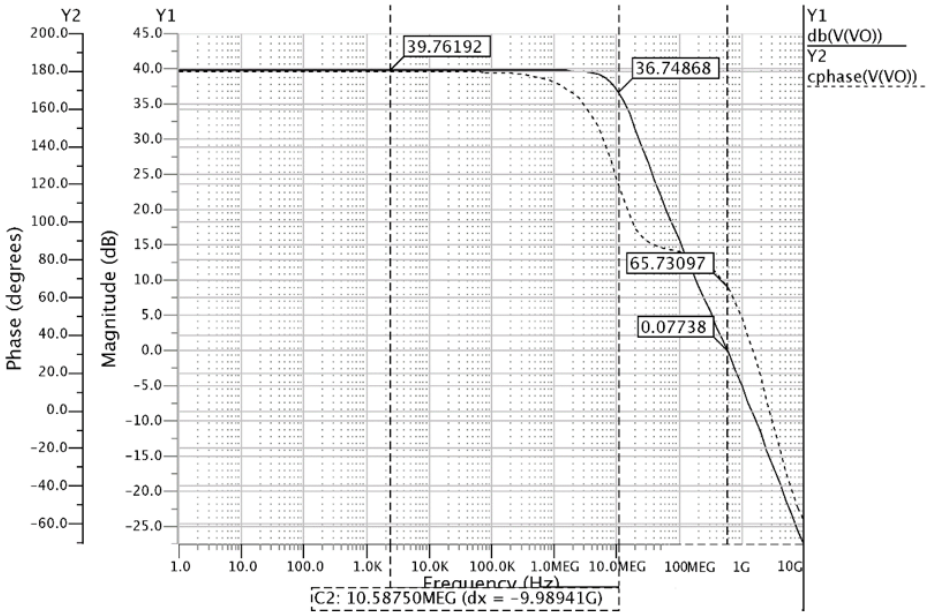

Figure 3.24. AC frequency response of LNA.

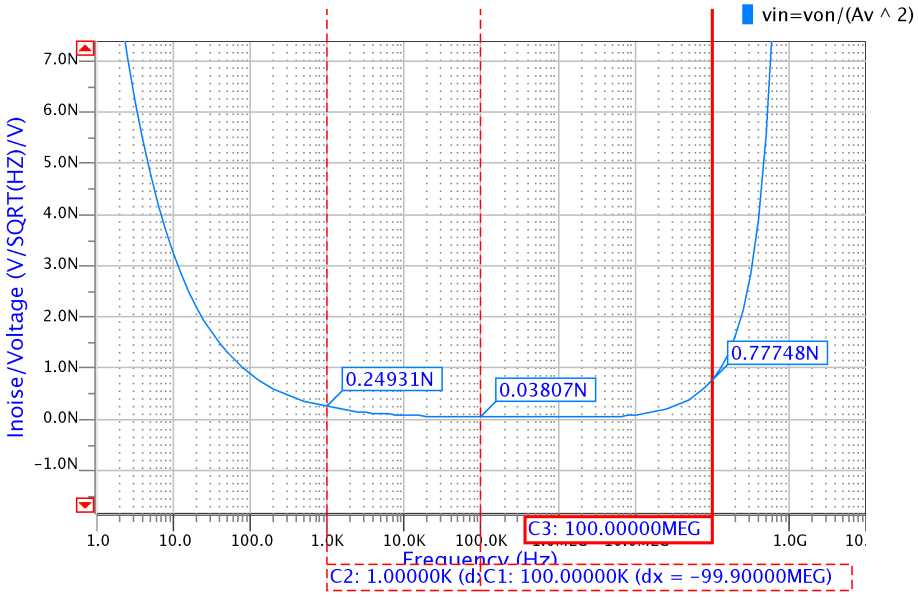

Figure 3.25. Noise simulation of proposed amplifier. The input referred noise is simulated here.

3.6. Layout techniques

In previous section a design procedure for several analog blocks, which are going to be used in CAB, is presented. The waveforms obtained from schematic circuit simulations. In this section the results of Monte Carlo simulations for some of the proposed analog circuits, based on repeated random sampling, will be presented. Also some of the major layout design techniques will be discussed. The layout of analog circuits will be depicted and obtained post-layout results will be compared with the schematic simulation results listed in previous section.

3.6.1. Transistor Orientation

Orientation is important in analog circuits for matching purposes. Hence, all the transistor must be placed in same orientation as depicted in Figure 3.26.

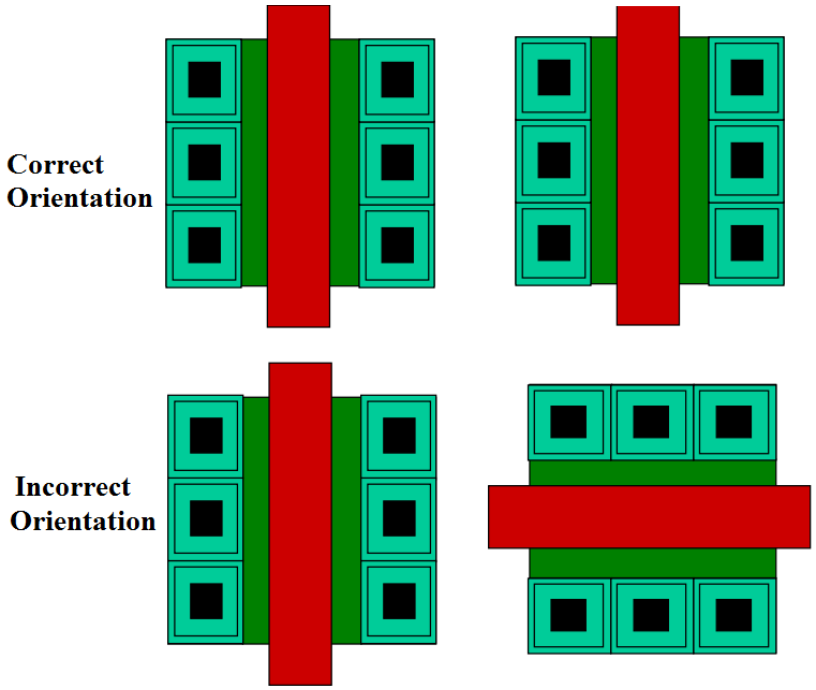

Figure 3.26. Transistor orientation.

3.6.2. Use of Multiple Fingers

Wide transistors need to be split. In this case parallel connections of n elements is required. Therefore, as depicted in Figure 3.27, contact space is shared among transistors and parasitic capacitances are reduced, especially for high speed applications.

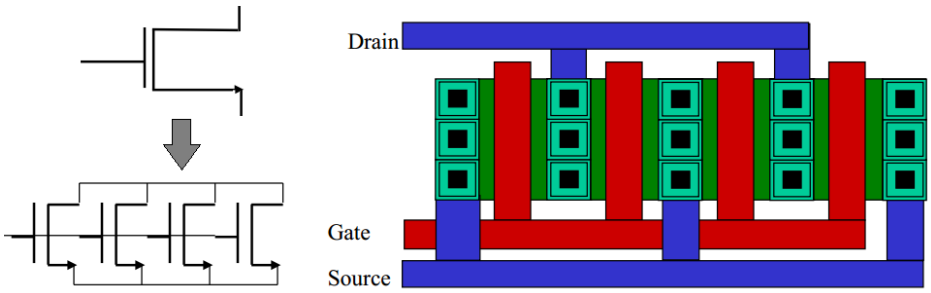

Figure 3.27. Fingered transistor.

3.6.3. Interdigitated Devices

In order to avoid mismatches between two pair transistors with one node in common transistors after fabrication, interdigitized Layout technique is implemented. This

technique Averages the process variations among transistors; so that, process variations in the x and y directions will effect subcomponents of each transistor equally. Matched transistors are split in an equal part of fingers. Figure 3.28 depicts two interdigitated transistors with 8 elements (ABBAABBA). This technique is appropriate for matching dc conditions; however, it is undesirable for ac conditions since, it causes capacitances and other parameters not be equal in two nodes.

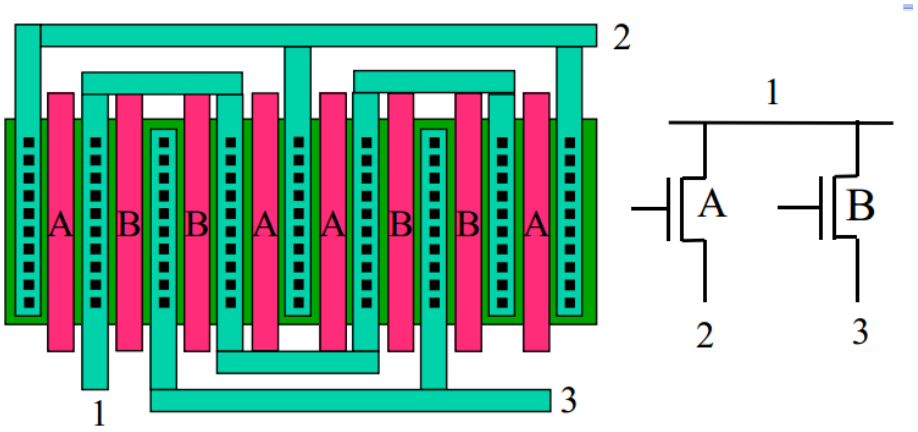

Figure 3.28. Interdigitated transistors.

3.6.4. Dummy Devices

Ending elements have different boundary conditions than the inner elements. Therefore in order to avoid mismatches dummy transistors are used at the ending parts (Figure 3.29). Dummy transistors need to be shorted, generally drain,source and gate of dummies are shorter. Disadvantage of using dummy transistors is their parasitic contribution.

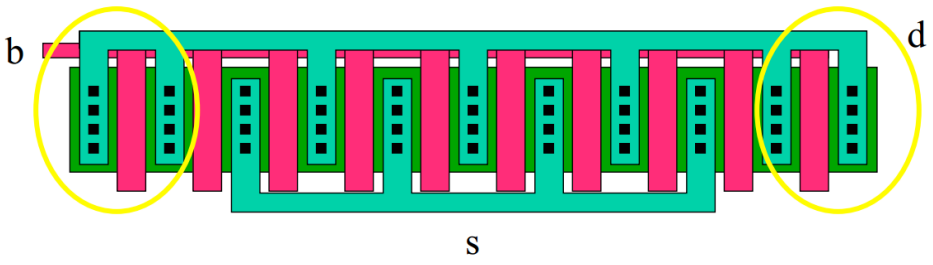

Figure 3.29. Interdigitated transistors.

3.7. Layout of Analog Blocks

The layout of proposed analog blocks are implemented using TSMC-90nm singl-poly 9 metal layer CMOS technology. In this section the Post-layout simulation waveforms which are obtained from Eldo simulation environment of MentorGraphics tool suit, will be presented.

Design issues for layout:

- Wide transistors are split.
- Transistors are positioned with same orientations.
- Matched devices are interdigitized in order to avoid mismatches.
- Dummy transistors are used at the ending parts of interdigitated devices.
- Metal 2 and 3 (and 4 in some blocks) are used for routing.
- Metal 8 and 7 are used for supply voltage and ground.
- The Bulk and supply voltage are separated by using metal 6 and 8 for each in order to prevent the supply voltage being distorted by the bulk variations.

3.7.1. Layout of Tunable Transconductance Amplifier

Figure 3.30 shows the layout of OTA t.1 (Table 3.2), which is presented in Section 3.1. The interdigitated devises are labeled as ABBAA ... and dummy cells are indicated with red squares.

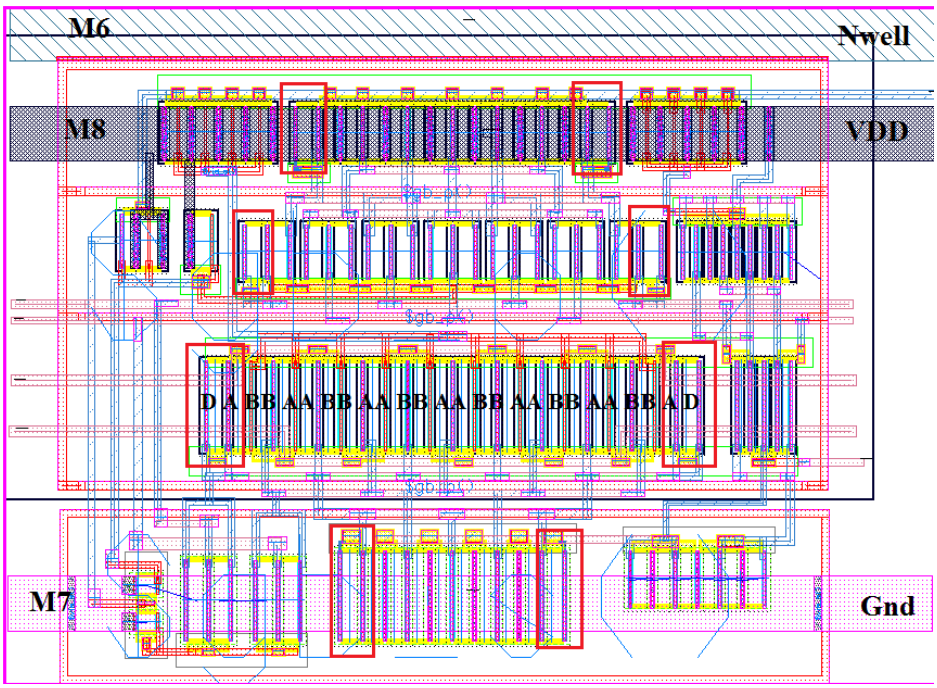

Figure 3.30. layout of OTA t.1. The total area is $\approx 35 \times 43\ (\mu m)^2$

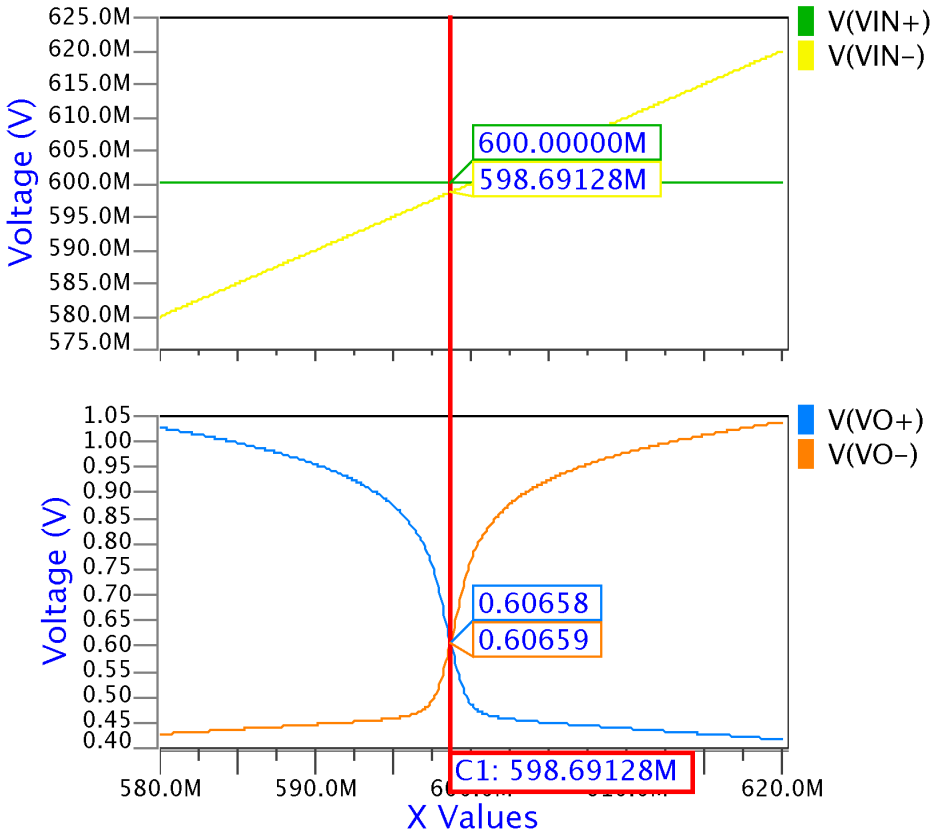

Figure 3.31. 1.3mv input-referred Off-set voltage.

Due to some mismatches after layout design, a minor input-referred DC offset is appeared in the circuit. In order to compensate this, an offset voltage is applied at the input of circuit which is shown in Figure 3.31.

Figure 3.32 depicts the comparison between frequency response obtained from schematic and post layout simulations. Wave forms are obtained from OTA t.1 while the bias current is fixed at 100 μA. It can be observed that the gain is increased slightly in post-layout results; however, bandwidth decreased due to the parasitics effect.

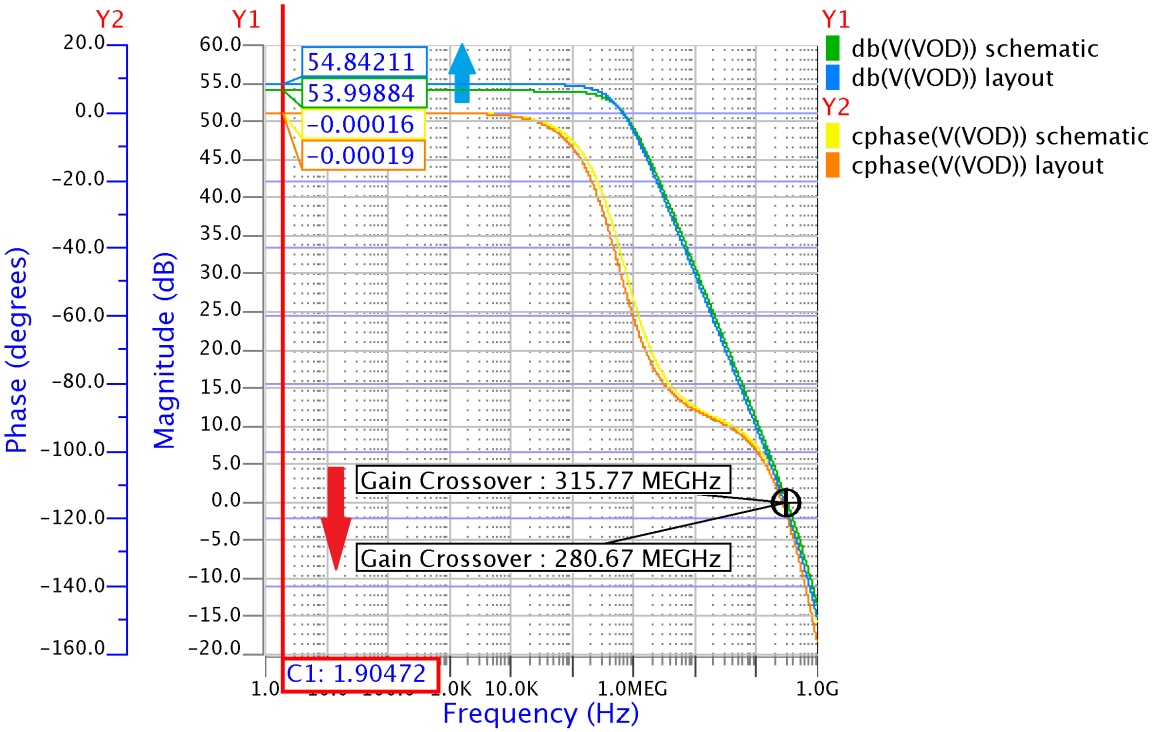

Figure 3.32. Comparison between AC frequency response of schematic and post layout for OTA t.1 at bias current of 100 μA .

Figure 3.33 depicts the comparison between obtained transconductances from schematic and post layout simulations. Wave forms are obtained from OTA t.1 while the bias current varies in range over 10-100 μA. It can be observed that the transconductances are reduced 10 μA/V in post-layout results.

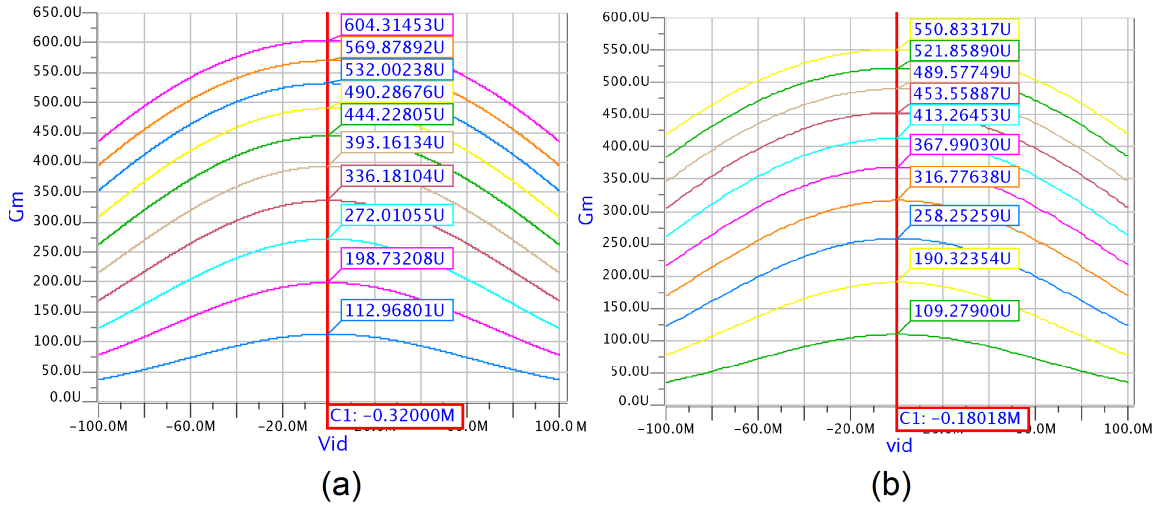

Figure 3.33. Comparison between obtained transconductances for OTA, while bias current varies over range of 10-100 μA. (a) Schematic results. (b) Post-layout results.

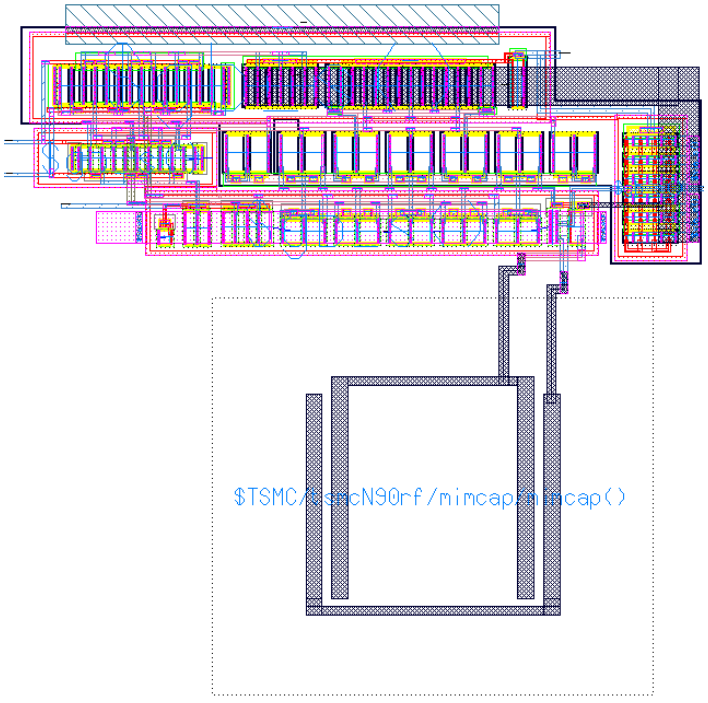

Figure 3.34. layout of OPAMP with compensation capacitor. The total area usage is $\approx 25 \times 74\ (\mu m)^2$ for OPAMP and $\approx 42 \times 48\ (\mu m)^2$ for the compensation capacitance Cc.

3.7.2. Layout of wide range OPAMP

Figure 3.34 shows the layout view of wide common-mode range OPAMP which is presented in Section 3.2. Same layout design techniques which are implemented in design of OTA, are applied here.

As discussed for OTA, an input referred DC offset of 1.4mv is accrued after layout design similarly for OPAMP, due to mismatches. Figure 3.35 depicts the comparison between frequency response obtained from schematic and post layout simulations. As expected both bandwidth and gain are reduced in post-layout simulations.

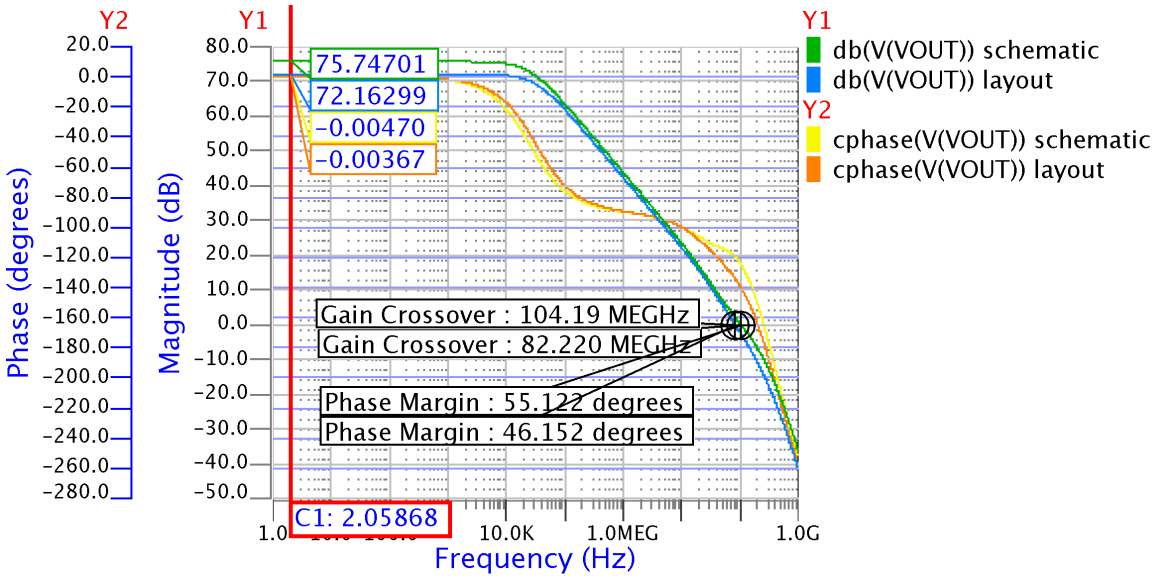

Figure 3.35. Comparison between AC frequency response of schematic and post layout simulation results for OPAMP.

3.7.3. Layout of Linear V-I converter

Figure 3.36 shows the layout view of linear V-I converter which is presented in Section 3.3. Same layout design techniques which are implemented in design of previous layouts, are applied here.

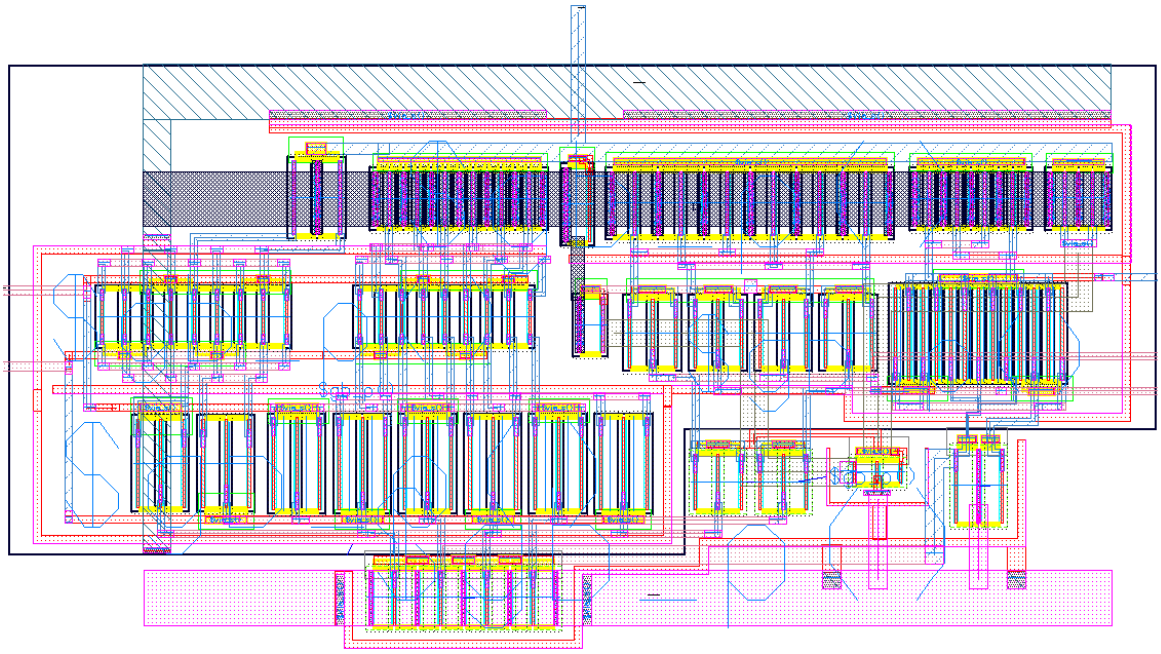

Figure 3.36. layout of V-I converter. The total area usage is $\approx 30 \times 60\ (\mu m)^2$.

Figure 3.37 depicts the comparison between obtained transconductances from schematic and post layout simulations. Wave forms are obtained from OTA t.1 while the bias current varies in range over 1-15 μA. It can be observed that the transconductance values are reduced in post-layout results.

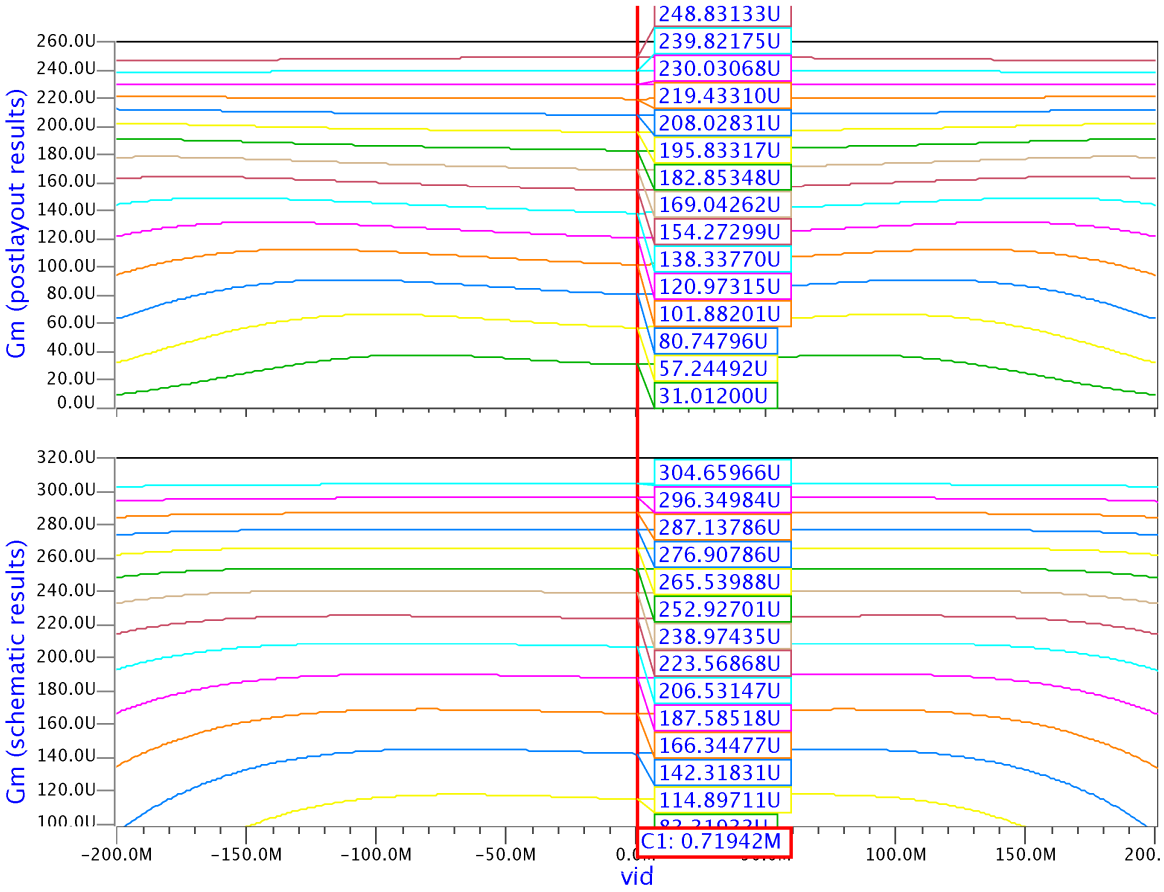

Figure 3.37. Comparison between obtained transconductance values obtained from schematic and post-layout simulations for V-I converter, while bias current varies over range of 1-15 μA.

3.7.4. Layout of Comparator

Figure 3.38 shows the layout view of dynamic comparator which is presented in Section 3.4. Same layout design techniques which are implemented in design of previous layouts, are applied here.

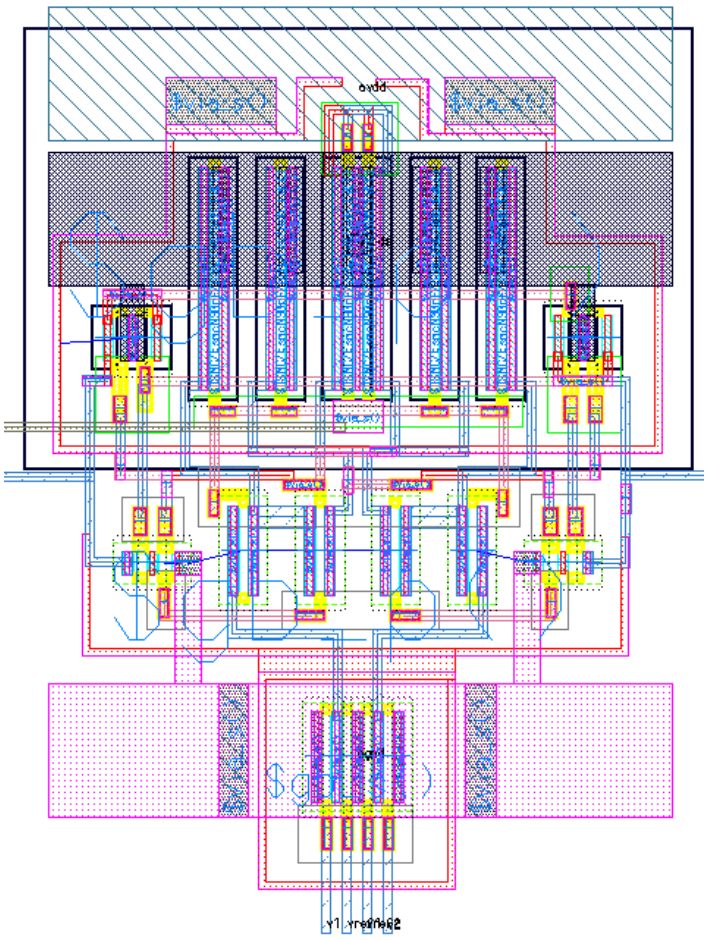

Figure 3.38. layout of dynamic comparator converter. The total area usage is $\approx 20 \times 15\ (\mu m)^2$.

Figure 3.39 depicts the comparison between transient analysis results of schematic and post layout simulations. It is observed that the maximum differential input sensitivity is increased to 2.5mv and also the output delay is increased after layout.

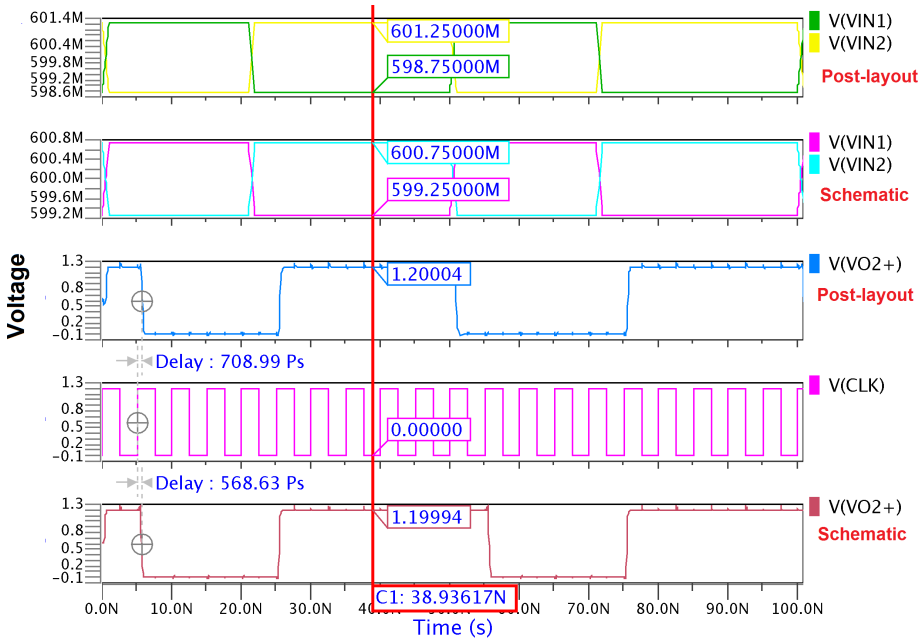

Figure 3.39. Transient analysis simulations of schematic and post-layout for comparator.

4. ANALOG APPLICATIONS

Design procedure and layouts of analog blocks, which are used in configurable analog blocks, were presented in previous section. In this section some analog applications, which can be implemented using available blocks, will be discussed.

4.1. Current to Voltage Conversion

In electronics current to voltage conversion can be implemented using an OPAMP which is called a transimpedance amplifier(TIA) [37]. The TIA can be used to amplify the current output of Geiger–Müller tubes, photo multiplier tubes, accelerometers, photo detectors and other types of sensors. Current to voltage converters are used with sensors that have a current response that is more linear than the voltage response. Figure4.1 depicts the simple I-V converter. This circuit can be implemented with analog array by connecting a resistor and OPAMP. Transmission gates are used to include the effects of switches in the circuit. Figure 4.2 shows a example of I-V conversion transient simulation results. The output voltage of circuit including transmission gates has large swing comparatively because of extra resistance values added by transistors.

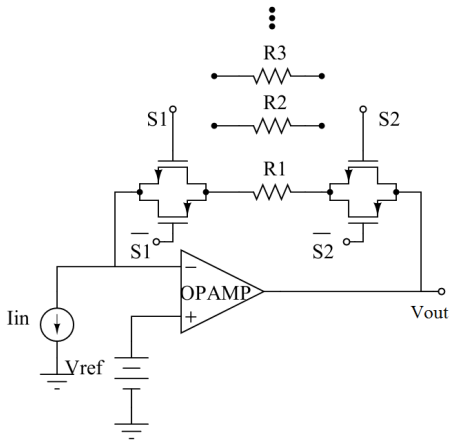

Figure 4.1. Implementation of Transmittance amplifier.

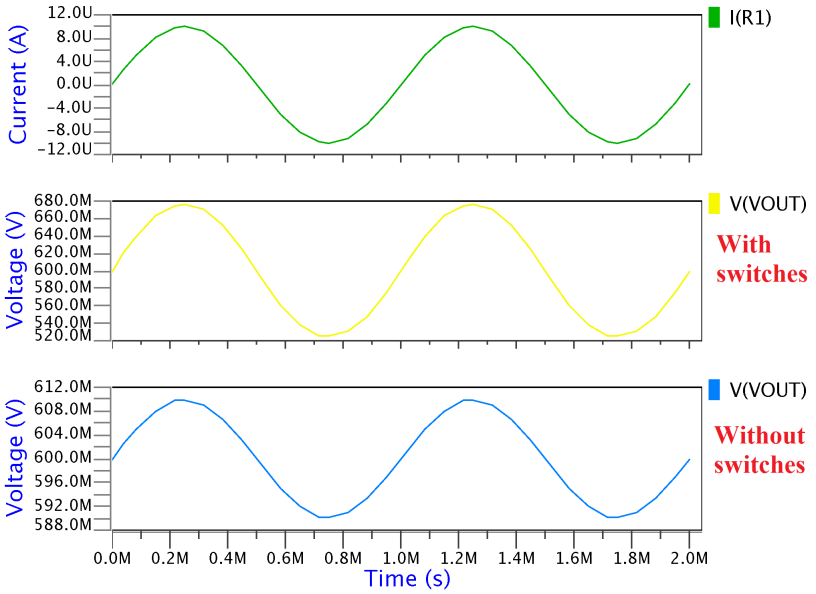

Figure 4.2. Implementation of Transmittance amplifier.

4.2. Signal Multiplication

Analog multipliers are included into many applications, such as ring modulator, Product detector, Frequency mixer, Automatic gain control, etc. Such circuits can be used to implement functions such as squares and square roots. Comparing to digital multiplication, the functions implemented by an analog multiplier may be performed worst and at higher cost. At low frequencies a digital multiplier is cheaper and more appropriate to implement.However in high frequencies, the cost of implementing digital solutions increases much more rapidly than for analog solutions. As digital technology advances, the use of analog multipliers increases.

As shown in Figure it is possible to implement a multiplier using linear V-I converter. As discussed in Section 3.3 the output current of V-I converter is the product of G_m and V_{id} terms.

$$i_o = G_m v_{id} => y = a.x \tag{4.1}$$

It is possible to use G_m as coefficient and v_{id} as input signal. Therefore, it can be used for implementation of analog signal or coefficient multiplication. Figure 4.3 depicts some transient simulation results for multiplication purpose, which are obtained from linear V-I converter circuit.

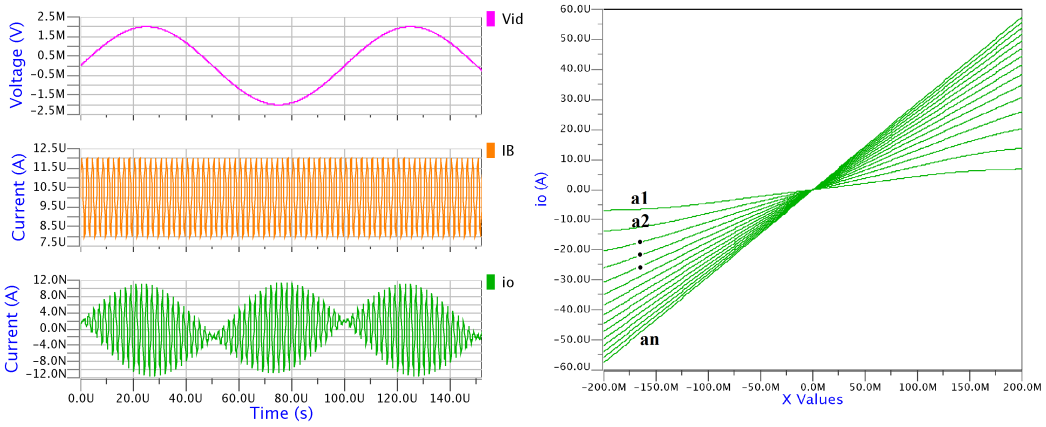

Figure 4.3. Implementation of analog multiplier and coefficient multipliers using linear V-I converter.

4.3. Low-Pass and Band-Pass Filters

One of the most important applications for analog circuits is continuous-time filtering. Even if filtering can be performed digitally like most signal processing tasks, unwanted frequencies must be filtered in the analog domain to avoid aliasing prior to converting the original analog signal to digital. Different applications require processing signals in different frequency bands varying from very low to very high frequency values. Therefore, availability of a wide range of continuous-time analog filters is crucial in many fields such as biomedical, multimedia, communication systems, etc. GmC filters are commonly used in IC implementations of analog filters because of the suitability of the building blocks of these filters (namely, OTAs and capacitors) to IC technology. Using a network of OTAs and capacitors that can be connected in various ways and tuning OTA transconductances (Gm) via bias currents allows realization of analog filters with a wide dynamic range of corner frequencies. FPAA switches can be used to connect different number of OTAs and capacitors resulting in implement-

ing many different filter types of different orders. By changing either the capacitance values at different nodes or OTA transconductances, the corner frequency and the output voltage gain can also be tuned. Lowpass and bandpass filters up to 5^{th} order are implemented to demonstrate possible circuit applications with FPAA.

4.3.1. Low-pass Filters

Figure 4.4a shows a second order biquad filter implemented by connecting four identical OTAs from neighboring CABs where corner frequencies are tuned by OTA bias currents. Proposed filter is implemented using four different OTAs that are optimized for operating in four different frequency ranges. Higher order filters such as a fifth order butterworth lowpass filter depicted in Figure 4.4b, which is realized as a first order GmC filter cascaded with two biquadratic sections, can also be implemented. Each biquad is a standard GmC configuration based on the double integrator loop. The transfer function of the lowpass biquad filter is:

$$\frac{V_o}{V_i} = H(s) = \frac{\frac{g_{m1}}{g_{m4}}\frac{g_{m3}g_{m4}}{C_1C_2}}{s^2 + \frac{g_{m2}}{C_1}s + \frac{g_{m3}g_{m4}}{C_1C_2}} \tag{4.2}$$

where $g_{m1} = g_{m3} = g_{m4} = g_m$ and $C_1 = C_2 = C$, resulting in the cut-off frequency $\omega_0 = \frac{g_m}{C}$ and quality factor $Q = \frac{g_m}{g_{m2}}$. Transfer function of the 5th order lowpass filter can be similarly written as:

$$H_{5th}(S) = [\frac{G_{m1}}{G_{m2} + Cs}] \times H_1(s) \times H_2(s) \tag{4.3}$$

Equations 4.2 and 4.3 show that the corner frequencies of filters can be tuned by adjusting OTA transconductances. Filters were programmed to corner frequencies to meet the specifications for various application domains such as biomedical applica-

tions (<50Hz) [38], wireless and computer communications (100KHz to 2MHz), wide band code division multiplexing access (WCDMA) (10MHz) [39], Hard Disk drivers (20MHz), and disk-drive read-channel systems (10-50MHz) [40].

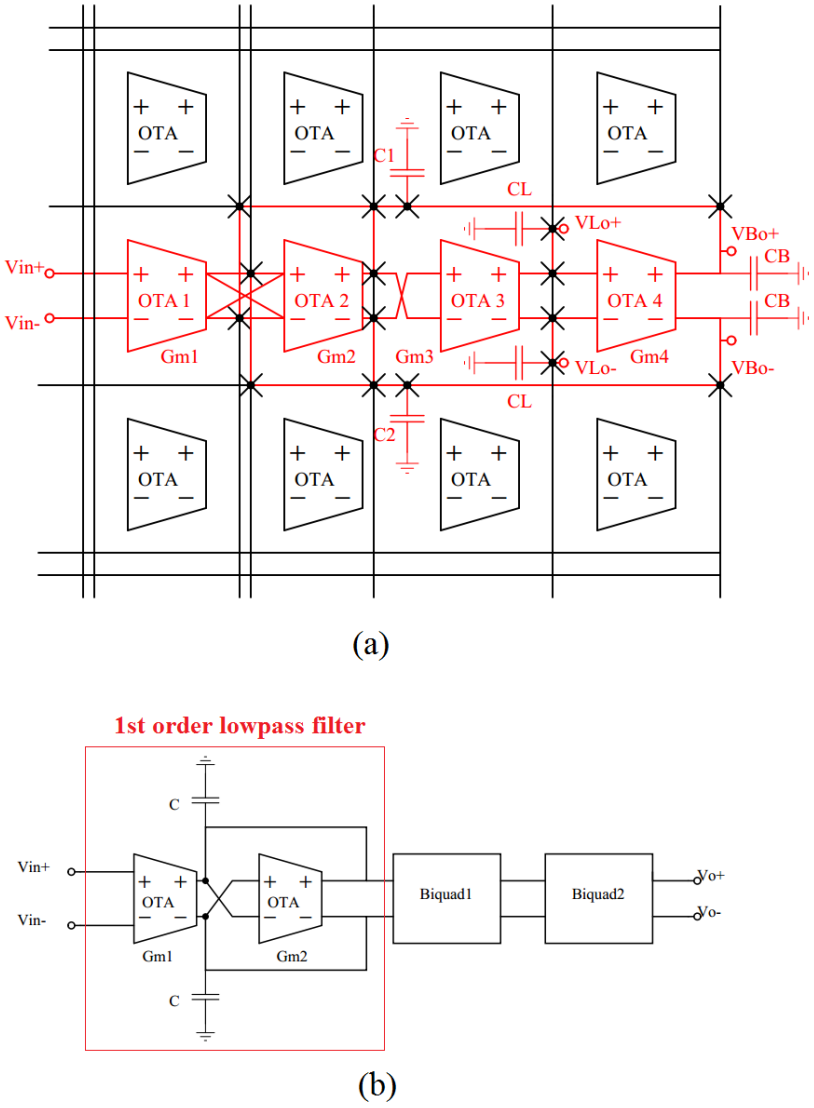

Figure 4.4. Implementation of filters using configurable analog array. (a) Second order biquad lowpass and bandpas filter. Outputs and capacitances V_{Lo}, C_L and V_{Bo}, C_B are used for lowpass filter and bandpass filters. (b) Fifth order low-pass filter is implemented by cascading one 1st order and two biquad filters.

4.3.2. Band-pass Filters

It is also possible to implement bandpass filters by reconfiguring the OTAs and capacitors in the analog array. A second order bandpass filter can be obtained by connecting four OTAs with a minor placement difference in the voltage node polarity and output voltage node compared to the lowpass filter. The transfer function of the bandpass biquad filter is:

$$\frac{V_o}{V_i} = \frac{s\ \frac{g_{m1}}{c}}{s^2 + \frac{g_{m2}}{C_1}s + \frac{g_{m3}g_m4}{C_1C_2}} \tag{4.4}$$

The corner frequency and the quality factor is tunable similar to ω_0 and Q as obtained for the second-order lowpass biquad filter, where all OTA transconductances except g_{m2} are identical.

4.3.3. Simulation Results of Filters

All filters and programmable OTAs are simulated with Eldo using TSMC-90nm CMOS models. Figure 4.5 and Figure 4.6 depict the frequency responses for fifth-order lowpass and second order bandpass filters with various corner frequencies. To span a wide range of filter frequencies, five different OTAs optimized for operating with a different range of bias currents were designed and included in the FPAA. By sweeping the bias currents from 20 nA to 100 uA, and using node capacitance values in the range of 100 fF to 1 pF, filter corner frequencies from 10 Hz to 150 MHz were obtained. Table 4.1 lists obtained frequency corners for low-pass filter using different types of OTAs and biasing them with variable tail current.

Table 4.1. Obtained frequency ranges using different types of OTAs.

Type of OTAs used in Low-pass filter	Bias current	Corner Frequency
t.1	10-120 uA	25-170 MHz
t.2	1 u-12 uA	2-25 MHz
t.3	100 nA-1 uA	200 KHz - 2 MHz
t.4	20 nA - 100 nA	16 KHz - 150 KHz
t.5	1-20 nA	10 - 500 Hz

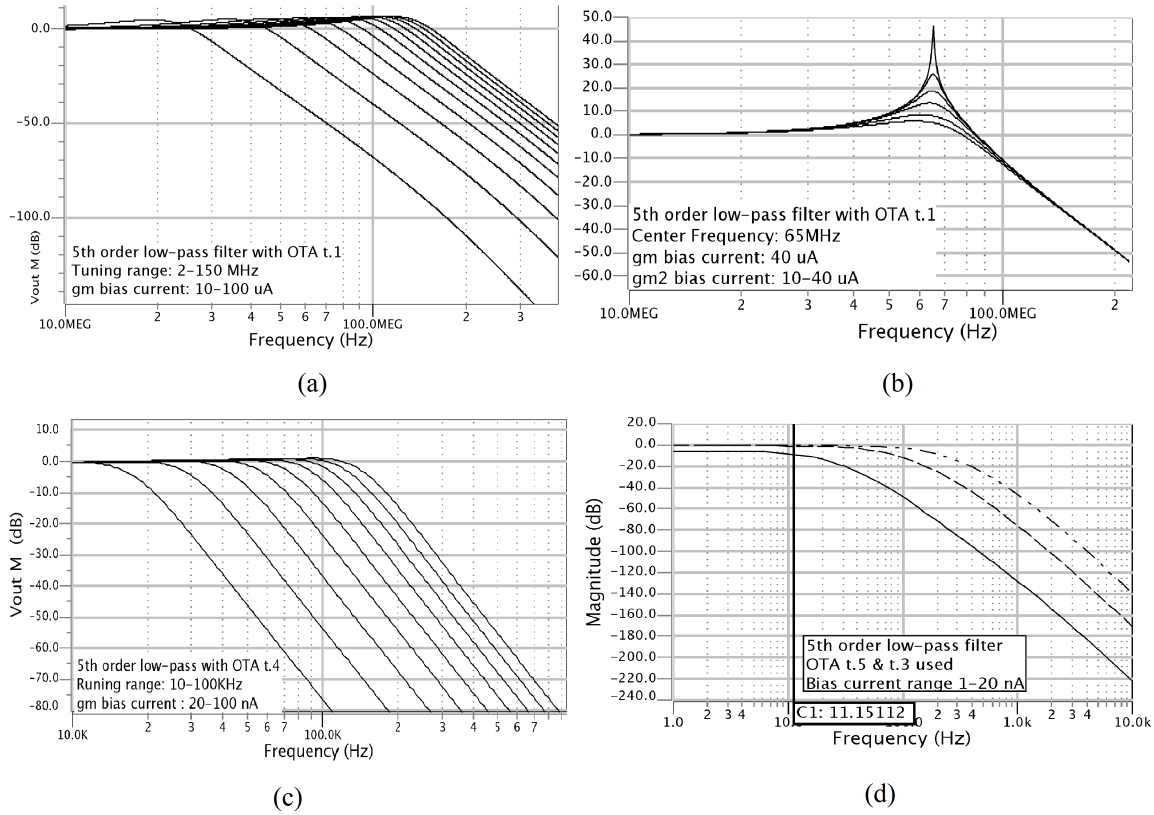

Figure 4.5. Frequency response simulation of fifth order low-pass filter. (a) A fifth order low-pass filter which is built connecting ten identical t.1 OTAs. (b) Tuning the quality factor. (c) A similar low-pass filter in low frequency ranges from 10 to 100KHz implemented by using ten identical OTA t.4. (d) cut-off frequencies below 100Hz.

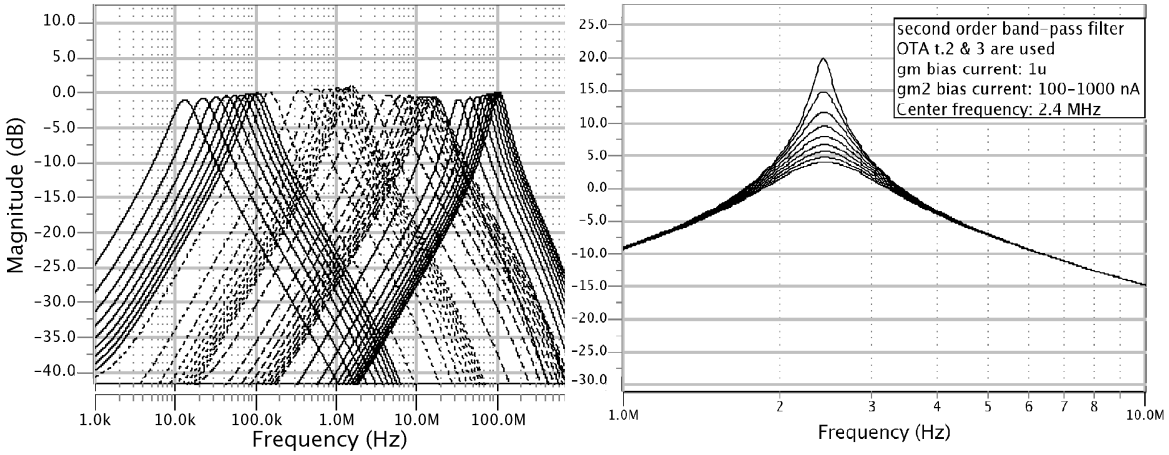

Figure 4.6. Frequency response simulation of second order band-pass filter implementation on FPMA in different frequency ranges and quality factors. Wide range frequency tuning from 10KHz to 100MHz using OTA type.1,2,3 and 4. and tuning Q of filter in a fixed frequency of 2.4 MHz.

In order to include the effects of switches on filter performance, the 5th order filter is implemented with switched OTAs as depicted in Figure 4.7. Two transmission gates are place at input terminals and two gates are placed at the output terminals of OTAs. As an example, OTA t.2 is replaced with switched topology and 10 switched OTA are connected to form a 5th order low-pass filter. Figure 4.8 gives the comparison between two AC frequency responses for ideal filter and for the filter consist of switched OTAs. It is observed that the maximum 3-dB cut-off frequency is reduced by 2MHz because of parasitics which are added by extra switches.

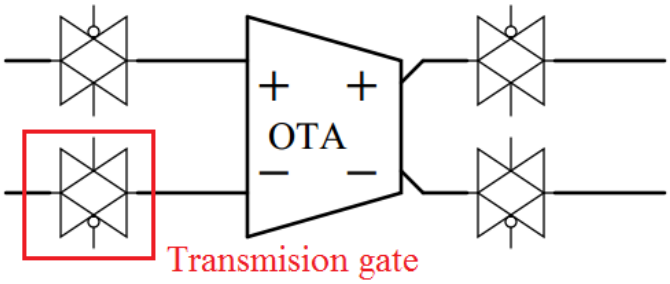

Figure 4.7. Switched OTAs. Transmission gates used for switching OTAs.

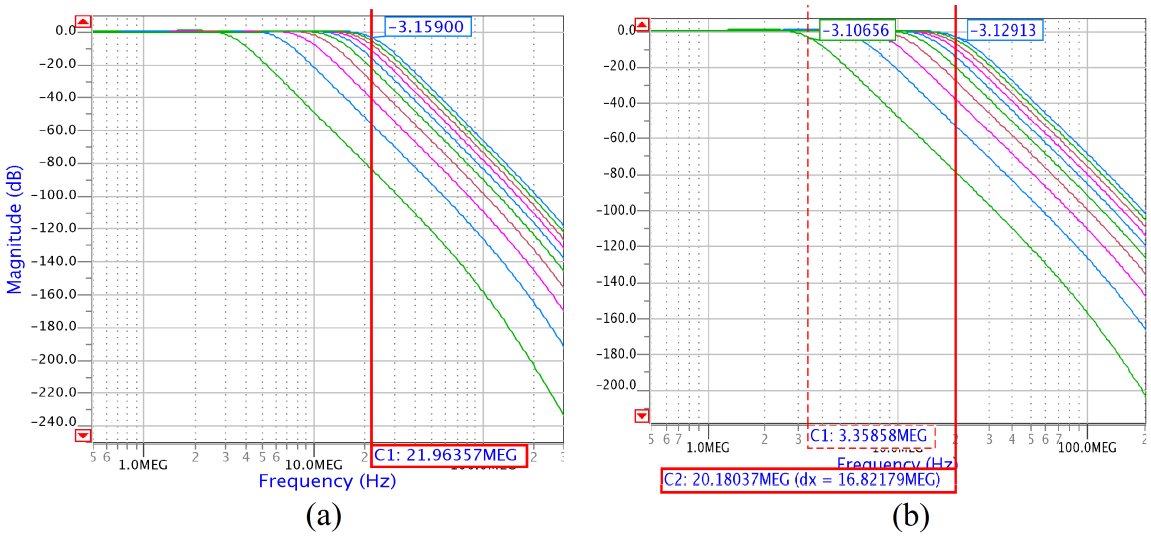

Figure 4.8. comparison between two AC frequency responses with different bias currents. (a) AC frequency response of ideal filter. (b) AC frequecy response of ideal filter consist of switched OTAs.

Different applications require processing signals in low to high frequency values with demand for reaching better linearities. Specially multimedia, ADLS cable-modem applications [41], Wireless applications, Wimax receivers (10MHz) and disk-drive read-channel systems (10-50MHz) [40] are those which requires higher linearities. Figure 4.10 depicts the layout of low-pass filter which consists of linear OTAs, mim-cap capacitors and DACs for tuning bias currents. For maximum corner frequency the bias current of OTAs is tuned up to 15 μ A. Figure 4.11 depicts the post-layout frequency response simulations of proposed filter. The corner frequency changes over 6MHz to 40MHz with varying bias current. The corner frequency change versus bias current tuning is shown in figure 4.12 shows the IM3 simulation result which are extracted from MATLAB tool. Two sinusoidal tones separated by 200 KHz around 40 MHz with total amplitude of 200 mv p-p are applied in the input and the IM3 of filter is -59 dB at 40MEG MHz for the filter at 400 mv p-p. The HD3 of filter at 40MHz is -70dB and -60dB for 200mv and 400mv p-p input voltage respectively (Figure 4.13). The HD3 of filter for 200mv p-p at 6MHz is -55dB.

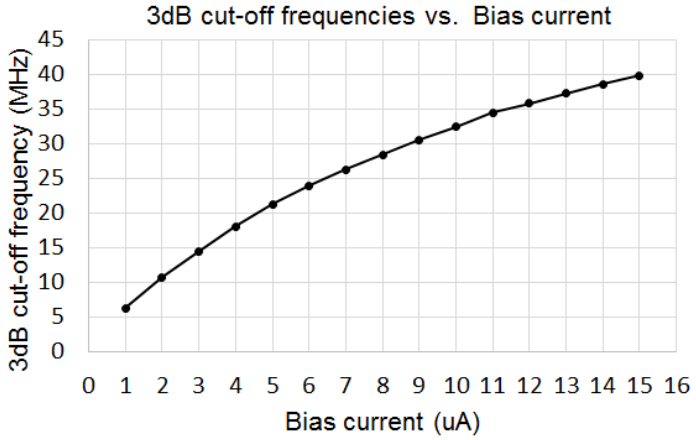

Figure 4.9. Corner frequency tuning with bias current.

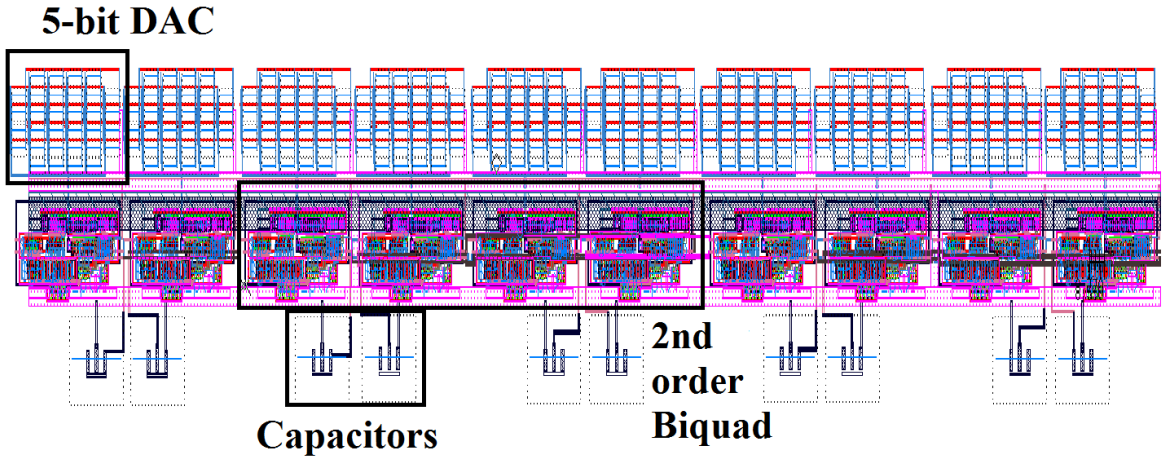

Figure 4.10. Layout of full 5 order low-pass filter with bias DACs.

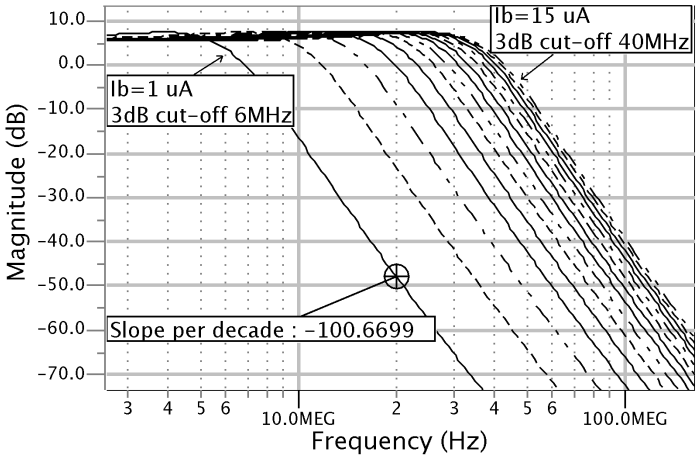

Figure 4.11. AC frequency response of proposed filter in different tail currents. The 3dB cut-off frequency can be tuned using bias current over range of 6-40MHz.

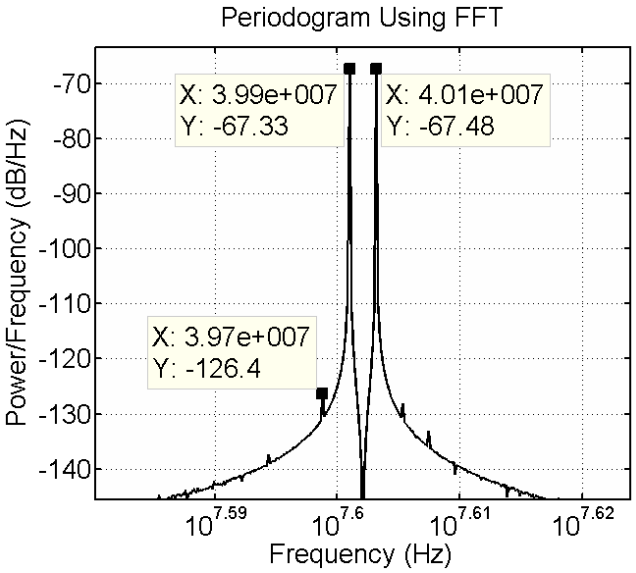

Figure 4.12. Power spectrum simulation of output voltage, where two tones with total amplitude of 400mv p-p is applied in the input.

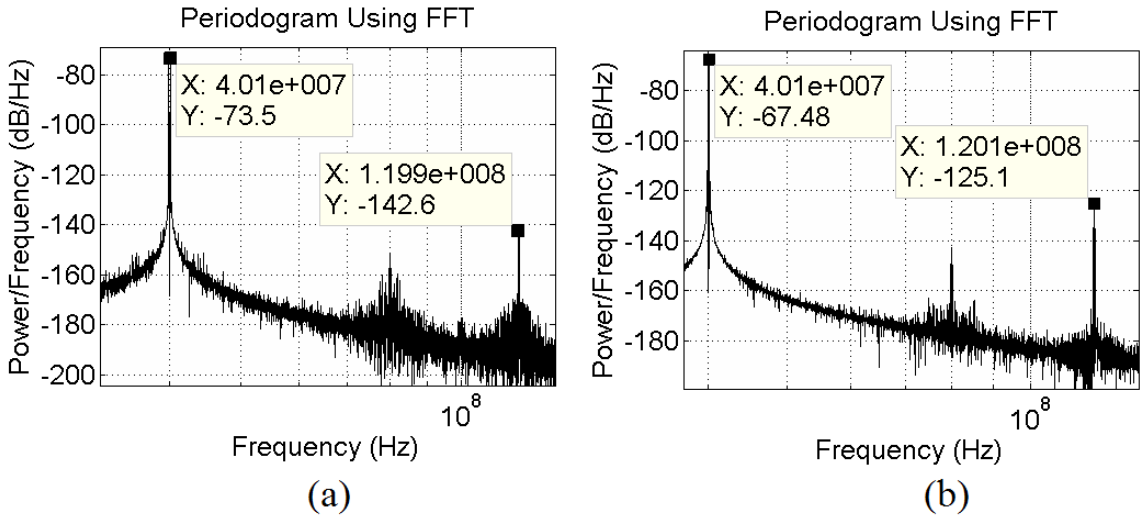

Figure 4.13. Power spectrum simulation of output voltage. (a) The HD3 of output voltage at 40MHz is -70dB for 200mv p-p. (b) The HD3 of output voltage at 40MHz is -60dB for 400mv p-p input voltage.

5. CONCLUSION AND FUTURE WORK

In this thesis, an introduction over the evolution of field programmable digital and analog arrays is presented. Design issues for various types FPGAs and FPAAs are introduced. Some design issues are presented for FPMAs and most of all focused on analog part of FPMA. Some challenges of analog design is sub micron technology are explained.

The analog core of FPMA is array of configurable and fix analog blocks which is used for prototyping analog circuits. Some FPMA design examples are introduced in literature. The architecture of arrays, interconnect network and design of analog blocks are introduced. The proposed analog circuits, which are suited for 90nm technology, are five tunable OTAs and linear V-I converter, Wide common-mode range OPAMP, comparator and low noise pre-amplifier.

This thesis focuses on design of tunable and fix analog circuits, which are targeted to be used in configurable analog blocks. A cascode differential tunable OTA is designed and simulated. In order to achieve wide range of transconductances from 40n to 600μ A/V, four extra OTAs with same topology but different sizes are designed. Low noise amplifier for pre-amplification purpose is designed and simulated. A linear OTA is designed for obtaining constant transconductance and simulated for V-I conversion purpose. A dynamic comparator is designed with high sensitivity and high speed performance. A wide-range input common-mode voltage opamp with a voltage gain of 74dB and 100MHz bandwidth is designed and simulated. Some layout techniques for analog circuits are introduced. The layout of most of the proposed blocks are implemented with TSMC-90nm nine-metal single-poly technology and post-layout simulations are compared with schematic results.

Fully differential integrated low-pass and band-pass filters with tunable quality factor and corner frequencies have been implemented using the proposed OTAs and capacitors. The corner frequency of the filters can be tuned in the range of 10Hz to 150 MHz by applying bias currents to each OTA. Using the same components, a band-pass filter was also simulated to operate with center frequencies from 10 kHz to 100 MHz. The entire system works with 1.2V supply voltage.

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