DESIGN OF A GAN-BASED HIGH GAIN X-BAND POWER AMPLIFIER

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By
Utku Ağtaş
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Design of a GaN-based High Gain X-Band Power Amplifier
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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

DESIGN OF A GAN-BASED HIGH GAIN X-BAND POWER AMPLIFIER

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M.S. in Electrical and Electronics Engineering
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May 2024

RF power amplifiers remain a vital element of space, airborne, and radar applications. Modern systems require high power and gain while maintaining high efficiency. However, obtaining these features with a compact design brings challenges. Monolithic Microwave Integrated Circuits (MMIC) provide flexibility and enhanced performance while operating at higher frequencies. Among other transistor technologies, GaN on SiC based high electron mobility transistors (HEMTs) provide extraordinary performance with high power density, thermal conductivity, and high band gap.

In this thesis, we present a three-stage X-Band MMIC power amplifier (PA) based on NANOTAM 250 nm GaN-on-SiC process technology. The characterization steps of the transistors are discussed to extract process parameters for the design. The amplifier is designed on the Keysight ADS environment. The design is realized on a 3-inch GaN-on-SiC wafer. In the 8.5–10.5 GHz frequency band, measurements show that the PA achieves a 40 dB small signal gain, PAE higher than 40%, and average 20 W output power under 28 V, 100 mA/mm pulsed biasing conditions at room temperature. The MMIC occupies 10.26 mm^2 area and has 1.96 W/mm^2 power density.

Keywords: Gallium Nitride, MMIC, high gain power amplifier, X-Band.

ÖZET

GAN TABANLI YÜKSEK KAZANÇLI GÜÇ YÜKSELTEÇ TASARIMI

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Mayıs 2024

RF güç yükselteçleri uzay, hava ve radar uygulamalarının hayati bir unsuru olmaya devam etmektedir. Modern sistemler, yüksek verimliliği korurken yüksek güç ve kazanç gerektirmektedir. Ancak bu özellikleri kompakt bir tasarımla elde etmek zorlukları da beraberinde getirmektedir. Monolitik Mikrodalga Entegre Devreler (MMIC), yüksek frekanslarda çalışırken tasarımda esneklik ve gelişmiş performans sağlamaktadır. Diğer transistör teknolojileri arasında, SiC üzerinde Galyum Nitrür (GaN) tabanlı yüksek elektron hareketli transistörler (HEMT'ler), yüksek güç yoğunluğu, termal iletkenlik ve yüksek bant aralığı ile olağanüstü performans sağlamaktadır.

Bu tezde, NANOTAM 250 nm SiC üzeri GaN teknolojisine dayanan üç katlı bir X-Bant MMIC güç yükselteci sunuyoruz. Tasarım için işlem parametrelerinin çıkarılması amacıyla transistörlerin karakterizasyon adımları tartışılmıştır. Güç yükselteci Keysight ADS ortamında tasarlanmıştır. Tasarım, 3 inçlik SiC üzeri GaN levha üzerinde üretilmiştir. 28 V, 100 mA/mm darbeli sinyal altında ve oda sıcaklığında 8.5-10.5 GHz frekans bandında alınan ölçümlerde, yükseltecin 40 dB küçük işaret kazancına, %40'tan yüksek PAE'ye ve ortalama 20 W çıkış gücüne ulaştığı gözlemlenmiştir. MMIC 10,26 mm^2 alan kaplamaktadır ve 1,96 W/mm^2 güç yoğunluğuna sahiptir.

Anahtar sözcükler: Galyum Nitrür, MMIC, yüksek kazançlı güç yükselteçi, X-Bant.

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

Power amplifiers are a critical part of the communication systems. Over the years, different technologies have been introduced to meet the demand [2]. Microwave monolithic integrated circuit (MMIC) technology introduced flexibility to designers and enhanced performance and reliability. Increased gain, power, and efficiency of power amplifiers have always been the main objectives of power amplifiers. Although different design techniques have been used to reach these objectives, the material defines the overall limit. Among others, Gallium Nitride (GaN) offers high power density for high-frequency applications [3]. In modern systems, different frequency bands are in use for allocated technologies. Although the main focus of the MMIC design shifted to higher frequencies [4], X-Band still preserves its importance in space, airborne, and radar applications.

Recent works in the X-Band mainly focus on 2-stage topologies; thus, the gain does not exceed 30 dB while having output power greater than 40 dBm [5, 6, 7, 8, 9]. 3-stage topologies provide a gain of more than 30 dB, but there is no design with a gain of 40 dB while achieving efficiency greater than 40% [10].

1.2 MMIC Technology

While the first monolithic IC was introduced by Robert Noyce in 1959, the first microwave monolithic IC was reported in 1976 by Ray Pengelly and James Turner about X-Band power amplifiers using Gallium Arsenide (GaAs). [11, 12]. The paper was also the first MMIC working in the X-Band [12]. After the development of GaN HEMTs, the GaN-based MMICs emerged in literature for RF applications in the 2000s [13].

The most notable advantage of MMICs is the fabricating of a large number of chips with lower cost and high yield compared to hybrid circuits [14]. Hybrid circuits are composed of discrete components, and the interconnections are done with wire bonds. On the other hand, all passive and active components of MMICs are fabricated together on wafers, and thousands of circuits can be manufactured simultaneously at a lower cost [14]. The integrated topology also eliminates the parasitics coming from interconnections in hybrid circuits [14]. Reduced parasitics enable reproducibility and high yield.

1.3 GaN HEMT Technology

GaN HEMTs become very popular in the last decade due to their unique performance in high-power applications. GaN HEMTs are developed following the footsteps of GaAs HEMTs [15]. The first HEMT structure was reported by T. Mimura in 1980 using GaAs-AlGaAs heterostructure [16, 17]. The structure enables elevated electron mobility and increased speed at electron transportation using the 2D electron gas (2DEG) near the GaAs-AlGaAs interface. In 1991, the first GaN-AlGaN heterojunction was demonstrated by M. A. Khan et al., which achieved extraordinary electron mobility [18, 19]. Using this structure, the first GaN HEMT was reported in 1993 again by M. A. Khan et al. [20]. Finally, Eudyna of Japan produced GaN HEMT for RF applications, which was suitable for mass production [19, 21].

GaN-based transistors can offer a high power density due to their several physical properties given in Table 1.1. Gallium Nitride has a 3.4 eV high bandgap, which results in high breakdown voltages [3]. The critical breakdown field rises to 3.3 MV/cm, while GaAs and Silicon (Si) have 0.4 and 0.3 MV/cm, respectively. Hence, GaN transistors can be biased with high voltage levels. Large drain voltage leads to higher output impedance per watt during RF operation, resulting in easier and low-loss matching networks and eventually higher efficiencies [22].

The high electron mobility and high saturated current velocity at the GaN-AlGaN structure enable high current density. Hence, these transistors can achieve high RF current and voltage swing and offer high power densities [22].

High power densities over a wide frequency range come with excessive power dissipation in a small area. GaN has a thermal conductivity of around 1.5 W/cm·K. However, high-power operations demand better thermal performances. Here, Silicon Carbide (SiC) offers high thermal conductivity with 4.5 W/cm·K. Hence, when GaN HEMTs are combined with SiC substrate, they can prevent excessive channel temperatures and achieve outstanding thermal properties [22].

Table 1.1: Properties of Semiconductor Materials at Room Temperature [1].

Property	**Si**	**InP**	**GaAs**	**SiC**	**GaN**
Bandgap (eV)	1.1	1.35	1.42	3.25	3.4
Electron Mobility (cm^2/V·s)	1500	5400	8500	650	2000
Critical Breakdown Field (MV/cm)	0.3	0.5	0.4	3	3.3
Saturated Electron Velocity (x10^7 cm/s)	1	1	1.3	2	2.5
Thermal Conductivity (W/cm·K)	1.5	0.7	0.5	4.5	>1.5

1.4 Thesis Outline

This thesis discusses a 3-stage X-Band GaN on SiC MMIC power amplifier implemented in a 250 nm GaN-on-SiC process. In Chapter 2, the transistor characterization is explained, with the measurement setups. The parameters used in the design are obtained.

In Chapter 3, the MMIC design steps are discussed. The topology and transistors are selected using the results in Chapter 2. Then, the stability of each HEMT is discussed, and the stability networks are designed. Finally, the matching networks are designed, and the final design is illustrated.

Chapter 4 presents the simulation and measurement results. Small and large signal results are discussed. The results are compared with the recent works in the literature.

Finally, Chapter 5 concludes the thesis and examines what can be done in the future.

Chapter 2

Transistor Characterization

The first step of the design is characterizing the transistors of NANOTAM 250 nm GaN on the SiC Process. In this chapter, we have discussed the parameters that define the transistor performance with the characterization steps and measurement procedure to extract them. The transistor in Figure 2.1 has a size of 8×125 μm. Since its periphery is 1 mm, all the results have already been normalized for per mm.

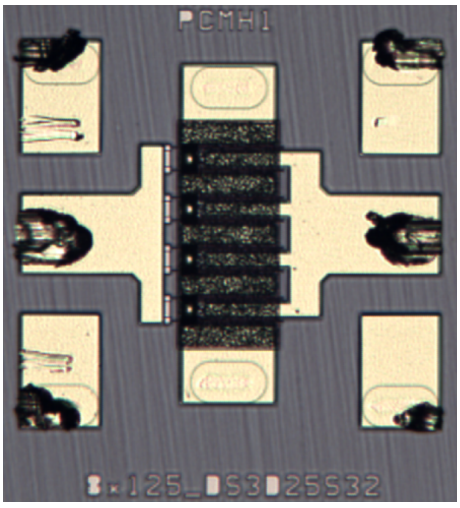


Figure 2.1: Microscopic photograph of 8 x 125 um HEMT.

2.1 DC Measurements

The setup in Figure 2.2 extracts the DC characteristics of the transistors. The main device in the setup is the Keysight B1505A Power Device Analyzer. We have used SMU 1 and SMU 3 ports for measurements, which are for high voltage and high current measurements, respectively. The high voltage port is connected to the gate since there is no high current flow instead of leakage. The high current port is connected to a Kelvin connector, which is necessary to reduce the residual resistance effects of cables. Then, Kelvin connector's force is connected to the drain, and the sense port is to the ground. Figure 2.3 describes the connections.

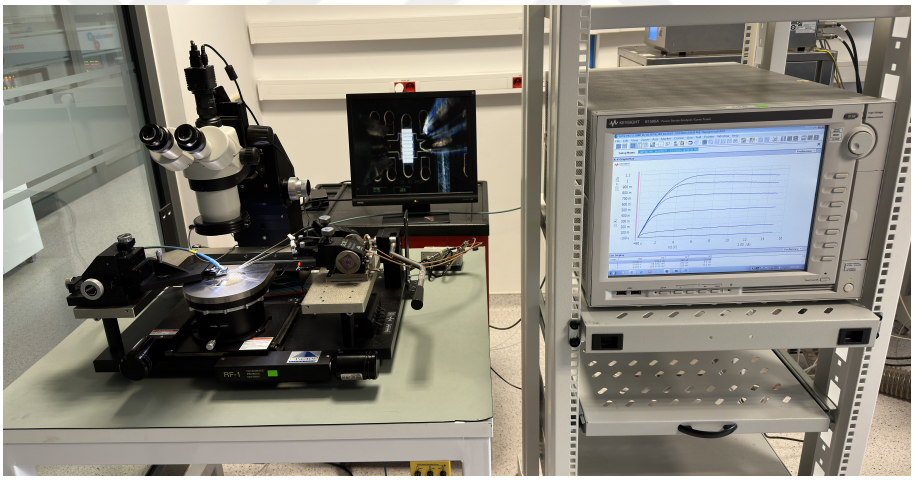


Figure 2.2: Photograph of DC Measurement Setup.

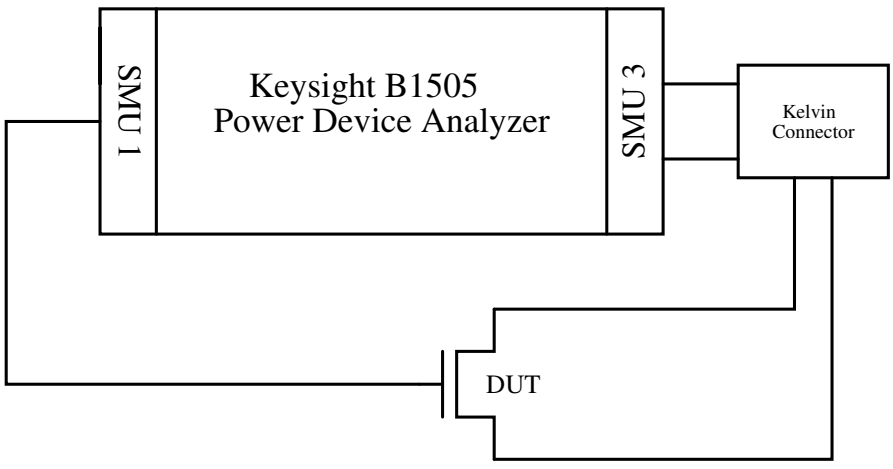


Figure 2.3: Schematic of DC Measurement Setup.

We start with I_d vs. V_d measurement for measuring R_{on}, V_{knee}, and current density. R_{on} is the resistance between the drain and the source of the transistor when it is turned on. We define the on-resistance as $\frac{V_d}{I_d}$ measured at V_d = 100 mV and V_g = 1 V. Knee voltage is the drain voltage when the current level is 95% less than the maximum current at V_g = 1 V. The current density is the $\frac{I_{d,max}}{HEMT\ Size}$ value. For extracting these parameters, we swept drain voltage from 0 to 15 V for six gate voltages and measured the drain currents. Figure 2.4 shows the results.

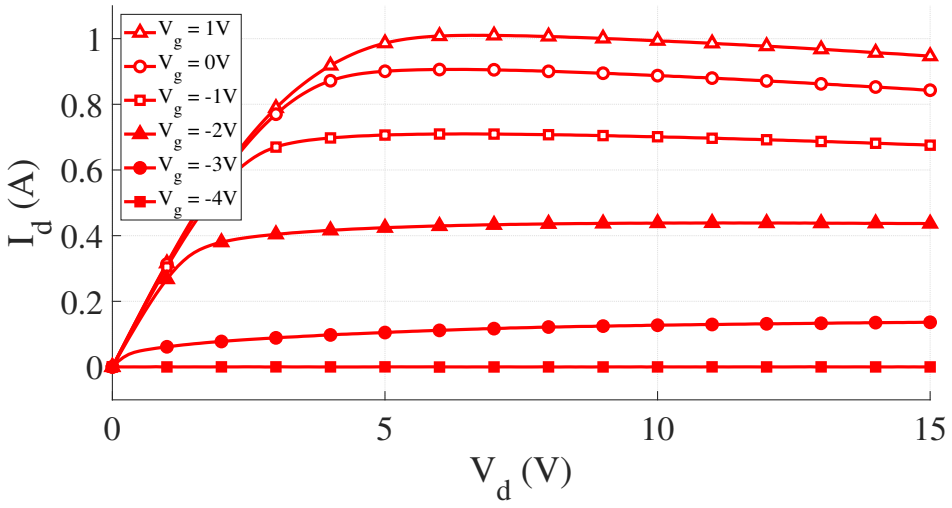


Figure 2.4: I_d vs. V_d measurement results of 8×125 μm HEMT.

From Figure 2.4, the maximum current is 1.01 A at V_d = 6 V. At V_d = 4.6 V, I_d equals 0.95; hence, the knee voltage is 4.6 V. The on-resistance is 3.1 Ω.

To extract the threshold voltage and the transconductance, I_d vs. V_g measurements are performed. The threshold voltage is the V_g value when the drain current starts to increase rapidly. Transconductance is the ratio of change in drain current to gate voltage and calculated by $g_m = \frac{\partial I_d}{\partial V_{gs}}$ [23]. The measurement sweeps the gate voltage, and measures changes in the drain current level for 6 different drain voltages. The average maximum points give $g_{m,max}$. From Figure 2.5, the maximum transconductance is 315 mS, and the threshold voltage is −3.3 V.

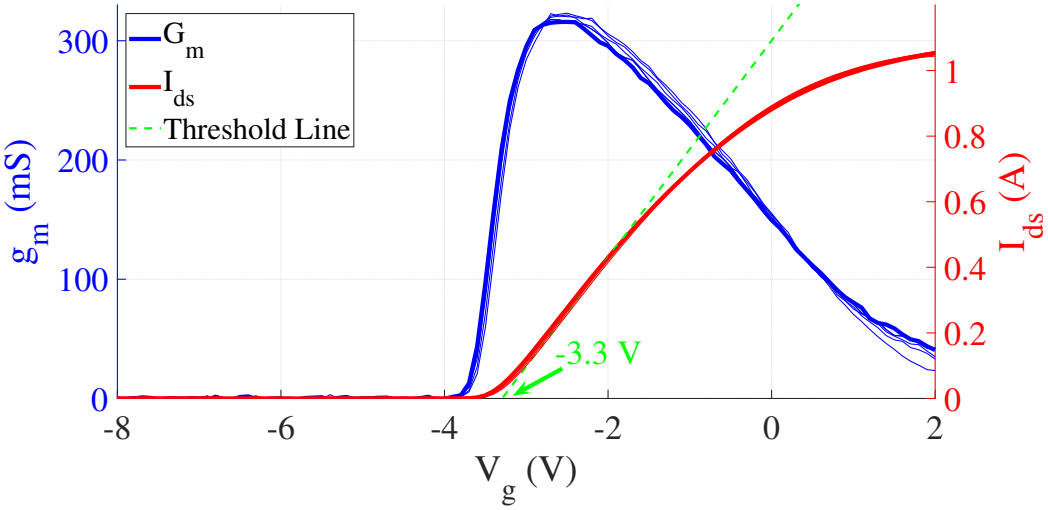


Figure 2.5: I_d vs. V_{gs} measurement results of 8×125 μm HEMT.

Moreover, the forward I-V measurement is carried out to determine the turn-on point of the gate. We define the turn-on point as when the gate current exceeds 1 mA/mm. In the measurement, the gate voltage is swept from -8 to 2 V with 0.1 V steps, while the drain voltage is constant at 0 V. To prevent device destruction, the measurement system limits the current to 1 mA. Figure 2.6 shows that the HEMT is turned-on at $V_{gs} = 1.1$ V

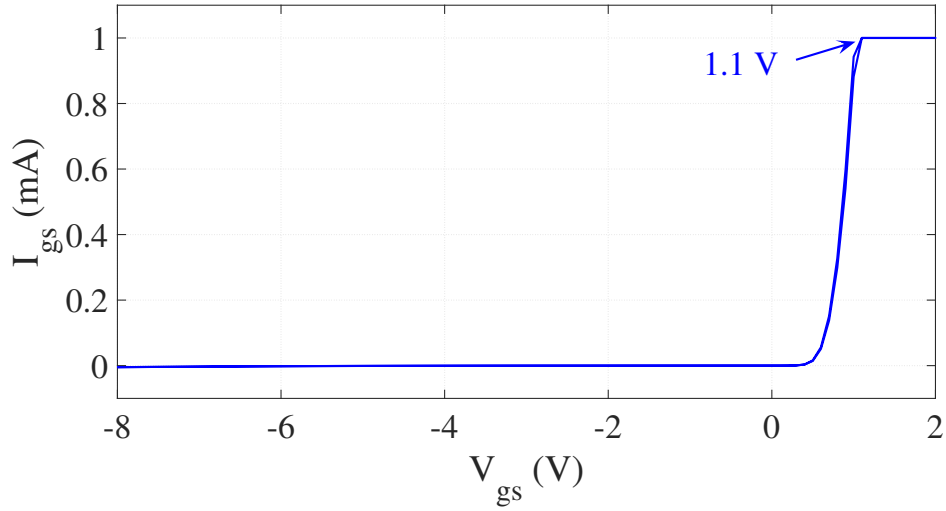


Figure 2.6: Forward I-V measurement results of 8×125 μm HEMT.

The final measurement in the DC section is taken to calculate the breakdown characteristics. The purpose is to find the maximum drain voltage level the device can handle while the gate is off. We define breakdown as the gate or drain leakage current exceeding 1mA/mm. The maximum voltage level under RF stress is $2V_{dd}$, so the breakdown voltage should be greater than 56 V since the recommended drain bias voltage is 28 V. To make conditions harsher, we have swept the drain voltage to 90 V to see if the transistor can handle $3V_{dd}$. Figure 2.7 shows that the gate and drain leakages are 35 μA and 232 μA at 90 V, respectively. Hence, the breakdown level is greater than 90 V. Table 2.1 summarizes the DC results.

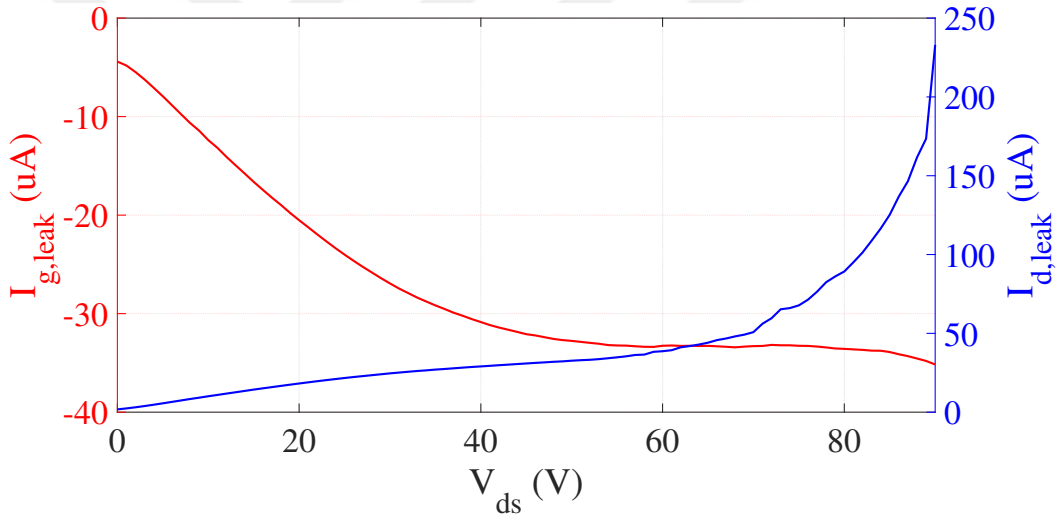


Figure 2.7: Breakdown measurement results of 8×125 μm HEMT.

Table 2.1: DC Measurement Results.

Characteristic	**Value**
Current Density @ V_g = 1 V	1.01 A/mm
V_{knee} @ V_g = 1 V	4.6 V
R_{on} @ V_g = 1 V	3.1 Ω x mm
V_{th}	-3.3 V
$g_{m,max}$	315 mS/mm
V_{br}	> 90 V
$I_{d,leak}$ @ V_d = 28 V	23 µA/mm
$I_{g,leak}$ @ V_d = 28 V	26 µA/mm

2.2 RF-Small Signal Measurements

The second step of the characterization is to get scattering parameters. Scattering parameters describe the input and output relations of a system [24]. Figure 2.8 shows the signal graph of a two-port system.

$$a_x \triangleq \frac{1}{2}\left(\frac{V_x}{\sqrt{Z_0}} + I_x\sqrt{Z_0}\right) \quad (\sqrt{W}) \tag{2.1}$$

$$b_x \triangleq \frac{1}{2}\left(\frac{V_x}{\sqrt{Z_0}} - I_x\sqrt{Z_0}\right) \quad (\sqrt{W}) \tag{2.2}$$

Figure 2.8: Signal flow of 2-port system.

With a and b, S-parameters are defined in the equation 2.3. S_{11} and S_{22} represent the input and output reflection coefficients with respect to Z_0 (in our case 50 Ω) which are used to design matching networks to eliminate mismatches. S_{21} represents the gain of 2 port network. With S-parameters, we can find the stability factor and the maximum gain.

$$\begin{aligned} S_{11} &= \left.\frac{b_1}{a_1}\right|_{a_2\,=\,0} & S_{12} &= \left.\frac{b_1}{a_2}\right|_{a_1\,=\,0} \\ S_{21} &= \left.\frac{b_2}{a_1}\right|_{a_2\,=\,0} & S_{22} &= \left.\frac{b_2}{a_2}\right|_{a_1\,=\,0} \end{aligned} \tag{2.3}$$

We will discuss stability in Chapter 3 in detail; however, to understand maximum gain, Rollet's stability factor (K) is needed. The K factor shows if the active device is stable in that frequency or not [24]. If $K > 1$ and $\text{mag}(\Delta) < 1$,

the device is unconditionally stable. We want our design to be unconditionally stable from DC to 26 GHz. Equation 2.4 gives the stability factor in terms of S-parameters [24].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}, \ \Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.4}$$

The maximum gain equation consists of two regions for an active device: Maximum Available Gain (GMAX or MAG) and Maximum Stable Gain (MSG). The MAG is only defined in the regions where K>1 since equation 2.5 becomes imaginary in other regions. For K<1, MSG gives the maximum gain.

$$MAG = (K - \sqrt{K^2 - 1}) \frac{|S_{21}|}{|S_{12}|} \tag{2.5}$$

$$MSG = \frac{|S_{21}|}{|S_{12}|} \tag{2.6}$$

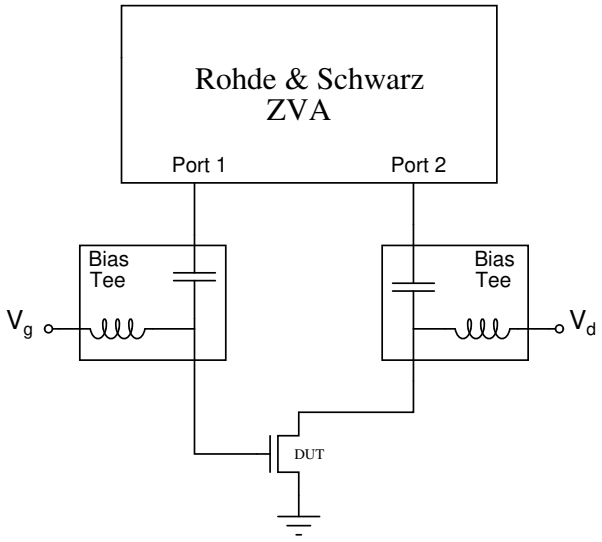


Figure 2.9: Schematic of the RF Measurement Setup.

The measurement setup in Figure 2.9 characterizes the S-parameters, which consist of Rohde&Schwarz ZVA vector network analyzer and two bias tees to feed DC bias externally. The process technology recommends biasing a transistor

28 V, 100 mA/mm, so these conditions are used. Port 1 applies −30 dBm input power to the gate of the transistor. Al signals are in CW condition. Figure 2.10 shows the input and output reflection coefficient results (S_{11} and S_{22}) on the Smith Chart.

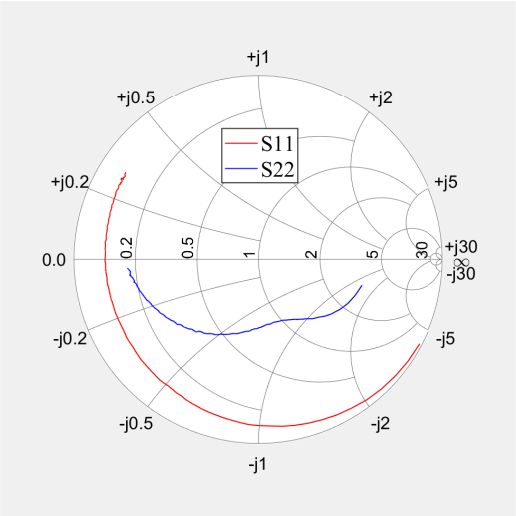


Figure 2.10: S_{11} and S_{22} of the transistor from 0.4 to 26.5 GHz.

From equation 2.5 and 2.6, maximum gain is derived using the S-parameters. Figure 2.10 shows the port 2 gain (S_{21}) and Max Gain of our HEMT. At 10 GHz, the 8×125 μm transistor has a 17 dB max gain.

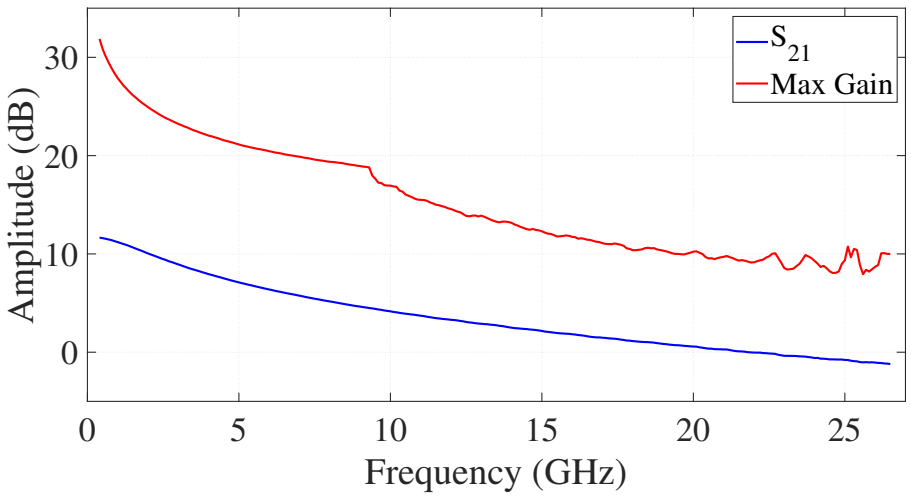


Figure 2.11: S_{21} and Max Gain of the Transistor.

2.3 Load-Pull Measurements

In the characterization step, it is essential to determine the impedances that give maximum power, gain, or efficiency. The load-pull measurement analyzes the DUT for varying source and load impedances. The system tracks a and b parameters and calculates gain, efficiency, and power levels for each impedance. The load-pull setup is described in Figure 2.12.

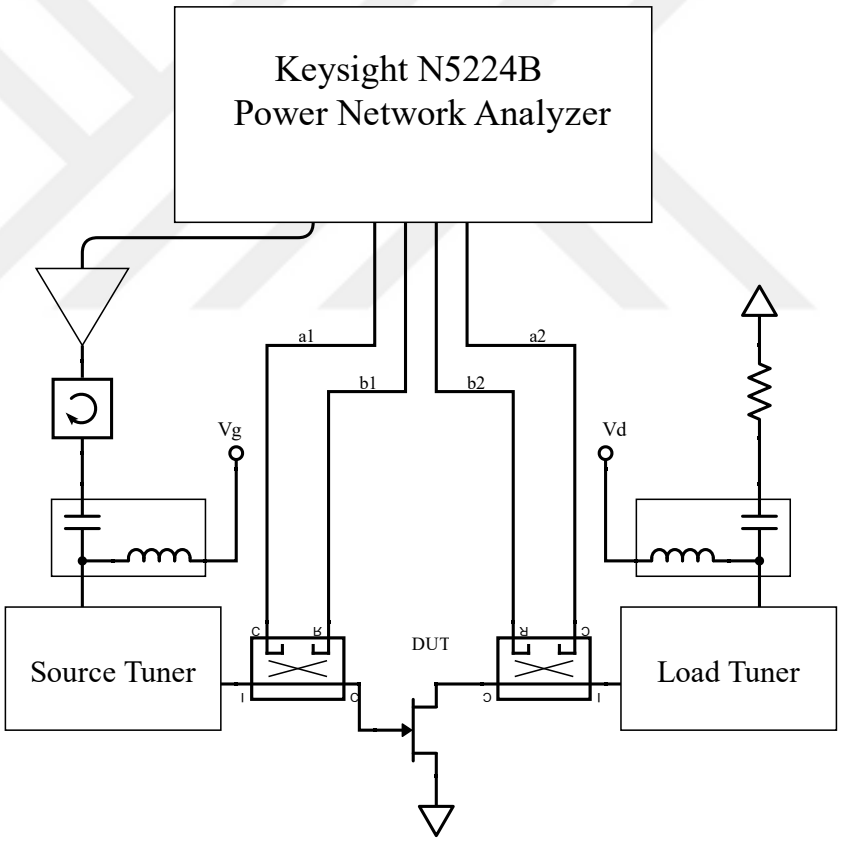
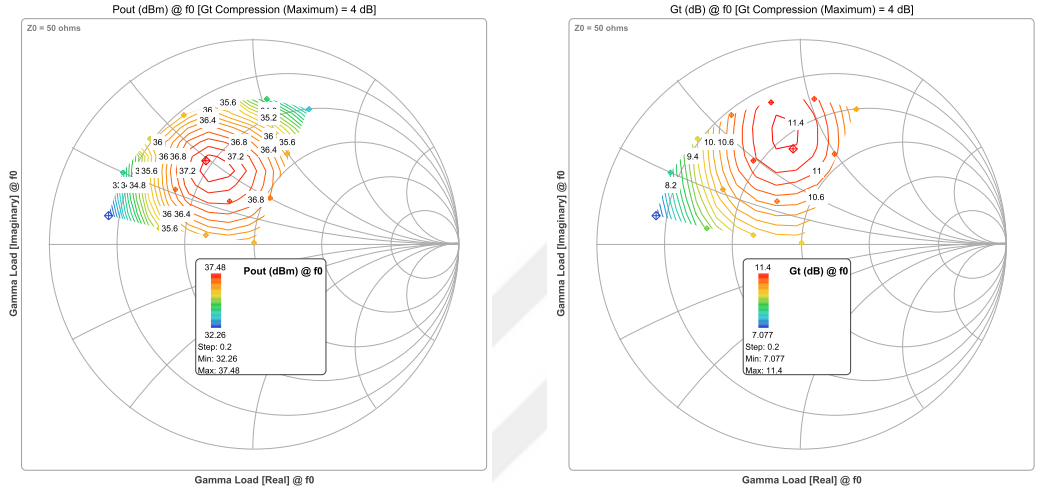


Figure 2.12: Schematic of the Load-Pull measurement setup.

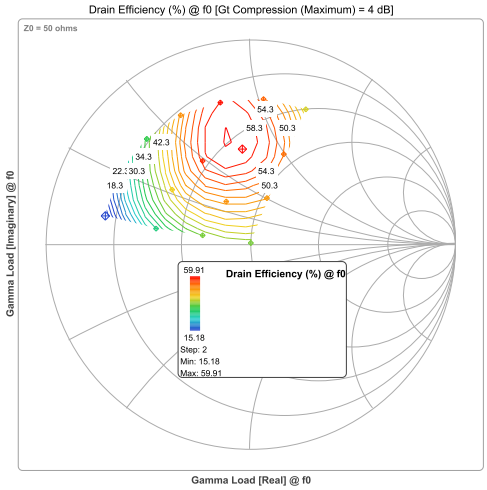
The setup uses Keysight N5224B Power Network Analyzer for measurements. The AMCAD 3200 PIV system generates a gate and drain bias signal. Maury impedance tuners are used for changing source and load impedances. A driver amplifier amplifies the input power since PNA's maximum power level is insufficient. The circulator is connected to the output of the driver amplifier to protect

the amplifier from reflected signals. Hybrid couplers deliver a and b parameters to the PNA.



(a) Power Contours

(b) Gain Contours



(c) Drain Efficiency Contours

Figure 2.13: 10 GHz Load-Pull measurement results at 4 dB compression point.

We have not performed source-pull measurements since IV-CAD software has a source-pull toolbox. For load-pull, the source impedance is fixed to 8 +3j. The transistor is biased with the same values in the RF measurements. The delivered input power is swept from −5 dBm to the 26 dB compression point for each load impedance. We have looked into 4 dB compression points at 10 GHz. Figure 2.13 shows the results.

The maximum output power is 5.6 W, given at a load impedance of 23+24j, where voltage and current swings reach their maximum. At the same impedance, the large signal gain is 11 dB, and drain efficiency (DE) is 53.7%. However, the maximum gain and efficiency impedances differ from 23+24j due to the non-linear characteristics of HEMTs. The maximum efficiency is 55.9% at 20+40j, and the maximum gain is 11.2 dB at 30+35j.

2.4 Summary

Table 2.2 summarizes the measurement results in this chapter. We will use these parameters in Chapter 3 to determine transistor sizes and topology.

Table 2.2: DC, RF and Load-Pull Measurement Results of 8x125 µm HEMT.

Characteristic	**Value**
Current Density @ V_g = 1 V	1.01 A/mm
V_{knee} @ V_g = 1 V	4.6 V
R_{on} @ V_g = 1 V	3.1 Ω x mm
V_{th}	−3.3 V
$g_{m,max}$	315 mS/mm
V_{br}	> 90 V
$I_{d,leak}$ @ V_d = 28 V	120 µA/mm
$I_{g,leak}$ @ V_d = 28 V	130 µA/mm
Max Small-Signal Gain @ 10 GHz	17 dB
Power Density @ 10 GHz and 4 dB Comp.	5.6 W/mm
Max Drain Efficiency @ 10 GHz and 4 dB Comp.	55.9%
Max Gain @ 10 GHz and 4 dB Comp.	11.2 dB

Chapter 3

Power Amplifier MMIC Design

In this chapter, we present a high-gain three-stage X-Band MMIC power amplifier using the process parameters of Chapter 2. First, the topology and transistors are selected to fulfill the specifications in Table 3.1, which are at 25 ° C base temperature and 10% pulse condition. Then, we have stabilized our HEMTs using the Freitag Method. After continuing with matching circuit schematic and layout designs, the MMIC was ready for tape-out.

Table 3.1: MMIC Specification Goals at 25 °C and 10% Pulsed Condition.

Specification	**Value**
Frequency Range	8.5 - 10.5 GHz
Small Signal Gain	$>$ 35 dB
Input Return Loss	$>$ 10 dB
Output Return Loss	$>$ 8 dB
Gain Ripple	$\pm$ 2 dB
Output Power (P_{sat})	$>$ 43 dBm
Efficiency (PAE at P_{sat})	$>$ 40%
Area	3.8 mm $\times$ 2.7 mm

3.1 Process Technology and Topology & Transistor Selection

In addition to the transistor process, process parameters regarding passive elements are needed for matching circuit designs. The SiC substrate has a 100 µm thickness with 9.66 relative permittivity. Two metal layers are available for the designer, which are MET1 with 1 µm thickness and MET2 with 4 µm. The current density for MET2 is 16 mA/µm, and MET1 is 4 mA/µm proportional to its thickness. For the MIM capacitors, 240 nm Si_3N_4 is used as an insulator between MET1 and MET2 resulting with 270 pF/mm^2 capacitor density. An air bridge allows MET2 to cross MET1 without a significant capacitive coupling. Figure 3.1 illustrates the substrate layers.

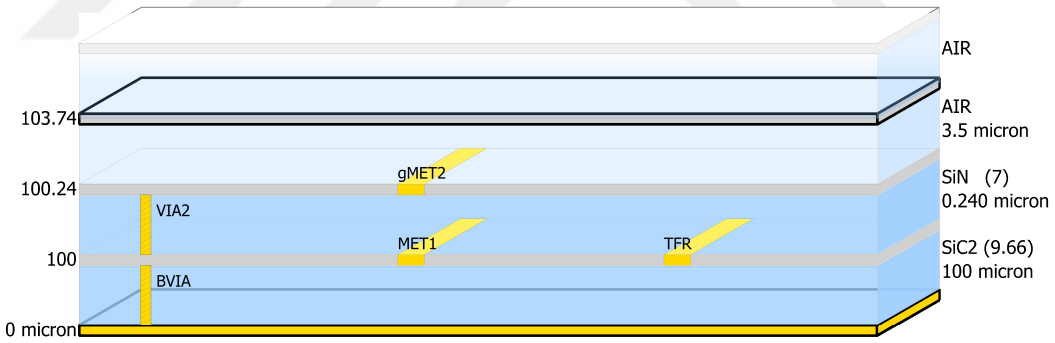


Figure 3.1: Substrate Layers of NANOTAM 250 nm GaN on SiC Process.

The primary motivation behind the MMIC is obtaining 43 dBm output power while having a small signal gain of 35 dB and efficiency better than 40%. A three-stage topology is selected to obtain a high gain since a two-stage design would not be enough to reach the goal. Regarding transistor numbers, the 1:1:4 ratio is selected for simplicity, as shown in Figure 3.2. If transistor peripheries are large enough to drive the next stage, the number of transistors is not a problem.

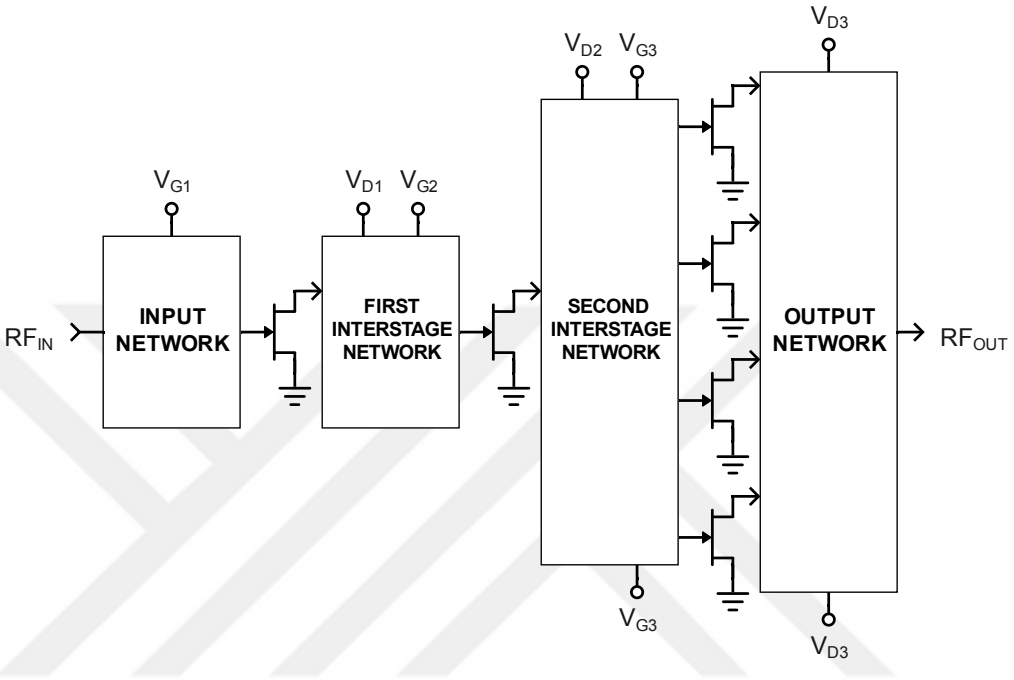
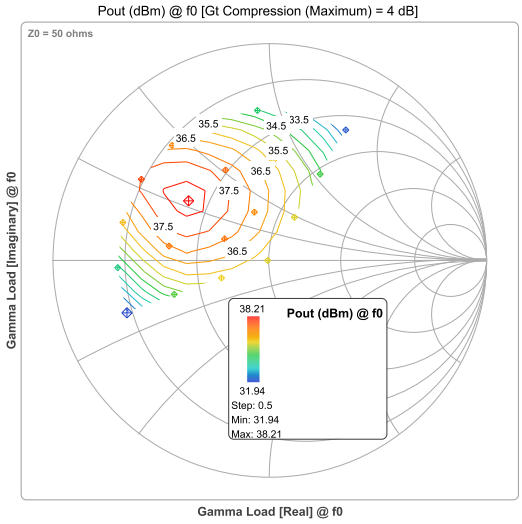
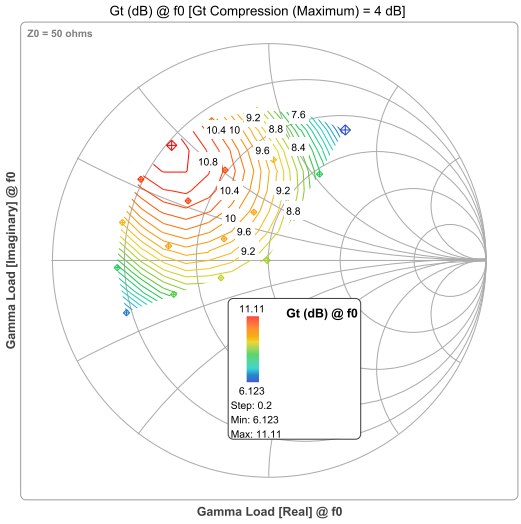


Figure 3.2: Block Diagram of the 3 Stage X-Band MMIC with 1:1:4 topology.

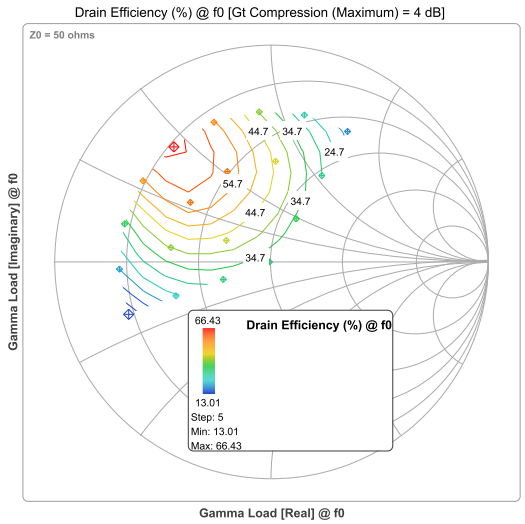
The process technology promises 5.5 W/mm power density at around 10 GHz. To obtain output power greater than 20 W, the last stage should have at least a 3.6 mm periphery without the losses. If we add a margin of 20% to size and aim for 0.5 dBm loss at the output stage, the size should be between 4.5−5 mm. Hence, 4 of 2×6×100 µm HEMTs should be enough. The HEMT has a maximum available gain of 18.6 dB at 10 GHz, as shown in Figure 3.6. Figure 3.3 shows the load-pull results at the 9.5 GHz and 4 dB compression point. One of the HEMTs can deliver a maximum of 6.62 W power, 11.11 dB gain, and 66.43% DE. Since the maximum points of these parameters differ on the smith-chart, we have to choose an optimal point to aim for. So, we have chosen Z_L = 15+22j and Z_S = 5+0j impedance points to combine high gain and power. The points for the start and end of the frequency band are provided in Table 3.2.



(a) Power Contours



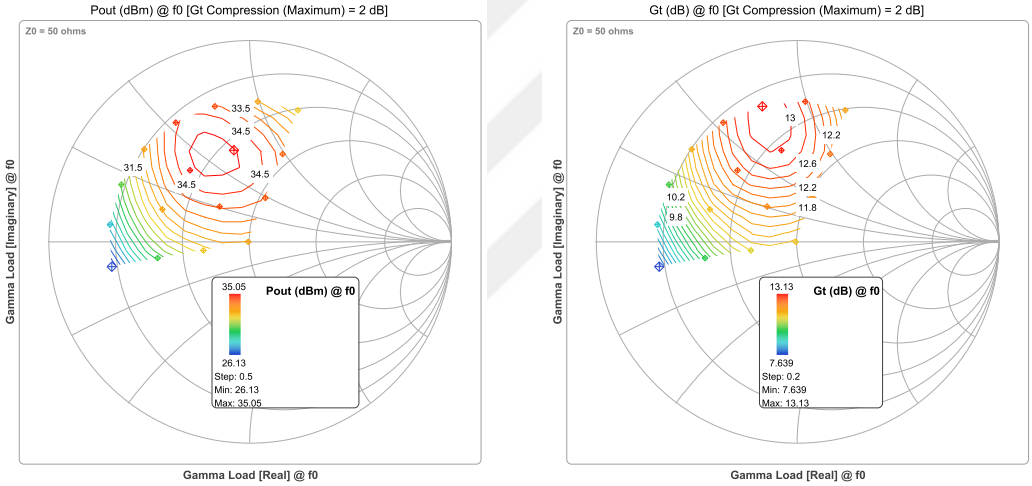
(b) Gain Contours



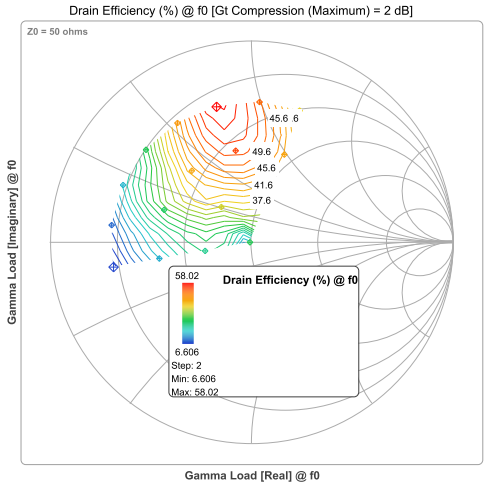
(c) Drain Efficiency Contours

Figure 3.3: 2x6x100 µm HEMT Load-Pull measurement results at 4 dB compression point and 9.5 GHz.

The middle stage has to drive the last stage without compromising PAE and gain. The transistor should deliver 0.5 W to the latter HEMTs at a minimum. However, the power splitter and stability networks at the second inter-stage bring significant losses. If we aim for a 3 dB loss, the chosen HEMT should deliver output power above 1 W at a compression point below 4 dB. Hence, 8×125 µm HEMT can be used. It can deliver 3 W output power with 58% DE and 13.1 dB gain at a 2 dB compression point and 9.5 GHz. So, we choose Z_L = 17+40j and Z_S = 5+8j. The HEMT has a 16 dB MAG around 10 GHz.



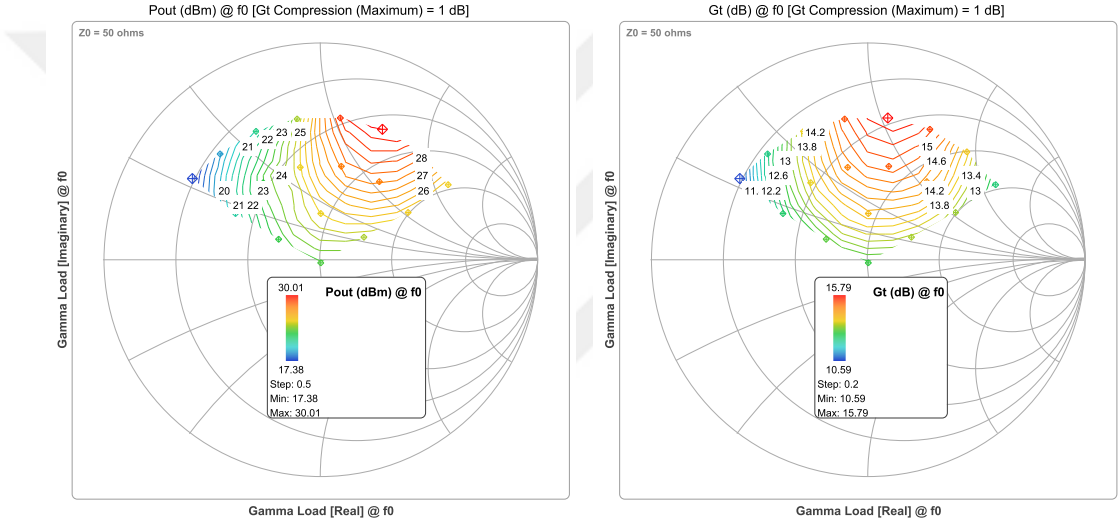
(a) Power Contours (b) Gain Contours



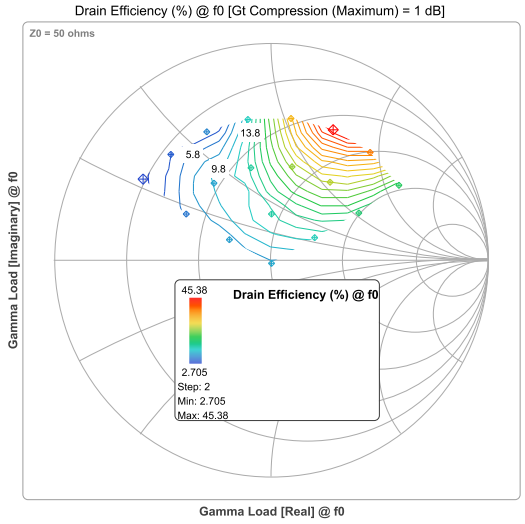
(c) Drain Efficiency Contours

Figure 3.4: 8×125 µm HEMT Load-Pull measurement results at 2 dB compression point and 9.5 GHz.

Finally, the first stage acts as a driver amplifier, which means the gain is the priority. Since the second stage needs 0.3 W at minimum input power to drive the last stage, 0.5 mm HEMT is enough for sufficient output power. 4x125 µm HEMT would be a great choice with a 19 dB MAG. At a 1 dB compression point, the transistor can deliver 1 W output power and 15 dB large signal gain, as seen in Figure 3.5. We choose $Z_L = 35+70j$ and $Z_S = 5+19j$ to get maximum gain.



(a) Power Contours (b) Gain Contours



(c) Drain Efficiency Contours

Figure 3.5: 4x125 µm HEMT Load-Pull measurement results at 1 dB compression point and 9.5 GHz.

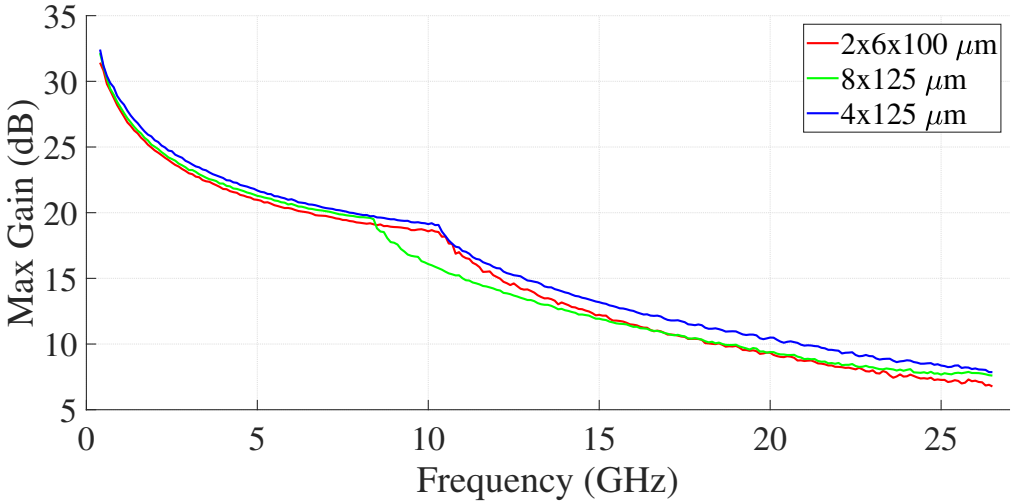


Figure 3.6: Maximum Gain of Chosen HEMTs from 0.4 to 26.5 GHz.

The same procedure has been repeated for 8.5 and 10.5 GHz to cover the frequency band. Table 3.2 shows all the chosen impedances. In Section 3.3, Matching Networks, we will design our circuits using these values.

Table 3.2: Target impedances optimal for each HEMT according to the pulsed load-pull measurements at the drain bias of 28 V, 100 mA/mm.

HEMT	**Frequency**	$\mathbf{Z_{source}}$	$\mathbf{Z_{load}}$
4×125	8.5 GHz	5+20j	40+75j
	9.5 GHz	5+19j	35+70j
	10.5 GHz	5+18j	28+65j
8×125	8.5 GHz	5+10j	20+40j
	9.5 GHz	5+8j	17+40j
	10.5 GHz	5+5j	16+28j
2×6×100	8.5 GHz	5+3j	15+25j
	9.5 GHz	5+0j	15+22j
	10.5 GHz	5-3j	12+20j

3.2 Stability Network Design and Analysis

Stabilizing transistors is crucial to prevent undesired oscillations that could damage circuit and measurement equipment under large signals. We briefly mentioned the stability in section 2.2 since it is directly linked to maximum gain. In this section, we have analytically discussed how to design networks to prevent oscillation and how to analyze them.

The stability can be divided into two: odd and even modes. Even mode stability considers all the parallel transistors excited with the same phase and amplitude [25]. This can be checked with the K factor in equation 2.4 [26]. On the other hand, the odd mode considers the changes in phase and magnitude for parallel transistors [27]. For odd mode, we used the Freitag method [27]. Since only the last stage has multiple parallel transistors, we only applied the Freitag method to this stage.

To ensure even mode stability, the real part of the impedance seen by a transistor has to be positive [24]. Regarding S parameters, the conditions in equation 3.1 make the circuit unconditionally stable.

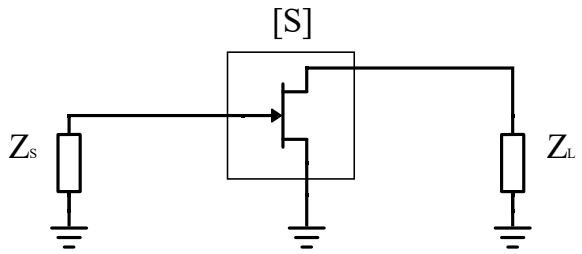


Figure 3.7: Transistor with Load and Source.

$$\begin{aligned} \left| S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L} \right| \leq 1 \quad for\ all \quad |\Gamma_L| \leq 1 \\ \left| S_{22} + \frac{S_{21}S_{12}\Gamma_S}{1 - S_{11}\Gamma_S} \right| \leq 1 \quad for\ all \quad |\Gamma_S| \leq 1 \end{aligned} \tag{3.1}$$

K factor puts these conditions into one equation. If K $>$ 1 and $\Delta < 1$, the circuit is unconditionally stable. To ensure this, we need to use resistive networks. We put our stability network to the gate sides of the transistors since we do not want to burn power at the output.

We used a parallel RC network and a series RL network for all stages given in Figure 3.8. RL networks dominate lower frequencies, whereas RC networks dominate higher frequencies. The stability network is used as a part of the gate bias circuit. Therefore, a bypass capacitor is added to the network after the gate bias to reduce spikes and improve RF isolation.

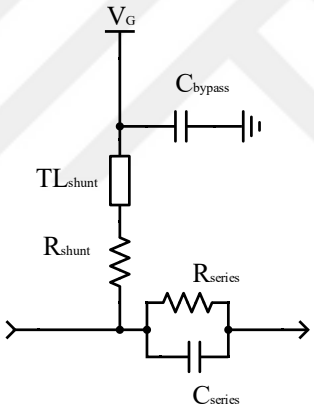
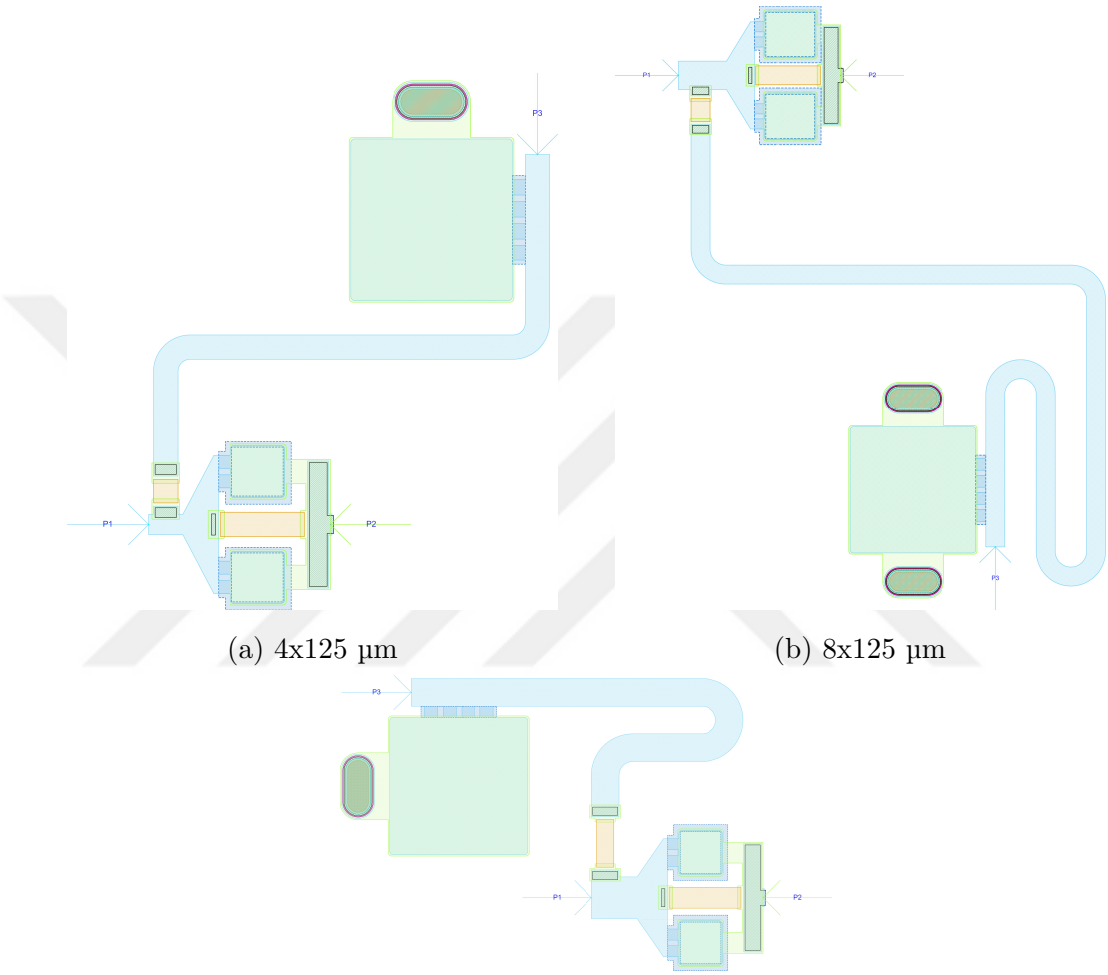


Figure 3.8: Stability network topology for the transistors.

Figure 3.9 shows the designed stability networks for each stage. The orientations of the networks were edited after the matching networks. The series capacitors are divided into two for symmetry. The values of components are tuned to preserve a high maximum gain in the band. Figure 3.10 illustrates the results of these networks. The minimum of K factors are located in the band for gain. The values are just above unity since the matching networks bring extra losses and increase the value after the full design. We have designed the stability network of the first stage with more loss than others since too much gain can also be problematic and cause oscillations after tape-out. Δ of each design is less than one; hence, the stages are unconditionally stable. The maximum available gains are reduced to 14 dB at the first stage and 16 dB at the second and third

stages at 10 GHz.

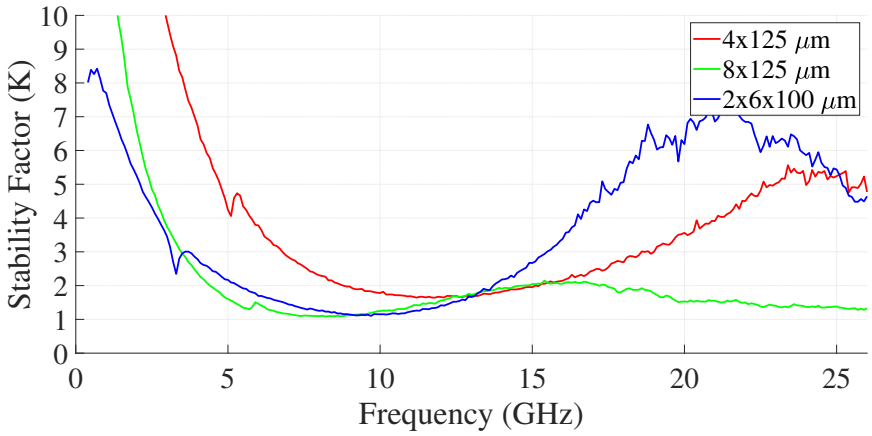


(a) 4x125 µm

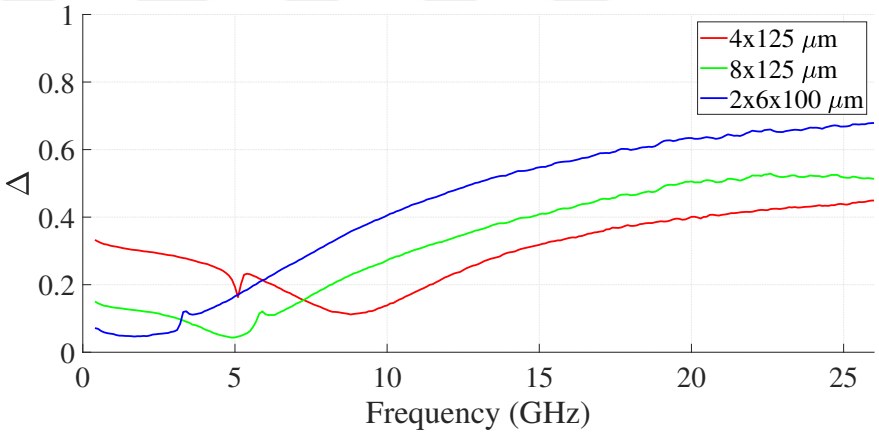
(b) 8x125 µm

(c) 2x6x100 µm

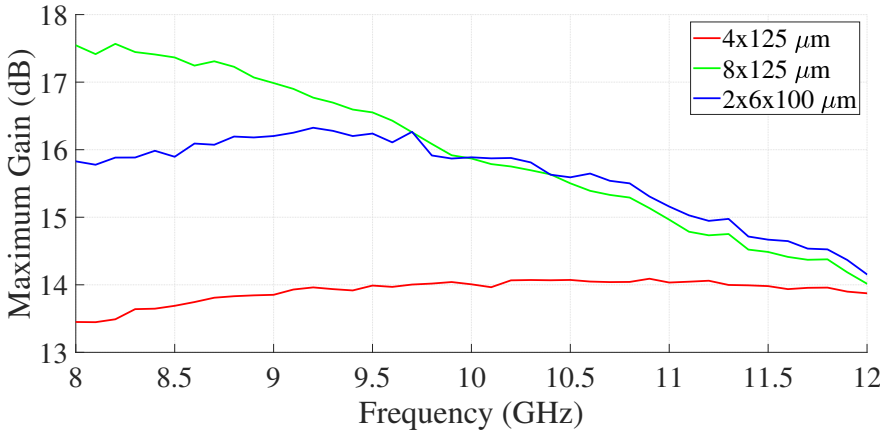
Figure 3.9: Stability Network Layouts of Each HEMT.



(a) K Factor after Stability Network



(b) Δ after Stability Network



(c) Max Gain after Stability Network

Figure 3.10: Results of Stability Networks.

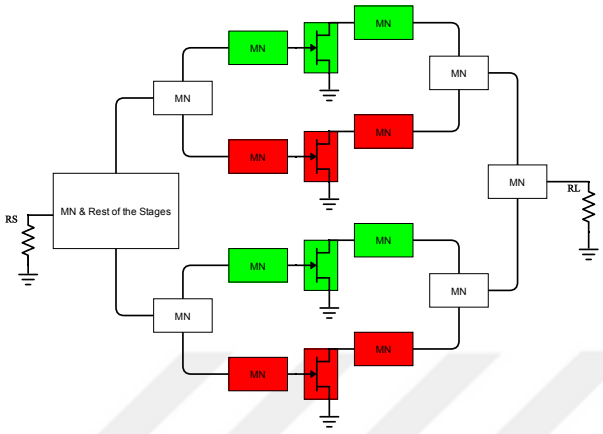
The last stage consists of four parallel transistors to fulfill output power criteria. The simulation design assumes four transistors are identical. However, variations in the fabrication may result in changes in transistor parameters. This could result in mismatches in the phase and magnitude of the RF signal during power splitting and combining and eventually might lead to oscillations [25]. Hence, the parallel transistors create a multi-loop system that requires special treatment in terms of stability. To tackle this issue, we have used the Freitag method to detect odd mode stabilities [27].

The Freitag method considers all the possible loops in the circuit. Four parallel devices result in four orthogonal voltage/current modes, which are one even mode and three odd modes [27]. We have approached each combiner branch (after a HEMT) as a port and calculated impedances at the input and output in each one of them. In other words, ports are located at the drain node of each transistor.

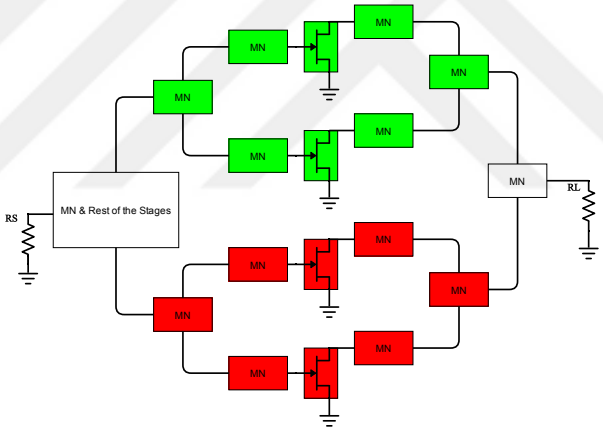
Freitag uses z parameters and current vectors at each branch to calculate eigenvectors where each eigenvector corresponds to a mode [27]. The resulting modes are given in Figure 3.11. The same colored branches describe modes of operation that are in the same phase. Voltage and current in red branches are 180° out of phase. Equation 3.2 explains the oscillation condition for the odd modes.

$$\left.\begin{array}{rcl} Re\{z_{odd,input,n} + z_{odd,output,n}\} & < & 0 \\ Im\{z_{odd,input,n} + z_{odd,output,n}\} & = & 0 \end{array}\right\} = n^{th}\ odd\ mode \tag{3.2}$$

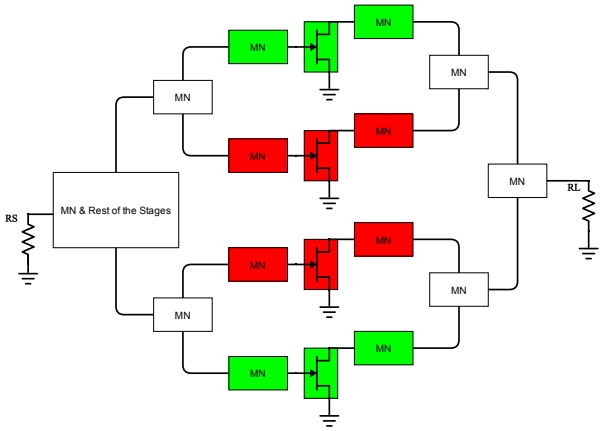
At each port, we want to avoid detecting this condition. With this purpose, odd mode resistors are added to both the input and output of HEMTs. The resistors are located between parallel HEMTs to improve stability, as shown in Figure 3.13. Figure 3.12 illustrates the real and imaginary parts of impedance sums according to equation 3.2. Since all the real parts are positive, we can say that the circuit is oscillation-free without looking at the imaginary parts.



(a) (+,-,+,-)

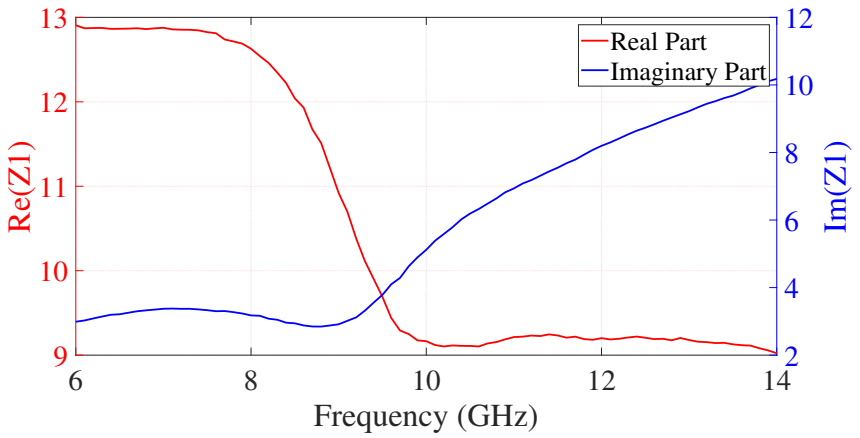


(b) (+,+,-,-)

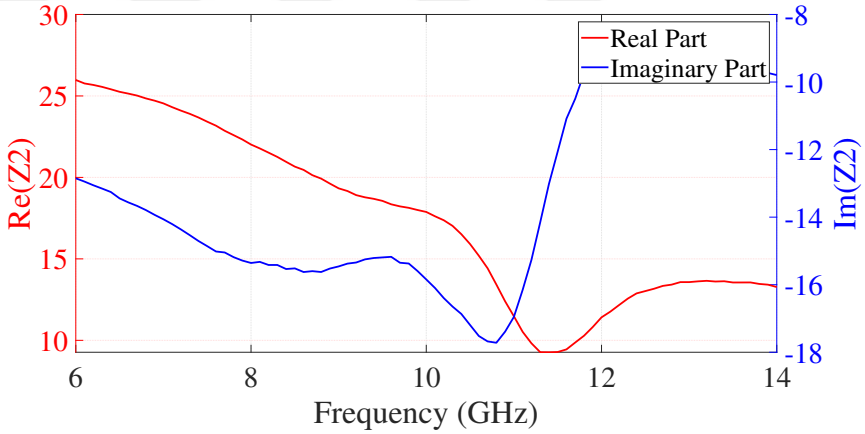


(c) (+,-,-,+)

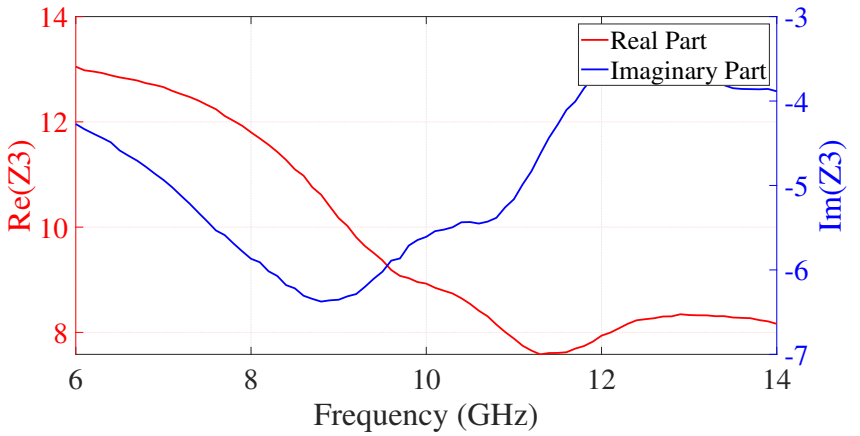
Figure 3.11: Schematic of the Odd Modes.



(a) Result of 1st Odd Mode



(b) Result of 2nd Odd Mode



(c) Result of 3rd Odd Mode

Figure 3.12: Result of Odd Mode Impedance Calculations.

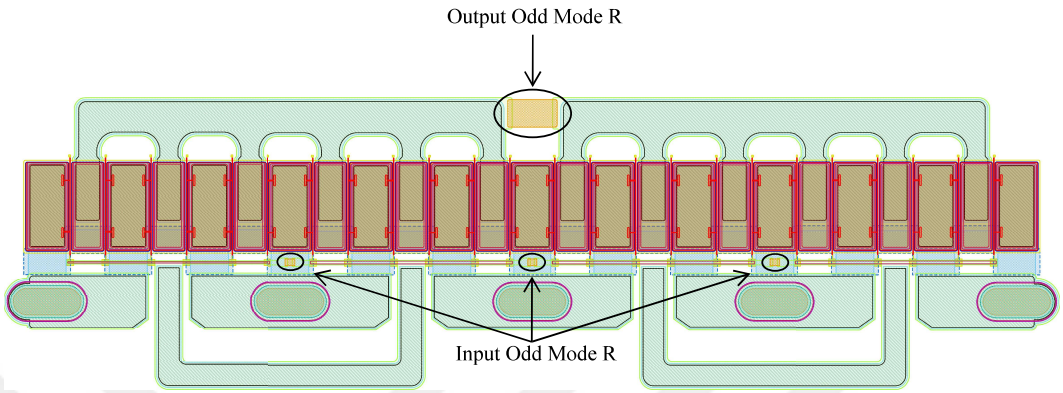


Figure 3.13: Two of 2×6×100 µm HEMTs with odd mode resistors.

3.3 Matching Networks

Matching networks are the most crucial part of the MMIC design since impedances shown to the transistors determine the amplifier's overall performance. We have used the values in Table 3.2 for our matching networks to get the desired specs. Networks consist only of transmission lines and capacitors.

3.3.1 Output Matching Network

We start the design from the output and continue towards the input since OMN is the most crucial part for the output power. We aim to strictly obey the load-pull results to get the desired power levels. However, the impedances for the other stages may vary to meet ripple and gain specifications since we need mismatches for a flat gain.

The output-matching network adopts a cluster-matching technique to present chosen impedances to transistors. We want all transistors to see the same impedance to avoid phase mismatches at branches. Figure 3.14 shows the general structure.

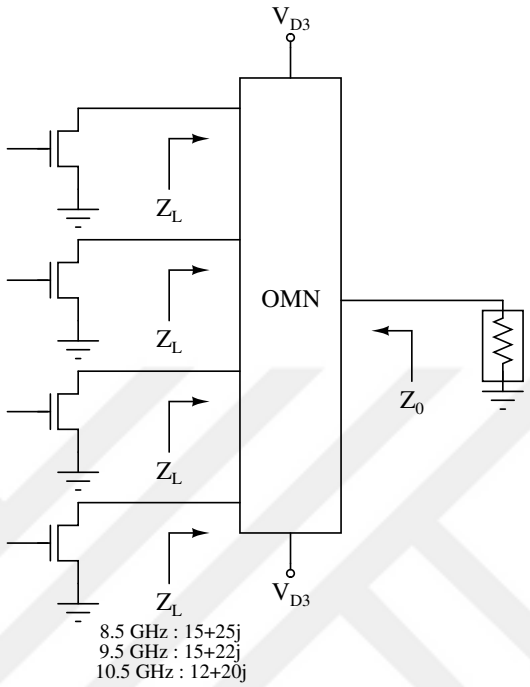


Figure 3.14: General Structure of Output Matching Network.

Power-combining circuitry only consists of transmission lines, as shown in Figure 3.15. We did not use any inductor since it requires a MET1 layer, and the current density of the layer is not enough to operate at high power levels. The bias lines are placed close to the transistors to reduce loss. By-pass capacitors are large enough to reduce current spikes and maintain RF isolation. The MIM capacitor has a non-ideal response at higher frequencies. The capacitance decreases as the frequency increases. Hence, a minimum number of capacitors is used in the RF line to reduce inconsistencies between the schematic and layout.

We adopt an asymmetrical matching during the layout design in Figure 3.16. In the schematic design, the ideal components do not include coupling effects and asymmetry in impedances presented to HEMTs. So, to show the same load impedances to inner and outer transistors, the shunt transmission lines in the middle are shortened. To increase the power handling of the shunt capacitor, two series capacitors are placed to decrease the voltage level on a capacitor from V to V/2. The shunt capacitor is divided into two parallel components to reduce the consequences of fabrication variances.

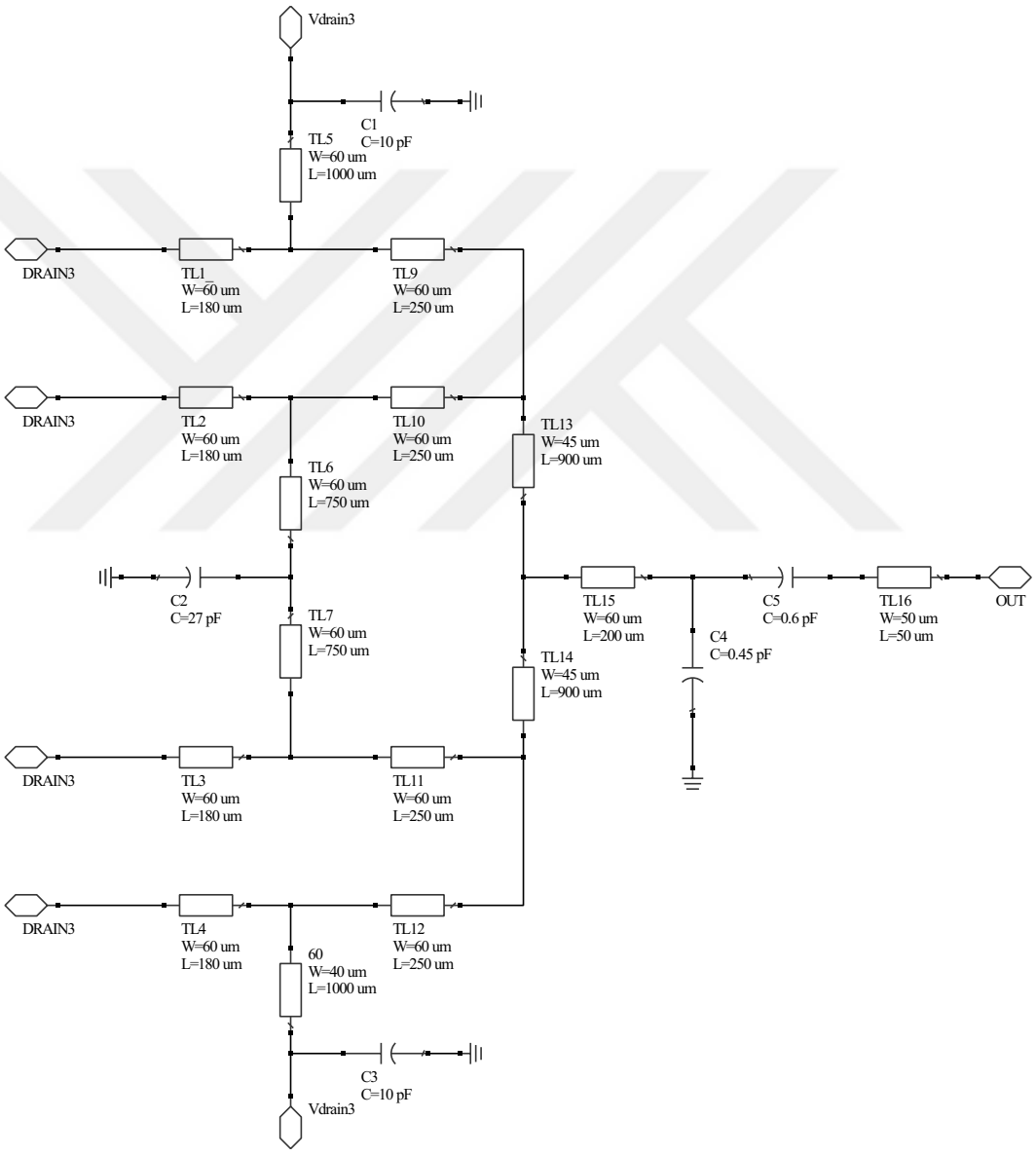


Figure 3.15: Schematic of Output Matching Network.

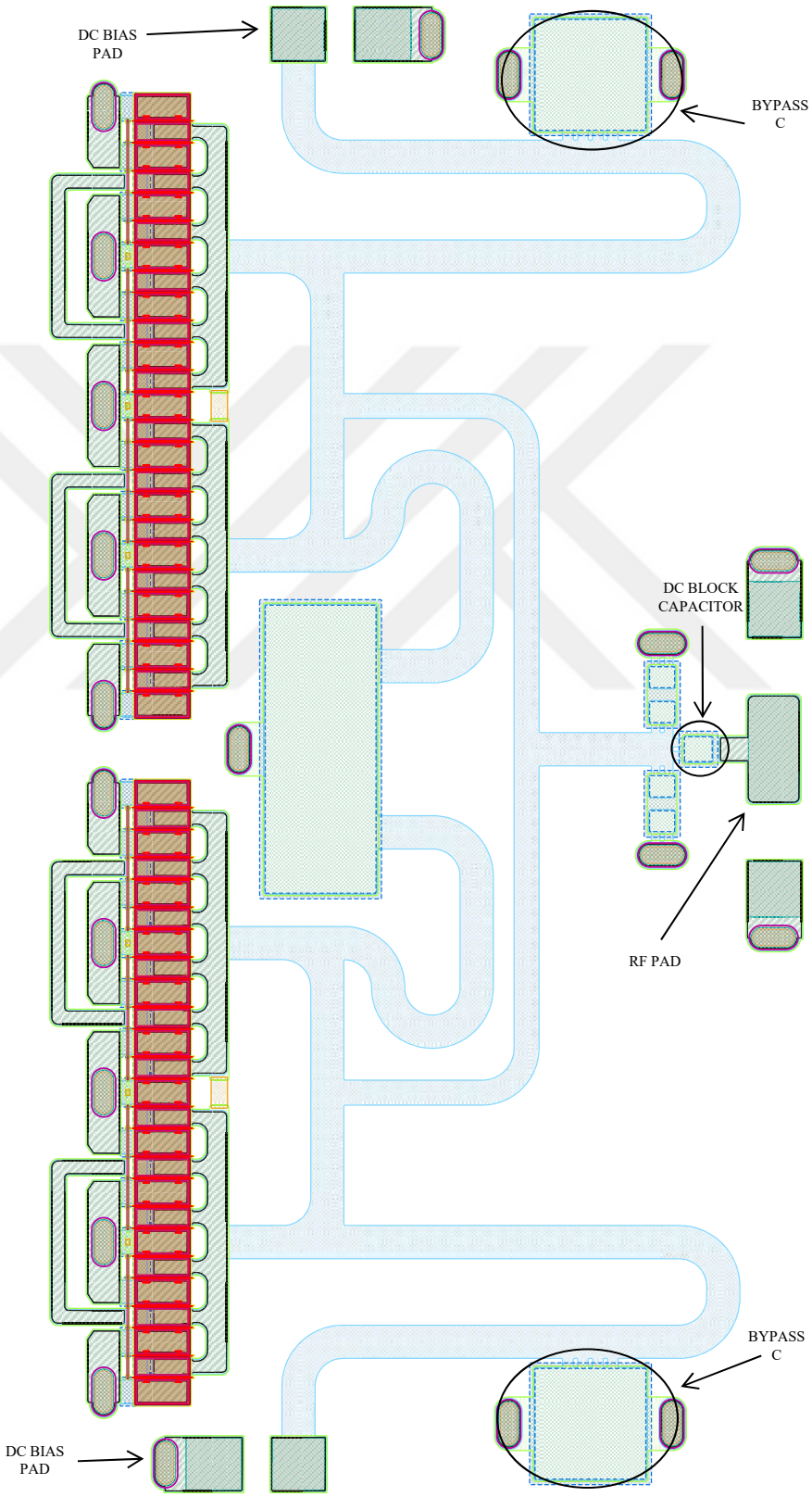


Figure 3.16: Layout of Output Matching Network.

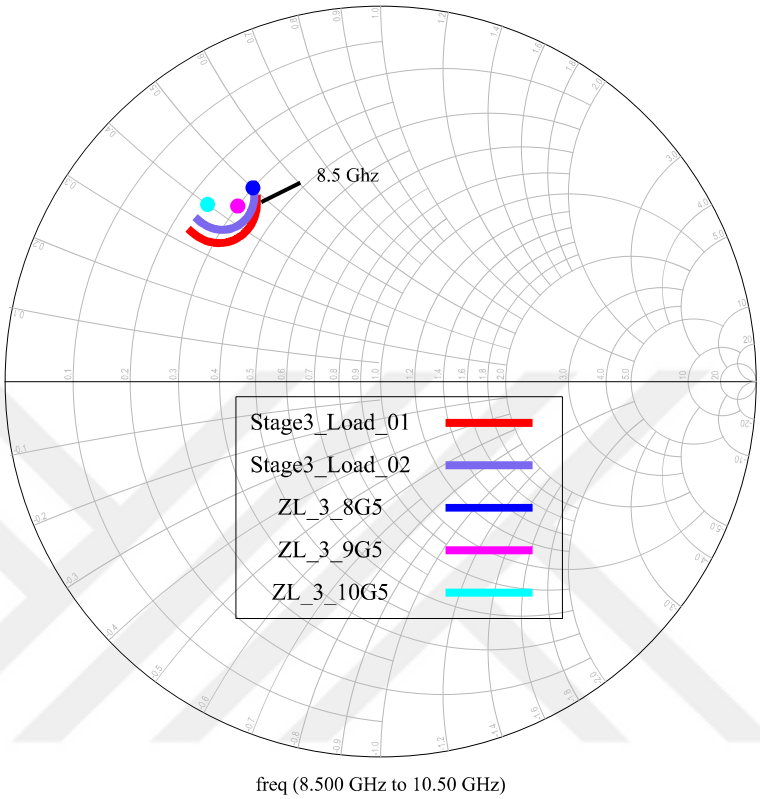


Figure 3.17: Impedance seen from drain of a 2x6x100 µm HEMT in the 3rd stage.

After EM simulations, the impedances seen by the HEMTs are very close to our target values. The inner and outer HEMT impedances almost overlap in the frequency band. With these, output power and PAE greater than 20 W and 40% should be achieved after the fabrication. The loss of OMN is around 0.5 dB.

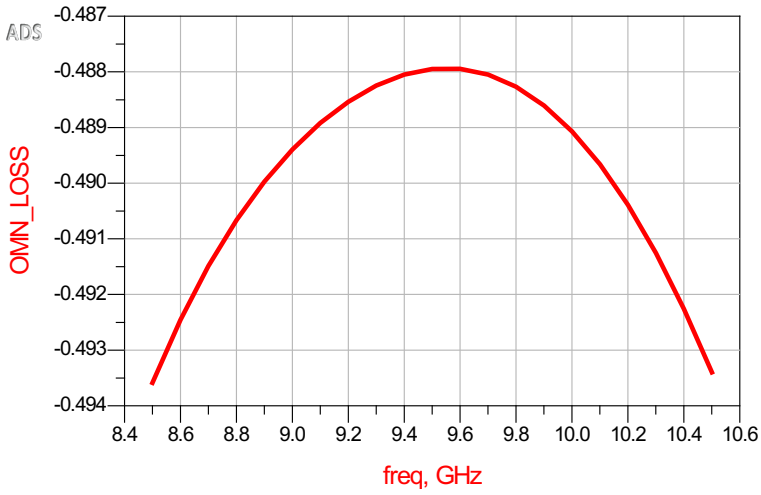


Figure 3.18: Loss at the Output Matching Network (dB).

3.3.2 Second Interstage Network

The second interstage network (ISMN2) is responsible for impedances presented to the third-stage transistors' gate and the second-stage's drain. Since achieving impedances in Table 3.2 for both sides is difficult, we must prioritize one before the design. The source impedance of transistors mostly affects the gain rather than output power. On the other hand, the load impedance of the second stage is crucial to deliver enough power to drive the third stage and to get high power at the output. Hence, the load impedance of 8×125 µm transistor is prioritized. Figure 3.19 shows the network structure.

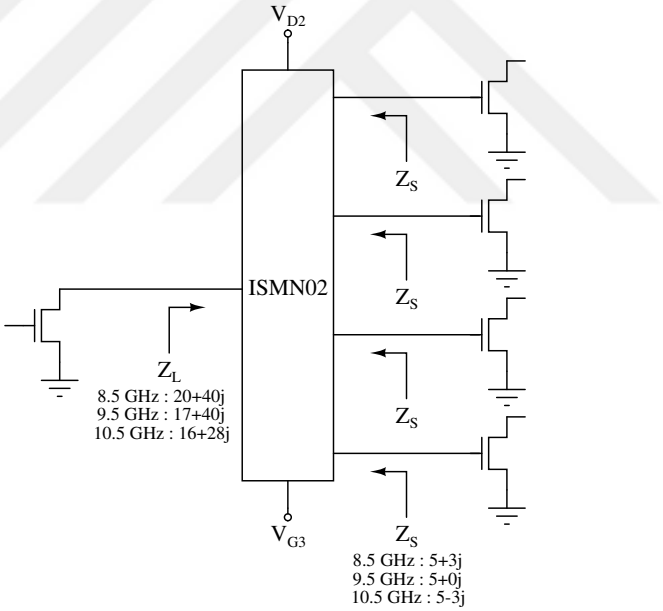


Figure 3.19: General Structure of Second Interstage Matching Network.

To get the desired performance in all of the frequency band, the order of the components is increased compared to the OMN. The network is horizontally symmetric to present the same impedance to each third-stage HEMT. In each branch, we have used a TL-C-TL combination. The design has one DC-Block capacitor and 3 bypass capacitors, and other components. The gate bias of the third stage has two ports, which are at the top and bottom, to get a uniform voltage distribution along the gates. This also affects the thermal distribution and overall MMIC performance. Figure 3.20 illustrates the overall network design.

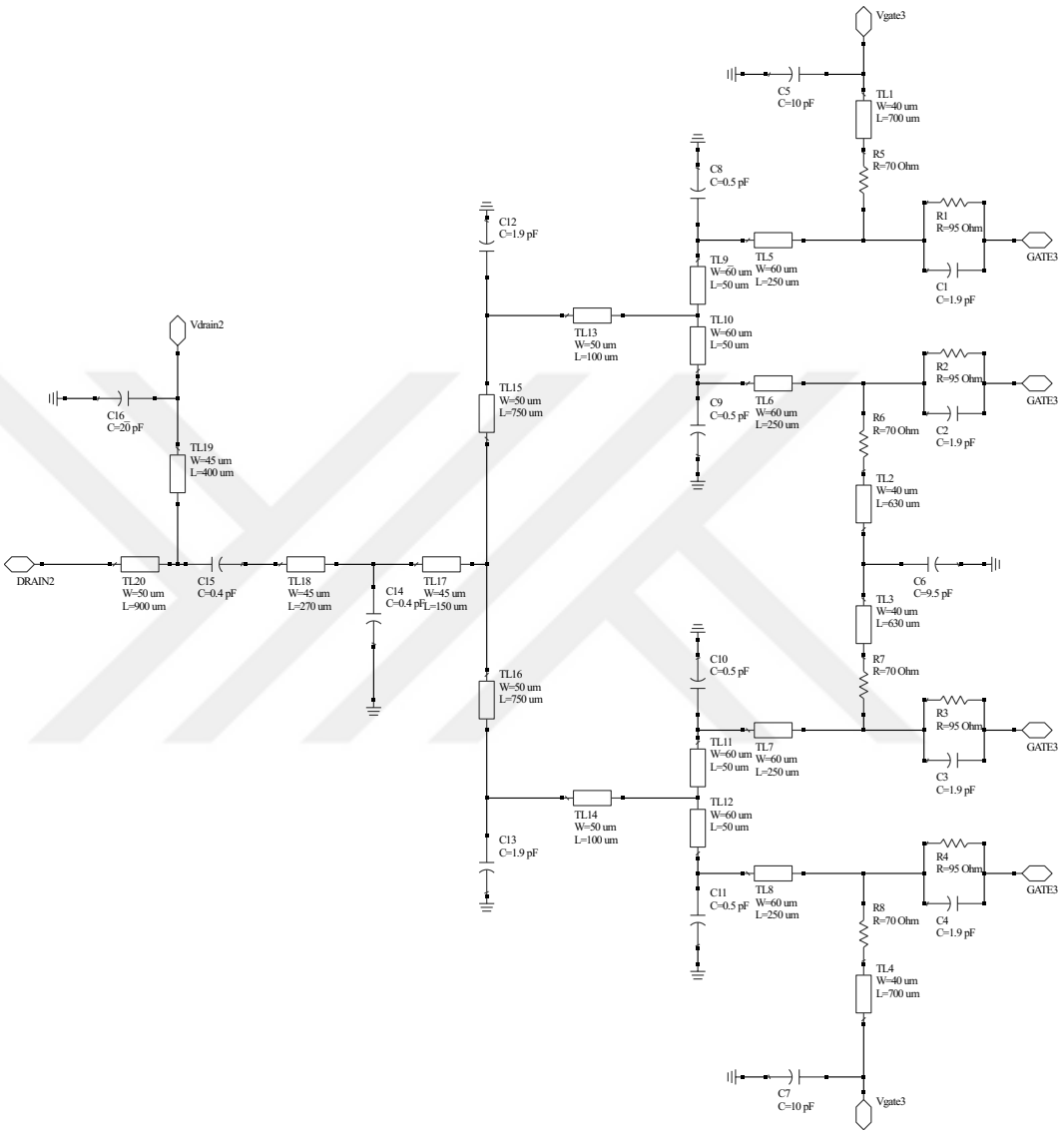


Figure 3.20: Schematic of Second Interstage Matching Network.

To protect symmetry for inner and outer HEMTs, shunt capacitors are divided into two parallel ones with the same capacitance in the power-dividing stage. Similar reasons in the OMN stage, the inner and outer shunt gate bias lines have different lengths to present the same impedances to inner and outer HEMTs. Two series capacitors are used for the DC-Block capacitor to reduce fabrication variance effects since the size would be very small if one capacitor was used. Figure 3.21 shows the layout of the ISMN2.

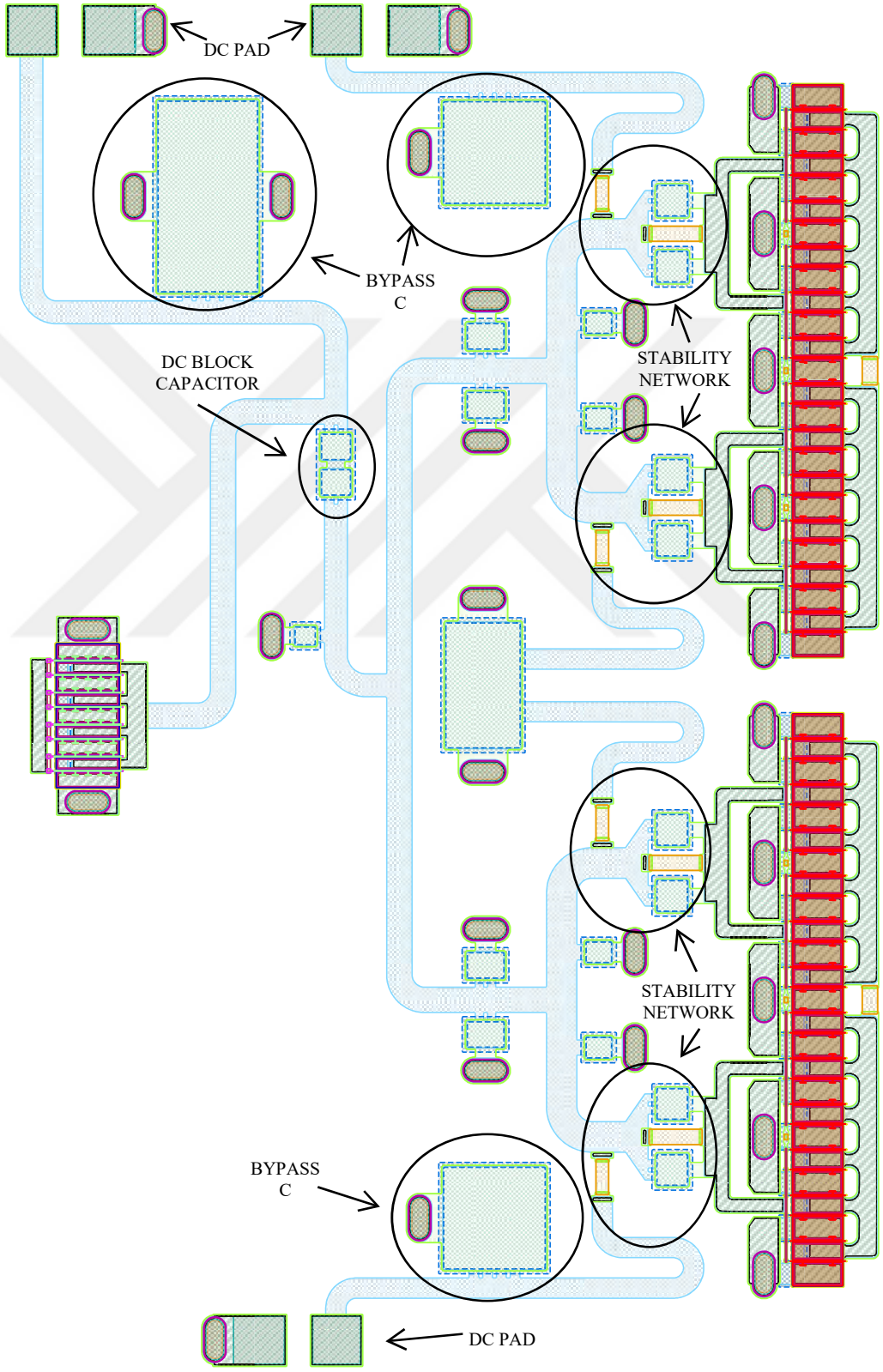


Figure 3.21: Layout of Second Interstage Matching Network.

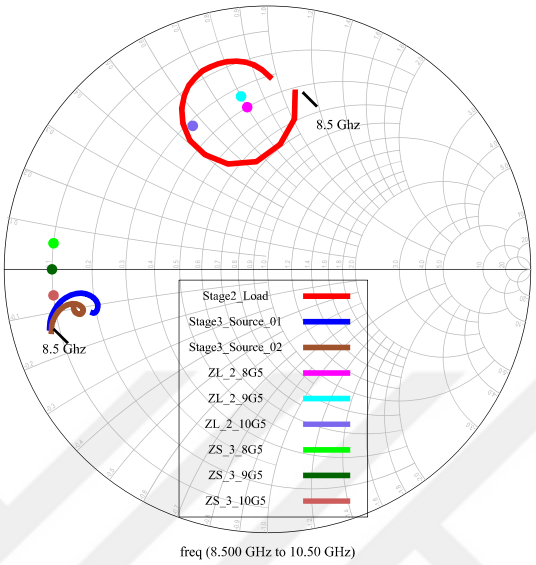


Figure 3.22: Impedances seen from gate of a 2×6×100 µm HEMT in the 3rd stage and drain of 8×125 µm HEMT in the 2nd stage.

The load impedance of 8x125 µm HEMT circles around the target impedances, as can be seen in the Smith chart in Figure 3.22. The source impedances of the inner and outer HEMTs of the third stage are almost identical. There is a small variance at the higher frequencies; however, it is not significant enough to affect overall performance. The loss of the matching network is higher at the lower frequencies with 2.35 dB and lower at the higher frequencies with 1.85 dB to get a flat gain. The average loss is around 2 dB, illustrated in Figure 3.23.

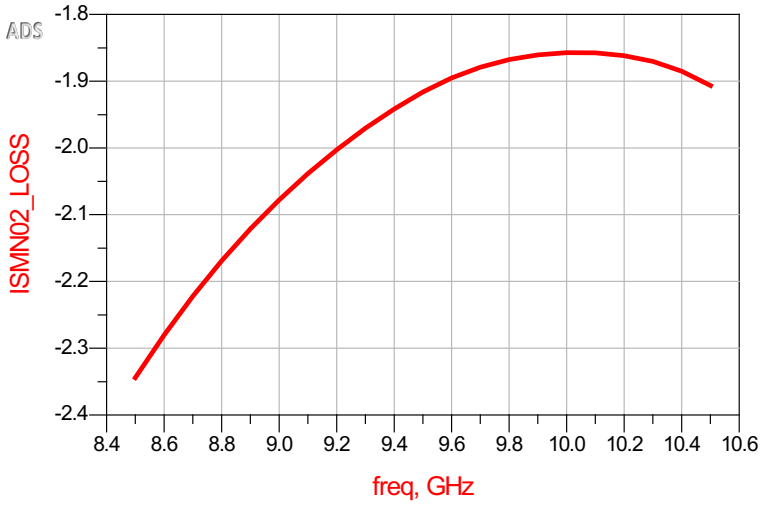


Figure 3.23: Loss at the Second Interstage Matching Network (dB).

3.3.3 First Interstage Network

The first interstage network (ISMN1) is simpler than the second since there is no power dividing/combining network; however, it is as important as the latter to get a high gain. The network is responsible for impedances presented to drain of the 4x125 µm first stage and source of the 8x125 µm second stage transistors. The chosen impedances (Figure 3.24) for the first stage are important to get enough power to drive the second; however, since the drive ratio is 1:2 between them, we can prioritize high gain and low loss for the network.

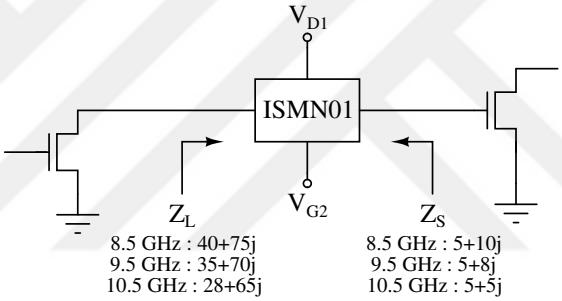


Figure 3.24: General Structure of First Interstage Matching Network.

The network design has only one branch with transmission lines and capacitors, described in Figure 3.25. Two bias lines are used for the drain of the first stage and gate of the second stage. Each one consists of a long transmission line and a bypass capacitor. For matching, TL-C-TL topology is used for both sides divided by a DC-Block capacitor.

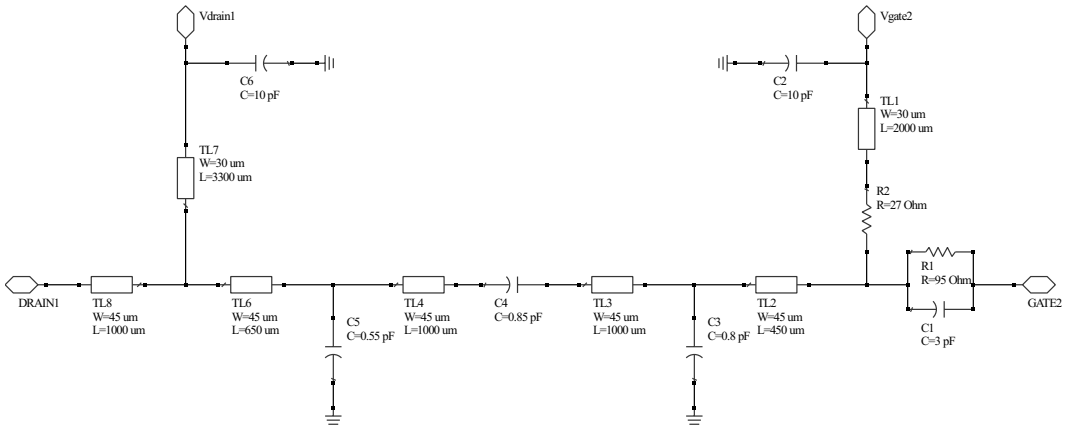


Figure 3.25: Schematic of First Interstage Matching Network.

The network layout is designed using mostly the y-axis to fit in the specified area. Both bias pads are at the bottom, as shown in Figure 3.26. The capacitors are not divided into two like the previous networks since the values are not too small nor big.

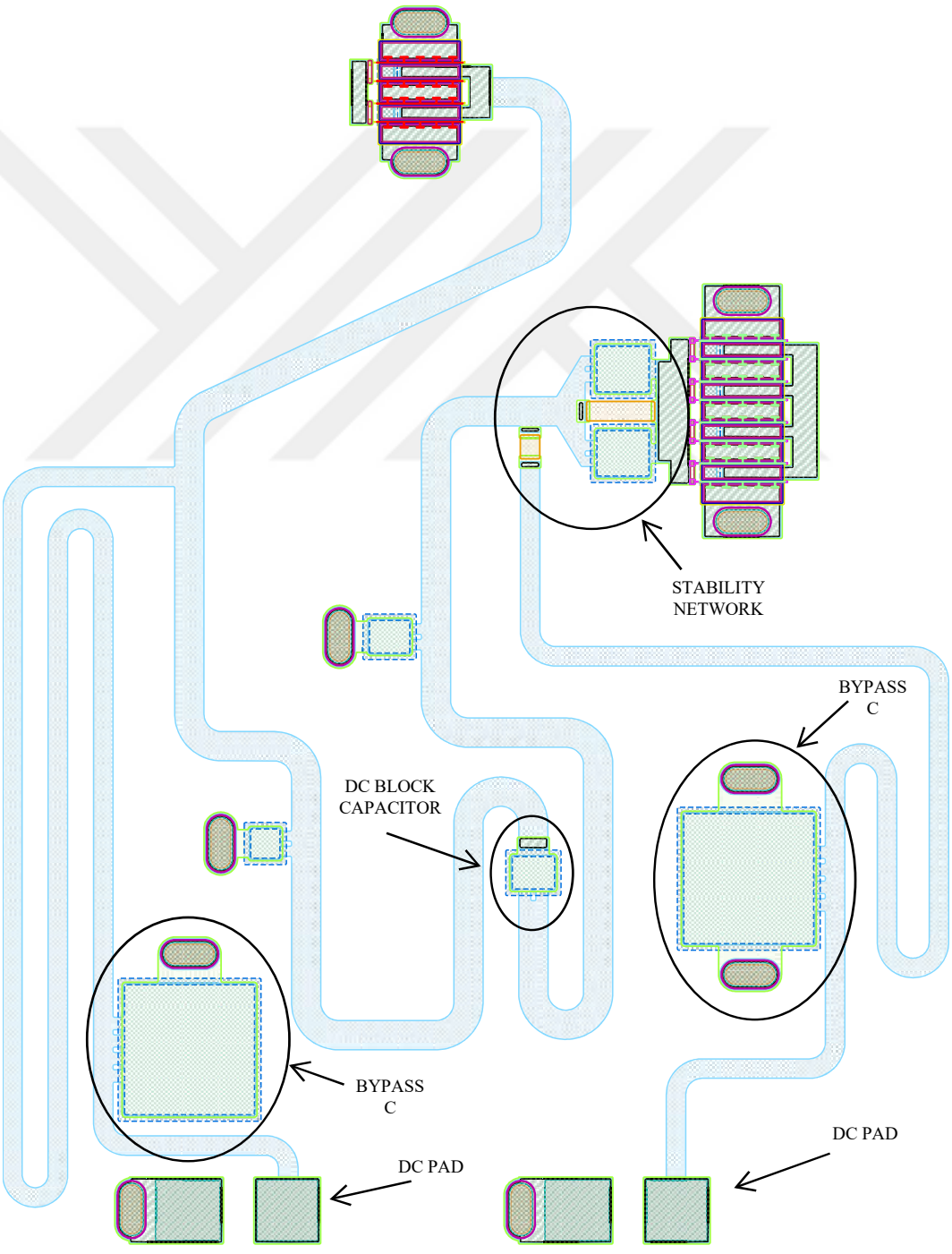


Figure 3.26: Layout of First Interstage Matching Network.

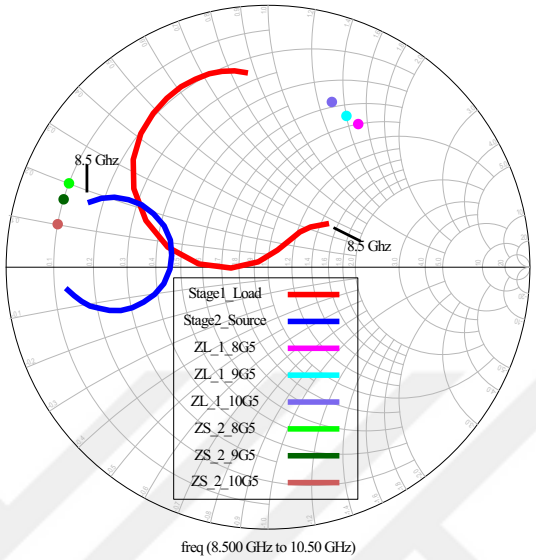


Figure 3.27: Impedances seen from gate of 8×125 µm HEMT in the 2nd stage and drain of 4×125 µm HEMT in the 1st HEMT stage.

The resulting impedances in Figure 3.26 scatter more on the Smith chart compared to previous networks, and the distance between target impedances is high. However, extra losses would be needed from the network to make the curve more dense on the smith-chart. This would result in a lower gain. Moreover, a mismatch is needed to get a flat gain. If the first stage can drive the second, the scattering will not be a problem. The loss coming from the network is around 1.2 dB, as can be seen in Figure 3.28.

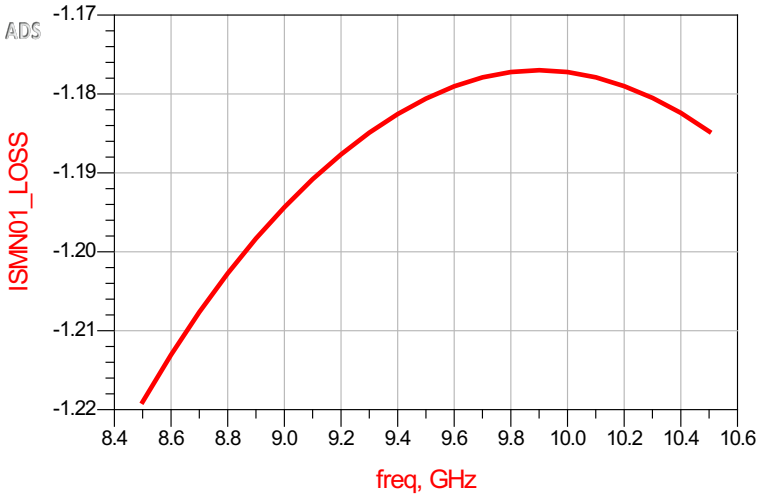


Figure 3.28: Loss at the First Interstage Matching Network (dB).

3.3.4 Input Matching Network

Input matching network (IMN) significantly affects the S_{11} result. The IMN should present 50 Ω to the source and selected impedances to the gate of the first stage in the frequency band. Since the remaining networks are already designed, we can focus on high input return loss while preserving flat gain. Figure 3.29 shows the general structure.

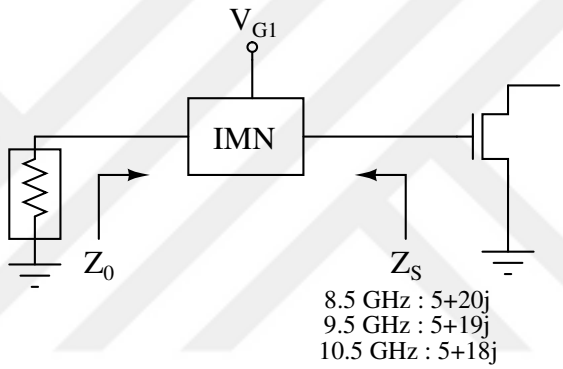


Figure 3.29: General Structure of Input Matching Network.

The IMN design has only one bias line for the gate of the 4x125 µm transistor. The bias line is combined with the stability network. The order of components is higher than the previous ones to get the desired S_{11} level with low ripple gain. The DC-Block capacitor is placed just before the input to reduce its effect to the matching as shown in Figure 3.30.

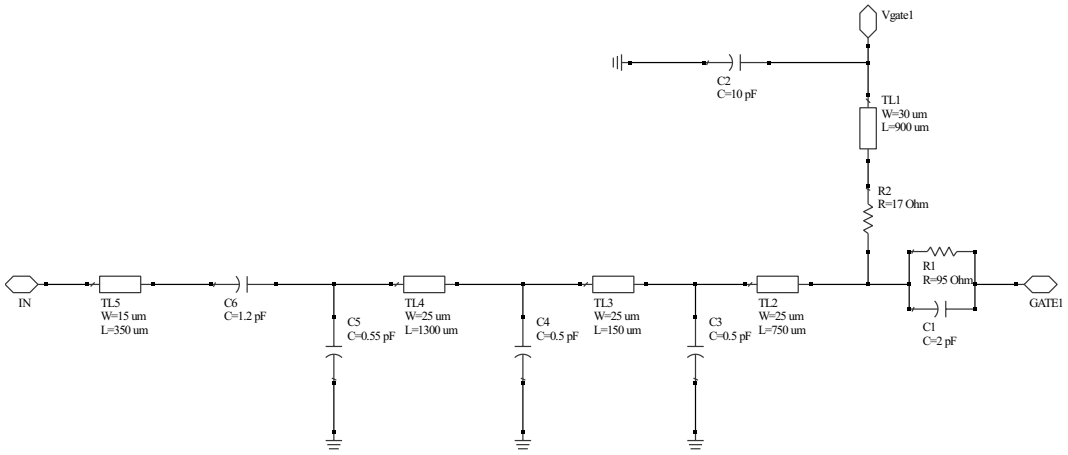


Figure 3.30: Schematic of Input Matching Network.

The layout in Figure 3.31 is designed to fit the remaining area and placed on the top of ISMN1. The final design is connected to an RF probe pad for on-wafer measurements.

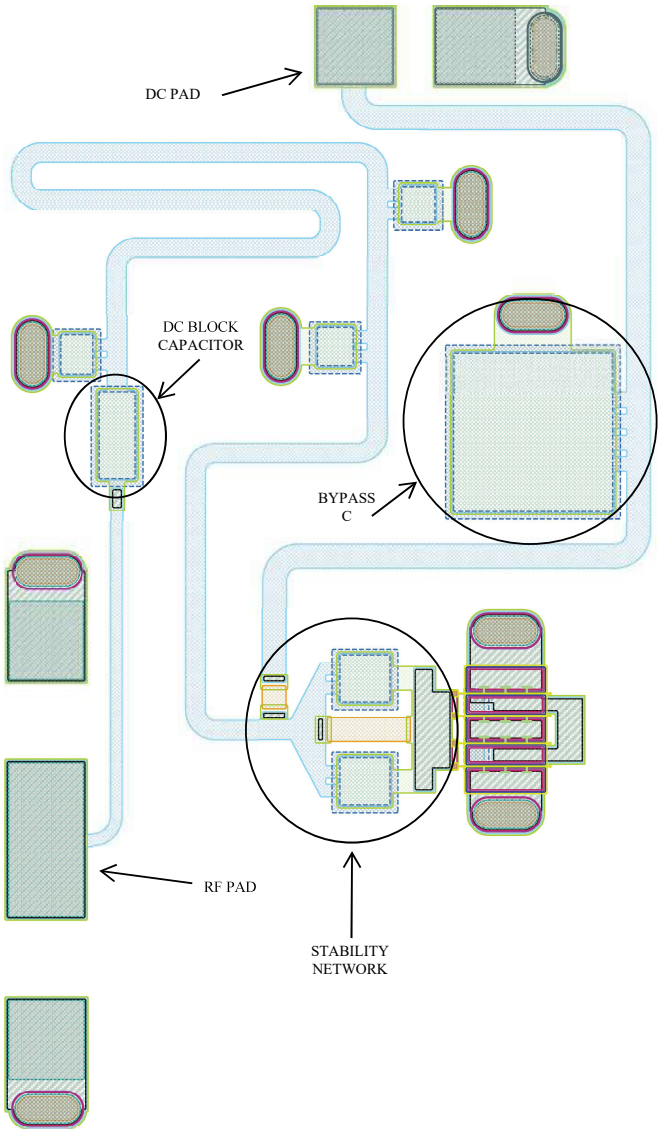


Figure 3.31: Layout of Input Matching Network.

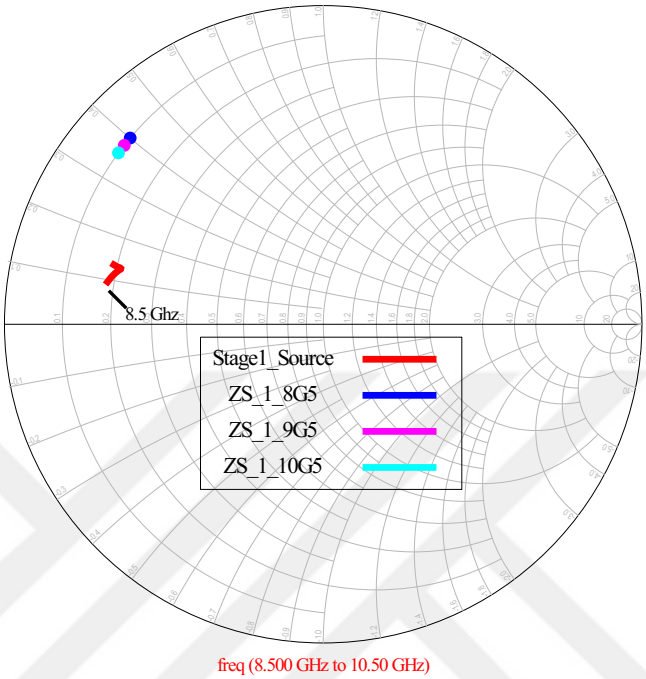


Figure 3.32: Impedance seen from gate of a 4×125 µm HEMT in the 1st stage.

The resulting impedance in Figure 3.32 is close enough to the desired points to get input return loss better than 10 dB in the measurements. The loss of IMN is around 2.5 dB. The loss is the highest among the networks. However, it is required to achieve the S_{11} target. The measurement results are discussed in Chapter 4.

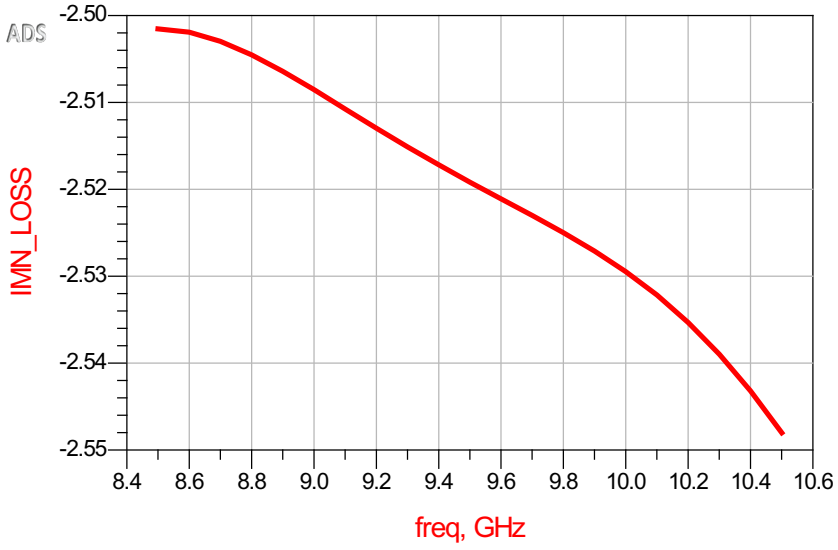


Figure 3.33: Loss at the Input Matching Network (dB).

3.4 Layout Optimization

The networks are connected after EM simulations, and DC bias pad locations are modified for 600 µm DC probe pitch. The total area is 3.8 x 2.7 mm^2 as planned. The corners of each shape are rounded, which is recommended by the foundry for the fabrication process. A STREET layer surrounds the design. The Street layer is patterned on the backside of the wafer for dicing after on-wafer measurements. Figure 3.34 shows the final design, which is ready for tape-out.

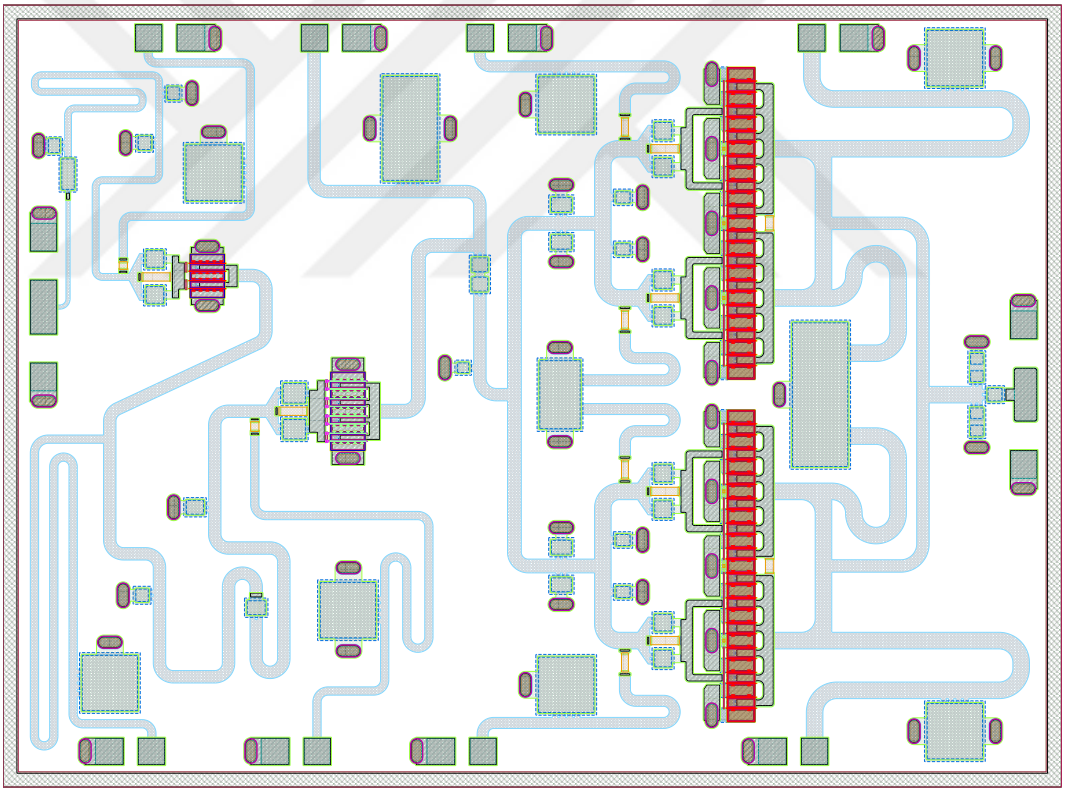


Figure 3.34: Layout of the MMIC.

Chapter 4

Simulation and Measurement Results

The MMIC is fabricated on 250 nm GaN on SiC process. The MMIC occupies a 3.8×2.7 mm^2 area. Its photograph is given in Figure 4.1.

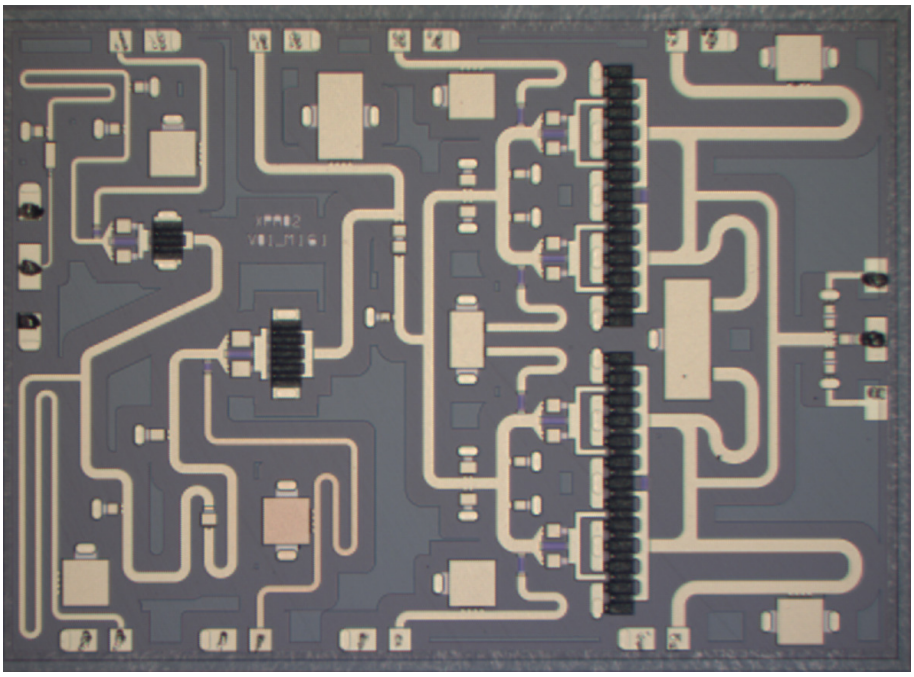


Figure 4.1: Microscopic photographs of fabricated three-Stage X-Band MMIC with 3.8×2.7 mm^2.

All measurements are performed on-wafer with base temperature fixed to 25°C. The transistors are biased with V_{DS} = 28 V, I_{DQ} = 630 mA. Small and large-signal measurements are conducted in pulsed condition with 10% duty cycle and 250 µs pulse period. The AMCAD 3200 PIV system generates the pulsed gate and drain bias signal. Keysight N5224B Power Network Analyzer (PNA) is used for measurements. IVCAD Measurement & Modeling Software used for the measurements.

4.1 Scattering Measurements

First, we executed small-signal measurements with −30 dBm available input power, and 50 Ohm input and output impedances were shown to the MMIC to compare design performance with the simulations. The measurement was conducted in the 7.5 – 12.5 GHz band. Figure 4.3 shows input and output return losses with small signal gain for simulations and measurements. All simulations are done in Keysight ADS.

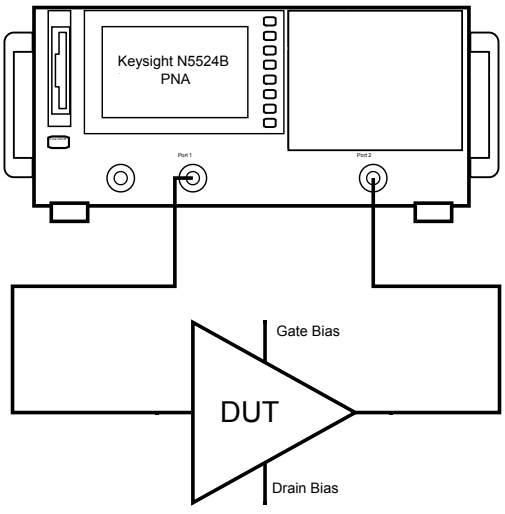


Figure 4.2: Scattering Measurements Setup.

The fabricated MMIC achieves a small signal gain of 38.1 dB to 42.9 dB in the 8.5 to 10.5 GHz band, resulting ±2.4 dB ripple as shown in Fig. 4.3. On

the other hand, simulation results achieved a gain of 38.3 dB to 40.9 dB with ±1.2 dB ripple. Input (IRL) and output (ORL) return losses are better than 11 dB and 12 dB in simulation, while the measurement results are better than 5 dB and 11 dB, respectively.

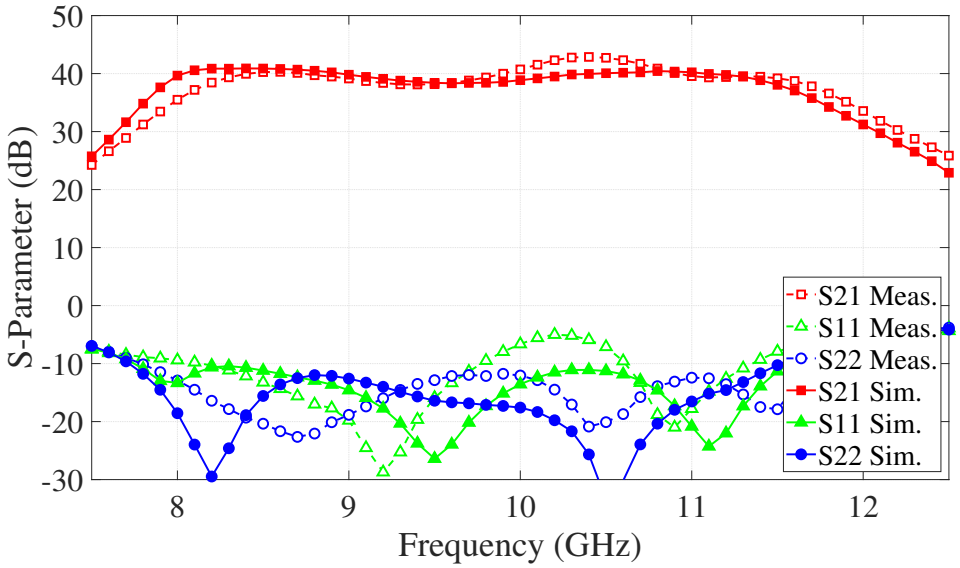


Figure 4.3: Small Signal results of simulation and measurement in pulsed condition with V_{DS} = 28 V, I_{DQ} = 630 mA, T_{base} = 25°C, Duty Cycle = 10%, and Pulse Period = 250 µs.

The measurement results are in sufficient agreement with the simulations. On the other hand, there is a 100 MHz band shift to higher frequencies and an increase in the ripple. The minimum input return loss decreases from 10 dB to 5 dB. The S-parameter comparison table between the simulation and measurements is given in Table 4.1.

Table 4.1: S-parameter results at the drain bias of 28 V 100 mA/mm.

Result	**S_{21} (dB)**			**S_{11} (dB)**			**S_{22} (dB)**		
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
Sim.	38.3	39.4	40.9	-26.4	-15.6	-11.1	-33.5	-17.0	-12.0
Meas.	38.1	40.0	42.9	-28.7	-13.8	-5.0	-22.6	-16.4	-11.8

4.2 Large Signal Pulsed Measurements

We conducted large signal characterization in the 8.5–10.5 GHz band with a 0.5 GHz step size. The available input power swept is from −15 dBm to 15 dBm. Each measurement's maximum input power differs since the stop conditions were gate-turn on with 1 mA/mm or 13 dB compression, whichever comes first. 50 Ohm input and output impedances are presented to the MMIC by impedance tuners. In addition to the setup in Figure 4.2, a driver amplifier is connected to the input port to get the desired available input power. The hybrid coupler at the input reads the available input power. The output coupler protects the output port from exceeding power by burning it. Figure 4.4 presents the load-pull measurement setup.

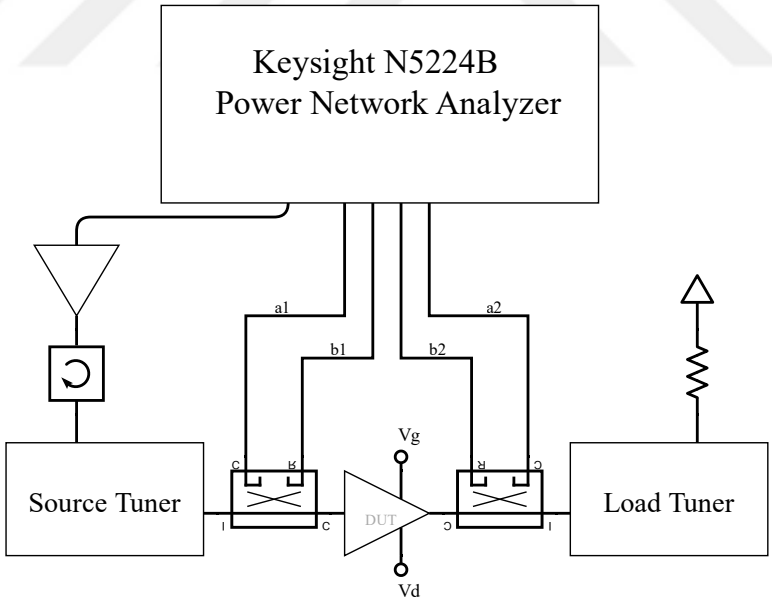
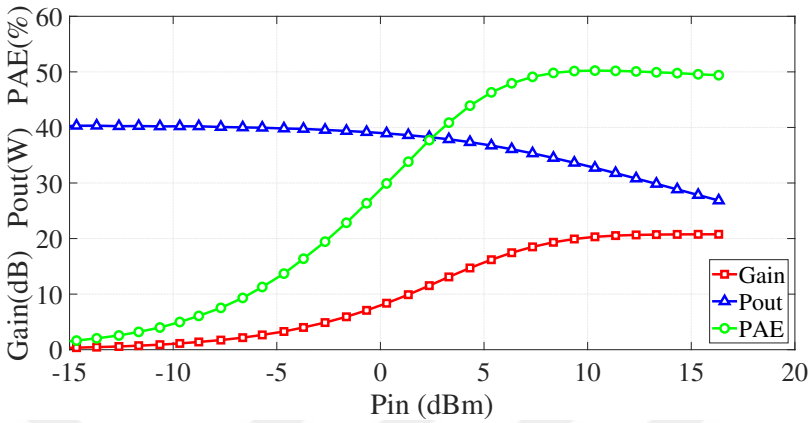
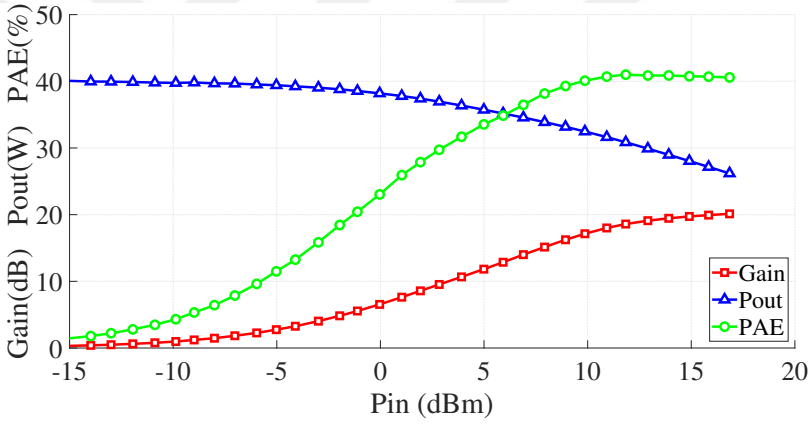


Figure 4.4: Large Signal Measurement Setup.

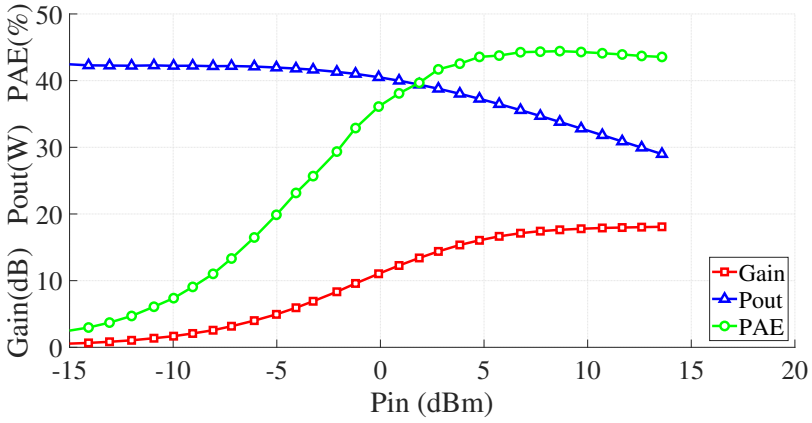
Figure 4.5 demonstrates the gain, output power, and efficiency vs. input power results at the band's start, middle, and end. Small-signal gains match with the scattering measurements. After 10 dBm of input power, efficiency exceeds 40% level, which was our aim. At 10 dB compression, the output power is around 20 W.



(a) 8.5 GHz



(b) 9.5 GHz



(c) 10.5 GHz

Figure 4.5: P_{in} vs gain, output power and PAE measurement results of the MMIC in pulsed condition with, V_{DS} = 28 V, I_{DQ} = 630 mA, T_{base} = 25 °C, Duty Cycle = 10%, and Pulse Period = 250 µs for different frequencies.

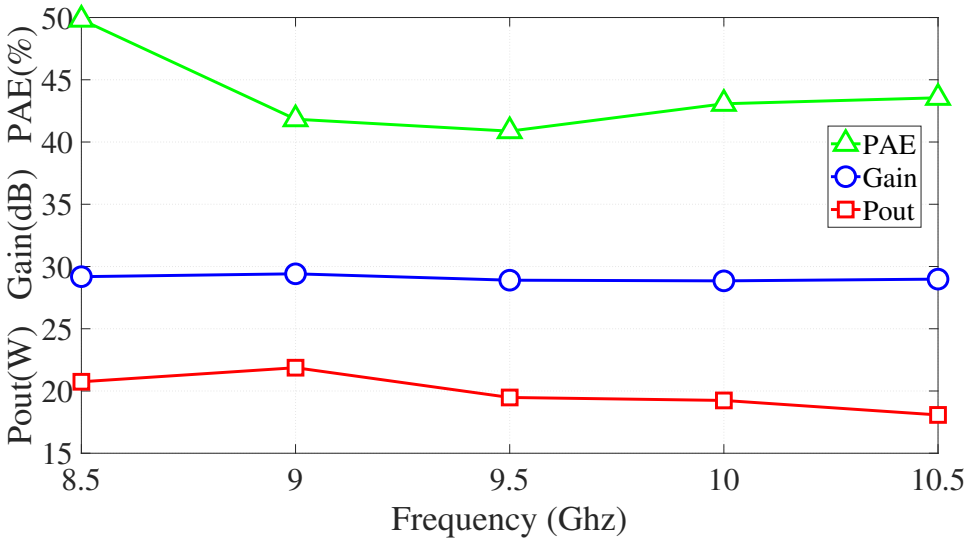


Figure 4.6: Frequency vs gain, output power and PAE measurement results of the MMIC over the band in pulsed condition with P_{in} = 14 dBm, V_{DS} = 28 V, I_{DQ} = 630 mA, T_{base} = 25 °C, Duty Cycle = 10%, and Pulse Period = 250 µs.

For 14 dBm fixed available input power, the MMIC is in saturation for the frequencies in the band. As shown in Figure 4.6, the amplifier achieves an output power of 42.5 dBm to 43.4 dBm and a power gain of 28.8 dB to 29.4 dB. The PAE is 43% on average and reaches the maximum value at 8.5 GHz with 50%. We cannot compare with simulation results since nonlinear ADS models are unavailable. However, we can say that the design achieves the aimed efficiency and output power levels, which shows that the matching networks present the impedance values chosen in Chapter 3.2 to the transistors. Table 4.2 summarizes the large-signal measurement results.

Table 4.2: Large Signal results in pulsed condition with P_{in} = 14 dBm, V_{DS} = 28 V, I_{DQ} = 630 mA, T_{base} = 25 °C, Duty Cycle = 10%, and Pulse Period = 250 µs.

Freq. (GHz)	**Output Power (dBm)**	**PAE (%)**	**Gain (dB)**
8.5	43.2	49.8	29.2
9.0	43.4	41.8	29.4
9.5	42.9	40.9	28.9
10.0	42.8	43.1	28.8
10.5	42.6	43.6	28.6

4.3 Comparison with Recent Works in the Literature

Table 4.3 compares the MMIC with the recent X-Band MMIC PAs developed with 250 nm GaN on SiC technology. Most of the recent works emphasize a two-stage design; hence, the small signal gain does not exceed 26 dB. The only three-stage design in the table achieves 36 dB, which was also designed with the NANOTAM process. This work has the highest gain among them, with 40 dB. Due to the mismatch in the input matching network, the minimum IRL is limited to 5 dB, while other works have greater than 5 dB. On the other hand, this MMIC has the best ORL.

The design has 21% fractional bandwidth, which puts it in a decent position among the others. It is not fair to compare the efficiency with the designs measured in CW conditions. However, this work achieves the best PAE with 43% for the ones measured in pulsed condition. The design occupies 10.26 mm^2 area. It is not wise to compare the sizes directly since HEMT's sizes and topologies differ in each design. Power density is a good figure of merit for comparing output power and size. Equation 4.1 defines the power density.

$$Power\ Density\ =\ \frac{Output\ Power}{Size}\ \ (W/mm^2) \tag{4.1}$$

The amplifier has a 1.95 W/mm^2 power density, which is the second best in the table. While other designs have a two stage topology, the MMIC achieves similar density levels with an additional driver stage. Overall, this work exhibits competitive results among the recent publications with high gain and efficiency.

Table 4.3: Comparison of three-Stage X-Band MMIC with 250 nm GaN-on-SiC process based on recent works.

Ref.	**[5]**	**[6]**	**[7]**	**[8]**	**[9]**	**[10]**	**This Work**
Topology	1:4	1:4	2:4	2:8	2:4	1:1:4	1:1:4
Drive Ratio	1:4	1:4	1:2.2	1:4	1:2	1:1.25:4	1:2:9.6
Freq. (GHz)	7.0–13.0	8.5–10.5	9.0–10.0	7.8–8.8	8.8–10.4	8.5–11.0	8.5–10.5
Gain (dB)	15	23	20	26	26	36	40
Min. IRL (dB)	6	7.5	5	10	-	16	5
Min. ORL (dB)	10	10	11	7.5	-	7	11
Pout (W)	10	16	14.9	22.5	14	15	20
PAE (%)	39	40	37	50	38	40	43
Duty Cycle	CW	10%	10%	CW	15%	6%	10%
Size (mm^2)	6.12	9.13	5.04	21.6	18	12.69	10.26
Power Density (W/mm^2)	1.64	1.95	2.96	1.04	0.78	1.18	1.95

Chapter 5

Conclusion

This thesis demonstrated an X-Band MMIC power amplifier design developed with 250 nm GaN on SiC process. The GaN and MMIC technology is reviewed with the works in the literature. The GaN on Sic technology offers great thermal properties and power density for high-power applications. First, we extracted the process parameters with DC, RF, and load-pull measurements using a 1 mm HEMT.

The transistor characterization was followed by MMIC design in the ADS design environment. First, topology and transistor sizes were selected. We used a three-stage 1:1:4 topology to get a gain over 35 dB. To get output power above 20 W, transistors with 4.8 mm overall periphery were selected. The driving ratio was 1:2:9.6. After selecting transistors; we determined the impedances for our matching networks according to the load-pull measurement. Each HEMT was stabilized according to the K-factor and Freitag Method while maintaining high gain. Then, matching networks are designed to achieve specifications.

The amplifier achieves a 40 dB small signal gain, 43% PAE, and 20 W output power on average in pulsed conditions. The chip occupies a 3.8×2.7 mm^2 area and has a power density of 1.95 W/mm^2.

As a future work, We plan to improve the input return loss using a lossy input

matching network in the next fabrication iteration. In the worst case, a 2.5 dB attenuator can be used at the input to improve the input return loss to 10 dB at the expense of 2.5 dB loss in gain. The frequency band can be improved to cover all of the X-Band frequency range, which is 8 to 12 GHz. This requires overall new matching network designs with new impedances.

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