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HYBRID OPTIMIZATION ALGORITHM BASED THD REDUCTION IN THREE PHASE MULTILEVEL INVERTER

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BY

MEHMET HALİL YABALAR

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Supervisor

Prof. Dr. Ergun ERÇELEBİ

by

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June 2024

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Mehmet Halil YABALAR

ABSTRACT

HYBRID OPTIMIZATION ALGORITHM BASED THD REDUCTION IN THREE PHASE MULTILEVEL INVERTER

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Ph.D. in Electrical and Electronics Engineering
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This study presents an innovative hybrid optimization approach that combines teaching-learning based optimization (TLBO) with the whale optimization algorithm (WOA) for selective harmonic elimination (SHE) technique in a modified reduced switch topology three phase 11-level multilevel inverter (MLI). This hybrid strategy effectively tackles the issues of harmonic reduction and total harmonic distortion (THD) on the line-to-line voltage, significantly improving the quality of the output power through the optimal determination of switching angles. The study leverages the TLBO and WOA to solve the non-linear set of equations associated with the SHE technique, aiming to overcome the limitations of classical methods prone to local optimal solutions and dependent on initial controlling parameters. By using MATLAB®/Simulink software environment, the performance of the hybrid TLBO with WOA method has been simulated, and this algorithm for lowering THD values is found to be 3.96% better compared to the other algorithms. The simulation results reveal that proposed hybrid approach becomes advantageous in terms of SHE and output voltage quality across various modulation indices. Experimental results verified that the proposed algorithm has been validated with a three-phase 11-level inverter application with a difference of approximately 1% compared to the simulation results.

Key Words: Teaching-learning based optimization (TLBO), whale optimization algorithm (WOA), selective harmonic elimination (SHE), multilevel inverter (MLI), total harmonic distortion (THD).

ÖZET

HİBRİT OPTİMİZASYON ALGORİTMASI TABANLI ÜÇ FAZLI ÇOK SEVİYELİ EVİRİCİLERDE THD AZALMASI

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Bu çalışma, öğretim-öğrenme tabanlı optimizasyon (ÖÖTO) ile balina optimizasyon algoritmasını (BOA) birleştiren yenilikçi hibrit bir optimizasyon yaklaşımını, modifiye edilmiş azaltılmış anahtar topolojisi üç fazlı 11-seviyeli evirici için seçici harmonik eliminasyon (SHE) tekniği ile sunmaktadır. Bu hibrit strateji, harmonik azaltma ve hatlar arası voltajdaki toplam harmonik distorsiyon (THD) sorunlarını etkili bir şekilde ele almakta, anahtarlama açılarının optimal belirlenmesi yoluyla çıkış gücünün kalitesini önemli ölçüde iyileştirmektedir. Çalışma, SHE tekniği ile ilişkili doğrusal olmayan denklem setini çözmek için ÖÖTO ve BOA'dan yararlanmakta, klasik yöntemlerin yerel optimum çözümlere eğilimli ve başlangıç kontrol parametrelerine bağlı sınırlamalarının üstesinden gelmeyi amaçlamaktadır. MATLAB®/Simulink yazılım ortamında, hibrit ÖÖTO ile BOA yönteminin performansı simüle edilmiş ve THD değerlerini düşürmeye yönelik bu algoritmanın diğer algoritmalara göre 3.96% daha iyi olduğu bulunmuştur. Simülasyon sonuçları, önerilen hibrit yaklaşımın çeşitli modülasyon indekslerinde SHE ve çıkış voltajı kalitesi açısından avantajlı hale geldiğini ortaya koymaktadır. Deneysel sonuçlar, önerilen algoritmanın üç fazlı 11 seviyeli bir evirici uygulamasıyla simülasyon sonuçlarına göre yaklaşık 1% farkla doğrulanmış olduğunu sağlamaktadır.

Anahtar Kelimeler: Öğretim-öğrenme tabanlı optimizasyon (ÖÖTO), balina optimizasyon algoritması (BOA), seçici harmonik eliminasyon (SHE), çok seviyeli evirici, toplam harmonik distorsiyon (THD).

"Dedicated to my family"

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LIST OF SYMBOLS

α	Alfa
β	Beta
Ω	Ohm
π	Pi
θ	Theta
C	Capacitor
L	Inductance
F	Fahrad
H	Henry
P	Active Power
Q	Reactive Power
V	Voltage
I	Current
W	Watt
N	Number of Level
m	Modulation index
$\mathbf{V_{DC}}$	DC Voltage
Hz	Hertz
$\mathbf{V_{in}}$	Input Voltage
$\mathbf{I_{in}}$	Input Current
$\mathbf{V_L}$	Line Voltage
$\mathbf{I_L}$	Line Current

LIST OFABBREVIATIONS

TLBO	Teaching Learning Based Optimization
WOA	Whale Optimization Algorithm
SHE	Selective Harmonic Elimination
MLI	Multilevel Inverter
MI	Modulation Index
EMI	Electromagnetic Interference
PV	Photovoltaics
HVDC	High Voltages Direct Current
FACTS	Flexible AC Transmission Systems
DC	Direct Current
AC	Alternative Current
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
NPC	Neutral Point Clamped
FC	Flying Capacitor
CHB	Cascaded H-Bridge
NSVC	Nearest Space Vector Control
NLC	Nearest-Level Control
CHBMLI	Cascaded H-Bridge Multilevel Inverter
SHEPWM	Selective Harmonic Elimination PWM
NM	Numerical Methods
AM	Algebraic Methods
EA	Evolutionary Algorithms
NR	Newton Raphson
mDOA	Modified Dingo Optimization Algorithm
BWOA	Black Window Optimization Algorithm
GWOA	Grey Wolf Optimization Algorithm

JSOA	Jumping Spider Optimization Algorithm
MGWOA	Modified Grey Wolf Optimization Algorithm
MAO	Mexican Axolotl Optimization
CGO	Chaos Game Optimization
COOT	Coot Bird Algorithm
GEO	Golden Eagle Optimizer
HHO	Harris Hawks Optimization
UPS	Uninterrupted Power Supply
PSO	Particle Swarm Optimization
PID	Proportional-Integral-Derivative
GA	Genetic Algorithm
PDM	Pulse Duration Modulation
NSPWM	Near State Pulse Width Modulation
IWOA	Improved Whale Optimization Algorithm
MWOA	Modified Whale Optimization Algorithm
SOP	Synchronous Optimal Pulse
SVC	Space Vector Control
FFT	Fast Fourier Transform
PCB	Printed Circuit Board
DSP	Digital Signal Processor
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor

CHAPTER 1
INTRODUCTION

1.1 Introduction

Power Electronics engineers have paid more attention to MLI in upcoming years. Generally MLI is used to minimize THD in output waveform without minimizing inverter power output. Major advantage of MLI compared to 2-level inverters are: reduced THD, minimization of dv/dt stresses, high power quality, reduced switching losses, low rating of power semiconductor switches, electromagnetic capacity [1], minimized switching frequency, minimization of EMI, voltage device analysis, high efficiency and interfacing renewable energy resources like PV to electric power grid [2]. The benefits improves practicality of MLI over industrial applications like High voltage direct current (HVDC), FACTS devices, micro grids, distributed generation. Generally MLI is categorized into 3 types: cascaded MLI, diode clamped MLI, flying capacitor MLI. Based on source values these inverters have been classified to asymmetric and symmetric configuration. DC voltage sources which are utilized in MLI consist of renewable energy sources, capacitors and batteries. Whole DC sources have been equal in symmetric topology. Whereas asymmetric topology includes DC sources with various values. With defined number of switches in asymmetric MLI produce larger number of steps in output voltage compared to symmetric one. MLI's stepwise output voltage has been composed from numerous DC voltage source. By enhancing count of output voltage steps in MLI which reduces THD of output voltage. These levels have been confined by factors like voltage clamping, circuit layout and voltage unbalance. There are numerous study discussed to enhance quality of output waveform and to reduce THD because of significance of THD. Switching strategy attracks performance of multilevel converters. Various modulation techniques has been used to enhance output voltage waveform quality. Most popular switching strategies are PWM (Pulse Width Modulation), Space Vector modulation, SPWM (sinusoidal PWM), SHE, reduction of THD and optimal reduction of THD.

Previously multilevel inverters has been introduced by Nabaei especially for three phase inverters with intention to reduce harmonics of switching frequency and amplitude. Nabaei separates DC source which have ultra-capacitors, fuel cell, solar cells which are used with MLI. These kind of DC sources have potential to develop suitable voltage waveforms. General controller of MLI are sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM), used to adjust waveform of output voltage and to eliminate unwanted harmonics. Previously, PWM wouldn't eliminate THD of multilevel inverters mainly for low order harmonics [3]. However, optimum of switching angles in removing particular lower order dominant harmonics could be handled with implementation of SHE. Newton Raphson algorithm utilize real time computation of switching depending on chosen harmonic elimination for MLI. This method needs suitable computation time with equal DC sources of multilevel inverter applications. Issue of equal DC sources in MLI could be resolved with support of hybrid algorithm. The hybridization of the Teaching-Learning-Based Optimization (TLBO) and the Whale Optimization Algorithm (WOA) is a novel conceptual contribution. This hybrid algorithm has been developed to effectively address the challenges encountered in reducing Total Harmonic Distortion (THD).

1.2 Background

The vast proliferation of renewable energy technologies in recent years has created a vital need for innovative power conversion systems capable of transforming the electrical output from these sources into forms suitable for various types of loads [4], [5]. Among the power electronic devices available for such conversions, inverters stand out due to their ability to convert direct current (DC) power into alternating current (AC) with desired electrical characteristics [6]. This phenomenon has significantly boosted the development of power electronic converter topology, particularly the MLIs since their discovery in 1975 [7]. Multilevel inverters (MLIs), specific type of inverters, have been at the forefront of technological advancement thanks to their capacity to generate a staircase output waveform synthesized at different voltage levels [8]. This output is mainly controlled by the accurate angle switching of the MLI power switching devices [9]. Known for their superior electromagnetic compatibility, high power quality, low switching losses, and reduced total harmonic distortion, so MLIs are commonly used use in industrial drivers,

compensators, medium and high voltage inverters, as well as interfaces to renewable energy systems [8], [9]. One distinct advantage of MLIs is the use of separate DC sources, which proves highly beneficial for applications in fuel cells and photovoltaic arrays [7]. Further categorization of MLIs yields three primary configurations: cascaded H-bridge, diode clamped, and capacitor clamped inverters. Among these, cascaded H-bridge inverters are noted for their structure of series connected H-bridge cells, where the sum of each cell's voltage is utilized to generate the desired output waveform [10], [11].

In recent years, multilevel converters have garnered significant attention, leading to the introduction of new topologies with various control algorithms[7]. Figure 1.1 illustrates the three fundamental topologies of MLIs. A primary drawback of the neutral point clamped (NPC) topology is the unequal voltage distribution between series-connected capacitors, which results in an imbalance in the dc-link capacitor and requires a large number of clamping diodes for higher voltage levels. In the flying capacitor (FC) MLI and stacked MLI [12], [13], flying capacitors serve as clamping devices. Compared to NPC converters, FC-MLI topologies offer several advantages, such as redundant phase leg states and transformerless operation, which help distribute switching stress uniformly across semiconductor switches [14]. However, these converters need a substantial number of storage capacitors for numerous voltage steps.

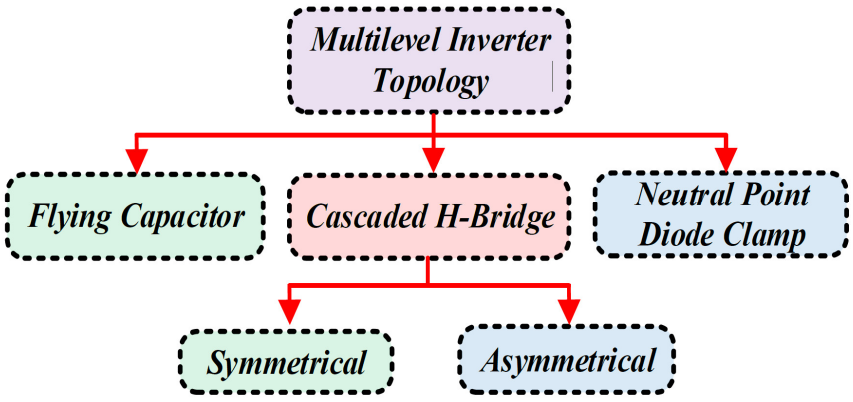

Figure 1.1 Classification of multilevel inverter topology [15].

Among conventional topologies, the cascaded H-bridge (CHB) topology is the most widely used due to its simplicity, modular structure, and reduced component

requirements. The CHB-MLI produces a staircase sinusoidal AC output voltage because of the separate DC sources it employs. To enhance the performance and quality of the output power of MLIs, various controlling techniques are used. The operation of MLIs, based on control and modulation schemes, is divided into two categories: (a) high switching frequency modulation and (b) low or fundamental switching frequency modulation. Operating the inverter at a high switching frequency lead to significant power loss in the switches [16]. Therefore, the fundamental switching frequency scheme is preferred for high power utilities to minimize switching-associated power loss. Figure 1.2 categorizes fundamental switching frequency modulation strategies.

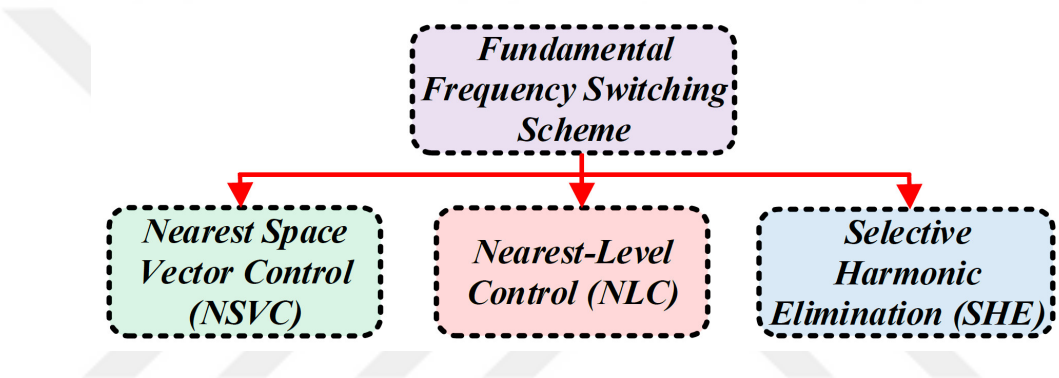

Figure 1.2 Classification of fundamental switching frequency techniques [17].

Despite the advancements in MLI design and structure, a continuous effort is in progress to reduce the harmonic content of MLIs [18]. Harmonic reduction, an essential aspect of an MLI's operation, largely depends on the modulation strategy chosen to control the inverter [19]. On the other hand, SHE [20]-[22] is a pulsed width modulation (PWM) control strategy aimed at suppressing low-order harmonics by determining the angles to control the switching sequence of the MLI power semiconductor devices [23], [24]. However, the search for an efficient and effective algorithm to solve every optimization problem in engineering and research fields always remains as a complex endeavour [25]. Among the variants of MLI, the Cascaded H-Bridge Multilevel Inverter (CHBMLI) stands out for its modular and simple structure [6]. The number of levels in CHBMLI is defined by the expression (2s+1) where s represents the number of single-phase full-bridge inverters controlled with the use of either high or low-frequency PWM techniques [10]. However, the use of high frequency switching techniques in CHBMLI can result in power losses,

attributed to the numerous switching devices involved [23], [24]. To mitigate this issue, the Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) method, a low-frequency modulation strategy has been used to eliminate undesired lower harmonics effectively [19]. Despite the growing prominence of SHEPWM, solving the transcendental equations required by these methods become a daunting task due to their complexities [25], [26]. This necessitates the development of fast and efficient algorithms capable of providing solutions [27]. Current methods used for solving the SHEPWM problem can be categorized into three main types: numerical methods (NMs), algebraic methods (AMs), and evolutionary algorithms (EAs) or bio-inspired methods [28], [29].

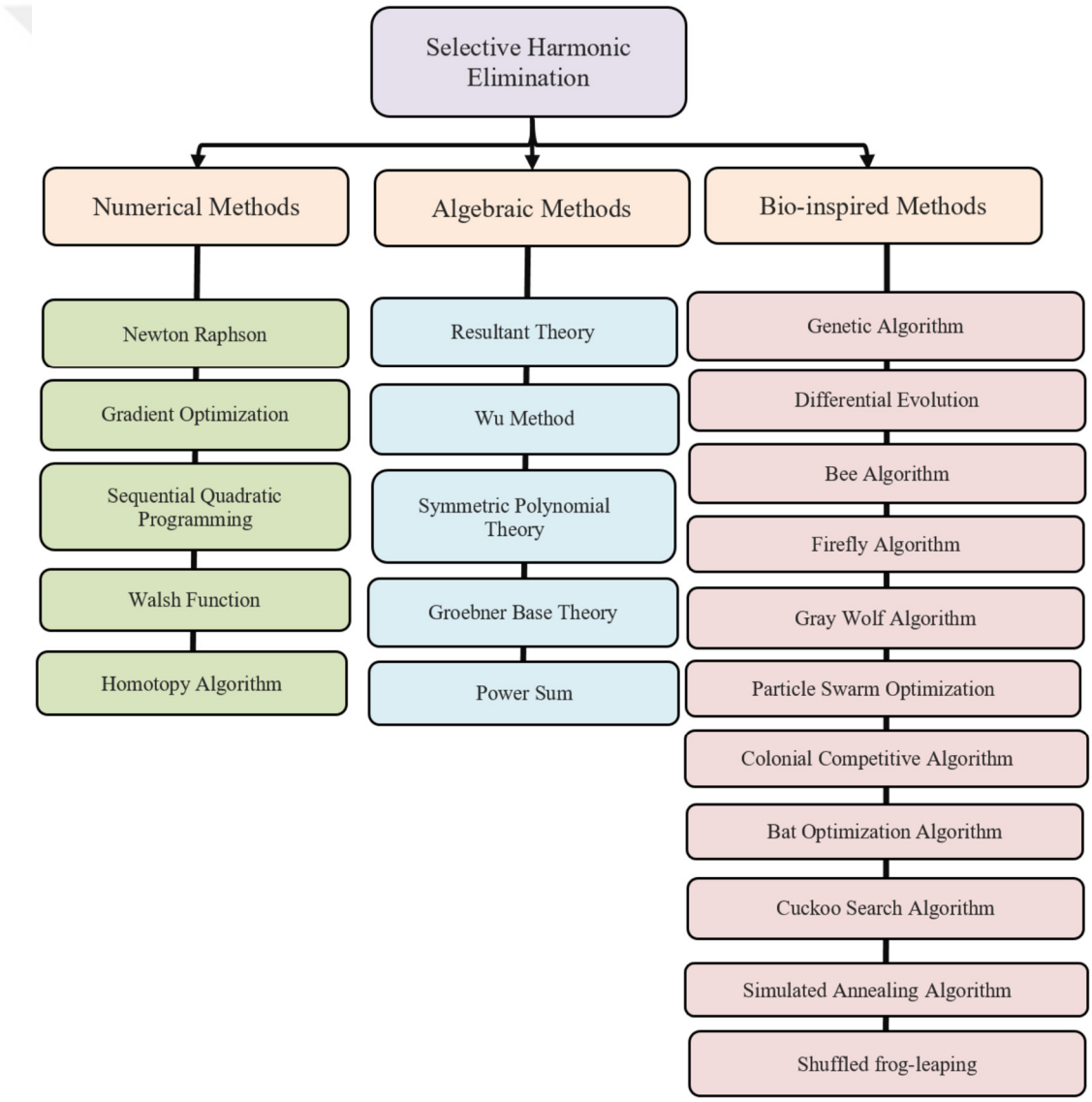

Figure 1.3 SHEPWM techniques with different methods [30].

In NMs, the Newton Raphson (NR) technique is utilized for solving SHE equations, offering precise and promising solutions [31]. However, these require an initial guess and may fall into local optima, risking sub-optimal outcomes.

AMs like the method of resultant theory has been discussed for optimized switching angles [32], not requiring initial guesses unlike numerical methods. However, their increased complexity and computational needs at higher inverter levels limit their use in advanced harmonic elimination.

The search for optimization solutions has led to the development of numerous Eas or bio-inspired methods [33]. However, despite their benefits, most of them fail in ensuring a balance between exploration and exploitation, which is primarily vital for effective convergence of optimization [34]. Consequently, the need for algorithms that provide a global solution rather than focusing on one specific region has become increasingly prominent [35].

Considering the challenges posed by the non-linear equations associated with the SHEPWM formulation, a variety of iterative, stochastics, and metaheuristics methods have been utilized [36]-[41]. In the recent algorithms including the Modified Dingo Optimization Algorithm (mDOA) [38], Black Window Optimization Algorithm (BWOA) [42], Grey Wolf Optimization Algorithm (GWOA) [38], Jumping Spider Optimization Algorithm (JSOA) [28], Modified Grey Wolf Optimization Algorithm (MGWOA) [43], Mexican Axolotl Optimization (MAO) [44], Chaos Game Optimization (CGO) [45], Coot Bird Algorithm (COOT) [46], Golden Eagle Optimizer (GEO) [47], and Harris Hawks Optimization (HHO) [48] have gained significant favour due to their proficiency in finding local optima and circumventing stagnation points [17], [49]-[53]. Despite the success of individual metaheuristics methods like the Teaching-Learning Based Optimization (TLBO), Whale Optimization Algorithm (WOA), and others, none of them are free of limitations and constraints [54]. For instance, these methods might provide optimal results for one specific application while failing to find the global optimum in other applications [55].

While WOA excels in exploration, it may suffer from excessive exploration and insufficient exploitation, leading to suboptimal results in certain scenarios. To address

this limitation, it has been combined the strengths of TLBO and WOA to create a hybrid optimization algorithm that capitalizes on their complementary characteristics. In this context, the necessity for a hybrid approach becomes inevitable, which integrates different algorithms to harness their respective strengths while reducing their limitations [56].

Thus, this study introduces a hybrid optimization methodology incorporating the TLBO and the WOA for SHE in a three-phase 11-level MLI with modified reduced switch topology [57]. This hybrid method has been implemented in MATLAB®/Simulink environment and applied to experimental prototype for seeking to offer a versatile and efficient solution to the challenge of harmonic minimization in MLIs [58]. The primary goal of this study is to improve the output power quality on the line-to line voltage of the MLI by optimally determining the switching angles and reducing lower-order harmonics, thus enhancing the efficiency of renewable energy systems [59].

1.3 Problem Identification

- The multilevel inverters have been used to decrease the harmonic distortion in the output waveform without decreasing the inverter power output.
- It has been calculated the switching angles in term of time for each level.
- For each level (V_{dc}, $2V_{dc}$, $3V_{dc}$, $4V_{dc}$, $5V_{dc}$) contains the θ1, θ2, θ3, θ4, θ5.
- The THD depends on the switching angle, by manual calculation of switching angle is not effective and THD will not be reduced.
- Implementing the optimization technique to adjust the switching angle in order to minimize the total harmonic distortion (THD).

1.4 Contributions of the Thesis

- Auxiliary switch MLI minimize number of switches compared to cascaded MLI and also gives better result than cascaded MLI.
- Hybrid TLBO-WOA optimization algorithm with auxiliary switch MLI works efficiently in a way to resolve optimization issues.

1.5 Objective

- To minimize THD value hybrid TLBO-WOA optimization algorithm is used.
- To reduce number of switches, auxiliary switch MLI is used instead of cascaded MLI.
- PWM is designed without triangular wave with use of reference magnitude PWM technique.

1.6 Thesis Methodology

The methodology used is as follows:

- Offline calculation of optimal switching angles.
- Develop 11-level modified reduced switch three phase MLI circuit using MATLAB®/Simulink.
- Develop SPWM circuit for generating all gate signals of three phase MLI using offline calculation parameters.
- Simulation model validation and testing.
- Implementation of hardware design of 11-level three phase MLI.
- Programming Texas Instruments®-TMDS-DOCK-28335 digital signal processor directly from MATLAB®/Simulink via C2000 feature for PWM gate signals as hardware.
- Observe the circuit behaviour under dynamic load test.
- Obtain results and compare thre results with other algorithm methods.

1.7 Organization of the Thesis

Chapter 1: mentions the generic introduction, background, problem identification, contribution of the thesis, objective, and thesis methodology.

Chapter 2: presents the previous studies concerning thesis work.

Chapter 3: represents the design of proposed system which are detailed reduced switch topology, selective harmonic elimination, analysis of power loss, and hybrid optimization algorithm for this thesis.

Chapter 4: analyzes simulations and results.

Chapter 5: contains hardware implementation and experimental results.

Chapter 6: compares of the results with other methods.

Chapter 7: concludes the thesis work.

CHAPTER 2
LITERATURE REVIEW

2.1 Related Work In The Literature

In this study, [60] Proposed a BDCLCRV MLI (Boost DC-Link based Reversing Voltage Multilevel Inverter) for applications of UPS (Uninterrupted Power Supply). Comparative analysis of the proposed system has been made with the traditional methods. The results have shown that the proposed system has used only limited switches and is more suitable for power converters utilised in UPS. Thus the proposed system has been found to show better results in terms of efficiency, reliability, cost reduction, performance and size of the inverter and requires only few resources to lower the THD (Total Harmonic Distortion) operation. In addition, [61] utilised a tuning algorithm called PSO-PID for Micro-grid system with respect to 15-level smart inverter topology. Simulation has been carried out to determine the efficiency of the system. The results obtained via simulation has been analysed and it has been found that the proposed system has been more appropriate for micro-grid system thereby obtaining a good power quality and carefully managing the co-energy. Moreover, [62] employed a modified PSO (Particle Swarm Optimisation) algorithm in the proposed 6S-7L MLI (Six Switch-Seven Level Multilevel Inverter) for eliminating the selective harmonics. Analysis has been performed by comparing the proposed algorithm with two frequently utilised PSO variants. The analytical results have shown that the modified PSO algorithm is more appropriate for the proposed system. Simulation has been performed to assess the performance of the proposed system. In the near future, the proposed topology's single-phase and three-phase design can be prolonged to various levels for several applications. Here [63] demonstrated a modified PWM (Pulse Width Modulation) for MLI optimization on the basis of Differential Evolution (DE) algorithm for THD reduction. Best angle shift, frequency and amplitude have been exhibited via the optimization process. Simulation has been performed through the use of resistive load and single-phase NPC (Neutral Point Clamped) MLI. Results have shown that the proposed system performs better in THD reduction.

Consequently, [64] suggested an optimized GA (Genetic Algorithm) method for THD minimization with respect to cascaded H-bridge MLI. A five-level inverter has been simulated in MATLAB® (Matrix Laboratory) and comparison of THD has been performed between optimization and step modulation method. Thus through the proposed system, THD reduction has been achieved. Similarly [65], [66] utilized PDM (Pulse-Duration Modulation) for modelling asymmetric cascaded MLI with minimum switches. Simulation has been performed to evaluate the proposed system's performance. Results have showed that the circuit complexity and overall cost has been reduced effectively through the proposed system. Minimum THD has also been achieved through the proposed technique. This study [67], [68] Proposed a PSO method to obtain switching angle optimisation and to mitigate the non-triplen harmonics effect from H-bridge Cascaded MLI. Simulation has been implemented to evaluate the performance of the proposed method. The obtained results have shown that the proposed technique provides better results than the existing techniques by producing less THD. Despite that more research has to be conducted regarding the proposed system for THD reduction and to progress the quality of output voltage of a MLI. In the same way [69] aimed for THD reduction in a MLI through the use of enhanced PWM method. Simulation has been made to determine the productivity of the proposed system. The results showed that harmonics have been reduced efficiently along with less arithmetic computation via the use of the proposed technique. Another method called utilized pattern search has been utilized for cascaded H-bridge inverter to lower THD. Switching angles has also been calculated to achieve minimum THD. Simulation has been performed for various levels of H-bridge MLI via the use of MATLAB®. Analysis has been carried for motor load, resistive-inductive load and THD of current and voltage for resistive load. Thus effective results have been obtained from the proposed method. Thus THD has been reduced through the pattern search algorithm [70]. Additionally, [71], [72] examined the structure and functioning of asymmetrical and symmetrical MLI with minimum number of switching components. Simulation has been undertaken to assess the performance of the system. The results showed that the semiconductor losses has been reduced and THD has been minimised. Thus through the use of proposed system, the voltage level obtained as output can be maintained even with minimum switching devices. Similarly [73] developed an optimized switching angle and DC source magnitude with PSO algorithm for THD minimization of MLI. The proposed system has been analysed.

Simulation has been carried out with a seven-level inverter to validate the proposed method's efficiency. The proposed system has also been compared with other traditional methods. Results obtained from comparative analysis has showed that the proposed system outperformed other traditional methods in THD minimization.

Furthermore surveyed various MLIs with respect to harmonic optimization: various optimization methods discussed in this paper includes PSO, biography based algorithm, fuzzy logic controller and GA (Genetic algorithm). Thus a comparative analysis of various algorithms have been made [74]. Furthermore proposed a MLI topology for grid integration of renewable energy. Comparative analysis has been made by comparing the proposed and traditional methods. The comparative results have showed that the proposed system minimizes the power switches and related gate driver circuits [75]. Likewise [76] developed a Z source cascaded MLI for harmonic reduction in the output voltage. Simulation was undertaken with various PWM methods to determine the productivity of the proposed method. Thus the results showed that the proposed system had better percentage in THD reduction. Moreover [77] suggested NSPWM (Near State PWM) for executing in dual-inverter fed in order to minimise THD. Experiment has been conducted and simulation has been undertaken. The results has showed that efficient reduction of THD has been achieved through the proposed method. Another method called Sinusoidal tracking algorithm has been employed with an improved H-bridge MLI to achieve minimum THD, switching losses and conduction. The proposed system was simulated in MATLAB and efficient results were obtained through the proposed algorithm [78].

In this study, [79] introduced solution to eliminate THD in MLI with help of (IWOA) improved WOA. IWOA is one of nature inspired optimization algorithm. It utilize new diffusion process with use of random walk method and additionally use a ranking system to examine optimum solution to reduce THD. Moreover, reduction of THD is done through 9 different metaheuristic algorithms for comparative analysis and investigation. Chosen algorithm with IWOA was tested on single phase five and seven level cascade H-Bridge MLI for different performance parameter like speed of convergence, computational efficiency and consistency. Result illustrated that proposed algorithm excels 9 algorithm and also effective method for THD reduction for modulation index (MI) in 0 to 1 range.

This research focused on [80] minimization of THD in multilevel inverter is tedious optimization issue. To overcome this issue, this study deals with THD elimination in cascaded MLI for equal DC supply with use of new WOA. The main intention of this study was to determine good combination of switching angles to reduce lower order harmonics and also minimize THD. Proposed WOA was used with 11 level cascaded H-bridge MLI. Results express that WOA provides best result compared to other technique. This study introduce modified WOA (MWOA) for elimination of harmonic in 3 phase 11-level hybrid cascaded MLI. Proposed MWO enhances rate convergence rate compared to traditional WOA. This is attained by enhancing exploration features of traditional WOA. SHE and PWM was used over MWOA to generate optimal switching angles of MLI in a way to remove lower-order harmonics like thirteenth, eleventh, sixth and fifth from output voltage [81]. In proposed work, capacitor voltage was balanced even though at higher modulation indices with use of existing switching states of MLI. This proposed work suits low switching frequency. Experiments was conducted on 1.5kw prototype and result express that proposed MWOA was most accurate and efficient than other existing algorithm [82].

Further, introduced novel single phase MLI with WOA dependent switching method. Proposed MLI needs only minimum number of power semiconductor devices when compared with significant MLI. Proposed work excels current optimization methods in terms of MLI performance, computational overheads and rate of convergence. Simulation was performed to evaluate performance of proposed work and result proved its efficiency. THD is most significant factor to analyse harmonic contents of waveforms. This research focus on minimization of THD with suitable switching scheme. Line voltage reduction of THD is one of significant need from load. TLBO algorithm was utilized to acquire best switching angles in a way to minimize line voltage THD. Results illustrate that TLBO proved in efficiency in minimization of line voltage THD compared to other traditional techniques [83]. Introduced effective switching scheme to reduce line voltage THD value of MLI. THD reduction was switching scheme utilized in applications like electrical drives, AC transmission system, etc. with use of THD reduction DC link values were set to pre-define values in a way to optimize THD. This research introduced TLBO to resolve optimization issues. Here line voltage THD was reduced and compared with existing research with

Genetic algorithm (GA). Comparison result proved that TLBO was more efficient than GA in resolving optimization issues [84].

This study [85] introduced optimization technique for THD minimization in cascade MLI with use of TLBO. Main intention of using SHE was to remove low order harmonics by resolving non-linear equation and reaches optimal solution, while fundamental component was satisfied. Here, in one side optimal DC source was investigated to achieve goal of SHE and on other hand other optimization techniques was considered for comparison. TLBO was introduced to give good result for SHE compared to GA, harmony search, artificial bee colony. For comparison 15, 9 and 5 level MLI was selected and for optimization MATLAB was used. Result proved that TLBO was more efficient that other optimization algorithms. This research [86] studied minimization of THD in output voltage of MLI. Correct choosing of switching angles minimize THD in MLI. Here TLBO was utilized to predict optimum switching angle in a way to develop preferred voltage value with least possible THD. Experiments was performed on various 7-level MLI and compared with GA. Results proved benefits of this proposed work. This research [87] concentrates on level shifted and phase shifted PWM depending on cascaded MLI. It provide numerous benefits compared to traditional three phase bridge MLI in terms of high efficiency, smaller rating, low electromagnetic interference and minimized dt/dv stress. Here proposed technique was modelled with 13 level cascaded MLI with use of level and phase shifted PWM in a way to provide minimum THD. Results proved possibility of proposed work.

In this work [88], non-linear SHE in three phase cascaded MLI with unequal DC sources were solved by using TLBO algorithm to choose optimum switching angle to reduce THD. Experiments was performed on various values of MI to receive value of THD. The obtained THD value was least compared to other optimization methods. For the THD minimization in cascaded multilevel inverter (CMLI), the PSO algorithm application is examined. For the 5 and 7 level inverter the simulation has performed in this study in which PSO is utilized to eliminate harmonics. Nearer to numerical method, the results is obtained and also PSO converges rapidly. Related with 5 level, THD is minimized for the 7 level inverter. The fifth and seventh harmonics magnitude are smaller among the modulation indexes in 0.7 – 0.8 ranges. By switching angle

increased with increasing CMLI level the proposed study is extended. More number of harmonics have been minimized when switching angles are increased [89]. The THD and low-order selective harmonics reduced by the multilevel voltage source invertors and Salp optimization algorithm. The THD percentage magnitudes and selective harmonics are illustrated based on the proposed simulation outcomes. The lower THD value and rapid convergence rate are evaluated in this study [90]. The invertors with realistic, unequal and justifiable DC sources have been considered in this study. Using evolutionary algorithm the switching angles and DC voltages has to utilize to reduce the THD level. For the optimization issues, the LSHADE-EpSin is developed which is the Differential Evolution (DE) advanced form. In successive generations, this proposed technique used to control evolutionary algorithm parameters and also to enhance the additional adaptation method. For inverters at higher level this proposed algorithm is executed [91]. By output voltage level increasing, the THD is reduced and better voltage waveform is obtained. The switching angles are found by the PSO and GA in order to obtain the minimum THD. The various modulation indices of 27 level inverter have been utilized in this study. Less THD is observed in this study [92].

CHAPTER 3
DESIGN OF PROPOSED SYSTEM

3.1 Introduction

This section provides a comprehensive examination and comparison of the modified reduced switch count topology with other reduced switch topology and the traditional cascaded H-Bridge. Also, this section outlines the selective harmonic reduction method used for the suggested topology. Additionally, this section provides an analysis of power loss and an overview of the hybrid optimization algorithm. Figure 3.1 shows the working principle of proposed design 11-level three phase MLI.

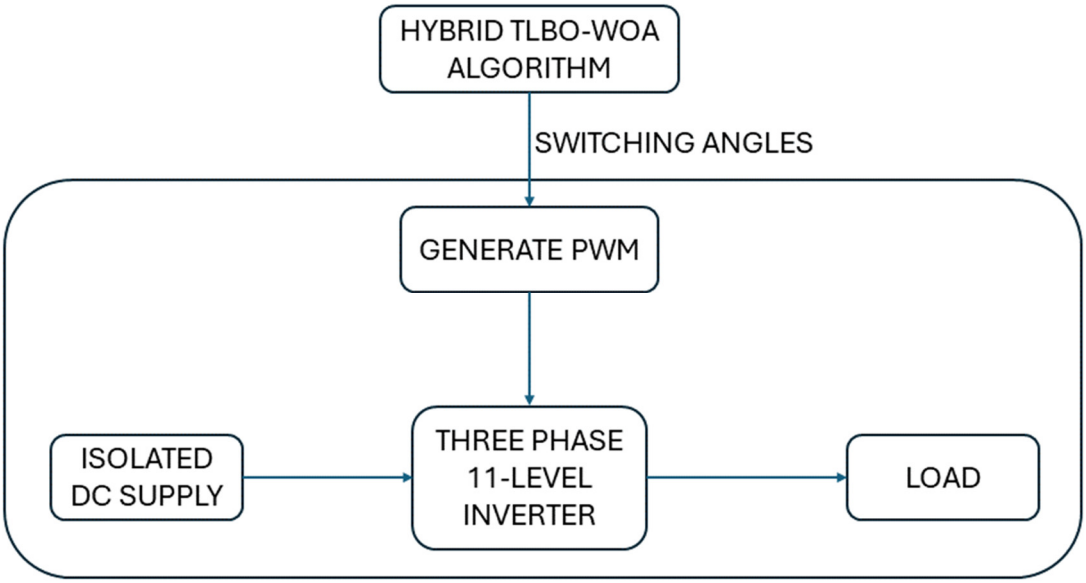

Figure 3.1 Working principle of proposed design system.

3.2 Reduced Switch Topology

The number of switches needed in a traditional single-phase cascaded multilevel inverter is determined by the following expression (3.1):

$$k = 2(l - 1) \tag{3.1}$$

where "k" represents the required number of switches and "l" corresponds to the number of levels in the multilevel inverter. The reduced switch topology calculates the count of switches in the single-phase multilevel inverter in accordance with (3.2):

$$k = l + 3 \tag{3.2}$$

Figure 3.2 presents the design of an 11-level MLI with a reduced switch. This inverter is linked to a cascaded basic unit that inverts the waveform alternately to achieve positive, zero, negative levels. Notably, the design eliminates the requisite for additional clamping diodes or voltage balancing capacitors by utilizing isolated DC power supplies. Clamping diodes and capacitors help in balancing the voltage across each level of the inverter unless isolated DC power supplies used.

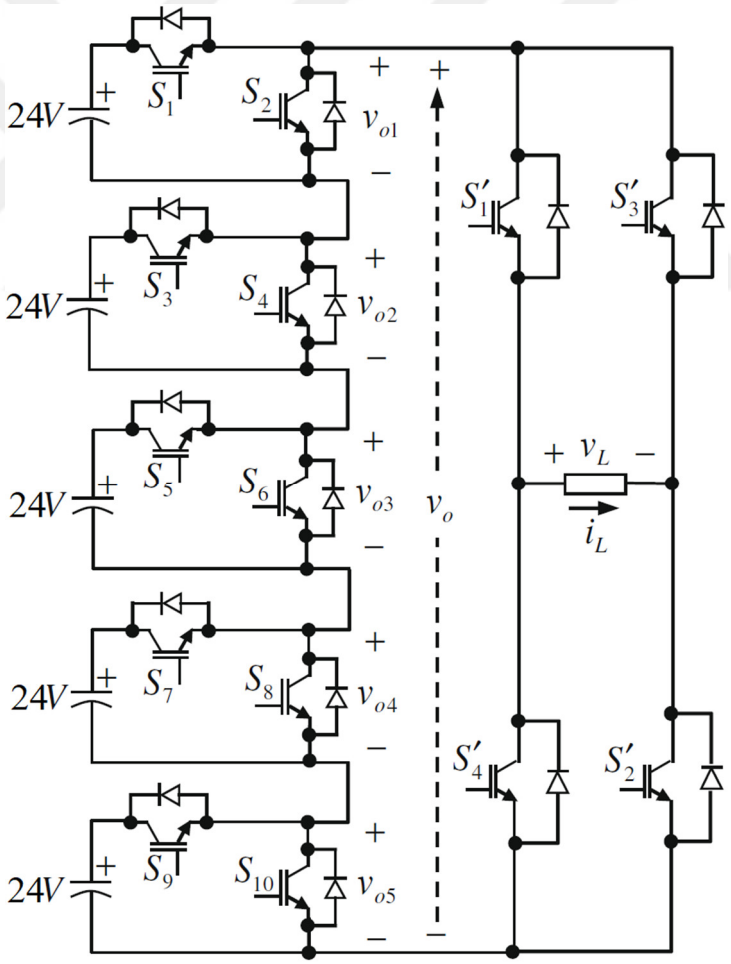

Figure 3.2 Reduced switch 11-level MLI topology.

Figure 3.3 shows the design of an 11-level MLI with a modified reduced switch. This design has two switches less. The number of switches needed in a modified reduced switch topology is determined by the following expression (3.3):

$$k = l + 1 \tag{3.3}$$

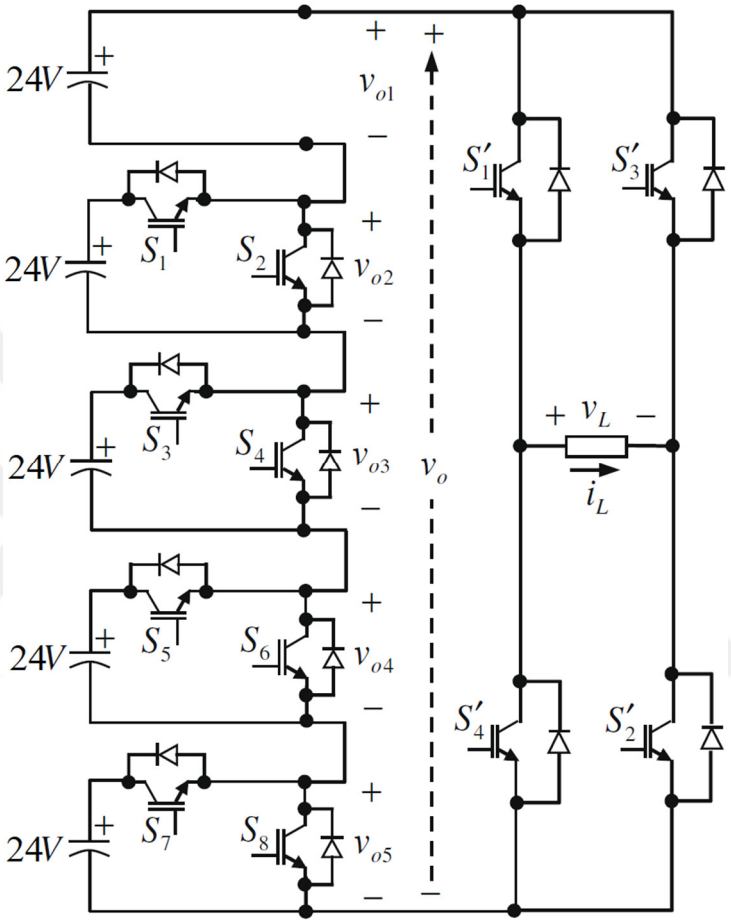

Figure 3.3 Modified reduced switch 11-level MLI topology.

Furthermore, it also allows for adjustable output voltage levels. Switching losses are minimized by activating and deactivating the switching devices only once in each cycle. During the time interval $0 < t < (T/2)$, switches S'_1, S'_2 are simultaneously ON, generating the positive half of the output voltage waveform V_L. Conversely, in the interval $(T/2) < t < T$, the turning ON of switches S'_3, S'_4 results in the negative half of the output voltage waveform $-V_L$. The output phase voltage in this proposed topology is characterized by (3.4):

$$l = 2s + 1 \tag{3.4}$$

where "*l*" signifies the quantity of levels and "*s*" represents the requisite quantity of DC sources. In a standard cascaded MLI setup, the quantity of DC voltage sources is needed to match the number of output phase voltages. Figure 3.4 presents a comparative analysis of the number of switches required in a conventional cascaded MLI against the number of switches required in the proposed topology. Figure 3.4 also shows that the proposed topology requires fewer switches to achieve "*l*" level voltages in the output. This is a great advantage in terms of a reduction in both the installation space and the quantity of gate drivers needed [93]. For instance, the generation of a single-phase output voltage with $l = 11$ levels: the proposed topology necessitates the use of 12 switches, whereas a conventional cascaded H-bridge multilevel inverter would require 20 switches and other reduced switch topology would require 14 switches.

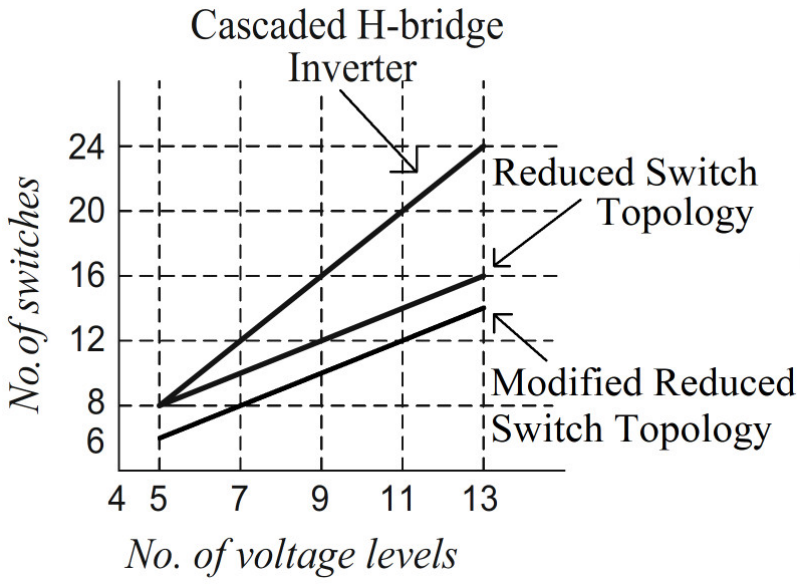

Figure 3.4 Switch counts versus output voltage levels.

Table 3.1 shows that number of components per phase for different 11-level inverter topologies and three phase.

Table 3.1 Number of switches for 11-level inverter.

#	Configuration	Number of switches per phase	Number of switches for three phase
1	Cascaded H-Bridge	20	60
2	Reduced Switch	14	42
3	Modified Reduced Switch	12	36

MLIs make use of variety of modulation methods, broadly divided into two categories based on their switching frequencies as high or low frequency values. High frequency switching approaches including space vector pulse width modulation (SVPWM) and sinusoidal pulse width modulation (SPWM), typically require multiple commutating semiconductor switches throughout each cycle of the output voltage waveform.

On the other hand, low switching frequency schemes including SHE, synchronous optimal pulse width modulation (SOP), and space vector control (SVC) [94], typically involve only one or two commutations per cycle. The primary benefits of low frequency switching schemes are their minimal switching losses, reduced need for filtering components, and absence of harmonic interference. These advantages make these techniques particularly well-suited for high-voltage applications [20], [95].

In this study, low frequency switching has been applied with selective harmonic elimination method for less switching losses. The fundamental frequency and switching frequency are 50 Hz.

3.3 Selective Harmonic Elimination Method

In the design of cascaded H-bridge inverters, the staircase-like voltage output is derived from the cumulative addition of each DC source voltage (V_{dc}) across individual H-bridge cells (m), with the count of these cells (m) equating to the number of sources (s). This design establishes a relationship between the number of levels (n) and sources, expressed mathematically as $2s + 1$. Figure 3.5 demonstrates a behavioural comparison between an idealized single-phase sine voltage waveform ($f(t)_V$) and the corresponding staircase voltage output of a multilevel inverter over a period (T). In this setup, the peak phase voltage matches sV_{dc} voltage, and the defined angles, which are calculated for quarter-wave symmetry, adhere to the following criteria (3.5):

$$0° \leq \alpha_1 \leq \alpha_2 \leq \ldots \leq \alpha_{(S-1)} \leq \alpha_S \leq 90° \tag{3.5}$$

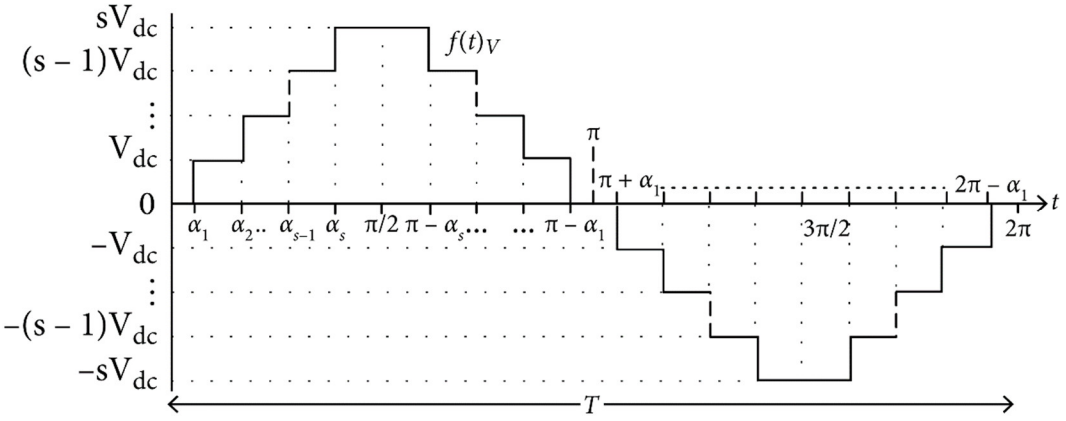

Figure 3.5 Phase voltage output of the MLI staircase.

Utilizing Fourier analysis [23], [96], on the MLI staircase output depicted in Figure 3.5 can be characterized in the following (3.6):

$$f(t)_V = \begin{cases} \frac{4V_{dc}}{n\pi}[cos(n\alpha_1) + \ldots + cos(n\alpha_n)], & for\ odd\ n \\ 0, & for\ even\ n \end{cases} . \tag{3.6}$$

SHE focuses on removing low-order harmonics while maintaining the fundamental component at a specified amplitude. In a three-phase connected system similar the one treated in this study; the triplen harmonic contents are naturally nullified on the line-to-line voltage due to the implementation of a balanced three-phase system [13], [97], [98], [99]. Consequently, (3.6) is solved to exclude the fifth, seventh, eleventh, and thirteenth order harmonics, ensuring that the amplitude of the fundamental component remains constant at *M*. For this reason, (3.6) can be reformulated as expressed in (3.7):

$$\begin{gathered} cos(\alpha_1) + cos(\alpha_2) + \ldots + cos(\alpha_5) = M \\ cos(5\alpha_1) + cos(5\alpha_2) + \ldots + cos(5\alpha_5) = 0 \\ cos(7\alpha_1) + cos(7\alpha_2) + \ldots + cos(7\alpha_5) = 0 \\ cos(11\alpha_1) + cos(11\alpha_2) + \ldots + cos(11\alpha_5) = 0 \\ cos(13\alpha_1) + cos(13\alpha_2) + \ldots + cos(13\alpha_5) = 0 \end{gathered} \tag{3.7}$$

where

$$M = \frac{V_l \times \pi}{4 \times s \times V_{dc}} \tag{3.8}$$

M is known as the modulation index within the range of $0 < M \leq 1$ and V_l represents the desired fundamental component [100]. Under the constraints outlined in Equation 3.5 and 3.7 can be reformulated as an optimization problem [23], [101] in (3.9):

$$minf(\alpha_1, \alpha_2, \alpha_3, \alpha_4, \alpha_5) = \left[\sum_{i=1}^{5} cos(\alpha_i) - M\right]^2 + \left[\sum_{i=1}^{5} cos(5\alpha_i)\right]^2 + \left[\sum_{i=1}^{5} cos(7\alpha_i)\right]^2 + \left[\sum_{i=1}^{5} cos(11\alpha_i)\right]^2 + \left[\sum_{i=1}^{5} cos(13\alpha_i)\right]^2. \quad (3.9)$$

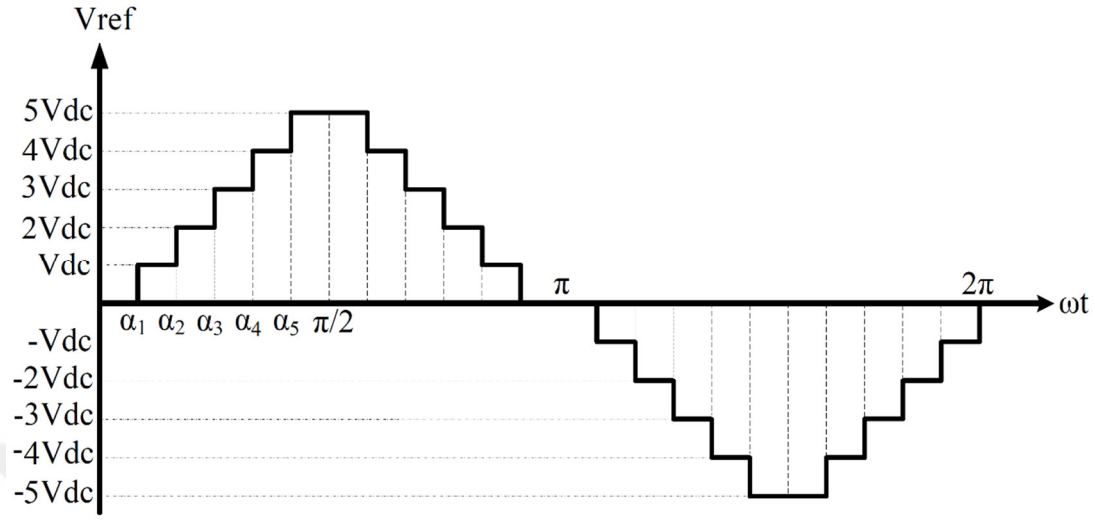

Figure 3.6 Phase voltage output of the 11-level MLI staircase.

Upon presenting the definition of the objective function or fitness function, and before introducing the analysis of power loss and Hybrid TLBO-WOA in detail in the next section, the states of staircase voltage have been shown in Figure 3.7 and 3.8. All steps in Figure 3.6 have been described as switches ON or OFF in Table 3.2. Figure 3.7 (i) and Figure 3.8 (vii) are zero-state. Figure 3.7 (ii)-(vi) are positive cycle and Figure 3.8 (viii)-(xii) are negative cycle of output.

Table 3.2 Switching table of the proposed multilevel inverter.

#	Output	S_1	S_3	S_5	S_7	S_2	S_4	S_6	S_8	S'_1	S'_2	S'_3	S'_4
i	0	0	0	0	0	0	0	0	0	0	0	0	0
ii	V_{dc}	0	0	0	0	1	1	1	1	1	1	0	0
iii	$2V_{dc}$	1	0	0	0	0	1	1	1	1	1	0	0
iv	$3V_{dc}$	1	1	0	0	0	0	1	1	1	1	0	0
v	$4V_{dc}$	1	1	1	0	0	0	0	1	1	1	0	0
vi	$5V_{dc}$	1	1	1	1	0	0	0	0	1	1	0	0
vii	0	0	0	0	0	0	0	0	0	0	0	0	0
viii	$-V_{dc}$	0	0	0	0	1	1	1	1	0	0	1	1
ix	$-2V_{dc}$	1	0	0	0	0	1	1	1	0	0	1	1
x	$-3V_{dc}$	1	1	0	0	0	0	1	1	0	0	1	1
xi	$-4V_{dc}$	1	1	1	0	0	0	0	1	0	0	1	1
xii	$-5V_{dc}$	1	1	1	1	0	0	0	0	0	0	1	1

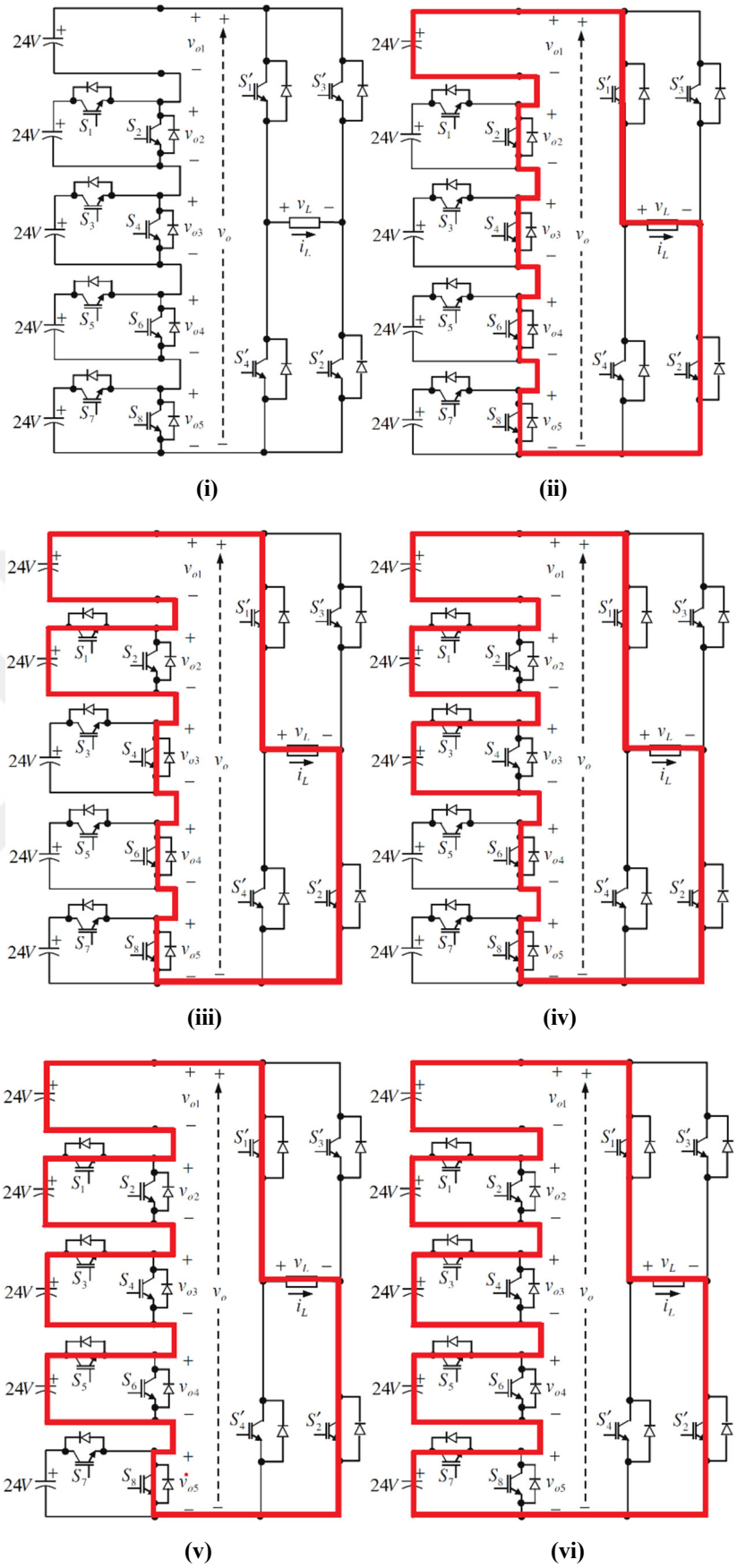

Figure 3.7 Different switching states of the proposed multilevel inverter in positive half cycle and zero state.

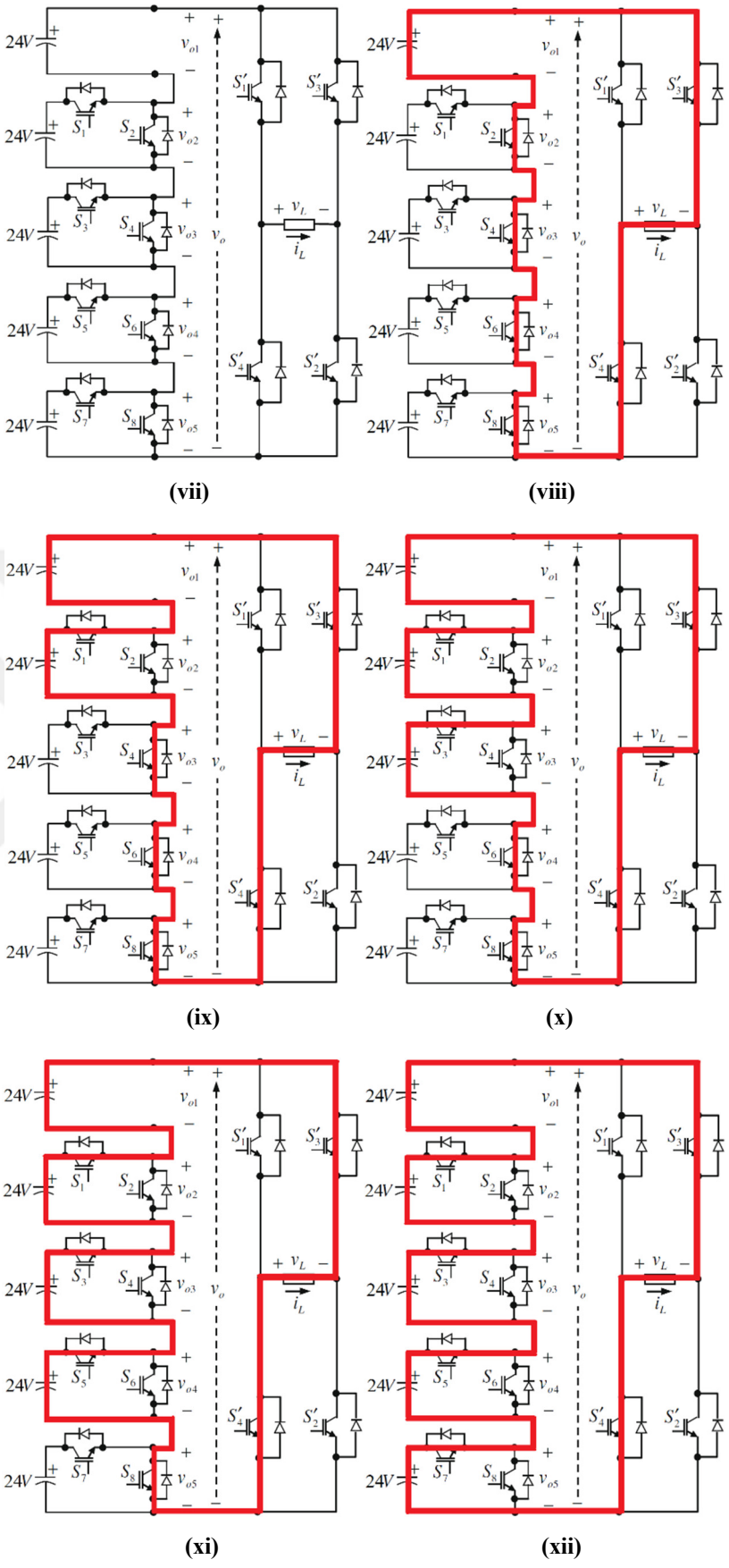

Figure 3.8 Different switching states of the proposed multilevel inverter in negative half cycle and zero state.

3.4 Analysis of Power Loss

In a multilevel inverter (MLI), two types of losses occur when the power electronic switches operate:

a. Conduction losses

b. Switching losses

Conduction losses occur when the switch is conducting and current flows through it. This current flow leads to a significant rise in temperature. If the temperature is not properly managed, the device can overheat and burn out, potentially damaging the circuit. Therefore, analyzing power loss or thermal loss is crucial. The switching losses are further divided into two categories: turn-on losses and turn-off losses. These losses are significant because they impact the dv/dt rating. Understanding these losses, along with their calculation expressions, is essential for efficient MLI operation [102].

3.4.1 Conduction Losses

Conduction loss can be defined as the loss that occurs when a power electronic device is in conduction mode. For a specific MOSFET and diode, this loss can be calculated using the following formula (3.10):

$$P_{C,loss} = \sum_{all\ components} I_{C,ON}^2 \times R_{int} \tag{3.10}$$

where $I_{C,ON}$ is the current flowing during conduction, and R_{int} represents the internal resistance of the component, such as an MOSFET and diode.

3.4.2 Switching Losses

Switching loss (P_S) refers to the power dissipated during the turn-ON and turn-OFF events of the MOSFET and diode. These turn-ON and turn-OFF losses are proportional to the switching frequency and can be expressed as follows (3.11), (3.12):

$$E_{t,ON} = \int_0^{T_{ON}} V(t) \times I(t)\, dt = \frac{V_{s,ON} \times I \times t_{ON}}{6} \tag{3.11}$$

$$E_{t,OFF} = \int_0^{T_{OFF}} V(t) \times I(t)\, dt = \frac{V_{s,OFF} \times I \times t_{OFF}}{6} \tag{3.12}$$

where $V_{s,ON}$, $V_{s,OFF}$ are the turn-ON and turn-OFF voltages. Therefore, the total power loss is equal to the sum of these losses which is shown by Equations 3.10, 3.11, and 3.12. Power loss is a crucial factor in designing a new topology. Ideally, power loss should be evenly distributed among all the switches to ensure uniform thermal dissipation throughout the converter. This balanced heat distribution prevents the formation of localized hot spots, which can ultimately cause switch failure [102].

3.5 Overview of the Proposed Hybrid Optimization Algorithm

In this section, TLBO, WOA and hybrid optimization method are properly presented. Proposed hybrid optimization algorithm uniquely merges two different TLBO and WOA metaheuristic techniques. A comprehensive analysis of the algorithm, including its fundamental components, has been described.

3.5.1 Teaching-Learning-Based Optimization

The TLBO, functioning as a class-based optimization method, mimics the instructional and learning dynamics found in a classroom environment. It was introduced by R. Venkata Rao in 2011 [103]. It utilizes interactions between teachers and students to enhance solution quality. This algorithm unfolds in two distinct stages: the Teacher Phase and the Learner Phase. During the Teacher Phase, the optimal solution, referred to as the 'teacher,' imparts its knowledge to the rest of the solutions, termed 'students,' within the group. The goal of this exchange is to elevate the over-all solution quality by leveraging the teacher's experience and insight. Subsequently, in the Learner Phase, the students engage in peer-to-peer learning, promoting both collaborative discovery and exploration [104]. The process of the TLBO algorithm is graphically depicted in Figure 3.9.

Key Concepts and Phases:

a) **Population:** The algorithm starts with a population of candidate solutions, referred to as learners or students. Each learner represents a potential solution to the optimization problem.

b) **Teacher Phase:** In this phase, the best solution in the current population is considered the teacher. The teacher attempts to improve the mean result of the class by moving the learners towards a better solution.

c) **Learner Phase:** In this phase, learners interact with each other to increase their knowledge. In this phase, learners interact with each other to increase their knowledge.

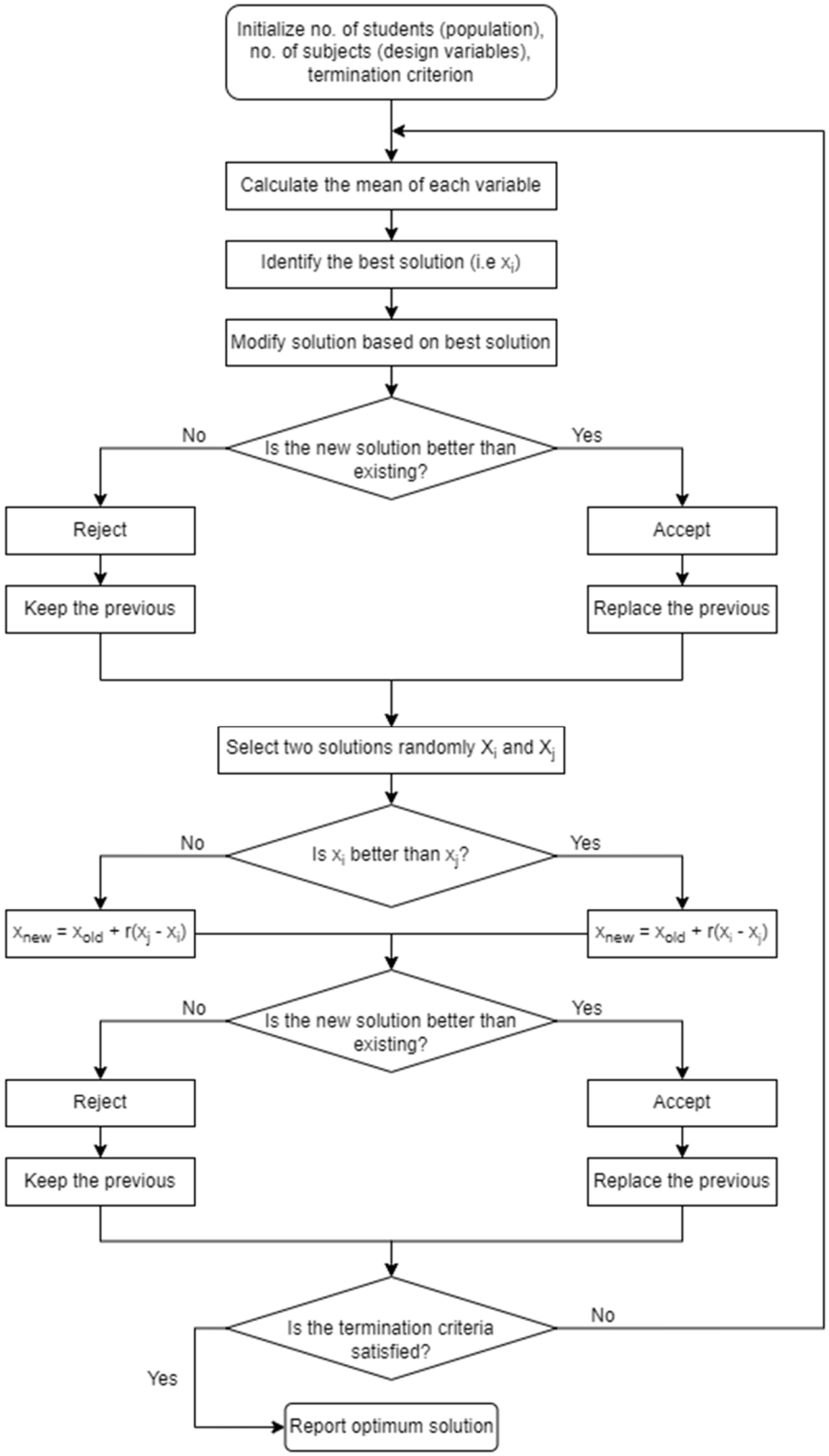

Figure 3.9 TLBO-algorithm flowchart.

The flowchart demonstrates the process where a user-generated population undergoes a design phase, involving setting variables and termination criteria, and the calculation of other parameters like each variable's average value to determine the optimal solution. Iteration commences to find a superior solution, which, upon meeting established criteria, is adopted as the new optimum, or the search continues for an improved solution. This involves randomly selecting two solutions and keeping the better one for comparison with the previously determined best solution to decide if it should replace the existing 'teacher' solution. This process repeats until fulfilment of the completion criteria, culminating in the reporting of the finest solution achieved through these iterations.

One of the key strengths of TLBO is its simplicity; it only necessitates the population size and problem dimensions as its parameters. This algorithm excels in balancing exploration and exploitation, ensuring an extensive search across the solution space while effectively utilizing areas with potential. However, in certain cases, the exploration capabilities of TLBO may not be sufficient to achieve the most favorable results then the inclusion of another metaheuristic algorithm is prompted to boost its performance [100].

3.5.2 Whale Optimization Algorithm

The WOA is a nature-inspired algorithm primarily inspired by the hunting behavior of humpback whales. It was introduced by Seyedali Mirjalili and Andrew Lewis in 2016 [55]. Whales exhibit an impressive ability to locate and capture their prey using unique strategies such as spiral path movement and encircling behavior. These traits make WOA well-suited for global optimization tasks, as the algorithm mimics the whales' hunting process to explore the search space efficiently [105]. The processes in the WOA algorithm are graphically depicted in Figure 3.10.

Key Concepts and Phases:

a) **Hunting Mechanism:** Humpback whales primarily use a unique hunting method called bubble-net feeding. This involves creating bubble circles or spirals to encircle and trap prey.

b) **Mathematical Modeling:** The WOA algorithm mathematically models the bubble-net feeding behavior and the whales' movement towards prey.

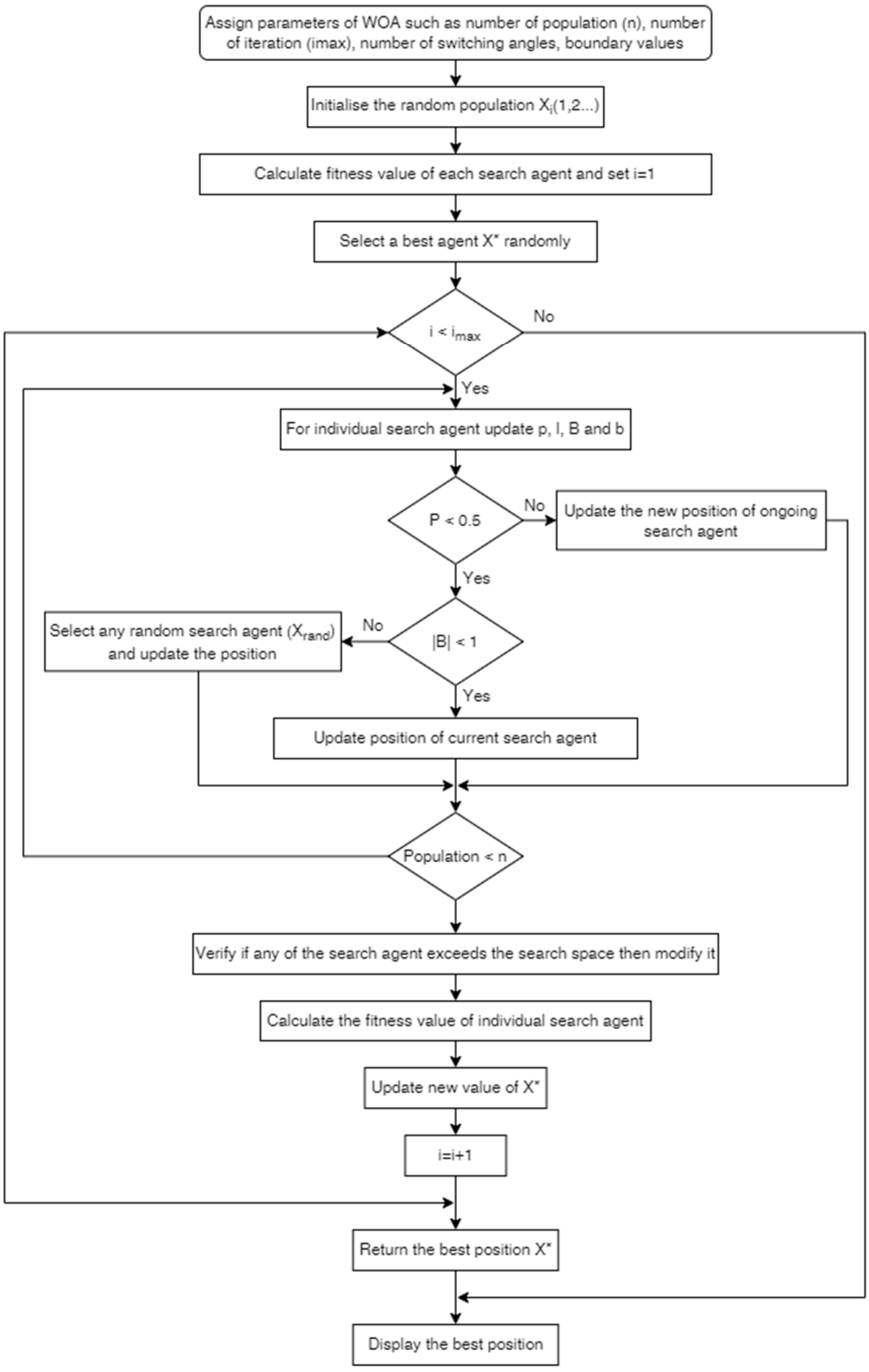

Figure 3.10 WOA-algorithm flowchart.

Although WOA is highly effective in exploration, it can sometimes be prone to over-exploration and inadequate exploitation, which might result in suboptimal outcomes under specific conditions [101].

3.5.3 Hybrid TLBO-WOA Optimization Algorithm

Population-based algorithms work with a set of candidate solutions by using a random search strategy. This multiple search process generally allows them to quickly reach the region where the global optimum is located. However, since these algorithms have highly probability-based search strategies, it may generally take a long time to find the optimum solution in their region. On the other hand, iterative-based algorithms generally work on a single solution candidate. With this serial structure, iterative-based algorithms can generally find the best global optimum of the search problem in a shorter-time than population-based algorithms. In this study, hybridization of TLBO and WOA algorithms is proposed in order to eliminate the above-mentioned disadvantage of population-based algorithms and increase their performance by providing serial structure. Thus, the attributes of both the TLBO and WOA are synergized in a hybrid optimization algorithm, leveraging their combined strengths for more balanced and effective results.

The proposed hybrid TLBO-WOA algorithm's primary objective is to minimize THD in a three-phase eleven-level MLI. By optimizing the switching angles of the MLI, the algorithm aims to significantly reduce lower-order harmonics, thereby enhancing the power quality of the MLI. In accordance with this purpose, the switching angles are optimized in the first stage of the proposed TLBO-WOA by TLBO algorithm and then optimized switching angles solutions are improved by WOA algorithm. This process has been repeated as iterative based until termination criterion is met. So, the optimum switching angles values has been obtained by the proposed TLBO-WOA algorithm compared with the benchmark TLBO and WOA algorithms.

Proposed hybrid algorithm, named TLBO-WOA, leverages the interaction-based learning of TLBO and the hunting mechanism of WOA to achieve a balanced exploration and exploitation strategy. Our objective in merging these two algorithms is to amplify their collective efficiency and address the specific limitations each one possesses individually. The hybrid optimization algorithm is performed in two stages. In first stage, TLBO is executed, then the solution obtained from TLBO algorithm run is used as an initial solution for WOA algorithm in second stage. Thus, an iterative-based structure has been obtained by using the TLBO and WOA algorithms together.

Furthermore, TLBO-WOA hybrid algorithm is also explained meticulously, and the flowchart for hybrid algorithm is shown in Figure 3.11.

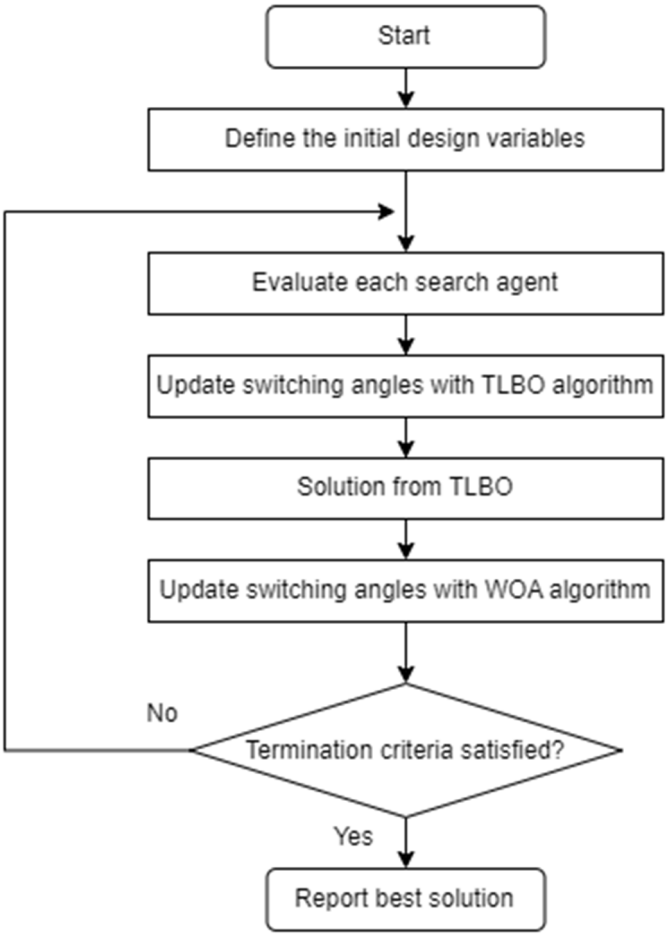

Figure 3.11 Hybrid TLBO-WOA-algorithm flowchart.

In the TLBO-WOA algorithm, the Teacher Phase from TLBO plays a crucial role in spreading knowledge from the optimal solution, known as the 'teacher,' to the remaining solutions, referred as 'students,' within the population. This exchange of knowledge allows the students to learn from the teacher's experiences and improves their solutions. Subsequently, the Learner Phase facilitates cooperative learning and exploration among the students, allowing them to interact and exchange information. The pseudo code of the TLBO-WOA is described below in Table 3.3.

Table 3.3 Pseudo Code of Hybrid TLBO-WOA

Begin procedure
Set the generation number, T=0
Initialize N (number of students) and D (dimension)
Generation of initial students and evaluate them
while termination criterion is not satisfied **do**
  Choose the best student as $x_{teacher}$
  Calculate the mean x_{mean} of all students
  for each student x_i
    $T_F = round[1 + rand(0,1)]$
    Update the student according to
$x_{i,new} = x_{i,old} + rand \cdot (x_{teacher} - T_F \cdot x_{mean})$
    Evaluate the new student $x_{i,new}$
    Accept $x_{i,new}$ if it is better than the old one $x_{i,old}$
    Randomly select another student x_j which is different from x_i
    Update the learner according to
$$x_{i,new} = \begin{cases} x_{i,old} + rand \cdot (x_i - x_j), & \text{if } f(x_i) \le f(x_i) \\ x_{i,old} + rand \cdot (x_j - x_i), & \text{if } f(x_i) > f(x_i) \end{cases}$$
    Evaluate the new learner $x_{i,new}$
    Accept $x_{i,new}$ if it is better than the old one $x_{i,old}$
  end for
Set the whales population according to the best students of TLBO
Calculate the fitness of each search agent X*.
  while $i < i_{max}$
    Calculate the value of a
    for each search agent
      if $p < 0.5$ then
        if $|\boldsymbol{A}| < 1$ then $X(t+1) = X^*(t) - A \cdot D$
          else if $|\boldsymbol{A}| \geq 1$ then $X(t+1) = X_{rand}(t) - A \cdot D''$
          end if
        else if $p \geq 0.5$ then
          $X(t+1) = D' \cdot e^{bl} \cdot \cos(2\pi l) + X^*(t)$
        end if
    end for
    Evaluate the fitness of $X(t+1)$ and update X*
  end while
end while
Display X*, the best optimal solution
end procedure

Teacher Phase

Learner Phase

CHAPTER 4
SIMULATION RESULTS

4.1 Introduction

The proposed hybrid TLBO-WOA algorithm has been implemented and offline calculated in MATLAB to obtain the optimized switching angles for SHE of reduced switch MLI. Simulink has been utilized for the simulation of the multilevel inverter. Utilizing equal voltage sources, various voltage levels have been generated. The specifics of the simulation and optimization parameters are given with in Table 4.1. A MLI is connected to the resistor of value 120 Ω for simulation analysis. Also, inductive load 120 Ω and 100 mH RL load has been tested in simulation design.

Table 4.1 Simulation and Optimization Parameters.

S. No.	Parameters/Components	Specifications	No. of Component
1.	Population Size	100	
2.	Number of Iterations	250	
3.	Number of Dimensions	5	
4.	Lower Boundary	[0° , 0° , 0° , 0° , 0°]	
5.	Upper Boundary	[90° , 90° , 90° , 90° , 90°]	
6.	Voltage Source (DC)	24 V	15
7.	Switching frequency	50 Hz	
8.	Fundamental frequency	50 Hz	
9.	R Load	R=120 Ω	Δ-connected
10.	RL Load	R= 120 Ω and L=100 mH	Δ-connected

4.2 Simulation Setup

MATLAB®/Simulink has been used for designing the 11-level three phase MLI circuit. Figure 4.1 shows the measurement of line-to-line voltage and THD value in simulation. The three phase load has been connected Y configuration for different measurements. Figure 4.2 illustrates the voltage and current measurement of line-to-neutral for Y-connected.

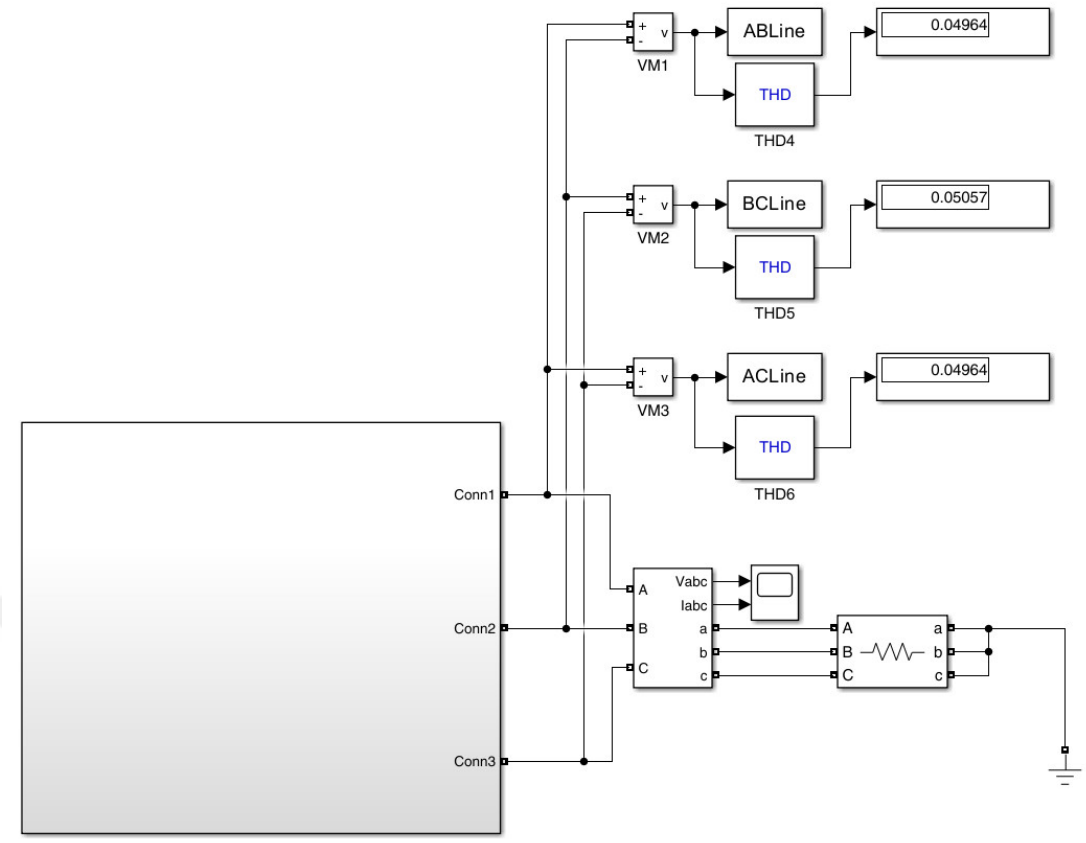

Figure 4.1 Main block diagram of measurement three phase MLI with three phase load configurations Y connected.

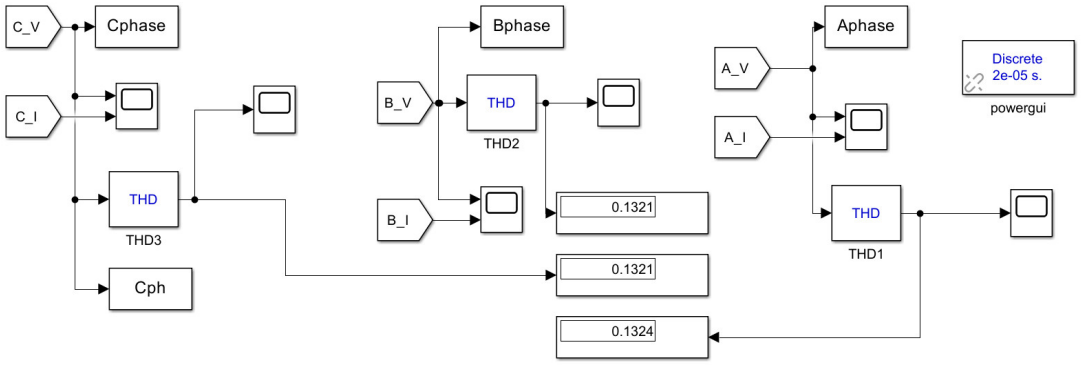

Figure 4.2 Measurement voltage and current of line-to-neutral for Y connected.

Figure 4.3 shows the measurement of line-to-line voltage and THD value in simulation. The three phase load has been connected Δ configuration for different measurements. Figure 4.4 illustrates the voltage and current measurement of phase for Δ-connected.

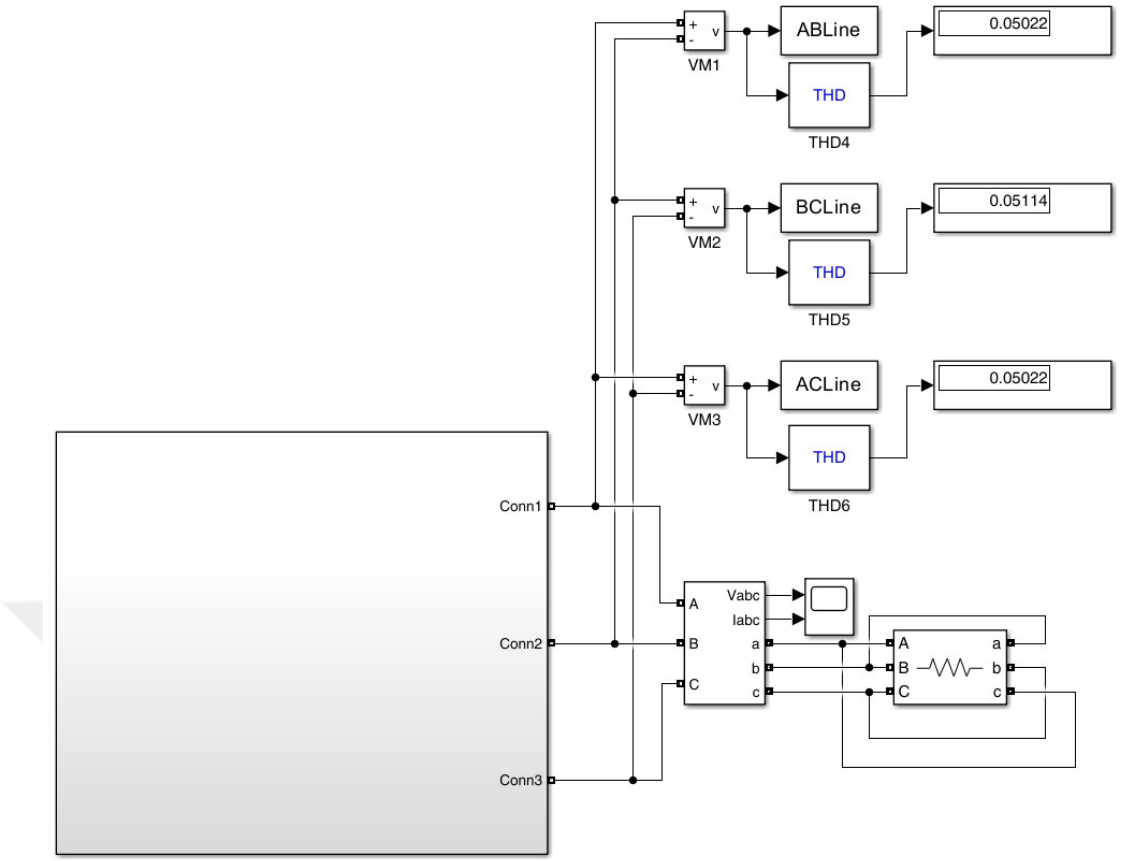

Figure 4.3 Main block diagram of measurement three phase MLI with three phase load configurations Δ-connected.

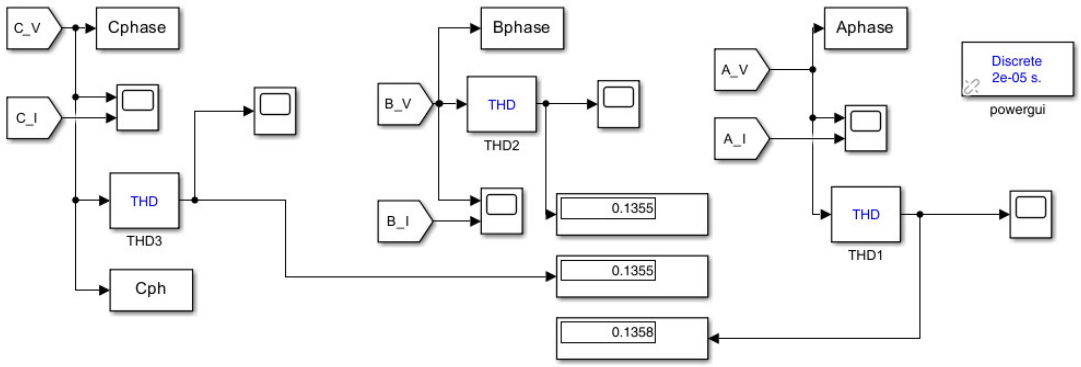

Figure 4.4 Measurement voltage and current of phase for Δ connected.

Figure 4.5 shows that the block diagram of applying switching angles to SPWM circuit. These angles come frome offline calculation of hybrid optimization algorithm. Figure 4.6 illustrates the modified reduced switch 11-level MLI for phase A which is reference. Also, Figure 4.7 depicts the same circuit with 120˚ and 240˚ shifted for phase B and phase C, respectively.

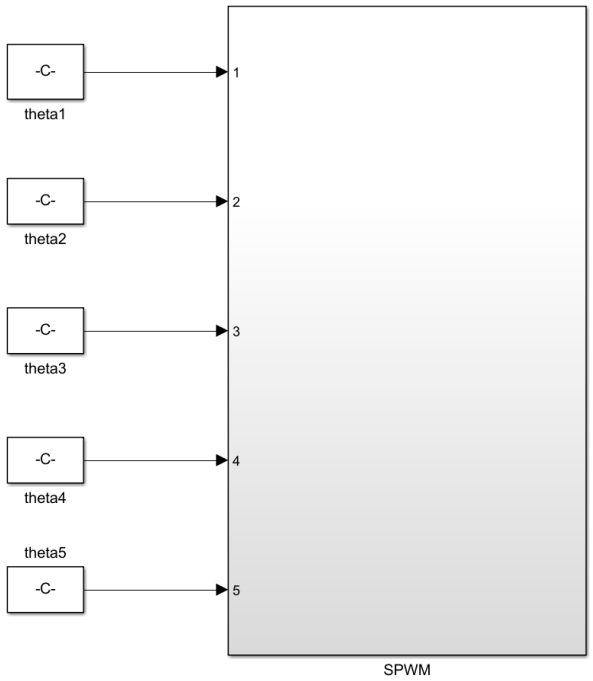

Figure 4.5 Block diagram of applying switching angles to SPWM circuit.

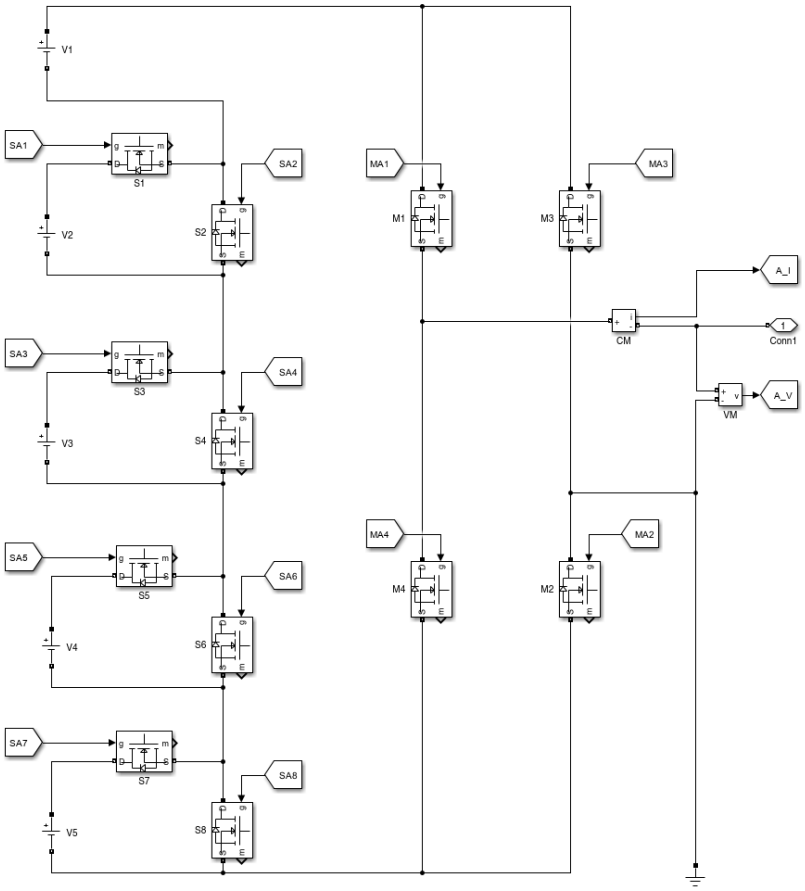

Figure 4.6 Modified reduced switch 11-level MLI for phase A.

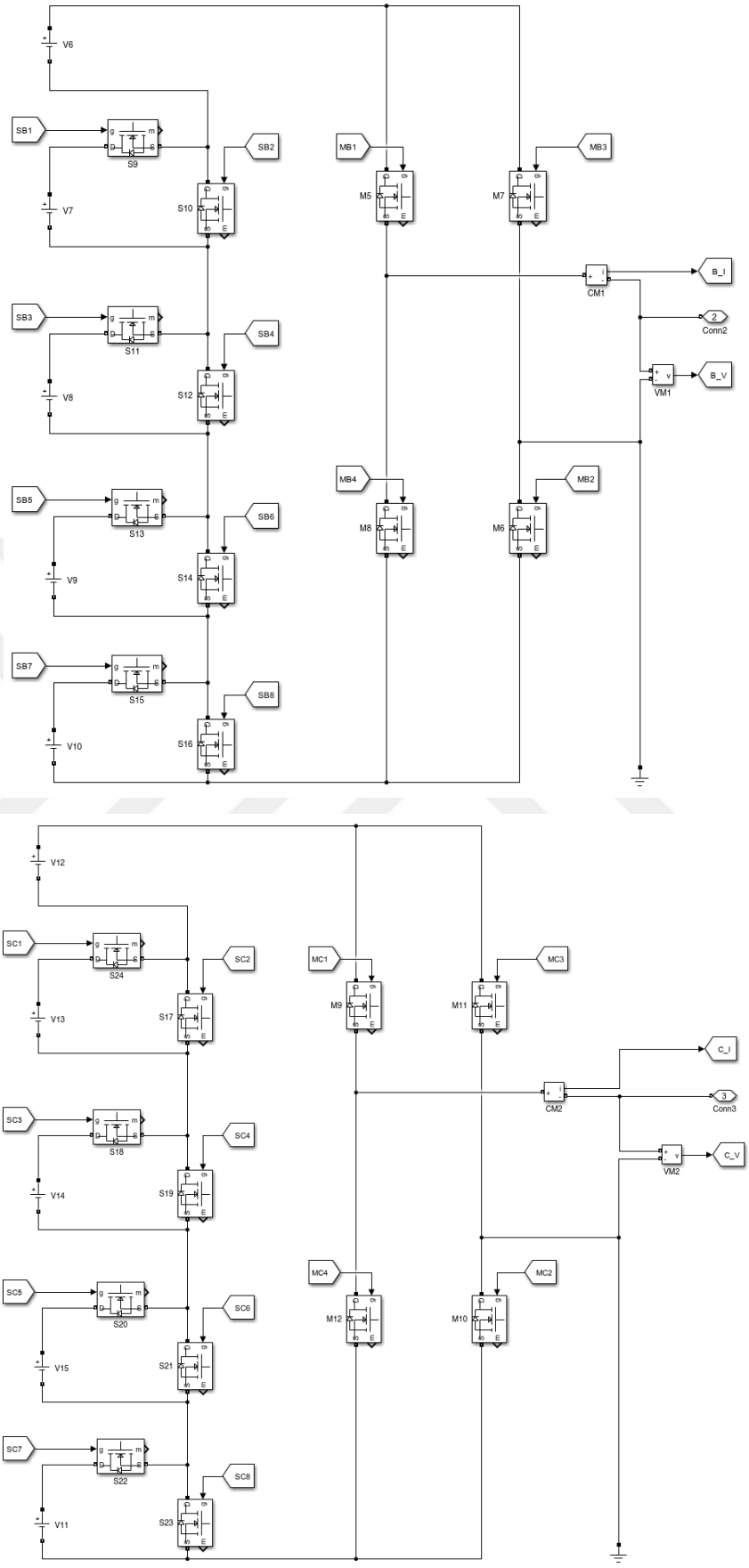

Figure 4.7 Modified reduced switch 11-level MLI for phase B and C.

Figure 4.8 shows that block diagram of generating PWM signals for 11-level MLI for phase A which is 0˚ reference. For phase B and phase C are also same configurations, however only difference is phase shift 120˚ and 240˚, respectively. There are several gates such as: AND, OR, SUM, NOT, bigger, smaller, smaller equal, bigger equal, and multiply have been used for this circuit.

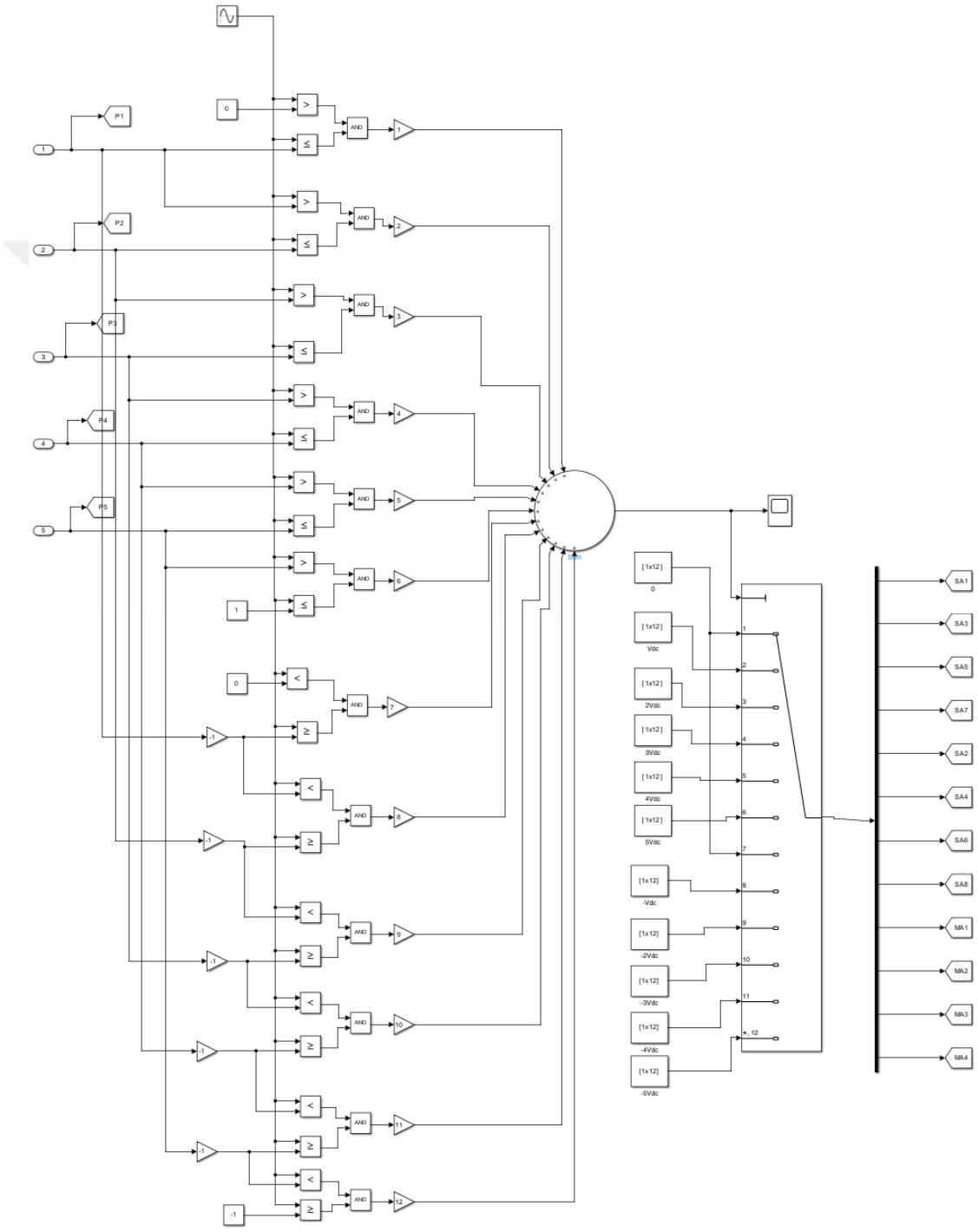

Figure 4.8 Block diagram of generating PWM signals of Phase A.

Figure 4.9 illustrates the oscilloscope view of multiport output on Figure 4.8. There are 12 PWM signals for 12 different sequences.

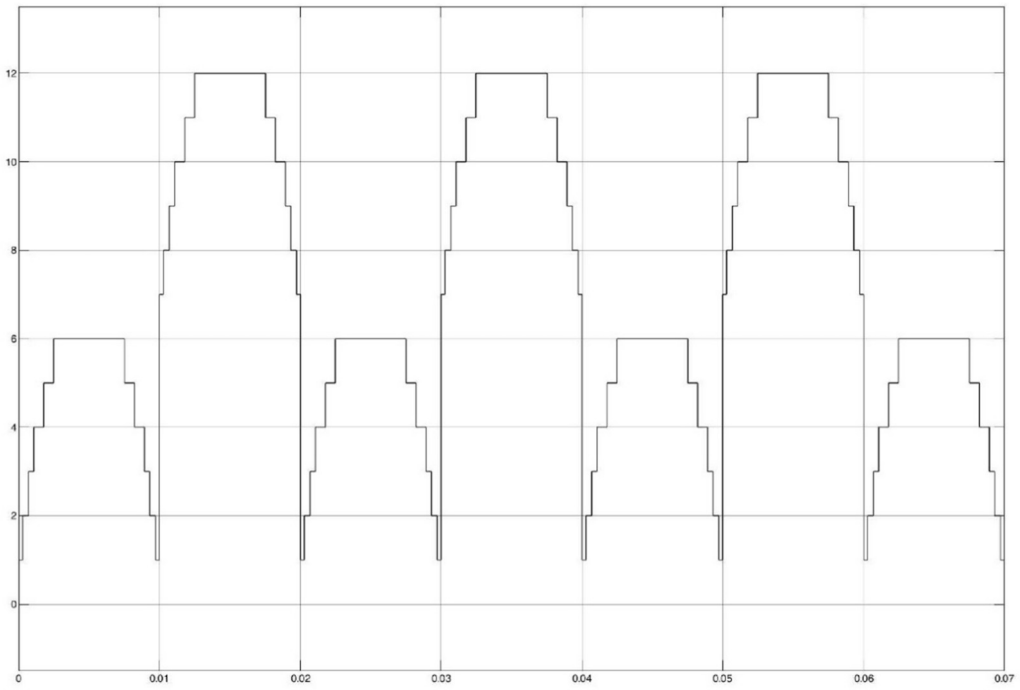

Figure 4.9 Oscilloscope view of multiport output on Figure 4.8.

4.3 Simulation Validation

For the validation purpose, the performance of TLBO-WOA algorithm has been demonstrated with an implementation of algorithm in the MATLAB®/Simulink environment as shown in Figure 4.10. Additionally, a comparative analysis has been conducted to assess the performance of TLBO-WOA against other optimization algorithms in terms of convergence solution quality.

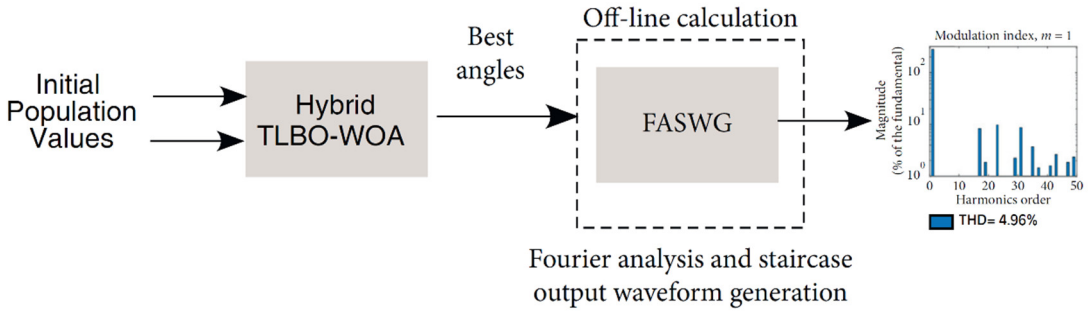

Figure 4.10 Simulink design to determine the THD for the optimal angles calculated by TLBO-WOA.

The test system is run on MATLAB® installed on an Intel® Core ™ i7 10th Gen. CPU in a 2.3 GHz system with 32 GB RAM. For each test, a consistent population size of 100 and a total of 250 iterations have been conducted. The optimization process times have been calculated as follow: Hybrid TLBO-WOA at 5.81 seconds, TLBO at 5.65 seconds, and WOA at 5.53 seconds. The convergence graph of optimization algorithms has been shown in Fig. 4.11.

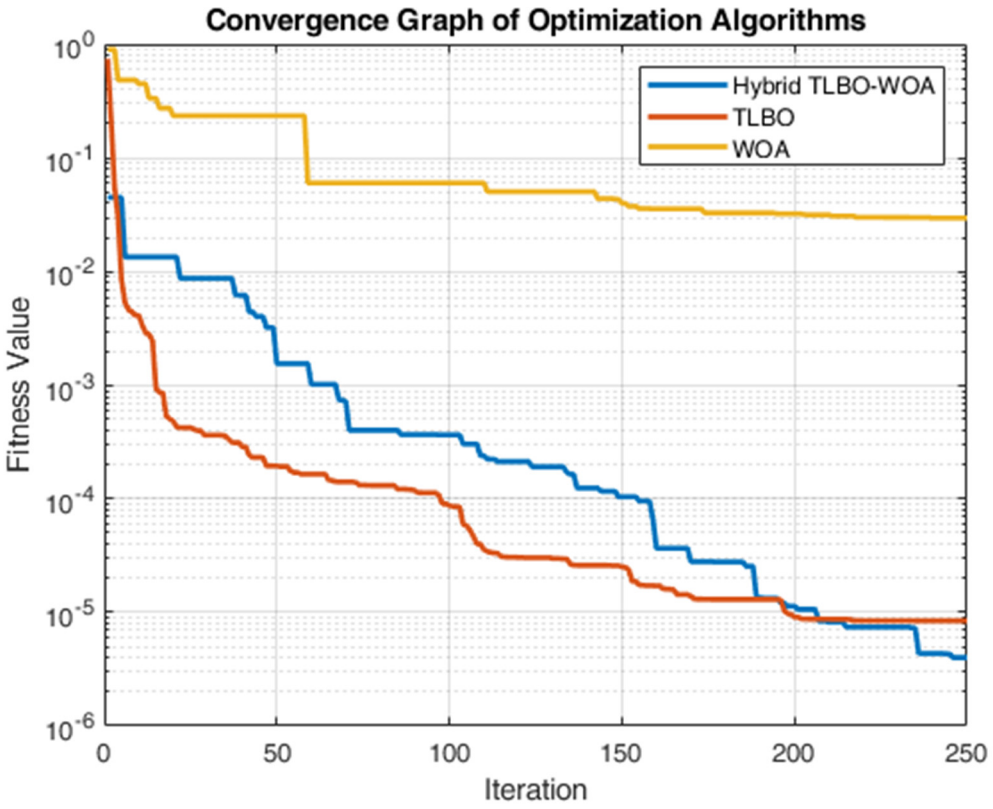

Figure 4.11 Convergence graph of optimization algorithms with population size of 100 population and 250 iterations.

The effectiveness of the Hybrid TLBO-WOA in solving the non-linear equations associated with the SHE technique, three tests have been performed for each algorithm under consideration. The modulation index M considered within ranges from 0 to 1 as defined in Equation 3.9. Accordingly, analyses at modulation indices (m) of 0.6, 0.8, and 1 have been conducted. These values are commonly utilized in MLIs and thus have been chosen for their relevance. Results, summarized in Tables 4.3, 4.4, 4.5, demonstrate that the TLBO-WOA consistently achieved superior fitness across all tested modulation indices. The angles approximating the optimal solution, as determined by the TLBO-WOA, have been then applied in Fourier analysis to evaluate

THD and the effective elimination of the 5th, 7th, 11th, and 13th order harmonics at the specified modulation indices. Exhibiting the most favourable outcomes, Figure 4.17, 4.19, 4.21 display the Fast Fourier Transform (FFT) spectrum and line-to-line voltage output derived from the angles calculated by the TLBO-WOA, as detailed in Tables 4.3, 4.4, 4.5, confirming the successful minimization of the targeted low-order harmonics.

In this study, the harmonic contents in the output voltage signal of the inverter, associated with different optimization methods have been evaluated according to the IEEE-519 standard [106]. As per this standard, a minimum of 50 harmonics must be analysed to assess the quality of the inverter's output signal. The calculation of the THD percentage is conducted using (4.1), which is a crucial step in determining the signal quality.

$$\%THD = \left(\frac{\sqrt{\sum_{n=1,3,5\ldots}^{50} V_n^2}}{V_1} \right) \cdot 100 \tag{4.1}$$

where n represents the order of the odd harmonics (1, 3, 5, 7,…,49), V_1 is the amplitude of the first harmonic, which is the fundamental voltage, and V_n is as defined in (3.6).

Figure 4.12 illustrates the switching angles from Table 4.2, approximating the optimal values, computed via the Hybrid TLBO-WOA for various modulation indices.

Table 4.2 Results of TLBO-WOA with different modulation indexes.

Modulation Index	Switching Angles (in degree)					THD	Fitness
	α_1	α_2	α_3	α_4	α_5		
0.5	36.099	48.438	58.581	61.533	90.000	10.62	5.1112×10^{-2}
0.55	35.856	48.150	60.966	76.365	90.000	8.91	1.7276×10^{-3}
0.6	35.343	46.953	58.581	72.612	87.840	6.73	5.6476×10^{-9}
0.65	35.730	44.883	56.826	68.049	83.619	6.41	4.8950×10^{-8}
0.7	34.722	44.442	54.504	65.457	78.408	6.12	2.8120×10^{-4}
0.75	15.948	34.308	53.379	63.900	88.776	5.82	1.6110×10^{-5}
0.8	9.711	33.417	43.317	61.191	83.628	5.52	5.8950×10^{-6}
0.85	9.027	33.354	41.598	56.925	77.211	5.47	1.8599×10^{-7}
0.9	7.686	27.603	40.797	52.587	73.044	5.38	3.9907×10^{-6}
0.95	11.475	20.835	34.677	54.126	62.757	5.12	2.8957×10^{-3}
1.0	7.821	19.359	29.574	47.610	63.198	4.96	7.8095×10^{-6}

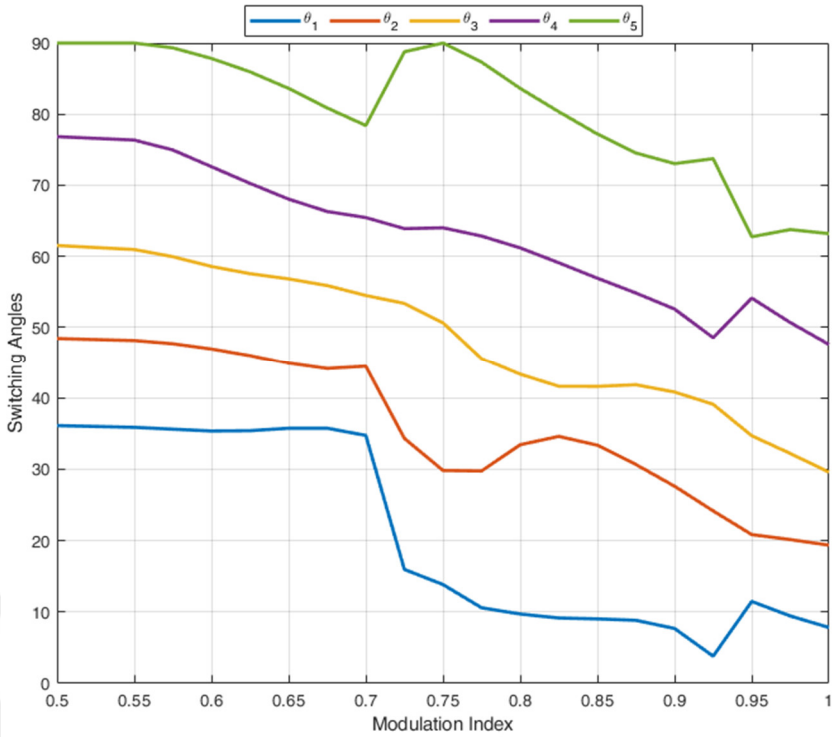

Figure 4.12 Optimized switching angles as a function of the modulation indices.

Figure 4.13 displays the gate signals of switches for the time interval of 50 ms. SA1, SA2, SA3, SA4, SA5, SA6, SA7, SA8, MA1, MA2, MA3, and MA4 are the gate signals for the first of the three-phase system shown in Figure 3.3 signals S1, S2, S3, S4, S5, S6, S7, S8, S'_1, S'_2, S'_3, and S'_4 respectively. The other gate signals for the second and third of the three-phase systems 120˚ and 240˚ shifted according to reference signals A, respectively.

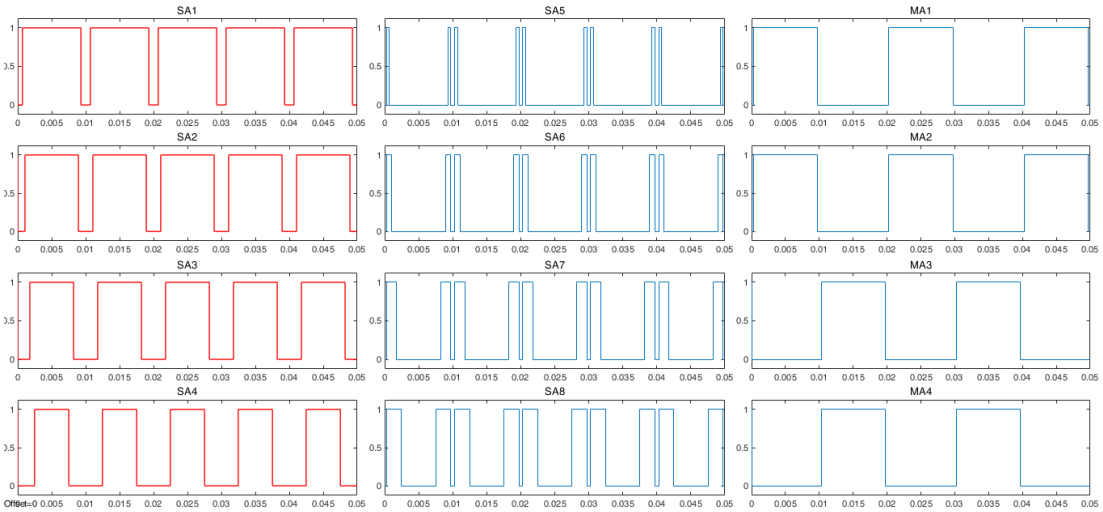

Figure 4.13 Gate signals of 11-level reduced switch MLI on Figure 3.3.

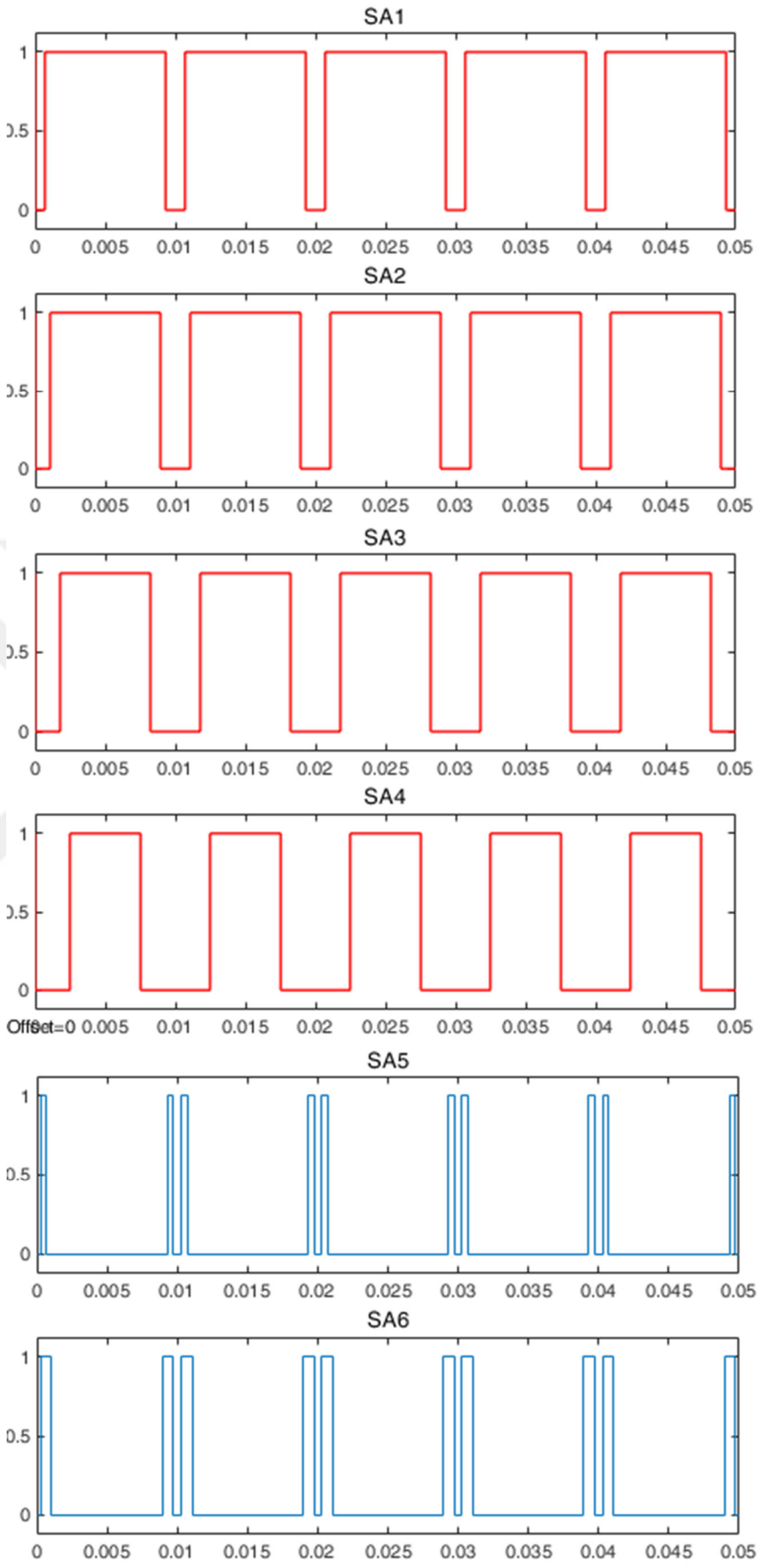

Figure 4.14 Zoom in gate signals of 11-level reduced switch MLI on Figure 4.13.

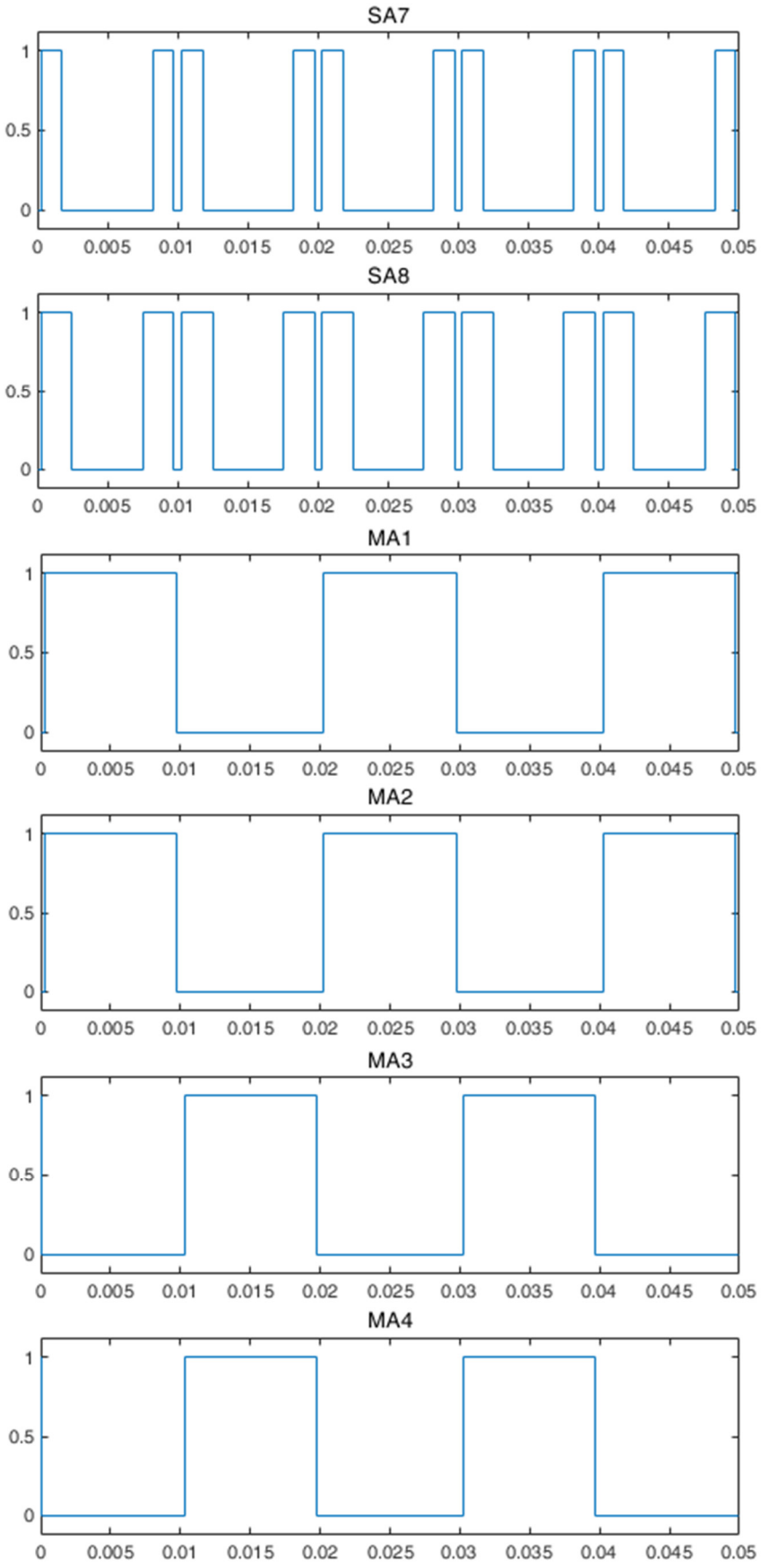

Figure 4.15 Zoom in gate signals of 11-level reduced switch MLI on Figure 4.13.

4.3.1 Case Study for Modulation Index 0.6

Figure 4.16 shows the line-to-line voltage output for modulation index (m) 0.6, R load 120 Ω, and Figure 4.17 displays the Fast Fourier Transform (FFT) spectrum derived from the angles calculated by the Hybrid TLBO-WOA, as detailed in Tables 4.3

Table 4.3 Results of algorithms for m=0.6.

Algorithm	Switching Angles (in degree)					THD	Fitness
	α_1	α_2	α_3	α_4	α_5		
TLBO	35.388	46.010	57.564	70.263	85.959	7.05	6.5267×10^{-8}
WOA	35.350	46.890	58.490	72.440	87.700	6.87	8.1700×10^{-5}
TLBO-WOA	35.343	46.953	58.581	72.612	87.840	6.56	5.6476×10^{-9}

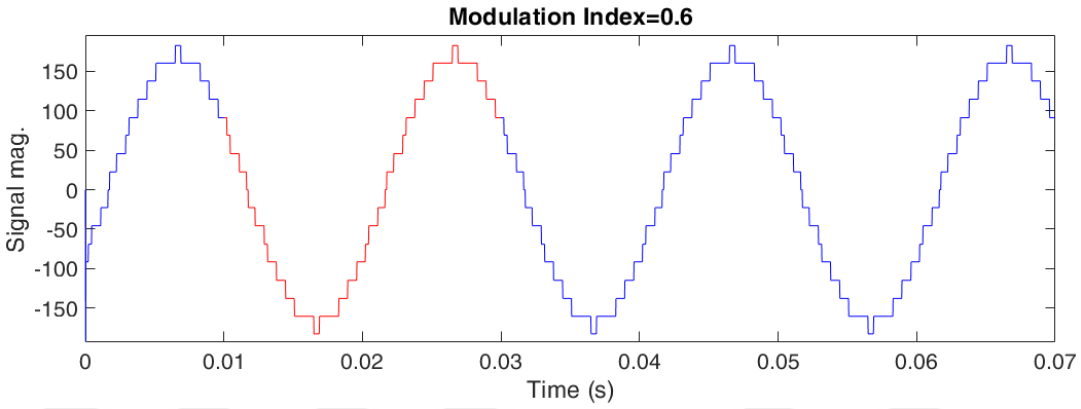

Figure 4.16 Line-to-line voltage output for m=0.6.

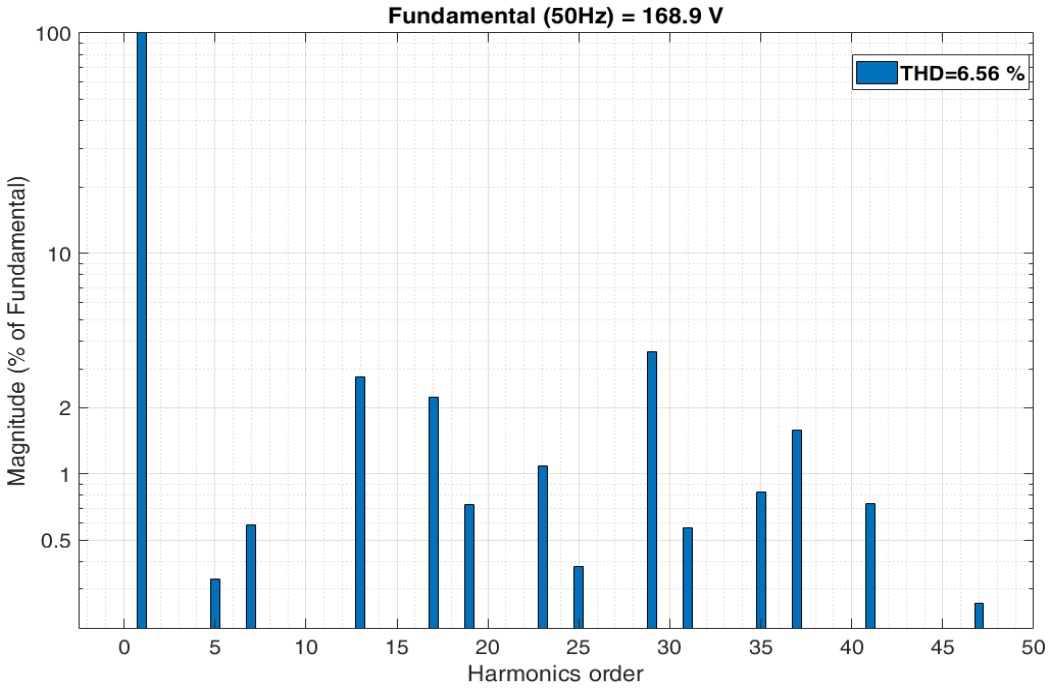

Figure 4.17 FFT analysis results of line voltage output for m=0.6.

4.3.2 Case Study for Modulation Index 0.8

Figure 4.18 shows the line-to-line voltage output for modulation index (m) 0.8, R load 120 Ω, and Figure 4.19 displays the Fast Fourier Transform (FFT) spectrum derived from the angles calculated by the Hybrid TLBO-WOA, as detailed in Tables 4.4.

Table 4.4 Results of algorithms for m=0.8.

Algorithm	Switching Angles (in degree)					THD	Fitness
	α_1	α_2	α_3	α_4	α_5		
TLBO	9.729	33.372	43.353	61.220	83.691	5.56	9.1894×10^{-6}
WOA	33.270	44.500	52.910	64.490	76.640	5.56	3.9300×10^{-2}
TLBO-WOA	9.711	33.417	43.317	61.191	83.628	5.52	5.8950×10^{-6}

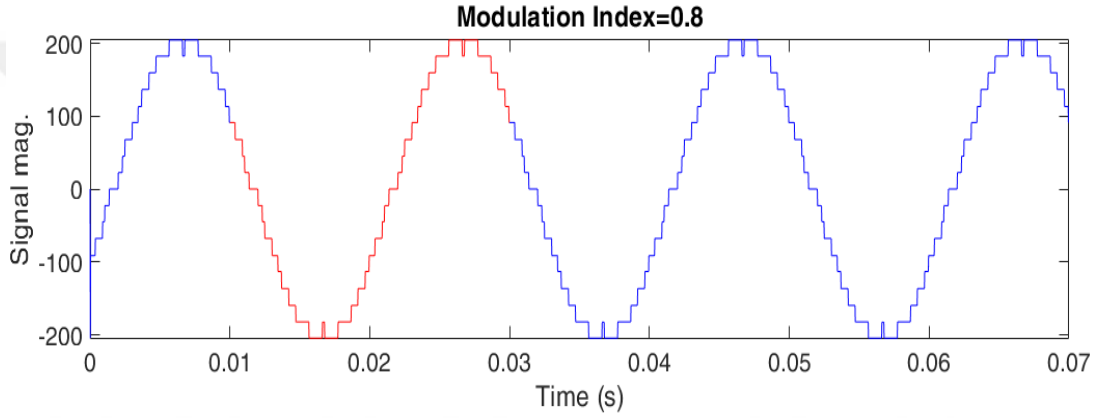

Figure 4.18 Line-to-line voltage output for m=0.8.

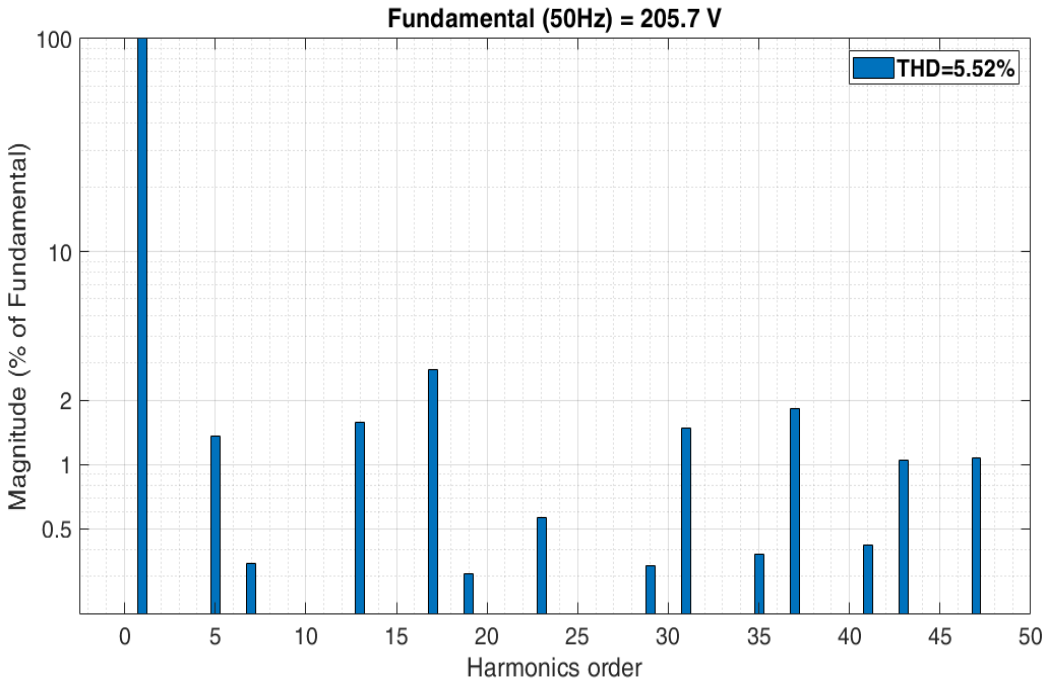

Figure 4.19 FFT analysis results of line voltage output for m=0.8.

4.3.3 Case Study for Modulation Index 1.0

Figure 4.20 shows the line-to-line voltage output for modulation index (m) 1.0, R load 120 Ω, and Figure 4.21 displays the Fast Fourier Transform (FFT) spectrum derived from the angles calculated by the Hybrid TLBO-WOA, as detailed in Tables 4.5.

Table 4.5 Results of algorithms for m=1.0.

Algorithm	Switching Angles (in degree)					THD	Fitness
	α_1	α_2	α_3	α_4	α_5		
TLBO	7.848	19.332	29.628	47.646	63.189	5.01	1.2657×10^{-5}
WOA	4.190	20.290	22.120	41.970	61.150	6.90	3.9300×10^{-2}
TLBO-WOA	7.821	19.359	29.574	47.610	63.198	4.96	7.8095×10^{-6}

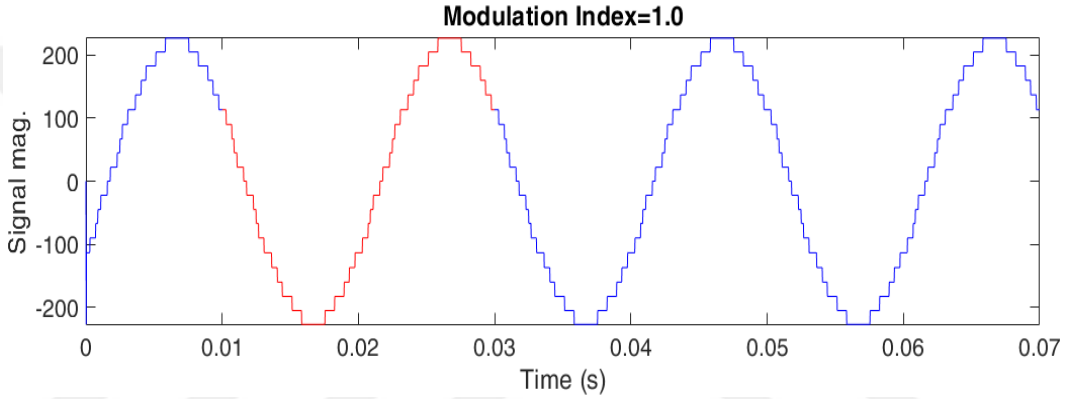

Figure 4.20 Line-to-line voltage output for m=1.0.

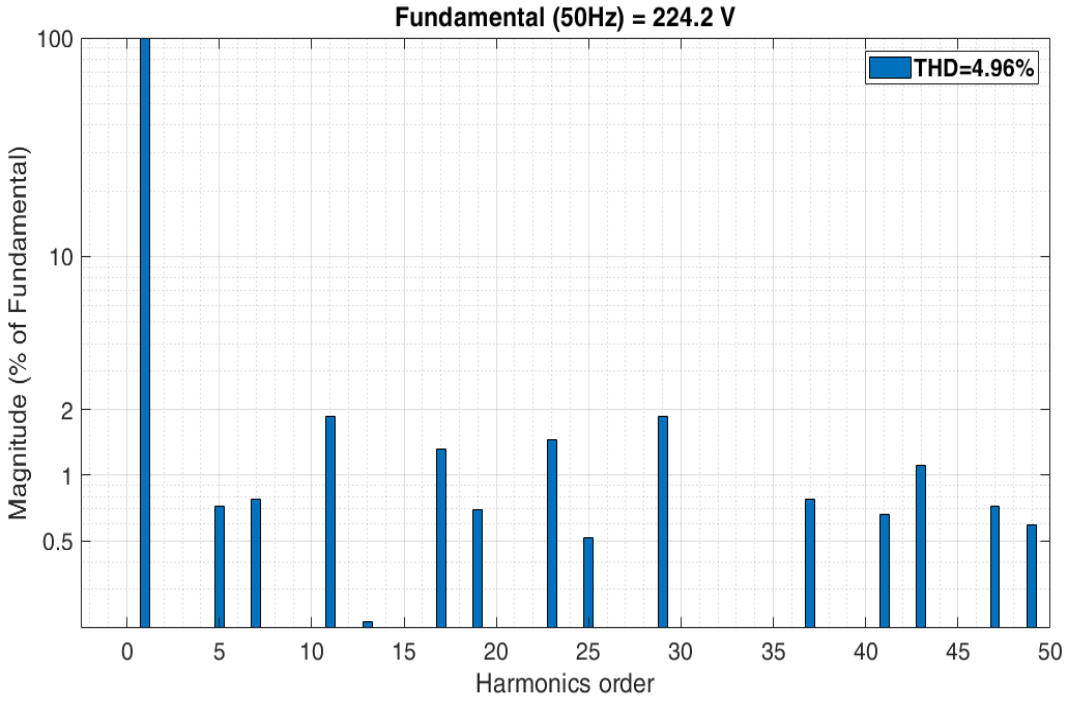

Figure 4.21 FFT analysis results of line voltage output for m=1.0.

Figure 4.22 shows the output voltage and current of 120 Ω R load with Δ-connected.

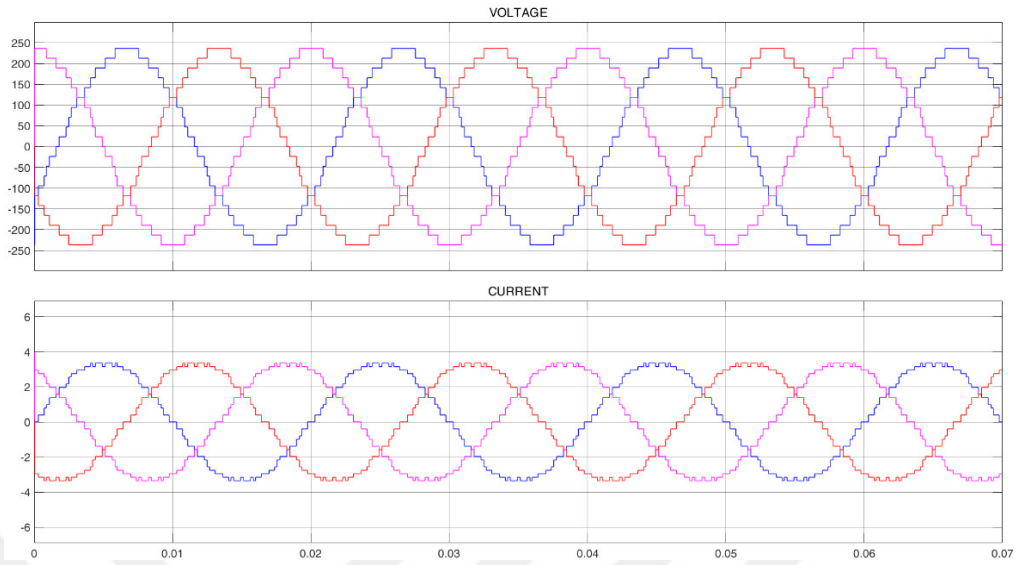

Figure 4.22 Output voltage and current of three-phase system with Δ-connected R load 120 Ω.

4.3.4 Case Study for RL Load

Figure 4.23 display FFT spectrum of line-to-line voltage with 120 Ω -100 mH RL load and Figure 4.24 shows the output line voltage and current of 120 Ω -100 mH RL load, with modulation index 1.0. THD value is 5.13% for RL load.

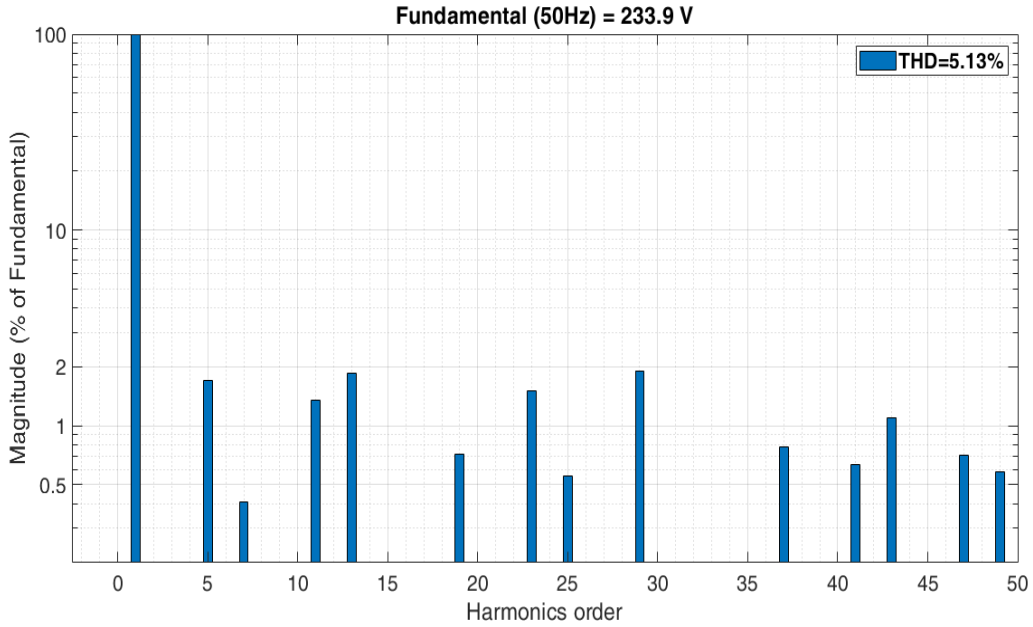

Figure 4.23 FFT spectrum of line-to-line voltage with RL load R=120 Ω, L=100 mH, modulation index=1.0.

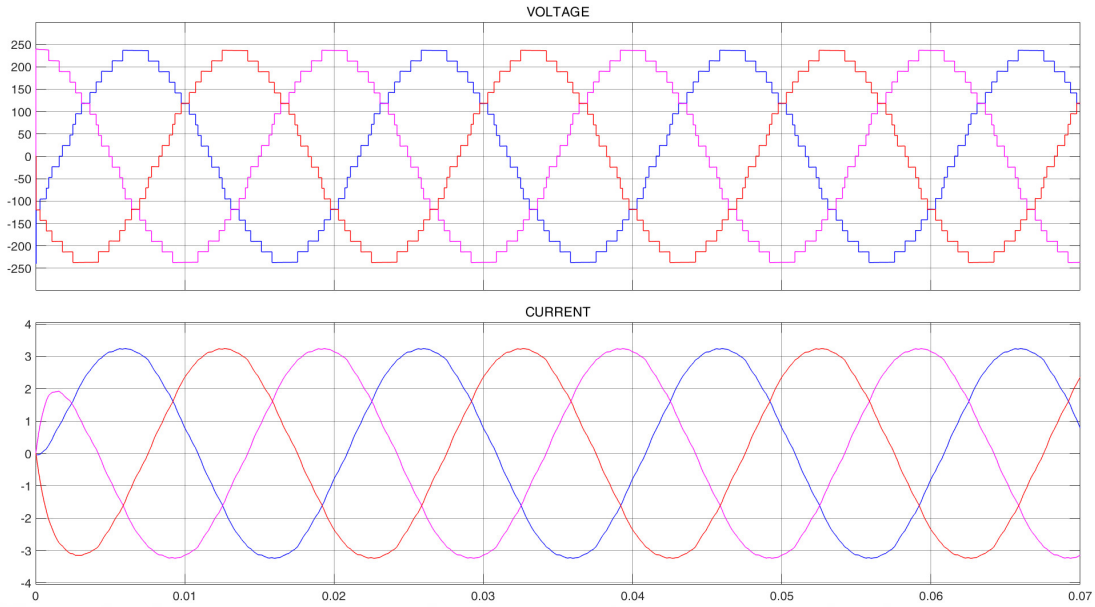

Figure 4.24 Output waveform of line-to-line voltage and current with RL load 120 Ω, 100 mH, modulation index=1.0.

4.4 Summary

The hybrid TLBO-WOA method has been built and executed offline using MATLAB to improve the switching angles for Selective Harmonic Elimination (SHE) in a reduced switch multilevel inverter (MLI). The MLI has been simulated using Simulink, which generated different voltage levels by utilizing identical voltage sources. For simulation investigation, the MLI has been connected to a 120 Ω resistor. In the simulation, a RL load consisting of a 120 Ω resistor and a 100 mH RL has been examined. A MATLAB®/Simulink program has been used to construct an 11-level three-phase MLI circuit. The performance of the TLBO-WOA method has been confirmed by implementing it in the MATLAB®/Simulink environment. A comparative analysis has been then undertaken to evaluate its performance in terms of convergence and solution quality, in comparison to other optimization algorithms. Case studies have been done to analyze the modulation indices of 0.6, 0.8, and 1.0, as well as the impact of RL loads.

CHAPTER 5
EXPERIMENTAL RESULTS

5.1 Introduction

A laboratory prototype has been developed to verify the performance of the proposed TLBO-WOA optimized reduced switch 11-level three-phase MLI. The block diagram of the hardware setup is shown in Figure 5.1. The parameters used in the experiment have been listed in Table 5.1. A Texas Instruments®-TMDS-DOCK-28335 digital signal processor has been used to implement PWM signals. Fluke-435-II Power Quality Analyzer has been used for calculation THD in experimental analysis. Logic analyzer has been used for showing gate signals of MLI. MLI is connected to the resistor of value 120 Ω for experimental analysis. Also, dynamic load test has been done from 120 to 40 Ω and 40 to 120 Ω in experimental design.

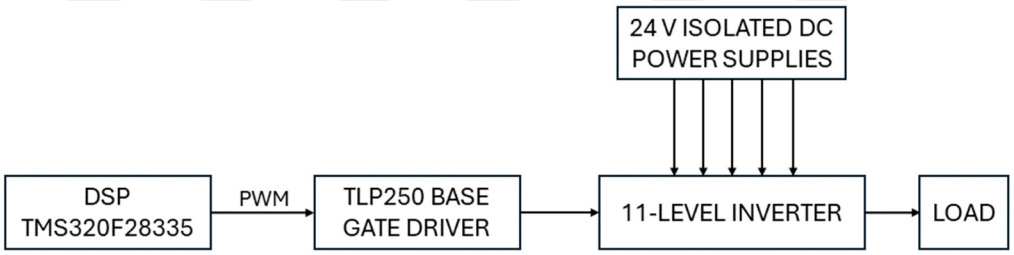

Figure 5.1 Block diagram of the hardware setup.

Table 5.1 Components used for experiment.

S. No.	Parameters/Components	Specifications	No. of Component
1.	Isolated DC power supply	24 V	15
2.	MOSFET	IRFB4227	36
3.	Gate Driver	TLP250	36
4.	DSP	TMS320F28335 (TI)	1
5.	Load	120 Ω, Δ connected	3

5.2 Hardware Implementation

The hardware module implemented here is a modified reduced switch H-bridge MLI. This experimental setup is developed to reveal the effectiveness of the reduced switch MLI. For developing the hardware setup, an electronic design automation software for printed circuit boards (PCB) is used.

5.2.1 Schematic Design

The schematic design involves creating a detailed circuit diagram of 11-level reduced switch MLI has been completed with computer aided electronic design automation sofware which shows the connections between all components . Figure 5.2 illustrates the each level of MLI.

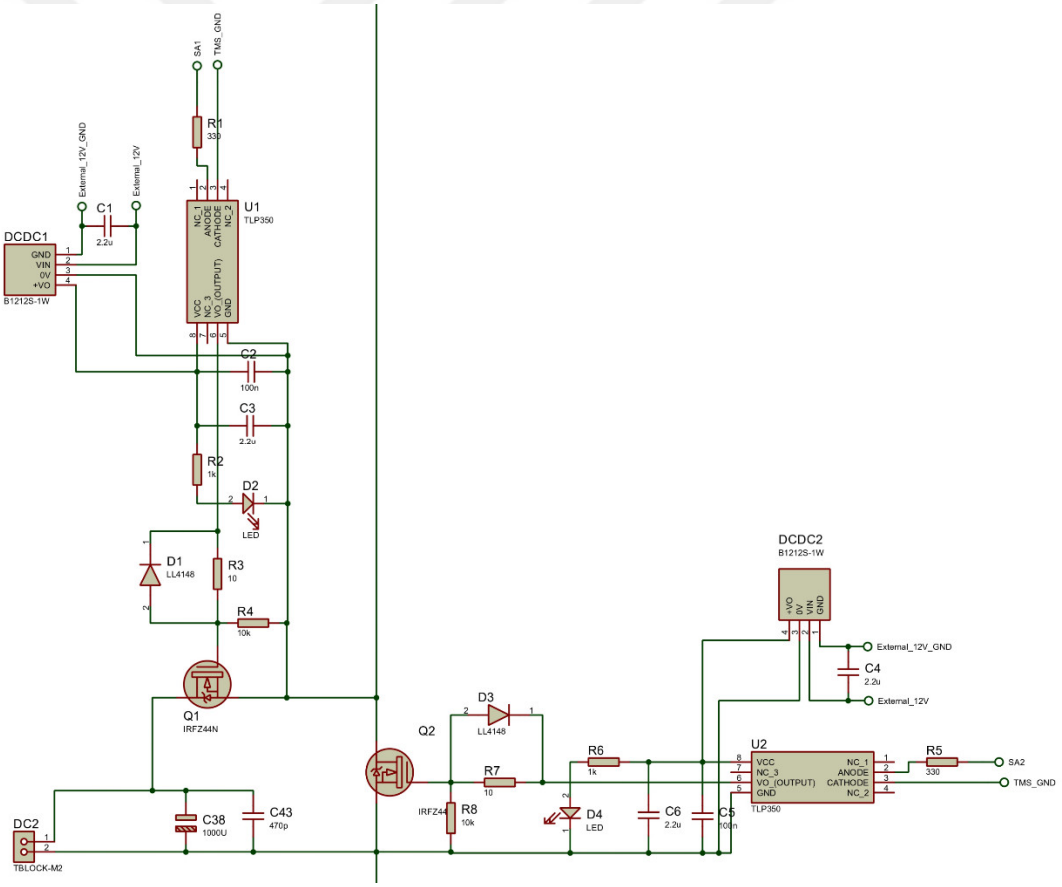

Figure 5.2 Block diagram for each level of MLI.

Figure 5.3 illustrates the block diagram for H-bridge of MLI.

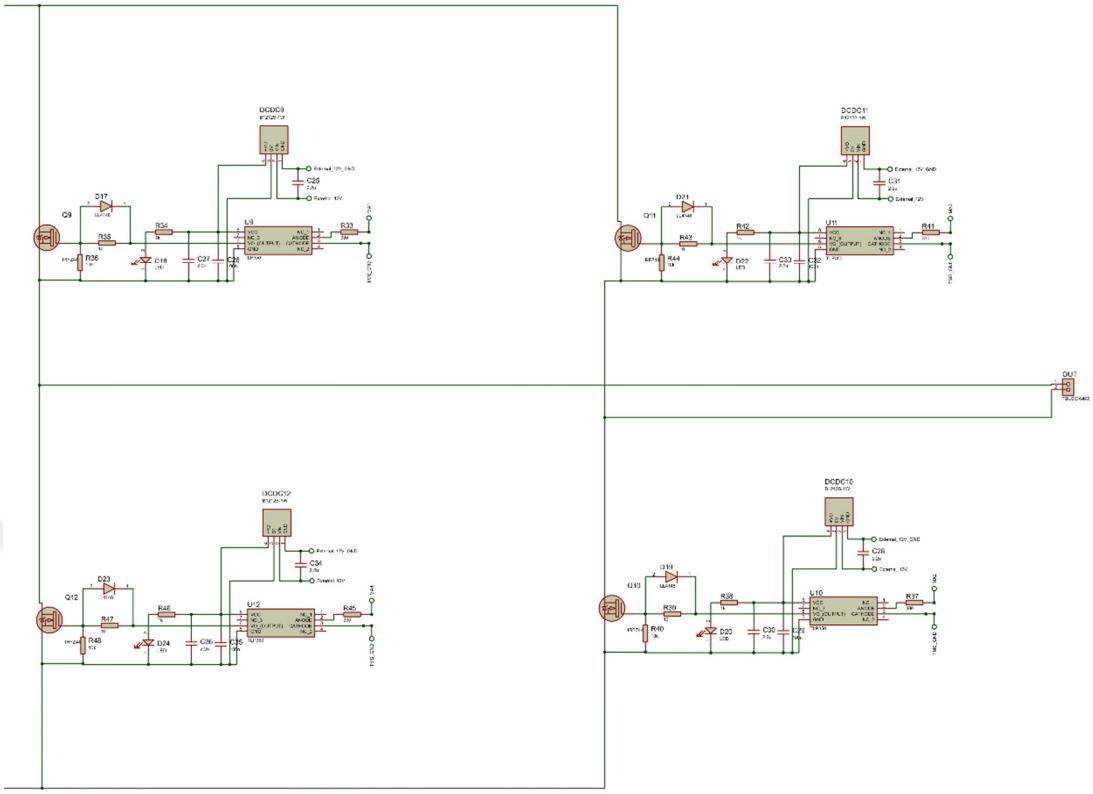

Figure 5.3 Block diagram for H-bridge of MLI.

5.2.2 PCB Design

The PCB layout is designed with the following considerations: Power and Signal Separation, Thermal Management, Ground Planes. A PCB layout of 11-level reduced switch MLI hardware module is demonstrated in Figure 5.4.

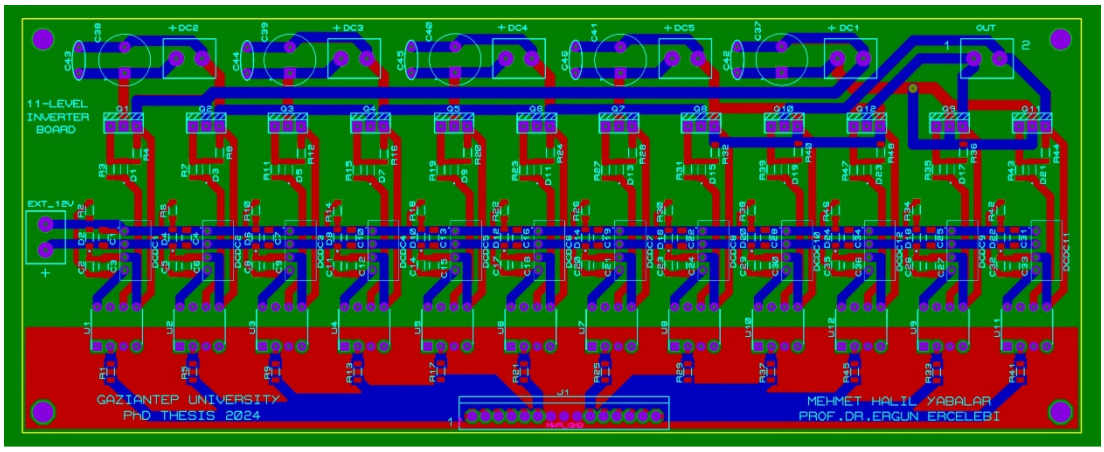

Figure 5.4 PCB layout of 11-level reduced switch MLI.

Figure 5.5, 5.6, and 5.7 demonstrate the developed PCB circuit of front view, top view, and back view recpectively in 3D.

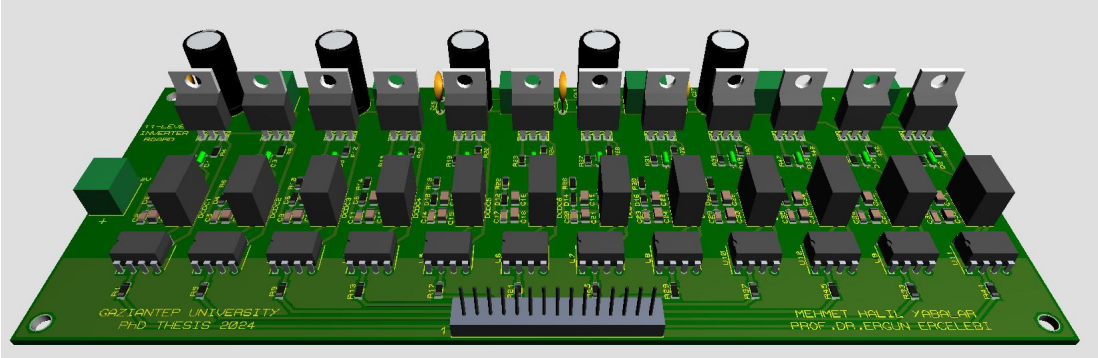

Figure 5.5 Front 3D view of power board.

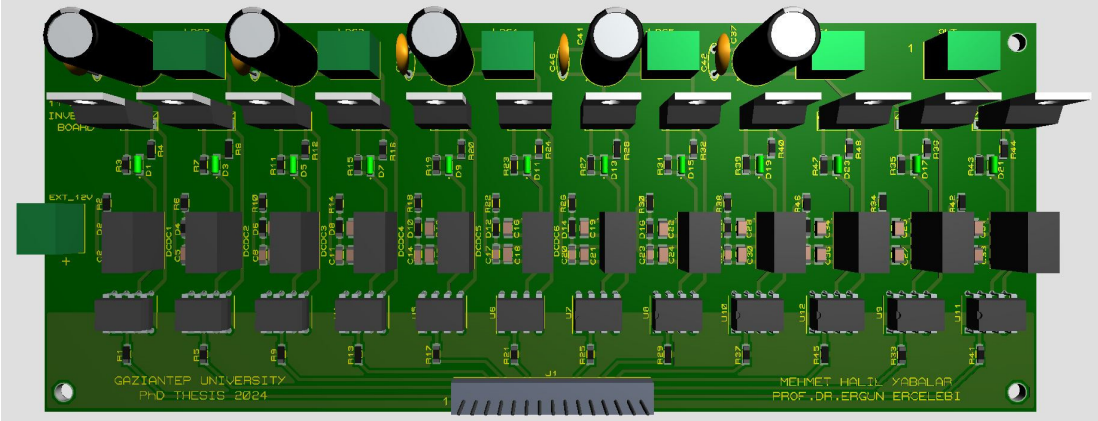

Figure 5.6 Top 3D view of power board.

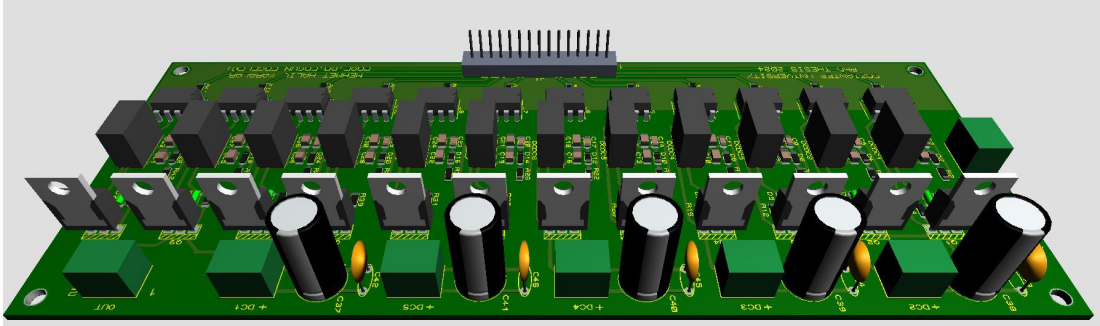

Figure 5.7 Back 3D view of power board.

Figure 5.8 demonstrates the developed circuit for each phase after mounting the components on the surface of PCB. Each component is chosen carefully to fit properly in the exact location in the circuit.

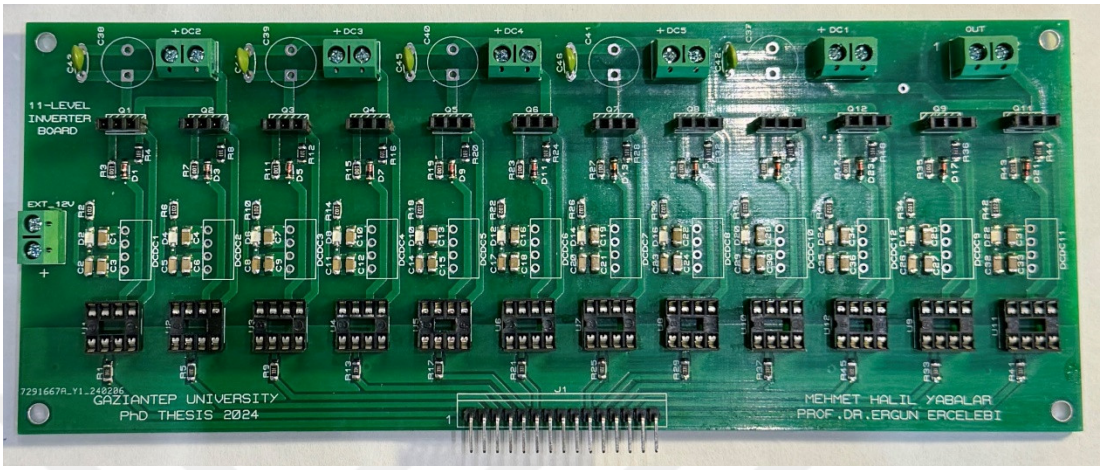

Figure 5.8 Top view of a PCB with some components mounted in real life.

The PCB layout is built taking into account the following factors:

- **Power and Signal Segregation:** The high-power and low-power signal lines are kept apart to minimize the presence of unwanted noise and interference.
- **Thermal Management:** Components that produce substantial heat are strategically positioned to optimize cooling efficiency.
- **Ground planes** are widely utilized to minimize electromagnetic interference (EMI) and enhance signal integrity.

5.2.3 Experimental Setup Design

The photograph of hardware setup and experimental setup are shown in Figure 5.9 and Figure 5.10, respectively. Using isolated DC power supply is critical to designing to avoid short-circuit on common point. Fuses have been used to protect circuit board and power supplies from overload and short-circuit case. The hardware setup has been provided with 12 switches for each phase, and totally 36 switches required for three phsae MLI. There are also five AC/DC isolated power supplies for supplying the levels. Moreover, Texas Instruments® F28335 Experimental kit has been used to generate PWM for the 36 switches. An illustration of SPWM is provided in Figure 5.10 on the monitor using logic analyzer.

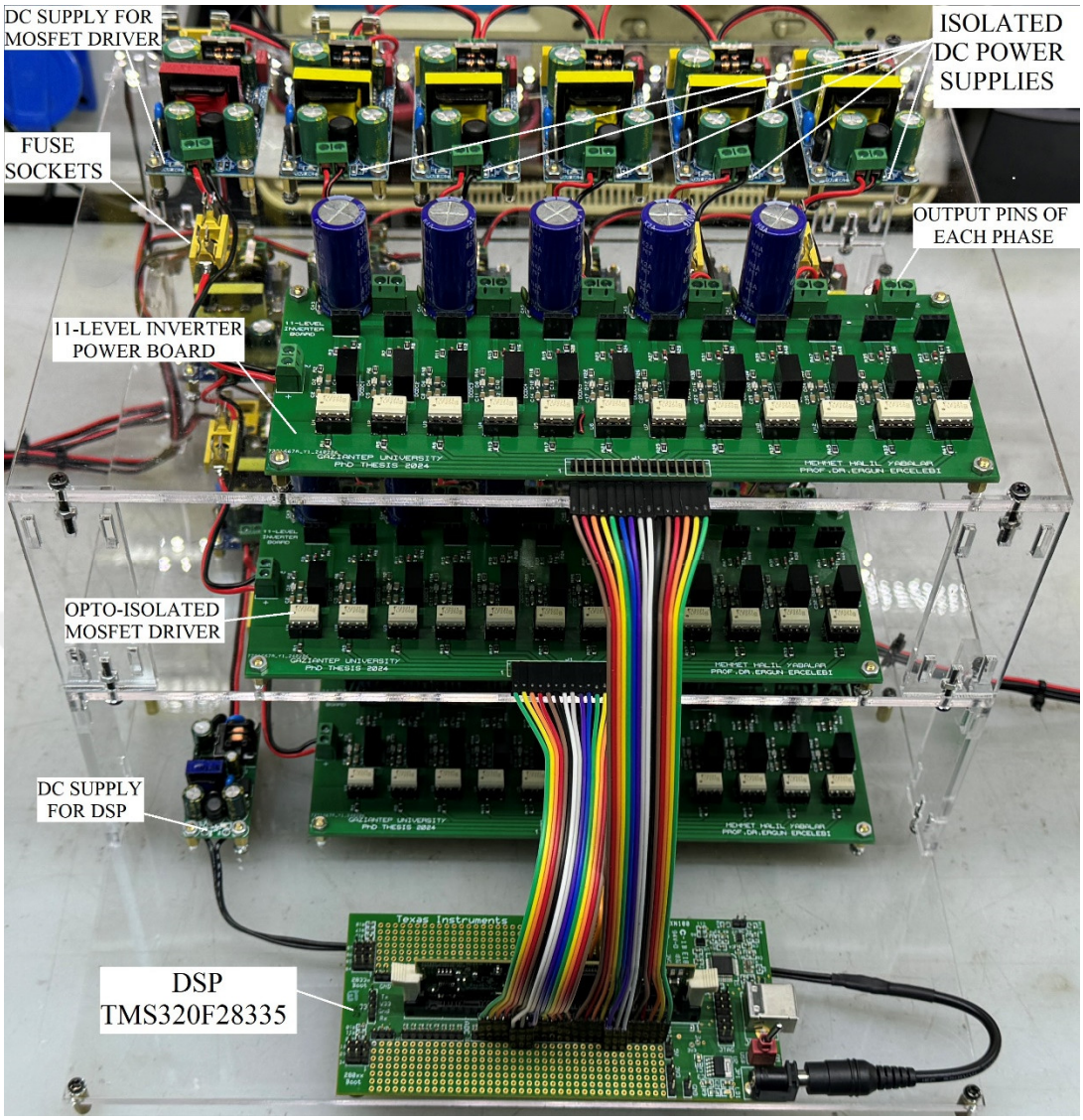

Figure 5.9 Photograph of the hardware setup.

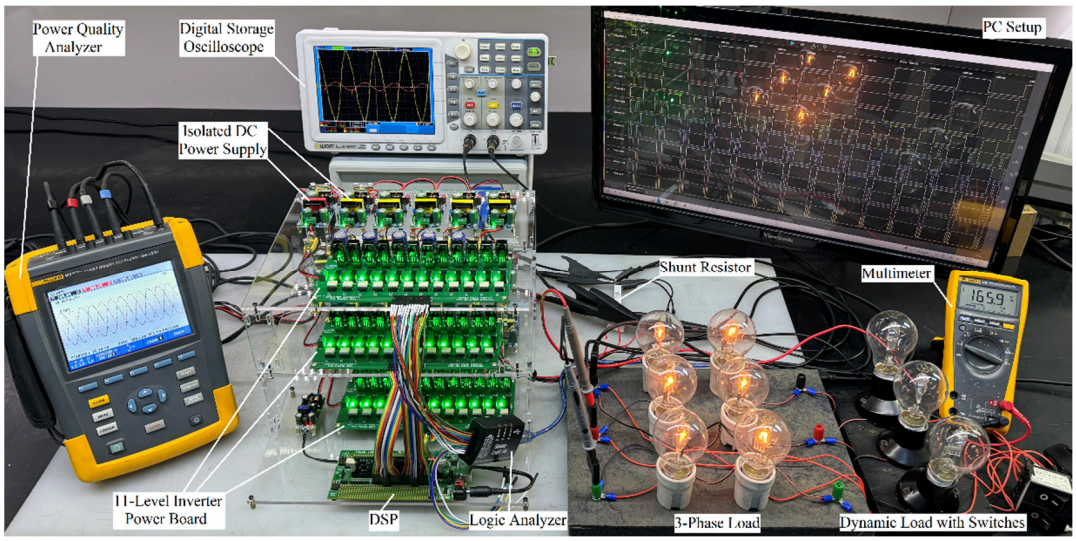

Figure 5.10 Photograph of the experimental setup.

Figure 5.11 showcases the DSP board, namely the Texas Instrument TMS320F382335 experimental kit. The purpose of this board is to serve as a development platform for assessing and creating prototypes of applications utilizing TMS320F28335 microcontroller, which is a member of the C2000 family. The microcontroller is highly suitable for real-time control applications because of its robust processing capabilities, seamless integration of peripherals, and user-friendly interface.

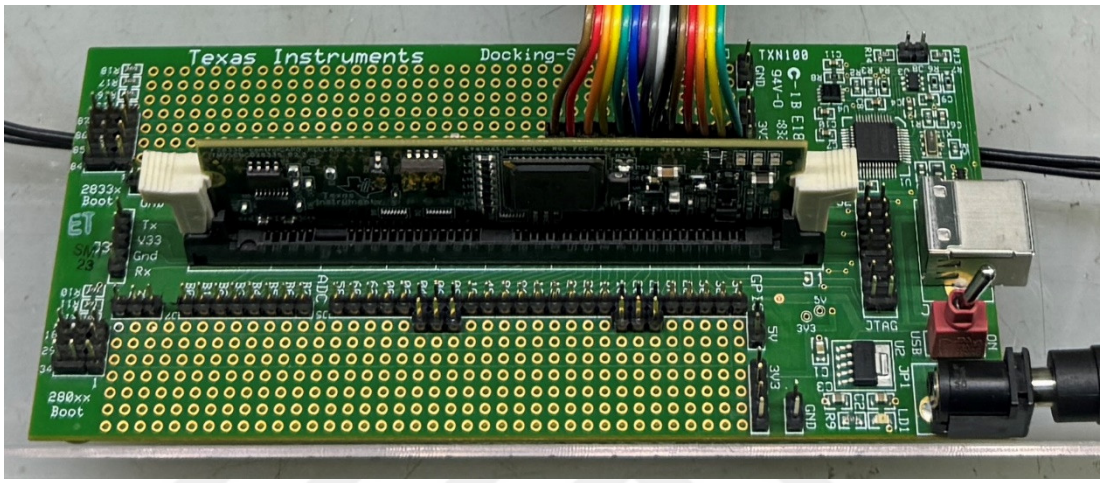

Figure 5.11 Photograph of the Texas Instruments TMS320F28335 experimenter kit.

5.3 Experimental Validation

Figure 5.12 illustrates the experimental results of gate signals from logic analyzer for single phase power board.

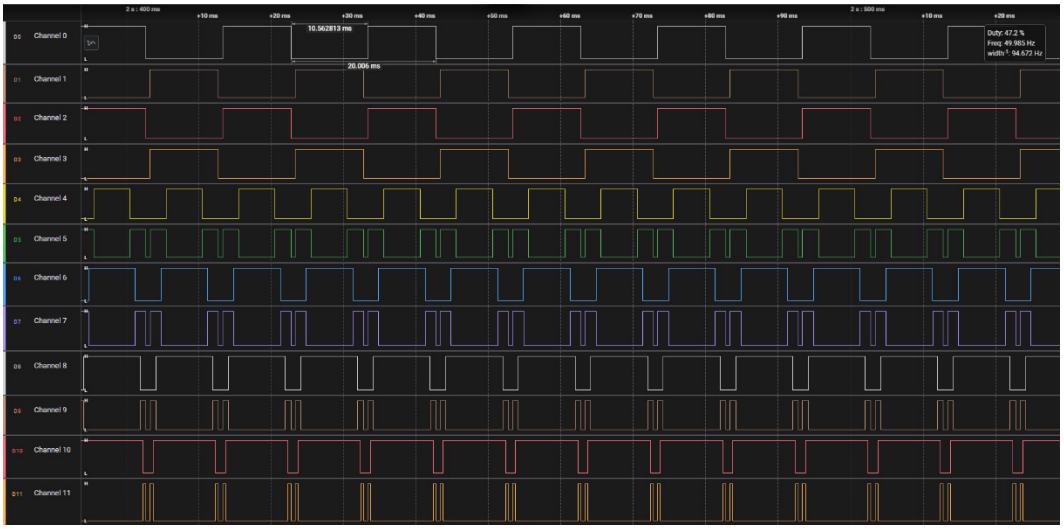

Figure 5.12 Gate signals of 11-level reduced switch MLI for experimental results.

5.3.1 Experimental Case Study for Modulation Index 0.6

Experimental line-to-line voltage results show that 125.54 V_{RMS} and 6.6% THD for modulation index 0.6 in Figure 5.13 and 5.14. Also, frequency is 49.983 Hz.

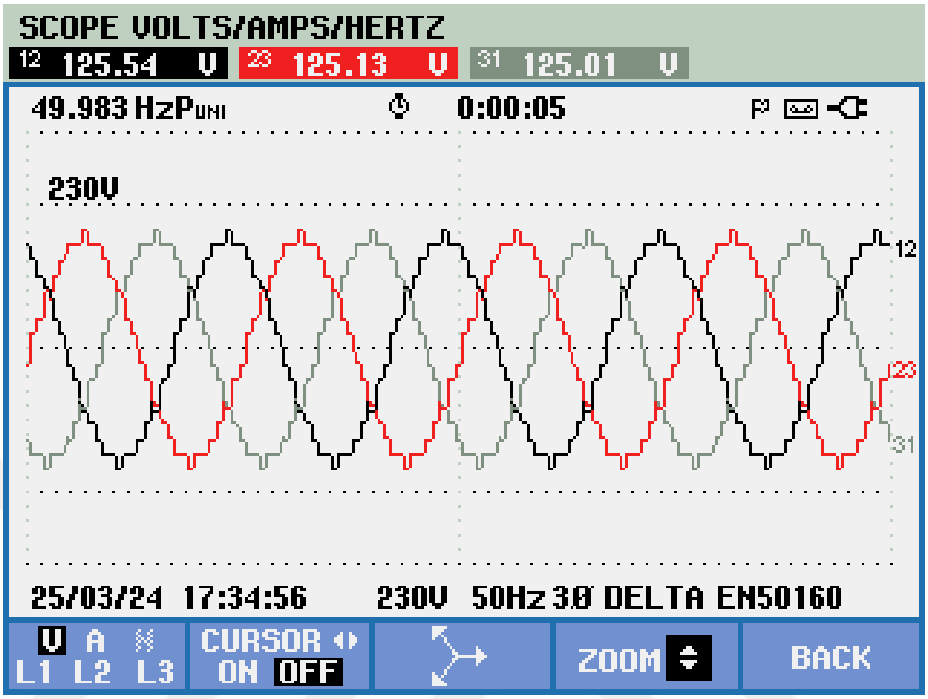

Figure 5.13 Experimental line-to-line voltage output for m=0.6.

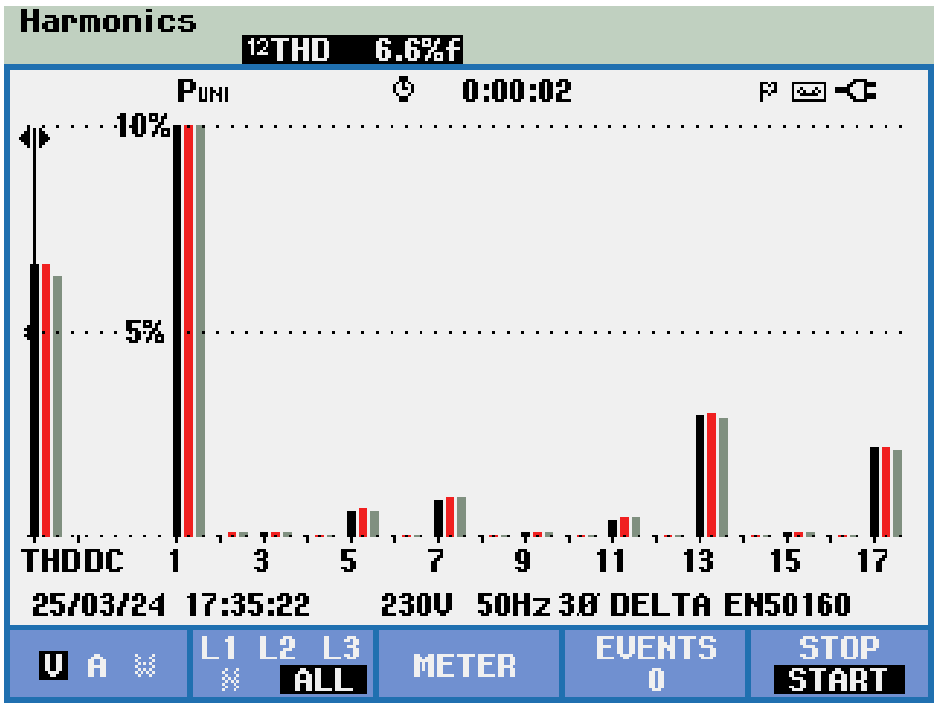

Figure 5.14 FFT spectrum for modulation index 0.6 with 120 Ω load.

Experimental line-to-line voltage phasor diagram has been depicted in Figure 5.15 for modulation index 0.6. Also, Figure 5.16 shows the oscilloscope view of line-to-line voltage for L1-L2 (yellow signal) and current measurement for L3 (red signal). Line current's peak value is 1.698 A, so RMS value of line current is 1.2 A.

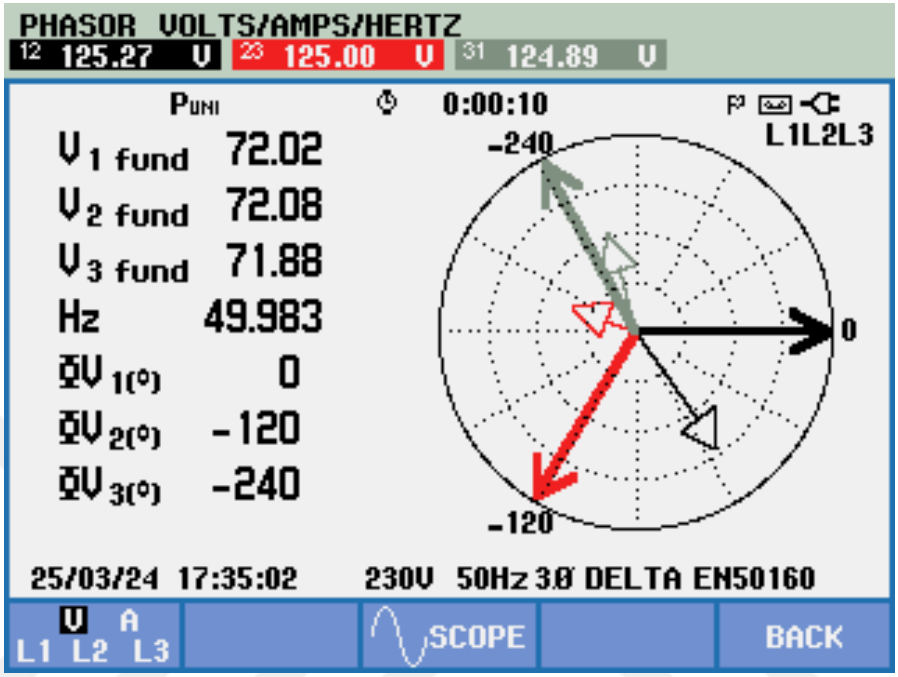

Figure 5.15 Phasor diagram for modulation index 0.6 with 120 Ω load.

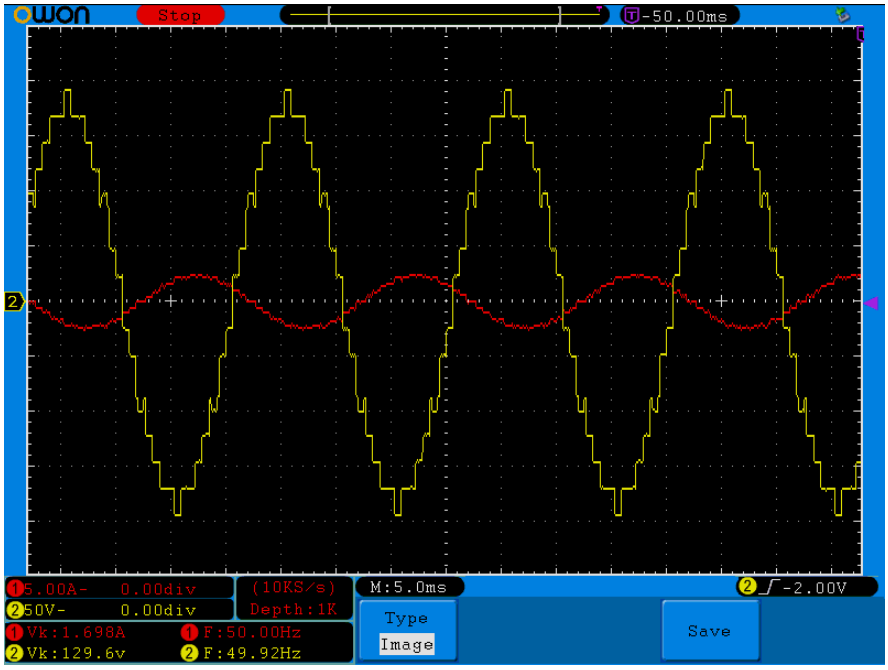

Figure 5.16 Oscilloscope view of line-to-line voltage and current for m=0.6.

5.3.2 Experimental Case Study for Modulation Index 0.8

Experimental line-to-line voltage results show that 152.16 V_{RMS} and 5.8% THD for modulation index 0.8 in Figure 5.17 and 5.18. Also, frequency is 49.983 Hz.

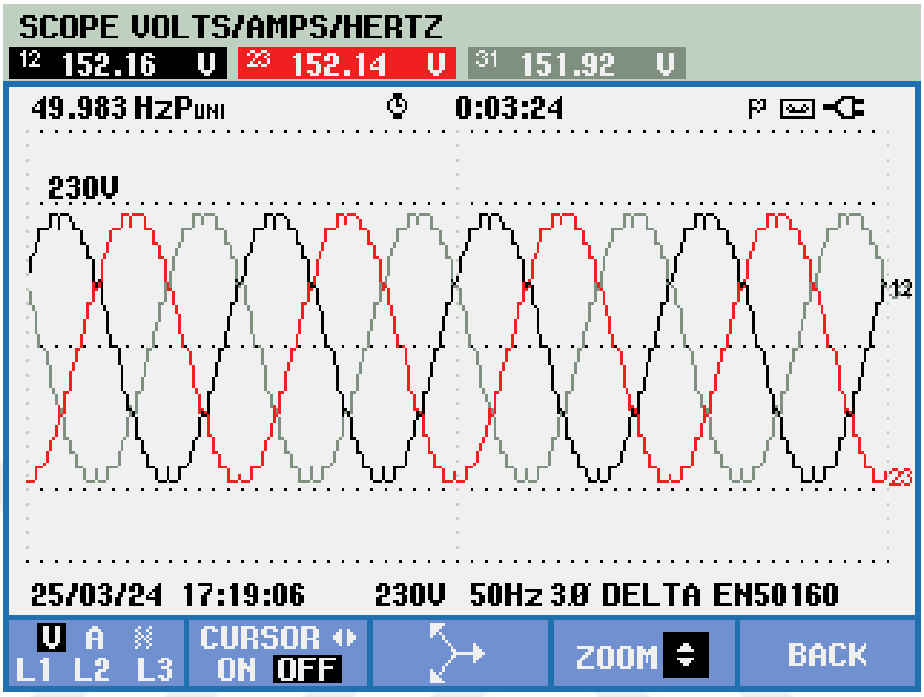

Figure 5.17 Experimental line-to-line voltage output for m=0.8.

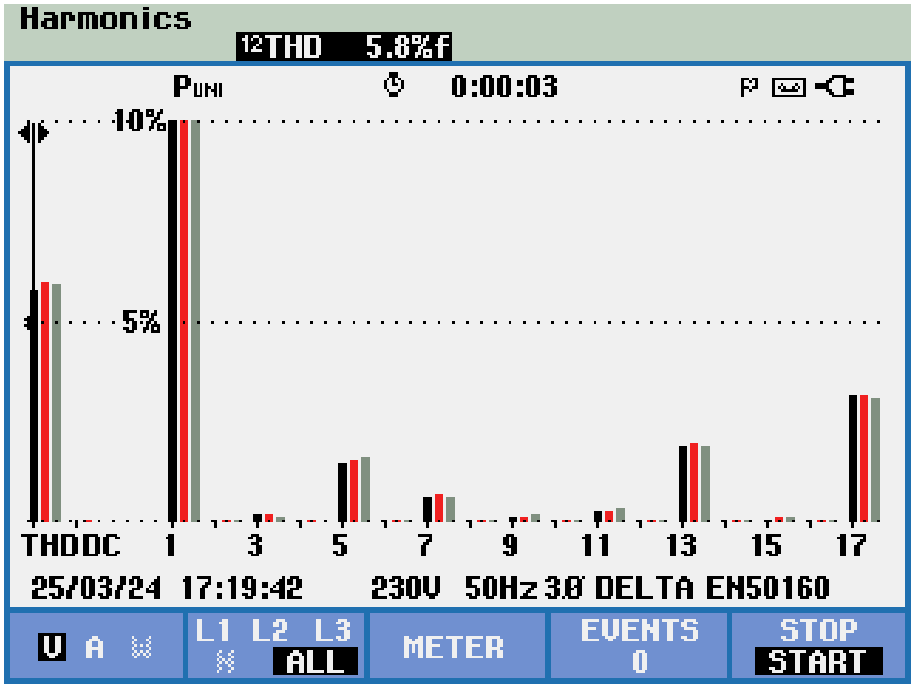

Figure 5.18 FFT spectrum for modulation index 0.8 with 120 Ω load.

Experimental line-to-line voltage phasor diagram has been depicted in Figure 5.19 for modulation index 0.8. Also, Figure 5.20 shows the oscilloscope view of line-to-line voltage for L1-L2 (yellow signal) and current measurement for L3 (red signal). Line current's peak value is 1.851 A, so RMS value of line current is 1.309 A.

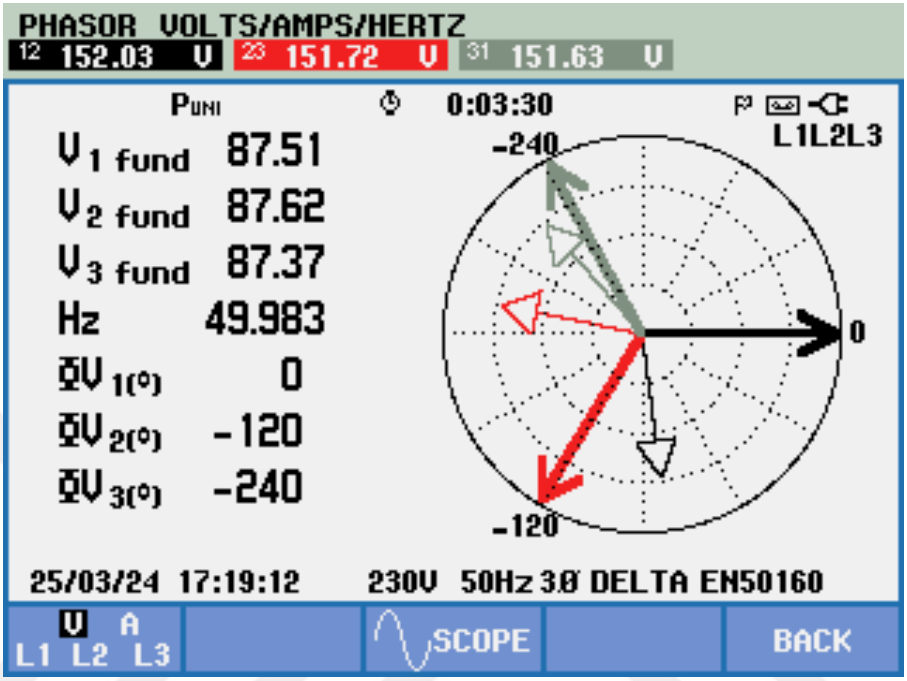

Figure 5.19 Phasor diagram for modulation index 0.8 with 120 Ω load.

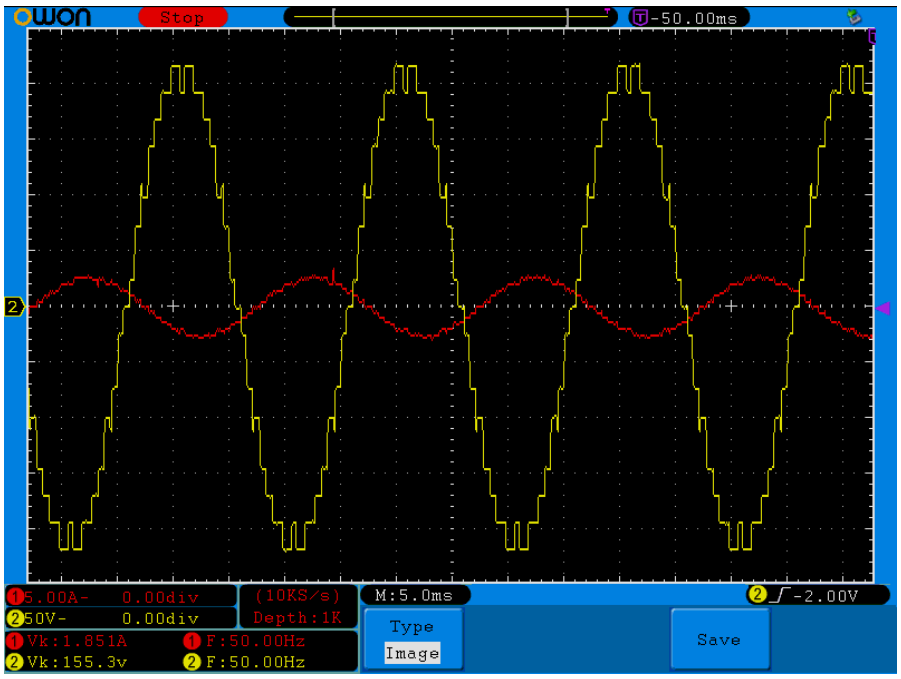

Figure 5.20 Oscilloscope view of line-to-line voltage and current for m=0.8.

5.3.3 Experimental Case Study for Modulation Index 1.0

Experimental line-to-line voltage results show that 165.98 V_{RMS} and 4.9% THD for modulation index 1.0 in Figure 5.21 and 5.22. Also, frequency is 49.983 Hz.

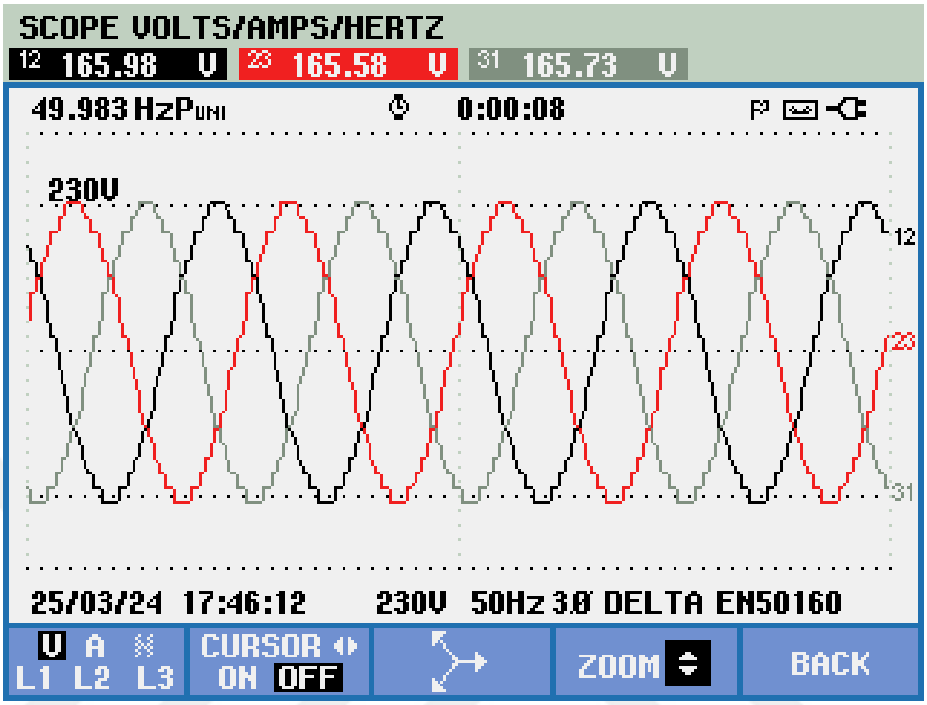

Figure 5.21 Experimental line-to-line voltage output for m=1.0.

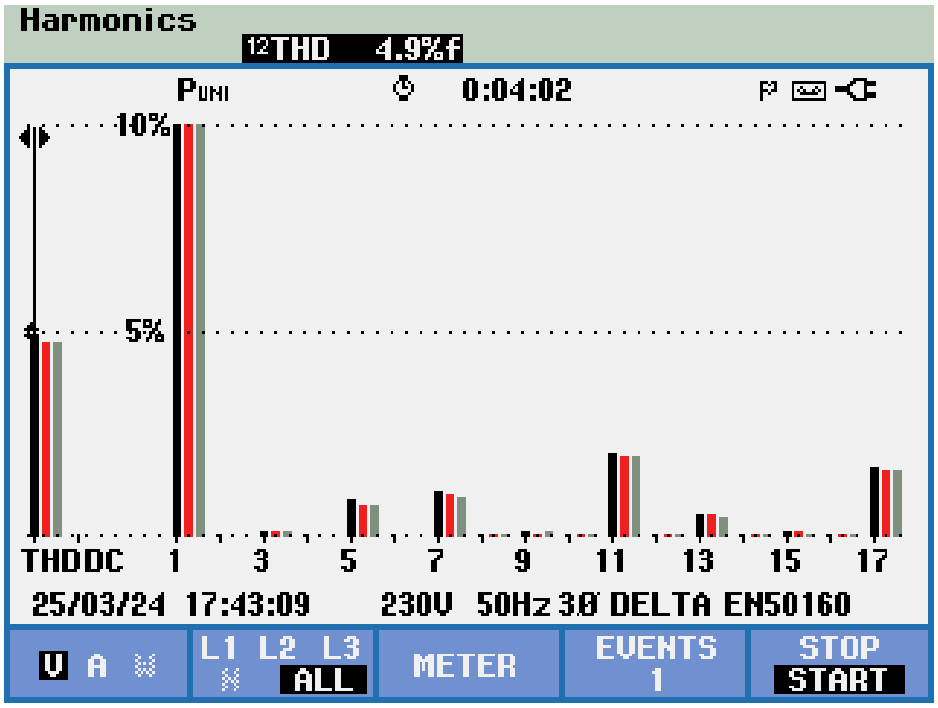

Figure 5.22 FFT spectrum for modulation index 1.0 with 120 Ω load.

Experimental line-to-line voltage phasor diagram has been depicted in Figure 5.23 for modulation index 1.0. Also, Figure 5.24 shows the oscilloscope view of line-to-line voltage for L1-L2 (yellow signal) and current measurement for L3 (red signal). Line current's peak value is 1.957 A, so RMS value of line current is 1.384 A.

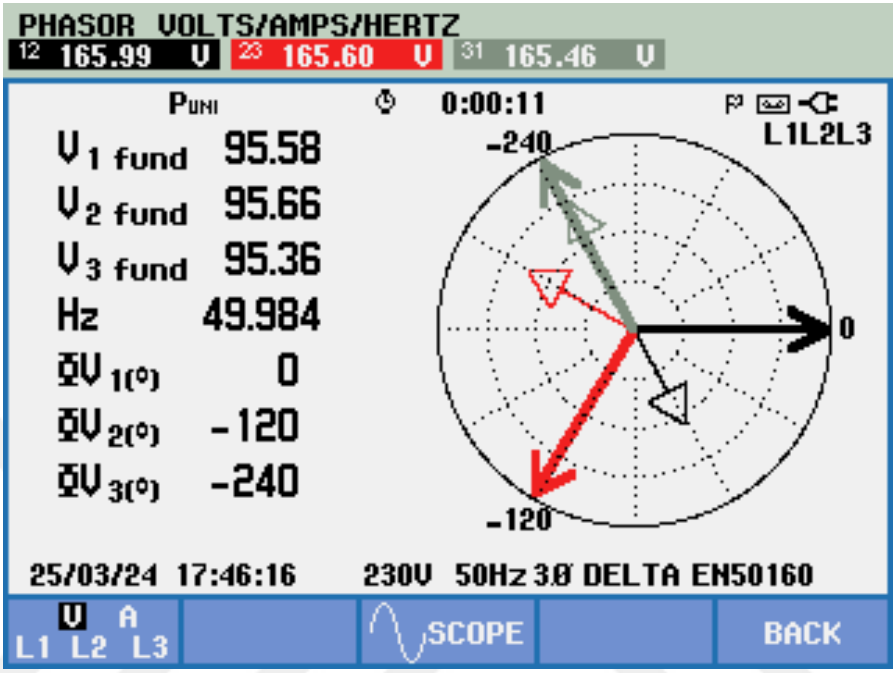

Figure 5.23 Phasor diagram for modulation index 1.0 with 120 Ω load.

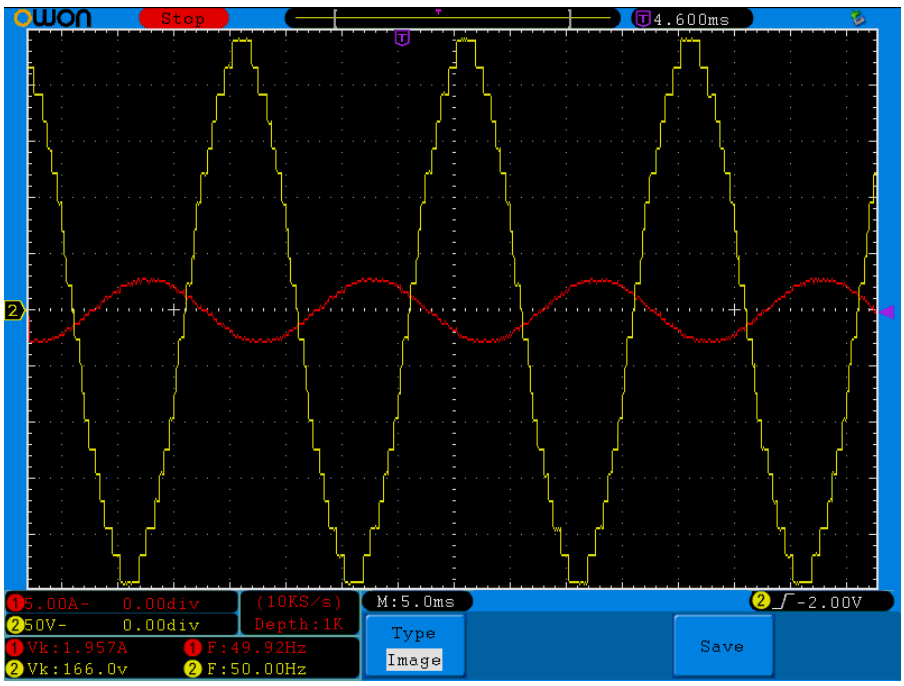

Figure 5.24 Oscilloscope view of line-to-line voltage and current for m=1.0.

It has been clear seen that oscilloscope view of line-to-line voltage 166 V_{RMS} and current 1.957 A of line with shunt resistor 0.1 Ω on Fig 5.24. Also, the multimeter shows the line-to-line voltage which is 165.9 V_{RMS} in Figure 5.10. Additionally, Figure 5.15, 5.19, 5.23 shows that phasor diagram confirms 120° phase difference between each line.

5.3.4 Dynamic Performance of the System

The dynamic performance of the system is validated through experimentation. The load resistance has been changed from 120 to 40 Ω to verify the dynamic behavior. It can be observed from Figure 5.25 that due to a decrease in load resistance, the output peak current increases from 1.957 to 5.871 A. Also, it can be seen from Figure 5.26 that due to an increase in load resistance, the output peak current decreases from 5.871 to 1.957 A. However, the output voltage remains at 165 V. Hence, the load change does not have any effect on the output voltage.

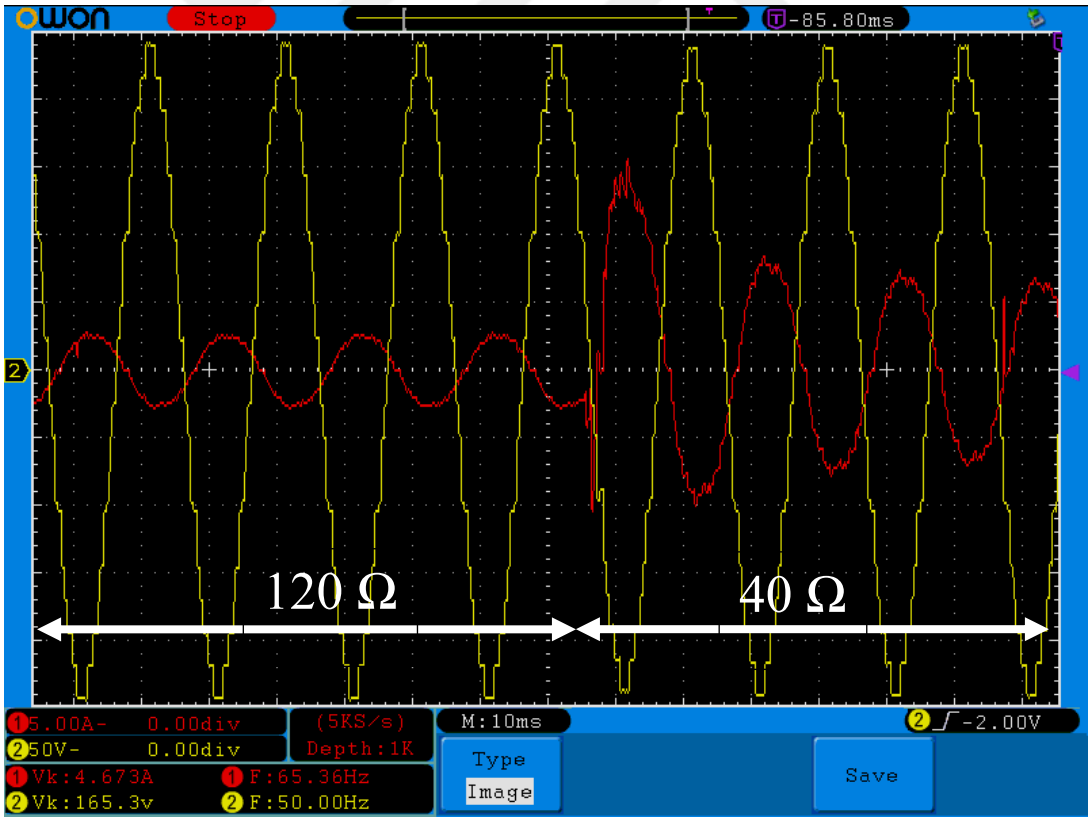

Figure 5.25 Dynamic load change from R=120 Ω to R=40 Ω.

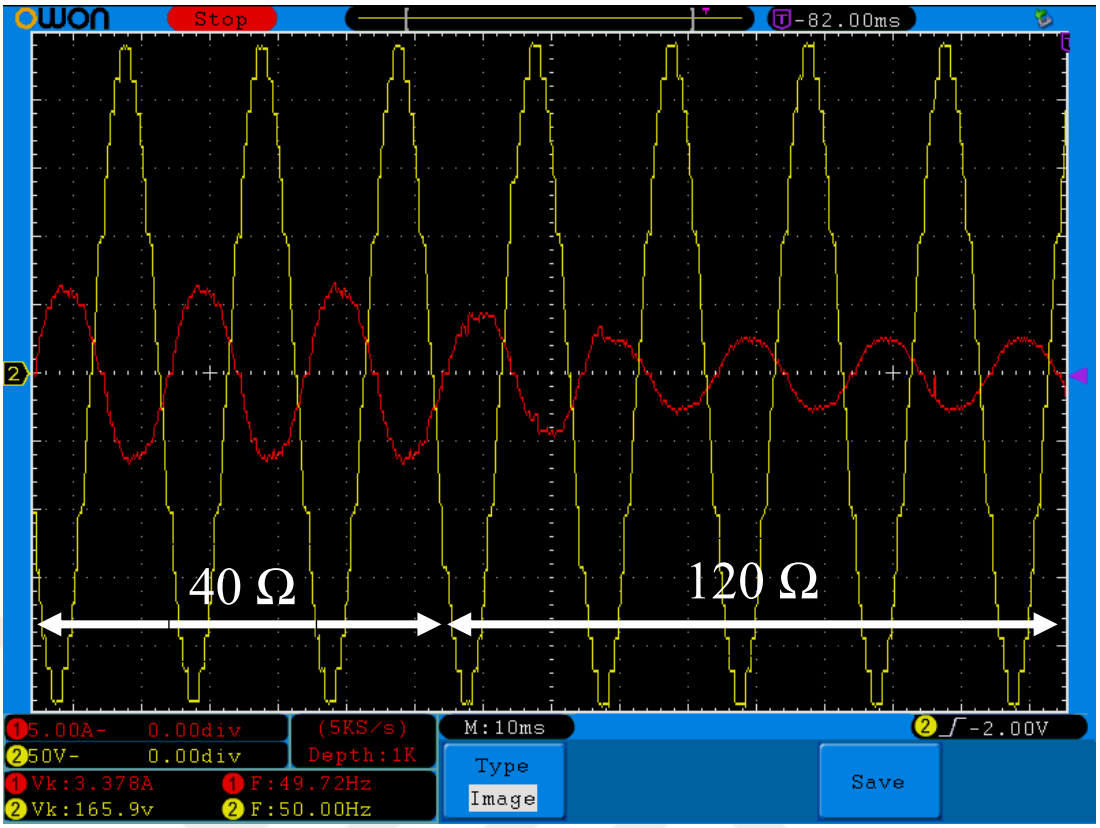

Figure 5.26 Dynamic load change from R=40 Ω to R=120 Ω.

5.4 System Efficiency

The system efficiency of a three-phase multilevel inverter is a crucial factor that influences the effectiveness of converting DC power to AC power while reducing losses. Below is an elaborate elucidation of the variables influencing efficiency and techniques for computing and enhancing it. Factors affecting efficiency:

- Switching losses refer to the energy dissipated during the transition of power semiconductors, such as MOSFETs or IGBTs, from the on state to the off state and vice versa. The magnitude of these losses is contingent upon the switching frequency, the voltage applied across the switch, and the current flowing through it.
- Conduction losses refer to the power dissipated by the semiconductors when they are in the on state. These quantities are directly proportional to the magnitude of the electric current passing through the device and the resistance or voltage drop experienced while the device is in the on-state.
- Passive component losses refer to the energy dissipation that occurs in inductors, capacitors, and resistors when they are utilized for the purposes of

filtering and energy storage. The performance of these components relies on their quality and design.

- Control and Gate Drive Losses: This refers to the power consumption of the microcontroller or DSP, as well as the gate driver circuits that control the switching devices.
- Thermal management losses occur when heat dissipation is not effectively managed, necessitating the use of efficient cooling technologies. Poor thermal management can result in elevated junction temperatures, which in turn can cause an increase in the on-state resistance and switching losses of power devices.

Calculation of Efficiency:

The efficiency (η) of a three-phase multilevel inverter is calculated as the ratio of the output power (P_{out}) to the input power (P_{in}), expressed as a percentage:

$$\eta = \left(\frac{P_{out}}{P_{in}}\right) \times 100\% \tag{5.1}$$

Measure Input Power (P_{in}):

- Calculate the power supplied to the inverter.
- V_{in} is the input voltage and I_{in} is the input current.

$$P_{in} = V_{in} \times I_{in} \tag{5.2}$$

Measure Output Power (P_{out}):

- Calculate the power delivered to the load.
- V_L is the line voltage, I_L is the line current, and cos(φ) is the power factor of the load.

$$P_{out} = \sqrt{3} \times V_L \times I_L \times \cos(\varphi) \tag{5.3}$$

Determine Losses (P_{loss}):

- This includes switching losses, conduction losses, passive component losses, and control losses.

$$P_{loss} = P_{in} - P_{out} \tag{5.4}$$

For this study, the input power has been calculated from the AC side of isolated AC/DC power supplies, as 15 isolated power supplies has been used. Measuring the DC side would require 15 DC ammeters, and this is not a practical way. Therefore, AC side power consumption has been used to determine efficiency. Also, the output power has been calculated from load side. This difference shows only total loss in the system. This test has been applied to resistive load, so power factor is 1.0. Figure 5.24 verify that peak value of each phase current is 1.957, so RMS value of output current is 1.384 A. Output voltage is 165.9 V_{RMS}. Also, the load is 120 **Ω**, Δ connected. Table 5.2 shows the parameters for calculating efficiency.

Table 5.2 Given data for calculation efficiency.

Parameter Name	Value
Input Voltage	225.4 V
Input Current	1.834 A
Input Power	**413.38 W**
Output Voltage	165.9 V
Output Current	1.384 A
Output Power	**397.69 W**

Total loss has been calculated in Equation 5.6, and efficiency has been calculated in Equation 5.6.

$$P_{loss} = P_{in} - P_{out} \ = 413.38 \text{ W} - 397.69 \text{ W} = 15.69 \text{ W} \tag{5.5}$$

$$\eta = \left(\frac{397.69 \text{ W}}{413.38 \text{ W}}\right) \times 100\% = 96.2\ \% \tag{5.6}$$

5.5 Summary

A laboratory prototype of an optimized 11-level three-phase multilevel inverter (MLI) with reduced switch has been created and examined. The performance was thoroughly confirmed by utilizing a Texas Instruments®-TMDS-DOCK-28335 digital signal processor for generating PWM signals and a Fluke-435-II Power Quality Analyzer for measuring Total Harmonic Distortion (THD). The thorough procedure encompassed the implementation of hardware, the design of schematic and PCB, and the setup and validation of experiments. The efficacy of the TLBO-WOA optimized design has been confirmed through various experimental case studies done for modulation indices of 0.6, 0.8, and 1.0. These investigations also included evaluations of dynamic performance and system efficiency.

CHAPTER 6
COMPARASION OF RESULTS

Several algorithms including the Modified Dingo Optimization Algorithm (mDOA) [38], Black Window Optimization Algorithm (BWOA) [42], Grey Wolf Optimization Algorithm (GWOA) [38], Jumping Spider Optimization Algorithm (JSOA) [28], Modified Grey Wolf Optimization Algorithm (MGWOA) [43], Mexican Axolotl Optimization (MAO) [44], Chaos Game Optimization (CGO) [45], Coot Bird Algorithm (COOT) [46], Golden Eagle Optimizer (GEO) [47], and Harris Hawks Optimization (HHO) [48] have been selected for a detailed comparative analysis in Table 6.1, 6.2, 6.3. These selected algorithms have been applied 11-level three phase circuit with different topology. The nearly optimal angles derived from these algorithms have been input into a Simulink to generate the staircase output waveform. Subsequently, THD has been calculated, and a Fourier spectrum has been produced to verify the effective minimize of undesirable low-order harmonics.

Table 6.1 Results of comparative analysis for SHE problem (m=0.6).

Algorithm	**Switching Angles (in degree)**					**THD**	**Fitness**
	α_1	α_2	α_3	α_4	α_5		
mDOA	35.420	46.940	58.570	72.670	87.850	6.79	4.1500×10^{-27}
BWOA	35.440	46.950	58.580	72.610	87.860	6.82	4.1900×10^{-27}
GWOA	35.290	46.800	58.450	72.460	87.740	6.87	2.7800×10^{-4}
WOA	35.350	46.890	58.490	72.440	87.700	6.87	8.1700×10^{-5}
TLBO	35.388	46.010	57.564	70.263	85.959	7.05	6.5267×10^{-8}
TLBO-WOA	**35.343**	**46.953**	**58.581**	**72.612**	**87.840**	**6.56**	**5.6476×10^{-9}**

Table 6.2 Results of comparative analysis for SHE problem (m=0.8).

Algorithm	**Switching Angles (in degree)**					**THD**	**Fitness**
	α_1	α_2	α_3	α_4	α_5		
mDOA	9.710	33.420	43.280	61.160	83.590	5.62	3.0100×10^{-29}
BWOA	9.700	33.430	43.300	61.180	83.600	5.63	3.0500×10^{-29}
GWOA	10.320	31.830	44.740	62.230	85.650	6.73	3.3700×10^{-3}
WOA	33.270	44.500	52.910	64.490	76.640	5.56	3.9300×10^{-2}
TLBO	9.729	33.372	43.353	61.220	83.691	5.56	9.1894×10^{-6}
TLBO-WOA	**9.711**	**33.417**	**43.317**	**61.191**	**83.628**	**5.52**	**5.8950×10^{-6}**

Table 6.3 Results of comparative analysis for SHE problem (m=1.0).

Algorithm	Switching Angles (in degree)					THD	Fitness
	α_1	α_2	α_3	α_4	α_5		
mDOA	7.840	19.370	29.630	47.660	62.900	5.01	1.2200×10^{-28}
BWOA	7.860	19.370	29.650	47.680	63.210	5.01	1.2900×10^{-28}
GWOA	0.490	14.740	25.610	40.570	89.160	5.71	16.0400×10^{-2}
JSOA	7.860	19.360	29.650	47.680	63.200	5.01	3.4900×10^{-31}
MGWOA	0.490	14.740	25.610	40.570	89.160	5.71	16.0400×10^{-2}
MAO	9.670	22.370	33.040	51.910	64.630	5.26	3.6400×10^{-1}
CGO	13.250	26.370	45.930	46.050	87.220	13.99	9.7600×10^{-2}
COOT	7.970	19.460	29.790	47.740	63.200	5.04	3.4300×10^{-4}
GEO	8.620	10.600	38.760	76.590	83.170	14.83	4.6400×10^{-1}
HHO	8.160	19.500	30.150	48.210	63.350	5.16	2.6900×10^{-4}
WOA	4.190	20.290	22.120	41.970	61.150	6.90	3.9300×10^{-2}
TLBO	7.848	19.332	29.628	47.646	63.189	5.01	1.2657×10^{-5}
TLBO-WOA	**7.821**	**19.359**	**29.574**	**47.610**	**63.198**	**4.96**	**7.8095×10^{-6}**

According to THD and fitness values presented in Table 6.3, the JSOA achieves the best fitness values, however Hybrid TLBO-WOA's THD result is better than others. This is related with other harmonics up to 50th shown in Figure 4.21. Also, Table 6.4 shows the results of comparative analysis for simulation and experimental. It can be understood that nearly %1 difference between simulation and experimental results.

Table 6.4 Results of comparative analysis for simulation and experimental with harmonic contents.

Index	Analysis	% h_5	% h_7	% h_{11}	% h_{13}	THD	V_{RMS}
m=0.6	Simulation	0.33	0.59	0.16	2.74	6.56%	126.81 V
	Experiment	0.34	0.60	0.17	2.76	6.60%	125.54 V
m=0.8	Simulation	1.36	0.34	0.12	1.59	5.52%	153.69 V
	Experiment	1.38	0.34	0.13	1.61	5.80%	152.16 V
m=1.0	Simulation	0.71	0.79	1.88	0.25	4.96%	167.64 V
	Experiment	0.72	0.80	1.90	1.41	4.90%	165.98 V

CHAPTER 7
CONCLUSIONS

This research has focused on using the Hybrid TLBO-WOA method to reduce THD on the line-to-line voltage in a modified reduced switch MLI topology. The proposed topology requires the use of 12 switches for 11-level inverter, whereas a conventional cascaded H-bridge MLI would require 20 switches and other reduced switch topology would require 14 switches in single phase inverter. The performance of the study has been verified by both simulation and experimental prototype. A comparative analysis of calculated THD values, using these optimized angles and those reported in existing literature using various optimization methods, revealed that the TLBO-WOA algorithm achieves favourably lower THD in the 11-level inverter than most reported methods. Proposed algorithm for lowering THD values is found to be 3.96% compared to the other algorithms. This algorithm's standout characteristic is its lack of parameter requirements, necessitating from users only the initial inputs of population size, design variables, maximum iteration count, and the objective function. The examination of the Hybrid TLBO-WOA algorithm demonstrates its efficiency in optimization, capability of effectively handling various types of problems with or without constraints. Its user-friendly nature, stemming from no need for tuning control parameters, making it highly adaptable to a wide array of problem scenarios. The main concluding remarks are as follows:

- The study under dynamic load conditions performed excellently.
- In each modulation indices, the hybrid algorithm provided better THD value.
- The experimental results have been verified the simulation results with %1 difference.
- Both simulation and experimental findings demonstrate that the Hybrid TLBO-WOA successfully maintained the output voltage THD within the acceptable limits prescribed by IEEE 519 standard.

7.1 Summary of Contributions

This thesis has made notable contributions in the following areas:

- Development of an auxiliary switch MLI design that reduces the number of switches needed, providing a more efficient and cost-effective solution compared to cascaded MLIs.
- Performance Enhancement: Validation of the superior performance of the auxiliary switch MLI compared to cascaded MLIs, achieved through extensive experimental testing and analysis.
- The Hybrid TLBO-WOA Optimization Algorithm is a customized implementation that combines the Teaching-Learning-Based Optimization (TLBO) and Whale Optimization Algorithm (WOA) specifically designed for the auxiliary switch MLI. This hybrid methodology effectively addresses optimization difficulties, improving the performance and efficiency of the inverter.

In summary, the thesis has a conceptual contribution on MLI topology and an improved optimization algorithm, which provide significant contributions to the field of power electronics by enabling more efficient and optimized inverter designs.

7.2 Recommendation for Future Works

Regarding this thesis, recommendations and areas for future research might be enumerated as follows:

- In the context of an asymmetrical cascaded H-bridge inverter, alternative control techniques can be employed or different asymmetrical voltage distributions can be applied.
- Implementation of alternative hybrid inverter configurations that enhance the output levels while reducing the inverter specifications.
- Implementation of closed-loop control techniques for better results.

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WORK EXPERIENCES

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R & D Engineer	Kalyon Güneş Teknolojileri Üretim A.Ş.	2020 -
Electrical Engineer	Asimetrik Ege Ses ve Işık Sistemleri Tic. Ltd.Şti.	2015

PUBLICATIONS

SCI/SCI-Expanded Journal Papers:

1) **Yabalar Mehmet Halil**, Ercelebi Ergun (2024). "Hybrid Optimization Based Harmonic Minimization in Three Phase Multilevel Inverter With Reduced Switch Topology," in *IEEE Access*, vol. 12, pp. 71010-71023, 2024, doi: 10.1109/ACCESS.2024.3401730.

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1) **Yabalar Mehmet Halil**, Ercelebi Ergun (2024). "Thd Minimization of Line Voltage In Three Phase Multilevel Inverter Using Teaching-Learning-Based Optimization Algorithm," in *2024 6th International Dicle Scientific Research and Innovation Congress*, Diyarbakır, Turkey.

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