İSTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY

NEW MOSFET THRESHOLD VOLTAGE EXTRACTION METHODS AND EXTRACTORS

Ms. Thesis by

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

MOSFET EŞİK GERİLİMİNİ ELDE ETMEK İÇİN ÖNERİLEN YENİ YÖNTEMLER İLE V_{TH} ÇIKTISI VEREN DEVRE YAPILARI

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PREFACE

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ABBREVIATION

AMS	: Austria Micro Systems
BSIM3v3	: Model Parameters named as BSIM
CC	: Constant current method
CMOS	: Complementary Metal Oxide Semiconductor
CTAT	: Complementary to Absolute Temperature
DDA	: Differential Difference Amplifier
ELR	: Extrapolation in the linear region method
ESR	: Extrapolation in the saturation region method
GMLE	: Transconductance linear extrapolation method
GND	: Ground
IC	: Integrated Circuit
ICPD	: Identical Currents –Proportional Dimensions Method
IDPC	: Identical Dimensions- Proportional Currents Method
IGFET	: Insulated Gate Field Effect Transistor
LCDO	: Linear cofactor difference operator method
MOS	: Metal Oxide Semiconductor
MOSFET	: Metal Oxide Semiconductor Field Effect Transistor
NMOS	: N-type Metal Oxide Semiconductor
OPAMP	: Operational Amplifier
PMOS	: P-type Metal Oxide Semiconductor
PTAT	: Proportional to Absolute Temperature
RM	: Ratio method
SD	: Second derivative method
SDL	: Second derivative logarithmic method

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Vs	**:** Source Voltage
Vd	**:** Drain voltage
Vg	**:** Gate voltage
$\mathbf{V_{TH}}$	**:** Threshold Voltage
$\mathbf{V_{TN}}$	**:** Threshold Voltage of NMOS
$\mathbf{V_{TP}}$	**:** Threshold Voltage of PMOS
$\mathbf{V_{GS}}$	**:** Gate-source voltage of MOS Transistor
$\mathbf{V_{DD}}$	**:** Positive Supply Voltage
$\mathbf{V_{SS}}$	**:** Negative Supply Voltage
$\mathbf{V_{DS}}$	**:** Drain-Source voltage of MOS transistors
$\mathbf{V_{GS}}$	**:** Gate-Source voltage of MOS transistors
$\mathbf{I_D}$	**:** Drain current of a MOS transistor
β_n	**:** Dimension NMOS transisitor
β_p	**:** Dimension PMOS transisitor
θ	**:** Coefficient of the effect of field on the mobility
ε_θ	**:** Discrepancies caused by mobility reduction
ε_Δ	**:** Discrepancy in the presence of mismatch in V_{TH} and size.
ε_T	**:** Discrepancy in the presence of temperature variation.
T	**:** Absolute temperature
To	**:** Room absolute temperature
TC	**:** Temperature coefficient
α_T	**:** Temperature parameter
Ψ	**:** Coefficient of temperature sensors
ϕ_F	**:** Fermi Potential
γ	**:** Body factor

MOSFET EŞİK GERİLİMİNİ ELDE ETMEK İÇİN ÖNERİLEN YENİ YÖNTEMLER İLE V_{TH} ÇIKTISI VEREN DEVRE YAPILARI

ÖZET

MOSFET modellenmesinde çok önemli bir yer taşıyan eşik gerilimi, yapılan bir çok deney sonucu matematiksel olarak hesaplanabilirken aynı zamanda çıkışında direk V_{TH}'i veren basit devre yapıları ile de elde edilebilir. Bu çalışmada, kuvvetli-evirtim, lineer bölge, karakteristiklerine dayalı yeni eşik gerilimi elde etme yöntemleri önerilmiş ve bu yöntemlere dayanarak çıkışlarında NMOS ve PMOS transistörler için eşik gerilimi veren devrelerin tasarlanması anlatılmıştır.

Önerilen yöntem temelde, analog bir yapı ile gerçeklenen aritmetik işlemin sonucuna dayandırılmıştır. Tasarlanan devrelerde belli amaçlarla kullanılan yardımcı elemanlar mevcuttur. Bunlardan bir tanesi MOS transistörün lineer bölgede çalışmasını sağlayan OPAMP elemanıdır. Temel aritmetik işlemi elde etmemizi sağlayan diğer bir yardımcı eleman ise DDA'dir. Gerçeklenen aritmetik işleme göre yöntemi iki ana başlık altında toplanabiliriz;1)Basit aritmetik işlem ve 2)Genelleştirilmiş aritmetik işlem. Basit aritmetik işlemde önerilen devre yapıları "$2V_{GS1}$-V_{GS2}" işlemini gerçekler. Genelleştirilmiş işlemde ise gerçeklenmesi gereken denklem "aV_{GS1}-bV_{GS2}"'dir.

Her bir aritmetik işlem için devre farklı şekillerde tasarlanabilir. Buna dayanarak geliştirilmiş tasarım metodları, "sabit boyut-orantılı akım" (IDPC), "sabit akım-orantılı boyut" (ICPD) ve "aynı oranlı akım-boyut" (Flexible) olarak üç başlık altında toplanabilir. Önerilen devreler yardımıyla, eşik gerilimi NMOS ve PMOS transistörler için ayrı ayrı elde edilmiştir. V_{TN} için V_{SS}, V_{TP} için ise toprak referans alınarak sonuçlar elde edilmiştir. Cadence-SpectreS ile yapılan simülasyonlar MOS transistorlerin eşik geriliminin tasarlanan yeni devreler ile % 1 veya % 0.8 hata ile elde edilebildiğini göstermiştir.

Tez kapsamında eşik gerilimi çıktısı veren devreler mobilite etkisi , kanal boyu modülasyonu, boyut uyuşmazlığı ve gövde etkisi gibi ikinci dereceden etkiler göz önüne alınarak analiz edilmiştir.

Devreler besleme gerilimi değişimlerinden az etkilenir ve sıcağa lineer olarak değişen bağımlılık gösterirler. NMOS eşik geriliminin sıcaklıkla negatif, PMOS eşik geriliminin sıcaklıkla pozitif olarak değişmesinden yararlanarak, sıcaklık katsayıları sırasıyla 1.99mV/^{o}C ve -1.42 mV/^{o}C olan PTAT ve CTAT sıcaklık sensörleri tasarlanmıştır. Yine aynı özellik yardımıyla, OPAMP toplayıcı yapısı kullanılarak sıcaklık ve besleme gerilimi değişimlerinden bağımsız bir gerilim referans devresi önerilmiş ve deney sonuçları ile desteklenmiştir.

NEW MOSFET THRESHOLD VOLTAGE EXTRACTION METHODS AND EXTRACTORS

SUMMARY

The threshold voltage value, which is the most important electrical parameter in modeling MOSFETs, can be extracted from either measured drain current or capacitance characteristics, using a single or more transistors. Practical circuits based on some of the most common methods are also available to automatically and quickly measure the threshold voltage. We have presented the existing methods which obtain threshold voltage of MOSFETs in two ways: Current/Voltage Measurement and Automatic Extraction.

In this thesis, new threshold voltage extraction methods based on the strong-inversion characteristic are proposed and the development of the NMOS and PMOS threshold voltage extractors implementing new methods is described. Proposed extraction method is based on an arithmetic operation which is classified into basic and generalized arithmetic operation schemes. Different implementations for each operation scheme such as IDPC (identical current-proportional dimensions), ICPD (identical dimensions-proportional current) and Flexible (proportional dimensions-proportional currents) method have been discussed and the effect of nonidealities such as mobility reduction, channel-length modulation, mismatch, and body effect has been analyzed.

Auxiliary components are needed to perform design conditions. DDA operates as an arithmetic processor to precisely implement multiplication by two and subtraction as needed for extrapolation and OPAMP is used to bias transistors in triode region. The Cadence-SpectreS simulations confirm that threshold voltage of an MOS transistor can be extracted with % 1 veya % 0.8 errors automatically using the V_{TH} extractor, without any need of calculation and delay. The extracted V_{TH} for NMOS and PMOS is referenced to V_{SS} and ground respectively. Experimental results have indicated that the accuracy of this method is as good as the complicated and tedious numerical method.

Additional applications such as temperature measurement where the V_{TH} extractor can be used either as a PTAT sensor or as a CTAT with small values of temperature coefficients (-1.42 mV/^{o}C and 1.99 mV/^{o}C, respectively), and voltage reference circuit which is independent of temperature and supply voltage fluctuation, are presented.

1. INTRODUCTION

The threshold voltage, V_{TH}, is a fundamental parameter for MOSFET modeling and characterization. There exist numerous methods to extract the value of threshold voltage such as extraction from either measured drain current or capacitance characteristics, using a single or more transistors. These conventional methods require typically over 30 measurements as a consequence, they are very time consuming. Practical circuits called “extractors” based on some of the most common methods are also available to quickly obtain the threshold voltage. Extractor circuits capable of determining V_{TH} automatically have received considerable attention because they not only greatly facilitate device characterization and process monitoring, but also enable on-chip temperature sensing and reference voltage generation.

In order to comprehend process dependency of threshold voltage, structure of the MOSFETs is given and determination of V_{TH} is discussed. After that, the overview of existing methods of determining the threshold voltage of MOSFETs are presented to put emphasize on the subject. In this thesis, new threshold voltage extraction methods based on the strong-inversion characteristic are proposed and the development of the NMOS and PMOS threshold voltage extractors implementing these methods is described. Different implementations have been discussed and the effect of nonidealities such as mobility reduction, channel-length modulation, mismatch, body effect and temperatures has been analyzed.

1.1 Metal Oxide Semiconductor

MOS transistor is a four terminal component, namely, the gate (G), substrate or bulk (B), source (S) and drain (D). Selecting the substrate as the reference terminal, we can define three independent port voltages called source voltage Vs, drain voltage Vd and gate voltage Vg.

Because the gate-substrate voltage controls the channel current between drain–source junctions, this component is also called IGFET (Insulated Gate Field Effect Transistor). Nowadays, highly doped polycrystalline silicon is preferred instead of suitable metal for gate electrode.

The structure depicted in Figure 1.1 is called an n-channel MOSFET because the channel charge is due to electrons. Alternatively, a p-channel MOSFET is obtained by forming two p^+n junctions on an n-type substrate. In n-channel MOSFET the drain is defined as the terminal with more positive voltage, in p-channel MOSFET, its definitions is just the opposite.

1.1.1 Structure of the MOSFET

As shown in Figure 1.1 the basic silicon substructure of the metal-oxide semiconductor transistor (MOSFET) consists of two n^+p junctions built on p-type silicon substrate and a surface space-charge region between two. A conductive gate electrode and an underling film of insulating SiO_2 from the superstructure by which the transversal boundary field ($E_X(0)$) at the surface can be controlled. The two junctions, being non-forward biased are not electrically interconnected unless this field induces sufficiently large population of electrons in the surface space-charge region. This region is called as “channel” and is present by the help of transversal boundary field which exists because of the positive gate bias. When such a channel of electrons is present, an external bias between the two junctions creates a channel current from drain to source. This current can be modulated by the gate-substrate voltage because the latter controls, which, in turn, controls the electron concentration in the channel.

Apart from ideal, in MOS transistors (here NMOS) channel will exists with the help of gate source voltage larger then a certain value. The minimum gate-source voltage which helps to produce of the drain-source channel is called “Threshold Voltage (V_{TH})”. For NMOS transistor, V_{GS} should be larger than V_{TH} ($V_{GS}>V_{TH}$), if chosen smaller channel will not arise.

V_{TH} threshold voltage strongly depends on the type of the semi-conductor, doping concentration, type of the gate conductor and process conditions.

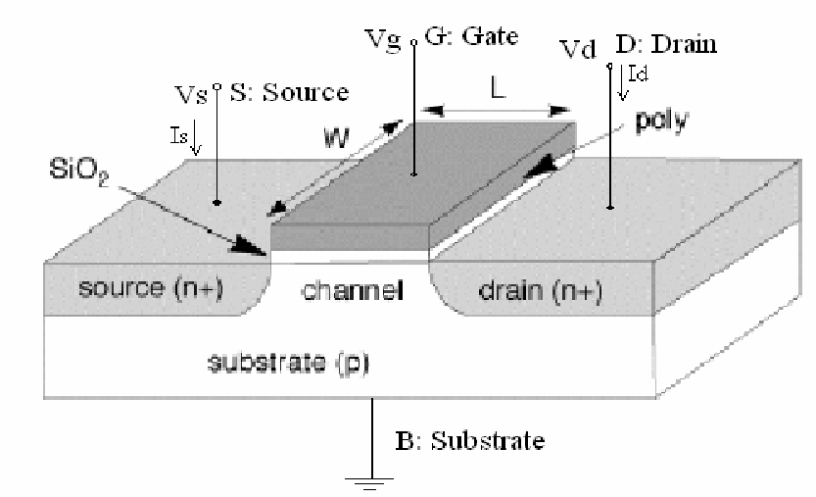


Figure 1.1: Structure of MOSFET.

Assuming that $V_{GS}>V_{TH}$, current to voltage characteristics will be different in two regions: "Linear Region" and "Saturation Region" in Figure 1.2. In Linear region conductivity of the channel will be linear to V_{GS}.

$$I_D = \beta V_{DS}(V_{GS} - V_{TH} - \frac{V_{DS}}{2}) \quad \textbf{(1.1)}$$

In saturation region, current will be independent of the changes in V_{DS} voltage for a constant V_{GS}, because current is saturated.

$$I_D = \frac{\beta}{2}(V_{GS} - V_{TH})^2 \quad \textbf{(1.2)}$$

1.1.2 Threshold Voltage of MOSFET

Threshold voltage of MOSFET can be explained as "the condition in which minority carriers (electrons in the case of an n-channel MOSFET) have the same concentration as the dopants at the surface". The expression of NMOS threshold voltage is,

$$V_{TH} = V_{TH0} + \gamma\left[\sqrt{(V_S + 2\phi_{FB})} - \sqrt{2\phi_F}\right] \quad \textbf{(1.3)}$$

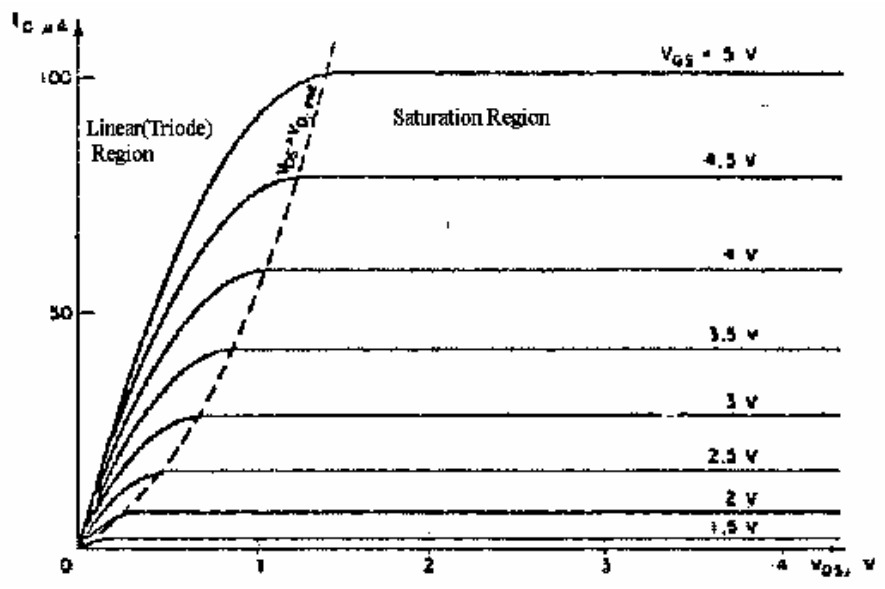


Figure 1.2: MOS transistor I_D-V_{DS} characteristics.

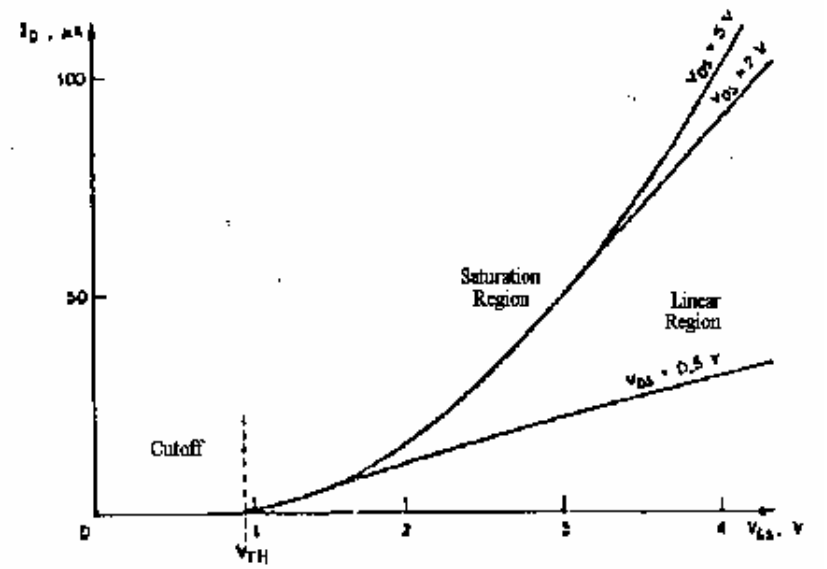


Figure 1.3: MOS transistor I_D-V_{GS} characteristic.

for PMOS,

$$V_{TH} = V_{TH0} - \gamma\left[\sqrt{(-V_S - 2\phi_F)} - \sqrt{(-2\phi_F)}\right] \quad \textbf{(1.4)}$$

$$\gamma = \frac{1}{C_{OX}}\sqrt{2q\varepsilon_s N_A} \quad \textbf{(1.5)}$$

where ϕ_F is Fermi Potential, γ is body factor and Vs is source voltage. The V_{TH0} represents the threshold voltage for Vs=0 and is called "Zero-bias threshold". In the

most popular of the present-day families, the CMOS, V_{TH0} is expected to be in the range of 0.5- 1.0 V for n-channel MOSFET and in the range of -0.5 to -1.0 V for p-channel MOSFET.

1.2 Threshold Voltage Determinations

The threshold voltage, $V_{TH,}$ is a fundamental parameter for MOSFET modeling and characterization. This parameter, which represents the onset of significant drain current flow, has been given several definitions, but it may be essentially understood as the gate voltage value at which the transition between weak and strong inversion takes place in the MOSFET channel.

There exist numerous methods to extract the value of threshold voltage such as extraction from either measured drain current or capacitance characteristics, using a single or more transistors. Practical circuits based on some of the most common methods are also available to automatically and quickly extracts the threshold voltage.

1.2.1 Existing Threshold Voltage Extraction Methods

Determining threshold voltage of a MOSFET transistor can be separated essentially in two:

1. *Measurement Methods:*

    i. Classical Graphical Method of determining threshold voltage that uses approximation of $V_{TH}=V_{GS}$ at very low currents (graphical method). This method is simple and quick but not accurate.

    ii. Indirect Mathematical Extraction of V_{TH} from a series of current/ voltage measurements (numerical method). This method is more accurate but can be time-consuming and expensive.

2. *Automatic Extraction Circuits:*

    These methods generate V_{TH} of MOSFET with the use of extractor circuits which generates the value of V_{TP} or V_{TN} at the output directly. This method

can be more accurate, quick and simple when compared with measurement methods.

1.2.1.1 Measurement Methods

The greater part of the methods available to determine V_{TH} are based on the measurement of the static transfer drain current versus gate voltage (I_D–V_{GS}) characteristics of a single transistor. Most of these I_D–V_{GS} methods use the strong inversion region while only a few consider the weak inversion region. Extraction is mostly done using low drain voltages so that the device operates in the linear region. However, V_{TH} extraction with the device operating in saturation is also frequently carried out. [11]

The existing methods of determining V_{TH} voltage by the help of measurement are:

1. *Linear Region*: The transistor is biased in linear region ($V_{DS} < V_{GS}-V_{TH}$)

    i. *Constant current (CC) method*, which defines V_{TH} as the gate voltage corresponding to a certain predefined practical constant drain current when V_{DS}<100mV.

    ii. *Extrapolation in the linear region (ELR) method*, which finds the gate voltage axis intercept of the linear extrapolation of the I_D-V_{GS} characteristics at its maximum first derivative (slope) point. V_{TH} is calculated by adding $V_{DS}/2$ to the result.

    iii. *Transconductance linear extrapolation (GMLE) method*, which finds the gate voltage axis intercept of the linear extrapolation of the gm-V_{GS} characteristics at its maximum first derivative (slope) point.

    iv. *Second derivative (SD) method*, which determines V_{TH} at the maximum of the SD of I_D with respect to V_{GS}.

    v. *Ratio method (RM)*, which finds the gate voltage axis intercept of the ratio of the drain current to the square root of the transconductance. This V_{TH} includes mobility degration and parasitic capacitances.

vi. *Transition method*, which uses the sub-threshold-to-strong inversion transition region of the MOSFET's transfer characteristics to extract the threshold voltage. It is based on an auxiliary operator (G1) that involves integration of the drain current as a function of gate voltage.

vii. *Integral method*, which is insensitive to the effect of drain and source parasitic series resistances. It was demonstrated that substituting the necessary values of voltage and current in an integral function (D). This method evaluates the threshold voltage by doing a curve fitting of function D1.

viii. *Corsi function method*, which is implemented on the plot of the Corsi function versus V_{GS} of MOSFET for several arbitrary values of Vp. This method evaluates the threshold voltage by finding the plot for which the minimum just disappears and for this particular case $Vp=V_{TH.}$

ix. *Second derivative logarithmic (SDL) method*, which determines V_{TH} at the minimum of the SD of log (I_D)–$V_{GS.}$

x. *Linear cofactor difference operator (LCDO) method*, which is implemented on the plot of function ΔI_D versus V_{GS} of MOSFET.

xi. *Non-linear optimization*, which extracts V_{TH} based on optimization techniques applied to the MOSFET current-voltage characteristics.

2. *Saturation Region*: The transistor is biased in saturation ($V_{DS} > V_{GS}-V_{TH}$)

i. *Extrapolation in the saturation region (ESR) method*, which finds the gate voltage axis intercept of the linear extrapolation of the $\sqrt{I_D}$ –V_{GS} characteristics at its maximum first derivative (slope) point.

ii. *G1 function extraction method* implemented using the plot of the G1 function versus $\sqrt{I_D}$. This method consists of finding the gate-voltage axis intercept of the linear extrapolation of the $\sqrt{I_D}$ –V_{GS} curve.

1.2.1.2 Automatic Extraction Circuits

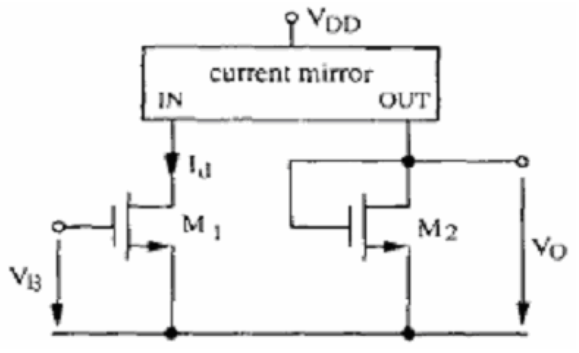
Conventional (numerical and graphical) methods require typically over 30 measurements of the drain current at different gate-source voltages and as a consequence, they are very time consuming. Therefore, circuits capable of providing an accurate V_{TH} in the form of electrical voltage, which are known as "V_{TH} extractors", arise as very useful blocks, not only for design engineers, but also for process engineers.

1.2.2 Overview of Existing V_{TH} Extractor Circuits

Because of the need of V_{TH} for MOS technology and their applications, there are several proposed V_{TH} extraction circuits. The extraction circuits are capable of obtaining threshold voltage of either NMOS or PMOS transistors as a difference of output voltages or as its output voltage.

In the following, the overview of the existing V_{TH} extraction circuits is presented.

- In 1992, Z. Wang presented a family of circuits based on square-law characteristics that directly produce an output voltage equal to V_{TH}, the threshold voltage of an MOSFET transistor. This is advantageous for device characterization, compared to the usual method employing linear regression, because the extractor circuit requires only a single measurement and it eliminates numerical calculations. [16]



$$V_T = \frac{V_o - \sqrt{\frac{K_1}{K_2}}\, V_B}{1 - \sqrt{\frac{K_1}{K_2}}}$$

Figure 1.4: Basic V_{TH} extractor presented by Z. Wang.

V_{TH} can be obtained directly from Vo and V_B. The corresponding circuit implementations are shown in Figure 1.5 (a) and (b), and referred to as

incremental (VTH^+ extractor) and decrimental (VTH^- extractor) respectively. [16]

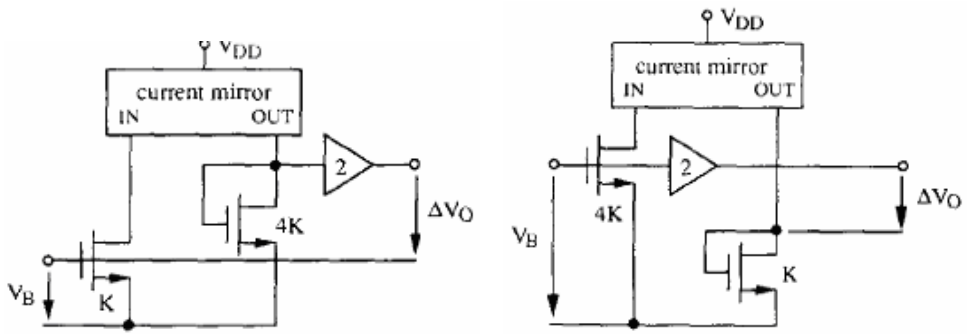


Figure 1.5: Corresponding V_{TH} extractor presented by Z. Wang.

The same method can be used by the help of nxn^2 transistor arrays with and without current mirrors. Transistor array is equal to a single MOS transistor with reduced K and increased V_{TH}.

- In 1993, a circuit which improves Z. Wang's circuit is presented by M.G. Johnson. A three-terminal modified V_{TH} extractor design obtains ground-referenced output voltage equal to V_{TH} with inclusion of self-bias and a differential amplifier built from two NMOS transistors. [11]

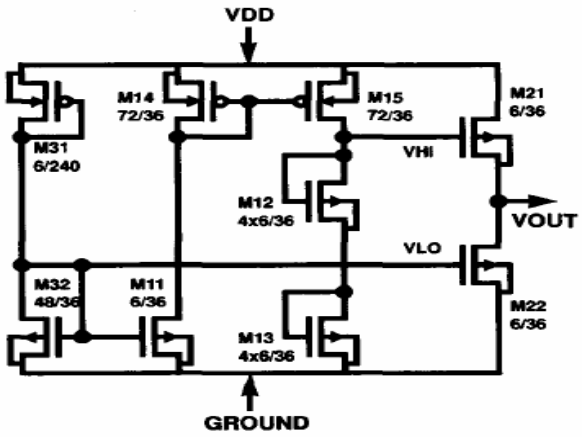


Figure 1.6: Improved V_{TH} extractor presented by M.G. Johnson.

- In 2003, a new V_{TH} extraction method is presented by C. Pope, A.M. Manolescu. V_{TN} extractor circuit is implemented which directly generate the value of the threshold voltage by taking the weight difference between gate-

source voltages of MOS transistors working in saturation with different effective gate-source voltages.[13]

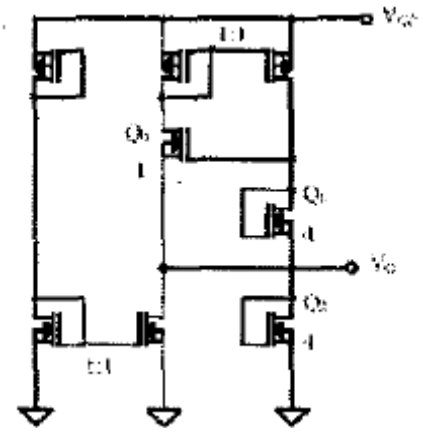


Figure 1.7: Basic V_{TH} extractor presented by C. Popa, A. M. Manolescu.

- The proposed V_{TH} structure in 2001 by Fikos and Siskos combines a simple low voltage V_{TH} extracting block and novel feedback, to achieve independence of the output from the supply voltage, low current consumption (therefore, low power consumption), accuracy of the extracted threshold voltage toward supply voltage variations and compensation of body effect and transistor mismatch. [9].

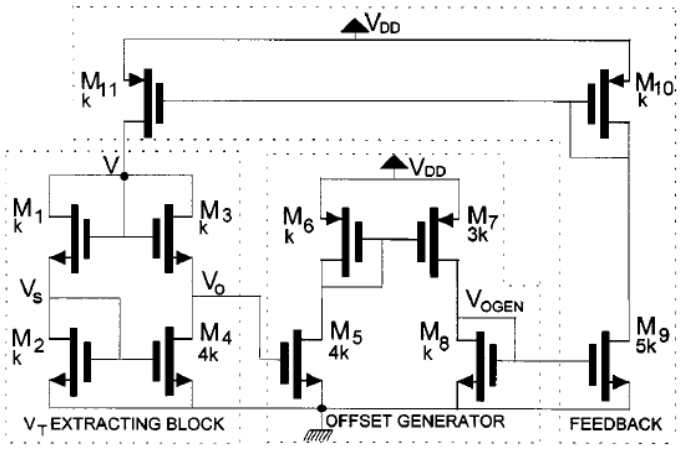


Figure 1.8: The proposed V_{TH} extractor structure by Fikos and Siskos.

- In 2004, new extractor circuits which directly produce output voltages equal to V_{TH} with a single measurement without traditionally numerical calculations are presented. Input-free NMOS and PMOS V_{TH} extractor

circuits use cascaded structure to eliminate the error caused by body effect.[17]

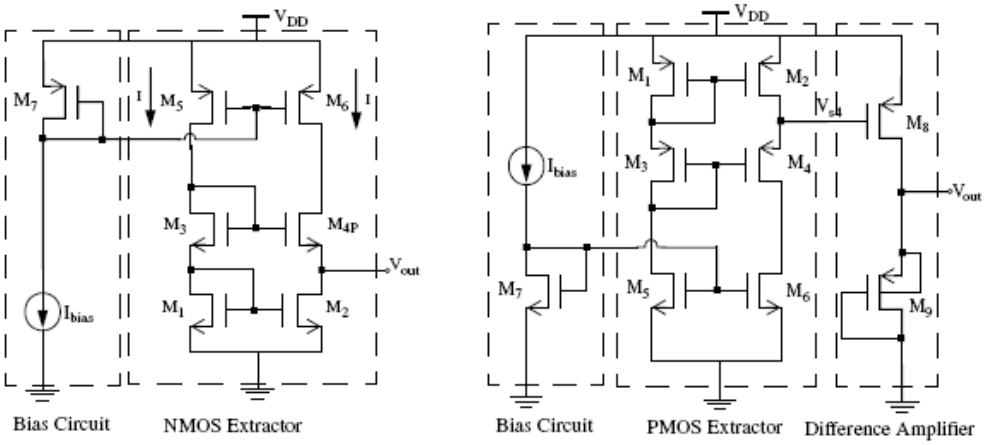


Figure 1.9: Presented NMOS and PMOS extractors Y. Wang and G. Tarr.

The extracted V_{TN} for NMOS is referenced to ground while the extracted absolute value of V_{TP} for PMOS is referenced to V_{DD} using additional PMOS difference amplifier. [17]

- Z. Wang developed one of the preliminary V_{TH} extractor circuits, which worked on the assumptions of square law behavior of long channel MOSFET devices with no body effects. If his technique is applied to an n-well CMOS process, one will be able to extract the V_{TH} of a PMOS device, but V_{TH} extraction of an NMOS device will be inaccurate due to body effect on the NMOS devices.

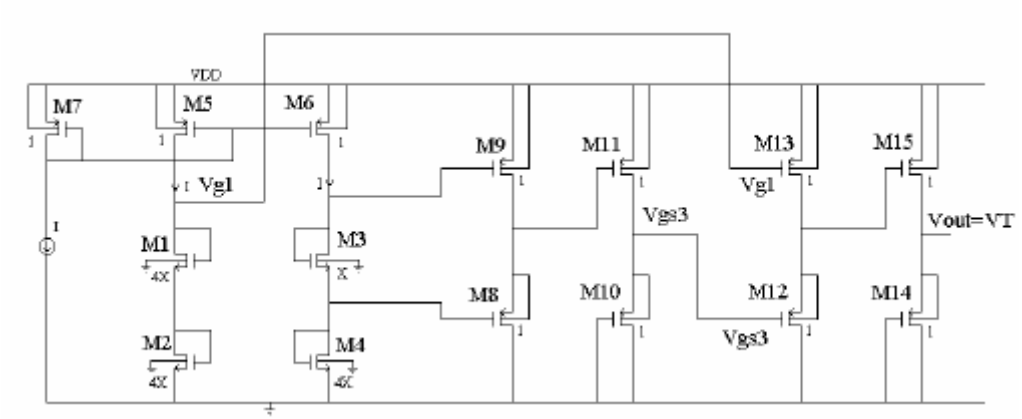


Figure 1.10: The improved V_{TH} extractor structure by Sengupta.

In an n-well CMOS process, Z. Wang's technique is modified for accurate V_{TH} extraction of the NMOS device by Sengupta, and the proposed circuit in 2004 is shown in Figure 1.10. In this structure, the bulks of all the NMOS and PMOS devices are tied to ground and V_{DD} respectively, and the threshold voltage of M_2 is extracted as the V_{TH} of the NMOS device. [15]

- Filanovsky have proposed another implementation of circuit that extracts $-V_{TN}$ in 1997 and implemented it with a V_{TP} extractor on the same chip. [5]

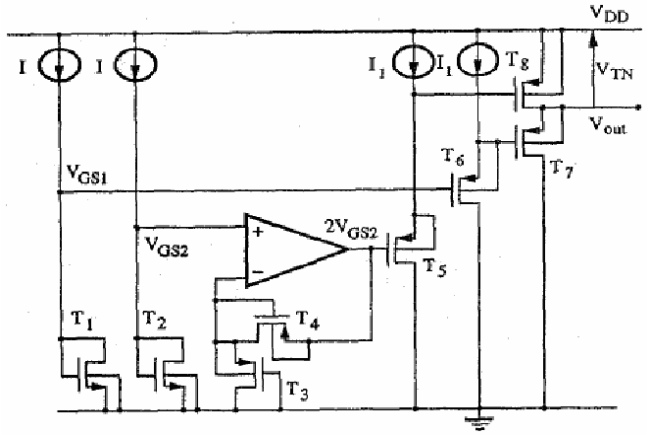


Figure 1.11: ($-V_{TN}$) extractor presented by Filonovsky.

- In 2000, Çilingiroğlu and Hoon have given another look in V_{TH} extraction that combines both auto biasing and extraction of MOSFETs. Extractor circuit implements the most popular industrial extraction algorithm of biasing a saturated MOSFET to the linear portion of its' $\sqrt{I_D}$, versus V_{GS} characteristic, and extrapolating the tangential line to V_{GS} axis.

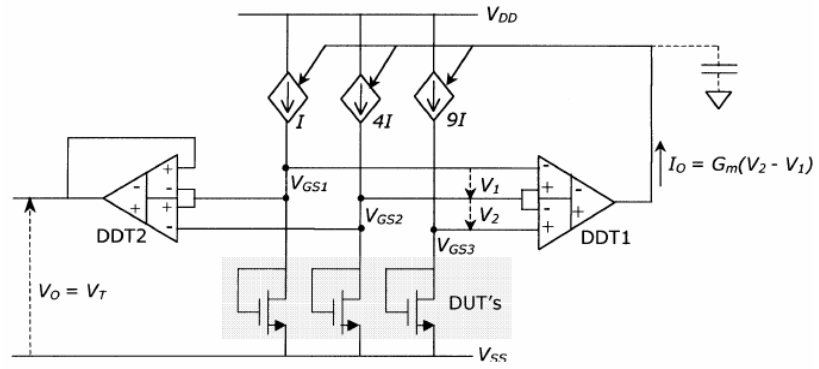


Figure 1.12: V_{TH} extractor presented by Çilingiroğlu and Hoon.

With appropriate modifications, the architecture can also serve as an extractor implementing the linear method. The proposed architecture is applicable to both PMOS and NMOS on the same chip, and generates the value of as a voltage with respect to the appropriate rail. [4].

- In 1997, Filonovsky presented a circuit for transistors of both polarities but the precision of measurements is different. When the configuration is used with transistors having bulk-to-source connection then good measurements can be performed in a wide range of transistor currents. If the topology is used with transistors having the common bulk the measurements are distorted by the body effect and a small error can be obtained in a smaller (compared with the Johnson's circuit) range of transistor currents. [7]

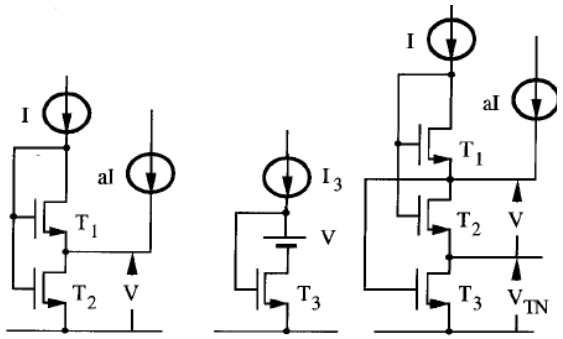


Figure 1.13: V_{TN} extractor presented by Filonovsky.

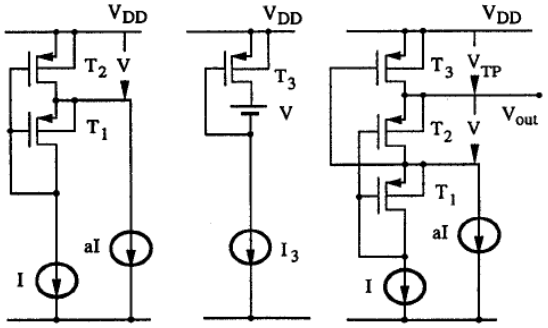


Figure 1.14: V_{TP} extractor presented by Filonovsky.

The circuits employ a specially arranged series connection of three transistors where the middle transistor is in linear operation and external transistors are in saturation. [7]

Most of the proposed extractors emulate the saturation method so proposed circuits are alternative to these methods that directly generate the value of V_{TH} based on strong-inversion characteristic.

In this thesis, we present design details and experimental evaluation of two new classes of extractor circuits that can extract V_{TP} or V_{TN}. In Chapter 2, the principle is described and the implementation of the V_{TH} extractors is presented in Chapter 3. The effect of the transistor nonidealities such as mobility reduction, channel-length modulation, device mismatch, and temperature dependency on the performance of V_{TH} extraction is discussed in detail in Chapter 4. Experimental results, which strongly demonstrate the advantage of using the V_{TH} extractors in V_{TH} extractions over the complicated and tedious numerical method, are presented in Chapter5. Additionally in Chapter 6, several interesting applications of the proposed V_{TH} extractor circuits are described, including MOS transistor characterization, voltage reference circuit, PTAT and CTAT sensors for temperature measurement and a square-root circuit. Finally, layouts of sample circuits for proposed extractors are shown in Chapter 7.

2. PRINCIPLE OF THE NEW EXTRACTION METHOD

In this work, a new V_{TH} extraction scheme is proposed and new VTH extractor circuits based on this principle are designed with the help of MOSFETs biased in linear region and obtains V_{TH} at the output, directly.

This V_{TH} extraction scheme is based on a simple arithmetic operation which gives V_{TH} by neglecting second-order effects. In order to eliminate plus term $V_{DS}/2$ at the end of the operation, coming from strong-inversion characteristics, proportional drain-source voltages are used.

The architecture of the presented circuit is shown in Figure 2.1.

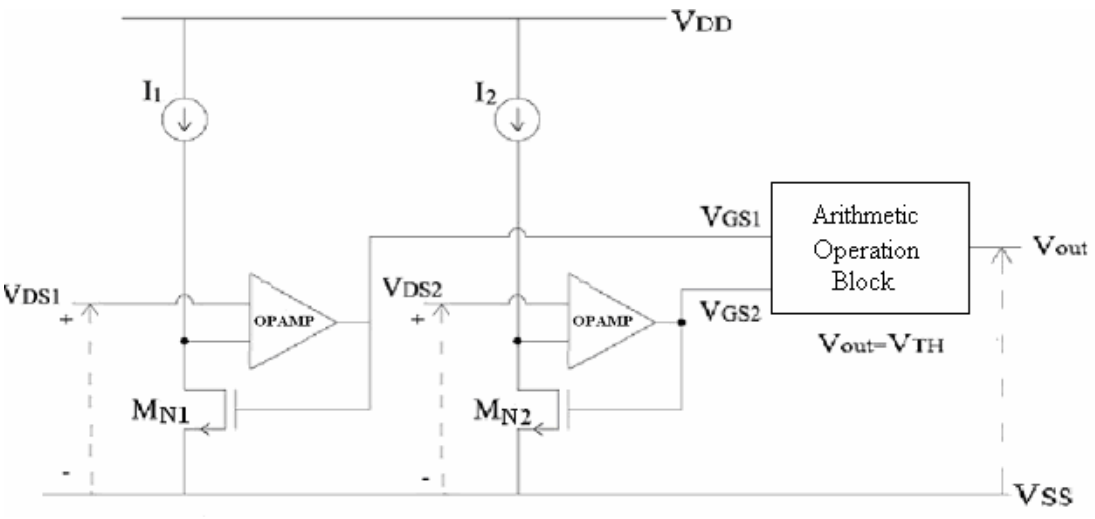


Figure 2.1: Basic scheme of V_{TH} extraction.

The explanation of the proposed architecture is given based on NMOS structure. We use two NMOSs biased with small V_{DS1} and V_{DS2} (proportional with V_{DS1}) voltages with the help of OPAMP which receives I_1 and I_2 (proportional with I_1) and develop gate-source voltages of V_{GS1} and V_{GS2}, respectively.

$$V_{GS1} = \frac{I_1}{\beta_1 V_{DS1}} + V_{TH1} + \frac{V_{DS1}}{2} \qquad \textbf{(2.1)}$$

$$V_{GS2} = \frac{I_2}{\beta_2 V_{DS2}} + V_{TH2} + \frac{V_{DS2}}{2} \quad \textbf{(2.2)}$$

Arithmetic operation block is formed with a DDA (or cascaded DDAs) performing the arithmetic operation which yields V_{TH} when design conditions are achieved.

We will realize the arithmetic operation scheme in two ways:

1. Basic Arithmetic Operation: This is the basic operation "$2V_{GS1}$-V_{GS2}".
2. Generalized Arithmetic Operation: This is the generalization of the basic operation "aV_{GS1}-bV_{GS2}".

There are two main design parameters in both extraction schemes:

1. Drain currents (I) of MOS devices.
2. Dimensions (β) of MOS devices.

The new V_{TH} extraction technique can be separated into three, depending on the design parameters defined above.

1. Identical Dimensions- Proportional Currents (IDPC) Method.
2. Identical Currents –Proportional Dimensions (ICPD) Method.
3. Flexible Design Method

Notice that, the use of "Proportional V_{DS}" voltages, which eliminates the plus term extracted with V_{TH}, is common to all methods.

Alternatively, the same principle is applicable to PMOS triode transistors with appropriate modifications for reversal polarities.

2.1 Basic Arithmetic Operation Scheme

The Basic Arithmetic Operation scheme performs the "$2V_{GS1}$-V_{GS2}" arithmetic operation with the use of $V_{DS2} = 2V_{DS1}$ to realize V_{TH} without a plus term at the output.

Arithmetic operation block is formed with a DDA performing the arithmetic operation "$V_O=2V_{GS1}-V_{GS2}$" which yields V_{TH} when design conditions are achieved.

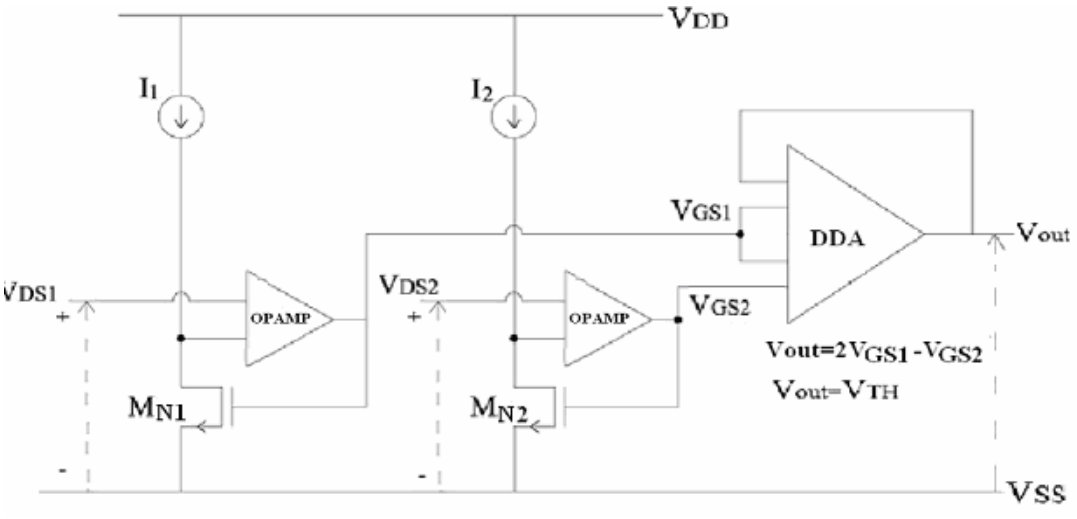


Figure 2.2: Basic Arithmetic Operation Scheme in V_{TH} extraction.

2.1.1 Identical Dimensions- Proportional Currents (IDPC) Method

The first extraction method assumes that M_{N1} and M_{N2} are identical ($\beta_1 = \beta_2 = \beta$) and drain currents of devices are proportional to each other.

V_{DS} voltages are chosen as, $V_{DS2} = 2V_{DS1}$.

In case of $I_2 = 4I_1$, V_{GS} voltages are written by rearranging equations (2.1) and (2.2) as,

$$V_{GS1} = \frac{I_1}{\beta V_{DS1}} + V_{TH} + \frac{V_{DS1}}{2} \quad \textbf{(2.3)}$$

$$V_{GS2} = \frac{4I_1}{\beta \cdot 2V_{DS1}} + V_{TH} + \frac{2V_{DS1}}{2} \quad \textbf{(2.4)}$$

At the output of the DDA, the arithmetic operation,

$$V_O = 2V_{GS1} - V_{GS2} \quad \textbf{(2.5)}$$

is realized. When equations (2.3), (2.4) and (2.5) are used, V_{TH} is achieved at the output of the DDA, as shown below.

$$V_O = 2V_{GS1} - V_{GS2}$$
$$V_O = 2\left(\frac{I_1}{\beta V_{DS1}} + V_{TH} + \frac{V_{DS1}}{2}\right) - \left(\frac{4I_1}{\beta \cdot 2V_{DS1}} + V_{TH} + \frac{2V_{DS1}}{2}\right) \quad \textbf{(2.6)}$$
$$V_O = V_{TH}$$

This result is obtained under the assumption below.

$$V_{TH1} = V_{TH2} = V_{TH} \quad \textbf{(2.7)}$$

2.1.2 Identical Currents –Proportional Dimensions (ICPD) Method

Here, we assume that transistor (M_{N1} and M_{N2}) dimensions are proportional ($\beta_1 = 4\beta_2$) and drain currents are identical.

Drain-source voltages are chosen as, $V_{DS2} = 2V_{DS1}$.

In case of $I_2 = I_1$, V_{GS} voltages are obtained by rewriting equations (2.1) and (2.2).

$$V_{GS1} = \frac{I_1}{4\beta_2 \cdot V_{DS1}} + V_{TH} + \frac{V_{DS1}}{2} \quad \textbf{(2.8)}$$

$$V_{GS2} = \frac{I_1}{\beta_2 \cdot 2V_{DS1}} + V_{TH} + \frac{2V_{DS1}}{2} \quad \textbf{(2.9)}$$

The DDA supplies the arithmetic operation of (2.5), so by using equations (2.8) and (2.9) we obtain V_{TH} at the output.

$$V_O = 2V_{GS1} - V_{GS2}$$
$$V_O = 2\left(\frac{I_1}{4\beta_2 \cdot V_{DS1}} + V_{TH} + \frac{V_{DS1}}{2}\right) - \left(\frac{I_1}{\beta_2 \cdot 2V_{DS1}} + V_{TH} + \frac{2V_{DS1}}{2}\right) \quad \textbf{(2.10)}$$
$$V_O = VTH$$

This result is performed under the assumption in equation (2.10).

2.1.3 Flexible Design Method

The extraction method can also be called "Proportional Dimensions-Proportional Current". The assumption is that, both transistors should have the same proportion in current and dimension.

The chosen proportion is **2** which means that $\beta_1 = 2\beta_2$ and $I_2 = 2I_1$ to be able to realize design conditions,

V_{DS} voltages are chosen as, $V_{DS2} = 2V_{DS1}$.

In case of defined conditions, V_{GS} voltages are written by rearranging equations (2.1) and (2.2) as,

$$V_{GS1} = \frac{I_1}{2.\beta V_{DS1}} + V_{TH} + \frac{V_{DS1}}{2} \quad \textbf{(2.11)}$$

$$V_{GS2} = \frac{2I_1}{\beta \cdot 2V_{DS1}} + V_{TH} + \frac{2V_{DS1}}{2} \quad \textbf{(2.12)}$$

At the output of the DDA, the arithmetic operation,

$$V_O = 2V_{GS1} - V_{GS2} \quad \textbf{(2.13)}$$

is realized with the help of (2.11) and (1.12) and V_{TH} is achieved as an output (2.14).

$$\begin{aligned} V_O &= 2V_{GS1} - V_{GS2} \\ V_O &= 2\left(\frac{I_1}{\beta V_{DS1}} + V_{TH} + \frac{V_{DS1}}{2}\right) - \left(\frac{4I_1}{\beta \cdot 2V_{DS1}} + V_{TH} + \frac{2V_{DS1}}{2}\right) \\ V_O &= V_{TH} \end{aligned} \quad \textbf{(2.14)}$$

This result is obtained under the assumption below.

$$V_{TH1} = V_{TH2} = V_{TH} \quad \textbf{(2.15)}$$

2.2 Generalized Arithmetic Operation Scheme

We have proven that V_{TH} can be extracted from the simple arithmetic operation in (2.5). Here, we will show that we can also obtain V_{TH} by using a more general arithmetic operation.

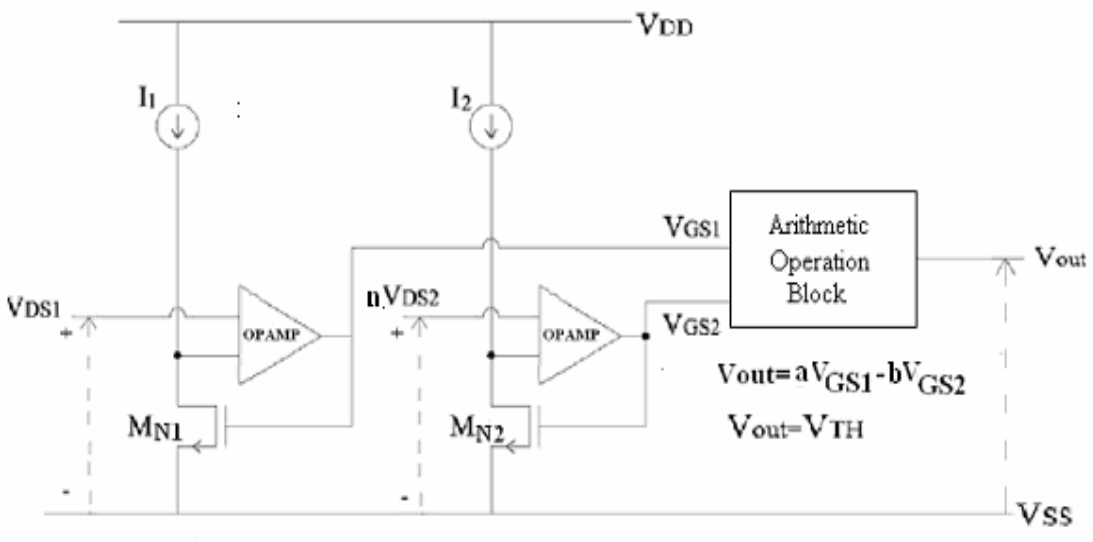


Figure 2.3: Generalized Arithmetic Operation Scheme in V_{TH} extraction.

The arithmetic operation is changed into,

$$V_O = aV_{GS1} - bV_{GS2} \quad \text{(a and b are integer numbers)} \tag{2.16}$$

We assume that M_{N1} and M_{N2} are proportional ($\beta_1 = m\beta_2$), as well as the drain bias currents ($I_2 = kI_1$). We use proportional V_{DS} voltages ($V_{DS2} = nV_{DS1}$) to eliminate the positive term appearing at the end of the operation. During design, m, k and n must be chosen appropriately.

In this generalized approach, V_{GS} expressions are obtained as follows.

$$V_{GS1} = \frac{I_1}{m\beta_2 \cdot V_{DS1}} + V_{TH} + \frac{V_{DS1}}{2} \tag{2.17}$$

$$V_{GS2} = \frac{kI_1}{\beta_2 \cdot nV_{DS1}} + V_{TH} + \frac{nV_{DS1}}{2} \tag{2.18}$$

The result of the generalized arithmetic operation is,

- if $a > b$,

$$V_O = aV_{GS1} - bV_{GS2}$$
$$V_O = a\left(\frac{I_1}{m\beta_2 \cdot V_{DS1}} + V_{TH} + \frac{V_{DS1}}{2}\right) - b\left(\frac{kI_1}{\beta_2 \cdot nV_{DS1}} + V_{TH} + \frac{nV_{DS1}}{2}\right) \quad \textbf{(2.19)}$$
$$V_O = V_{TH}$$

- if $a < b$,

$$V_O = -V_{TH} \quad \textbf{(2.20)}$$

Then,

$$V_O = (a\text{-}b)\ V_{TH} \quad \textbf{(2.21)}$$

is obtained, if the conditions below are fulfilled.

$$\frac{a}{m} = \frac{b \cdot k}{n} \quad \textbf{(2.22)}$$

$$a = b \cdot n \quad \textbf{(2.23)}$$

From (2.22) and (2.23), the following condition is also obtained:

$$k \cdot m = n^2 \quad \textbf{(2.24)}$$

All design methods, IDPC, ICPD and Flexible method can be applied to this type of extraction scheme.

A design example

If $V_O = V_{TH}$ is desired, a=3, b=2 can be selected. Then, n will be equal to 3/2 from (2.18) and $k \cdot m = \frac{9}{4}$ from (2.19), which means $\frac{I_2}{I_1} \cdot \frac{\beta_1}{\beta_2} = \frac{9}{4}$. Using the following proposed methods, new extractors can be designed separately, with the use of appropriate devices to realize required conditions.

- Choosing identical transistors and $\frac{I_2}{I_1} = \frac{9}{4}$ ratio as the proportion of currents. (IDPC method)

- Current sources are chosen equal to each other and transistor dimension ratio is $\frac{\beta_1}{\beta_2} = \frac{9}{4}$. (ICPD method)

- Both Current sources and dimension ratio of transistors are chosen the same, $\frac{I_2}{I_1} = \frac{3}{2}$ and $\frac{\beta_1}{\beta_2} = \frac{3}{2}$. (Flexible Design)

In following Chapter 3, you can find brief design implementation details using generalized arithmetic operation scheme.

In this section, new V_{TH} extraction methods based on arithmetic operation are presented. The arithmetic operation scheme is examined two ways such as basic and generalized each using three different methods. These methods which depend on biasing the MOSFETs in triode region are IDPC method, ICPD method and Flexible Method, respectively. All these methods utilize the DDA functional block to realize the required arithmetic operation.

We have also mentioned that, the arithmetic operation which helps to extract V_{TH} are examined in two ways named basic and generalized operation schemes. Extractor circuits which realize both basic and generalized operation have been implemented in Chapter 3.

3. DEVELOPMENT OF V_{TH} EXTRACTORS

As mentioned before, V_{TH} is an important parameter in MOSFET operation so we want to extract V_{TH} of MOSFETs to use for different purposes.

We have proved in Chapter 2 that, V_{TH} of MOS (for both polarities) can be extracted with the help of new presented method. New V_{TH} extractor circuits are designed based on these methods. All proposed methods use common idea of the arithmetic operation obtained with the help of auxiliary components.

In this section, we will first give detailed design of auxiliary components and then explain the extractor circuit implementations based on the new methods explained in Chapter 2.

The main idea used by the proposed extractors is the realization of the arithmetic operation which yields V_{TH} at the output, under some matching conditions. By the use of small V_{DS} voltages, the additional terms dependent on V_{DS} voltage will be eliminated by the help of arithmetic operation and the output will be independent of V_{DS1} and $V_{DS2.}$ In addition to basic arithmetic operation realizing "$V_O = 2V_{GS1} - V_{GS2}$", the idea of "generalized operation" is confirmed with designs realizing "$Vo = 3V_{GS1} - 2V_{GS2} = V_{TH}$" and "$Vo = 4V_{GS1} - 3V_{GS2} = V_{TH}$" by the use of appropriate proportion for applied drain-source voltage.

3.1 Implementation of Auxiliary Components of V_{TH} Extractors

In the V_{TH} extractor circuits, proposed here, there are two auxiliary components;

1. OPAMP
2. DDA
3. Simple Voltage Divider

which help to obtain V_{TH} as an output.

3.1.1 OPAMP (Operational Amplifier) Design

In V_{TH} extractor, a basic two-stage operational amplifier is used to bias the MOSFET in linear region. We use the advantage of the node relations of OPAMP to keep the V_{DS} of the MOSFET at a desired.

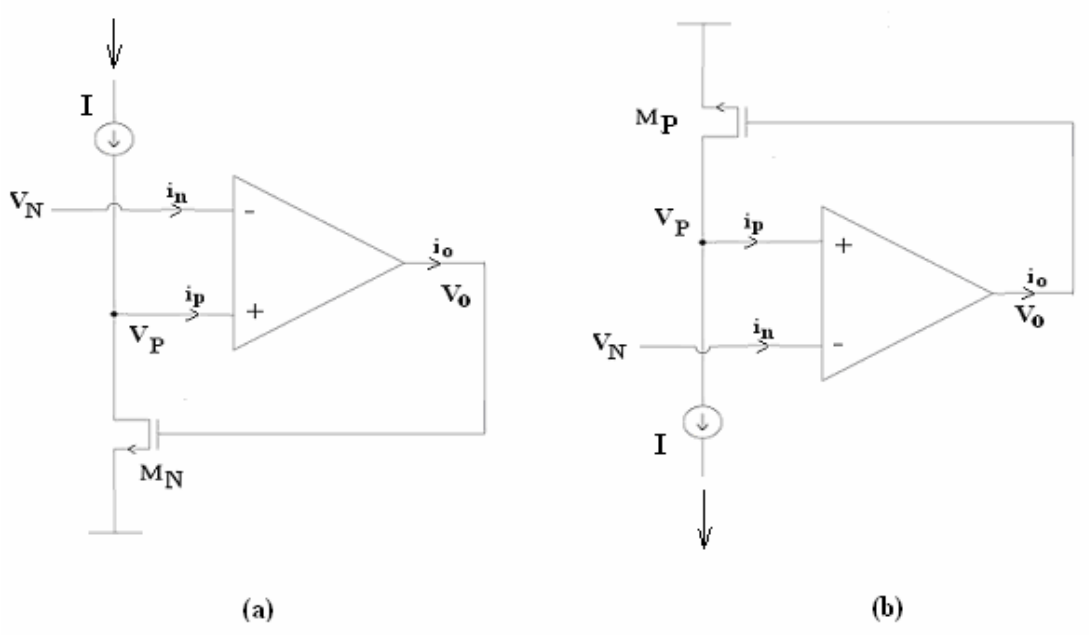


Figure 3.1: Block diagram of OPAMP (a) for NMOS bias (b) for PMOS bias.

Node relations of OPAMP are,

$$V_P = V_N \tag{3.1}$$

$$i_n = i_p = 0 \tag{3.2}$$

$$V_O = A_V.(V_P - V_N) \tag{3.3}$$

The open-loop voltage gain of the amplifier is calculated with the help of calculation of the voltage-gains of two stages separately and multiplication of the results.

$$A_{V1} = \frac{g_{m1}}{g_{o2} + g_{o4}} \tag{3.4}$$

$$A_{V2} = \frac{g_{m8}}{g_{o8} + g_{o7}} \quad \textbf{(3.5)}$$

At the end of multiplication (3.6) is obtained.

$$A_V = A_{V1}.A_{V2} \quad \textbf{(3.6)}$$

The implementation of amplifier is shown in Figure 3.2.

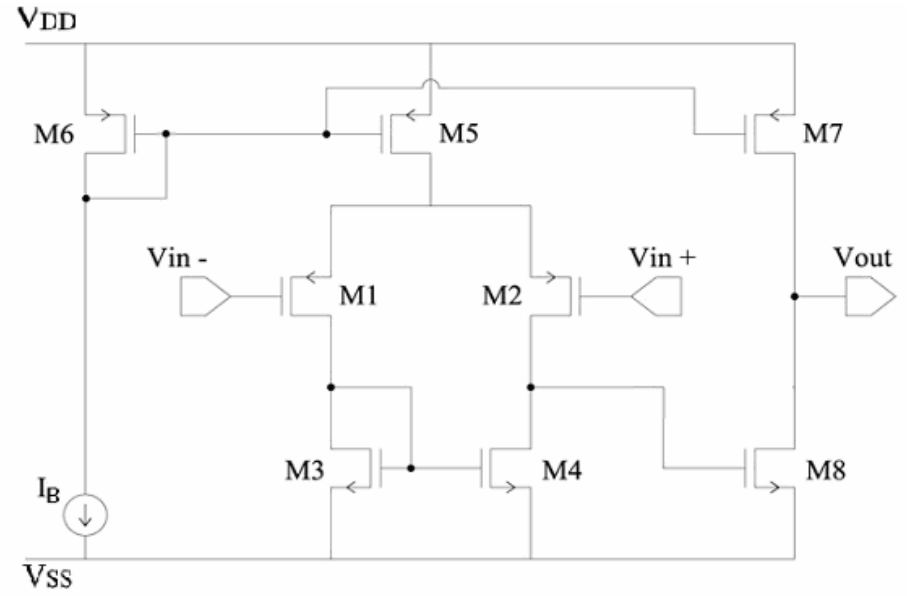


Figure 3.2: Schematic of Operational Amplifier.

Table 3.1: Transistor Ratios of OPAMP

Transistor	**Type**	**W(μm)**	**L(μm)**
M1	PMOS	13	8
M2	PMOS	13	8
M3	NMOS	10	8
M4	NMOS	10	8
M5	PMOS	12	4
M6	PMOS	12	4
M7	PMOS	23	4
M8	NMOS	40	8

PMOS transistor based input stage is formed to perform design conditions. The bias current is chosen $2\mu A$ and transistor aspect ratios are listed in Table 3.1. The current mirroring ratio is 2.

In order to determine the input range designed OPAMP, it is configured as a buffer. The simulation results in Figure 3.3 show that the relation (3.1) is valid between -2.5V and 1.8V because of the limitation coming from PMOS-input pair.

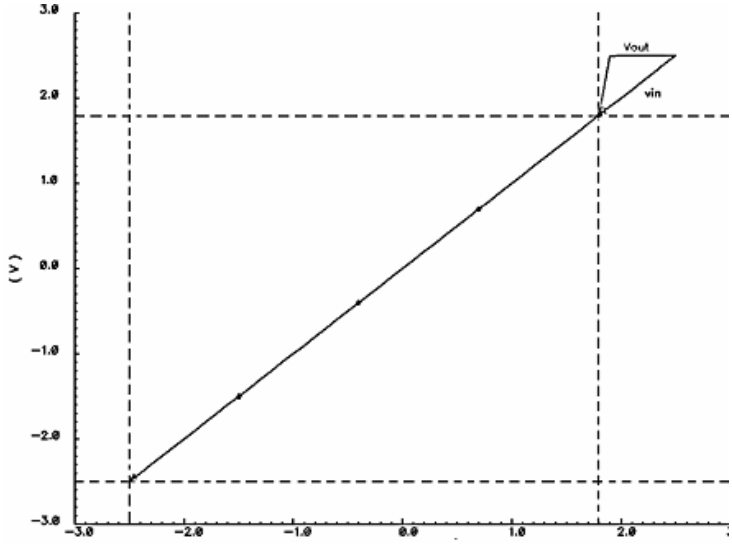


Figure 3.3: Transfer characteristic of OPAMP configured as a buffer

3.1.2 Design of DDA (Differential Difference Amplifier)

The Differential Difference amplifier (DDA), whose symbol is shown in Figure 3.4, is a useful CMOS analog building block.

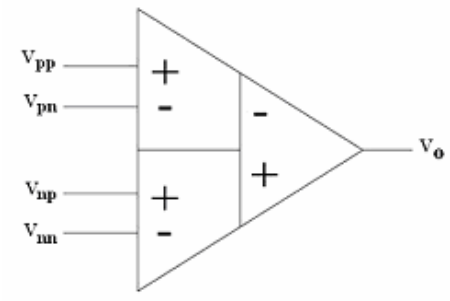


Figure 3.4: Block diagram of Differential Difference Amplifier.

DDA is an extension to the concept of the operational amplifier. Analogous to an ideal operational amplifier, an ideal DDA with negative feedback has a non-inverting

input port (Vpp and Vpn) and an inverting input port (Vnp and Vnn), and (Vpp-Vpn) is equal to (Vnp-Vnn). Therefore, the output voltage (Vo) of an ideal DDA is written in (3.7).

$$V_O = A_V.[(V_{PP} - V_{PN}) - (V_{NP} - V_{NN})] \quad \text{with} \quad A_V \to \infty \qquad \textbf{(3.7)}$$

In V_{TH} extractor design, we realize the arithmetic operation with the help of "DDA based analog adder" applying Vpn =V_1, Vnp=V_2, Vnn=V_3, Vpp=Vo (with negative feedback) as shown in Figure 3.5.

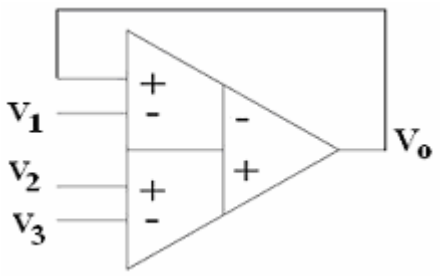


Figure 3.5: DDA Adder/Subtractor.

The arithmetic operation realized by DDA Adder is shown in (3.8),

$$V_O = V_1 + V_2 - V_3 \qquad \textbf{(3.8)}$$

Note that not only no additional components are needed, but also high input impedances are achieved. Some special functions can therefore be realized by this circuit.

The required basic mathematical expression "$2V_{GS1}$-V_{GS2}" is realized by connecting V_{GS1} to both V_1 and V_2 and applying V_{GS2} to V_3 node.

The realization of the DDA is almost the same as that of the OPAMP, but the DDA uses two input differential pairs instead of one. (See Figure 3.6)

The transistor dimensions are listed in Table 3.2. The bias currents (I_B) are chosen $35\,\mu A$.

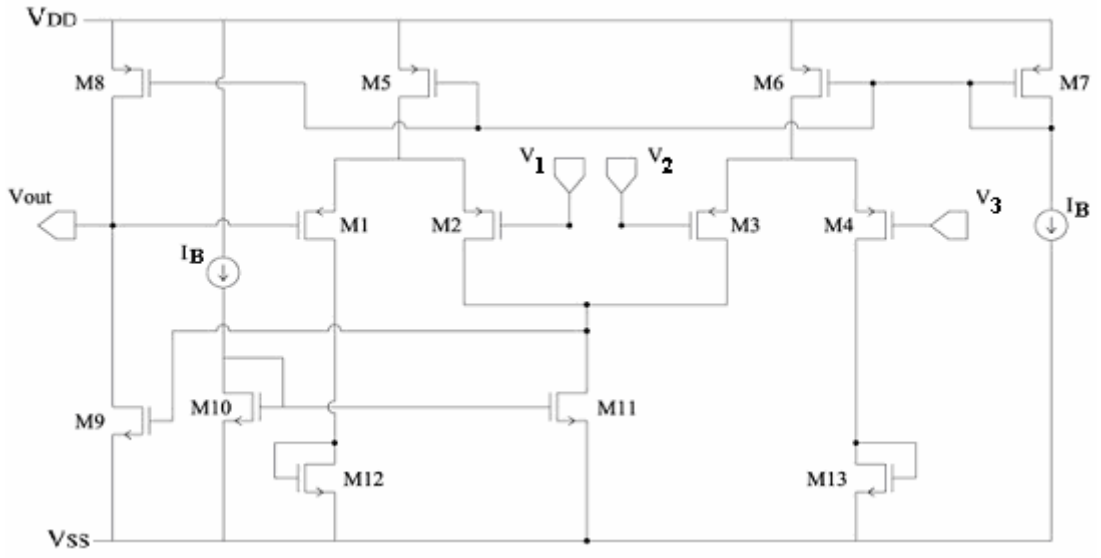


Figure 3.6: Implementation of DDA Circuit.

The experimental result of DDA adder with following inputs is shown in Figure3.7. V_{in1} is a 1V-amplitude sinusoidal input at 1 KHz; V_{in2} is a 500mV-amplitude sinusoidal input at 1 KHz. All inputs have the DC levels -1V. The operation is $V_{out} = 2V_{in1}-V_{in2}$. The result is equal to 1.5V-amplitude sinusoidal output with -1V DC level.

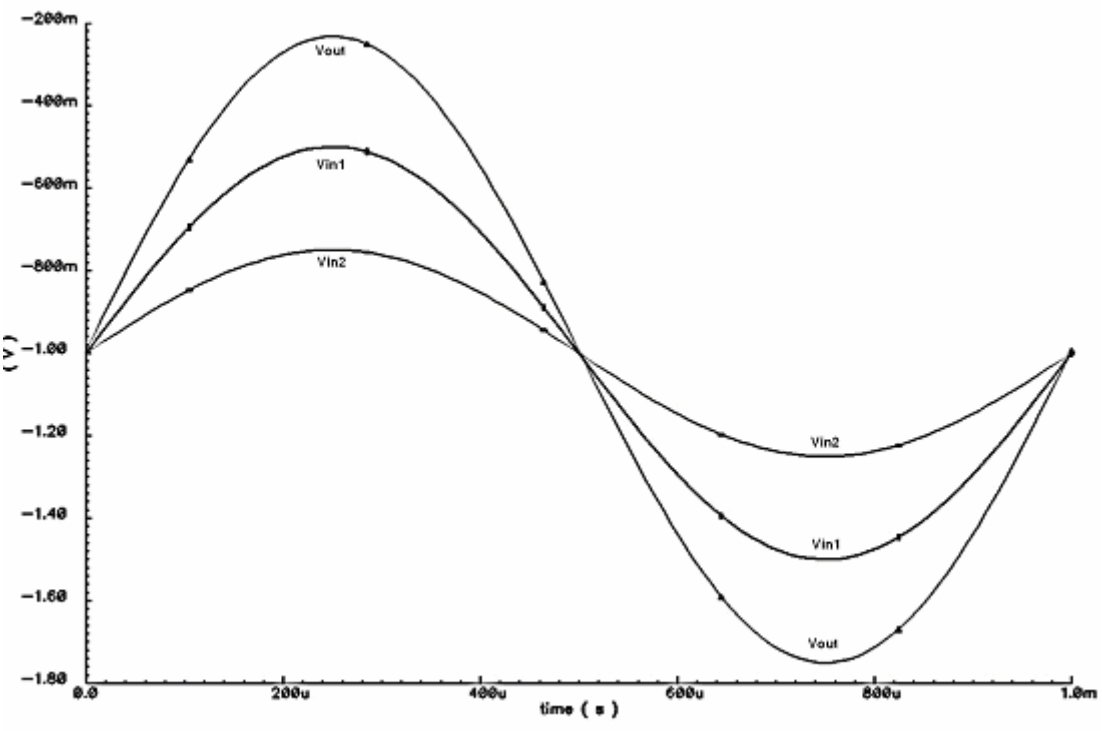


Figure 3.7: Simulation result of DDA adder realizing the arithmetic operation $V_O=2V_{in1}-V_{in2.}$

Table 3.2: Transistor Ratios of DDA Adder.

Transistor	Type	W(μm)	L(μm)
M1	PMOS	28	16
M2	PMOS	28	16
M3	PMOS	28	16
M4	PMOS	28	16
M5	PMOS	25	8
M6	PMOS	25	8
M7	PMOS	25	8
M8	PMOS	25	8
M9	NMOS	6	2
M10	NMOS	6	2
M11	NMOS	6	2
M12	NMOS	3	2
M13	NMOS	3	2

3.1.3 Simple Voltage Divider Design

We have dwelled upon that small drain-source voltages are applied to the negative inputs of the OPAMPs order to bias transistors in triode region. When they are biased in triode, the proportional usage of drain source voltages will eliminate the V_{DS} related term at the output. As a result we can say, the proportion between V_{DS1} and V_{DS2} is one of the most important design conditions to obtain V_{TH}.

In proposed extractor implementation, V_{DS1} and V_{DS2} can be formed to be applied either separately or single from one bias with the use of a voltage divider given in Figure 3.8.

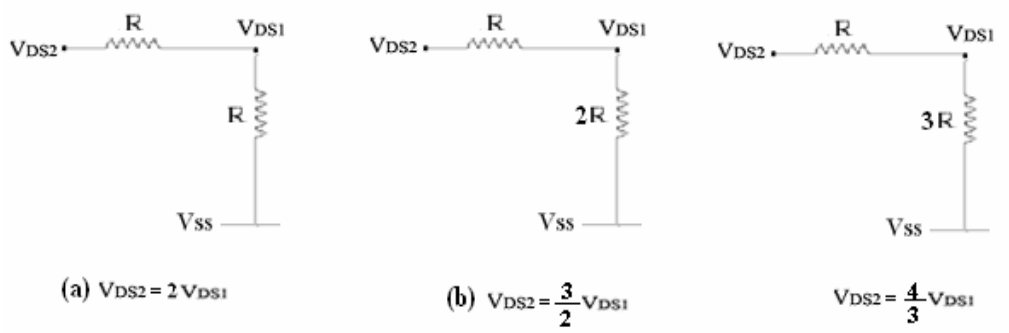


Figure 3.8 Different implementations of Voltage divider

3.2 Implementation of V_{TH} Extractors Based on Basic Arithmetic Operation

All V_{TH} extractors, designed in this section, are based on the arithmetic operation "$2V_{GS1}$-V_{GS2}" which is commonly used in existing methods.

3.2.1 NMOS V_{TH} Extractor Circuits

V_{TH} extractor extracts the threshold voltage of a NMOS device which is also called V_{TN} extractor. (See Figure 3.9) Three new V_{TN} extractor circuit design details, based on the methods described in Chapter 2, are given in this section.

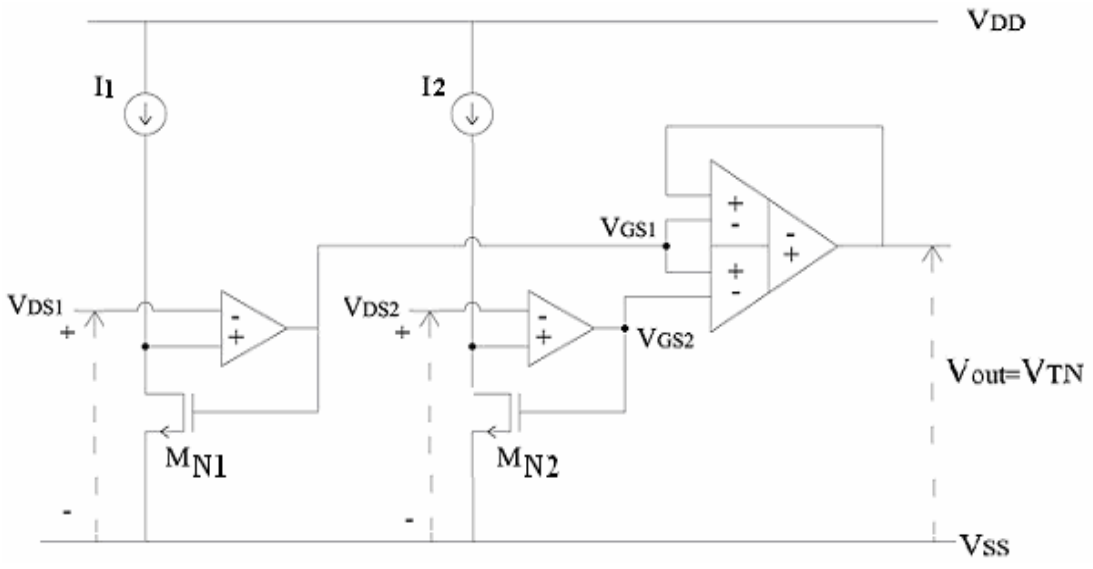


Figure 3.9: Realizing NMOS V_{TH} Extractor

To obtain V_{TH} as an output, M_{N1} and M_{N2} are biased to operate in strong-inversion (triode) region. Drain currents of transistors can be written as,

$$I_D = \beta.(V_{GS} - V_{TH\,N} - \frac{V_{DS}}{2}).V_{DS} \quad \textbf{(3.9)}$$

V_{TN} extraction scheme is formed by two biased NMOS which receives bias currents I_{D1} and I_{D2}, and develop the gate-source voltages V_{GS1} and V_{GS2}, respectively.

M_{N1} and M_{N2} are forced to operate in triode region with the help of DC voltages V_{DS1} and V_{DS2} which applied to the positive inputs of OPAMPs. A simple voltage divider circuit, shown in Figure 3.8 (a), is used to apply drain-source voltages.

The DDA based adder satisfies the output voltage equal to "Vo = $2V_{GS1}$- V_{GS2}" and this directly yields V_{TH} voltage. This result is obtained under the assumption of V_{TH1}= V_{TH2}= $V_{TH.}$

The transistor level schematic of V_{TN} extractor is given in Figure 3.10.

3.2.1.1 V_{TN} Extractor Circuit Based on IDPC Method

Assuming that M_{N1} and M_{N2} are matched (M_N); the implementation of the extractor is given in Figure 3.11. M_{N1} supplies the unit current I. Four units of this device are combined to construct the scaled current source of M_{N2}. We use proportional V_{DS} voltages to eliminate plus term extracted at the end of the operation at DDA.

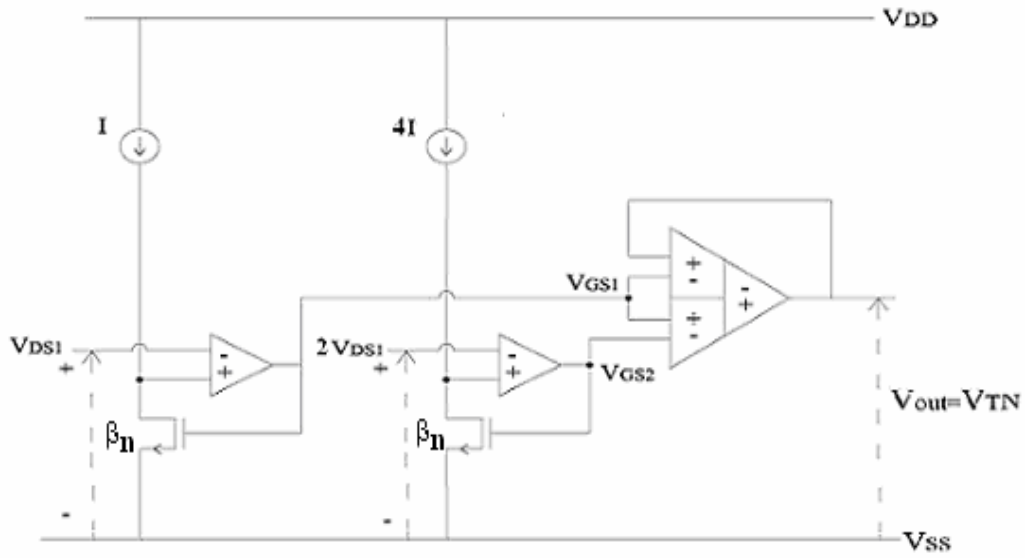


Figure 3.11: Schematic of V_{TN} Extractor based on IDPC Method

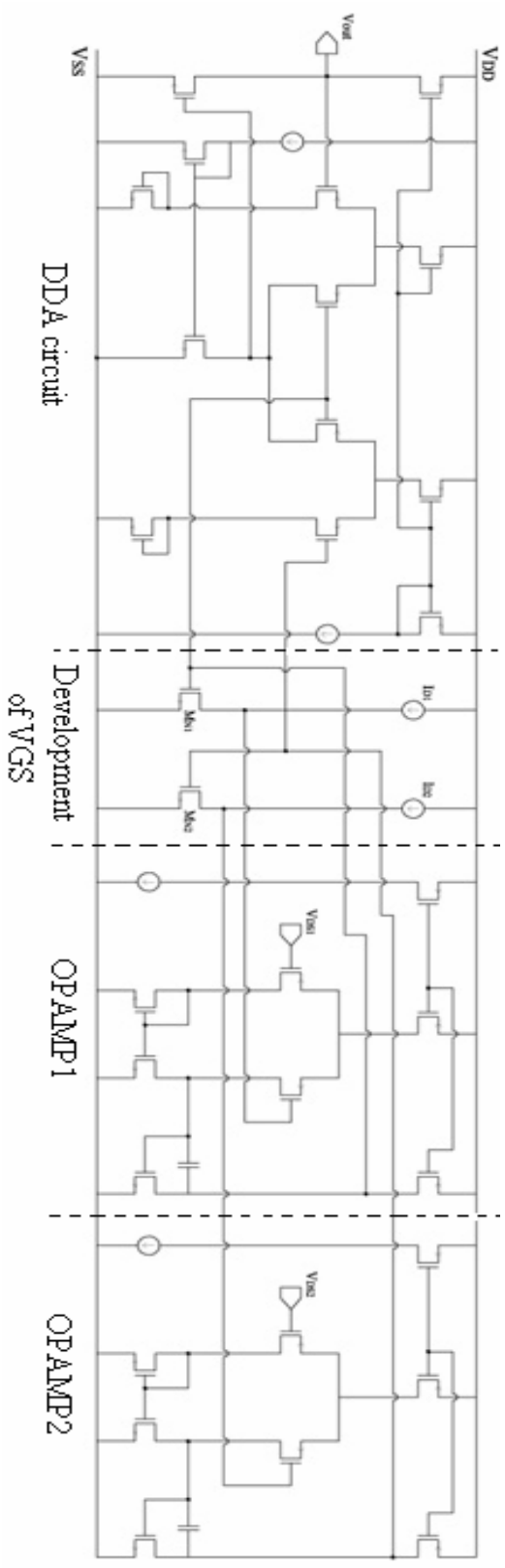


Figure 3.10: Schematic of V_{TN} Extractor

The conditions $V_{DS2} = 2V_{DS1}$, $\beta_1 = \beta_2 = \beta$ and $I_2 = 4I_1$ are formed as in Figure3.11. Additionally, W/L ratios of the chosen transistors are listed in Table 3.3.

Table 3.3: Transistor Ratios of V_{TN} Extractor based on IDPC Method

Device	Type	W(μm)	L(μm)
M_{N1}	NMOS	5	1
M_{N2}	NMOS	5	1

The extracted V_{TN} after simulation is 830mV at 25ºC where operation point information gives 840.1mV, when unit current is chosen 5μA. The result is obtained with %1.2 relative error. (Please see Chapter 5 for detailed results)

3.2.1.2 V_{TN} Extractor Circuit Based on ICPD Method

In identical-currents design, the aspects of two transistors are chosen proportional. The implementation of the circuit is shown in Figure 3.12. M_{N2} has the unit dimension of β. Four units of this device are combined to construct M_{N1}. Here, proportional V_{DS} voltages are used to be able to extract V_{TH} directly.

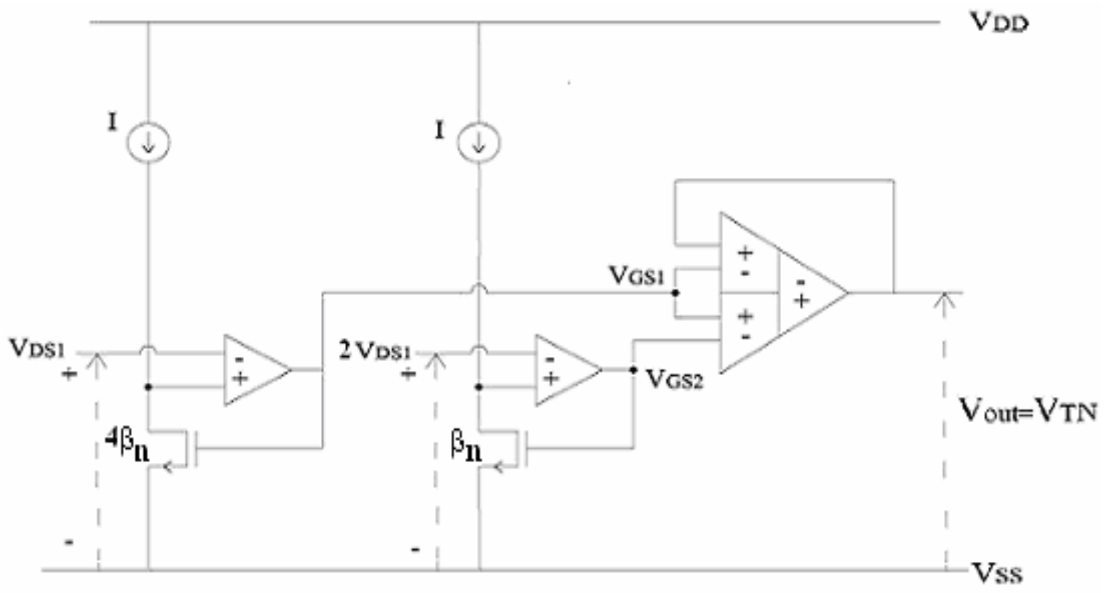


Figure 3.12: Schematic of V_{TN} Extractor based on ICPD Method

Assuming the conditions $V_{DS2} = 2V_{DS1}$, $\beta_1 = 4\beta_2$ and $I_2 = I_1$ are formed. (See Figure 3.12). W/L ratios and current sources listed in Table 3.4.

The extracted V_{TN} after simulation is 830mV while the DC operation gives the value 840.1mV, when current I is chosen 20μA. So the result is obtained with %1.2 error. (Please see Chapter 5 for detailed information)

Table 3.4: Transistor Ratios of V_{TN} Extractor based on ICPD Method

Device	Type	W(μm)	L(μm)
M_{N1}	NMOS	20	1
M_{N2}	NMOS	5	1

3.2.1.3 V_{TN} Extractor Circuit Based on Flexible Method

In Flexible design, the aspects of two transistors and current sources are chosen proportional. The implementation of the circuit is shown in Figure 3.13. M_{N2} has the unit dimension of β. Two units of this device are combined to construct M_{N1}. I_1 will have two units of I_2. In addition, proportional V_{DS} voltages are used to be able to extract V_{TH} directly.

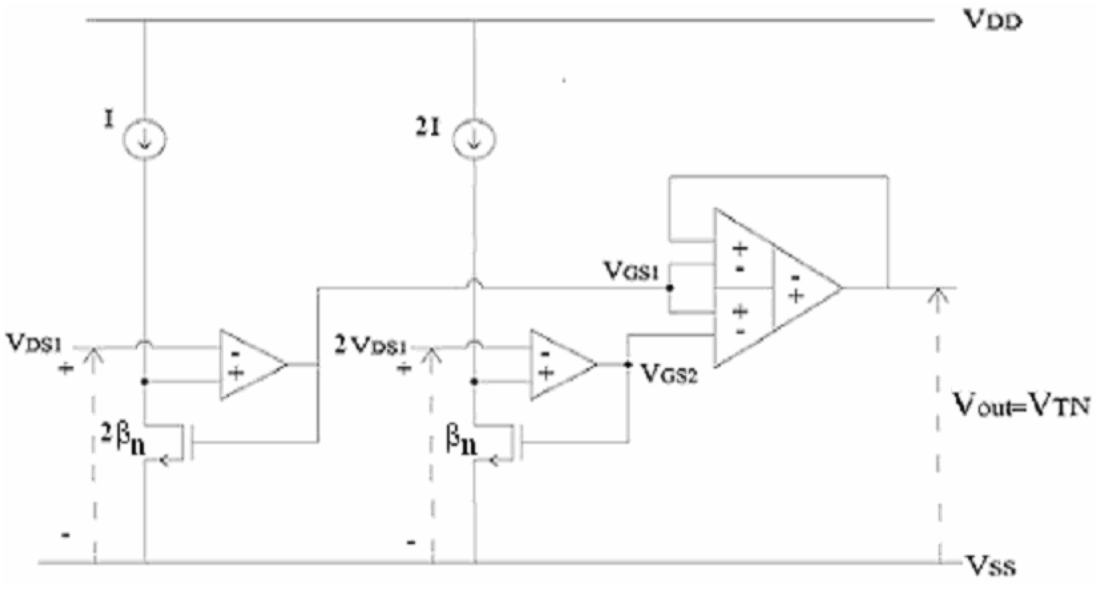


Figure 3.13: Schematic of V_{TN} Extractor based on Flexible Method

Assuming the conditions $V_{DS2} = 2V_{DS1}$, $\beta_1 = 2\beta_2$ and $I_2 = 2I_1$ are formed. (See Figure 3.13). W/L ratios and current sources listed in Table 3.5.

The extracted V_{TN} after simulation is 830mV while the DC operation gives the value 840.1mV, when current I_1 is chosen 5μA and I_2=10μA. So the result is obtained with %1.2 error. (Please see Chapter 5 for detailed information)

Table 3.5: Transistor Ratios of V_{TN} Extractor based on Flexible Method

Device	Type	W(μm)	L(μm)
M_{N1}	NMOS	10	1
M_{N2}	NMOS	5	1

3.2.2 PMOS V_{TH} Extractor Circuits

The V_{TH} extraction method explained in Chapter 2 is also applied to extract threshold voltage of a PMOS device. But the difficulty in design is to bias PMOS devices under strong inversion conditions. In order to perform M_{P1} and M_{P2} operate in linear-region, ground applied to the source of the PMOS devices under control. It is important to note here that bulk and source of the PMOS transistors are tied together in order to avoid body effect.

In this configuration the drain current will be,

$$I_D = \beta.(V_{GS} - |V_{TH\,P}| - \frac{V_{DS}}{2}).V_{DS} \qquad \textbf{(3.10)}$$

The same structure in Figure3.9 is realized with modifications for PMOS in Figure3.14.

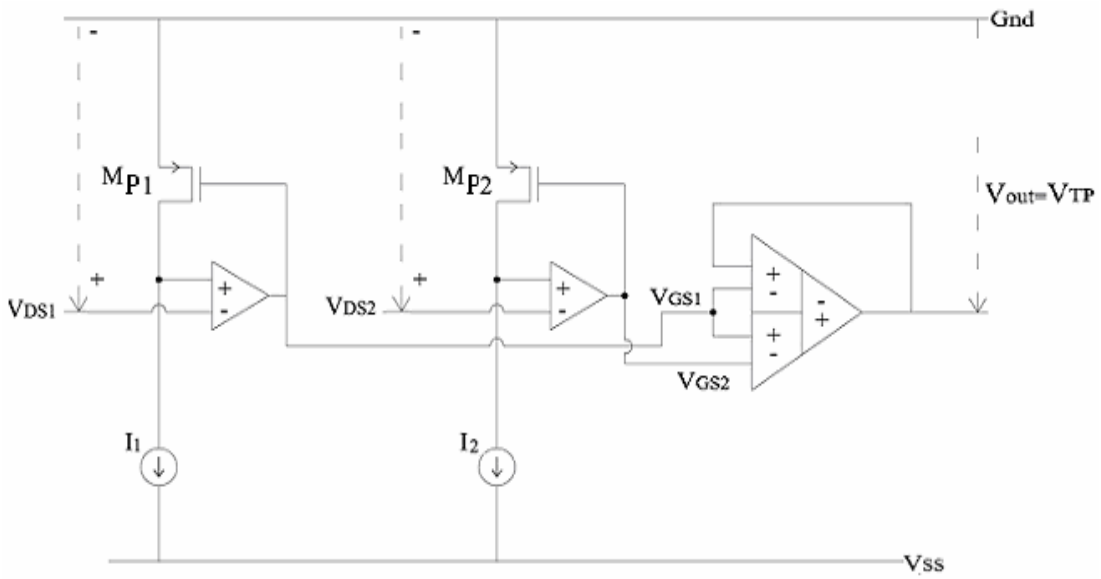


Figure 3.14: Realization of PMOS V_{TH} Extractor

In schematic implementation, OPAMP and DDA circuits are the same, only V_{GS} development part is different from V_{TN} circuit. (See Figure 3.14)

Three V_{TP} Extractor circuits are proposed by the means of design parameters, drain currents and transistor matching.

3.2.2.1 V_{TP} Extractor Circuit based on IDPC Method

Assume that matched transistors are used and M_{P1} supplies the unit current I. Four units of this device are combined to construct the scaled current source of M_{P2}. The implementation of the circuit is shown in Figure 3.16. To acquire V_{TH}, $V_{DS2} = 2V_{DS1}$ must be applied to the positive inputs of the OPAMPs to eliminate plus term extracted at the end of the operation at DDA.

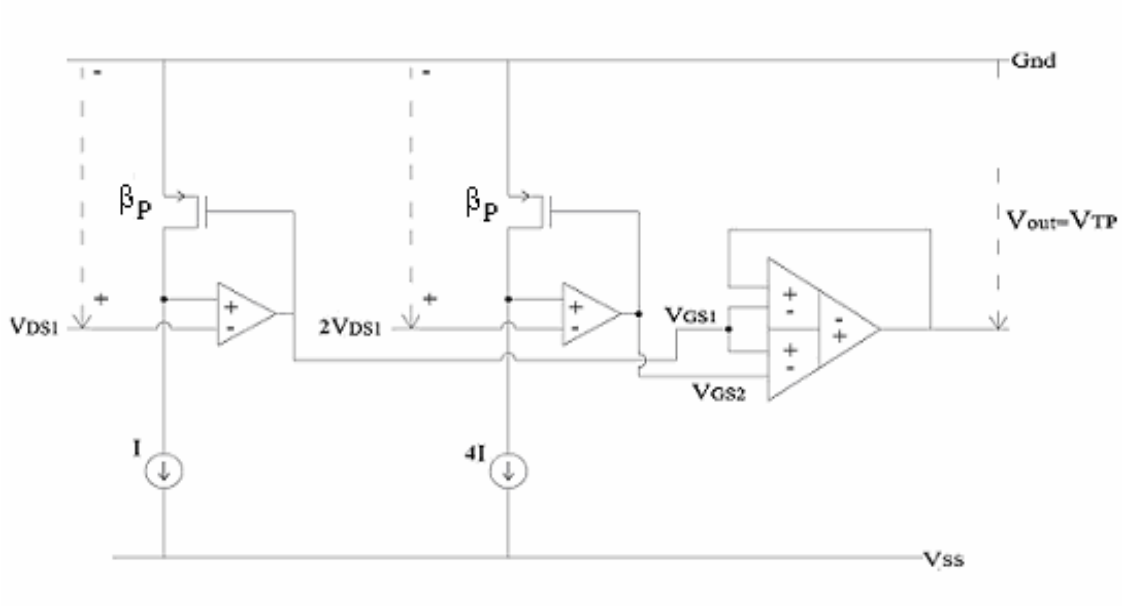


Figure 3.16: Schematic of V_{TP} Extractor based on IDPC Method

W/L ratios of the chosen transistors are listed in Table 3.6.

Table 3.6: Transistor Ratios of V_{TP} Extractor based on based on IDPC Method

Device	Type	W(μm)	L(μm)
M_{P1}	PMOS	5	1
M_{P2}	PMOS	5	1

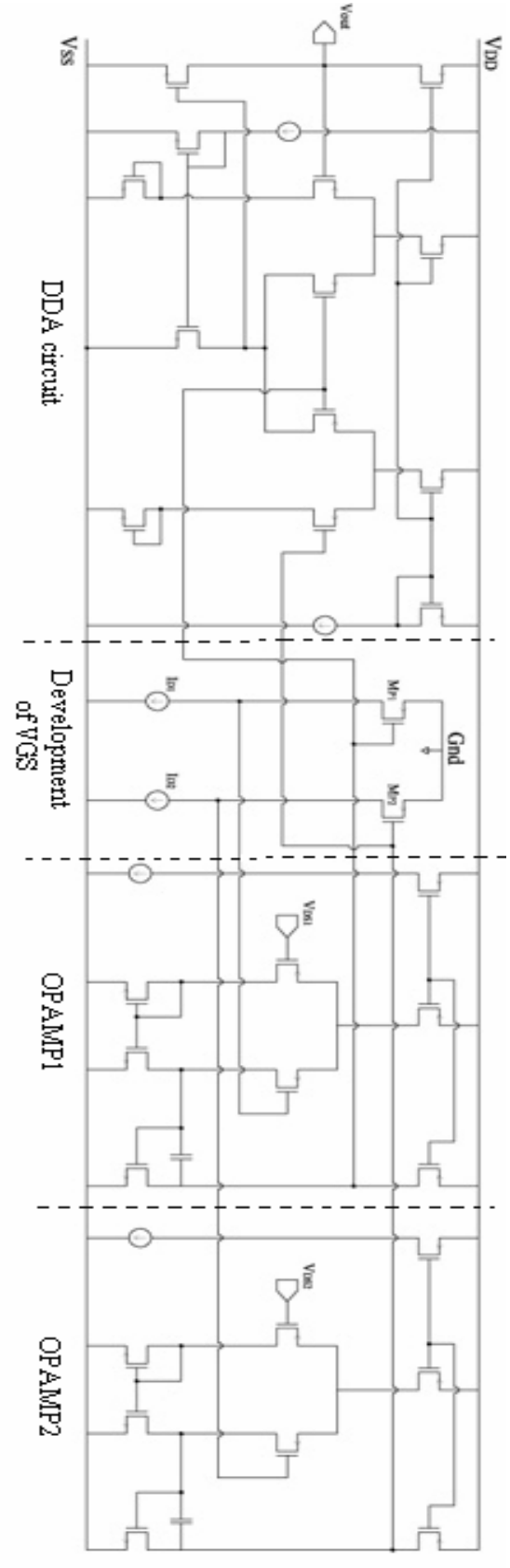


Figure 3.15: Schematic of transistor-level V_{TP} Extractor

The detailed results of the simulations are listed in Chapter 5 in addition to the experimental result of V_{TP} extractor. When unit current is chosen 1μA, the extracted V_{TP} after simulation is -1.063V, obtained with %0.8 relative error, while the DC operation gives the value -1.072V.

3.2.2.2 V_{TP} Extractor Circuit based on ICPD Method

In identical current design, the two transistors are chosen proportional. M_{P2} has the unit dimension β. Four units of this device are combined to construct M_{P1}. The conditions $V_{DS2} = 2V_{DS1}$, $\beta_1 = 4\beta_2$ and $I_2 = I_1$, the schematic of the extractor is shown in Figure 3.17.

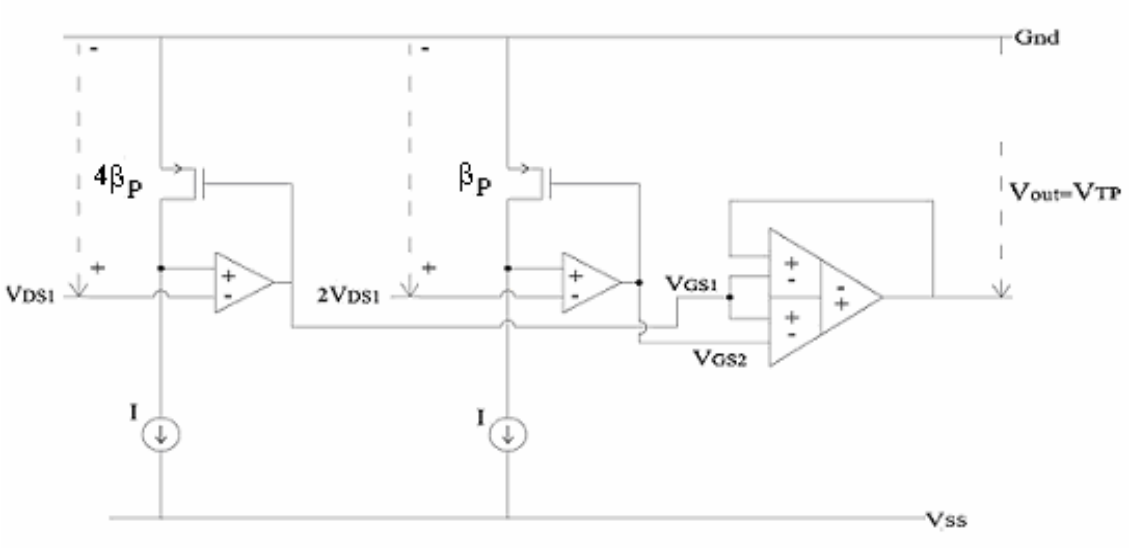


Figure 3.17: Schematic of V_{TP} Extractor based on ICPD Method

W/L ratios of the chosen transistors are listed in Table 3.7.

Table 3.7: Transistor Ratios of V_{TP} Extractor based on ICPD Method

Device	Type	W(μm)	L(μm)
M_{P1}	PMOS	20	1
M_{P2}	PMOS	5	1

When current I is chosen 4µA, the extracted V_{TP} after simulation is -1.063V, while the DC operation gives the value -1.072V, so it is obtained with %0.8 relative error. Related information is detailed in Chapter 5.

3.2.2.3 V_{TP} Extractor Circuit based on Flexible Method

Assume that both PMOS transistors' dimensions have the same proportion with drain current ratio. M_{P1} supplies the unit current I, two units of this device are combined to construct the scaled current source of M_{P2}. In addition, M_{P2} has the unit dimension and M_{P1} has two units of it. The implementation of the circuit is shown in Figure 3.18. To acquire V_{TH}, $V_{DS2} = 2V_{DS1}$ must be applied to the positive inputs of the OPAMPs to eliminate plus term extracted at the end of the operation at DDA.

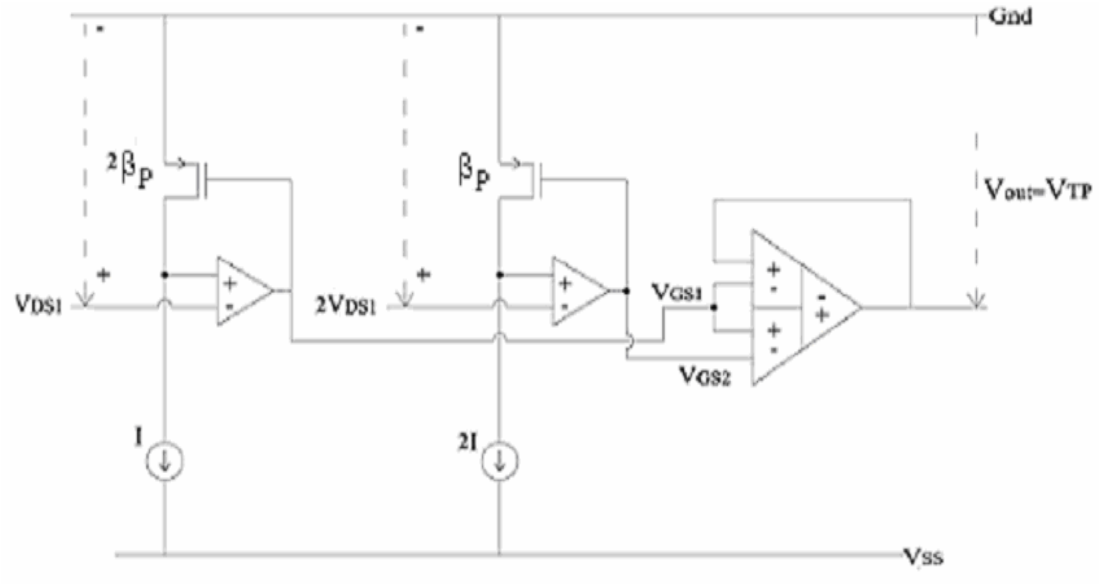


Figure 3.18: Schematic of V_{TP} Extractor based on Flexible Method

W/L ratios of the chosen transistors are listed in Table 3.8.

Table 3.8: Transistor Ratios of V_{TP} Extractor based on based on Flexible Method

Device	Type	W(µm)	L(µm)
M_{P1}	PMOS	10	1
M_{P2}	PMOS	5	1

The detailed results of the simulations are listed in Chapter 5 in addition to the experimental result of V_{TP} extractor. When I1 current is chosen 1µA and I_2=2µA, the

extracted V_{TP} after simulation is -1.063V, obtained with %0.8 relative error, while the DC operation gives the value -1.072V.

3.3 Implementation of V_{TH} Extractor Circuit Based on Generalized Arithmetic Operation

All V_{TH} extractors, designed in this section, are based on the generalized arithmetic operation which is newly used in extractors. Two extractor circuit realizing "$3V_{GS1}$-$2V_{GS2}$" and "$4V_{GS1}$-$3V_{GS2}$" respectively are designed with a few modifications on the same structure.

The main difficulty of this type of extractors is the realization of the arithmetic operation with a circuit. In this work, two cascaded DDAs are used to perform the operations.

3.3.1 NMOS V_{TH} Extractor based on "$3V_{GS1}$-$2V_{GS2}$"

In order to realize the operation $3V_{GS1}$-$2V_{GS2}$= $V_{TH,}$ drain –source voltages should have the proportion of $V_{DS2} = \frac{3}{2} V_{DS1}$. A simple voltage divider circuit, shown in Figure 3.8 (b), is used to apply drain-source voltages.

The next step to be decided is design parameter usage, extractor circuits can be designed in two ways by using following assumptions

- Using IDPC Method: Choosing identical transistors and $\frac{I_2}{I_1} = \frac{9}{4}$ as the current ratio.
- Using IDPC Method: Choose current sources equal and transistor dimensions ratio as $\frac{\beta_1}{\beta_2} = \frac{9}{4}$.

- Flexible Design Method: Choose current sources $\frac{I_2}{I_1}=\frac{3}{2}$ and transistor dimensions ratio as $\frac{\beta_1}{\beta_2}=\frac{3}{2}$.

V_{TN} Extractor based on IDPC Method is implemented using two cascaded DDA.(See Figure 3.19)

Table 3.9: Transistor Ratios of V_{TN} Extractor based on IDPC Method realizing $3V_{GS1}$-$2V_{GS2}$ operation

Device	Type	W(μm)	L(μm)
M_{N1}	NMOS	5	1
M_{N2}	NMOS	5	1

*Current sources I_1 and I_2 are chosen 4μA and 9μA, respectively.

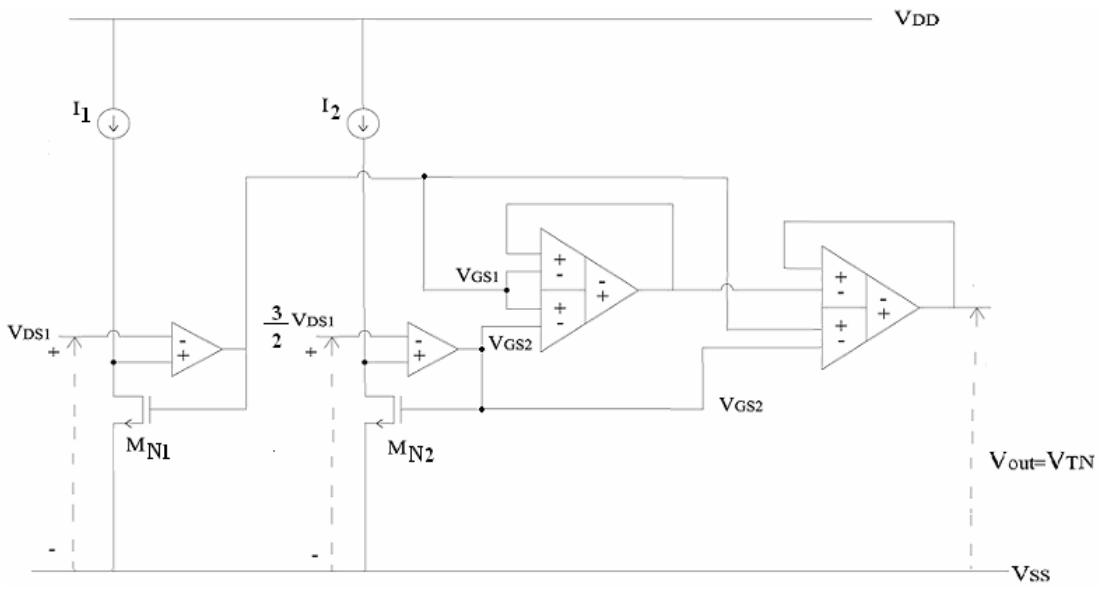


Figure 3.19: V_{TN} extractor circuit based on IDPC Method using "$3V_{GS1}$-$2V_{GS2}$"

3.3.2 NMOS V_{TH} Extractor based on "$4V_{GS1}$-$3V_{GS2}$"

The operation $4V_{GS1}$-$3V_{GS2}$=$V_{TH,}$ is performed with the use of $V_{DS2}=\frac{4}{3}V_{DS1}$, which is realized with a simple voltage divider circuit, shown in Figure 3.8 (c).

The design conditions can be performed in two ways using following assumptions,

- Using IDPC Method: Choosing identical transistors and $\frac{I_2}{I_1}=\frac{16}{9}$ as the current ratio.

- Using IDPC Method: Choose current sources equal and transistor dimensions ratio as $\frac{\beta_1}{\beta_2}=\frac{16}{9}$.

- Flexible Design Method: Choose current sources $\frac{I_2}{I_1}=\frac{4}{3}$ and transistor dimensions ratio as $\frac{\beta_1}{\beta_2}=\frac{4}{3}$.

IDPC Method is performed to extract threshold voltage of NMOS using two cascaded DDA to realize the arithmetic operation. (See in Figure 3.20)

Table 3.10: Transistor Ratios of V_{TN} Extractor based on IDPC Method realizing $4V_{GS1}$-$3V_{GS2}$ operation

Device	**Type**	**W(μm)**	**L(μm)**
M_{N1}	NMOS	5	1
M_{N2}	NMOS	5	1

*Current sources I_1 and I_2 are chosen 9μA and 16μA, respectively.

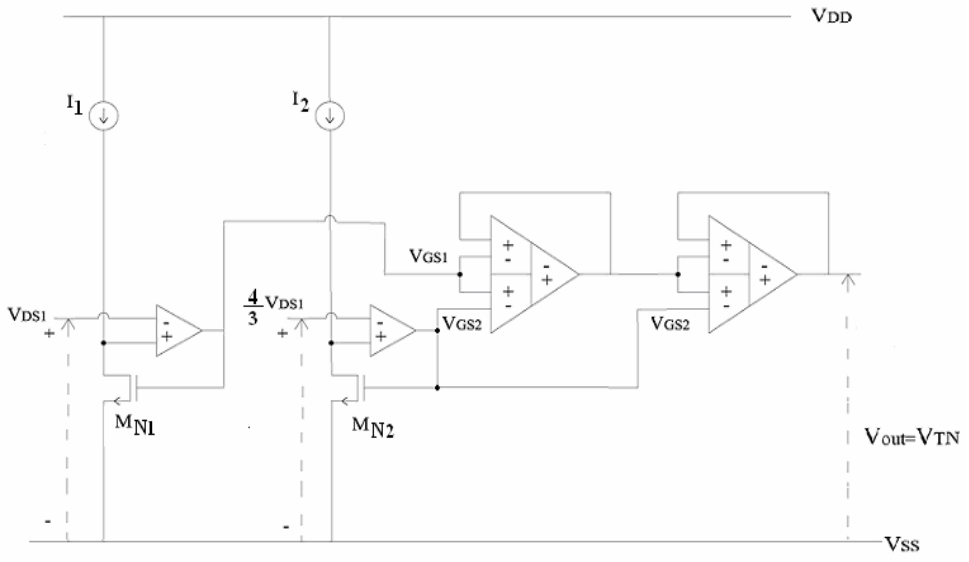


Figure 3.20: V_{TN} extractor circuit based on IDPC Method "$4V_{GS1}$-$3V_{GS2}$"

The disadvantage of the extraction circuits designed using generalized arithmetic operation is the chip area. NMOS V_{TH} extractors based on this technique are given above. The same structure is also applicable to PMOS V_{TH} extractors with appropriate modifications.

4. NON-IDEALITIES IN NEW V_{TH} EXRACTION SCHEME

In this section, we will consider the effect of nonidealities of the MOS transistor on the performance of V_{TH} extractors, based on basic and generalized arithmetic operation. The main nonideality sources associated with MOS devices are mobility reduction, channel-length modulation, mismatch, body effect, and temperature dependency, causing discrepancies from the expected output values.

4.1 Mobility Reduction

The mobility of electrons in the inversion layer is smaller than bulk mobility due to an increasing electric field. For a given temperature, this surface mobility depends primarily on the gate field and may be modeled approximately by,

$$\mu = \frac{\mu_0}{1 + \theta(V_{GS} - V_{TH})} \tag{4.1}$$

where μ_0 represents zero field mobility of carriers and θ is the coefficient of the effect of field on the mobility.

The drain current in linear region is expressed including the effect of mobility reduction,

$$I_D = \frac{\beta . V_{DS}}{[1 + \theta(V_{GS} - V_{TH})]}(V_{GS} - V_{TH} - \frac{V_{DS}}{2}) \tag{4.2}$$

writing V_{GST} instead of the $(V_{GS} - V_{TH})$ the equation will be,

$$I_D = \frac{\beta . V_{DS}}{[1 + \theta V_{GST}]}(V_{GST} - \frac{V_{DS}}{2}) \tag{4.3}$$

$$V_{GST} = \frac{I_D}{[\beta.V_{DS} - \theta.I_D]} + \frac{\beta.V_{DS}^{\ 2}}{2(\beta.V_{DS} - \theta.I_D)} \quad \textbf{(4.4)}$$

The gate-source voltage will be equal to,

$$V_{GS} = \frac{I_D}{[\beta.V_{DS} - \theta.I_D]} + \frac{\beta.V_{DS}^{\ 2}}{2(\beta.V_{DS} - \theta.I_D)} + V_{TH} \quad \textbf{(4.5)}$$

At the end of the arithmetic operation, output will have the following discrepancies caused by mobility reduction.

$$\varepsilon_\theta = V_O(\text{with}\theta) - V_O \quad \textbf{(4.6)}$$

- The results of the proposed extractors based on $V_O = 2V_{GS1} - V_{GS2}$ arithmetic operation are affected from mobility reduction.

    1. By the use of Identical Dimensions ($\beta_1 = \beta_2 = \beta$)-Proportional Currents (I_2=4I_1) Method,

$$\varepsilon_\theta = V_{TH} - \frac{\theta.I_1.(2.I_1 + \beta.V_{DS1}^{\ 2})}{(\beta^2.V_{DS1}^{\ 2} - 3.\theta.I_1.\beta.V_{DS1} + 2.\theta^2.I_1^{\ 2})} \quad \textbf{(4.7)}$$

    2. By the use of Identical Currents (I_1=I_2=I)-Proportional Dimensions ($\beta_1 = 4.\beta_2$) Method,

$$\varepsilon_\theta = V_{TH} - \frac{\theta.I.(I + 2.\beta_2.V_{DS1}^{\ 2})}{(8.\beta_2^{\ 2}.V_{DS1}^{\ 2} - 6.\beta_2.V_{DS1}.\theta.I + \theta^2.I^2)} \quad \textbf{(4.8)}$$

    3. By the use of Flexible Method (Proportional Current (I_1=2I_2)-Proportional Dimensions($\beta_1 = 2.\beta_2$)),

$$\varepsilon_\theta = V_{TH} - \frac{\theta.I.(2I + 2.\beta_2.V_{DS1}^{\ 2})}{(4.\beta_2^{\ 2}.V_{DS1}^{\ 2} - 3.\beta_2.V_{DS1}.\theta.I + 4.\theta^2.I^2)} \quad \textbf{(4.9)}$$

- The proposed extractor based on $V_O = 3V_{GS1} - 2V_{GS2}$ arithmetic operation is affected from mobility reduction as in the following.

By the use of Identical Dimensions ($\beta_1 = \beta_2 = \beta$)-Proportional Currents (I_1=4I and $I_{2=}$ 9I) Method

$$\varepsilon_\theta = V_{TH} - \frac{(36.\theta.I^2 + 3/8.\beta^2.V_{DS1}{}^3)}{(3/2.\beta^2.V_{DS1}{}^2 - 15.\beta.V_{DS1}.\theta.I + 36.\theta^2.I^2)} \quad \textbf{(4.10)}$$

- The proposed extractor based on $V_O = 4V_{GS1} - 3V_{GS2}$ arithmetic operation is affected from mobility reduction as in the following.

  By the use of Identical Dimensions ($\beta_1 = \beta_2 = \beta$)-Proportional Currents (I_1=9I and I_2= 16I) Method

$$\varepsilon_\theta = V_{TH} - \frac{(144.\theta.I^2 + 2/9.\beta^2.V_{DS1}{}^3)}{(4/3.\beta^2.V_{DS1}{}^2 - 28.\beta.V_{DS1}.\theta.I + 144.\theta^2.I^2)} \quad \textbf{(4.11)}$$

4.2 Channel-Length Modulation

Channel-length modulation is another nonideality in connection with MOS transistors. In proposed V_{TH} extractors, the transistors under test are biased in triode region with the use of very small V_{DS} voltages so they are not affected from channel length modulation.

4.3 Body Effect

The bulks of all NMOS and PMOS transistors in proposed V_{TH} extractors are tied V_{SS} and V_{DD}, respectively. Because, an NMOS device, whose source not connected to V_{SS} or a PMOS device whose source not connected to V_{DD} will suffer from body effect.

Therefore, the relationship between V_{TH} and V_{BS} can be written as for NMOS,

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F}) \quad \textbf{(4.12)}$$

For PMOS,

$$|V_{TH}| = |V_{TH0}| + \gamma(\sqrt{|2\phi_F - V_{BS}|} - \sqrt{|2\phi_F|}) \quad \textbf{(4.13)}$$

In proposed extractors, the bulk and the source terminals of the MOS devices are tied together (V_{BS}=0) in order to avoid body effect. Thus, the extracted V_{TH} values are not affected from body effect.

4.4 Mismatch

Processing non-idealities occur due to mismatches during fabrication. In general, these mismatches can be classified into two categories:

The discussion will proceed centered around the M_2 which is considered as a reference transistor.

1. **V_{TH} mismatch:** During fabrication, mismatch in V_{TH} is primarily caused by variations in the gate oxide thickness and channel doping. V_{TH} is affected as,

$$V_{TH1} = V_{TH2} + \Delta V_{TH} \quad \textbf{(4.14)}$$

2. **Size mismatch:** These mismatches are probably the most dominant source of error in integrated circuits. For proposed circuits, M_1 and M_2 should match each other and can be modeled with mismatch,

$$\beta_1 = \beta_2 + \Delta\beta \quad \textbf{(4.15)}$$

Current sources will have mismatch because of device size, and can be given as:

$$I_2 = I_1 + \Delta I \quad \textbf{(4.16)}$$

At the end of the arithmetic operation, output will have discrepancies (ε_Δ) in presence of V_{TH} and size mismatch.

$$\varepsilon_{\Delta} = V_O(\text{with}\Delta) - V_O \quad \textbf{(4.17)}$$

- The results of the proposed extractors based on $V_O = 2V_{GS1} - V_{GS2}$ arithmetic operation is affected by mismatches as in the following,

  1. By the use of Identical Dimensions ($\beta_1 = \beta_2 + \Delta\beta$)-Proportional Currents ($I_2 = 4(I_1 + \Delta I)$) Method,

$$\varepsilon_{\Delta} = V_{TH2} + (2.\Delta V_{TH}) - \frac{2.(\Delta\beta.(I_1 + \Delta I) + \beta_2.\Delta I)}{V_{DS1}.\beta_2.(\beta_2 + \Delta\beta)} \quad \textbf{(4.18)}$$

  2. By the use of Identical Currents ($I_2 = I_1 + \Delta I$)-Proportional Dimensions ($\beta_1 = 4.(\beta_2 + \Delta\beta)$) Method,

$$\varepsilon_{\Delta} = V_{TH2} + (2.\Delta V_{TH}) - \frac{I.(\Delta\beta.(I_1 + \Delta I) - \beta_2.\Delta I)}{2.V_{DS1}.\beta_2.(\beta_2 + \Delta\beta)} \quad \textbf{(4.19)}$$

  3. By the use of Flexible Method (Proportional Current (I_1=2I_2)-Proportional Dimensions($\beta_1 = 2.\beta_2$)),

$$\varepsilon_{\Delta} = V_{TH2} + (2.\Delta V_{TH}) - \frac{I.(\Delta\beta.(I_1 + \Delta I) - \beta_2.\Delta I)}{V_{DS1}.\beta_2.(\beta_2 + \Delta\beta)} \quad \textbf{(4.20)}$$

- The results of the proposed extractors based on $V_O = 3V_{GS1} - 2V_{GS2}$ arithmetic operation is affected by mismatches as in the following,

  By the use of Identical Dimensions ($\beta_1 = \beta_2 + \Delta\beta$)-Proportional Currents ($I_2 = \frac{9}{4}(I_1 + \Delta I)$) Method,

$$\varepsilon_{\Delta} = V_{TH2} + (2.\Delta V_{TH}) - \frac{2(\Delta\beta.(2.I_1 + \Delta I) + \beta_2.(2{,}5.I_1 + \Delta I))}{3.V_{DS1}.\beta_2.(\beta_2 + \Delta\beta)} \quad \textbf{(4.21)}$$

- The results of the proposed extractors based on $V_O = 4V_{GS1} - 3V_{GS2}$ arithmetic operation is affected by mismatches as in the following,

By the use of Identical Dimensions ($\beta_1 = \beta_2 + \Delta\beta$)-Proportional Currents ($I_2 = \frac{16}{9}(I_1 + \Delta I)$) Method,

$$\varepsilon_\Delta = V_{TH2} + (2.\Delta V_{TH}) - \frac{6(\Delta\beta.(I_1 + \Delta I) + \beta_2.(I_1/3 + \Delta I))}{V_{DS1}.\beta_2.(\beta_2 + \Delta\beta)} \quad \textbf{(4.22)}$$

4.5 Temperature Dependency

The threshold voltage will be function on temperature because of the temperature dependence of MOS transistor parameters: the carriers' mobility, Fermi potential and carriers' intrinsic concentration.

The temperature behavior of the threshold voltage can be described as,

$$V_{TH}(T) = V_{TH0} - \alpha_T(T - To) \quad \textbf{(4.23)}$$

where T is absolute temperature, To is room absolute temperature and α_T is constant.

Drain current and mobility varies with temperature.

$$I_D(T) = I_{D0}.[1 + \gamma.(T - To)] \quad \textbf{(4.24)}$$

$$\beta(T) = \beta o\left(\frac{T}{To}\right)^{-m} \quad \textbf{(4.25)}$$

With the help of these equations gate-source voltage can be written as:

$$V_{GS}(T) = \frac{I_{DO}[1 + \gamma(T - To)]\left(\frac{T}{To}\right)^{m}}{\beta o.V_{DS}} + \frac{V_{DS}}{2} + [V_{TH0} - \alpha(T - To)] \quad \textbf{(4.26)}$$

At the end of the arithmetic operations like $V_O(T) = 2V_{GS1}(T) - V_{GS2}(T)$ and $V_O(T) = 3V_{GS1}(T) - 2V_{GS2}(T)$ or $V_O(T) = 4V_{GS1}(T) - 3V_{GS2}(T)$, output is obtained as in the following:

$$V_O(T) = V_O(To) - \alpha_T.(T - To) \quad \textbf{(4.27)}$$

If temperature is increased by Δ_T, meaning that $T = To + \Delta_T$.

We find the change of the output voltage with temperature as:

$$\varepsilon_T = -\alpha(T - To) = -\alpha_T.\Delta_T \quad \textbf{(4.28)}$$

The temperature coefficient of the proposed extractor can be expressed as:

$$\frac{\varepsilon_T}{\Delta_T} \cong \frac{\partial.Vo(T)}{\partial T} \cong -\alpha_T \quad \textbf{(4.29)}$$

The output voltage of the proposed V_{TN} circuits exhibited an almost constant negative slope, $-1.42mV/^{\circ}C$, with temperature and both can be used as a CTAT (Complementary to Absolute Temperature) voltage reference. (Please refer to Figure 5.7, Figure 5.8 and Figure 5.9)

The output voltage of the proposed PMOS V_{TH} extractors referenced to ground exhibited a positive slope of $1.99mV/^{\circ}C$ with respect to the temperature. Thus, both can be formed as PTAT (Proportional to Absolute Temperature) voltage references. (Please see Figure 5.10, Figure5.11 and Figure 5.12)

5. SIMULATION RESULTS OF NEW V_{TH} EXTRACTORS

In this section, the proposed NMOS and PMOS V_{TH} extractor circuits given in Chapter 3 are simulated with Cadence-SpectreS based on 0.35µm nwell CMOS BSIM3v3 technology file which is provided by AMS (Austria Micro Systems). The supply voltage is $\mp 2.5V$.

The important point which must be observed in simulations is applied drain currents because they determine the operation region of the transistor under test. If drain current is chosen too small, our design will not outcome V_{TH}, because transistors will work in weak inversion or saturation region where design conditions are not performed. In addition, we should keep from high values of drain current which will result high V_{GS} voltages that will not realize V_{TH} at the output of DDA because of the DDA input range limitations and cause mobility reduction effects. In order to keep away mobility degradation due to high V_{GS}, we have also chosen proper bias conditions and device dimensions to prevent V_{GS} to go higher values.

The simulation results prove that, proposed V_{TH} extractors show good tracking of the output on threshold voltage variations due to transistor's size, power supply and temperature.

We can summarize this chapter as following:

1. Result of Basic Operation: Simulations run over sample circuits based on "$2V_{GS1}$-V_{GS2}" arithmetic operation.

    - Firstly, V_{TN} and V_{TP} voltages are extracted for different W/L ratios. (Using three different ways: IDPC,ICPD and Flexible)

    - Then supply voltage dependencies of V_{TN} and V_{TP} are examined.

    - Temperature dependency is shown.

2. Result of Generalized Operation: Simulations run over two sample circuit based on "$3V_{GS1}$-$2V_{GS2}$" and "$4V_{GS1}$-$3V_{GS2}$" arithmetic operations using identical dimensions-proportional currents method. Supply voltage, temperature and W/L ratio dependencies of the proposed circuits are examined.

3. Comparing the results: The comparison of different implementation of NMOS V_{TH} extraction based on IDPC method is given.

5.1 Results of Basic Arithmetic Operation

In this section, all simulations were run over sample circuits based on "$2V_{GS1}$-V_{GS2}" arithmetic operation realized with the help of a DDA. During these simulations, drain-source voltages were chosen V_{DS1}=50mV and V_{DS2}=100mV, then applied to the inverting inputs of OPAMPs.

5.1.1 W/L Ratio Dependency of Proposed Extractors based on Basic Arithmetic Operation

First simulations test the accuracy of the proposed extractors depended on transistor ratios. The extracted values are in close agreement with the manually extracted ones.

5.1.1.1 W/L Dependency of V_{TN} Extractor based on "$2V_{GS1}$-V_{GS2}"

V_{TN} extractors circuit implemented in three different ways are simulated to find out the dependency of the output on aspect ratio of transistor under test. In order to extract V_{TN}, proper current sources are chosen to maintain the transistors in strong inversion region.

If we compare the results given in Table 5.1, Table 5.2 and Table 5.3, they indicate the same results that the difference between the two sets of threshold voltages is typically 1% in the case of wider NMOS device.

Table 5.1: IDPC Method Based V_{TN} Extractor Circuit

W/L Ratio of NMOS	Obtained V_{GS1} (V)	Obtained V_{GS2} (V)	Obtained Output of Extractor (mV)	Expected V_{TH} Voltage (mV)	Error (%) $\Delta V_{TH}/V_{TH}$
5u/1u	1.028	1.226	830	840.1	1.2
10u/1u	1.028	1.221	835.5	845.2	1.2
15u/1u	1.029	1.22	837.3	846.9	1.1

Table 5.2: ICPD Method Based V_{TN} Extractor Circuit

W/L Ratio of NMOS	Obtained V_{GS1} (V)	Obtained V_{GS2} (V)	Obtained Output of Extractor (mV)	Expected V_{TH} Voltage (mV)	Error (%) $\Delta V_{TH}/V_{TH}$
5u/1u	1.028	1.226	830	840.1	1.2
10u/1u	1.028	1.221	835.5	845.2	1.2
15u/1u	1.029	1.22	837.3	846.9	1.1

Table 5.3: Flexible Method Based V_{TN} Extractor Circuit

W/L Ratio of NMOS	Obtained V_{GS1} (V)	Obtained V_{GS2} (V)	Obtained Output of Extractor (mV)	Expected V_{TH} Voltage (mV)	Error (%) $\Delta V_{TH}/V_{TH}$
5u/1u	1.028	1.226	830	840.1	1.2
10u/1u	1.028	1.221	835.5	845.2	1.2
15u/1u	1.029	1.22	837.3	846.9	1.1

5.1.1.2 W/L Dependency of V_{TP} Extractor based on "$2V_{GS1}$-V_{GS2}"

During simulations, drain currents are chosen proper to bias PMOS transistors under test, in strong inversion region.

The obtained and expected V_{TH} values for different size of PMOS transistors used in VTP extractors are shown in Table 5.4, Table 5.5 and Table 5.6. They indicate the same results that extracted V_{TP}'s are close agreement with the real ones.

Table 5.4: IDPC Method Based V_{TP} Extractor Circuit

W/L Ratio of NMOS	Obtained V_{GS1} (V)	Obtained V_{GS2} (V)	Obtained Output of Extractor (mV)	Expected V_{TH} Voltage (mV)	Error (%) $\Delta V_{TH}/V_{TH}$
5u/1u	-1.262	-1.461	-1.063	-1.072	0.8
10u/1u	-1.334	-1.615	-1.053	-1.062	0.8
15u/1u	-1.246	-1.442	-1.05	-1.059	0.8

Table 5.5: ICPD Method Based V_{TP} Extractor Circuit

W/L Ratio of NMOS	Obtained V_{GS1} (V)	Obtained V_{GS2} (V)	Obtained Output of Extractor (mV)	Expected V_{TH} Voltage (mV)	Error (%) $\Delta V_{TH}/V_{TH}$
5u/1u	-1.262	-1.461	-1.063	-1.072	0.8
10u/1u	-1.334	-1.615	-1.053	-1.062	0.8
15u/1u	-1.246	-1.442	-1.05	-1.059	0.8

Table 5.6: Flexible Method Based V_{TP} Extractor Circuit

W/L Ratio of NMOS	Obtained V_{GS1} (V)	Obtained V_{GS2} (V)	Obtained Output of Extractor (mV)	Expected V_{TH} Voltage (mV)	Error (%) $\Delta V_{TH}/V_{TH}$
5u/1u	-1.262	-1.461	-1.063	-1.072	0.8
10u/1u	-1.334	-1.615	-1.053	-1.062	0.8
15u/1u	-1.246	-1.442	-1.05	-1.059	0.8

5.1.2 Supply Voltage Dependency of Proposed Extractors based on Basic Arithmetic Operation

Next observed simulations compare the accuracy of the output regarding the nominal threshold given by MOSFET models, sweeping the supply voltage ($V_{DD} = -V_{SS}$), and for new proposed V_{TN} extractors and V_{TP} extractors.

As mentioned before, extractor circuits are designed for the supply voltage between V_{DD} = 2.5V and V_{SS} = -2.5V. A %10 discrepancy from these values is used as

variation. As far as operation under low voltage supply is concerned, the simulations show that over this supply range the extracted V_{TN} and V_{TP} is almost constant with %1 average error.

All simulations are obtained by the use of W/L = 5µm/1µm ratio as unit dimension for both NMOS and PMOS transistors.

5.1.2.1 Supply Voltage Dependency of V_{TN} Extractor based on "$2V_{GS1}$-V_{GS2}"

The dependence of the extracted V_{TH} on supply voltage is expected to be constant. Obtained results for new proposed V_{TN} extractors are shown in Table 5.7,5.8 and 5.9.

V_{TN} Extractor based on IDPC Method

Both NMOS transistors under test have ratio of W/L = 5µm/1µm and current sources are 5µA and 20µA for sample test circuit. Extracted V_{TN} values based on IDPC method with variation of supply voltage are listed in Table 5.7. (See Figure 5.1)

Table 5.7: Extracted V_{TN} with V_{DD} (and V_{SS}) variations at 25 ºC based on IDPC

Supply Voltage (V)	4.5	4.6	4.7	4.8	4.9	5.0
Obtained V_{TN} (mV)	837.1	835.6	834.1	832.7	831.3	830
Error (%)	0.35	0.53	0.71	0.88	1.04	1.2

V_{TN} Extractor based on ICPD Method

NMOS transistors under test have ratio of W/L_1=20µm/1µm and W/L_2 = 5µm/1µm with the use of 20µA current sources. Extracted V_{TN} values based on ICPD method with variation of supply voltage are listed in Table 5.8. (See Figure 5.2).

Table 5.8: Extracted V_{TN} with V_{DD} (and V_{SS}) variations at 25 ºC based on ICPD

Supply Voltage (V)	4.5	4.6	4.7	4.8	4.9	5.0
Obtained V_{TN} (mV)	837.1	835.6	834.1	832.7	831.3	830

Error (%)	0.35	0.53	0.71	0.88	1.04	1.2

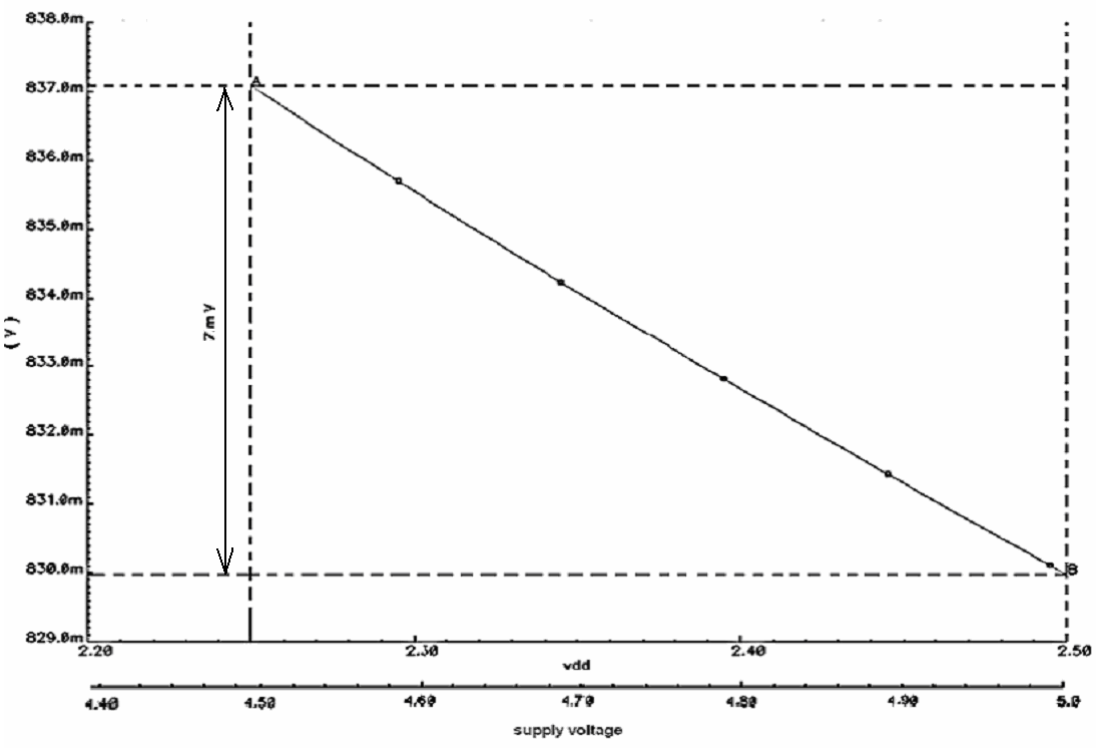


Figure 5.1: The extracted V_{TN} changes with the supply variation based on IDPC.

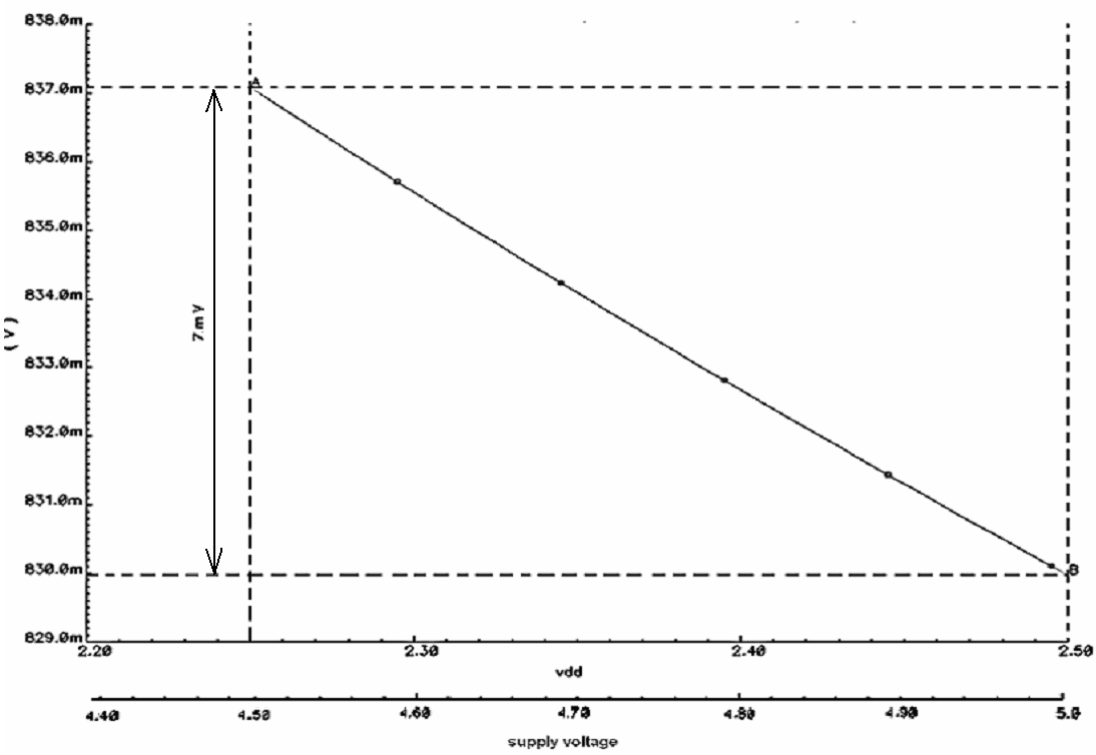


Figure 5.2: The extracted V_{TN} changes with supply variation based on ICPD.

V_{TN} Extractor based on Flexible Method

NMOS transistors under test have ratio of W/L_1=10µm/1µm and W/L_2 = 5µm/1µm with the use of 5µA and 10µA current sources, respectively. Extracted V_{TN} values based on Flexible method with variation of supply voltage are listed in Table 5.9. (See Figure 5.3)

Table 5.9: Extracted V_{TN} with V_{DD} (and V_{SS}) variations at 25 ºC based on Flexible

Supply Voltage (V)	4.5	4.6	4.7	4.8	4.9	5.0
Obtained V_{TN} (mV)	837.1	835.6	834.1	832.7	831.3	830
Error (%)	0.35	0.53	0.71	0.88	1.04	1.2

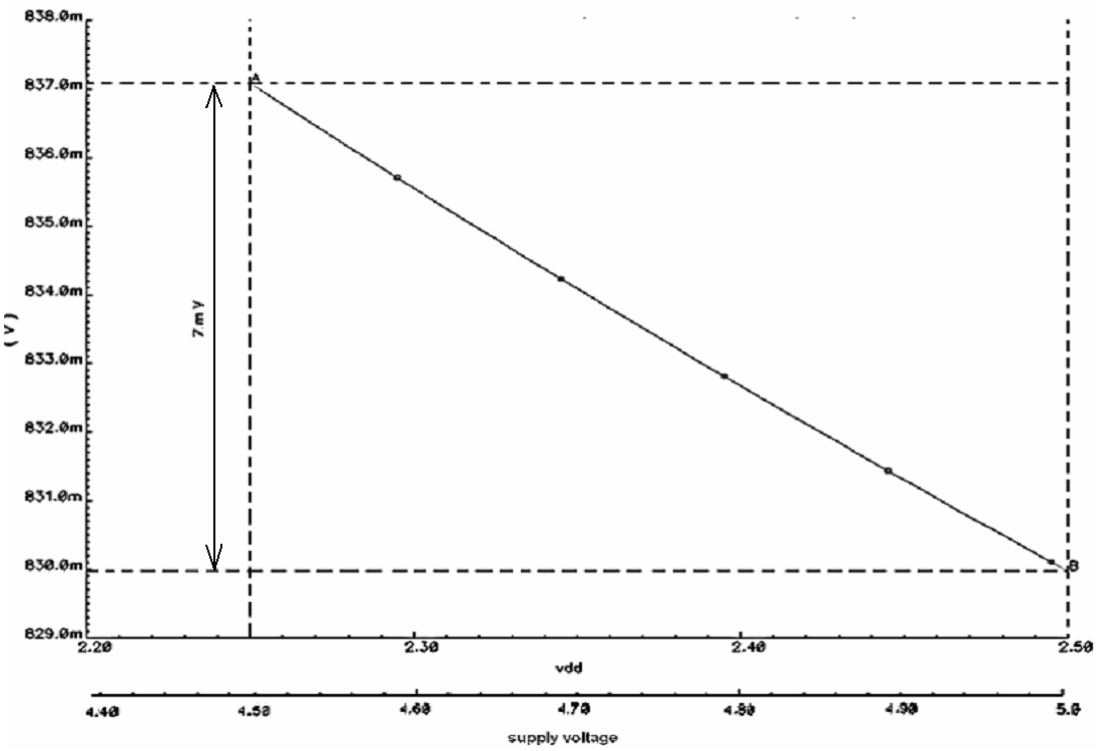


Figure 5.3: The extracted V_{TN} changes with supply variation based on Flexible.

As expected, the extracted V_{TH} remained almost constant with variations in V_{DD} and $V_{SS.}$ (See Figure 5.1, Figure 5.2 and Figure 5.3). Because of second order effects output will have a discrepancy. (For detailed information, please refer to Chapter 4.)

5.1.2.2 Supply Voltage Dependency of V_{TP} Extractor based on "$2V_{GS1}$-V_{GS2}"

The supply voltage variation effects on extracted V_{TH} of proposed PMOS extractors are listed in Table 5.10 , Table 5.11 and Table 5.12

V_{TP} Extractor based on IDPC Method

PMOS transistors under test have ratio of W/L = 5µm/1µm and current sources are chosen1µA and 4µA, respectively. (See Figure 5.4). Extracted V_{TP} values using IDPC method with variation of supply voltage are listed in Table 5.10.

Table 5.10: Extracted V_{TP} with V_{DD} (and V_{SS}) variations at 25 ºC based on IDPC

Supply Voltage (V)	4.5	4.6	4.7	4.8	4.9	5.0
Obtained V_{TP} (V)	-1.059	-1.06	-1.061	-1.061	-1.062	-1.063
Error (%)	1.2	1.11	1.10	1.10	0.93	0.83

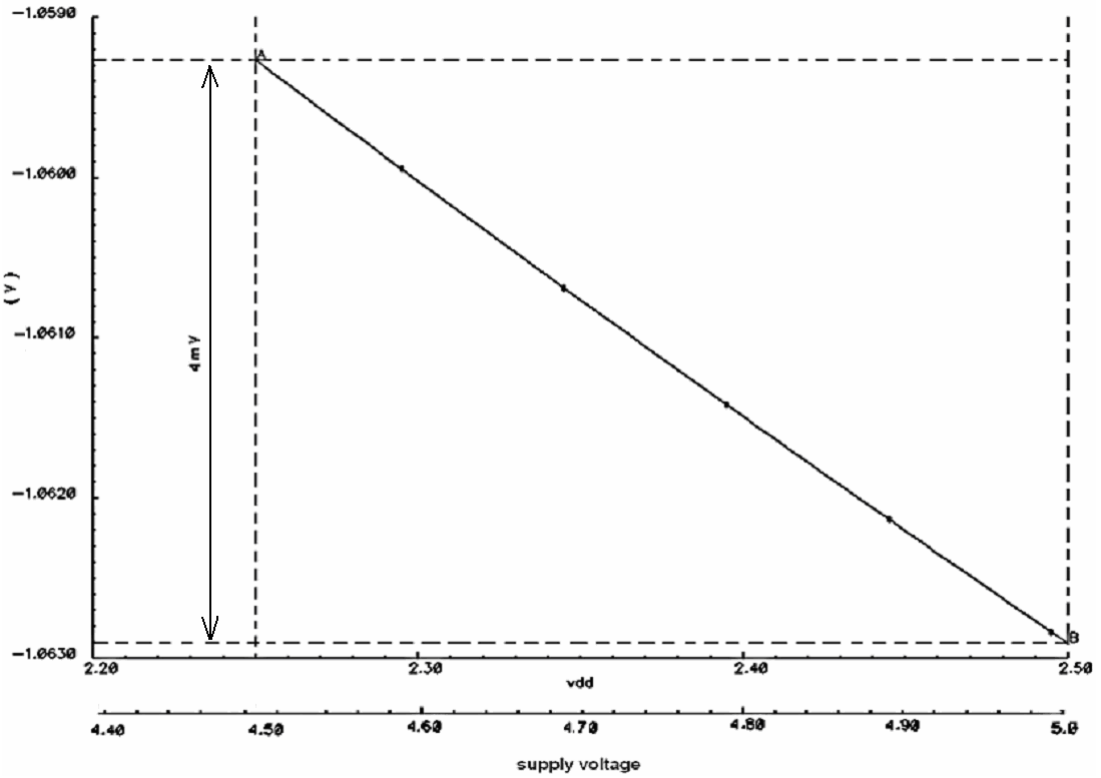


Figure 5.4: The extracted V_{TP} changes with supply variation based on IDPC.

V_{TP} Extractor based on ICPD Method

PMOS transistors under test have ratio of W/L_1 = 20µm/1µm and W/L_2 = 5µm/1µm current sources are 4µA for sample test circuit. (See Figure 5.5). Extracted V_{TP} values using ICPD method with variation of supply voltage are listed in Table 5.11.

Table 5.11: Extracted V_{TP} with V_{DD} (and V_{SS}) variations at 25 ºC based on ICPD

Supply Voltage (V)	4.5	4.6	4.7	4.8	4.9	5.0
Obtained V_{TP} (V)	-1.059	-1.06	-1.061	-1.061	-1.062	-1.063
Error (%)	1.2	1.11	1.10	1.10	0.93	0.83

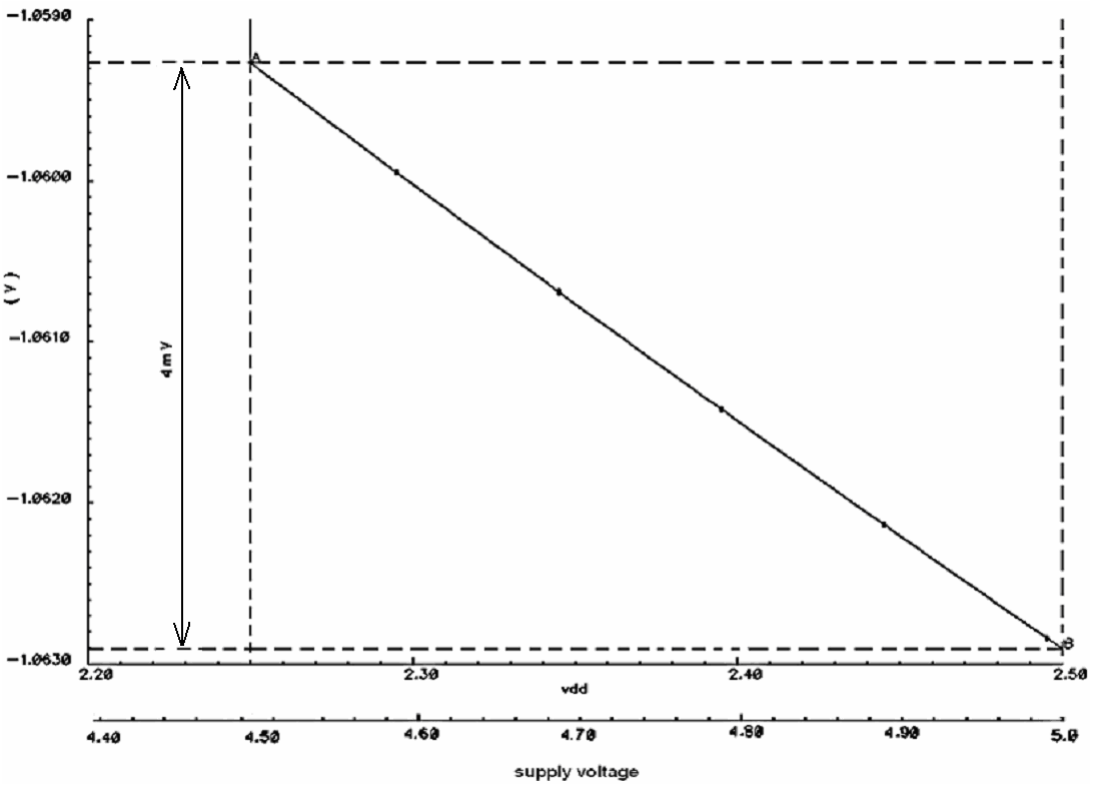


Figure 5.5: The extracted V_{TP} changes with supply variation based on ICPD.

V_{TP} Extractor based on Flexible Method

PMOS transistors under test have ratio of W/L_1 = 10µm/1µm and W/L_2 = 5µm/1µm with current sources I_1= 1µA and I_2=2µA respectively. (See Figure 5.6). Extracted

V_{TP} values using Flexible method with variations of supply voltage are listed in Table 5.12.

Table 5.12: Extracted V_{TP} with V_{DD} (and V_{SS}) variations at 25 ºC based on Flexible

Supply Voltage (V)	4.5	4.6	4.7	4.8	4.9	5.0
Obtained V_{TP} (V)	-1.059	-1.06	-1.061	-1.061	-1.062	-1.063
Error (%)	1.2	1.11	1.10	1.10	0.93	0.83

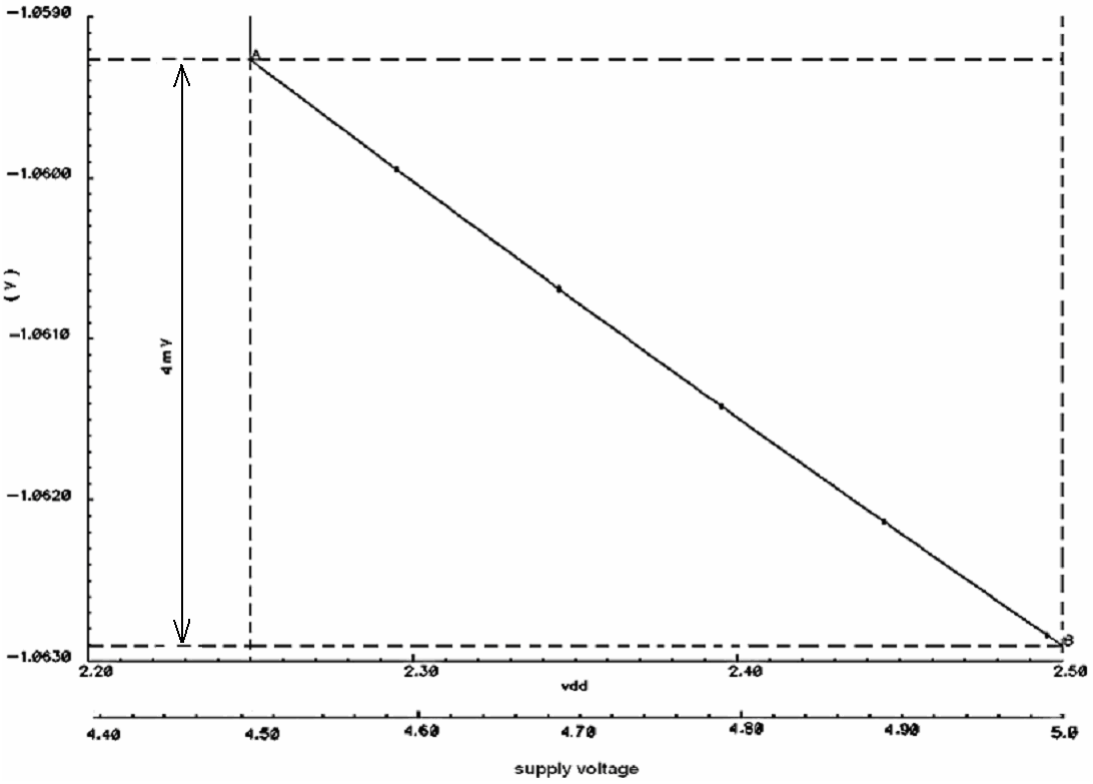


Figure 5.6: The extracted V_{TP} changes with supply variation based on Flexible.

Figure 5.4, Figure 5.5 and Figure 5.6 show that the extracted V_{TP} voltages are almost constant with variations in V_{DD} and V_{SS}. There is only 4mV discrepancy because of second order effects. (Please refer to Chapter 4 for details.)

5.1.3 Temperature Dependency of Proposed Extractors based on Basic Arithmetic Operation

Finally, the linear dependence of the extracted V_{TN} and V_{TP} voltages on temperature is confirmed by sweeping temperature from -20ºC to 80ºC with a fixed supply value.

The proposed V_{TP} and V_{TN} extractor circuits have the capability to generate both PTAT and CTAT voltage references, regularly.

5.1.3.1 Temperature Dependency of V_{TN} Extractor based on "$2V_{GS1}$-V_{GS2}"

V_{TH} extracted from the proposed method has good temperature dependence with about %1 error as compared with the manually experimented values.

The output voltage of the both V_{TN} extractors circuits have constant negative slope with temperature, and they can be used as a CTAT (Complementary to Absolute Temperature) voltage reference. (Please refer to Chapter 6 for detailed information.)

The experimented temperature coefficient of both proposed V_{TN} Extractors is -1.4191 mV/ºC. (Please refer to Figure 5.7, Figure 5.8 and Figure5.9)

V_{TN} Extractor based on IDPC Method

NMOS transistors under test have ratio of W/L = 5µm/1µm and current sources are 5µA and 20µA for sample test circuit. Extracted V_{TN} values based on Flexible method with variation of temperature are listed in Table 5.13.(See Figure 5.7)

Table 5.13: Extracted V_{TN} with Temperature Variation at 5V based on IDPC

Temperature	**0**	**5**	**15**	**25**	**45**	**65**	**85**	**100**
Obtained V_{TN}	868.2	861.1	847	832.8	804.5	776	747.4	725.8
Expected V_{TN}	880.6	873.1	858.1	843.1	813.1	783.1	753.1	730.6
Error (%)	1.40	1.37	1.29	1.22	1.05	0.91	0.75	0.65

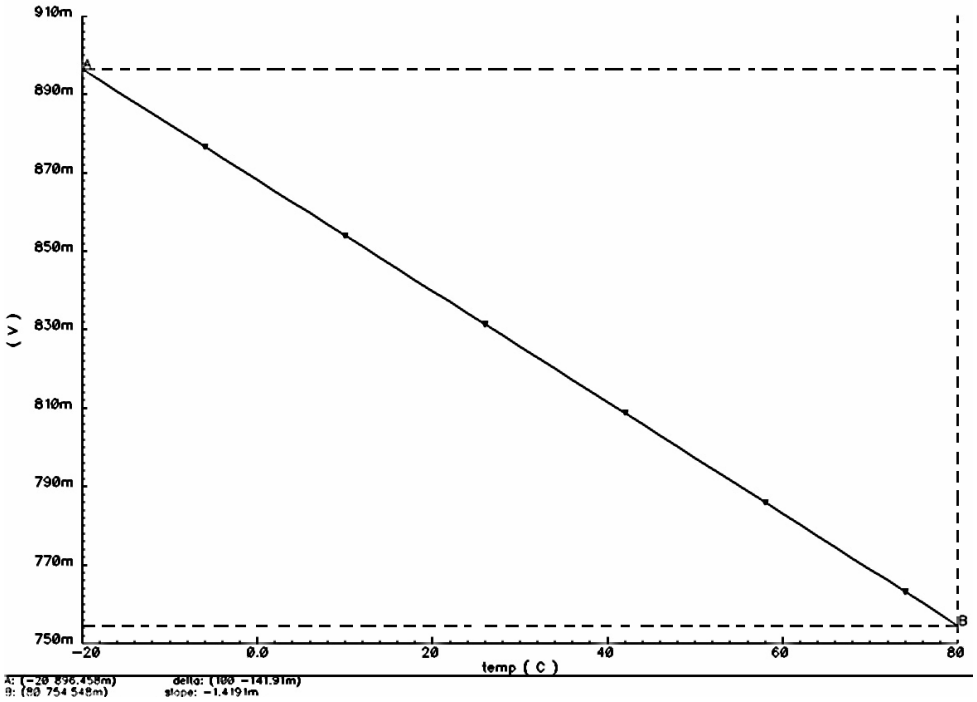


Figure 5.7: Variation of the extracted value of V_{TN} with temperature based on IDPC.

V_{TN} Extractor based on ICPD Method

NMOS transistors under test have ratio of $W/L_1 = 20\mu m/1\mu m$ and $W/L_2 = 5\mu m/1\mu m$ current sources are 20µA for sample test circuit. Extracted V_{TN} values using ICPD method with variation of temperature are listed in Table 5.14.(See Figure 5.8)

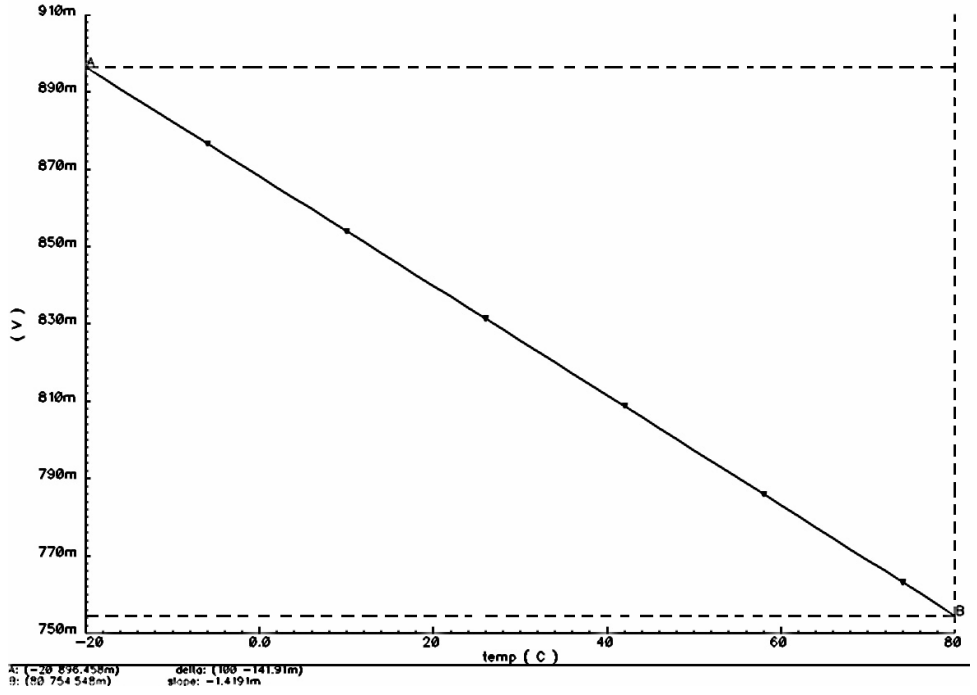


Figure 5.8: Variation of the extracted value of V_{TN} with temperature based on ICPD.

Table 5.14: Extracted V_{TN} with Temperature Variation at 5V based on ICPD

Temperature	**0**	**5**	**15**	**25**	**45**	**65**	**85**	**100**
Obtained V_{TN}	868.2	861.1	847	832.8	804.5	776	747.4	725.8
Expected V_{TN}	880.6	873.1	858.1	843.1	813.1	783.1	753.1	730.6
Error (%)	1.40	1.37	1.29	1.22	1.05	0.91	0.75	0.65

V_{TN} Extractor based on Flexible Method

NMOS transistors under test have ratio of W/L_1 = 10µm/1µm and W/L_2 = 5µm/1µm with current sources 5µA and 10µA for sample test circuit. Extracted V_{TN} values based on Flexible method with variation of temperature are listed in Table 5.15.(See Figure 5.9)

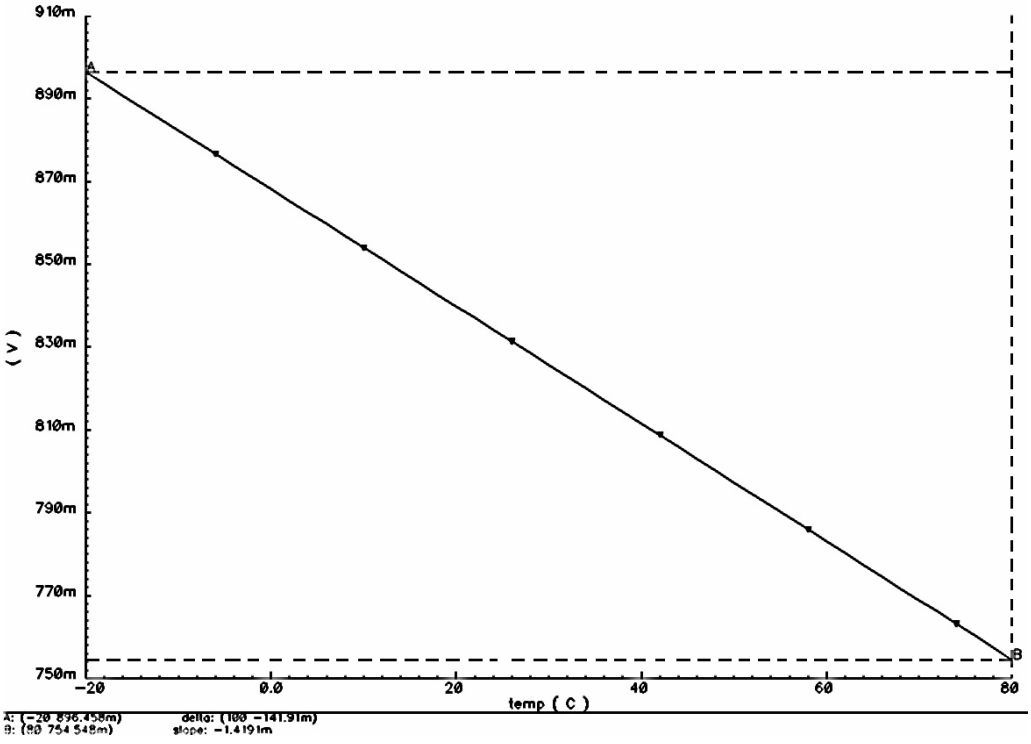


Figure 5.9: Variation of the extracted value of V_{TN} with temperature based on Flexible.

Table 5.15: Extracted V_{TN} with Temperature Variation at 5V based on Flexible

Temperature	**0**	**5**	**15**	**25**	**45**	**65**	**85**	**100**
Obtained V_{TN}	868.2	861.1	847	832.8	804.5	776	747.4	725.8
Expected V_{TN}	880.6	873.1	858.1	843.1	813.1	783.1	753.1	730.6
Error (%)	1.40	1.37	1.29	1.22	1.05	0.91	0.75	0.65

5.1.3.2 Temperature Dependency of V_{TP} Extractor based on "$2V_{GS1}$-V_{GS2}"

The output voltage of the proposed V_{TP} circuits have an almost constant positive slope with temperature, thus it can be used as a PTAT (Proportional to Absolute Temperature) voltage reference which is detailed in Chapter 6.

Simulations confirmed the PTAT behavior of V_{TP} extractors, and both extracted V_{TP} has an approximate positive slope of 1.992mV/° C with temperature. (See Figure 5.10, Figure 5.11 and Figure 5.12)

V_{TP} Extractor based on IDPC Method

PMOS transistors under test have ratio of W/L = 5µm/1µm and current sources are 1µA and 4µA for sample test circuit. Extracted V_{TP} values based on IDPC method with variation of temperature are listed in Table 5.16.(See Figure 5.10)

Table 5.16: Extracted V_{TP} with Temperature Variation at 5V based on IDPC

Temperature	**0**	**5**	**15**	**25**	**45**	**65**	**85**	**100**
Obtained V_{TP}	-1.117	-1.107	-1.087	-1.067	-1.027	-987.7	-948.4	-919
Expected V_{TP}	-1.126	-1.116	-1.096	-1.076	-1.036	-996.2	-956.2	-926.2
Error (%)	0.79	0.80	0.82	0.83	0.86	0.85	0.815	0.77

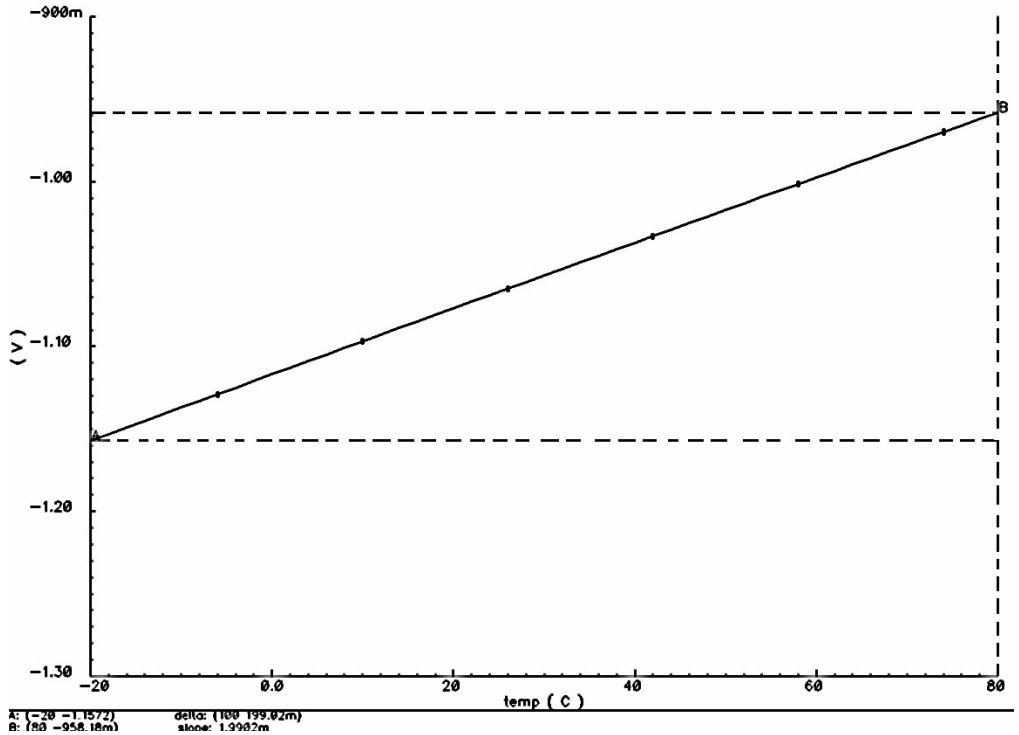


Figure 5.10: Variation of the extracted value of V_{TP} with temperature based on IDPC.

V_{TP} Extractor based on ICPD Method

NMOS transistors under test have ratio of $W/L_1 = 5\mu m/1\mu m$ and $W/L_2 = 20\mu m/1\mu m$ current sources are 4µA for sample test circuit. Extracted V_{TP} values based on ICPD method with variation of temperature are listed in Table 5.17.(See Figure 5.11)

Table 5.17: Extracted V_{TP} with Temperature Variation at 5V based on ICPD

Temperature	**0**	**5**	**15**	**25**	**45**	**65**	**85**	**100**
Obtained V_{TP}	-1.117	-1.107	-1.087	-1.067	-1.027	-987.7	-948.4	-919
Expected V_{TP}	-1.126	-1.116	-1.096	-1.076	-1.036	-996.2	-956.2	-926.2
Error (%)	0.79	0.80	0.82	0.83	0.86	0.85	0.815	0.77

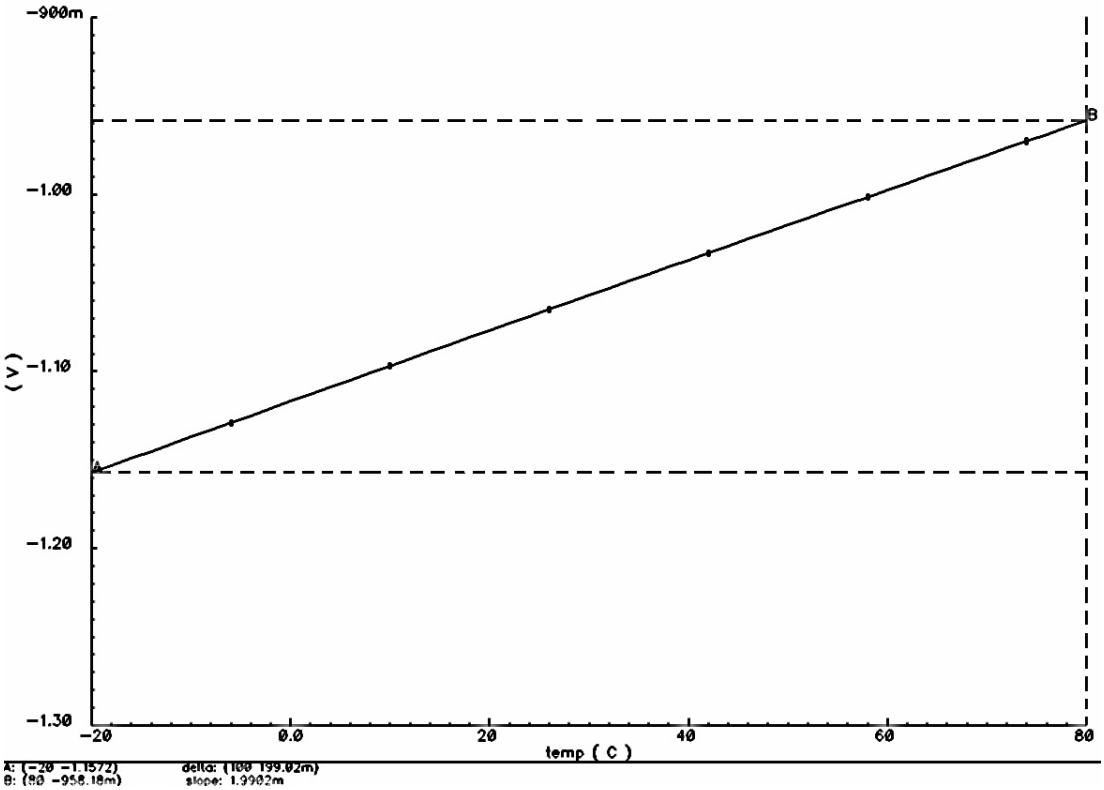


Figure 5.11: Variation of the extracted value of V_{TP} with temperature based on ICPD.

V_{TP} Extractor based on Flexible Method

PMOS transistors under test have ratio of W/L_1 = 10µm/1µm and W/L_2 = 5µm/1µm current sources are 1µA and 4µA for sample test circuit. Extracted V_{TP} values based on IDPC method with variation of temperature are listed in Table 5.18.(See Figure 5.12)

Table 5.18: Extracted V_{TP} with Temperature Variation at 5V based on Flexible

Temperature	**0**	**5**	**15**	**25**	**45**	**65**	**85**	**100**
Obtained V_{TP}	-1.117	-1.107	-1.087	-1.067	-1.027	-987.7	-948.4	-919
Expected V_{TP}	-1.126	-1.116	-1.096	-1.076	-1.036	-996.2	-956.2	-926.2
Error (%)	0.79	0.80	0.82	0.83	0.86	0.85	0.815	0.77

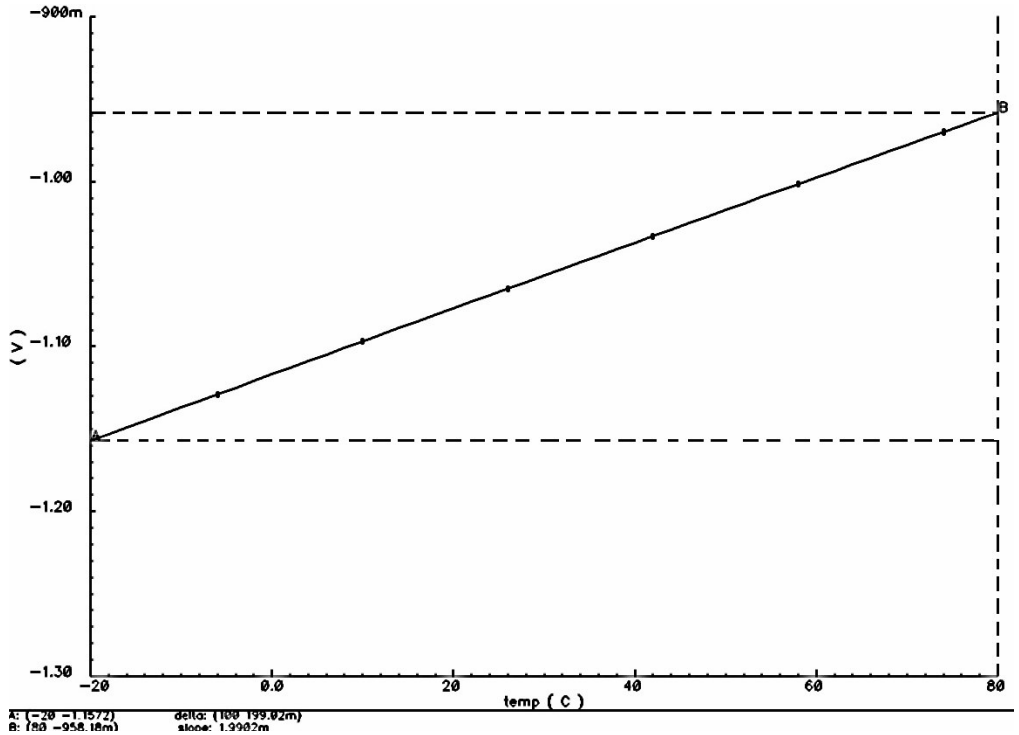


Figure 5.12: Variation of the extracted value of V_{TP} with temperature based on Flexible.

5.2 Results of Generalized Arithmetic Operation

In this section, simulation results for new extractor circuits, designed with the help of generalized arithmetic operation, are overviewed.

The sample extractors are based on "$3V_{GS1}$-$2V_{GS2}$" and "$4V_{GS1}$-$3V_{GS2}$" arithmetic operation realized with the help of cascaded DDAs detailed in Chapter 3. Both extractor circuits use identical dimensions-proportional current method.

Drain source voltages are used to bias test transistors under strong-inversion,

- In order to realize operation "$3V_{GS1}$-$2V_{GS2}$", drain-source voltages are applied V_{DS1}=50mV and V_{DS2}=75mV, respectively.
- For realizing "$4V_{GS1}$-$3V_{GS2}$" operation, drain-source voltages are chosen V_{DS1}=60mV and V_{DS2}=80mV, respectively.

Both sample circuit examined for W/L ratio, temperature and supply voltage dependencies.

NMOS threshold voltage extraction based on generalized operation has been given but it is also applicable to PMOS device with appropriate modifications.

5.2.1 W/L Dependency of Proposed V_{TN} Extractors Based on Generalized Operation

New V_{TN} extractors are simulated for different size of transistors. In order to extract V_{TN}, proper current sources are chosen to maintain the transistors in strong inversion region.

Extracted V_{TN} values based on IDPC method with variation of aspect ratio are listed in Table 5.19 and Table 5.20.

5.2.1.1 V_{TN} Extractor based on "$3V_{GS1}$-$2V_{GS2}$"

Table 5.19: Extracted V_{TN} with the use of "$3V_{GS1}$-$2V_{GS2}$" arithmetic operation.

W/L Ratio of NMOS	Obtained V_{GS1} (V)	Obtained V_{GS2} (V)	Obtained Output of Extractor (mV)	Expected V_{TH} Voltage (mV)	Error (%) $\Delta V_{TH}/V_{TH}$
5u/1u	0.995	1.077	831	840.1	1.08
10u/1u	0.997	1.078	835.7	845.2	1.12
15u/1u	0.9972	1.0768	837.3	846.9	1.13

5.2.1.2 V_{TN} Extractor based on "$4V_{GS1}$-$3V_{GS2}$"

Table 5.20: Extracted V_{TN} with the use of "$4V_{GS1}$-$3V_{GS2}$" arithmetic operation.

W/L Ratio of NMOS	Obtained V_{GS1} (V)	Obtained V_{GS2} (V)	Obtained Output of Extractor (mV)	Expected V_{TH} Voltage (mV)	Error (%) $\Delta V_{TH}/V_{TH}$
5u/1u	1.114	1.209	828.1	840.1	1.42
10u/1u	1.112	1.205	834.3	845.2	1.28
15u/1u	0.9972	1.0768	836.4	846.9	1.23

5.2.2 Supply Voltage Dependency of Proposed V_{TN} Extractors Based on Generalized Operation

Extractor circuits are designed for the supply voltage between V_{DD}=2.5V and V_{SS}=2.5V.A %10 discrepancy from these values is used as variation.

5.2.2.1 V_{TN} Extractor based on "$3V_{GS1}$-$2V_{GS2}$"

Dimensions of device under test are 5µm/1µm and proportional currents are chosen 4µA and 9µA respectively. Extracted V_{TN} values based on IDPC method with variation of supply voltage are listed in Table 5.21.

Table 5.21: Extracted V_{TN} with V_{DD} (and V_{SS}) variations at 25 ˚C with the use of "$3V_{GS1}$-$2V_{GS2}$" arithmetic operation

Supply Voltage (V)	4.5	4.6	4.7	4.8	4.9	5.0
Obtained V_{TN} (V)	847.4	843.9	840.5	837.3	834.1	831
Error (%)	0.86	0.45	0.04	0.33	0.71	1.08

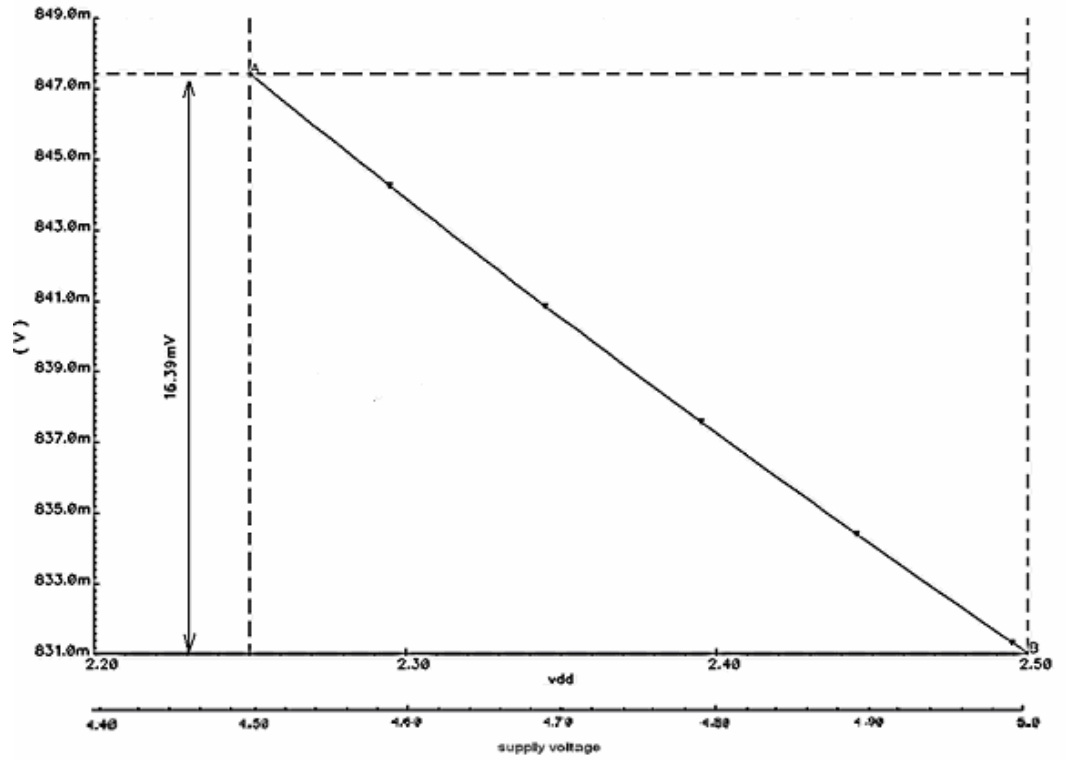


Figure 5.13: The extracted V_{TN} changes with supply variation with the use of "$3V_{GS1}$-$2V_{GS2}$" arithmetic operation.

5.2.2.2 V_{TN} Extractor based on "$4V_{GS1}$-$3V_{GS2}$"

Proportional currents are chosen 9µA and 16µA respectively and dimensions of the device under test is 5µm/1µm. Extracted V_{TN} values based on IDPC method with variation of supply voltage are listed in Table 5.22.

Table 5.22: Extracted V_{TN} with V_{DD} (and V_{SS}) variations at 25 ˚C with the use of "$4V_{GS1}$-$3V_{GS2}$" arithmetic operation

Supply Voltage (V)	4.5	4.6	4.7	4.8	4.9	5.0
Obtained V_{TN} (V)	849.8	845.1	840.6	836.3	832.1	828.1
Error (%)	1.15	0.59	0.059	0.45	0.95	1.4

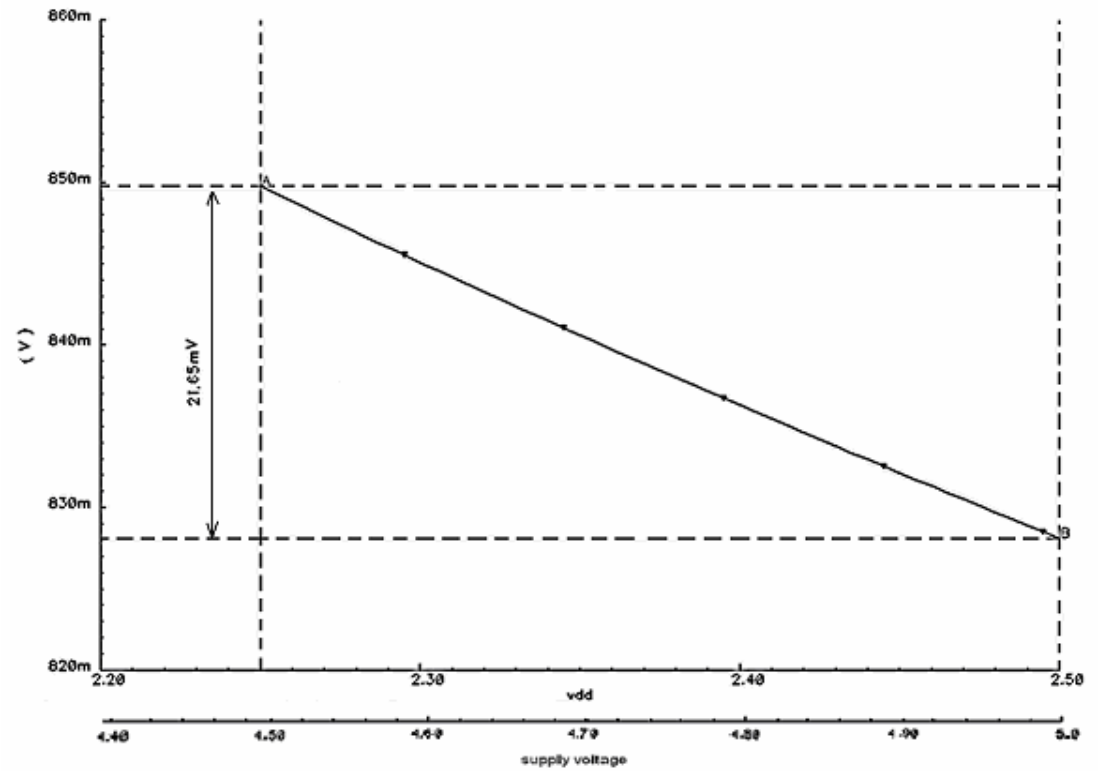


Figure 5.14: The extracted V_{TN} changes with supply variation with the use of "$4V_{GS1}$-$3V_{GS2}$" arithmetic operation.

5.2.3 Temperature Dependency of Proposed V_{TN} Extractors Based on Generalized Operation

The output voltage of the proposed V_{TN} circuits based on generalized operation have almost constant negative slope with temperature

5.2.3.1 V_{TN} Extractor based on "$3V_{GS1}$-$2V_{GS2}$"

Dimensions of device under test are 5µm/1µm and proportional currents are chosen 4µA and 9µA respectively. Extracted V_{TN} values based on IDPC method with variation of temperature are listed in Table 5.23.

Table 5.23: Extracted V_{TN} with Temperature Variation at 5V with the use of "$3V_{GS1}$-$2V_{GS2}$" arithmetic operation

Temperature	**0**	**5**	**15**	**25**	**45**	**65**	**85**	**100**
Obtained V_{TN}	867.5	860.8	847.2	833.7	806.8	780	753.2	733.1
Expected V_{TN}	880.6	873.1	858.1	843.1	813.1	783.1	753.1	730.6
Error (%)	1.48	1.40	1.27	1.11	0.77	0.39	0.01	0.34

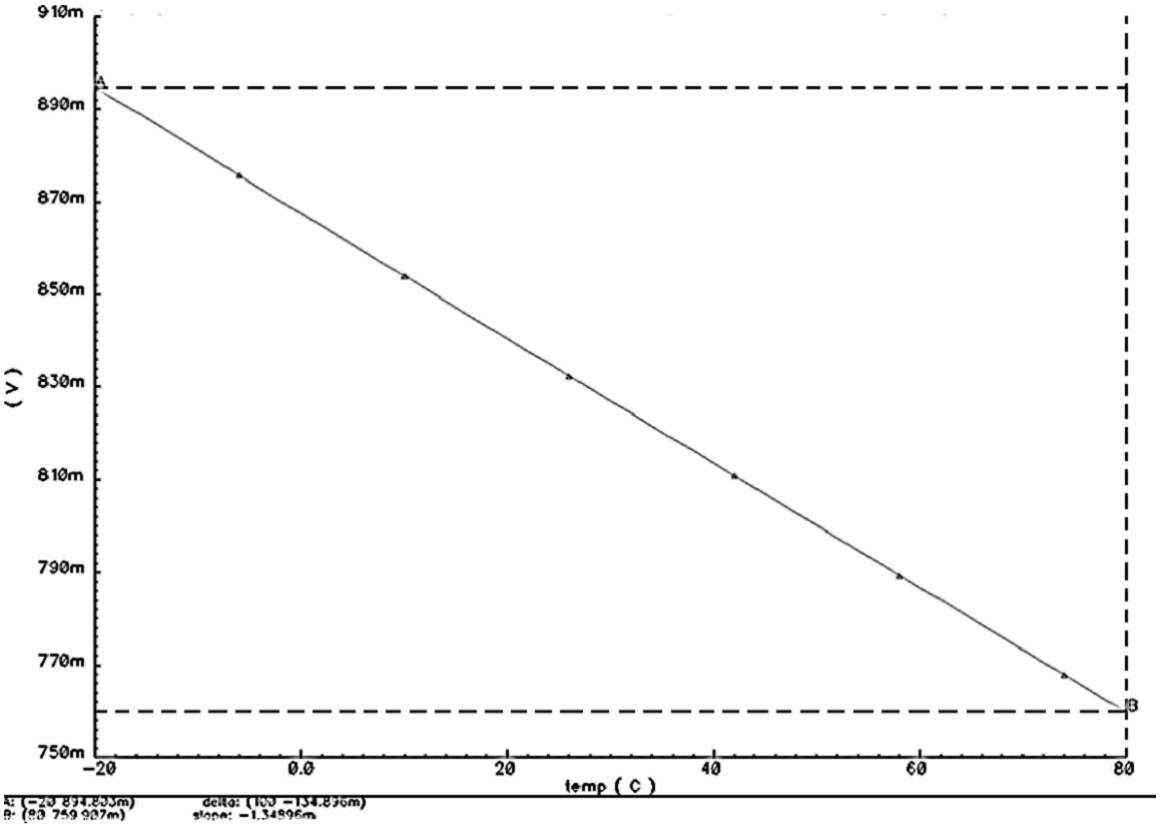


Figure 5.15: Variation of the extracted value of V_{TN} with temperature at 5V with the use of "$3V_{GS1}$-$2V_{GS2}$" arithmetic operation.

5.2.3.2 V_{TN} Extractor based on "$4V_{GS1}$-$3V_{GS2}$"

Proportional currents are chosen 9µA and 16µA respectively and dimensions of the device under test is 5µm/1µm. Drain source voltages in order to bias test transistors under strong-inversion are chosen V_{DS1}=60mV and V_{DS2}=80mV. Extracted V_{TN} values based on IDPC method with variation of temperature are listed in Table 5.24.

Table 5.24: Extracted V_{TN} with Temperature Variation at 5V with the use of "$4V_{GS1}$-$3V_{GS2}$" arithmetic operation

Temperature	**0**	**5**	**15**	**25**	**45**	**65**	**85**	**100**
Obtained V_{TN}	868.5	861.1	846.1	831.1	800.9	770.2	739.2	715.7
Expected V_{TN}	880.6	873.1	858.1	843.1	813.1	783.1	753.1	730.6
Error (%)	1.37	1.37	1.39	1.42	1.5	1.64	1.84	2.03

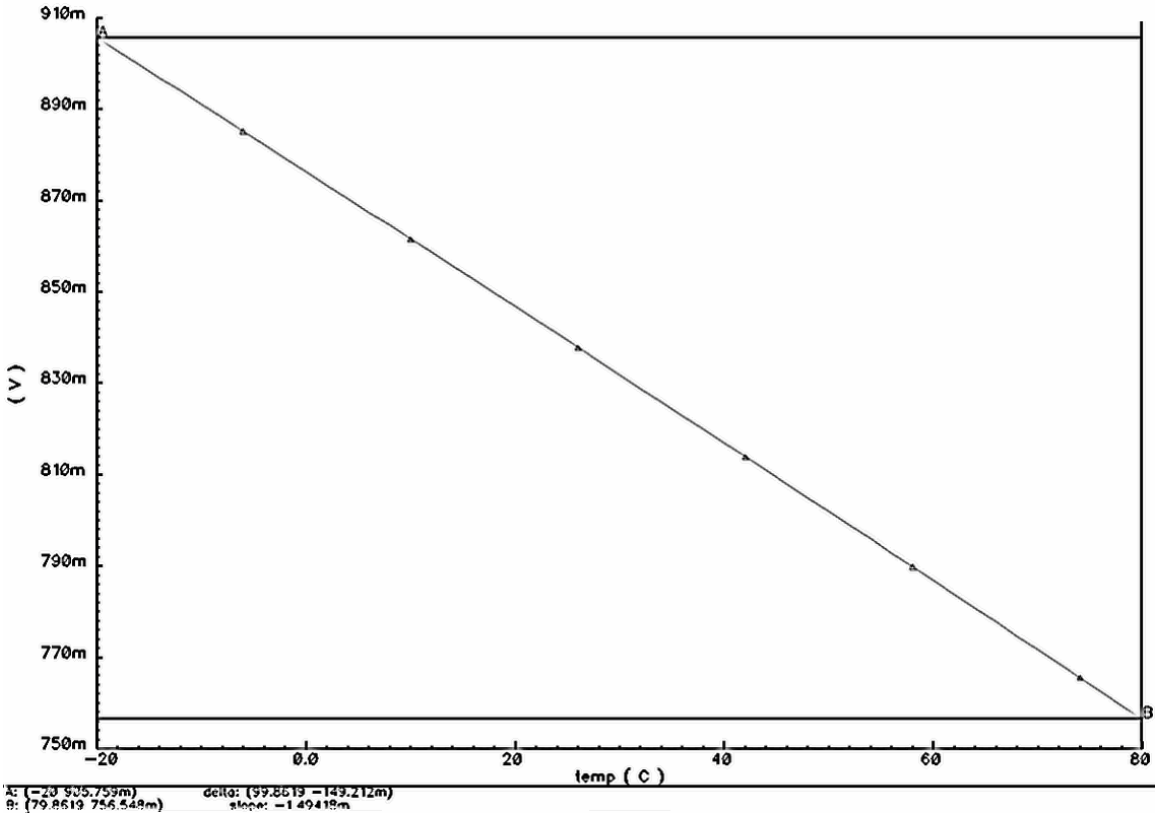


Figure 5.16: Variation of the extracted value of V_{TN} with temperature at 5V with the use of "$4V_{GS1}$-$3V_{GS2}$" arithmetic operation

5.3 Comparison of the Results

Simulations, given above, have run over sample circuits based on the following arithmetic operations "$2V_{GS1}$-V_{GS2}", "$3V_{GS1}$-$2V_{GS2}$" and "$4V_{GS1}$-$3V_{GS2}$". Both NMOS and PMOS extractor circuits are designed depending on the basic operation ("$2V_{GS1}$-V_{GS2}") and two different implementations of them, based on IDPC and ICPD methods are examined. The results for both implementations are exactly the same. For generalized operation, two separate NMOS extractors realizing different arithmetic operation based on IDPC method are designed and simulated.

The comprasion of different implementation of NMOS V_{TH} extraction based on IDPC method is given in Table 5.25.

Table 5.25: Extracted V_{TN} over different implementations

V_{TH} extracted for NMOS	**Basic Operation**	**Generalized Operation**	
	"$2V_{GS1}$-V_{GS2}"	**"$3V_{GS1}$-$2V_{GS2}$**	**"$4V_{GS1}$-$3V_{GS2}$"**
W/L = 5µm/1µm	830	831	828.1
W/L = 10µm/1µm	835.5	835.7	834.3
W/L = 15µm/1µm	837.3	837.3	836.4

Table 5.25 indicates that, the difference between the three sets of threshold voltages is typically 0.1%, maximum 0.9% in the case of different operation.

Table 5.26 show three sets of threshold voltages extracted in different tempertures, they differ typically 0.4%, maximum 1.3% in the case of different operation.

Table 5.27 gives three sets of threshold voltages extracted with different power supply, basic operation based extractor circuti has minimum change with power supply.

All results given until now, show that V_{TH} extractor circuit based on basic aritmetic operation has more accurate results with comprasion of generalized ones, because of second order effects.

Table 5.26: V_{TN} variation with temperature over different implementations

Temperature (Centigrade)	**Extracted V_{TH} values for NMOS**		
	Basic Operation	**Generalized Operation**	
	"$2V_{GS1}$-V_{GS2}"	**"$3V_{GS1}$-$2V_{GS2}$**	**"$4V_{GS1}$-$3V_{GS2}$"**
0	868.2	867.5	868.5
25	832.8	833.7	831.1
45	804.5	806.8	800.9
85	747.4	753.2	739.2

Table 5.27: V_{TN} variation with power supply over different implementations

Power Supply (Volt)	**Extracted V_{TH} values for NMOS**		
	Basic Operation	**Generalized Operation**	
	"$2V_{GS1}$-V_{GS2}"	**"$3V_{GS1}$-$2V_{GS2}$**	**"$4V_{GS1}$-$3V_{GS2}$"**
4.5	837.1	847.4	849.8
4.7	834.1	840.5	840.6
5	830	831	828.1

6. APPLICATIONS USING NEW V_{TH} EXTRACTORS

The V_{TH} extractors, presented in Chapter IV, have wide applications among analog integrated circuits. Some examples of them will be presented in this section such as MOS transistor characterization, temperature measurement, voltage reference and square-root circuit.

6.1 Automatic MOS Characterization

This is an important topic both for analog circuit designers and wafer manufacturers. The most important parameter of an MOS transistor is V_{TH}. Circuit designer needs do hand calculations after simulations in order to know V_{TH}, additionally a wafer manufacturer finds out V_{TH} by monitoring the process variations on the wafer. So far, parameter V_{TH} is extracted using either the graphical method or numerical method. The drawbacks associated with these methods are substantial measurement time and complicated calculations. Comparing existing results, automatic MOS characterization is more efficient because the V_{TH} value of an MOS transistor is obtained directly from the output of the V_{TH} extractor.

6.1.1 Automatic Extraction of V_{TH}

V_{TH} can be directly, quickly and precisely measured using either implemented ICPD, IDPC or Flexible extractor circuits, described in Chapter 3. Please refer to Chapter 5 to see results which prove that V_{TH} of the PMOS and NMOS devices can be obtained directly from the output of the extractors.

6.2 Temperature Measurements

Thermal sensors are being integrated along with other IC sensors for on the spot temperature measurement. Electronic temperature sensing is a mature art, yet each new technology brings new possibility for innovation.

Two new temperature sensors, PTAT and CTAT, are designed with the use of V_{TH} extractors. This usage is very attractive because temperature coefficient α_T is linearly proportional to absolute temperature.

The most attractive advantages of this type of temperature sensors are:

1. Low-cost IC fabrication and integration because the sensors can be fully integrated with other circuitries on a silicon chip using the popular CMOS technology.

2. Easy implementation because the sensors, like other monolithic counterparts, are very simple and do not require the costly linearization and amplification circuitry common to other sensors, such as thermocouples.

6.2.1 PTAT Sensor

The classic PTAT sensor is based on a linear dependence of V_{BE} voltage from a temperature. In the new solution bipolar transistors are replaced by MOS transistors.

The Figure 6.1 shows the PTAT sensor temperature characteristic. For a PTAT sensor, the most important parameter is the proportionality constant ψ, which is determined by the fabrication process. This constant represents the temperature coefficient or sensitivity of the sensor.

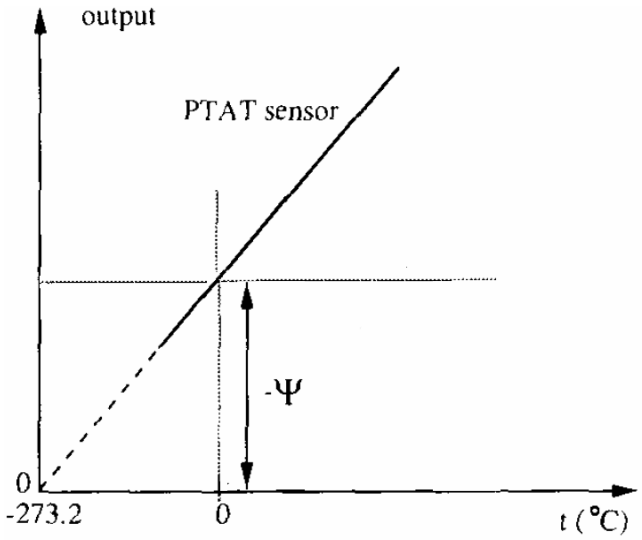


Figure 6.1: PTAT sensor characteristic.

For proposed V_{TP} extractor, temperature dependency can be written as:

$$V_O(T) = V_O(To) - \alpha(T - To) \quad \textbf{(6.1)}$$

We see that the output voltage increases linearly with absolute temperature. This means the V_{TP} extractor is potential PTAT sensor itself. (See Figure6.2)

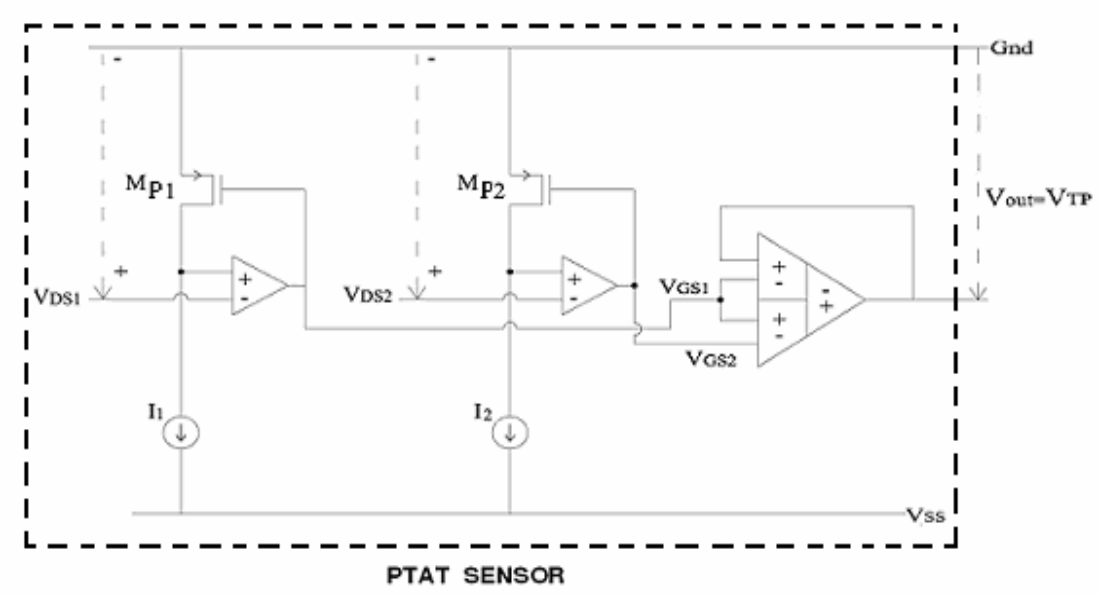


Figure 6.2: Realization of PTAT sensor.

Presented PTAT sensor temperature sensitivity can be expressed by the means of temperature coefficient of V_{TP} extractor.

$$\psi = \alpha \quad \textbf{(6.2)}$$

Simulation results confirmed behavior of V_{TP} extractors has an approximate positive slope of 1.99mV/°C with temperature. (See Figure 6.3)

6.2.2 CTAT Sensor

CTAT sensors have characteristic complementary proportional to temperature. (See Figure 6.4)

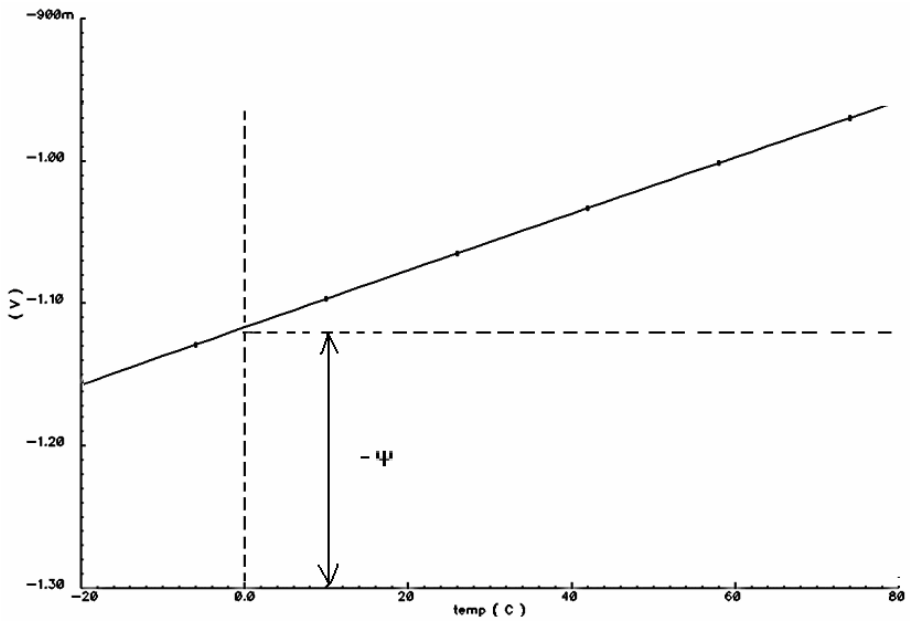


Figure 6.3: Proposed PTAT sensor temperature characteristic.

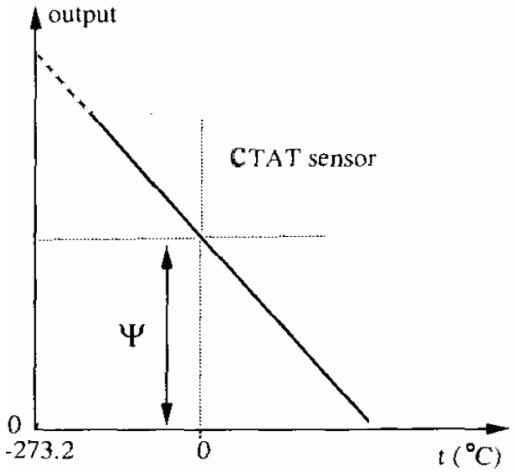


Figure 6.4: CTAT sensor characteristic.

Presented V_{TN} extractor have almost constant negative slope with temperature, so they can be formed as a CTAT (Complementary to Absolute Temperature) voltage reference without any addition.

The realization of the CTAT sensor is shown in Figure 6.5. Measurement results show that, CTAT sensor has an approximate negative slope of -1.42mV/° C with temperature. (See Figure 6.6)

$$\psi = -\alpha \qquad \textbf{(6.3)}$$

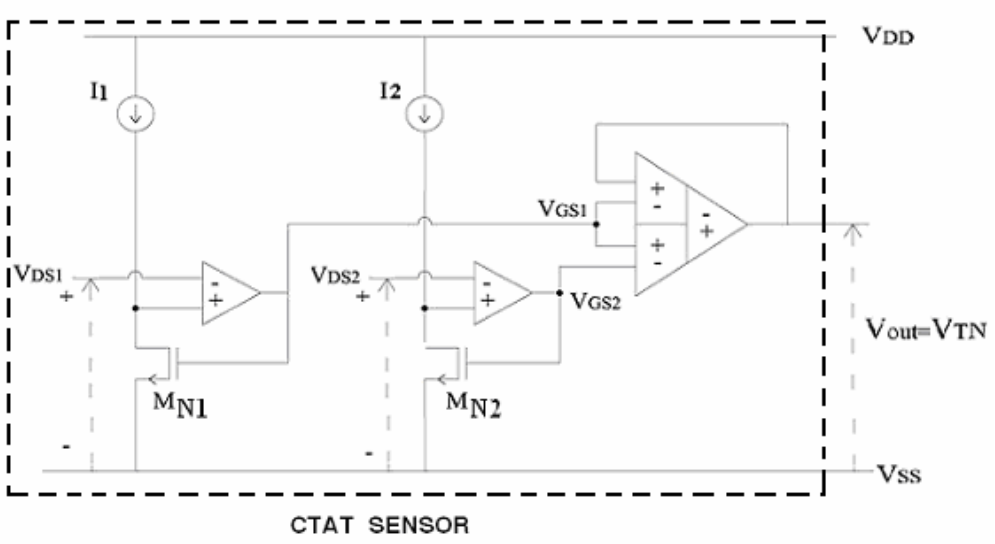


Figure 6.5: Realization of CTAT sensor.

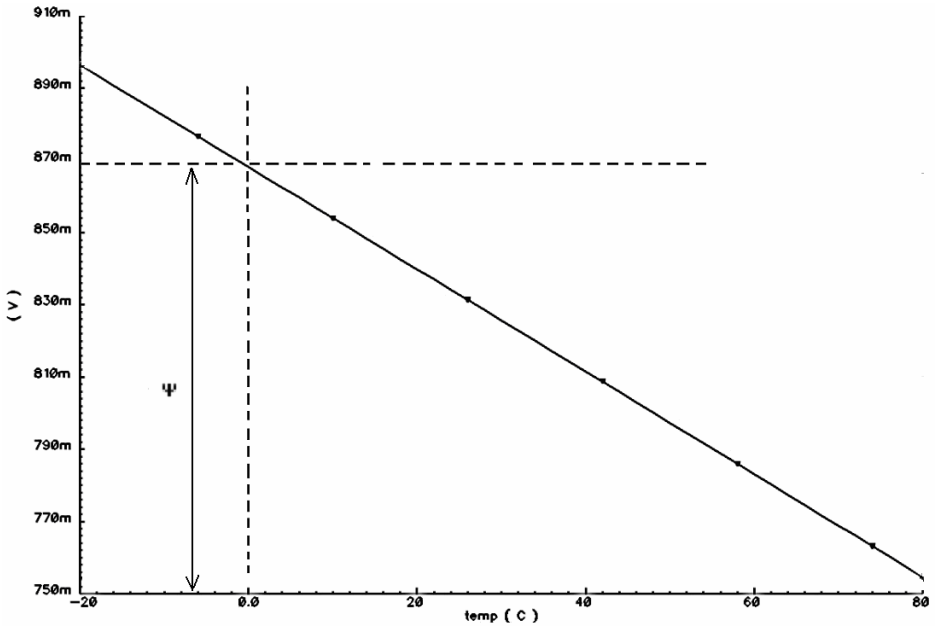


Figure 6.6: Proposed CTAT sensor temperature characteristic.

6.3 Voltage Reference Circuit

An ideal voltage reference should provide a constant output voltage that is independent of temperature, power supply voltage, fabrication process and other operating conditions.

As the industry trend toward less expensive, basic CMOS processes continues, IC designers are challenged with designing circuits that perform equally as well as their

bipolar predecessors. Many variations of bandgap references utilize the temperature dependence of the base-emitter junction voltage (V_{BE}) of bipolar transistors. The Brokaw bandgap cell, for example, is a widely used bipolar reference. The goal of the voltage reference, described here, is to achieve performance comparable to bandgap reference using a circuit that is fabricated in CMOS technology.

Voltage references can be found in a wide range of applications, including linear and switching regulators, A/D and D/A converters, voltage-to-frequency converters, power supply supervisory circuits and other circuits requiring a precision reference voltage.

The proposed Voltage reference circuit depends on the sum of the temperature dependent voltages references. Two linear voltages, one associated with PMOS threshold voltage and the other associated with NMOS threshold voltage, are combined to generate a reference voltage that is stable with temperature.

The two currents are scaled so that the linear components of the two temperature coefficients are equal in magnitude, but opposite in sign. The currents are then summed with the help of an operational amplifier based analog adder to form the voltage reference.

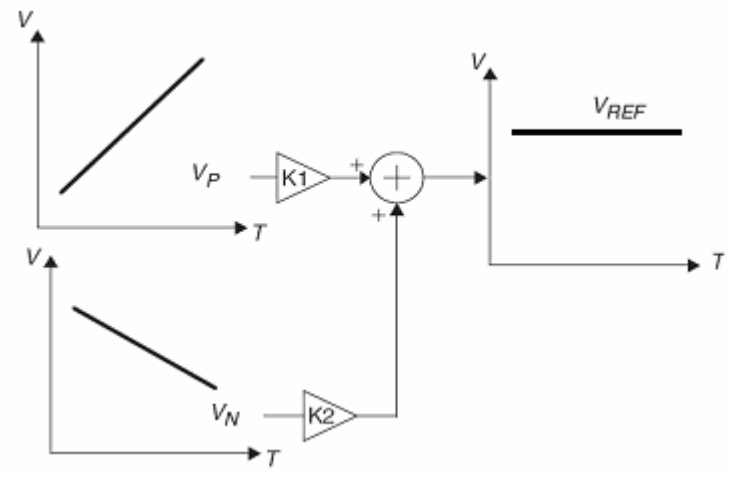


Figure 6.7: Voltage reference concept.

The proposed voltage reference is based upon two voltages, V_{TP} and V_{TN} that are proportional to PMOS device threshold voltage and NMOS device threshold voltage, respectively. By combining V_{TP} and V_{TN}, the temperature coefficients are cancelled

and the resulting voltage can be adjusted to the desired output reference voltage. The concept is illustrated in Figure 6.7.

Figure 6.8 shows the proposed voltage reference schematic. Block I generates V_{TN} using NMOS transistors M_{N1} and M_{N2} (Please refer to Figure 3.8). In block II, V_{TP} is generated using PMOS transistors M_{P1} and M_{P2}. (Please refer to Figure 3.12) The two voltages are then combined by an adder to generate a zero-TC reference voltage in block III. Owing to the OPAMPs, V_{TP} and V_{TN} are both supply independent.

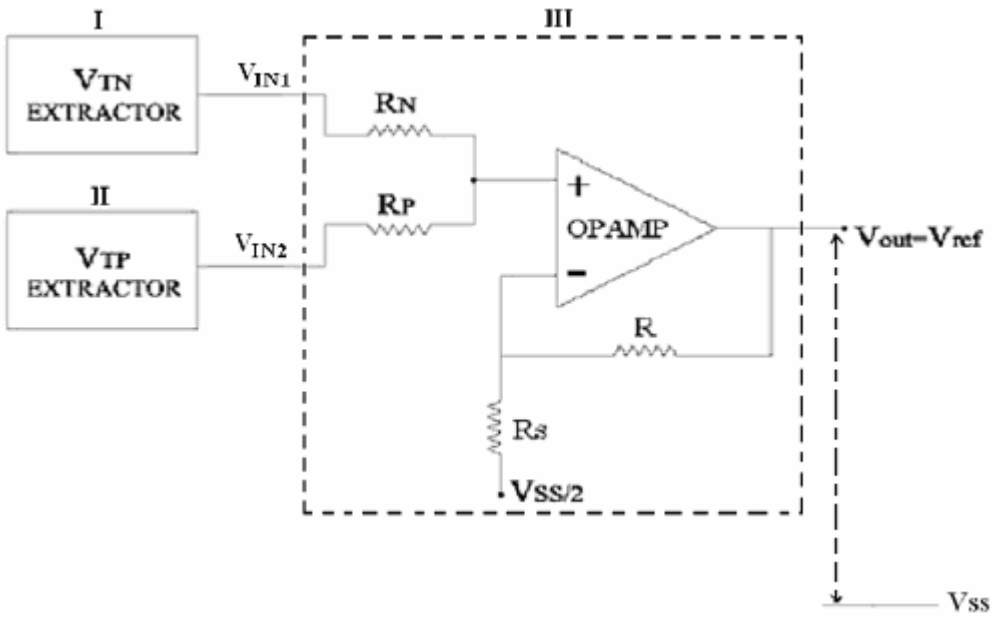


Figure 6.8: Voltage reference schematic.

PTAT and CTAT voltages have temperature coefficients of -1.42 mV/˚C and 1.99mV/˚C, respectively. (See Figure 6.3 , Figure 6.6 and Figure 6.9)

V_{TP} has positive, V_{TN} has negative temperature sensitivity but they are different in value. Hence, they can be added with different weighting values to form a near zero-temperature coefficient output voltage. An OPAMP is used to form an adder circuit as shown in block III of Figure 6.8.

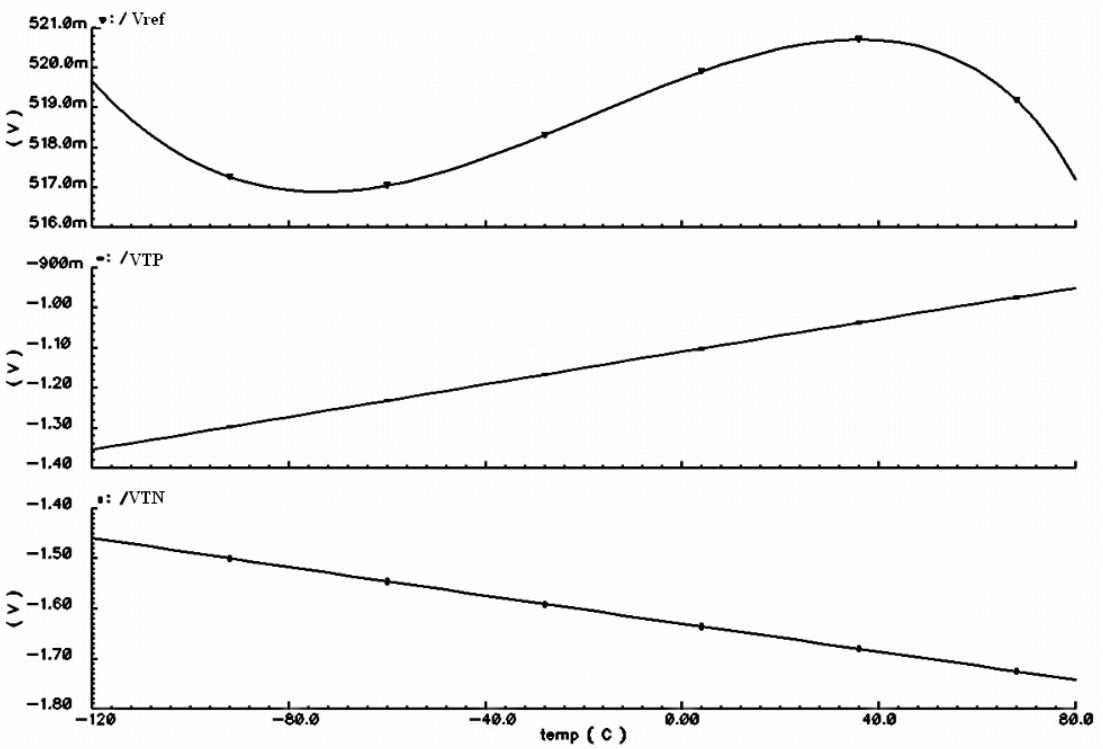


Figure 6.9: PTAT and CTAT voltages, and the sum of the two voltages.

The transfer function of this adder is,

$$V_{REF} = \frac{R + R_S}{R_S}\left(\frac{(V_{IN1}).R_P + V_{IN2}.R_N}{R_P + R_N}\right) - \frac{R.V_{SS}}{2.R_S} \qquad \textbf{(6.4)}$$

The input voltages are assumed as the following;

- The input coming from V_{TN} extractor is (V_{TN}+V_{SS}) because the output voltage of the V_{TN} extractor is referenced to V_{SS}.
- The second input, output of the V_{TP} extractor is equal to V_{TP} while it is referenced to ground.
- The out put voltage will be referenced to $V_{SS.}$

The transfer function of the adder can be rewritten by the help of assumptions,

$$V_{REF} + Vss = \frac{R + R_S}{R_S}\left(\frac{(V_{TN} + V_{SS}).R_P}{R_N.(R_P + R_N)} + V_{TP}\right) - \frac{R.V_{SS}}{2.R_S} \qquad \textbf{(6.5)}$$

R_P and R_N are combined to cancel the temperature coefficient difference of voltages V_P and V_N, while R and R_S is used for both purposes, one is to cancel V_{SS} dependency of the V_{IN1} voltage.

The presented two-stage OPAMP is used to realize adder and resistance values are given in Table 6.1.

Table 6.1: Resistances values of voltage reference circuit

Resistance	Value
RN	10K
RP	14.3K
R	34K
RS	10K

The circuit is tested over temperature from 0 ºC to 100 ºC and over the supply voltage between 4.5 and 5 V.

Figure 6.10 confirms that the resulting voltage is nearly 521mV, independent of temperature. The line sensitivity of the CMOS voltage reference was measured by noting how the output voltage changed as the supply voltage was varied from 4.5 to 5V. Over this supply range, the output voltage varied by 2 mV, which is shown in Figure 6.11.

6.4 Square-root Circuit Using a Threshold Voltage Extractor

There are many possibilities of implementation a voltage square-root circuit using the characteristic of the MOS transistor in saturation.

The proposed square-root circuit is implemented in Figure 6.12 using exclusively classic MOS transistors. The circuit realizes the square-root of the Io current at the output. Presented DDA is used to multiply V_{TP} voltage by 2 realized in Figure 6.12.

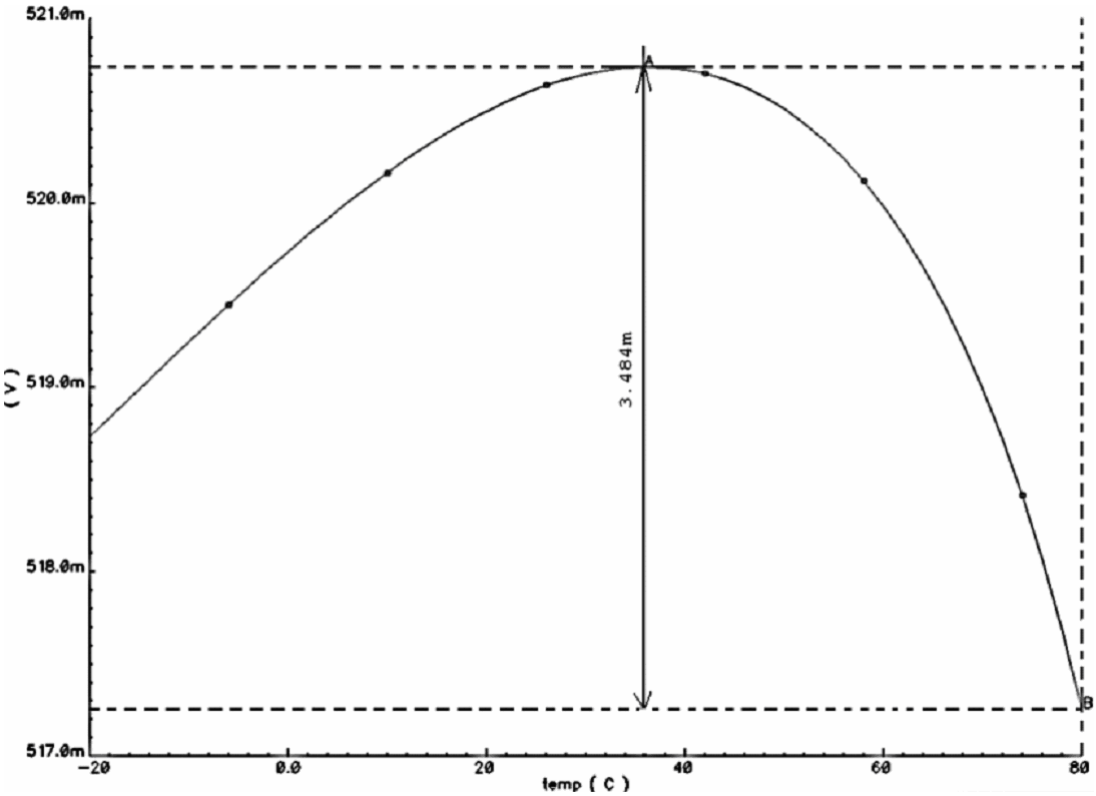


Figure 6.10: The output voltage of the voltage reference circuit versus temperature.

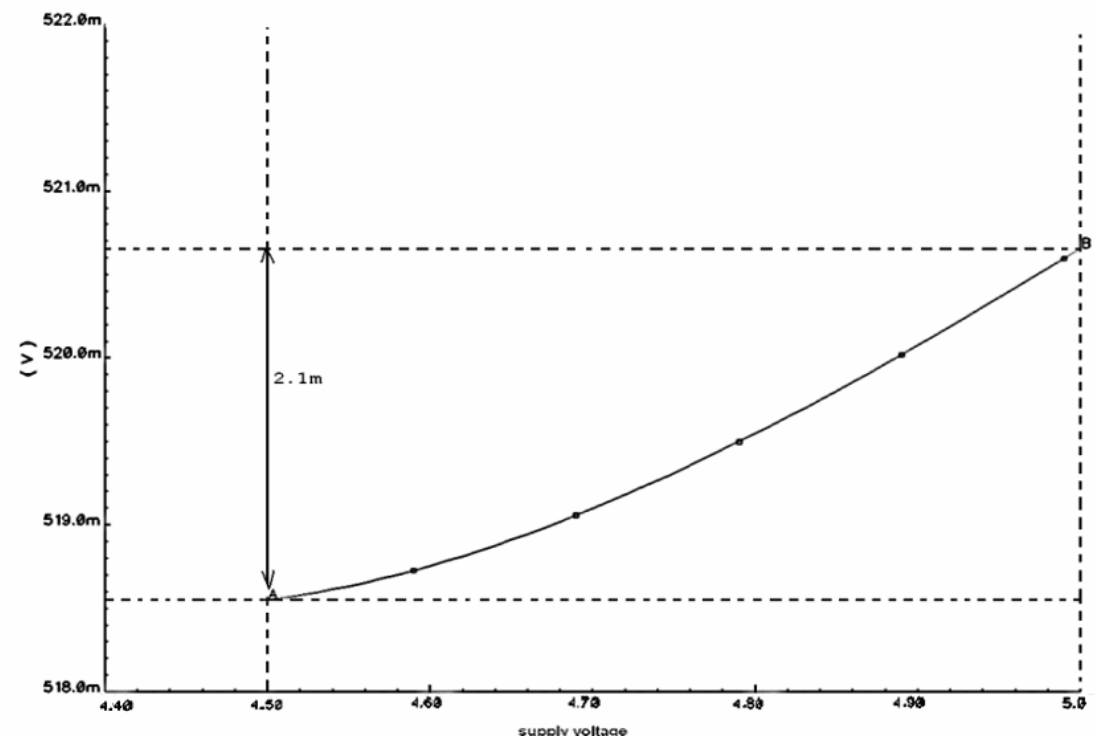


Figure 6.11: The output voltage of the voltage reference circuit versus supply voltage variation.

Obtained $2V_{TP}$ is applied to the gate of the reference transistor M_{P3} then it is mirrored to the gate of M_{P4} with the help of n-type (M_{N1}-M_{N2}) current mirror, assuming that all transistors are in saturation. With the use of single stage differential amplifier formed by M_{P5} and M_{P6}, $\sqrt{Io}$ is obtained.

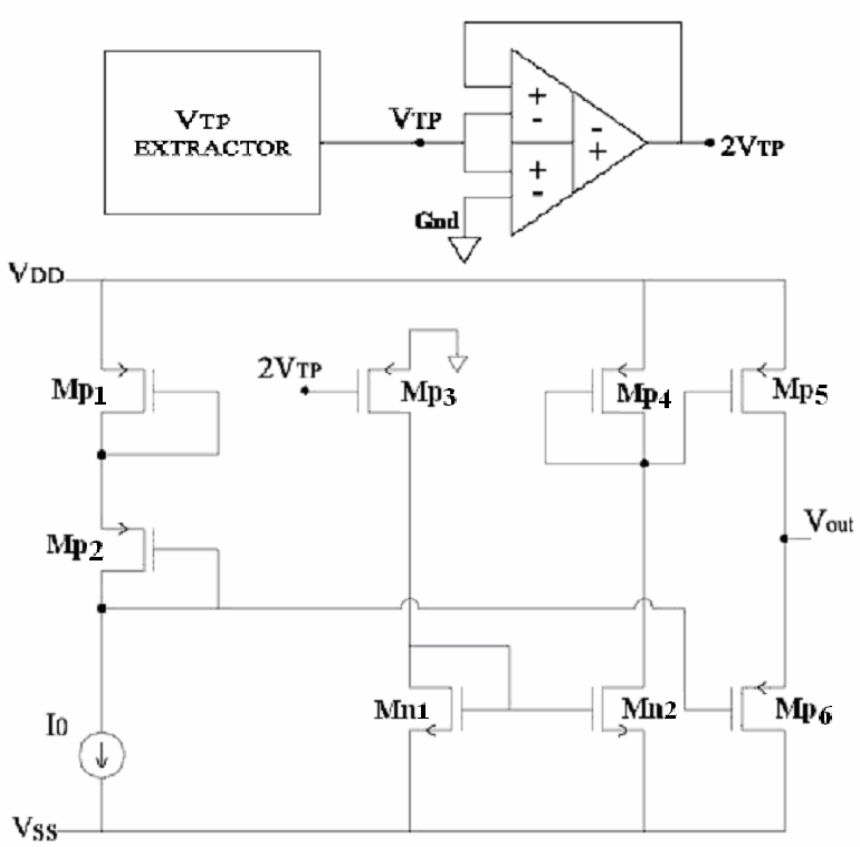


Figure 6.12: Square-root circuits using a threshold voltage extractor.

The output voltage expression of the presented square-root circuit is

$$Vout = 2V_{GSP} - 2V_{TP} \tag{6.6}$$

$$Vout = 2\left(\sqrt{\frac{2.Io}{\beta_P}} + |V_{TP}|\right) - 2.|V_{TP}| \tag{6.7}$$

$$Vout = \frac{2\sqrt{2}}{\beta_P}.\sqrt{Io} \tag{6.8}$$

We know that $\frac{2\sqrt{2}}{\beta_P}$ is a constant and can be renamed with A, so obtained voltage will be equal to,

$$V_{OUT} = A.\sqrt{Io} \quad \textbf{(6.9)}$$

Table 6.2: Transistor Ratios of Square-root circuit.

Transistor	**Type**	**W(μm)**	**L(μm)**
MP1	PMOS	50	1
MP2	PMOS	50	1
MP3	PMOS	50	1
MP4	PMOS	50	1
MP5	PMOS	50	1
MP6	PMOS	50	1
MN1	NMOS	150	1
MN2	NMOS	150	1

Table 6.3: Simulation results of Square-root circuit.

Outputs	**Obtained Results**	**Expected Results**
$2V_{GSP}$	-2.936	-2.950
$2V_{TP}$	-2.091	-2.104
V_{OUT}	0.920	0.848

Table 6.3 indicates discrepancies dependent on implementation, first one is $2V_{TP}$ voltage error because of the DDA output voltage range limitations and the second one is the difference in output voltage caused by the use of one stage differential stage (M_{P5} and M_{P6}) which does not have accurate result. In addition to these, the results of hand calculation and simulation results differ because of the iterations that Cadence-SpectreS uses.

β_P is found 1.2mA/V^2 so A is calculated 81.6 which can be approximated to 82, the simulated output of the square-root circuit is expected to be 820mV because of the relation (6.9). After simulation, we have obtained 920mV having %10 error, because of the non accurate output of the differencing stage. In order to have stable results more accurate output stages can be applied.

This usage of V_{TH} extractor is not practical so it is not preferred in square-root circuit applications especially where the silicon area procession is important. But by implementing this type of square-root circuit, we prove that V_{TH} extractor circuits can be adapted to various applications.

7. PROPOSED V_{TH} EXTRACTORS LAYOUT AND LAYOUT STRATEGY

It is not simple to achieve simulated V_{TH} value because of process variations and mismatches. So, layout techniques should be applied and layouts must be drawn very dense for both temperature and element matching (especially for open loop OPAMP).

7.1 Layout Strategy

In further subsections, the idea of layout placements will be explained in details which can be named as layout strategy. Layout strategy hierarchy is determined as: area consumption matching, symmetry and biasing.

7.1.1 Area Consumption

Generally in circuit layout, most important design parameter is the area consumption. Drawing the layout more compact affects the properties like matching and thermal gradients in a good way.

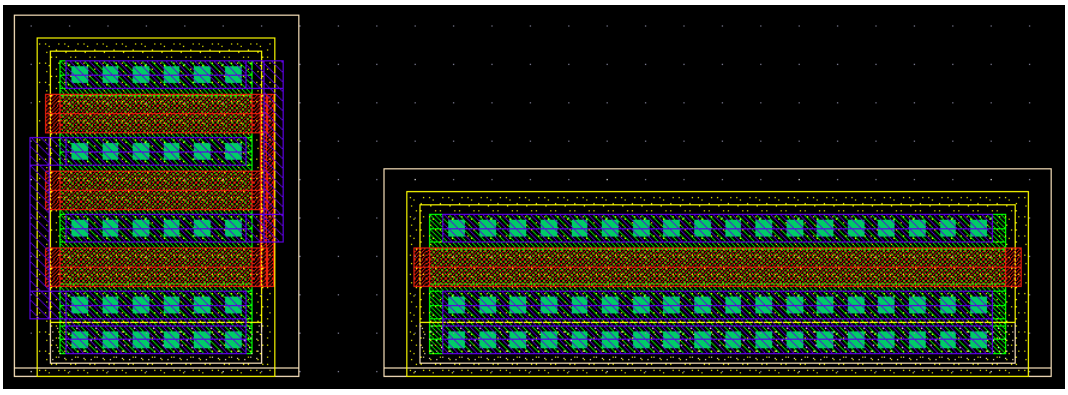


Figure 7.1: Layouts of different transistors of same gate length a) three fingered gate b) single finger gate

Simulations of the extractor circuits are realized with single gate transistors of AMS. AMS also provides multi-fingered-gate transistors. By using these transistors same gate area can obtained. Layout of single gate and three fingered gate transistors are

shown in Figure 7.1. Proper transistor selection of the circuit depends on transistor dimensions and placement of the circuit.

7.1.2 Matching

Matching of the elements in V_{TH} extractor circuit is an important issue while drawing the layout. In order to satisfy proper matching conditions, all of the same type of elements must be laid in the same direction.

Transistors in layout are placed as close as possible, provided that design rule check restrictions are not violated. Matching of mirrored currents is one of the most important issues on circuits design.

7.1.3 Biasing

It was shown before that matching of current sources directly affects systems' performance. In schematically representation, current is provided by the diode connected MOSFETs placed at the gate of current source transistors.

In V_{TH} extractor system, bias currents are applied to the gate of the diode connected transistors in order to produce required current values.

7.1.4 Power Routing

Supply voltages applied to the circuit must be routed with the metal interconnects that have minimum sheet resistance. As total current flowing along supply interconnect increases, voltage drop also increases.

In V_{TH} extractor layout, only Metal1 and Metal2 are used and power lines are routed with Metal2 which have low parasitic resistance in comprasion with Metal1. Number of metal crossing vias is placed as much as possible.

7.2 Proposed V_{TH} Extractors Layout

In this chapter, NMOS and PMOS V_{TH} extractor circuit, based on basic arithmetic operation, layout implementation is shown. In order to simplify the whole circuit, firstly auxiliary component layouts are designed then they are combined. In addition

to this, ideal current sources are replaced with two MOSFETs which require bias current.

Both NMOS and PMOS extractor circuit layouts are capable of processing W/L=5µm/1µm device under test.

7.2.1 Auxiliary Components Layout

Instead of drawing complicated circuit, auxiliary components layouts are drawn first then they are combined in appropriate way.

7.2.1.1 OPAMP Layout

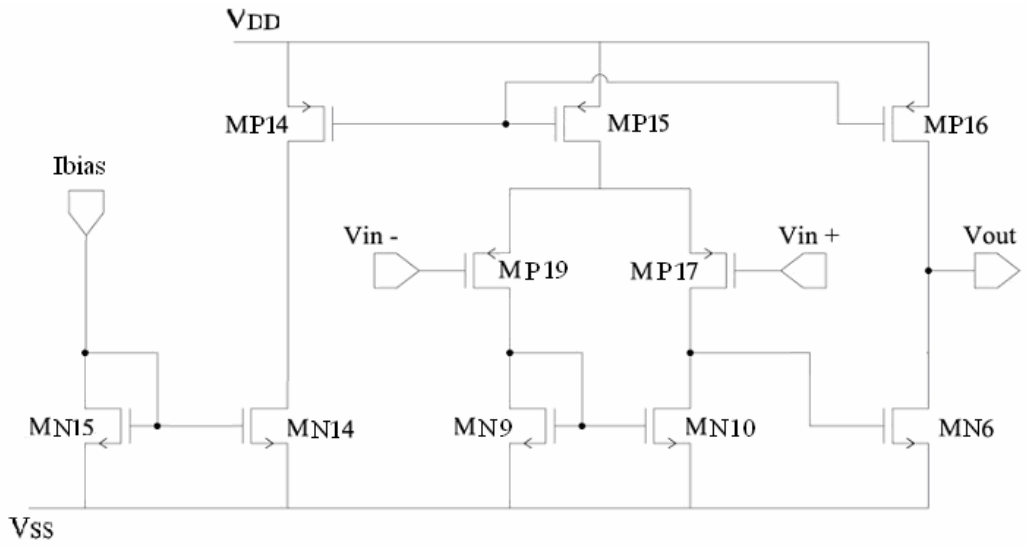


Figure 7.2: Schematic representation of OPAMP Layout

OPAMP layout in Figure 7.3 is formed dependent on the schematic view performing AMS process rules. DRC of layout is successful and LVS over the extracted view has also success. The whole OPAMP layout covers approximately “54µm x 45µm” chip area.

7.2.1.2 DDA Layout

As mentioned before, DDA is another auxiliary component which is used to form extractor circuit. In schematic representation of DDA have some modifications in order to feed circuit from one bias. (See Figure 7.4)

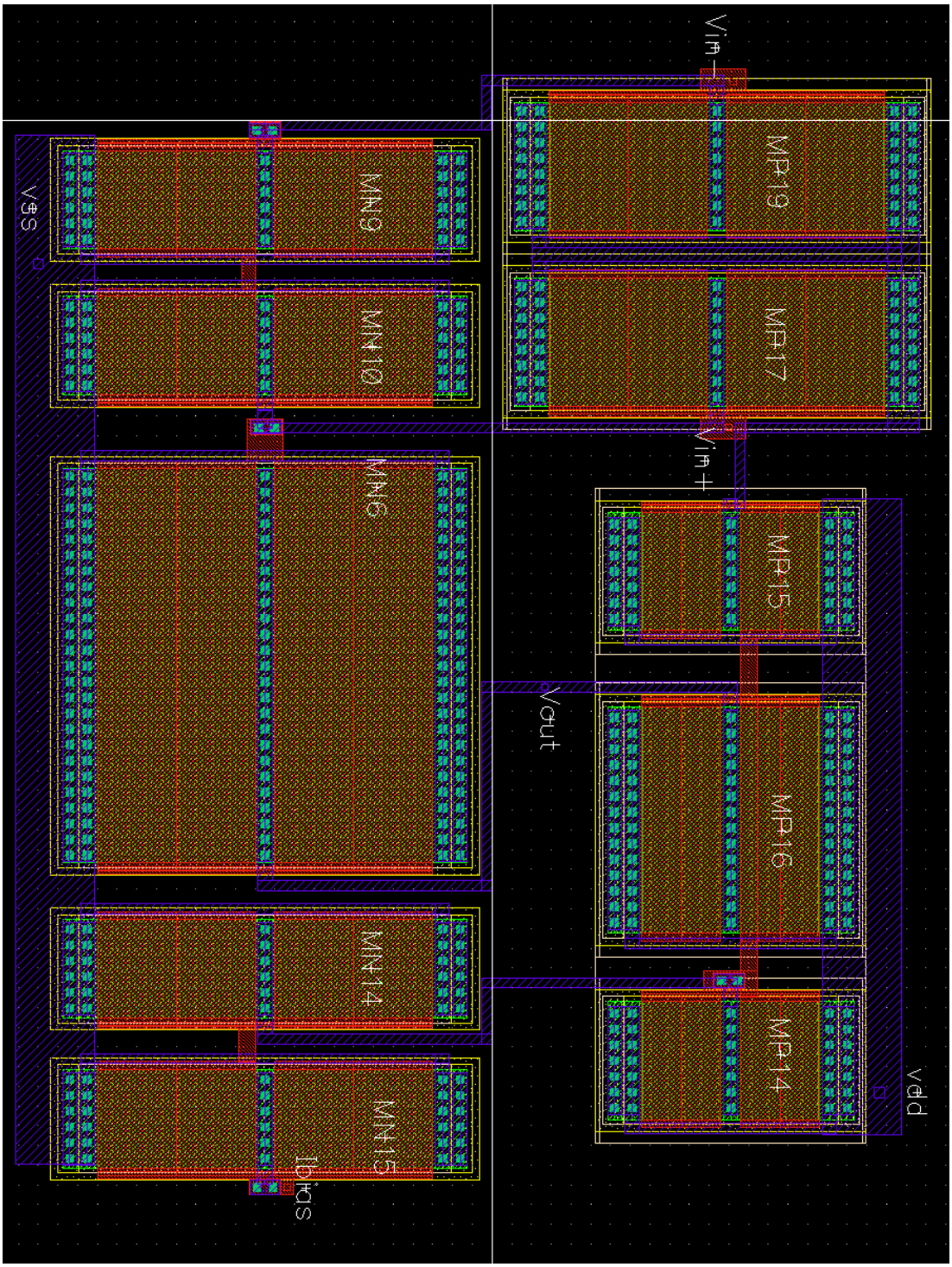


Figure 7.3: Layout of OPAMP

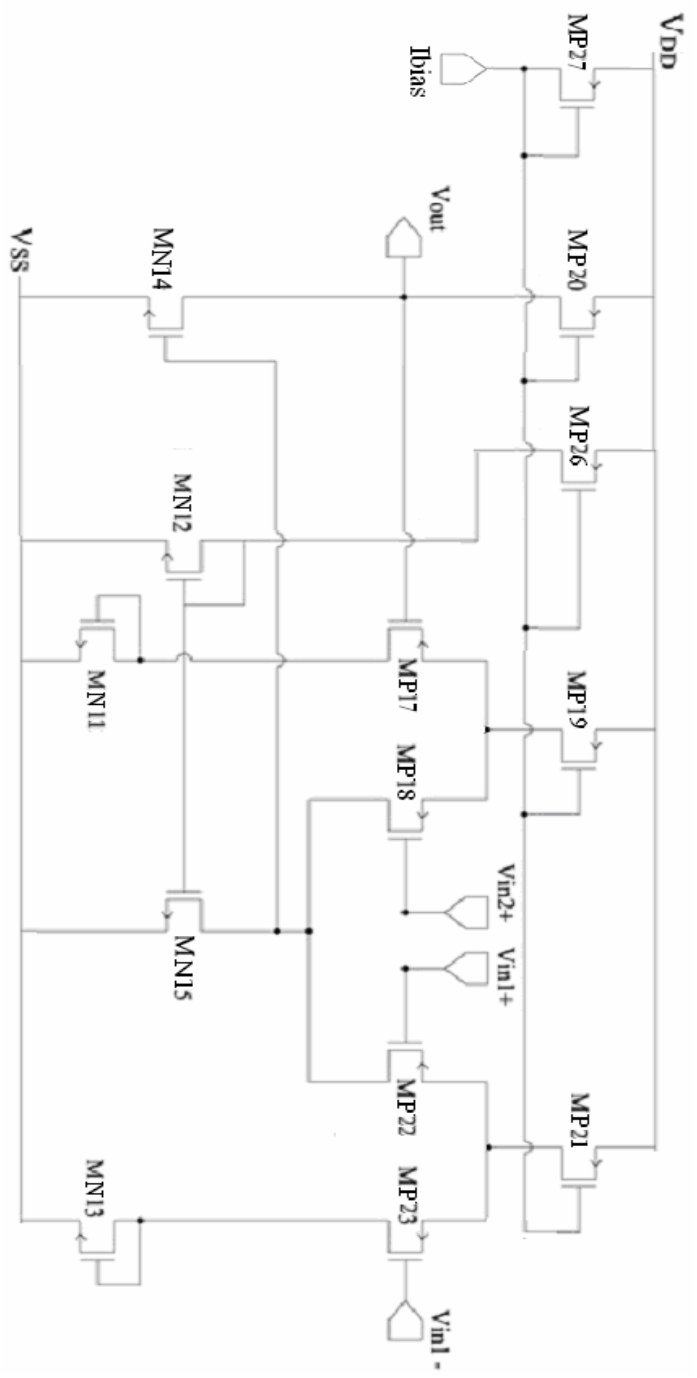


Figure 7.4: Schematic representation of DDA Layout

Rules of processing are performed while DDA layout in Figure 7.5 is formed depending on the schematic view. So Layout DRC and LVS are successful. The whole DDA layout covers approximately “76µm x 92µm” chip area chip area.

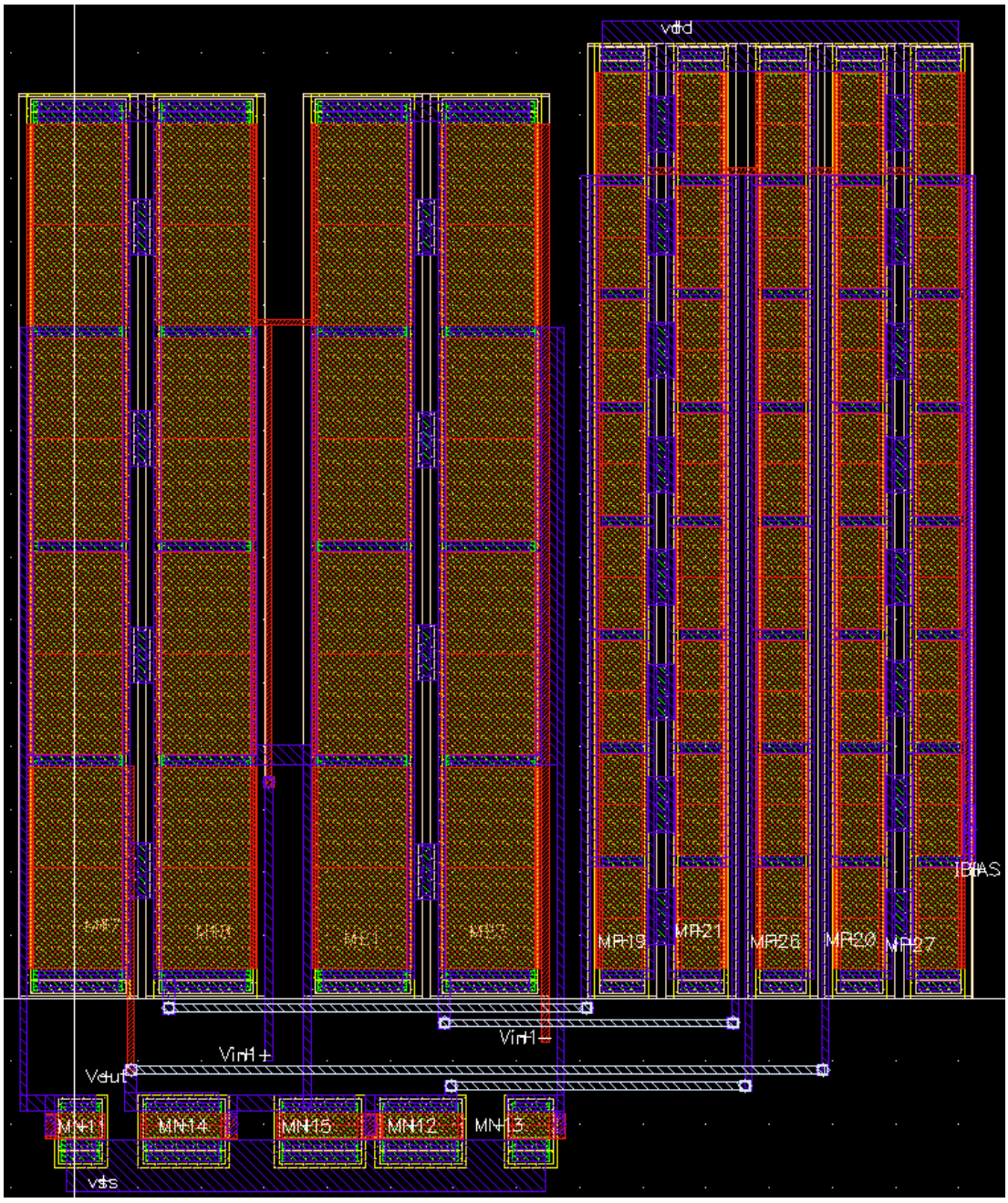


Figure7.5: Layout of DDA

7.2.2 V_{TN} Extractor Circuit based on Basic Arithmetic Operation Layout

NMOS V_{TH} extractor circuit layout, based on presented IDPC method, is implemented. Layout comes into existence with the use of auxiliary component layouts.

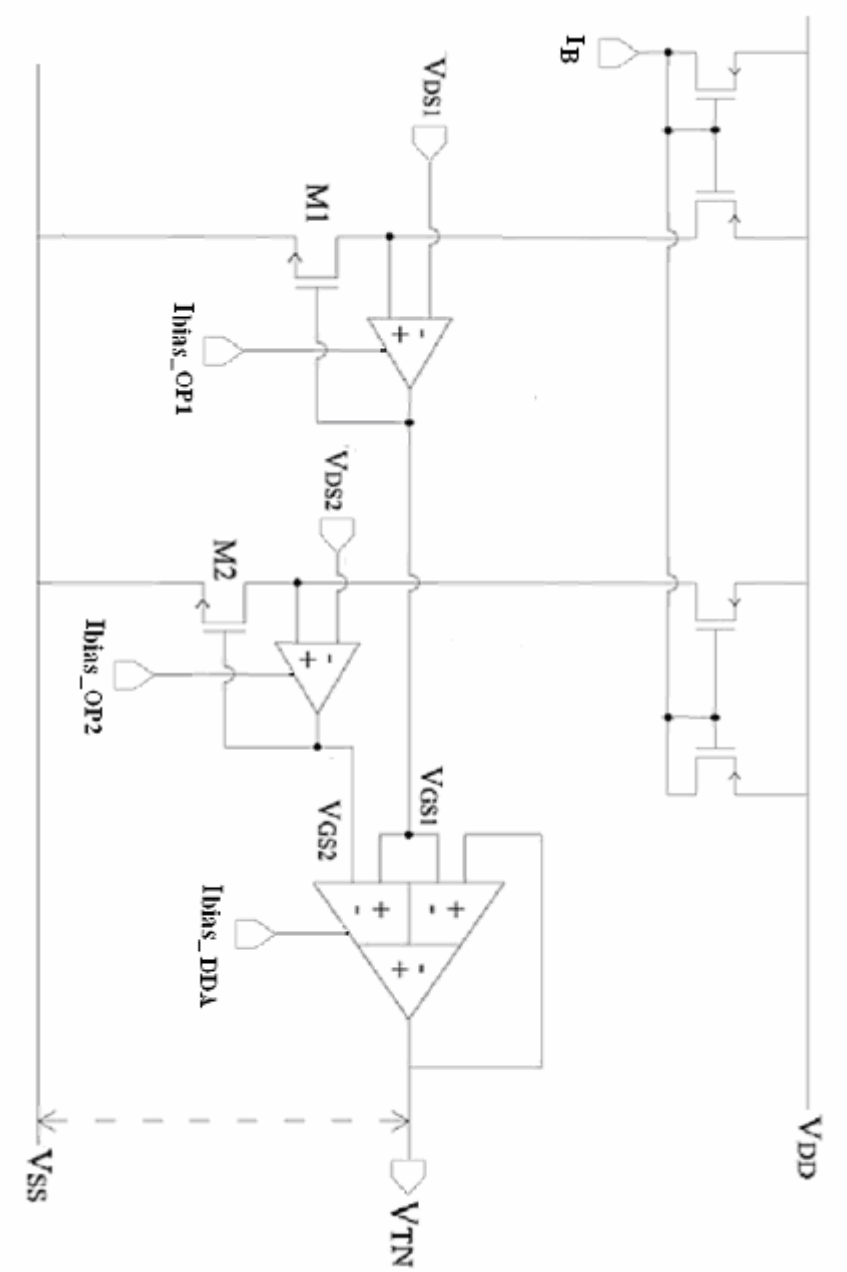


Figure7.6: Schematic representation of V_{TN} extractor based on basic arithmetic operation layout

In Figure 7.7 shows the layout of the V_{TN} extractor which is formed dependent on the schematic in Figure7.6.

Processing rules are performed so DRC is successful and extracted layout LVS matches with the schematic. The whole extractor layout covers approximately "165µm x 104µm" chip area.

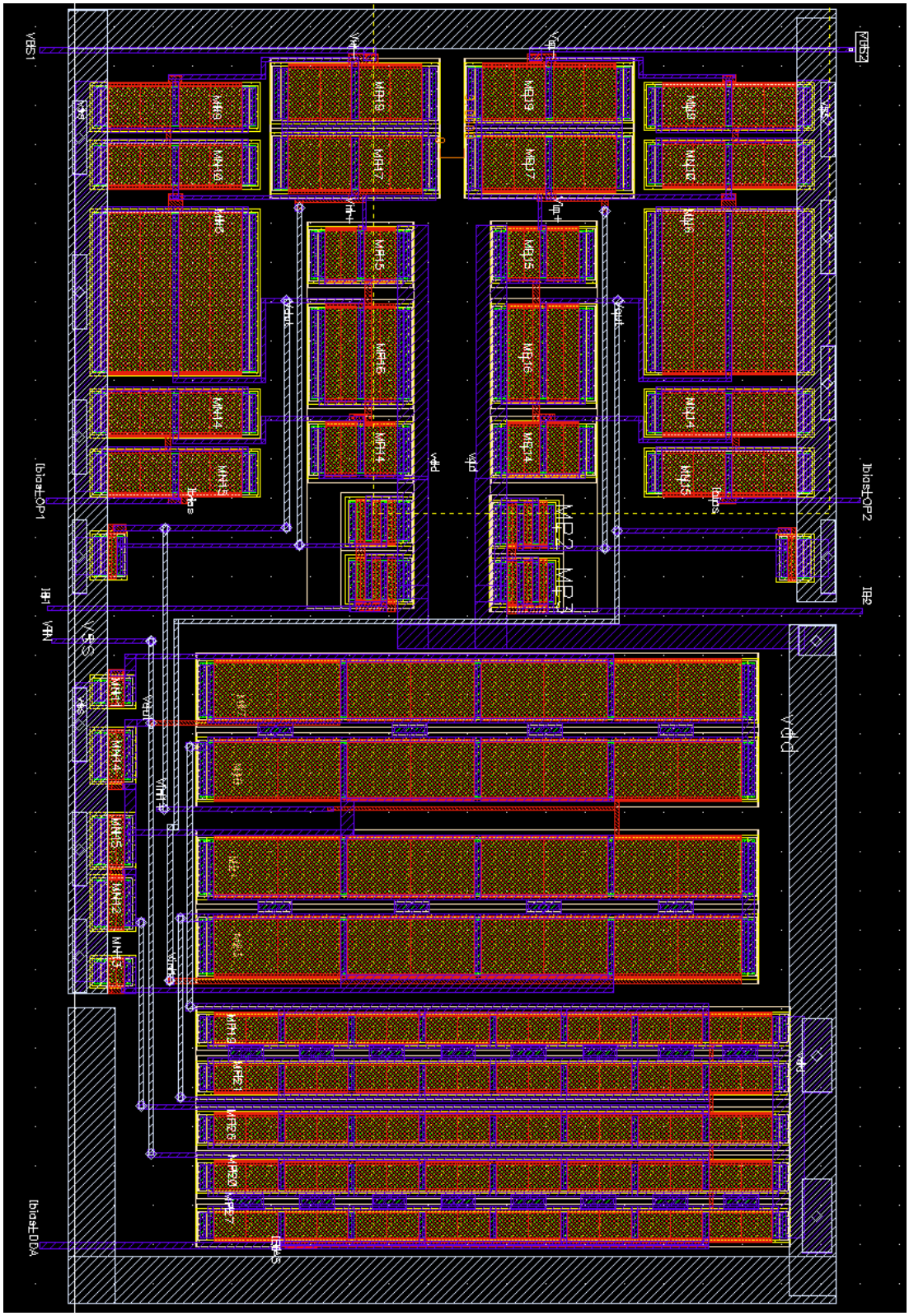


Figure7.7: Layout of V_{TN} Extractor based on basic arithmetic operation

7.2.3 V_{TP} Extractor Circuit based on Basic Arithmetic Operation Layout

The implementation of PMOS V_{TH} extractor circuit is shown in Figure7.8. The layout of this circuitry is realized based on presented IDPC method in Figure7.9. Whole layout consist auxiliary component layouts which help to realize the structure.

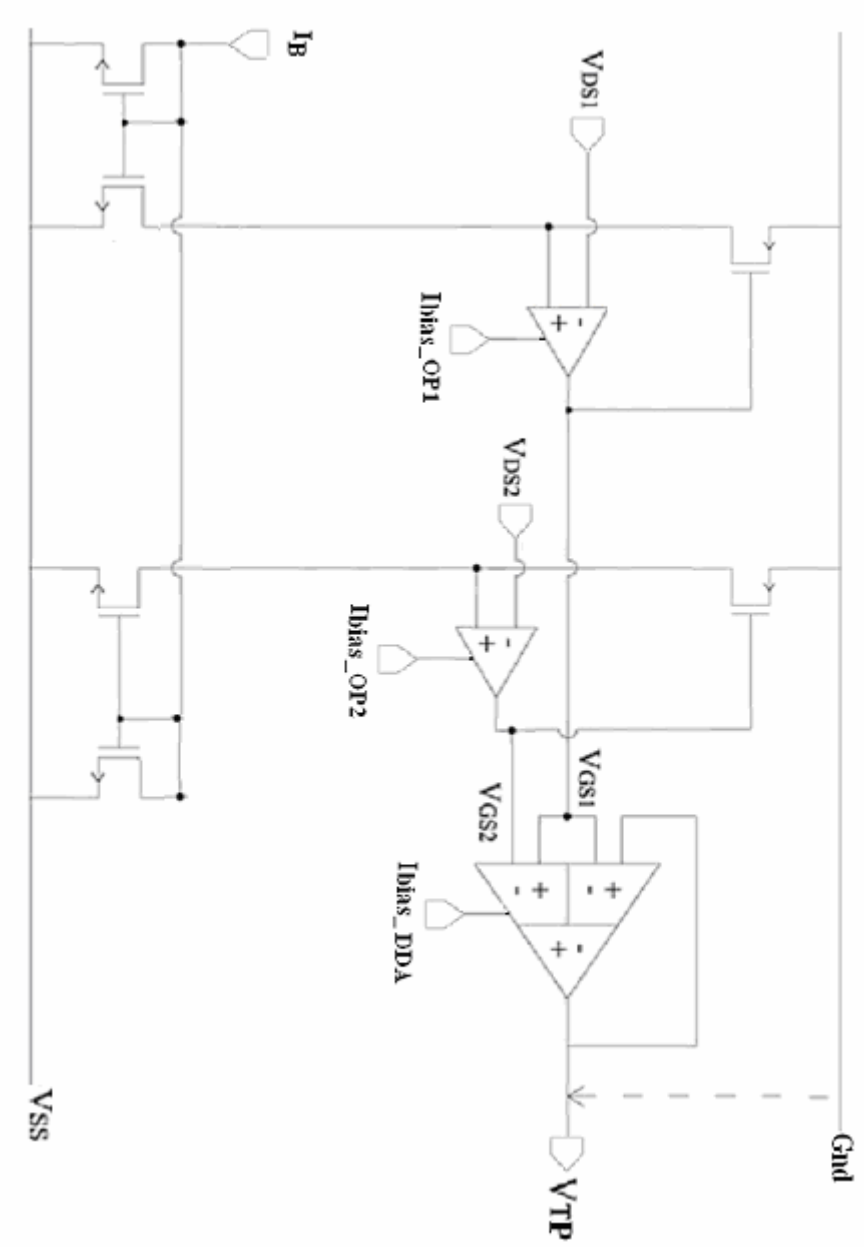


Figure7.8: Schematic representation of V_{TP} extractor based on basic arithmetic operation layout

Processing rules are performed so DRC is successful and extracted layout LVS matches with the schematic. The whole extractor layout covers approximately "167µm x 104µm" chip area.

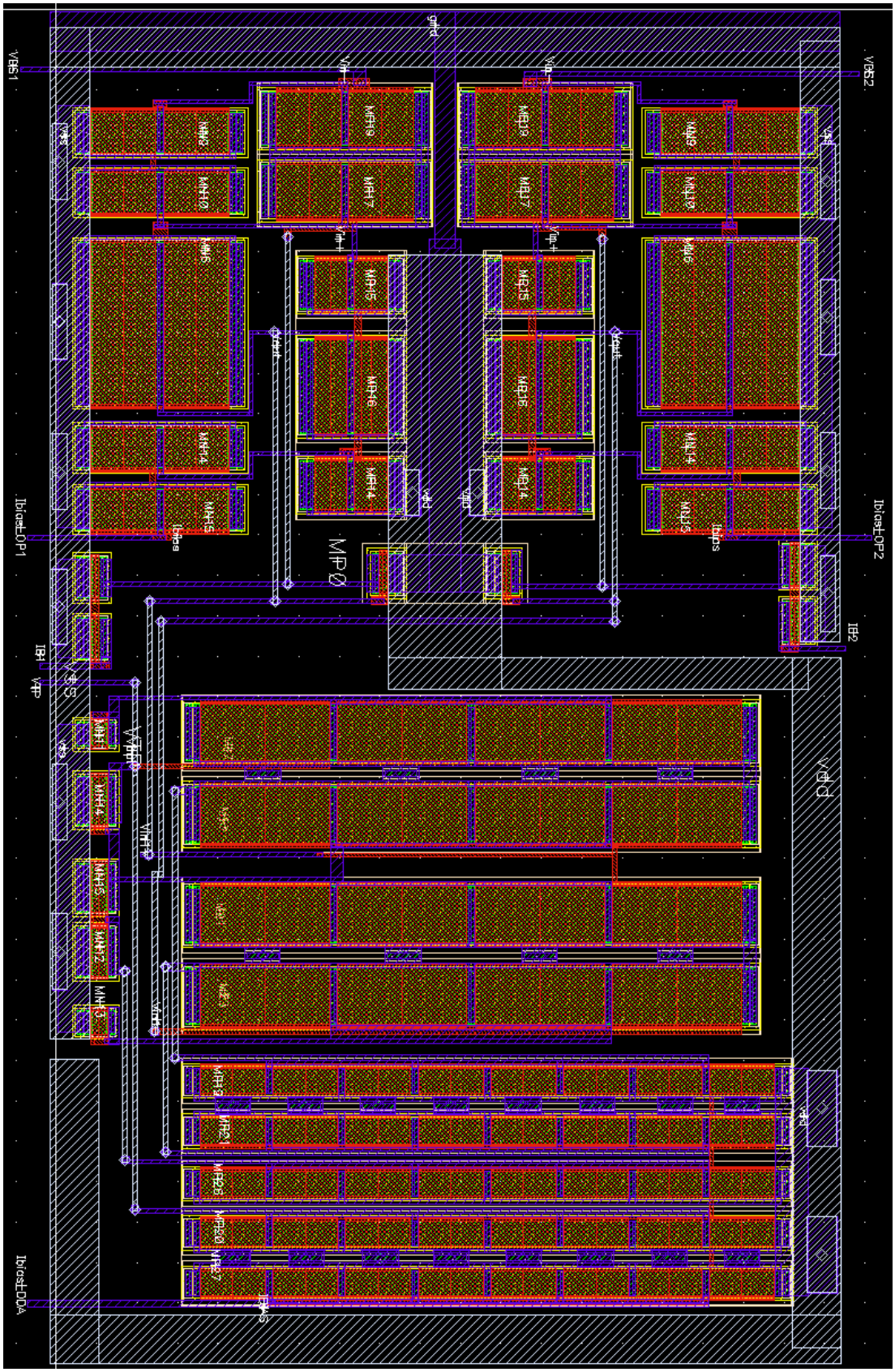


Figure7.9: Layout of V_{TP} extractor based on basic arithmetic operation

8. CONCLUSION

In this thesis, we have presented the existing methods to obtain threshold voltage of MOSFETs in two ways: Current/Voltage Measurement and Automatic Extraction. Firstly, we have reviewed several extraction methods currently used to determine the threshold voltage value of MOSFETs from their drain current and gate voltage measurements either in linear or saturation operation regions. Then, we have overviewed the existing automatic extraction circuits.

New methods for V_{TH} extraction are proposed based on the strong-inversion characteristic having the advantages of a very good accuracy. This method is divided into two main subjects based on the arithmetic operation, basic arithmetic operation and generalized arithmetic operation. Different implementations of V_{TH} extractors, using ICPD (identical current-proportional dimensions), IDPC (identical dimensions-proportional current) and Flexible (proportional dimensions-proportional current) method, have been discussed for both NMOS and PMOS transistors in basic arithmetic operation method. Generalized arithmetic operation is discussed with three methods but implementation of the extractors is developed by the means of IDPC method to show the extraction of NMOS threshold voltage. All methods are also applicable to PMOS with appropriate modifications.

The effect of nonidealities associated with MOS transistors such as mobility reduction, channel-length modulation, mismatch, body effect and temperature dependency has been examined.

The MOS V_{TH} extractor circuits have been simulated using Cadence-SpectreS simulator with AMS 0.35µm CMOS technology. The process, temperature and voltage variations are discussed and analyzed. The simulation results show that V_{TN} and V_{TP} have high accuracy of almost 100%. The V_{TN} and V_{TP} extractor have ability to work between 4.5V to 5V power supply.

The direct application of the proposed V_{TH} extractors is MOS transistor characterization. Using proposed structures V_{TH} of the transistor under test can be automatically measured, referenced to V_{SS} or Ground, respectively. Experimental results have indicated that the accuracy of this method is as good as the complicated and tedious numerical method.

The proposed circuits have the capability to extract V_{TN} voltage referenced to V_{SS} and V_{TP} voltage referenced to ground. The approximately linear dependencies with temperature of the threshold voltage make them suitable for applications like PTAT and CTAT sensors. In addition, a square-root circuit based on V_{TP} extractor has been implemented to confirm the adaptation capability of the extractors to various applications.

It has been also shown that the V_{TH} extractors can be advantageously applied to implement a voltage reference, independent from temperature and power supply fluctuations.

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Fulya Tezel was born in 8 April 1981 in Istanbul. She graduated from Silivri Super High School in 1999 and then she finished Electronics and Communication Engineering Department of Yıldız Tecnical University in 2003 with a "Third Degree of Graduation". After graduating from Yıldız Tecnical University, she has continued her education at Istanbul Tecnical University Master of Science in Electronics Engineering.

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