DESIGN OF A CONTINUOUS-TIME CURRENT-MODE SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER

by

Ahmet Yasin ÇİTKAYA

B.S. in E.E., Boğaziçi University, 2002

Submitted to the Institute for Graduate Studies in
Science and Engineering in partial fulfillment of
the requirements for the degree of
Master of Science

Graduate Program in Electrical and Electronics Engineering
Boğaziçi University
2006

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APPROVED BY:

Prof. Ömer Cerid (Thesis Supervisor)	……
Prof. Günhan Dündar	……
Assoc. Prof. Arda Yurdakul	……

DATE OF APPROVAL: 01.05.2006

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my thesis supervisor Prof. Ömer Cerid for his guidance, constructive critiques, motivation patience and continuous support.

I would also like to thank to Prof. Günhan Dündar for his kind interest and his valuable ideas through out the development of this thesis.

I would also like to thank Assoc. Prof. Arda Yurdakul for her kind interest and being a member of my thesis committee.

I would also like to thank to the instructors of the Electrical and Electronics Department of Boğaziçi University for their contributions to my education in electronics.

I am indebted to Umut Yazkurt and Mustafa Aktan for their continuous support and suggestions.

I would like to also thank Mehmet Yunus Dönmez for his help on the documentation of my thesis. Also special thanks to İpek Şen for her motivation in the toughest times of my study.

I would also like to express my thanks to BETA members for their help and friendship.

Finally, I thank to my family for their support and love that motivate me in handling and managing to finish my thesis.

ABSTRACT

DESIGN OF A CONTINUOUS TIME CURRENT-MODE SIGMA-DELTA ANALOG TO DIGITAL CONVERTER

The importance of the Analog-to-Digital converters (ADC) is increasing due to the necessity of an interface between the analog and digital world where computing and signal processing are executed.

Over the last years, their low cost development and good linearity made sigma-delta (ΣΔ) type converters widely available. In this thesis, due to their various advantages like low voltage operation, and lower power consumption than their discrete time (DT) counterpart, continuous time (CT) ΣΔ has been studied.

This thesis presents the design of a continuous time current-mode ΣΔ ADC starting from the building blocks as integrator, comparator and digital to analog converter (DAC) and its control circuitry. The transistor level circuit designs are verified with SPICE simulations.

ÖZET

SÜREKLİ ZAMANLI AKIM MODLU SİGMA-DELTA ANALOG / SAYISAL ÇEVİRİCİ TASARIMI

Analog / sayısal çeviricilerin önemi analog dünya ile hesap ve sinyal işlemenin gerçekleştiği sayısal dünya arasında bir arayüz olduğundan gün geçtikçe artmaktadır.

Geçtiğimiz yıllarda, düşük geliştirme maliyeti ve iyi lineer davranışları sigma delta tipi çeviricileri geniş kapsamda kullanılabilir yapmıştır. Bu tez kapsamında sürekli zamanlı sigma delta çeviriciler düşük çalışma gerilimi ve diğer benzeri ayrık zamanlı sigma delta çeviricilerden daha düşük güç tüketim gibi avantajlarından dolayı çalışılmıştır.

Bu tez ile akım modlu sürekli zamanda çalışan sigma delta analog sayısal çeviricinin tasarımı gerçekleştirilmiştir. Bu kapsamda tümlev devresi, karşılaştırıcı ve sayısal analog çevirici ve bu çeviricinin kontrol katı olan yapı blokları tasarlanmıştır. Bu tasarım nihayetinde SPICE benzetimi ile de doğrulanmıştır.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS / ABBREVIATIONS

A_{int}	Integrator gain
$A_{\Sigma\Delta}$	Gain of the input signal, which gives maximum SNR
C	Integrating capacitance
C_{ox}	Oxide capacitance
f_S	Sampling frequency
f_T	Device transition frequency
g_{ds}	Output conductance
g_m	Transconductance
I_o	Biasing current
I_{in}	Input current
k	Boltzman constant
L	Length of the transistor
m	Modulation index
T	Temperature
t_d	Delay time
V_{BC}	Cascode biasing voltage
V_{BS}	Bulk-Substrate voltage
V_{DD}	Positive power supply voltage
V_{EG}	Effective gate voltage
V_{o+}	Positive output-voltage
W	Width of the transistor
μ_n	Electron mobility
ΣΔ	Sigma-Delta
ω	Angular frequency
ADC	Analog-to-digital converter
AMS	Austria Micro Systems
BW	Bandwidth
CMOS	Complementary metal oxide semiconductor

CT	Continuous-time
DAC	Digital-to-analog converter
DC	Direct current
DT	Discrete-time
M	Metal oxide semiconductor field effect transistor
NMOS	N type metal oxide semiconductor
NRZ	Non-return-to-zero
OSR	Oversampling ratio
PMOS	P type metal oxide semiconductor
RZ	Return-to-zero
SC	Switched capacitor
SNR	Signal-to-noise ratio
SPICE	Simulation program with integrated circuit emphasis

1. INTRODUCTION

Analog-to-digital converters (ADCs) are important building blocks in all mixed-signal electronic systems. Over the last years, ADCs using the Oversampling Sigma-Delta (ΣΔ) modulation technique have become widely available, particularly for low-frequency applications such as high-fidelity audio, speech processing, metering applications, and voice-band data telecommunications [1].

Oversampling ΣΔ ADCs make more use of digital signal processing compared to the Nyquist-rate ADCs to perform analog-to-digital conversion. With the advantage of significantly relaxed matching requirements on analog components, they can achieve medium to high resolution in conversion of relatively low bandwidth signals. [2]. Using the oversampling method, ΣΔ ADCs do not need steep roll-off anti-alias filtering, which is usually required in Nyquist-rate ADCs. So power-hungry high-order high-linearity anti-alias filters with accurate cutoff frequencies are thus avoided [3]. In addition to the oversampling method, ΣΔ ADCs use the *noise-shaping* technique to reduce the quantization noise-power for further increasing the resolution of the conversion.

Many of the earlier ΣΔ ADCs are based on sampled-data or discrete-time (DT) ΣΔ modulators using switched capacitor (SC) techniques. The use of continuous-time (CT) ΣΔ modulators in ΣΔ ADCs has become very popular over the last years, mainly due to some advantages over the DT implementations. CT ΣΔ modulators can potentially operate at higher clock frequencies and/or consume less power [3].

Current-mode circuit techniques have recently become a viable alternative to conventional and SC circuits for CT and sampled-data analog signal-processing systems. With the ever-decreasing supply voltages, it becomes harder to design voltage-mode analog circuits with high linearity and wide dynamic range. Current-mode circuits merit considerable attention for signal-processing applications in scaled technologies because they operate with low power supply voltages due to their small voltage swings. High impedance nodes are not present in current mode circuits, and therefore their bandwidth

approaches the device transition frequency, f_T. Unlike voltage-mode SC circuits that require specially-processed floating linear capacitors, current-mode circuits are designed exclusively using active devices making them fully compatible with digital IC technologies [4].

Allowing to achieve more than 16-bits of resolution using an ADC as low as 1-bit, oversampling ΣΔ analog-to-digital conversion techniques constitute an interesting and sophisticated but also a very complex subject. Since both the current-mode and the continuous time approaches are relatively new and mainly promising for future ΣΔ converter implementations, in this thesis, we have focused on current-mode CT ΣΔ modulators. In addition to the literature search on the subject, we have designed a first–order current-mode CT ΣΔ modulator circuit.

The outline of this thesis is as follows. In section 2, motivations are introduced and the main objectives are stated. Section 3 discusses the design of the Low-Power Continuous-Time Current-Mode Integrators. Section 4 discusses the design of the Digital-to Analog Converter (DAC) of the modulator. In section 5, the simulation results are given.

2. PROBLEM DEFINITION AND MOTIVATION

2.1. Continuous-Time Versus Discrete-Time ΣΔ Modulators

In order to understand the main reasons for our interest in CT ΣΔ modulators, first of all we present the advantages and disadvantages of CT ΣΔ modulators compared to their DT counterparts.

In the following we will discuss the main advantages of CT ΣΔ modulators over their DT counterparts:

- Low voltage operation

  The continuously decreasing supply voltage of recent CMOS technologies is causing important limitations to the performances of switched-capacitor circuits.
- Sampling frequency

  In switched-capacitor circuits several errors occur while sampling the input signal. These errors are due to the switch non-linearity, charge injection, clock feedthrough and finite settling time. Sampling errors in switched-capacitor circuits limit the sampling frequency, f_S, of DT ΣΔ modulators.

  In CT modulators sampling occurs inside ΣΔ loop, therefore sampling errors are shaped out of the frequency band of interest just like quantization noise.
- Power Consumption

  In switched-capacitor circuits the unity gain frequency of the operational amplifiers must be at least five times the sampling rate. High quiescent current is then required to achieve high bandwidth. On the other hand, unity gain frequencies of the integrators in the CT ΣΔ are usually lower than the sampling frequency.

  Furthermore, since sampling occurs inside the ΣΔ loop, this strongly reduces the thermal noise aliasing in the frequency band of interest and aliasing of out of band signals, so that the antialiasing may be eliminated.

  It is then expected that for the same specifications, CT ΣΔ modulators will have lower power consumption than their DT counterparts.

While DT ΣΔ modulators are insensitive to the shape of the feedback signal as long as full settling occurs, the main disadvantages of CT ΣΔmodulators are related to switching characteristics of the feedback signal:

- Excess Loop Delay

  The delay in the feedback signal is mainly due to the comparator response-time. This delay has been found to alter the frequency response and degrade the signal-to-noise ratio (SNR) of the CT ΣΔ modulators [5]. Using a Return-to-Zero (RZ) feedback signal gives enough time for the comparator output to settle and thus eliminates any influence of the comparator delay on the SNR.
- DAC Output Rise and Fall Time Asymmetry

  Unequal rise and fall times of the DAC output current introduces harmonic distortion [6]. The effect of this waveform asymmetry can also be highly attenuated by the use of a RZ feedback DAC.
- Clock Jitter

  Clock jitter in feedback signal increases the noise level in the signal band. Unlike excess loop delay and DAC waveform asymmetry, clock jitter influence on the CT modulators cannot be attenuated by a RZ feedback signal. In fact, using a RZ feedback signal slighty increases the clock jitter effect on SNR.

The advantages and disadvantages of CT ΣΔ modulators compared to DT ΣΔ modulators are summarized in the following tables [7].

Table 2.1. Main advantages of CT ΣΔ modulators over DT ΣΔ modulators

	DISCRETE-TIME ΣΔ	CONTINUOUS-TIME ΣΔ
Input Switch Resistance	$r_{ds} = \frac{1}{\beta(V_{gs} - V_t)}$	No input switches
Sampling Errors	Critical	Shaped out of band
Unity Gain Frequency	$f_T = 5 * f_S$	$f_T \leq f_S$
Thermal Noise Aliasing	Increases noise level	Highly attenuated
Anti-Aliasing Filter	Essential	May be discarded

Table 2.2. Main disadvantages of CT ΣΔ modulators compared to DT ΣΔ modulators

	DISCRETE-TIME ΣΔ	CONTINUOUS-TIME ΣΔ
Excess Loop Delay	Low sensitivity	SNR degradation
Rise and Fall Time Asymmetry	Low sensitivity	Introduces harmonic distortion
Clock Jitter	Low sensitivity	Increases noise level

2.2. Continuous-Time ΣΔ Design Issues

2.2.1. System Design

In fact, CT ΣΔ are mixed CT-DT systems. While the input signal is continuous and the loop filter is composed of CT integrators, the output signal is sampled. The feedback DAC signal can either have a constant output during each clock cycle (NRZ case), or have its output change during the clock cycle (RZ cycle). This makes the calculation of the CT ΣΔ modulator coefficients, in order to obtain the required Noise Transfer Function (NTF), a mathematically difficult task [7].

2.2.2. Circuit Design

Continuous-time ΣΔ modulators are composed of CT integrators, comparators and feedback DACs:

- Integrator Circuit

  For proper operation of the CT ΣΔ modulator, integrator circuit frequency response must satisfy a specific transfer functions. In fact, each integrator has a gain, which is determined during system level design. This gain is also dependent on the sampling frequency of the modulator. Furthermore, the first integrator, along with the first feedback DAC, determines the circuit noise. (thermal and *1/f* noise) level of the modulator. Therefore the integrating capacitance and the biasing current of the first integrator have to be calculated carefully in order to satisfy the desired signal to

noise ratio while having the correct frequency response to insure proper operation of the ΣΔ modulator. Note however, that if the desired specifications cannot be met, the first integrator gain can be modified. In this case, it is necessary to go back to the system level design to scale the rest of the coefficients accordingly. The transistor lengths must be chosen in such a way that the area of the transistors is large enough to reduce the 1/f noise to the desired level. Satisfying all the above requirements while keeping the power consumption as low as possible, is indeed a challenging task in the circuit design of CT ΣΔ integrators.

- DAC Circuit and Digital control

  CT ΣΔ modulators are sensitive to the DAC output waveform characteristics. Any delay, rise and fall time asymmetry or jittered transitions can significantly degrade the signal to noise ratio of the modulator. The DAC circuit and its digital control circuitry have then tom be designed carefully in order to reduce all possible switching errors. Moreover, since the first DAC transistors contribute thermal and 1/f noise to the modulator, transistors dimensions must be chosen carefully.

2.3. Low Power Low Voltage Current Mode Circuit Design

Current mirror based circuits have been used to design the CT integrators. A design method is used to obtain the maximum modulation index (the ratio of the input signal over the biasing current). It is shown, by theoretical analysis and simulations, that maximum modulation index is obtained for significantly lower than the maximum supply voltage of a given technology. It is found that there exists an optimum supply voltage for minimum power consumption. This interesting result indicates that current-mode circuits may have interesting performances in recent and future low voltage CMOS technologies. The main source of harmonic distortion of the current mode integrator is transconductance variation with the input signal [8].

As a result, it has been shown that their advantages concerning low-voltage, low-power and high sampling frequency, CT ΣΔ modulators may outperform conventional DT ΣΔ modulators, especially in recent and future low-voltage CMOS technologies.

3. LOW POWER DESIGN OF CONTINUOUS TIME CURRENT MODE INTEGRATORS

3.1. Continuous-Time Current-Mode Integrator

Continuous-time current-mode integrators are based on the current-mirror circuit shown in Figure 3.1.

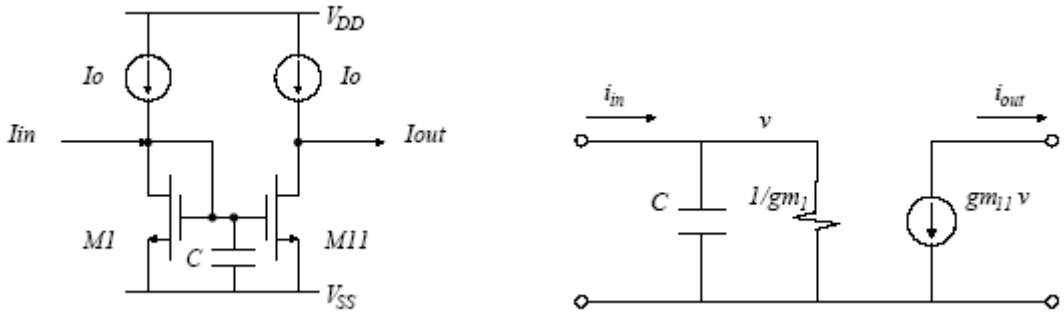

Figure 3.1. The simple current-mirror and its small-signal equivalent circuit.

Neglecting output conductances and parasitic capacitances and assuming identical transistors, we can derive the transfer function of the current-mirror circuit from the small-signal equivalent circuit,

$$H_{mir}(s) = \frac{i_{out}(s)}{i_{in}(s)} = \frac{-\frac{g_{m11}}{C}}{s + \frac{g_{m1}}{C}} \tag{3.1}$$

The differential current-mode integrator, shown in Figure 3.2, has been proposed in [9] and [10]. The circuit is composed of two cross-coupled current-mirrors and two output stages.

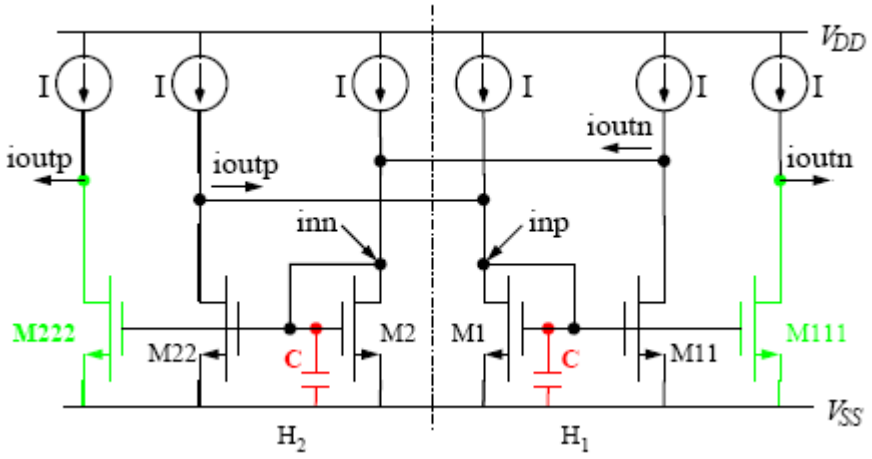

Figure 3.2. Differential current-mode integrator

In order to analyze this differential current-mode integrator, we will use the mathematical model described in Figure 3.3, where $H_1(s)$ and $H_2(s)$ are the transfer functions of the two cross-coupled current-mirrors. Assuming that the aspect ratio of all mirror transistors is equal to 1, the two output stages are omitted from the representation shown in Figure 3.3.

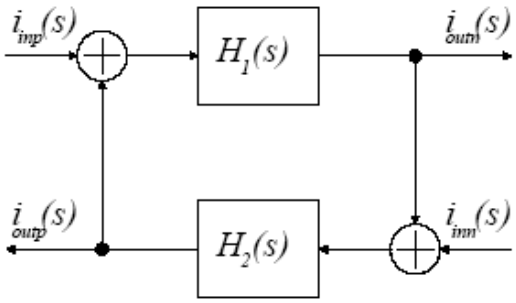

Figure 3.3. Mathematical model of the current-mode integrator of Figure 3.2.

The differential output current can then be described by

$$i_{outp}(s) - i_{outn}(s) = \left[\frac{H_1(s)H_2(s) - H_1(s)}{1 - H_1(s)H_2(s)}\right] i_{inp}(s) - \left[\frac{H_1(s)H_2(s) - H_2(s)}{1 - H_1(s)H_2(s)}\right] i_{inn}(s) \quad (3.2)$$

Assuming $i_{in}(s) = i_{inp}(s) = -i_{inn}(s)$, the input-output relation is found to be

$$\frac{i_{outp}(s)-i_{outn}(s)}{i_{in}(s)}=\frac{2H_1(s)H_2(s)-H_1(s)-H_1(s)-H_2(s)}{1-H_1(s)H_2(s)} \tag{3.3}$$

by substitution from Equation (3.1) into Equation (3.3), we get

$$\frac{i_{outp}(s)-i_{outn}(s)}{i_{in}(s)}=\frac{s\dfrac{g_{m11}+g_{m22}}{C}+\dfrac{\left(g_{m1}g_{m22}+g_{m2}g_{m11}+2g_{m11}g_{m22}\right)}{C^2}}{s^2+s\dfrac{\left(g_{m1}+g_{m2}\right)}{C}+\dfrac{\left(g_{m1}g_{m2}-g_{m11}g_{m22}\right)}{C^2}} \tag{3.4}$$

In the case of all mirror transistors having the same transconductance g_m, the transfer function of the differential circuit shown in Figure 3.2 becomes

$$\frac{i_{outp}(s)-i_{outn}(s)}{i_{inp}(s)-i_{inn}(s)}=\frac{g_m}{sC} \tag{3.5}$$

It is obvious from Equation (3.4), that this current-mode integrator is sensitive to the g_m matching. Thus, it is important to study the effect of g_m mismatch on the transfer function of the integrator.

In the derivation of Equation (3.4), the output conductance g_{ds} of the mirror transistors has been neglected. If it is taken into account, the differential current-mode integrator will have the following transfer function

$$\frac{i_{outp}(s)-i_{outn}(s)}{i_{inp}(s)-i_{inn}(s)}=\frac{\dfrac{g_m}{C}}{s+\dfrac{g_{ds}}{C}} \tag{3.6}$$

The DC gain of the integrator is then determined by the ratio $\frac{g_m}{g_{ds}}$. In order to have a sufficiently low output conductance, a cascode current-mirror configuration is used. In Figure 5.4 we illustrate the cascode current-mirror-based integrator.

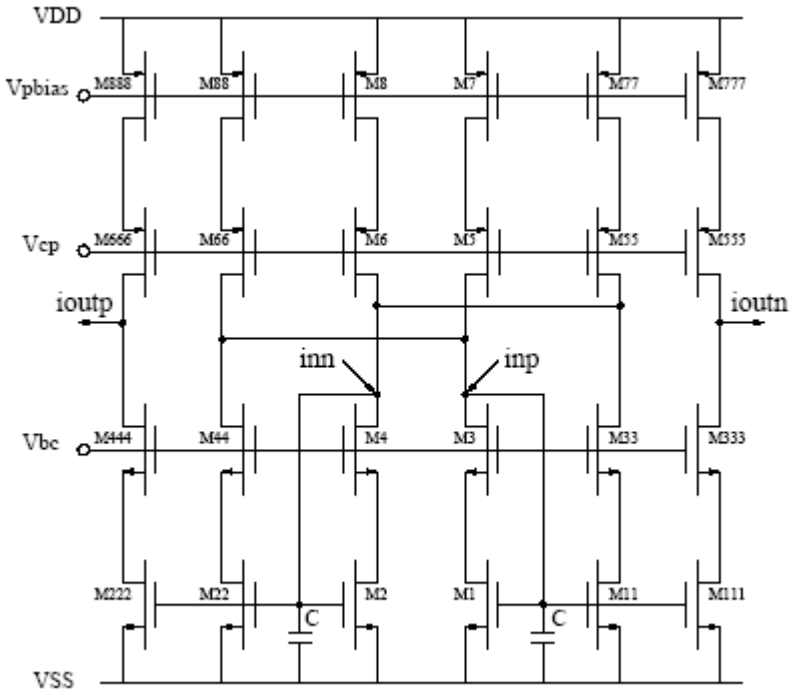

Figure 3.4. Differential cascode current-mode integrator

In the next section we will present a design method for the high swing cascode current-mirror [11] shown in Figure 3.5.

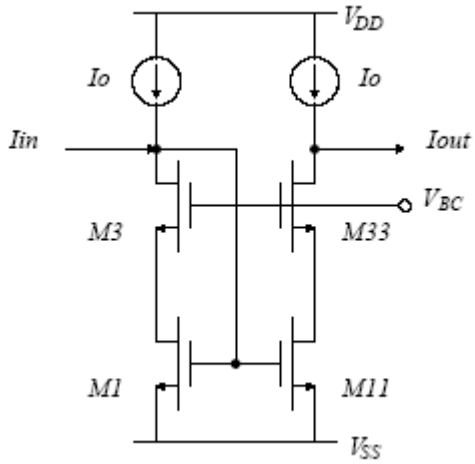

Figure 3.5. Cascode current-mirror

This method is used to obtain the maximum modulation index $m = I_{in} / I_o$, where

I_{in} is the input current and I_o is the biasing current. By theoretical analysis and simulations it can be shown that, the maximum modulation index is obtained for supply voltages significantly lower than the maximum supply voltage of a given technology [7].

3.2. Cascode Current Mirror Modulation Index

In this section a method to bias the cascode current-mirror shown in Figure 3.5 is described. This method gives maximum modulation index m for a given V_{eg10} and V_{eg30}, the effective gate voltage $\left(V_{gs}-V_{th}\right)$for $I_m = 0$, of the mirror transistor M_1, and the cascode transistor M_3 respectively. This method also gives the optimum value for the cascode transistor biasing voltage V_{BC}, in order to obtain maximum modulation index.

Starting from the simple square model of a MOS transistor in the saturation region,

$$I = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{GS}-V_{TH}\right)^2 \tag{3.7}$$

where μ_n is the electron mobility, C_{ox} is the oxide capacitance, W and L are the transistor's width and length respectively. Taking $\beta = \mu_n C_{ox}\cdot\frac{W}{L}$, the effective gate voltage, $V_{EG} = \left(V_{GS}-V_{TH}\right)$, can be written in function of the modulation index, $m = I_{in}/I_o$, as described in the following,

$$\begin{aligned} V_{EG} &= \sqrt{\frac{2I}{\beta}} = \sqrt{\frac{2\left(I_0 \pm I_{in}\right)}{\beta}} \\ V_{EG} &= \sqrt{1\pm m}\sqrt{\frac{2I_0}{\beta}} \\ V_{EG} &= \sqrt{1\pm m}\cdot V_{EG0} \end{aligned} \tag{3.8}$$

where $0 < m < 1$.

The condition for the mirror transistor M_1 to be operating in the saturation region:

$$\begin{aligned} V_{DS1} &\geq V_{GS1} - V_{TH1} \\ V_{BC} - V_{GS3} &\geq V_{GS1} - V_{TH1} \\ V_{BC} &\geq V_{EG1} + V_{EG3} + V_{TH3} \end{aligned} \tag{3.9}$$

Note that this condition must be considered for high input current, i.e. when $V_{EG1} = \sqrt{1+m} \cdot V_{EG0}$. In this case, the input-node voltage rises, consequently V_{GS1} increases and transistor M_1 could be driven out of the saturation region.

The condition for the cascode transistor M_3 to be operating in the saturation region:

$$\begin{aligned} V_{DS3} &\geq V_{GS3} - V_{TH3} \\ V_{GS1} - V_{DS1} &\geq V_{GS3} - V_{TH3} \\ V_{GS1} - V_{BC} + V_{GS3} &\geq V_{GS3} - V_{TH3} \\ V_{BC} &\leq V_{EG1} + V_{TH1} + V_{TH3} \end{aligned} \tag{3.10}$$

Note that this condition must be considered for low input current, i.e. when $V_{EG1} = \sqrt{1-m} \cdot V_{EG0}$ In this case, the input-node voltage diminishes, consequently V_{DS3} decreases and transistor M_3 could be driven out of the saturation region.

By substitution, from Equation (3.7) in Equation (3.9) and Equation (3.10) we get

$$V_{BC\min} = \sqrt{1+m} \cdot \left(V_{EG10} + V_{EG30}\right) + V_{TH3} \tag{3.11}$$

$$V_{BC\max} = \sqrt{1-m} \cdot V_{EG10} + V_{TH1} + V_{TH3} \tag{3.12}$$

In order to get maximum modulation index m we equate these two equations. By equating Equation (3.11) and Equation (3.12), we get

$$\sqrt{1+m}\left(V_{EG10} + V_{EG30}\right) - \sqrt{1-m} \cdot V_{EG10} - V_{TH1} = 0 \tag{3.13}$$

Since $V_{BC}= V_{GS30}+V_{DS10}$, and by substitution in Equation (3.12), we can deduce the value of V_{DS1}

$$V_{DS10} = \sqrt{1-m} \cdot V_{EG10} - V_{EG30} + V_{TH1} \tag{3.14}$$

Knowing V_{DS10}, we can get V_{BS3}, the Bulk-Substrate voltage of M_3, and then calculate V_{TH3} from the transistor model equations. From the values of V_{EG30} and V_{TH3} , the cascode biasing voltage V_{BC} can easily be deduced.

3.3. Integrating Capacitance and Biasing Current

In this section, we will define the design equations of a current-mirror based integrator for continuous-time ΣΔ modulator. The biasing current and the capacitance of this integrator are chosen to satisfy the thermal noise requirements and the bandwidth specifications of the modulator. It is known that there exists an optimum operating supply voltage for minimum power consumption of the integrator. For the correct operation of the modulator the following relation must be satisfied:

$$\frac{g_m}{C} = \frac{A_{\text{int}}}{T} = A_{\text{int}} f_S \tag{3.15}$$

Thermal noise calculations determine the minimum integrating capacitance C, and the minimum biasing current I_o necessary to achieve the required signal-to-noise ratio. Two design equations are given for calculating first the minimum integrating capacitance C and from that the biasing current I_o for a desired ∑Δ modulator with the input specifications of SNR, input signal bandwidth f_B, OSR and the integrator gain A_{int},

$$C = \frac{40 \cdot SNR_{th} 4kT}{A_{\text{int}} \cdot m^2 \cdot A_{\Sigma\Delta}^2 \cdot V_{EG10}^2 \cdot OSR} \tag{3.16}$$

$$I_O = \frac{40 \cdot SNR_{th} 4kT \cdot f_B}{m^2 \cdot A_{\Sigma\Delta}^2 \cdot V_{EG10}^2} \tag{3.17}$$

where m is the modulation index equal to I_{inmax}/I_o (ratio of the maximum input current to the biasing current), $V_{EG10} = V_{GS}-V_{th}$ of M_1, $A_{\Sigma\Delta}$ is the gain of the input signal which gives maximum *SNR* (usually equal to 0.5), k is the Boltzman constant and T is the temperature.

3.4. System Level Design Parameters

3.4.1. Oversampling Ratio

Along with the order of the ∑Δ modulator, the oversampling ratio, OSR, is chosen in such a way that the quantization noise is sufficiently low compared to the circuit thermal noise. The bandwidth of a ∑Δ modulator can be written in function of the sampling frequency, f_S, and the oversampling ratio,

$$BW = \frac{f_S}{2 \cdot OSR} \tag{3.17}$$

3.4.2. $A_{\Sigma\Delta}$

$A_{\Sigma\Delta}$ is the gain of the input signal which gives maximum signal-to-quantization-noise ratio. In ∑Δ modulator peak signal-to-noise ratio is usually obtained for a signal input amplitude lower than the maximum allowable input signal. The maximum allowable input signal of the integrator is usually given by I_{ref}. The modulation index determines this amplitude $I_{ref} = mI_o A_{\Sigma\Delta}$ is determined by simulation and is usually equal to 0.5.

3.4.3. A_{int}

Although the integrator gain, A_{int}, is also determined during system level design, we will see, in the next sections, that this value can be modified during circuit design. This is due to the considerable impact of the first integrator's gain on the linearity of the ∑Δ modulator. The gain of the other integrators will have to be scaled accordingly in order to keep the modulator transfer function unaltered.

3.5. Circuit Level Design Paramaters

3.5.1. The Effective Gate Voltage, V_{EG}

It can be seen easily from the equations that increasing the V_{EG} improves the signal-to-noise ratio. The effective gate voltage V_{EG} is dependent on the supply voltage V_{DD}. In this design transistors are biased such that their effective gate voltage $V_{EG} = 0.5V_{DD} - V_{TH}$. Due to the continuously decreasing supply voltages of the new CMOS technologies, it is expected that the effective gate voltage will decrease in future technologies [7].

3.5.2. The Modulation Index, m

Maximizing the modulation index, *m*, can significantly increase the signal-to-noise ratio. Calculations and simulations of the modulation index of cascode current-mirror has been shown that by proper biasing, modulation index close to the maximum, 1, can be obtained even for low voltage supply.

3.5.3. The Integrating Capacitance, *C*

The integrating capacitance, *C*, can be increased to compensate for any reduction in the effective gate voltage due to the low supply voltage of recent and future technologies.

4. CONTINUOUS TIME RETURN TO ZERO FEEDBACK DAC

4.1. Non-Return-to-Zero Feedback DAC

In the following, we will discuss the two main sources of errors in continuous-time ΣΔ modulators with Non-Return-to-Zero (NRZ) feedback signal.

4.1.1. Loop Delay

Any extra delay in the modulator loop modifies the response of the continuous-time modulator [12, 13]. The excess loop delay is mainly due to comparator response-time and the latch propagation delay. It has been shown in [5] and [14], that excess loop delay can have significant degrading effect on the SNR and may even affect the stability of the modulator.

Note also that for small signal amplitudes, the comparator response-time becomes signal dependent. This has the effect of jittering the edges of the NRZ feedback signal and consequently increasing the noise level in the signal band [15].

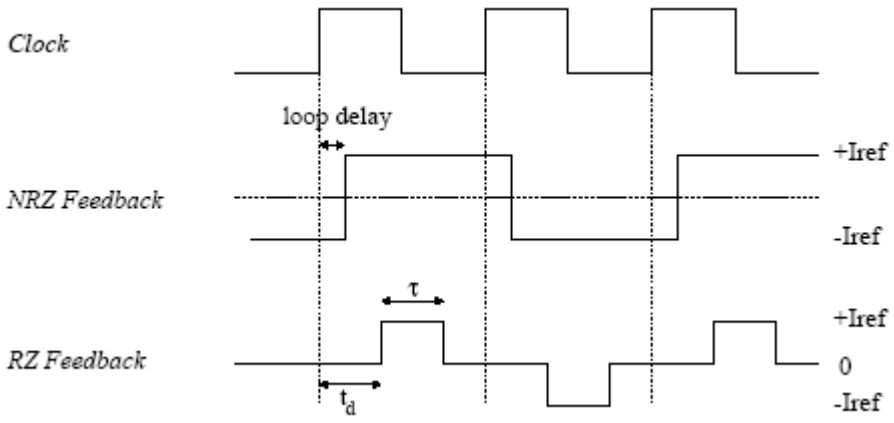

Figure 4.1. Rise and fall time asymmetry

If a Return-to-Zero (RZ) feedback signal is used, signal-to-noise ratio degradation due to excess loop delay can be significantly reduced. As shown in Figure 4.1, the

feedback signal is applied after a delay time, t_d, during which the feedback signal is zero. This delay should be sufficiently large to allow fore a complete settling of the quantizer output [7].

4.1.2. Rise and Fall Time Asymmetry

When DAC output current pulses, having unequal rise and fall times, are integrated, the result of the integration depends on the DATA sequence. This DATA dependency produces harmonic distortion [6].

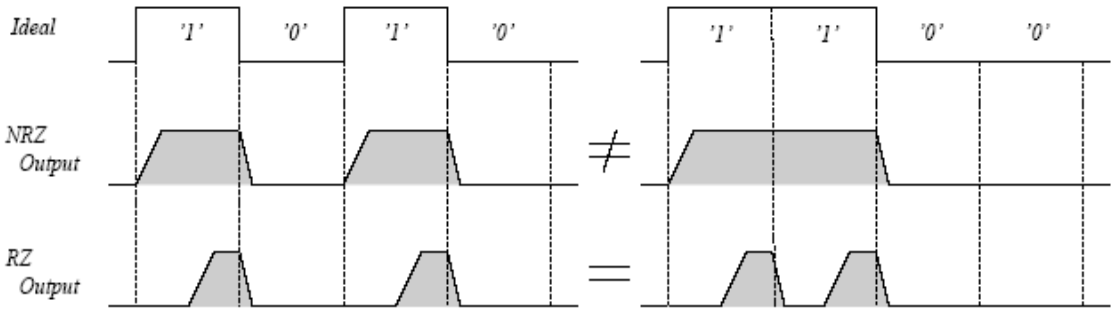

Figure 4.2. Rise and fall time asymmetry

As shown in Figure 4.2, the effect of this feedback waveform asymmetry can be highly attenuated by using a RZ feedback signal [16].

4.2. Return-to-Zero Feedback DAC Circuit

In the following, we will describe a RZ feedback DAC circuit with $t_d = \frac{T}{4}$ and $\tau = \frac{3T}{4}$. Special care was taken in the implementation of the digital control signal, in order to improve the switching characteristics of the DAC.

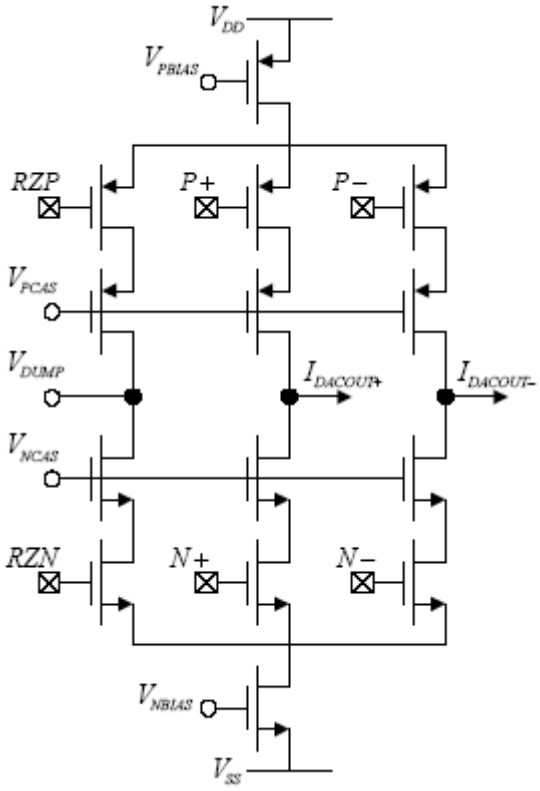

Figure 4.3. DAC circuit

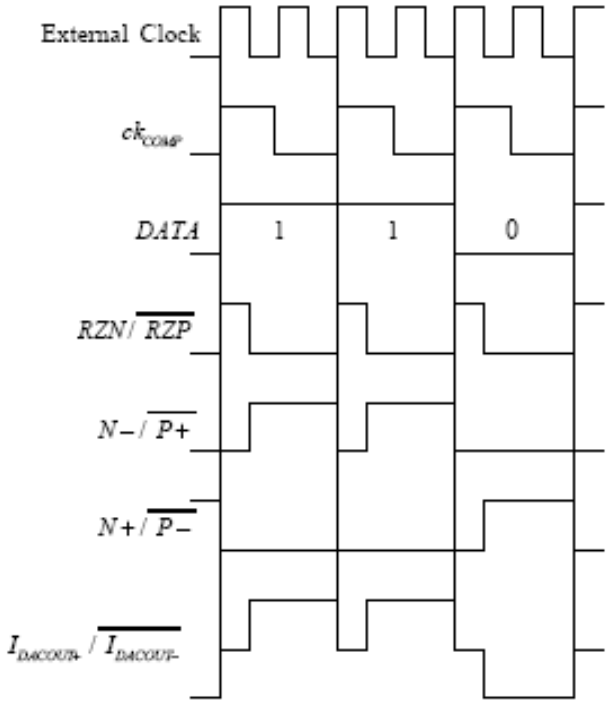

Figure 4.4. DAC control signals

Figure 4.3 and Figure 4.4 show the DAC circuit and the corresponding control signals respectively. An external clock frequency equal to twice the sampling frequency is required in order to get a $\frac{T}{4}$ RZ phase at the beginning of each cycle. The output current is directed either to $I_{DACOUT+}$ or $I_{DACOUT-}$ depending on the comparator output DATA.

During RZ phase, the positive and negative current sources are connected together through the DUMP node. In addition to reducing errors due to comparator delay and DAC output waveform asymmetry, connecting the current sources to the DUMP node at the beginning of each cycle has 2 other important features:

- The switching sequence is DATA independent. This renders charge injection DATA independent and then no harmonic distortion is produced.
- The drain of the current source transistor is always charged to the same potential before the new data signal connects the current source to one of the outputs. This reduces the error current due to residual charges on this node from the previous output connections.

The purpose of cascoding the switch transistor is to:

- reduce the capacitance seen by the output node (the input of the integrator). This reduces error current due to charging of the drain of the current source transistor to the potential of the output node.
- prevent any voltage variations at the output from reaching the drain of the current source transistor.
- increase the output resistance of the current source.
- prevent glitches that occur during switching from reaching the output through C_{gd} of the switch transistor [17].

Current source transistors must always keep constant current flow. If the switching transistors are simultaneously turned OFF, the current transistor drain rapidly discharges and will need much time to recharge [7].

To ensure that the current from the current source can flow to either one of the outputs, the signals controlling the NMOS switches (RZN, N+, and N-) have a high crossing point. In the same way, the PMOS switches control signals (RZP, P+ and P-) have a low crossing point. A timing diagram of the switching control signals is illustrated in Figure 4.5.

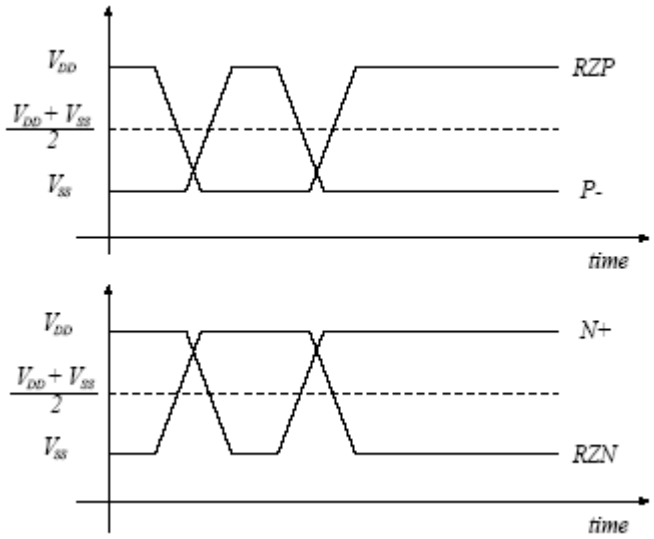

Figure 4.5. Timing diagram of high crossing NMOS-switch control signals and low crossing PMOS switch control signals

5. CIRCUIT SIMULATIONS AND RESULTS

5.1. Current-Mode Integrator

Figure 5.1 shows the fully differential current-mode integrator. Operating at an oversampling ratio of 250, the quantization noise power of the modulator is sufficiently low to be masked by the circuit noise. Based on the thermal noise calculations, the biasing current of the first integrator is calculated such that the signal-to-thermal-noise ratio is 80db.

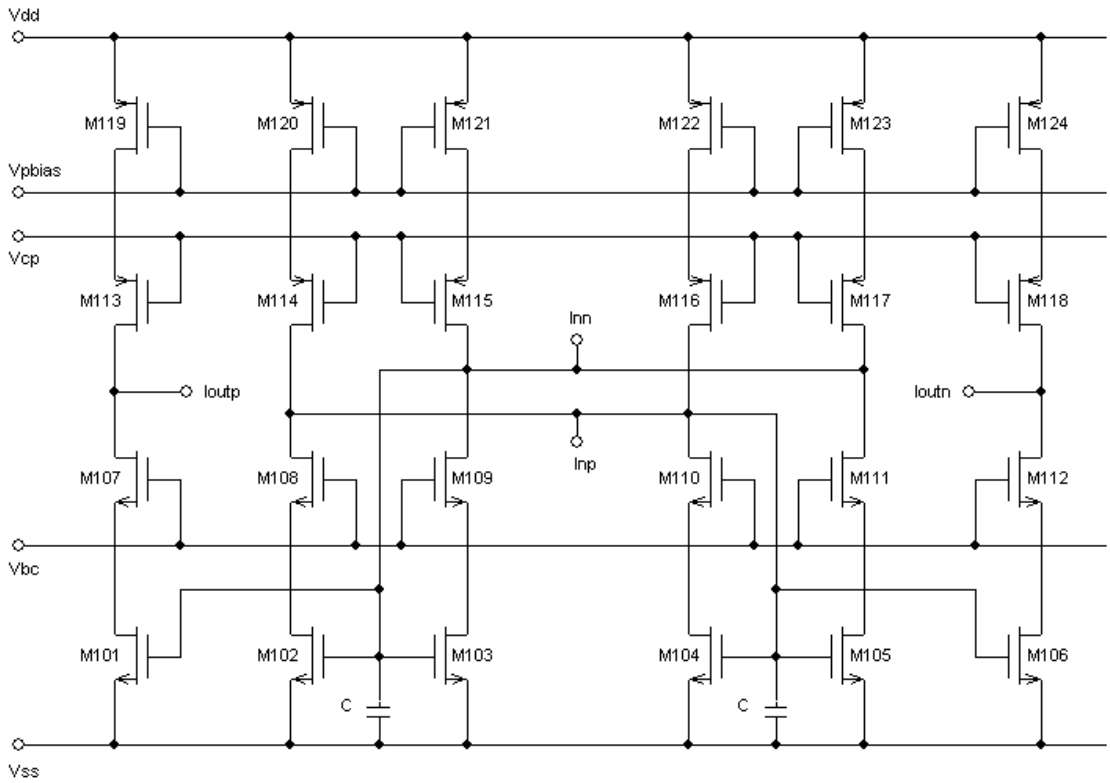

Figure 5.1. Differential current mode integrator circuit

We have calculated the integrating capacitance C = 7.0 pF and I_0 about 30 μA's for input specifications of SNR = 80dB, OSR =250, A_{int}=1.2, input bandwidth f_B = 40 kHz and

f_S=20 MHz at T=300K.

Cascode biasing voltages V_{CP} and V_{BC} are calculated for maximum modulation index of the current mirror. In this design, a modulation index of 0.8 is achieved.

Figure 4.2 shows the transient simulation of the integrator with 40kHZ sinusoidal differential current input signal.

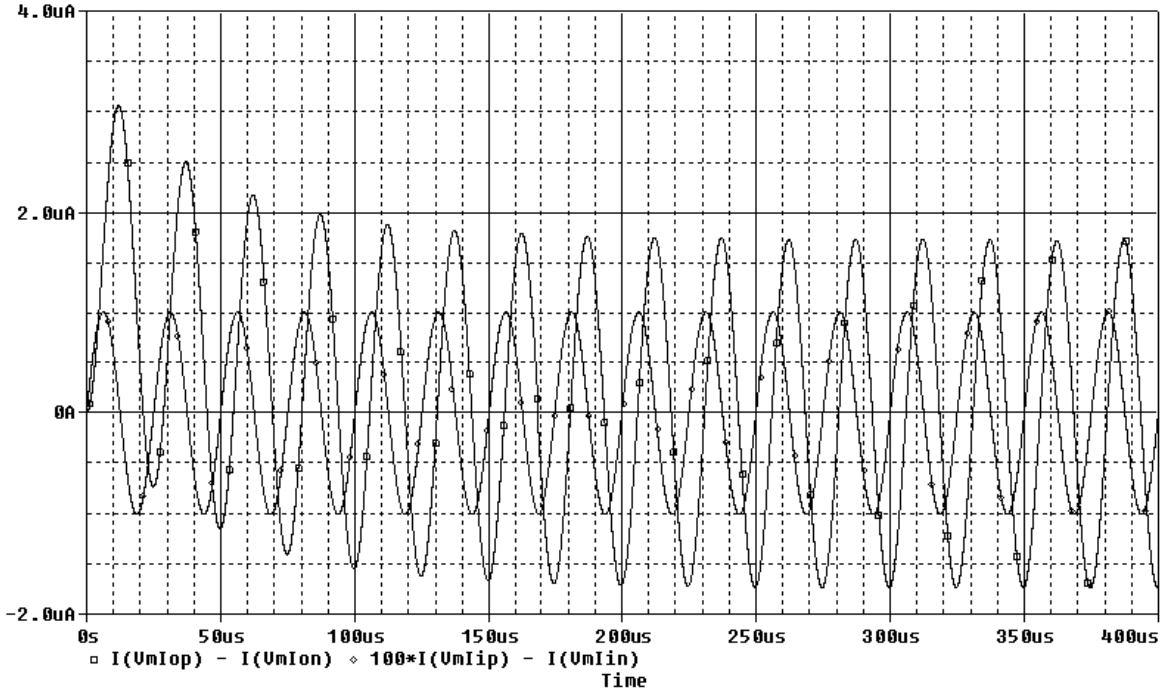

Figure 5.2. Time domain response of the current-mode integrator

Notice from the Figure 5.3 that, the output signal follows the input sinusoidal signal with 90 degrees of phase delay indicating the integrator action.

Figure 5.4 shows the AC simulation result of the integrator. It has a 56,8dB of DC gain and a cut-off frequency of 3.5kHz. The integrator behaves as a first order low-pass filter up to nearly 100MHz resulting from the differential current-mode operation.

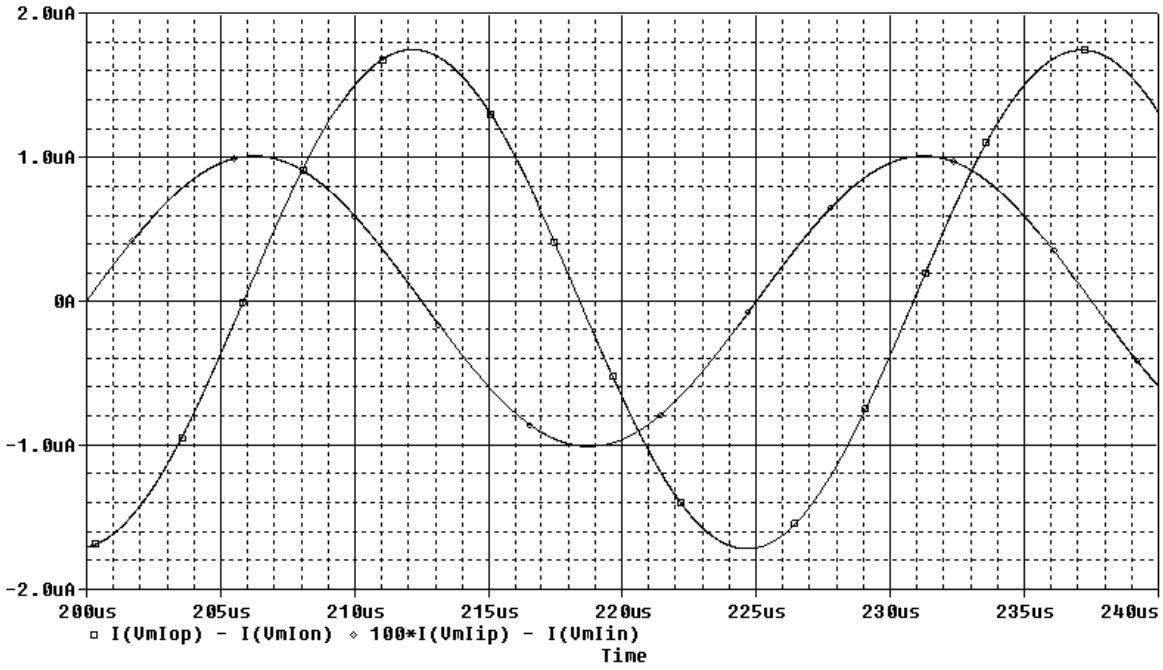

Figure 5.3. Differential input and output currents of the integrator versus time

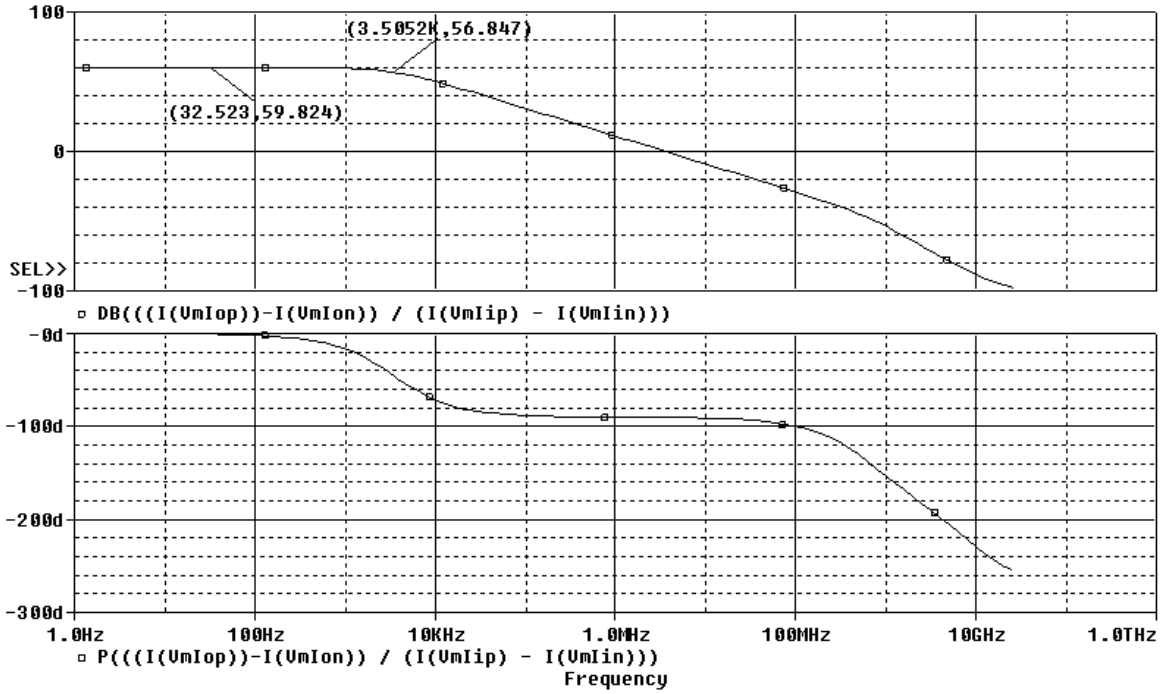

Figure 5.4. AC response of the integrator

5.2. Comparator

After designing the integrator, we have designed the comparator as our 1-bit ADC for quantizing the differential current-output of the integrator. The comparator has again a cascode structure like the integrator for the differential current input (biased at $I_o = 30\mu A$). Figure 5.5 shows the designed comparator circuit.

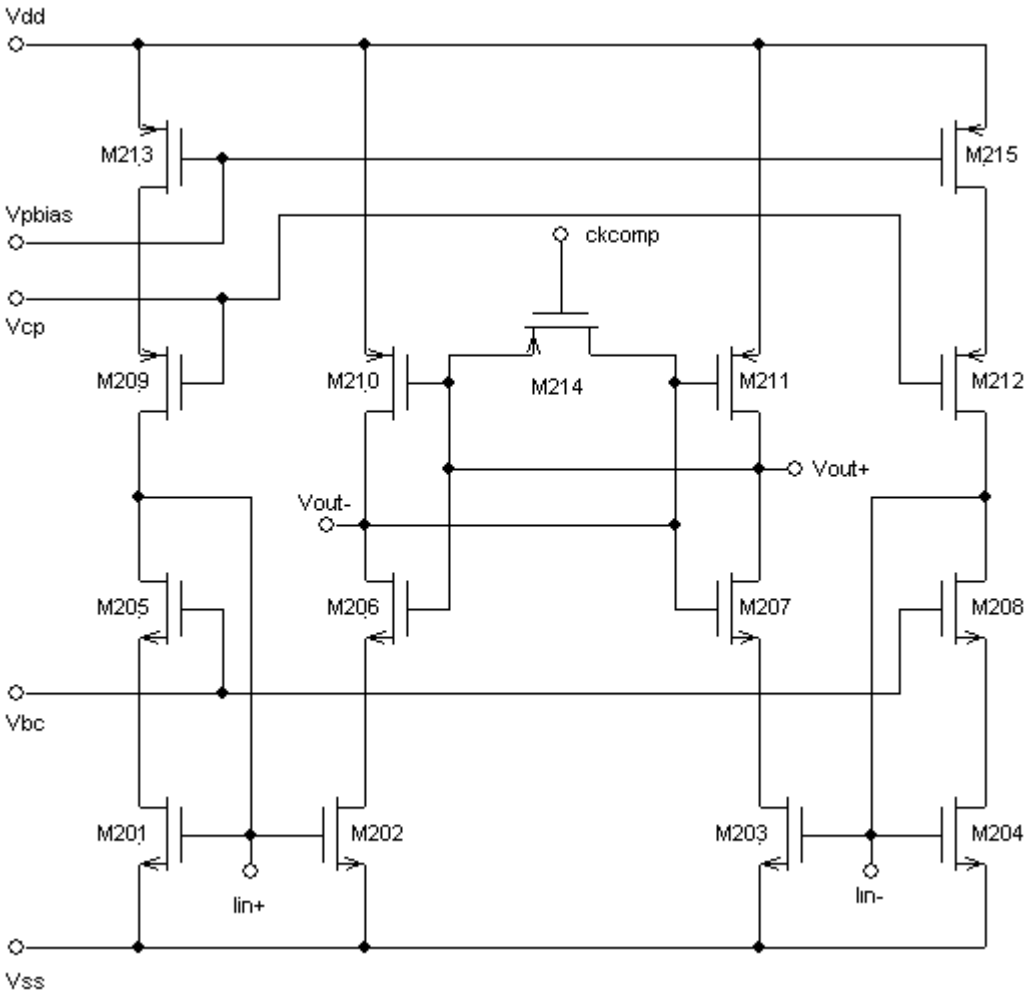

Figure 5.5. Differential current mode comparator

Figure 5.6 shows the transient simulation of the comparator showing the sinusoidal differential input current of 240kHz and the positive output-voltage (V_{o+}) of differential voltage output signal. As seen from the figure, the output voltage has three states:

- 0.9V (equal to $\frac{V_{DD}}{2} = 0.9V$) when the input-clock signal is at logic '0';
- 1.8V when the input-clock=logic '1' and the differential input-current is positive;
- 0V when the input-clock=logic '1' and the input differential current is negative.

So the comparator output corresponds to the binary equivalent of the input signal when the clock signal is at logic '1'. Actually the output of the comparator (and so the ΣΔ modulator) is a bipolar differential voltage signal.

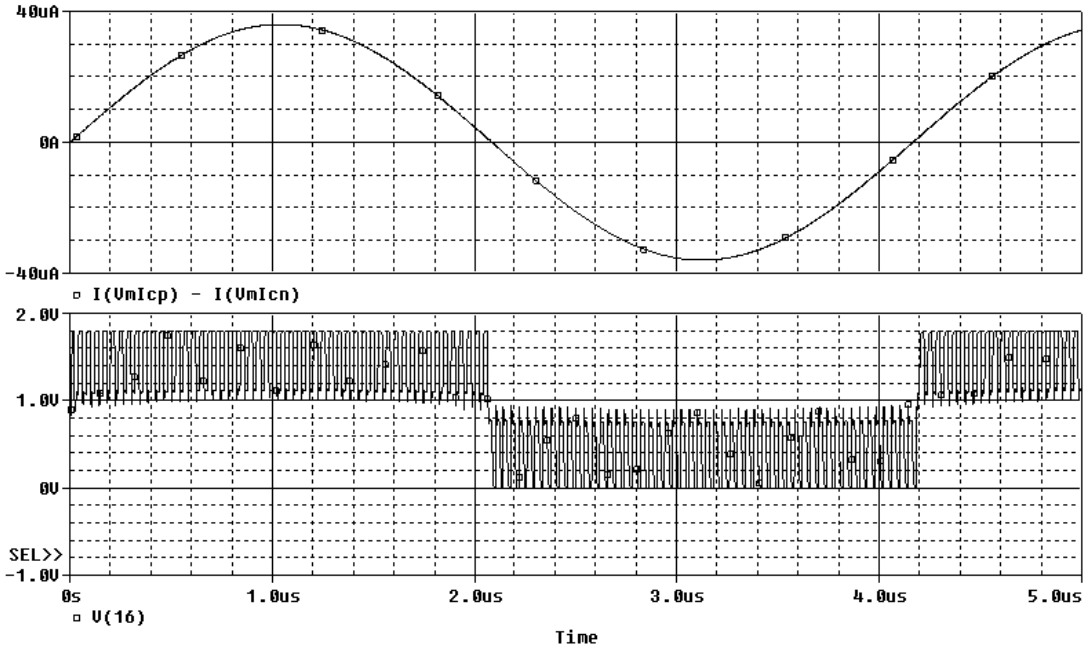

Figure 5.6. Time domain response of the differential current-mode comparator

Figure 5.7 shows the zoomed view of the zero-crossing of the comparator for the positive input current rising above 0A and the negative input current falling below 0A. The positive output voltage changes its transitions at the zero-crossing.

Figure 5.8 shows the zoomed view of the zero-crossing of the comparator for the positive input current falling below 0A and the negative input current rising above 0A. The positive output voltage again changes its transitions at the zero-crossing. It is clear from both of the figures that the comparator can perform 1-bit A/D conversion of input differential current signals of 240kHz bandwidth at a sampling frequency of 25MHz.

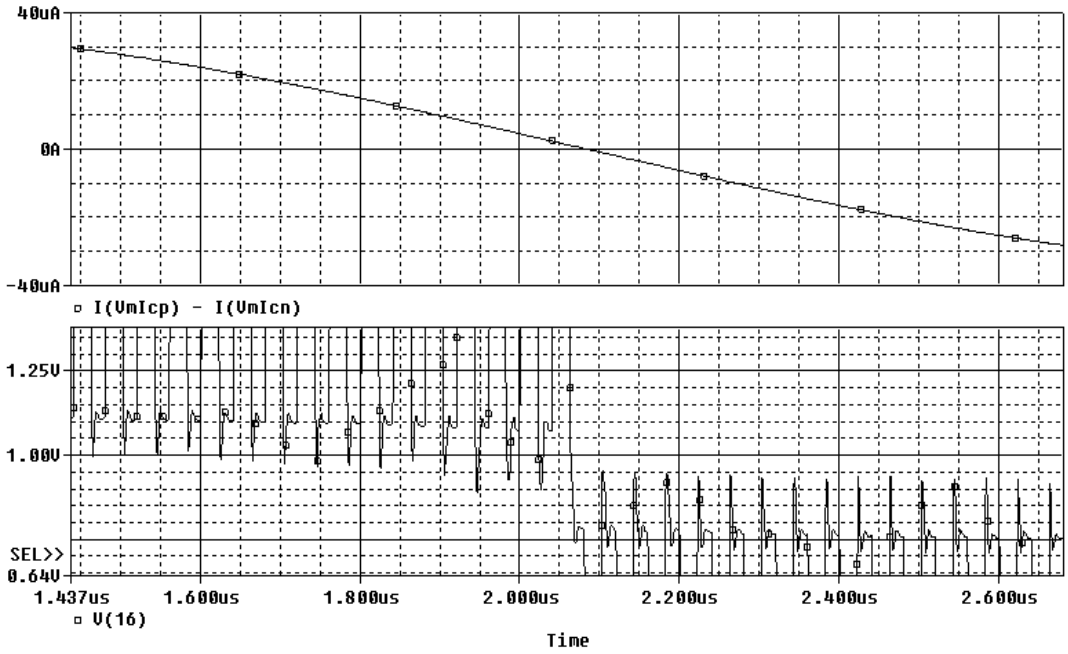

Figure 5.7. Positive zero transition of the comparator

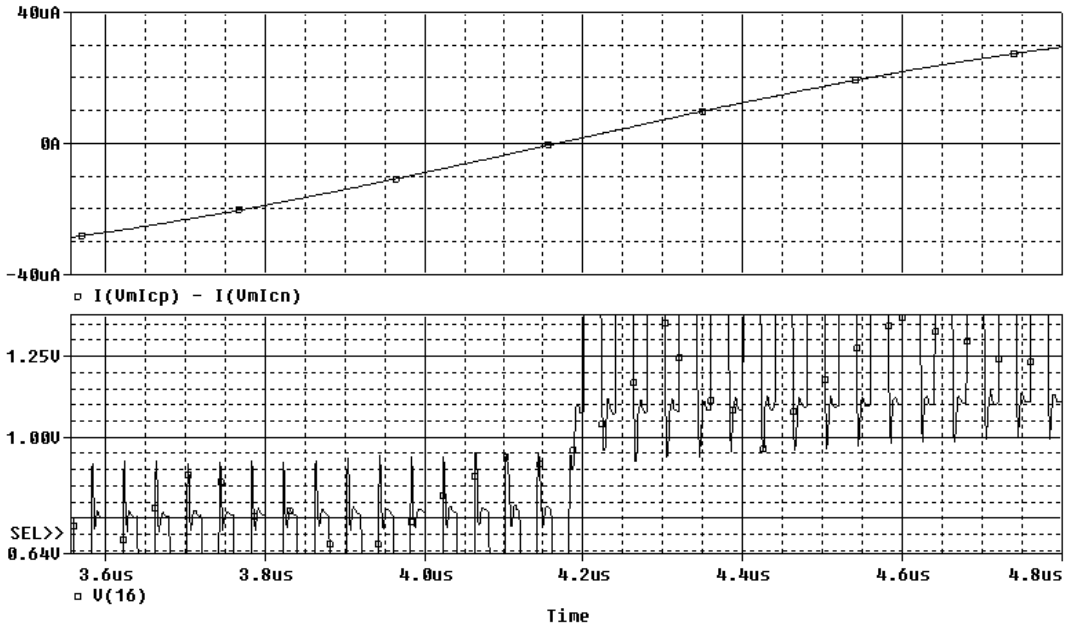

Figure 5.8. Negative zero transition of the comparator

5.3. DAC

After the comparator design, we have designed the feedback circuit: 1-bit RZ DAC and its control logic circuitry. Again we have used the 1-bit RZ DAC circuit given in [7] as

our model and for the purpose of SPICE simulation, we have designed a simpler control logic circuit needed for processing the differential voltage-output of the comparator. Our 1-bit RZ DAC and its control logic circuitry are given below in Figures 5.9 and 5.10.

The control circuit provides the necessary six logic signals for operating the 1-bit RZ DAC which has a biasing current of $\frac{I_o}{2} = 15\mu A$. The PMOS transistor M_{314} and the NMOS transistor M_{301} are always on and conduct this biasing current. During the return-to-zero phase (i.e., while the I_{outp} and I_{outn} are both zero) these transistors are kept on through the M_{311}, M_{308}, M_{305} and M_{302} transistors. After the RZ-phase, according to the input voltage, only the PMOS transistors or the NMOS transistors supply the current of one differential output signal. If the PMOS transistors (M_{312} and M_{309}) are on for supplying the current of I_{outp} (i.e., when the input voltage is logic '1'), then the NMOS transistors (M_{307} and M_{304}) are on for sinking the current of I_{outn} . So the magnitude of the output currents of the 1-bit RZ-DAC ($|I_{outp}|= |I_{outn}|$) are 15 μ A.

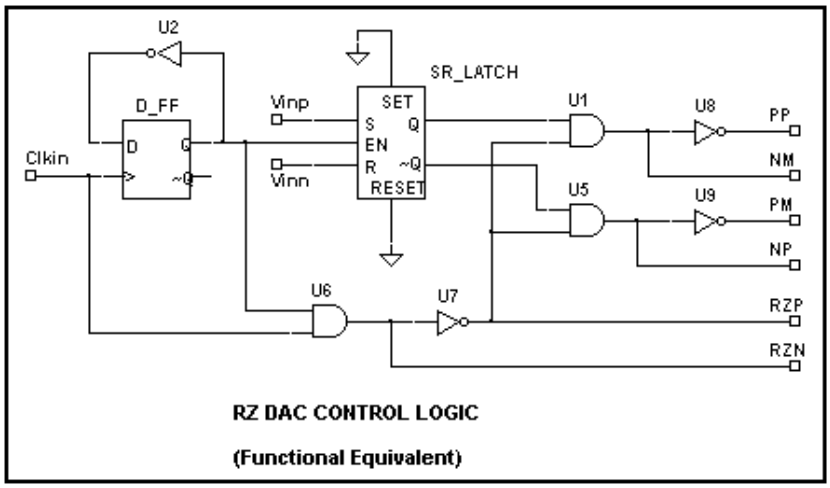

Figure 5.9. Differential current-mode 1-bit RZ DAC Control Logic Circuit

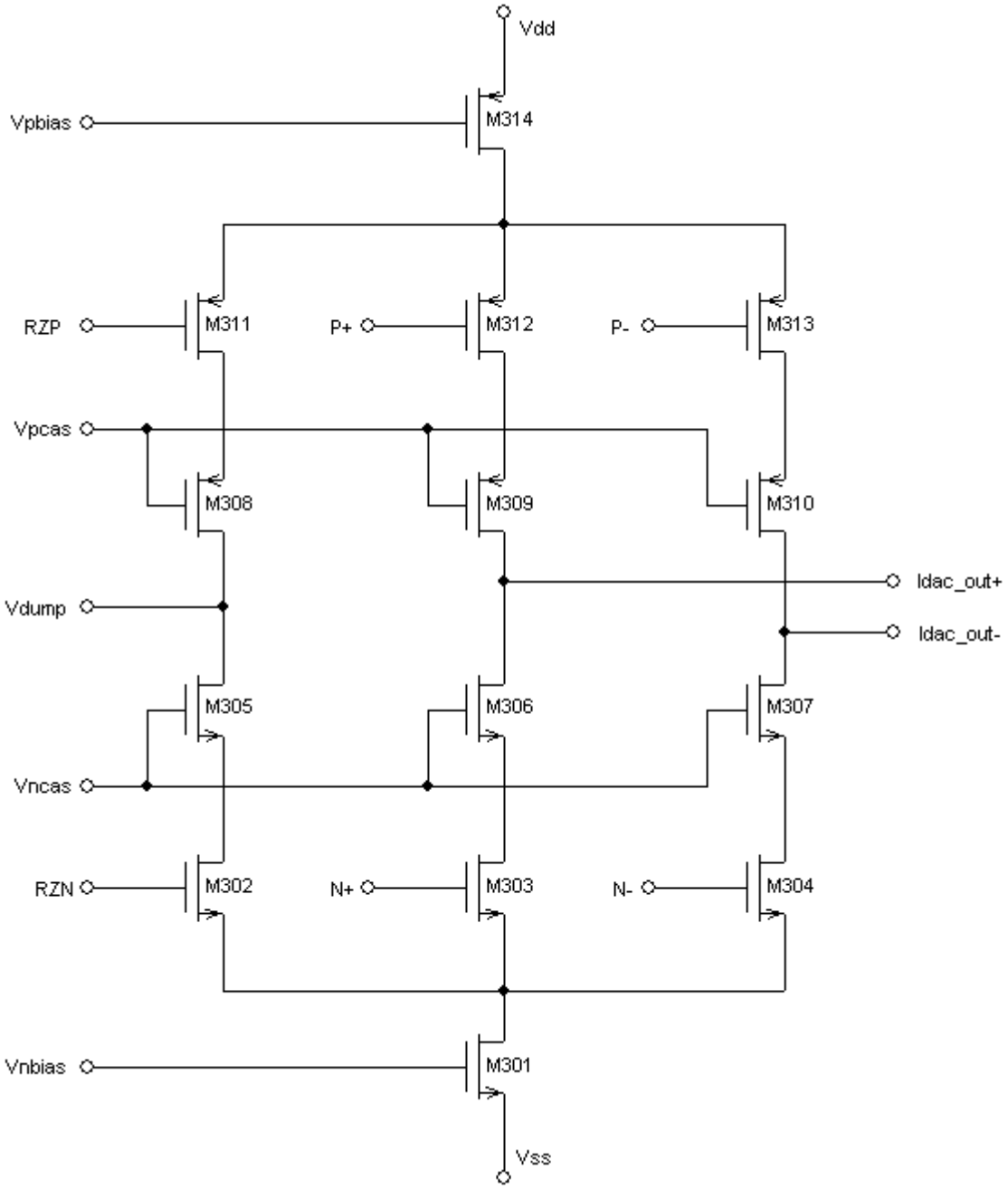

Figure 5.10. Differential current-mode 1-bit RZ DAC

Figure 5.11 shows the transient simulation result of the 1-Bit RZ-DAC for a square wave input signal (the latch-output of the RZ control logic circuitry is shown as the processed version of the differential voltage output of the comparator) of 20MHz clock frequency. As seen from the figure, for logic '1' inputs, the output of the DAC becomes positive and for logic'0' inputs the output of the DAC becomes negative. Also the output current returns to zero at the beginning of every clock cycle.

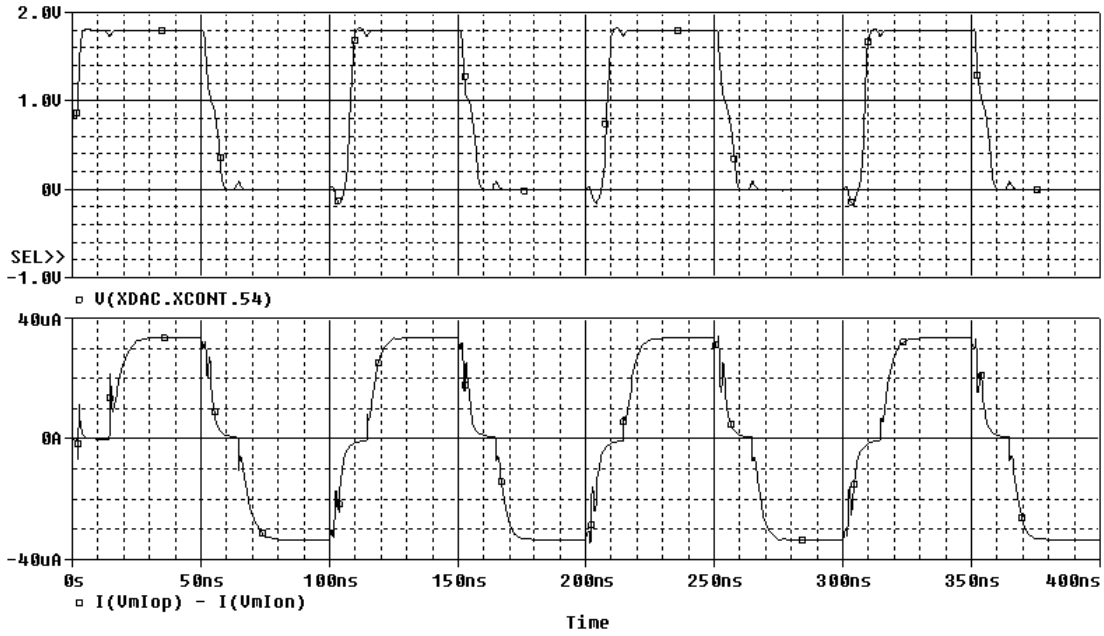

Figure 5.11. Time domain response of the differential current-mode 1-bit RZ DAC

In Figure 5.12, control logic signals generated by the RZ DAC Control circuitry are seen.

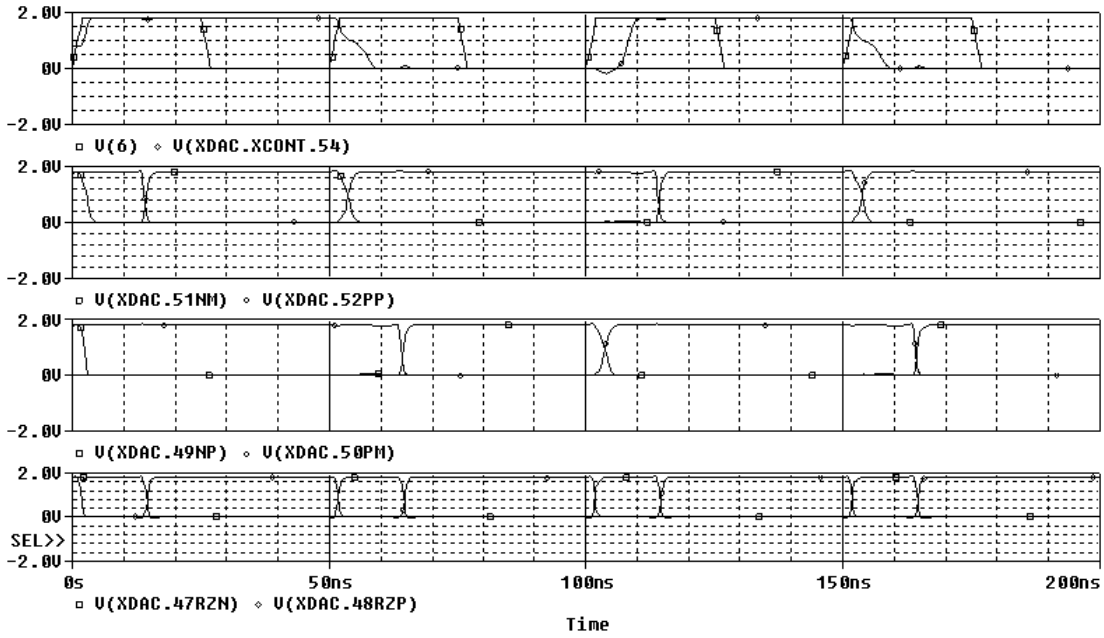

Figure 5.12. RZ DAC control circuitry signals

5.4. CT Current-Mode 1st Order ΣΔ Modulator Top-Level

After designing all the sub-blocks, we have connected them in SPICE using subcircuits. The final SPICE netlist of our CT current-mode 1st order ΣΔ Modulator is given in Appendix-D.

Transient simulation results of the final circuit can be seen in Figure 5.13. A differential sinusoidal current signal of 40kHz and amplitude $|I_{inp}| = |I_{inn}| = 10\mu A$ is applied to the input of the circuit and the circuit samples this signal with a clock frequency of 20.0 MHz. The 1-bit output signal oscillates very rapidly when the input signal magnitude is close to zero. For positive values of the input signal, the logic '1' state appears more than logic '0' state; and for negative values of the input signal, the logic '0' state appears more than logic '1' state. For the positive and negative peak values of the input signal, the output signal almost stops oscillating and stays at logic '1' and logic '0' states respectively.

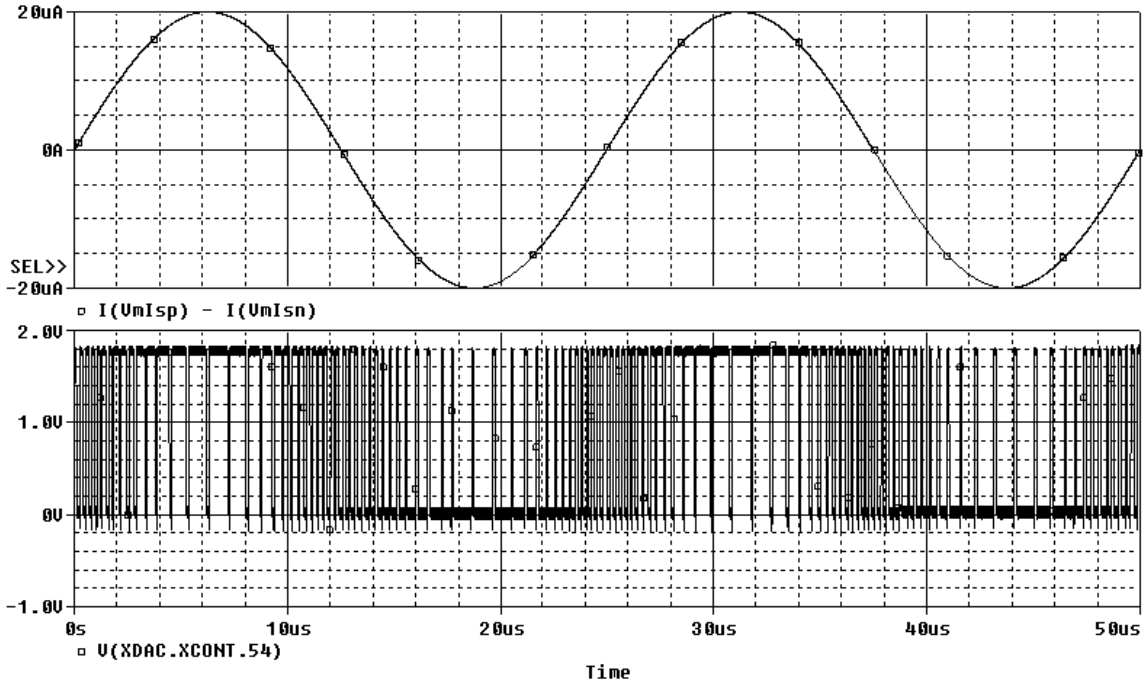

Figure 5.13. Time domain response of CT current-mode ΣΔ converter circuit.

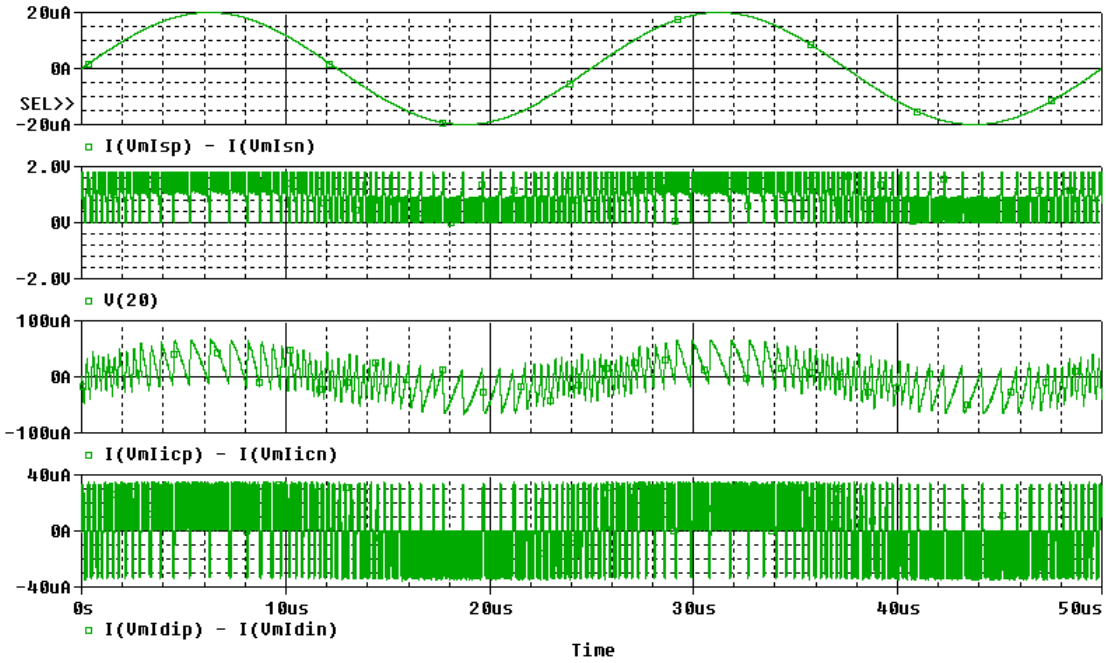

Figure 5.14. Input, output and internal signals for our designed ΣΔ converter

Figure 5.14 shows the internal differential signals of the CT current-mode 1st order ΣΔ Modulator simulation for the same 40kHz input signal: the integrator, the comparator and the DAC output signals. *V(20)* corresponds to the positive output voltage of the comparator (and of the modulator), *I(VmIcp)-I(VmIcn)* corresponds to the integrator output current and *I(VmIdp)-I(VmIdn)* corresponds to the DAC output current in the Figure 5.14.

5.5. Figure of Merit and SNR Results

Like the Nyquist-rate converters, performances of ΣΔ ADCs are evaluated with several parameters which all finally can be combined into a formula called the "*Figure Of Merit, (FOM)*" indicating the efficiency of the conversion. We use the *FOM* formula given below. It is expected that minimizing the *FOM*, increases the quality of the design.

$$\text{FOM} = \frac{(\text{Power Consumption x } 10^{12})}{(\text{Output - rate x } 2^{N})} \quad \text{(pJ)} \qquad (5.1)$$

Our design, 1st order CT current-mode ΣΔ modulator consumes 0.6mW power and

has an output rate of $2f_B$ = 80kHz with a resolution of N=12 bits corresponding to the SNR of 74dB. So we calculate the figure of merit of our design as 0.92pJ. For the purpose of comparison the following table will be useful.

Table 5.1. Figure of Merits for various ΣΔ implementations

Reference	SNR (db)	BW (kHz)	f_S (MHz)	V_{DD} V	Power (mW)	Area (mm^2)	CMOS Process	Architecture	FOM (pJ)
Our design	74	40	20	1.8	0.6	-	0.35μm	1-bit,1st order	0.92
[7]	79	100	26	1.8	5	1.56	0.18μm	3rd order Gm-C	2.7
[18]	82	100	13	2.5	1.8	0.2	0.35μm	4th order RC, Gm-C	0.7
[19]	93	160	20.48	5.0	65	1.6	1.2μm	2-1 MASH SC	4.4
[20]	66	100	13	2.7	2.0	0.18	0.5μm	2nd order SC	4.9
[21]	58	192	6	1.0	1.56	2.5	0.5μm	2nd order SC	5.0
[22]	90	100	3.25	5.0	40.0	2.0	1.2μm	2-2-2 MASH SC	6.1
[23]	79	100	5	2.7	14.8	5.4	0.6μm	3-bit, 2nd order	8.0
[24]	91	80	10.24	5.0	76.0	3.0	1.5μm	1-1-1 MASH SC	13
[25]	54	72	20	5.0	3.0	0.9	2.0μm	1st order Gm-C	40
[26]	68	100	13	5.0	94.0	-	0.8μm	7th order SC	182

Also computed Power Spectral Density plot are given for 20kHz and 40kHz input signals are given below.

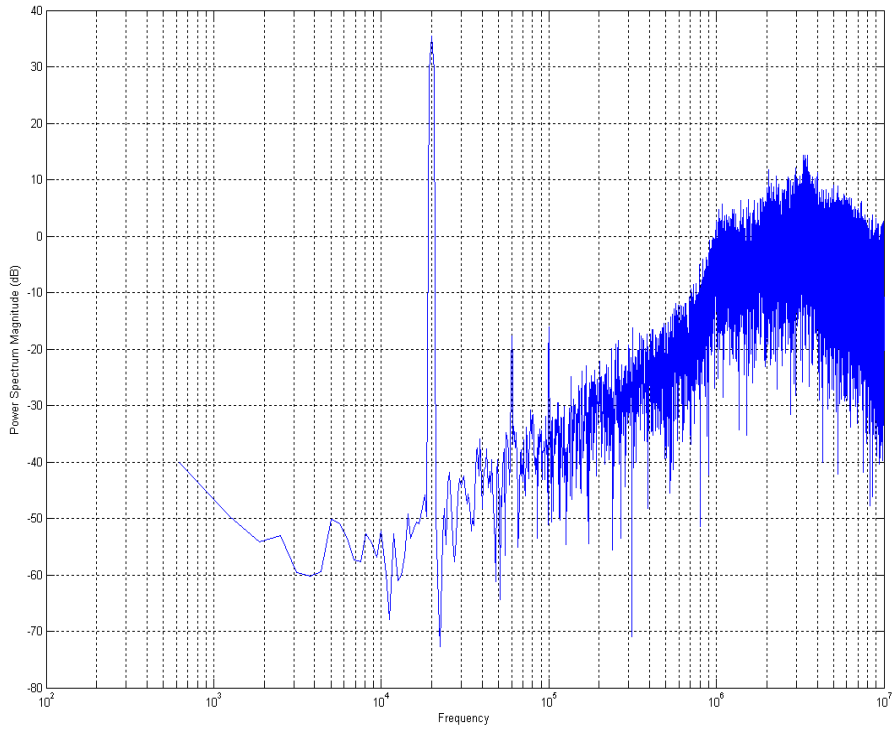

Figure 5.15. Computed Power Spectral Density for 20Khz input signal

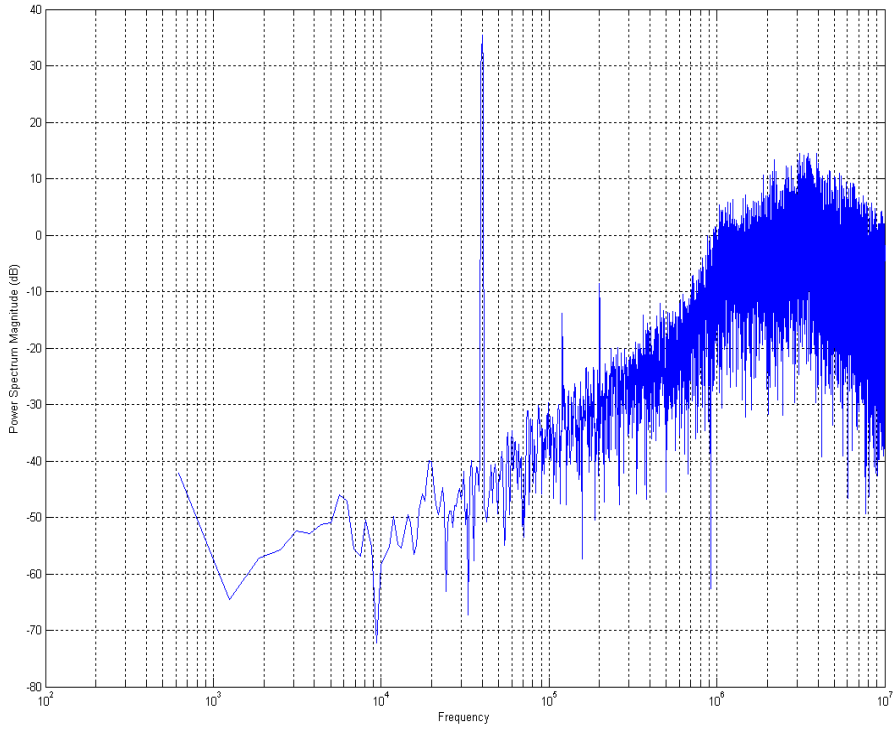

Figure 5.16. Computed Power Spectral Density for 40Khz input signal

6. CONCLUSION AND FUTURE WORK

ΣΔ A/D converters constitute a very interesting and also a very complex subject. It depends on a wide span of notions from nearly every branch of electronics and telecommunications. In this thesis, we have designed a continuous time current-mode sigma-delta A/D converter. In addition to literature search on the subject, we have designed a sample 1st order CT Current-mode ΣΔ modulator. The SPICE simulation results show that the circuit is working and the figure of merit calculation indicates a successful design.

The circuit we have designed, is not a fully current-mode ΣΔ modulator; its output is a voltage-mode differential signal. As a future work; we have to design the comparator and the 1-bit DAC circuits in fully current-mode in order to obtain a real current-mode ΣΔ modulator. Also for achieving higher resolution at lower sampling frequencies, we may design multi-bit and higher order versions of CT current-mode ΣΔ modulators using our readily available 1st order circuit.

APPENDIX A: SPICE CODE FOR TRANSIENT AND AC ANALYSIS OF THE INTEGRATOR

```
*Continuous Time Current-Mode Differential Integrator ( Cint = 7 pF )

******Reference Voltages Beginning
Vdd 1 0 dc 1.8
Vpbias 5 0 dc 0.8
Vnbias 2 0 dc 0.9
Vcp 4 0 dc 0.43
Vbc 3 0 dc 1.2006
******Reference Voltages End

******Integrator Stimulus Beginning
Iip 110 0 sin(0 -0.01u 40k)
Iin 60 0 sin(0 0.01u 40k)

VmIip 110 11
VmIin 60 6

Vop 201 0 dc 0.9
Von 202 0 dc 0.9
VmIop 10 201
VmIon 18 202

Iip 110 0 ac 1
Iin 60 0 ac 1 180
******Integrator Stimulus End

Xint 1 3 4 5 6 11 18 10 INTEGRATOR

.subckt INTEGRATOR 1 3 4 5 6 11 18 10

*1=VDD 3=Vbc 4=Vcp 5=Vpbias 6=Iin- 11=Iin+
*10=Iout+ 18=Iout-

M101 7 6 0 0 MODN W=7U L=2U AD=14P AS=14P PD=18U PS=18U
M102 8 6 0 0 MODN W=7U L=2U AD=14P AS=14P PD=18U PS=18U
M103 9 6 0 0 MODN W=7U L=2U AD=14P AS=14P PD=18U PS=18U
M107 10 3 7 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U
M108 11 3 8 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U
M109 6 3 9 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U

M113 10 4 12 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U
M114 11 4 13 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U
M115 6 4 14 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U
M119 12 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U
M120 13 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U
M121 14 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U

c1 6 0 7pf

M104 15 11 0 0 MODN W=7U L=2U AD=14P AS=14P PD=18U PS=18U
M105 16 11 0 0 MODN W=7U L=2U AD=14P AS=14P PD=18U PS=18U
```

```
M106 17 11 0 0 MODN W=7U L=2U AD=14P AS=14P PD=18U PS=18U
M110 11 3 15 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U
M111 6 3 16 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U
M112 18 3 17 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U

M116 11 4 19 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U
M117 6 4 20 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U
M118 18 4 21 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U
M122 19 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U
M123 20 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U
M124 21 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U

c2 11 0 7pf

.ends INTEGRATOR

**********Current Mode Integrator End


.include mos35u.cir

.op

.tran 1n 400u 0n 10n

.ac dec 10 1 20e9

.PROBE

.END
```

APPENDIX B: SPICE CODE FOR TRANSIENT ANALYSIS OF THE COMPARATOR

```
*Current-Mode Differential Comparator ( fs = 20 MHz , fin = 200 KHz )


******Reference Voltages Beginning
Vdd 1 0 dc 1.8
Vpbias 5 0 dc 0.8
Vnbias 2 0 dc 0.8752
Vcp 4 0 dc 0.43
Vbc 3 0 dc 1.2006
******Reference Voltages End


******Comparator Stimulus Beginning
Vclk 15 0 pulse(0 1.8 0ns 2ns 2ns 18ns 40ns)

Icp 110 0 sin(0 -0.000018 240KHz)
Icn 60 0 sin(0 0.000018 240KHz)

VmIcp 110 11
VmIcn 60 6
******Comparator Stimulus End

XComp 1 3 4 5 15 6 11 10 16 COMPARATOR

**********Current-Comparator Beginning

.subckt COMPARATOR 1 3 4 5 15 6 11 10 16

*1=VDD 3=Vbc 4=Vcp 5=Vpbias 15=Clk
*6=Iin- 11=Iin+ 10=Vout- 16=Vout+

M201 12 11 0 0 MODN  W=7U L=2U AD=14P AS=14P PD=18U PS=18U
M202 14 11 0 0 MODN W=3.5U L=2U AD=7P  AS=7P PD=11U PS=11U
M203 8 6 0 0 MODN W=3.5U L=2U AD=7P  AS=7P PD=11U PS=11U
M204 7 6 0 0 MODN W=7U L=2U AD=14P AS=14P PD=18U PS=18U
M205 11 3 12 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U
*Latch transistors****
M206 10 16 14 0 MODN W=9U L=1U AD=9P  AS=9P PD=20U PS=20U
M207 16 10 8 0 MODN W=9U L=1U AD=9P  AS=9P PD=20U PS=20U
******

M208 6 3 7 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U
M209 11 4 13 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U

*Latch transistors****
M210 10 16 1 1 MODP W=12U L=1U AD=12P AS=12P PD=26U PS=26U
M211 16 10 1 1 MODP W=12U L=1U AD=12P AS=12P PD=26U PS=26U
*****

M212 6 4 9 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U
M213 13 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U
```

```
M214 10 15 16 1 MODP W=16U L=1U AD=16P  AS=16P PD=34U PS=34U
M215 9 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U
.ends COMPARATOR
********* Current-Comparator End

.inc mos35u.cir
.tran 1n 5u 0n 10n
.PROBE
.END
```

APPENDIX C: SPICE CODE FOR TRANSIENT ANALYSIS OF THE DAC AND ITS CONTROL CIRCUITRY

```
*Continuous Time Current-Mode Differential RZ D/A CONVERTER (fclk = 20 MHz)


******Reference Voltages Beginning
Vdd 1 0 dc 1.8
Vpbias 5 0 dc 0.8
Vnbias 2 0 dc 0.8752
Vcp 4 0 dc 0.43
Vbc 3 0 dc 1.2006
******Reference Voltages End

******Clocked SR Latch Stimulus Beginning

*Fsample = 20 MHz
Vckcompext 6 0 pulse(0 1.8 0ns 2ns 2ns 23ns 50ns)
Vrznext  7 0 pulse(0 1.8 0 2ns 2ns 10.5ns 50ns)
Vrzpext  8 0 pulse(0 1.8 12.5ns 2ns 2ns 35.5ns 50ns)


Vs 20 0 pulse(0 1.8 0 2ns 2ns 48ns 100ns)

Vr 19 0 pulse(0 1.8 50ns 2ns 2ns 48ns 100ns)


Vopdac 302 0 dc 0.9
Vondac 301 0 dc 0.9

VmIop 22 301
VmIon 21 302

******Clocked SR Latch Stimulus End

XDAC 1 2 3 4 5 6 7 8 19 20 21 22 DAC_toplevel


**********RZ DA Converter Beginning

.subckt RZDAC 1 2 3 4 5 6 7 8 9 10 11 17 18

*1=VDD 2=Vnbias 3=Vncas 4=Vpcas 5=Vpbias
*6=RZN 7=RZP 8 =N+ 9=P+ 10=N- 11=P- 17=Iout+ 18=Iout-

M301 12 2 0 0   MODN W=4U L=2U AD=8P AS=8P PD=12U PS=12U
M302 13 6 12 0  MODN W=16U L=1U AD=16P AS=16P PD=34U PS=34U
M303 14 8 12 0  MODN W=16U L=1U AD=16P AS=16P PD=34U PS=34U
M304 15 10 12 0 MODN W=16U L=1U AD=16P AS=16P PD=34U PS=34U
M305 16 3 13 0  MODN W=16U L=1U AD=16P AS=16P PD=34U PS=34U
M306 17 3 14 0  MODN W=16U L=1U AD=16P AS=16P PD=34U PS=34U
M307 18 3 15 0  MODN W=16U L=1U AD=16P AS=16P PD=34U PS=34U
```

```
M308 16 4 19 1  MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
M309 17 4 20 1  MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
M310 18 4 21 1  MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
M311 19 7 22 1  MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
M312 20 9 22 1  MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
M313 21 11 22 1 MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
M314 22 5 1 1   MODP W=16U L=2U AD=32P AS=32P PD=36U PS=36U



.ends RZDAC
**********RZ DA Converter End


**********Clocked SR Latch Beginning

.subckt SRLATCH 1 2 3 4 6 7
*1=VDD 2=Clk 3=S 4=R 6=QB 7=Q

M401 5 3 0 0 MODN W=5U L=1U AD=5P AS=5P PD=12U PS=12U
M402 6 7 0 0 MODN W=3U L=1U AD=3P AS=3P PD=5U PS=5U
M403 7 6 0 0 MODN W=3U L=1U AD=3P AS=3P PD=5U PS=5U
M404 8 4 0 0 MODN W=5U L=1U AD=5P AS=5P PD=12U PS=12U

M405 6 2 5 0 MODN W=5U L=1U AD=5P AS=5P PD=12U PS=12U
M406 6 7 1 1 MODP W=8U L=1U AD=8P AS=8P PD=18U PS=18U
M407 7 6 1 1 MODP W=8U L=1U AD=8P AS=8P PD=18U PS=18U
M408 7 2 8 0 MODN W=5U L=1U AD=5P AS=5P PD=12U PS=12U
.ends SRLATCH

**********Clocked SR Latch End


**********Nand2 Gate Beginning
.subckt NAND2 1 2 3 4

*1=VDD 2=in0 3=in1 4=Nand2_out

M409 5 2 0 0 MODN W=8U L=1U AD=8P AS=8P PD=18U PS=18U
M410 4 3 5 0 MODN W=8U L=1U AD=8P AS=8P PD=18U PS=18U
M411 4 3 1 1 MODP W=4U L=1U AD=4P AS=4P PD=10U PS=10U
M412 4 2 1 1 MODP W=4U L=1U AD=4P AS=4P PD=10U PS=10U
.ends NAND2

**********Nand2 Gate End


**********Nor2 Gate Beginning
.subckt NOR2 1 2 3 4

*1=VDD 2=in0 3=in1 4=Nor2_out

M413 4 2 0 0 MODN W=2U L=1U AD=2P AS=2P PD=4U PS=4U
M414 4 3 0 0 MODN W=2U L=1U AD=2P AS=2P PD=4U PS=4U
M415 4 3 5 1 MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
M416 5 2 1 1 MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
.ends NOR2
```

```
**********Nor2 Gate End


**********Inverter Beginning

.subckt INVP 1 2 3
*1=VDD 2=inp 3=outp
M417 3 2 0 0 MODN W=2U L=1U AD=2P AS=2P PD=4U PS=4U
M418 3 2 1 1 MODP W=8U L=1U AD=8P AS=8P PD=18U PS=18U
.ends INVP
**********Inverter End

.subckt INVN 1 2 3
*1=VDD 2=inp 3=outp
M419 3 2 0 0 MODN W=3U L=1U AD=3P AS=3P PD=8U PS=8U
M420 3 2 1 1 MODP W=8U L=1U AD=8P AS=8P PD=18U PS=18U
.ends INVN

**********Inverter End


.subckt DACCONT 1 42 43 44 45 46 47 48 49 50 51 52

*1=VDD 42=Clk 43=Vin+ 44=Vin-
*45=RZN_ext 46=RZP_ext 47=RZN 48=RZP
*49=N+ 50=P- 51=N- 52=P+

X1 1 42 43 44 53 54 SRLATCH

*P-
XPM 1 46 53 50 NAND2


*P+
XPP 1 46 54 52 NAND2

*P- = node 50
*N+ = node 49
XNP 1 45 54 49 NOR2


*P+ = node 52
*N- = node 51

XNM 1 45 53 51 NOR2



*RZP = node 48
XRZP 1 45 48 INVN

*RZN = node 47
XRZN 1 46 47 INVP


.ends DACCONT
```

```
.subckt DAC_toplevel 1 2 3 4 5 6 7 8 9VM 10VP 11 12

*1=VDD 2=Vnbias 3=Vncas 4=Vpcas 5=Vpbias
*6=Clk 7=RZN_ext 8=RZP_ext
*9VM=Vin- 10VP=Vin+ 11=Iout- 12=Iout+

XCONT 1 6 10VP 9VM  7 8 47RZN 48RZP 49NP 50PM 51NM 52PP DACCONT

XRZDAC 1 2 3 4 5 47RZN 48RZP 49NP 52PP 51NM 50PM 12 11 RZDAC

.ends DAC_toplevel

.inc mos35u.cir
.tran 1n 0.90u 0n 10n

.PROBE

.END
```

APPENDIX D: SPICE NET LISTS OF THE ΣΔ MODULATOR

*Continuous Time Current-Mode Differential Sigma Delta A/D CONVERTER (fin=40KHz fs=20MHz OSR=250)

******Reference Voltages Beginning
Vdd 1 0 dc 1.8
Vpbias 5 0 dc 0.8
Vnbias 2 0 dc 0.8752
Vcp 4 0 dc 0.43
Vbc 3 0 dc 1.2006
******Reference Voltages End

********** Sigma Delta Stimulus Beginning

*Fsample = 100 KHz
*Vckcompext 6 0 pulse(0 1.8 0 2ns 2ns 4998ns 10us)
*Vrznext 7 0 pulse(0 1.8 0 2ns 2ns 2498ns 10us)
*Vrzpext 8 0 pulse(0 1.8 2.5us 2ns 2ns 7498ns 10us)

*Fsample = 500 KHz
*Vckcompext 6 0 pulse(0 1.8 0 2ns 2ns 998ns 2us)
*Vrznext 7 0 pulse(0 1.8 0 2ns 2ns 498ns 2us)
*Vrzpext 8 0 pulse(0 1.8 500ns 2ns 2ns 1498ns 2us)

*Fsample = 1 MHz
*Vckcompext 6 0 pulse(0 1.8 0 2ns 2ns 498ns 1us)
*Vrznext 7 0 pulse(0 1.8 0 2ns 2ns 248ns 1us)
*Vrzpext 8 0 pulse(0 1.8 250ns 2ns 2ns 748ns 1us)

*Fsample = 2 MHz
*Vckcompext 6 0 pulse(0 1.8 0 2ns 2ns 248ns 500ns)
*Vrznext 7 0 pulse(0 1.8 0 2ns 2ns 123ns 500ns)
*Vrzpext 8 0 pulse(0 1.8 125ns 2ns 2ns 373ns 500ns)

*Fsample = 10 MHz
*Vckcompext 6 0 pulse(0 1.8 0 2ns 2ns 48ns 100ns)
*Vrznext 7 0 pulse(0 1.8 0 2ns 2ns 23ns 100ns)
*Vrzpext 8 0 pulse(0 1.8 25ns 2ns 2ns 73ns 100ns)

*Fsample = 20 MHz
Vckcompext 6 0 pulse(0 1.8 0ns 2ns 2ns 23ns 50ns)
Vrznext 7 0 pulse(0 1.8 0 2ns 2ns 10.5ns 50ns)
Vrzpext 8 0 pulse(0 1.8 12.5ns 2ns 2ns 35.5ns 50ns)

***Current input to the integrator

Iin 9 0 sin(0 10u 40KHz)
Iip 10 0 sin(0 -10u 40KHz)

```
VmIsn 9 11
VmIsp 10 12

VmIin 11 13
VmIip 12 14

*********

****Integrator-comparator interface
VmIicn 15 17
VmIicp 16 18

****


****DAC-Integrator interface

VmIdin 21 12
VmIdip 22 11

***********Sigma Delta Stimulus End



XINT 1 3 4 5 13 14 15 16 INTEGRATOR
XCOMP 1 3 4 5 6 17 18 19 20 COMPARATOR
XDAC 1 2 3 4 5 6 7 8 19 20 21 22 DAC_toplevel




**********Current Mode Integrator Beginning

.subckt INTEGRATOR 1 3 4 5 6 11 18 10

*1=VDD 3=Vbc 4=Vcp 5=Vpbias 6=Iin- 11=Iin+
*10=Iout+ 18=Iout-

M101 7 6 0 0 MODN W=7U L=2U AD=14P AS=14P PD=18U PS=18U
M102 8 6 0 0 MODN W=7U L=2U AD=14P AS=14P PD=18U PS=18U
M103 9 6 0 0 MODN W=7U L=2U AD=14P AS=14P PD=18U PS=18U
M107 10 3 7 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U
M108 11 3 8 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U
M109 6 3 9 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U

M113 10 4 12 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U
M114 11 4 13 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U
M115 6 4 14 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U
M119 12 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U
M120 13 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U
M121 14 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U

c1 6 0 7pf


M104 15 11 0 0 MODN W=7U L=2U AD=14P AS=14P PD=18U PS=18U
```

```
M105 16 11 0 0 MODN W=7U L=2U AD=14P AS=14P PD=18U PS=18U
M106 17 11 0 0 MODN W=7U L=2U AD=14P AS=14P PD=18U PS=18U
M110 11 3 15 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U
M111 6 3 16 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U
M112 18 3 17 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U

M116 11 4 19 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U
M117 6 4 20 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U
M118 18 4 21 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U
M122 19 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U
M123 20 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U
M124 21 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U

c2 11 0 7pf

.ends INTEGRATOR

**********Current Mode Integrator End



**********Current-Comparator Beginning

.subckt COMPARATOR 1 3 4 5 15 6 11 10 16

*1=VDD 3=Vbc 4=Vcp 5=Vpbias 15=Clk
*6=Iin- 11=Iin+ 10=Vout- 16=Vout+

M201 12 11 0 0 MODN  W=7U L=2U AD=14P AS=14P PD=18U PS=18U
M202 14 11 0 0 MODN W=3.5U L=2U AD=7P  AS=7P PD=11U PS=11U
M203 8 6 0 0 MODN W=3.5U L=2U AD=7P  AS=7P PD=11U PS=11U
M204 7 6 0 0 MODN W=7U L=2U AD=14P AS=14P PD=18U PS=18U
M205 11 3 12 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U

*Latch transistors****
M206 10 16 14 0 MODN W=9U L=1U AD=9P  AS=9P PD=20U PS=20U
M207 16 10 8 0 MODN W=9U L=1U AD=9P  AS=9P PD=20U PS=20U
******

M208 6 3 7 0 MODN W=18U L=1U AD=18P AS=18P PD=38U PS=38U
M209 11 4 13 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U

*Latch transistors****
M210 10 16 1 1 MODP W=12U L=1U AD=12P AS=12P PD=26U PS=26U
M211 16 10 1 1 MODP W=12U L=1U AD=12P AS=12P PD=26U PS=26U
*****

M212 6 4 9 1 MODP W=24.1U L=1U AD=24.1P AS=24.1P PD=50.2U PS=50.2U
M213 13 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U
M214 10 15 16 1 MODP W=16U L=1U AD=16P  AS=16P PD=34U PS=34U
M215 9 5 1 1 MODP W=32U L=2U AD=64P AS=64P PD=68U PS=68U

.ends COMPARATOR


********* Current-Comparator End
```

```
**********RZ DA Converter Beginning

.subckt RZDAC 1 2 3 4 5 6 7 8 9 10 11 18 17

*1=VDD 2=Vnbias 3=Vncas 4=Vpcas 5=Vpbias
*6=RZN 7=RZP 8 =N+ 9=P+ 10=N- 11=P- 17=Iout+ 18=Iout-



M301 12 2 0 0   MODN W=4U L=2U AD=8P AS=8P PD=12U PS=12U
M302 13 6 12 0  MODN W=16U L=1U AD=16P AS=16P PD=34U PS=34U
M303 14 8 12 0  MODN W=16U L=1U AD=16P AS=16P PD=34U PS=34U
M304 15 10 12 0 MODN W=16U L=1U AD=16P AS=16P PD=34U PS=34U
M305 16 3 13 0  MODN W=16U L=1U AD=16P AS=16P PD=34U PS=34U
M306 17 3 14 0  MODN W=16U L=1U AD=16P AS=16P PD=34U PS=34U
M307 18 3 15 0  MODN W=16U L=1U AD=16P AS=16P PD=34U PS=34U


M308 16 4 19 1  MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
M309 17 4 20 1  MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
M310 18 4 21 1  MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
M311 19 7 22 1  MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
M312 20 9 22 1  MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
M313 21 11 22 1 MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
M314 22 5 1 1   MODP W=16U L=2U AD=32P AS=32P PD=36U PS=36U

.ends RZDAC
**********RZ DA Converter End



**********Clocked SR Latch Beginning

.subckt SRLATCH 1 2 3 4 6 7
*1=VDD 2=Clk 3=S 4=R 6=QB 7=Q

M401 5 3 0 0 MODN W=5U L=1U AD=5P AS=5P PD=12U PS=12U
M402 6 7 0 0 MODN W=3U L=1U AD=3P AS=3P PD=5U PS=5U
M403 7 6 0 0 MODN W=3U L=1U AD=3P AS=3P PD=5U PS=5U
M404 8 4 0 0 MODN W=5U L=1U AD=5P AS=5P PD=12U PS=12U

M405 6 2 5 0 MODN W=5U L=1U AD=5P AS=5P PD=12U PS=12U
M406 6 7 1 1 MODP W=8U L=1U AD=8P AS=8P PD=18U PS=18U
M407 7 6 1 1 MODP W=8U L=1U AD=8P AS=8P PD=18U PS=18U
M408 7 2 8 0 MODN W=5U L=1U AD=5P AS=5P PD=12U PS=12U
.ends SRLATCH

**********Clocked SR Latch End



**********Nand2 Gate Beginning
.subckt NAND2 1 2 3 4

*1=VDD 2=in0 3=in1 4=Nand2_out

M409 5 2 0 0 MODN W=8U L=1U AD=8P AS=8P PD=18U PS=18U
M410 4 3 5 0 MODN W=8U L=1U AD=8P AS=8P PD=18U PS=18U
```

```
M411 4 3 1 1 MODP W=4U L=1U AD=4P AS=4P PD=10U PS=10U
M412 4 2 1 1 MODP W=4U L=1U AD=4P AS=4P PD=10U PS=10U
.ends NAND2

**********Nand2 Gate End


**********Nor2 Gate Beginning
.subckt NOR2 1 2 3 4

*1=VDD 2=in0 3=in1 4=Nor2_out

M413 4 2 0 0 MODN W=2U L=1U AD=2P AS=2P PD=4U PS=4U
M414 4 3 0 0 MODN W=2U L=1U AD=2P AS=2P PD=4U PS=4U
M415 4 3 5 1 MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
M416 5 2 1 1 MODP W=32U L=1U AD=32P AS=32P PD=66U PS=66U
.ends NOR2

**********Nor2 Gate End



**********Inverter Beginning

.subckt INVP 1 2 3
*1=VDD 2=inp 3=outp
M417 3 2 0 0 MODN W=2U L=1U AD=2P AS=2P PD=4U PS=4U
M418 3 2 1 1 MODP W=8U L=1U AD=8P AS=8P PD=18U PS=18U
.ends INVP
**********Inverter End

.subckt INVN 1 2 3
*1=VDD 2=inp 3=outp
M419 3 2 0 0 MODN W=3U L=1U AD=3P AS=3P PD=8U PS=8U
M420 3 2 1 1 MODP W=8U L=1U AD=8P AS=8P PD=18U PS=18U
.ends INVN

**********Inverter End



.subckt DACCONT 1 42 43 44 45 46 47 48 49 50 51 52

*1=VDD 42=Clk 43=Vin+ 44=Vin-
*45=RZN_ext 46=RZP_ext 47=RZN 48=RZP
*49=N+ 50=P- 51=N- 52=P+

X1 1 42 43 44 53 54 SRLATCH

*P-
XPM 1 46 53 50 NAND2


*P+
XPP 1 46 54 52 NAND2

*P- = node 50
*N+ = node 49
XNP 1 45 54 49 NOR2
```

```
*P+ = node 52
*N- = node 51

XNM 1 45 53 51 NOR2



*RZP = node 48
XRZP 1 45 48 INVN

*RZN = node 47
XRZN 1 46 47 INVP


.ends DACCONT


.subckt DAC_toplevel 1 2 3 4 5 6 7 8 9VM 10VP 11 12

*1=VDD 2=Vnbias 3=Vncas 4=Vpcas 5=Vpbias
*6=Clk 7=RZN_ext 8=RZP_ext
*9VM=Vin- 10VP=Vin+ 11=Iout- 12=Iout+

XCONT 1 6 10VP 9VM  7 8 47RZN 48RZP 49NP 50PM 51NM 52PP DACCONT

XRZDAC 1 2 3 4 5 47RZN 48RZP 49NP 52PP 51NM 50PM 11 12 RZDAC

.ends DAC_toplevel


.include mos35u.cir

.op
.tran 1n 50us 0n 10n
*.ac dec 10 1 10e9
.PROBE
.END
```

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