# A NOVEL MODELING METHODOLOGY AND PERFORMANCE IMPROVEMENT TECHNIQUE FOR DMTL PHASE SHIFTERS

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Prof. Dr. Canan ÖZGEN

Director

I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science.

Prof. Dr. İsmet ERKMEN

Head of Department

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

| | |
|---|---|
| Assoc. Prof. Dr. Sencer KOÇ | Prof. Dr. Tayfun AKIN |
| Supervisor | Co-Supervisor |

Examining Committee Members:

| | | |
|---|---|---|
| Prof. Dr. Altunkan HIZAL | (METU, EEE) | |
| Assoc. Prof. Dr. Sencer KOÇ | (METU, EEE) | |
| Prof. Dr. Tayfun AKIN | (METU, EEE) | |
| Assoc. Prof. Dr. Şimşek DEMİR | (METU, EEE) | |
| Prof. Dr. Hayrettin KÖYMEN | (BİLKENT, EE) | |

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İpek İstanbulluoğlu

# ABSTRACT

## A NOVEL MODELING METHODOLOGY AND PERFORMANCE IMPROVEMENT TECHNIQUE FOR DMTL PHASE SHIFTERS

İstanbulluoğlu, İpek
M. Sc., Department of Electrical and Electronics Engineering
Supervisor: Assoc. Prof. Dr. Sencer Koç
Co-Supervisor: Prof. Dr. Tayfun Akın

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This thesis presents distributed MEMS transmission line (DMTL) phase shifters, emphasizing the circuit modeling and design as well as the performance improvement. A novel modeling methodology is introduced for DMTL unit sections, with bridge widths larger than 50 μm. The introduced model is compared with EM simulation results and the *CLR* modeling results. For structures with bridge widths larger than 50 μm, the introduced model fits the simulation results much better than the *CLR* model. The simulated structures are fabricated in METU micro-electronics facilities on glass substrates using gold structural layers. 1-20 GHz S-parameter measurement results of various DMTL structures are compared with the

introduced model. It is observed that the S-parameters match except for a scaling need in the insertion loss. The measurement results give 2 dB insertion and 15 dB isolation at 20 GHz.

The ABCD parameters of the introduced model are converted into S-parameters. Loss and the phase shift of the DMTL structures are expressed in terms of these S-parameters. These expressions are re-written as MATLAB code, from which the phase shift/loss (degree/dB) performance is evaluated. Therefore degree/dB plots with respect to bridge widths and center CPW conductor widths are obtained. From these plots the optimum DMTL phase shifters, which give maximum phase shift for minimum loss are determined for a pre-defined DMTL structure.

To increase the degree/dB performance of a DMTL phase shifter, a change in the geometry of the DMTL phase shifters is proposed. The geometry change is based on inserting an open-ended stub through the signal line and connecting one side of the stub to the bridge. By this way, the stub capacitance is added to the shunt capacitance of the bridge satisfying a larger phase shift. The simulations point out a performance of 217 degree/dB at 20 GHz with a 15 % change in the 25 μm wide bridge height ratio.

Keywords: RF MEMS, Distributed loaded line phase shifters, CPW open-ended stubs, Modeling, Micromachining.

# ÖZ

## DMİH FAZ KAYDIRICILAR İÇİN ÖZGÜN MODELLEME METODU VE PERFORMANS ARTTIRMA TEKNİĞİ

İstanbulluoğlu, İpek
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Doç. Dr. Sencer Koç
Ortak Tez Yöneticisi: Prof. Dr. Tayfun Akın

Eylül 2006, 135 sayfa

Bu tez, dağıtılmış hat MEMS iletim hattı (DMİH) faz kaydırıcılarını, devre modellemesi, tasarımı ve faz kaydırıma performansının iyileştirilmesi vurgulanarak sunmaktadır. Köprü genişliği 50 μm'den büyük olan DMİH'ların birim kesitleri için yeni bir modelleme yöntemi ortaya konmuştur. Önerilen model EM benzetim sonuçlarıyla ve *CLR* modellemesiyle karşılaştırılmıştır. Köprü genişliği 50 μm'den büyük olan yapılarda, önerilen yöntem *CLR*'a gore çok daha iyi sonuçlar vermektedir. Benzetimleri yapılan yapılar, METU mikro-elektronik tesislerinde taban malzemesi cam, yapısal malzemeler de altın olacak şekilde üretilmiştir. 1-20 GHz arası ölçülen S-parametreleri önerilen modelle karşılaştırmıştır. Araya girme kaybındaki artış dışında ölçümler modelle bire bir uyum göstermektedir. Ölçüm sonucunda, 20 GHz'te 2 dB araya girme kaybı, 15 dB yalıtım elde edilmiştir.

Önerilen modelin S-parametreleri ABCD parametreleri cinsinden ifade edilmiştir. Hattaki kayıp ve faz kaydırma miktarı elde edilen S-parametreleri cinsinden bulunmuştur. Bulunan ifadeler MATLAB kodu olarak tekrar yazılmış ve bu kod yardımıyla derece/kayıp performansı hesaplanmıştır. Bu sayede köprü genişliği ve sinyal hattı genişliğine göre değişen faz kaydırma/kayıp (derece/dB) grafikleri elde edilmiştir. Bu grafikleriden belirli bir DMİH faz kaydırıcı için maksimum derece/dB veren köprü ve sinyal hattı genişliği tesbit edilebilmektedir.

DMİH faz kaydırıcının derece/kayıp performansını arttırmak için, DMİH hattı yapısında fiziksel bir değişilik yapılması önerilmiştir. Yapılması planlanan değişiklik, sinyal hattına açık uçlu eş düzlemsel dalga kılavuzu kütük yerleştirilmesi esasına dayanmaktadır. Bu kütüğün açık olmayan ucu da köprüye bağlanmaktadır. Bu sayede, kütük kapasitansı da köprünün paralel kapasitansına eklenir ki bu da sonuçta elde edilen faz kaydırma miktarında bir artış demektir. EM benzetim sonuçları, 25 μm genişliğindeki köprülerin, köprü yüksekliğinin % 15 oranında değişmesi sonucu 217 derece/dB'lik bir performans öngörmektedir.

Anahtar Kelimeler: RF MEMS, Dağınık yüklenmiş hat faz kaydırıcılar, Açık uçlu EDK kütük, Modelleme, Mikroişleme.

*To My Mother and*
*My Father*

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# CHAPTER I

# INTRODUCTION

The MESSENGER spacecraft is the first mission to the planet Mercury, which will achieve Mercury orbit in 2011 to look for the answers concerning the geologic history and the present conditions of the planet. The MESSENGER communication system is designed to transmit the mission science data, receive spacecraft commands from Earth, and provide high-precision navigation data. This communication between the spacecraft and the earth will be established through an antenna system, which is referred as phased array systems [1]-[2]. MESSENGER is the first deep-space mission to use phased-array antennas, which allows the spacecraft to return a large amount of data without using a deployable, gimbaled antenna.

On the other hand, it is not necessary to go to deep-space missions to find an application area for phased-array antennas. Many AM broadcast stations use these systems to enhance signal coverage in the city of license, while minimizing interference to other areas. They are also used by warships of several navies including the Japanese, Spanish, and United States' navies. Considering these and other similar applications, it will be an appropriate conclusion to state that phased-array systems are of great importance in several RF communication implementations. Therefore, the issue should be to investigate what phased-array systems are and which components they are made of.

In telecommunication, a phased-array is defined as a group of antennas in which the relative phases of the respective signals feeding the antennas are varied in such a way

that the effective radiation pattern of the array is reinforced in a desired direction and suppressed in undesired directions (Figure 1.1). Therefore, the main components of a phased array system are power distributors, antennas, and some structures to change the relative phases of the respective signals. These structures are microwave phase shifters, which can be basically defined as circuit components used to change the transmission phase angle (phase of $S_{21}$) of a network. While the most important application of microwave phase shifters is within a phased array antenna system, there are many other implementation areas such as instrumentation systems or wireless communication [3].

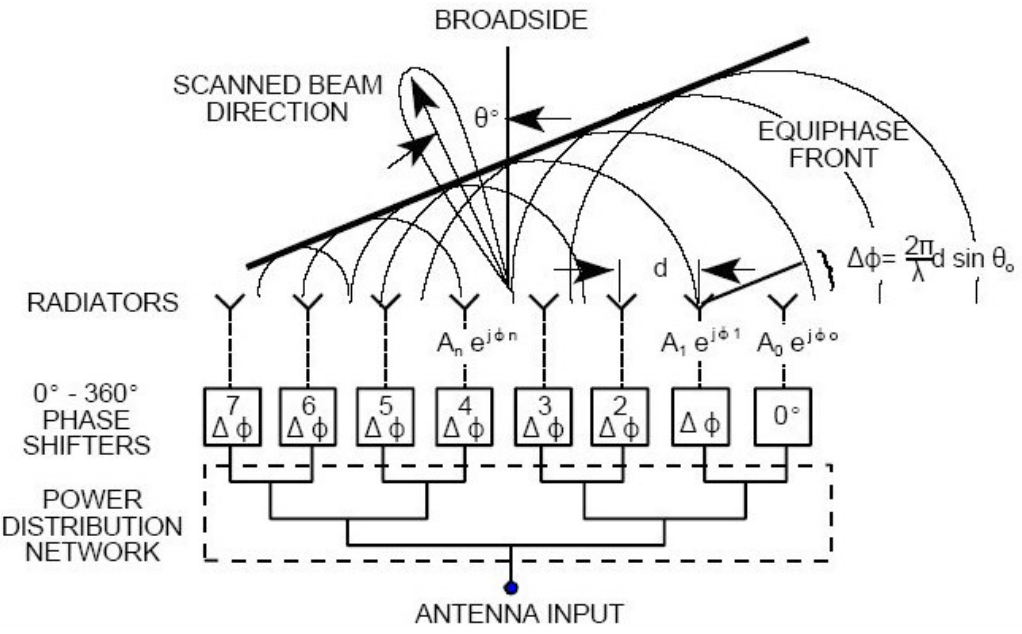



Figure 1.1 A phased-array system overview.

In this thesis it is aimed to present a complete modeling and performance improvement study on a specific type of microwave phase shifters, namely

distributed micro-electro-mechanical (MEMS) transmission line (DMTL) phase shifters. The main goals of this thesis are to introduce an improved modeling approach for DMTL structures and perform an improved performance DMTL phase shifter.

This chapter presents, these objectives will be detailed and essential background information about phase shifters. Section 1.1 will give the phase shifter overview and Section 1.2 will present the thesis organization.

## 1.1. PHASE SHIFTER OVERVIEW

The up to date phase shifters are mostly based on ferrite materials,PIN diodes,or FET switches [4]. The ferrite phase shifters are two-port components which satisfies a phase shift when the bias field of the ferrite is changed [5]. Although their performance is outstanding, their fabrication is expensive and they consume large amount of DC power. On the other hand, it is possible to built phase shifters by using switch mechanisms like PIN diodes or FET switches. Compared with ferrite phase shifters, the diode phase shifters offer small size structures and integration with planar circuitry. However, since the diodes require continuous bias current while a pulsed current is enough for ferrite devices, the DC power consumption is higher in PIN diode phase shifters. When the FET switch phase shifters are considered, it is observed that since they can be integrated with active elements on the same chip, the total assemble cost and size is reduced.

As stated previously, the phase shifting operation in the listed phase shifters currently depends on FET or PIN diode switches, when ferrite materials are eliminated because of their high power consumption. On the other hand, beside FET and PIN diode switches, RF MEMS switches have become a popular area of interest since 1995 because of the lower loss phase shifter designs they propose. Table 1.1

presents a performance comparison between the FET, PIN diode and RF MEMS switches [6]-[7], which brings the following comments:

- ⇨ The power consumption of MEMS switches is much lower than the other types of switches. This becomes a significant difference when phased-array like systems which contain a lot of switches are considered.
- ⇨ The up state capacitance is smaller in MEMS switches; therefore they can work in wider band operations.
- ⇨ The isolation of MEMS switches is better for all frequencies up to THz.
- ⇨ Since the MEMS switch and the other RF components such as antennas can be built on the same substrate (glass, quartz, ceramic…), the overall cost of the systems reduce.

Table 1.1 Performance comparison of FETs, PIN diode, and RF MEMS switches.

| Parameter | RF MEMS | PIN | FET |
|---|---|---|---|
| Voltage (V) | 20-80 | 3-5 | 3-5 |
| Power Consumption (mW) | 0.05-0.1 | 5-100 | 0.05-0.1 |
| Switching Time | 1-300 μs | 1-100 ns | 1-100 ns |
| $C_{up}$ (fF) | 1-6 | 40-80 | 70-140 |
| Cut off Frequency (THz) | 20-80 | 1-4 | 0.5-2 |
| Isolation (1-10 GHz) | Very high | High | Medium |
| Isolation (10-40 GHz) | Very high | Medium | Low |
| Isolation (60-100 GHz) | High | Medium | None |
| Loss (1-100 GHz) | 0.05-0.2 | 0.3-1.2 | 0.4-2.5 |
| $C_{up}$ (fF) | 1-6 | 40-80 | 70-140 |

On the other hand, RF MEMS switches have slower switching time, and lower power handling, which is in the order of 10 mWs. Because of these limitations they are not suitable for high-speed and high-power operations. However, beside these limitations, the major reasons which prevent RF MEMS switches to become the number one commercial switches are their reliability and packaging problems.

### 1.1.1. RF MEMS Phase Shifters

The advantages using RF MEMS technology in switch implementation is already covered. It is also possible to observe the same advantages in RF MEMS phase shifters as Table 1.2 illustrates [7]. As it is obvious, for all the band operations, RF MEMS phase shifters result in lower loss. Therefore, any complicated structure such as communication or radar systems which get use of RF MEMS phase shifters will benefit from the loss. This benefit can be directed to a reduction in the number of amplifying stages in the overall systems. Finally, this reduction decreases the overall DC loss and cost of the system.

Table 1.2 Average on Wafer Loss for MEMS and GaAs-FET 3-bit Phase Shifters

| Frequency (GHz) | X-Band | Ka-Band | V-Band | W-Band |
|---|---|---|---|---|
| RF MEMS Loss (dB) | -0.9 to -1.0 | -1.7 to -2.0 | -2.3 to -2.5 | -2.7 to -3.3 |
| GaAs FET Loss (dB) | -3 to -4 | -6 to -7 | -8 to -9 | -9 to -11 |

RF MEMS phase shifters, as well as PIN diode or FET phase shifters, can be examined in mainly three different types namely switched line, reflection, and loaded line, [8 ]-[9 ]. A simple switched-line RF MEMS phase shifter ( Figure 1.2 (a) ) is composed of two different length transmission lines ($l_1, l_2$) and SPDT (single pole double throw) MEMS switches, which are used to decide which path will be chosen,

[10]-[11]. $\Delta\phi = \beta(l_2 - l_1)$ is obtained as a differential phase difference between these two paths, where $\beta$ is the propagation constant of the line. The two different length transmission lines and the corresponding switches compose a bit. It is possible to design N-bit phase shifters, which satisfies digital phase shifting, [4].

Reflection type phase shifters use hybrid couplers to divide the input signal into two signals out of phase as Figure 1.2 (b) demonstrates. These signals reflect from a pair of switched loads. The lengths of the loads are changed with the help of MEMS switches and this change modifies the phase of the reflected signal [12]-[13].

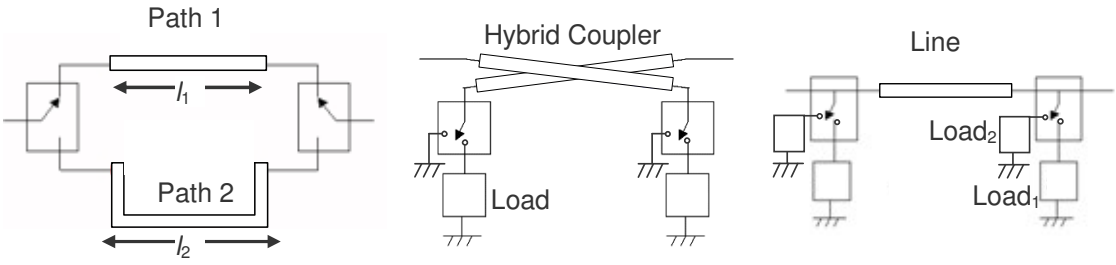



Figure 1.2 (a) Reflection phase shifter. (b) Switched-line phase shifter. (c) Loaded-line phase shifter.

The last category of phase shifter is the loaded-line phase shifter, which usually gives smaller phase shifts compared to reflection type, [14]-[15]. The study of loaded-line phase shifters began nearly half century ago and extensive analysis were executed during 1960s and 1970s [16]-[19]. In loaded-line phase shifters, the loads are connected to a transmission line such that they affect the phase of the signal significantly, while they have a small effect on the amplitude ( Figure 1.2 (c) ). Switching between two different loads, which are generally selected to be reactive and are shunt connected to the lines, changes the phase of the system.

### 1.1.2. Distributed MEMS Phase Shifters

This thesis mainly studies periodically loaded-line phase shifters with MEMS switch implementation, which are referred as distributed MEMS transmission lines (DMTL) [20]-[21]. In a distributed MEMS transmission line, the loading is realized by the MEMS bridges suspending over the center conductor. These bridges satisfy shunt capacitance for the transmission line. By adjusting the height of the bridges this capacitance is changed. Figure 1.3 shows such a configuration for a CPW based structure. It is also possible to use micro-strip (MS) lines instead; however, it will bring implementation difficulties, considering via holes needed in MS lines. Free from the type of the transmission line selected, usually the characteristic impedance of the unloaded line is selected to be larger than 50 Ω, since this value will decrease as the line is loaded. The conspicuous advantages of DMTL phase shifters can be listed as follows:

- ⇨ They can be designed using straightforward equations.
- ⇨ They offer wideband performance.
- ⇨ They can work well at very high frequencies.

The DMTL phase shifters can be categorized into two as analog and digital. In an analog type DMTL phase shifter, all the bridge heights are adjusted using a single bias voltage. By applying different actuations, the height of the bridges can be decreased continuously up to theoretically 2/3 of its original height, which satisfies an increase in the shunt capacitance. This brings a continuous change in phase shift amount [22] depending on the actuation voltage. In the digital distributed phase shifters, a discrete capacitor is placed in series with the MEMS bridge [23]-[26]. When there is no actuation, the effective capacitance is the up-state capacitance of the bridge. On the other hand, after actuation, the MEMS bridge is in the down-state

position and the effective capacitance becomes the discrete series capacitance. Therefore by actuation, the distributed capacitance can be digitally controlled. Many sections of digital phase shifters can with predefined phase shifts can be cascaded in order to have N-bit digital phase shifters.

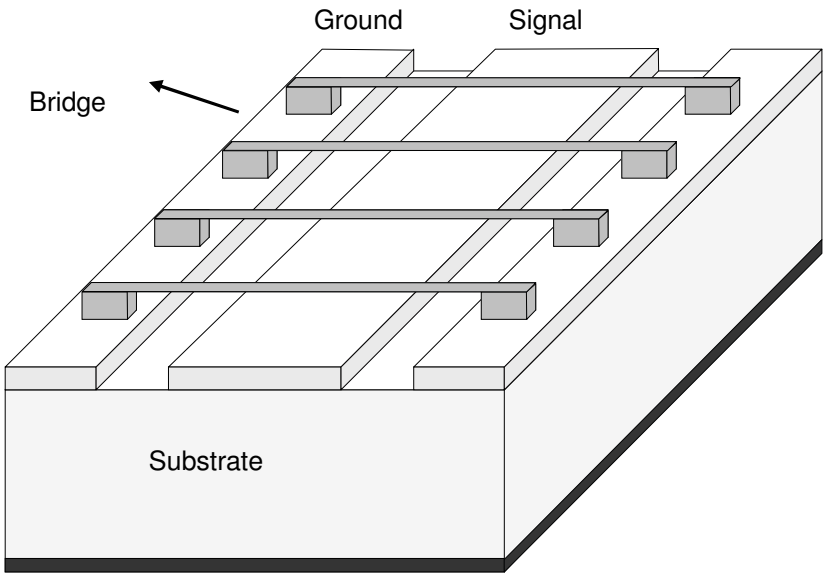



Figure 1.3 Distributed MEMS transmission line (DMTL) schematic.

It is better to decide the performance of a DMTL phase shifter by considering its phase shift amount for 1 dB loss (degree/dB). Barker and Rebeiz did an optimization study on analog type distributed phase shifters [27], where they obtained an U-band design wit a performance of 50 °/dB at 20 GHz with a change of 17 % in the loading capacitance. Before Barker and Rebeiz, another optimization was done by Nagra and York using Schottky diodes [22]. Table 1.3 presents some other studies made on DMTL phase shifters.

Table 1.3 Examples of fabricated DMTL Phase Shifters.

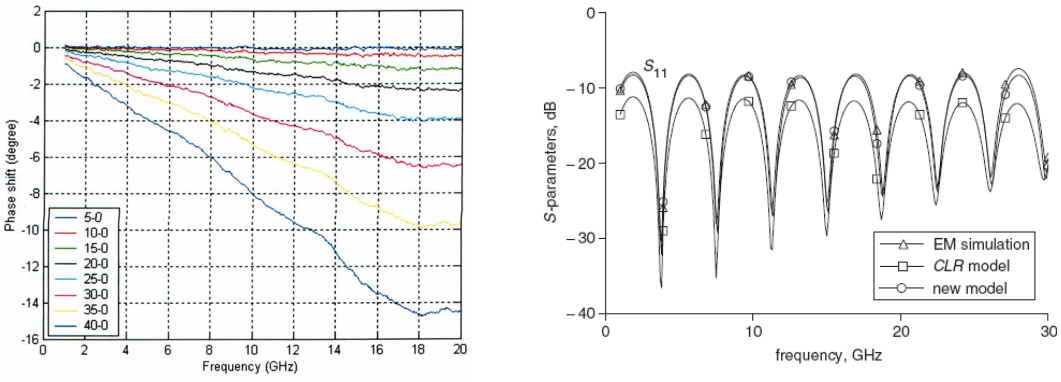
| Freq. (GHz) | Bits | Design | Substrate | Average Loss (dB) | Return Loss (dB) | Ref. |
|---|---|---|---|---|---|---|
| 13.6 | 2 | CPW | Quartz | −1.2 | −12.5 | [14] |
| 16.0 | 4 | μ-strip | Silicon | −3.0 | −9.5 | [15] |
| 26.0 | 3 | CPW | Glass | −1.7 | −7.0 | [16] |
| 37.7 | 2 | CPW | Quartz | −1.5 | −11.5 | [14] |
| 60.0 | 2 | CPW | Quartz | −2.2 | −10.0 | [17] |
| 94.0 | Analog | CPW | Quartz | −2.5 | −11.0 | [18] |

### 1.1.3. Previous DMTL Phase Shifter Studies at METU

The previous studies done in METU concerning DMTL phase shifters can be examined in two separate areas. First one is the initial DMTL phase shifter design, fabrication, and measurement study which was handled during the master thesis of Hüseyin Sağkol [28]. This study involves two different DMTL phase shifters: one with standard MEMS shunt bridge structure and another with T-wing type MEMS switch. The standard phase shifter is measured to give a phase shift of 15 degrees at 20 GHz when actuated by 40 volts, where the T-wing type could not be measured because of sticion problem during the release process. The result of the measured DMTL phase shifter in this thesis work is presented in Figure 1.4 (a).

The second study concerning DMTL structures is the modeling study which is finalized as in [29]. The model proposed in this study uses shunt capacitor and series inductor parameters to describe the discontinuities arise around the MEMS bridge.

Although, the model reactance parameters can not be analytical expressed, it gives better results compared with the *CLR* model as Figure 1.4 (b) points out.




(a) (b)

Figure 1.4 (a) The measured DMTL phase shifter in the thesis work of Hüseyin Sağkol. (b) The results of the modeling study finalized in [29].

## 1.2. THESIS OBJECTIVES AND ORGANIZATION

The main objectives of this thesis are to introduce an improved modeling approach for DMTL structures and perform an improved performance DMTL phase shifter. the specific objectives of this thesis can be listed as follows:

- ⇨ Improvement of the modeling studies for DMTL structures with bridge widths larger than 50 um. The *CLR* model and the previously introduced model [29] should be investigated in order to detect their deficiencies. A new and simple model which fills these deficiencies should be developed and its model parameters should be analytically expressed. This model should give very close results with the simulations and its validity should be verified by the measurements. Using this new model, a practical way to evaluate the

degree/dB performance of DMTL phase shifters should be developed in order to find the optimum performance phase shifter for a pre-defined DMTL structure before making long duration simulations.

- ⇨ Improvement of degree/dB performance of DMTL phase shifters by changing the structure topology. Coplanar Waveguide (CPW) discontinuities and their possible uses in DMTL structures should be investigated. The capacitance ratio for the up and down-states of the DMTL bridges should be increased satisfying a larger phase shift, using these discontinuities.

- ⇨ Setting a process flow for the fabrication of the designed DMTL structures in order to verify the introduced model and setting a measurement setup for the fabricated structures. The process flow developed at METU should be updated to result in a low loss and low stress structural layers. The calibration techniques for the measurement of the DMTL structures should be selected.

The thesis is organized as follows:

Chapter II introduces the background theory of the main structures mentioned in the following sections of the thesis. Coplanar waveguide (CPW) theory, RF MEMS switch theory, distributed MEMS transmission line (DMTL) theory, and DMTL phase shifter theory are explained in this chapter. This chapter also gives the details of the conductor backed and top covered CPW structures with attenuation characteristics analysis.

Chapter III describes the main design methodology of the DMTL phase shifters beginning with the modeling study. The expressions of the model parameters are extracted and the introduced model is compared with the *CLR* model and the

simulations. Additionally, in this chapter a MATLAB code is constructed from the introduced model ABCD parameters to evaluate the degree/dB performance of DMTL phase shifters. This chapter also presents an alternative way to improve degree/dB performance of DMTL phase shifters by inserting open-end stub CPW discontinuity through the center conductor of DMTL.

Chapter IV describes the major steps of the fabrication. Layout drawing and mask generation of the designed DMTL structures are summarized and general properties of fabrication materials and techniques are explained. SEM pictures of the fabricated structures are presented and thin-film stress observations are made in this chapter.

Chapter V presents the measurement results of the fabricated structures. The measurement setup is basically described and the measurement data are compared with the model results.

Finally, Chapter VI summarizes the research developed in this thesis, discusses the conclusions, and gives possible future works.

# CHAPTER II

# COPLANAR WAVEGUIDE, MEMS SWITCH AND DMTL PHASE SHIFTER THEORY

In this chapter essential basic background theory of some RF components will be resented. Section 2.1 will give the theory of coplanar waveguides, Section 2.2 will give the theory of RF MEMS switches, and Section 2.3 will give the theory of distributed MEMS transmission lines.

## 2.1. COPLANAR WAVEGUIDE THEORY

A coplanar waveguide (CPW) structure consists of a signal line centered on a dielectric substrate and separated from two ground planes by gaps as Figure 2.1 shows. This structure is first introduced by C. P. Wen in 1969 [30] and since then, it encountered several developments. Coplanar waveguides are classified as:

- ✓ Conventional CPW
- ✓ Conductor backed CPW (CBCPW)
- ✓ Micromachined CPW

The first introduced type is the conventional CPW in which the ground planes are extending to infinite, which is not possible in practice. In conductor backed CPW, there exist a ground plane covering the bottom side of the dielectric layer [31]. The micromachined CPWs are classified into two. First one is the microshield line and the second one is the CPW suspended by a silicon dioxide membrane above a micromachined groove which find detailed explanation in [32] and [33].

Coplanar waveguide structure has several advantages over the micro-strip line. The main advantage is that there is no need for via holes in CPW in spite of micro-strip lines. Therefore, series-shunt element mounting and fabrication is easier with CPW technology. As a second advantage, in CPW, the characteristic impedance ratio depends on only W/G ratio. This enables a reduction in CPW circuit size by lowering W and G values. Moreover, in CPW structures, the ground planes cover signal lines from both sides, which mostly eliminates the cross talk effects between two signal lines are mostly eliminated. Considering these advantages, it is obvious that CPW is suitable for both MIC and MMIC applications [30].

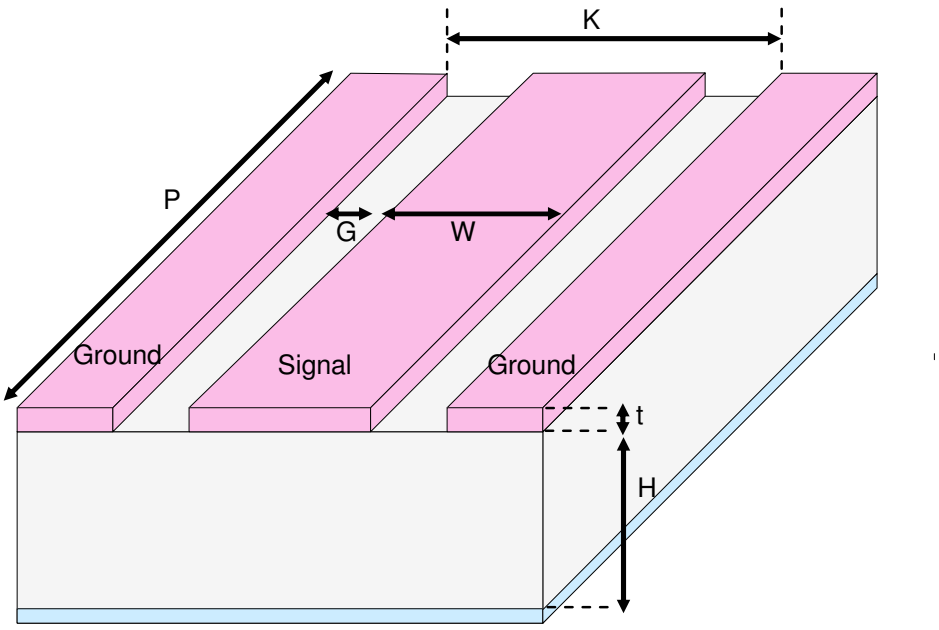



Figure 2.1 Coplanar Waveguide schematic.

### 2.1.1. Conductor Backed Coplanar Waveguide (CBCPW)

As mentioned in the previous section, there exists a ground plane covering the bottom side of the dielectric layer in CBCPW. This additional ground plane mechanically supports the substrate and operates as a heat sink for active device circuits. Moreover, it is advantageous to have such a ground plane at the bottom when CPW and micro-strip structures are designed to be built on the same substrate. The main parameters which are determined from the CPW dimensions are the characteristic impedance and the effective permittivity of CPW. These parameters are defined by (2.1)-(2.4) [34]-[35].

$$\varepsilon_{eff,H-CLR} = \frac{1+\varepsilon_r \dfrac{K(k')}{K(k)}\dfrac{K(k_3)}{K(k_3')}}{1+\dfrac{K(k')}{K(k)}\dfrac{K(k_3)}{K(k_3')}} \tag{2.1}$$

where $K$ is the elliptic integral of the first order.

$$Z_{H,CLR} = \frac{60\pi}{\sqrt{\varepsilon_{eff,H-CLR}}}\frac{1}{\left(\dfrac{K(k)}{K(k')}+\dfrac{K(k_3)}{K(k_3')}\right)} \tag{2.2}$$

$$k = W/K \qquad k_3 = \frac{\tanh(\pi W/2H)}{\tanh(\pi K/2H)} \tag{2.3}$$

$$k' = \sqrt{1-k^2} \qquad k_3' = \sqrt{1-k_3^2} \tag{2.4}$$

### 2.1.2. CBCPW Analysis in the Presence of a Top Metal Cover

The CBCPW structure can be used with a metal top cover over the signal and ground lines, which brings extra fields in the solution region as Figure 2.2 illustrates. With this configuration, basically four different situations [36] arise as a result of the variations in the height of the top metal, $H_1$ and the gap distance, G. The top metal height, $H_1$ is comparable with the substrate thickness, H and the ground planes are not at a very far distance from the center conductor in the first situation. With this configuration the structure shows the properties of a CBCPW with a top cover. Different from this case, in the second situation, the top cover height is much larger than the substrate height, which makes the structure behave as a simple CBCPW. The third situation is similar to the first situation, this time the ground planes are at a far distance from the center conductor, making G value increase. When this G value exceeds a limit, the fields in the solution region show the characteristics of a micro-strip line rather than a CPW. Therefore, for this situation the case resembles like a shielded micro strip line. Finally, the last situation differs from the third one by the increase in the height of the top cover, which converges to a simple micro strip line structure. For the topics covered in this thesis, the last case will be of great importance.

Since the last case resembles micro strip line, it will be a good approximation to use the micro-strip line equations to evaluate the characteristic impedance and the effective permittivity of this case as given in equations (2.5)-(2.7).

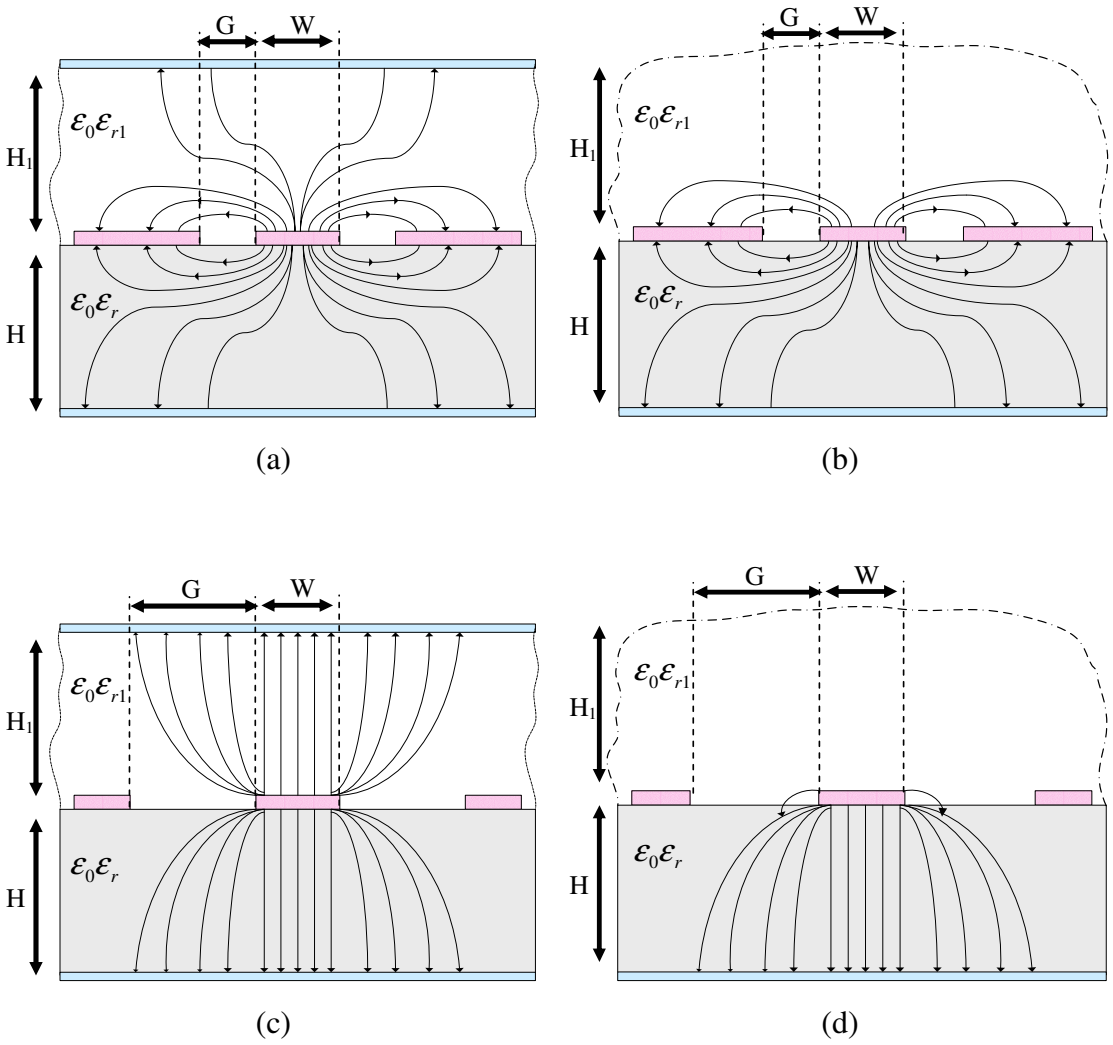



Figure 2.2 CBCPW with top cover limiting cases.

$$\varepsilon_{eff,L} = \frac{(\varepsilon_r + 1)}{2} + \frac{(\varepsilon_r - 1)}{2} F - \frac{(\varepsilon_r - 1)}{\varepsilon_{r1}} \frac{t}{h\sqrt{W/h}} \tag{2.5}$$

$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_{eff,L}}\left(\frac{\chi}{h} + 1.393 + 0.667 \ln\left(\frac{\chi}{h} + 1.444\right)\right)} \tag{2.6}$$

$$\chi = h\left(\frac{W}{h} + \frac{1.25t(1+\ln 2h/t)}{\pi h}\right) \tag{2.7}$$

For this last case, it is stated that the back conductor is closer to the signal line compared to the top cover. On the other hand, if the top cover gets much closer to the signal line compared to the back conductor, the line again behaves as a micro strip line. However, this time $\varepsilon_r$ and $\varepsilon_{r1}$ should be interchanged in equation (2.5). Moreover, if the second dielectric is air, i.e. the top cover is suspending in the air, $\varepsilon_{r1}$ becomes unity and so does $\varepsilon_{eff,L}$.

### 2.1.3. Attenuation Characteristics of CPW

The total CPW attenuation can be defined as the attenuation due to the dielectric losses in the substrate and the attenuation due to the conductor losses in the center conductor, ground planes and the bottom conductor [30]..

$$\alpha_H = \alpha_C + \alpha_D \tag{2.8}$$

The attenuation due to the dielectric loss can be defined as:

$$\alpha_D = \frac{8.686\pi f}{c}\frac{\varepsilon_r}{\sqrt{\varepsilon_{eff,H}}}\tan\delta_e q \ \text{dB/m} \tag{2.9}$$

where $\tan\delta_e$ is the loss tangent of the substrate and $q$ is defined as:

$$q = \frac{K(k_1)K(k')}{2K(k_1')K(k)} \tag{2.10}$$

On the other hand, the attenuation due to the conductor losses is expressed as:

$$\alpha_C = 8.686 \frac{R_C + R_G}{2Z_H} \text{ dB/m} \tag{2.11}$$

where, $R_C$ is the series resistance of the center conductor and $R_G$ is the distributed series resistance of the ground planes in ohms per unit length.

$$R_C = \frac{R_S}{4W(1-k^2)K^2(k)}\left(\pi + \ln(4\pi W/t) - k\ln\frac{1+k}{1-k}\right) \tag{2.12}$$

$$R_G = \frac{kR_S}{4W(1-k^2)K^2(k)}\left(\pi + \ln(4\pi K/t) - \frac{1}{k}\ln\frac{1+k}{1-k}\right) \tag{2.13}$$

$$k_1 = \frac{\sinh(\pi W/4H)}{\sinh(\pi K/4H)} \qquad k_1' = \sqrt{1-k_1^2} \tag{2.14}$$

$$R_S = \frac{1}{\delta\sigma}\ \Omega \qquad \delta = \sqrt{\frac{2}{\omega\mu\sigma}}\ \text{m} \tag{2.15}$$

here, $R_S$ is the skin effect surface resistance, $\sigma$ is the conductivity of the conductor and $\delta$ is the skin dept [37].

## 2.2. RF MEMS SWITCH THEORY

A switch is a device which allows signal transmission in one position and prevents it in the other. RF MEMS switches satisfy this operation at RF to millimeter wave frequencies with the help of mechanical movement and by achieving short or open

circuits in the RF transmission line [38]. This movement is mostly realized by electrostatic, magnetic, piezoelectric or thermal actuators. RF MEMS switches have advantages over the other types of switches namely pin diode or FET switches. These advantages are: low power consumption, very high isolation, very low insertion loss, and low cost. On the other hand, they also have disadvantages like low switching speed, low power handling, and high voltage drive. Moreover, packaging difficulty, reliability and the overall cost after packaging are the other issues which can be counted as the drawbacks of RF MEMS switches.

Although, there are several ways to achieve a mechanical movement, the most common way is the voltage actuation [38]. Voltage actuation depends on the idea of creating a voltage difference between the bridge and the bias electrode. Therefore, a downwards electrostatic force will occur between the bridge and the electrode which can be expressed as:

$$F_{electostatic} = \frac{1}{2}\varepsilon_0 A E^2 = \frac{\varepsilon_0 A V^2}{2\left(g + \frac{t_d}{\varepsilon_{rd}}\right)^2} \text{ Nt} \tag{2.16}$$

where, $A$ is the area of the intersection area of the bridge and the electrode, $V$ is the voltage and $g$ is the gap distance between the bridge and the electrode, $t_d$ is the thickness and $\varepsilon_{rd}$ is the relative permittivity of the dielectric layer on top of the electrode (Figure 2.4).

On the other hand, as a result of the deflection of the bridge an upwards force coming from the spring constant of the bridge arises as (2.17) expresses. Here, $g_0$ is the original gap distance before actuation and k is the spring constant.

$$F_{spring} = -k(g_0 - g) \text{ Nt} \tag{2.17}$$

For, stability these two forces should be in equilibrium. When the downwards force gets sufficiently larger, the bridge collapses on the electrode. This situation becomes possible when the bridge is deflected to make the gap 2/3 of its original position [38]. Therefore, if the expressions for the two forces are equated and the $g$ is taken as $2g_0/3$, the pull-down voltage can be found as in (2.18). Below this pull-down voltage, the bridge continues to bend, whereas above this value it collapses.

$$V_{pull-down} = \sqrt{\frac{8kg_0^3}{27\varepsilon_0 A}} \text{ Volts} \qquad (2.18)$$

As previously mentioned, long switching time is one of the disadvantages of RF MEMS switches. The expression for the switching time is found from nonlinear dynamic analysis of MEMS beams and expressed as [38]:

$$t = 3.67\frac{V_{pull-down}}{V_S \omega_0} \text{ seconds} \qquad (2.19)$$

where $V_S$ is the applied voltage. As the limitations on $V_S$ and the resonant frequency are considered, it is expected that the practical switching time will be about 1 μs.

There are two types of switches used in RF MEMS applications, namely series and shunt switch. The series switch enables a path for the signal when it is actuated (down-state position). When no bias is applied, it behaves as an open circuit as Figure 2.3 (a) illustrates. The shunt switch, conversely, allows the signal to pass through the transmission line when there is no actuation and the switch is in the up-state position. When a bias is applied, it connects the signal line to the ground and prevents the signal to reach to the other side of the transmission line. More detailed discussions about RF MEMS shunt switches will be presented in the next sections.

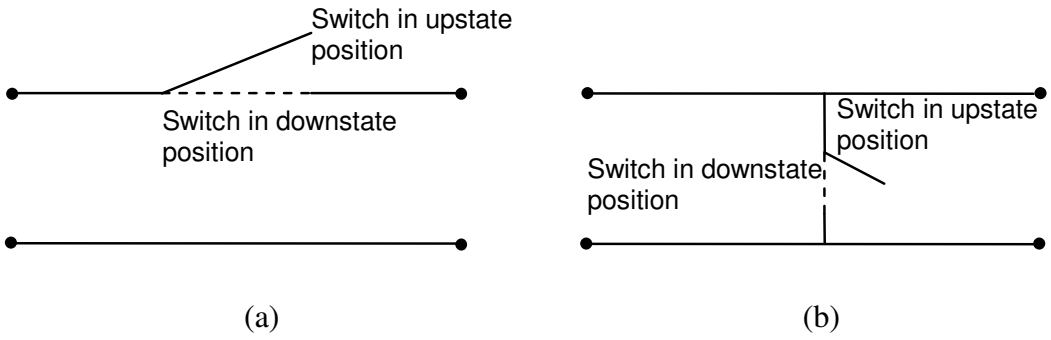



Figure 2.3 Schematic of (a) series switch (b) shunt switch.

### 2.2.1. RF MEMS Shunt Switch

The switch configuration that will be explained in this section is CPW RF MEMS shunt switch, which Figure 2.4 illustrates. Here, the bridge is suspending over the center conductor (signal line) and it is connected to ground planes on two sides.

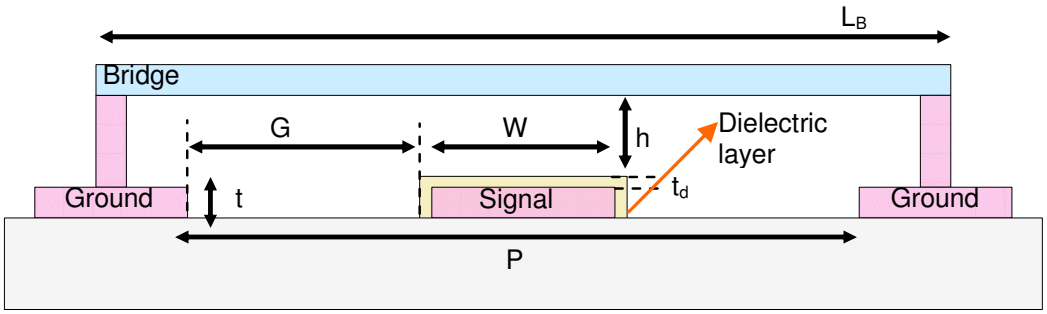



Figure 2.4 Side view of RF MEMS shunt switch with bridge anchors are connected to ground planes.

The actuation points for this configuration are the ground planes and the signal line; therefore, when a bias is applied, there will be a potential difference between the

bridge and the signal line. As a result of this difference, an electrostatic force occurs, which pulls the bridge down. The change in the position of the bridge causes a change in the amount of parallel plate capacitance between the signal line and the ground. When the applied voltage reaches and exceeds the pull-down voltage, the bridge collapses, which increases this parallel plate capacitance significantly. By this way, the signal going on the center conductor finds a low-impedance path to ground.

#### *2.2.1.1. RF MEMS Shunt Switch Circuit Model (The CLR Model)*

The top view and the *CLR* lumped model of the shunt switch is presented in Figure 2.5. As the figure reveals, the switch is modeled as two transmission lines and the *CLR* representation of the bridge [7]. The transmission lines are of *P*/2 length where the other parameters of these lines are calculated using the standard CPW transmission line equations (2.1)-(2.4).

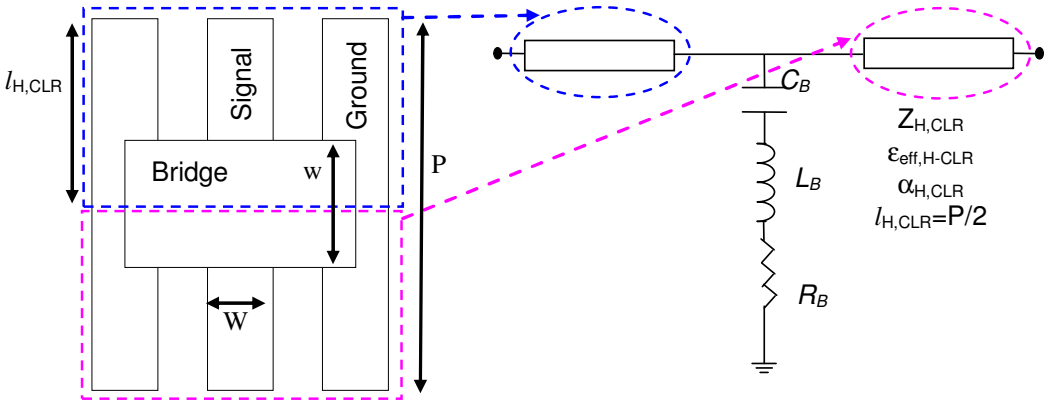



Figure 2.5 Top view of a shunt switch and its lumped element model.

From this *CLR* model the overall impedance of the switch can be driven as:

$$Z_S = R_B + j\omega L_B + \frac{1}{j\omega C_B} \tag{2.20}$$

From this equality, it is obvious that $Z_S$ can be approximated as follows for different frequency ranges:

$$Z_S = \begin{cases} \dfrac{1}{j\omega C_B} & for \quad f << f_0 \\ R_B & for \quad f = f_0 \\ j\omega L_B & for \quad f >> f_0 \end{cases} \tag{2.21}$$

where,

$$f_0 = \frac{1}{2\pi\sqrt{L_B C_B}} \tag{2.22}$$

From the overall impedance expression, the cut off frequency, which is defined as the frequency at which the up and down-state impedance ratio is one [7], can be evaluated as:

$$f_C = \frac{1}{2\pi C_{B\_up} R_B} \tag{2.23}$$

where, $C_{B\_up}$ is the up-state parallel plate capacitance. This cut off frequency determines the RF performance of a switch and it is in the order of 10-100 THz for RF MEMS switches.

#### *2.2.1.2. RF MEMS Shunt Switch Electromagnetic Model*

The defined parameters of the CLR model are extracted using some techniques which will be covered in this section. To begin with, the parallel plate capacitance when the bridge is in the up-state position is simply evaluated by:

$$C_{B\_up} = \varepsilon_0 \frac{wW}{h + t_d / \varepsilon_{rd}} \tag{2.24}$$

This value is the sum of the capacitance of the air and the capacitance of the dielectric layer, which where $w$,$W$,$h$, and $t_d$ are defined in Figure 2.4. For down-state position, the expression is shorter since the capacitance through the air is eliminated.

$$C_{B\_down} = \varepsilon_0 \frac{\varepsilon_{rd} wW}{t_d} \tag{2.25}$$

As opposed to the capacitance expressions, the resistance, $R_B$ and the inductance, $L_B$ do not have accurate formulas. Instead, they are modeled using numerical electromagnetic techniques [7]. Even though it can not be formulated, the inductance can be stated to depend on the part of the bridge which is on the gaps. Since the current distribution is mostly concentrated about the edges of the conductors. On the other hand, the resistance can be expressed as a sum of two components, which arise due to the transmission line loss and the bridge loss, [7]. The part which is due to the transmission line loss is evaluated using the expression:

$$R_{B\_TL} = 2Z_0 l\alpha, \quad \text{where } \alpha \text{ is the line loss in Np/m} \tag{2.26}$$

The resistance due to the bridge needs a more complicated evaluation process which will not be detailed here but can be found in [7].

After the electromagnetic modeling parameters are defined, what should be determined is the loss of the RF MEMS switch. It should be noted that the loss can not be expressed by $|S_{21}|^2$ alone, since it is only the insertion loss. However, what prevents the transmission of all the power to the other side of the line is the effect of both the insertion loss and the reflection. Therefore, the overall loss can be expressed as [7]:

$$Loss = 1 - \left|S_{11}\right|^2 - \left|S_{21}\right|^2 \tag{2.27}$$

For the up-state position where, the switch is not touching the signal line, the reflection coefficient can be given as:

$$S_{11} = \frac{-jC_{B\_up}Z_0}{2 + j\omega C_{B\_up}Z_0} \qquad \left|S_{11}\right|^2 = \frac{\omega^2 C_{B\_up}Z_0}{4} \tag{2.28}$$

which enables a direct calculation of up-state capacitance value. The second identity in equation (2.28) is found by assuming that $S_{11}$ is much smaller than -10dB or $\omega C_{B\_up}Z_0$ is much smaller than 2. For the down-state, the isolation, which can be defined as the amount of signal transferred from one port to the other when the signal line is shorted to ground, is found by:

$$S_{21} = \frac{1}{1 + j\omega C_{B\_down}Z_0/2} \qquad \left|S_{21}\right|^2 = \begin{cases} \dfrac{4}{\omega^2 C_{B\_down}^2 Z_0^2} & for \quad f << f_0 \\ \dfrac{4R_B^2}{Z_0^2} & for \quad f = f_0 \\ \dfrac{4\omega^2 L_B^2}{Z_0^2} & for \quad f >> f_0 \end{cases} \tag{2.29}$$

## 2.3. DISTIBUTED MEMS TRANSMISSION LINE THEORY

A transmission line can be loaded placing periodically spaced capacitive elements on it. In a distributed MEMS transmission line, this loading can be realized by the MEMS bridges suspending over the center conductor. Figure 2.6 shows such a configuration for a CPW based structure. It is also possible to use micro-strip lines instead; however, it will be difficult to implement since via holes are needed in micro-strip lines. Whatever the type of the transmission line selected, usually the characteristic impedance of the unloaded line is selected to be larger than 50 Ω, since the characteristic impedance of the line will decrease as it is loaded [39]. Therefore, if the loading is adjusted properly, the loaded line can have about 50 Ω characteristic impedance, which will match the 50 Ω feedings.

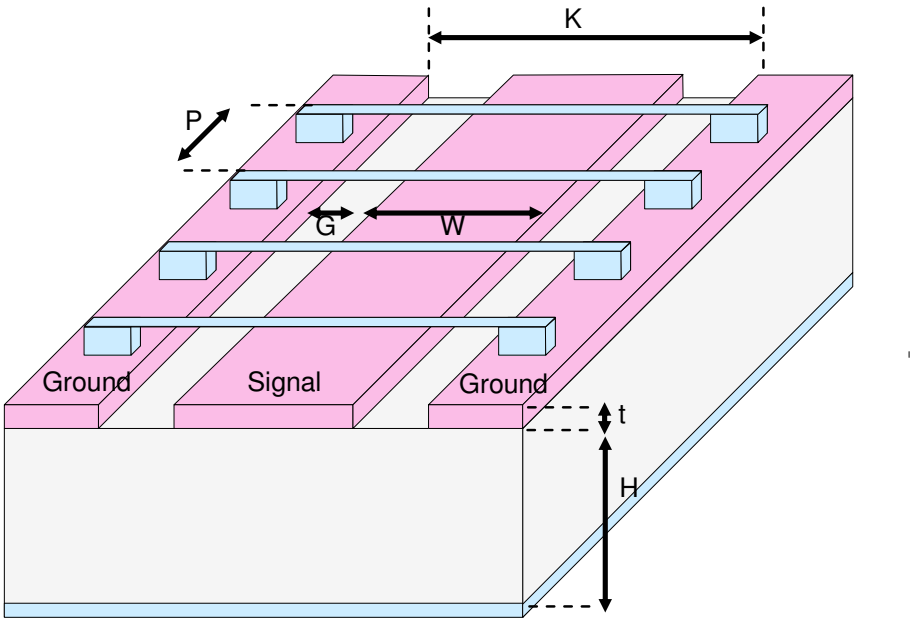



Figure 2.6 Distributed MEMS transmission line (DMTL) schematic

Figure 2.7 presents the lumped equivalent model of the unit length DMTL. Here, the $L_{tl}$ and $C_{tl}$ stand for per unit length inductance and capacitance of the unloaded line and P is the spacing between the consecutive MEMS bridges. (2.30) gives the

expressions for per unit length inductance and capacitance, where (2.31) defines the relation between the loaded line impedance and the model parameters.

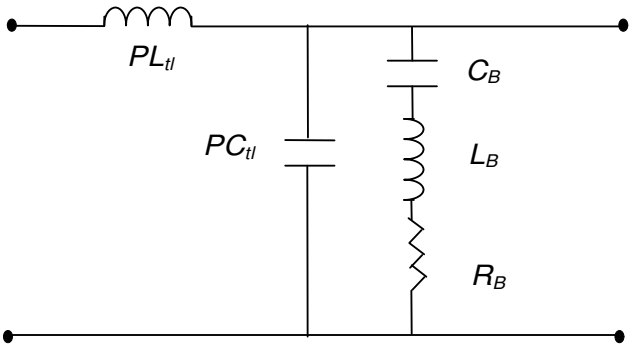



Figure 2.7 Lumped element transmission line model of the unit length DMTL

$$C_{tl} = \sqrt{\frac{\varepsilon_{eff,H}}{cZ_0}} \qquad L_{tl} = C_{tl} Z_0^2 \tag{2.30}$$

$$Z_{loaded} = \sqrt{\frac{PL_{tl}}{PC_{tl} + C_B}} \sqrt{1 - \left(\frac{\omega}{\omega_B}\right)^2} \tag{2.31}$$

The discontinuities that arise due to the periodic loading of capacitive bridges create reflections. In other words, each capacitor causes a reflection while the signal propagates through the transmission line. At a certain frequency the reflected and the incident signals interfere destructively, which prevents the transmission of the signal to the other port. This frequency is defined as the Bragg frequency (2.32) and acts as a cut off point for DMTL structures [39].

$$\omega_B = \frac{2}{\sqrt{PL_{tl}\left(PC_{tl} + C_B\right)}} \tag{2.32}$$

The operating frequency of a DMTL structure must be smaller than the Bragg frequency in order to satisfy a power transfer. At the Bragg frequency, the loaded

line impedance, $Z_{loaded}$ becomes zero as (2.31) predicts. When the operating frequency is much smaller than $\omega_B$, the loaded line impedance becomes:

$$Z_{loaded} = \sqrt{\frac{PL_{tl}}{PC_{tl} + C_B}} \tag{2.33}$$

On the other hand, from time delay calculations; it is possible to find the effective dielectric constant of the loaded line as [7]:

$$\sqrt{\varepsilon_{eff,loaded}} = \frac{c\sqrt{PL_{tl}(sC_{tl} + C_u)}}{P} = \frac{2c}{P\omega_B} \tag{2.34}$$

where c is the speed of the light in m/s.

When the line is loaded, the loss of the line differs from. The overall loss for a loaded transmission line can be shown to be [7]:

$$\alpha_{loaded\_line} = \frac{R_{tl}}{2Z_{loaded}} + \frac{G_{tl}Z_{loaded}}{2} \tag{2.35}$$

where, the first term accounts for the transmission line conductor losses and the second term represents the dielectric losses. Here, $R_{tl}$ is a series resistance and $G_{tl}$ is a shunt admittance which are used together with $L_{tl}$ and $C_{tl}$ to represent the per unit length loaded transmission line. On low loss substrates, the dielectric loss can be ignored and equation 2.35 simplifies to $R_{tl} / 2Z_{loaded}$. As it is seen, the loss is inversely proportional to the loaded line impedance. The bridge itself also adds a loss which is due to the $R_B$ value and can be expressed as:

$$\alpha_{Bridge} = \frac{R_B Z_{loaded} \omega^2 C_B}{2} \tag{2.36}$$

The transmission line loss and the bridge loss together form the overall loss per section of a DMTL:

$$\alpha_{loaded} = \frac{R_{tl}}{2Z_{loaded}} + \frac{R_B Z_{loaded} \omega^2 C_B}{2} \tag{2.37}$$

### 2.3.1. DMTL Phase Shifters

A distributed line phase shifter consists of a high impedance ≥ 50 Ω, line which is loaded by the periodic placement of capacitors. By actuating the switches, their height changes, which directly changes the capacitance and the phase velocity. This phase velocity change satisfies a phase shift, which is the main idea behind DMTL phase shifters. The phase shift per unit length in DMTL phase shifters is found as:

$$\Delta\phi = \beta_1 - \beta_2 = \omega\left(\frac{1}{v_1} - \frac{1}{v_2}\right) = \frac{\omega Z_O \sqrt{\varepsilon_{eff}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right) \text{rad/m} \tag{2.38}$$

where, $\varepsilon_{eff}$ is the effective permittivity of the unloaded line formulated in (2.1), $Z_{lu}$ and $Z_{ld}$ represents the loaded line impedances for up and down-states of the bridges, respectively, and $v_1$ and $v_2$ accounts for the phase velocities of up and down-states. Although this equation gives the phase shift amount, this quantity is not enough to decide the performance of a DMTL phase shifter. A commonly excepted performance criterion for DMTL phase shifters is the ratio of the phase shift to the insertion loss. This criterion was first introduced by Rodwell et al. [40]-[41] and Nagra et al. [42].

Since the amount of the phase shift is formulated, what is left for the evaluation of the degree/dB performance is the loss. The loaded line loss is inversely proportional to the characteristic impedance of line as explained in the previous section. By using (2.39), which is the open form of (2.8), the unloaded line loss can be calculated and (2.46)can be used as the relation between the unloaded line loss and loaded line loss. With the defined equations for the loss and the phase shift, it is possible to find the degree/dB performance of a DMTL phase shifter.

$$\alpha_{unloaded} = \beta \frac{8.686\times10^{-2} R_S \sqrt{\varepsilon_{r,eff}}}{4\eta_0 GK(k)K(k')(1-k^2)} \times \frac{2K}{W} \times \left( \pi + \ln\left( \frac{4\pi W(1-k)}{t(1+k)} \right) \right) + 2\left( \pi + \ln\left( \frac{4\pi S(1-k)}{t(1+k)} \right) \right) \text{ dB/cm} \tag{2.39}$$

$$Z_{loaded} Z_{unloaded} = \alpha_{loaded} \alpha_{unloaded} \tag{2.40}$$

The performance optimization can be extended by following the method in [43]. The main principle behind this method depends on relating the input reflection coefficient to the loaded line impedance of the DMTL structure, as will be explained next.

The input impedance of a terminated lossless transmission line (Figure 2.8) is given by [44] as:

$$Z_{in} = Z_{loaded} \frac{Z_T + jZ_{loaded} \tan\beta\ell}{Z_{loaded} + jZ_T \tan\beta\ell} \tag{2.41}$$

Where, $Z_T$ is the termination impedance and $\ell$ is the length of the DMTL. Hayden [43] uses quarter wavelength DMTLs ( $\ell = \lambda / 4$ ) in the rest of the analysis; however

in this thesis study the length will be left as a parameter. Input reflection coefficient and the return loss are defined as:

$$\Gamma_{in} = \frac{Z_{in} - Z_S}{Z_{in} + Z_S} \qquad RL = 20\log(\Gamma_{in}) \tag{2.42}$$

The relation between the input impedance and the return loss (*RL*) is obtained by combining (2.41) and (2.42) as:

$$Z_{in} = Z_S \frac{1+10^{RL/20}}{1-10^{RL/20}} = Z_{loaded} \frac{Z_T + jZ_{loaded}\tan\beta\ell}{Z_{loaded} + jZ_T\tan\beta\ell} \tag{2.43}$$

In a 50 Ω system, such as $Z_T$=$Z_S$=50 Ω, (2.43) reduces into:

$$50\frac{1+10^{RL/20}}{1-10^{RL/20}} = Z_{loaded} \frac{50 + jZ_{loaded}\tan\beta\ell}{Z_{loaded} + j50\tan\beta\ell} \tag{2.44}$$

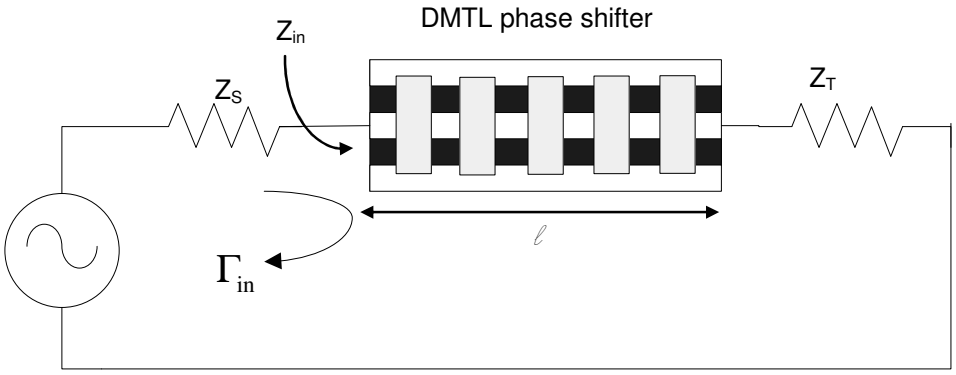



Figure 2.8 A DMTL phase shifter placed in a terminated circuit system.

The positive root of (2.44) is found to be:

$$Z_{loaded} = \frac{j50}{\tan\beta\ell(10^{RL/20}-1)}\left(10^{RL/20} + \sqrt{10^{RL/10} + (\tan\beta\ell)^2\left(10^{RL/10}-1\right)}\right) \qquad (2.45)$$

To illustrate the use of this formulation, a specific case can be examined. For instance, when the maximum return loss is selected to be -30 dB and the length is selected as 4 mm, which is 0.67 guided wavelength at 30 GHz, the loaded line impedance is evaluated as $51.6\,\Omega$. For a DMTL phase shifter, there are two states, namely up and down-states. The relation between the loaded line impedance of these states in a 50 $\Omega$ system can be chosen as:

$$(50)^2 = Z_{lu}Z_{ld} \qquad (2.46)$$

Therefore, if the upstate impedance is found as 51.6 $\Omega$ for the above example, then from (2.46), the down-state impedance should be 48.5 $\Omega$. For these values, the input reflection coefficient is 0.031. If the maximum return loss is selected to be -15 dB instead of -30 dB, then the up and down-state characteristic impedances will be 59.5 and 42.1 $\Omega$ respectively, and the reflection coefficient will be 0.1778. Since the difference between the loaded line impedances is larger in the second case, the amount of phase shift will also be larger. However, the main drawback of this situation is the increase in the reflection coefficient.

# CHAPTER III

# DMTL PHASE SHIFTER DESIGN, MODELING AND STRUCTURAL IMPROVEMENT

The implementation of DMTL employs the idea of periodically loading a high-impedance coplanar waveguide (CPW) with reactive loading elements. DMTL's are generally used as phase shifters, which are of great importance in many microwave applications. This thesis mainly studies the performance improvement of DMTL phase shifters. In this chapter, beside performance improvement techniques, an innovative DMTL unit section modeling method is introduced. Section 3.1 will give the details of the modeling studies, Section 3.2 will present the optimum DMTL phase shifter design, and Section 3.3 will present the analysis of open-ended stub embedded DMTL phase shifters.

## 3.1. DISTRIBUTED MEMS TRANSMISSION LINE MODELING

Accurate modeling of DMTL is beneficial in order to reduce the computational time and efforts. The most common and applicable model for unit DMTL is the fundamental *CLR* model where the suspended bridge structure is simply represented as a shunt capacitance to ground, which loads the high impedance transmission line [45] as Figure 3.1 shows and CHAPTER II explains (b). The major claim of the *CLR* model is its ability to represent all the DMTL unit sections, without a limitation on the dimensions of the structures. However, the *CLR* model is discussed to be capable of modeling up to a bridge width of 50 μm and a new modeling approach has been proposed in order to span all the bridge widths [29]. This approach models the

DMTL unit section as two high impedance transmission lines and a low impedance transmission line in between, where the discontinuities are represented as capacitors and inductors as shown in Figure 3.1 (c). Although this approach works well, there is a main drawback that analytical expressions for capacitor and inductor values can not be obtained, limiting the practical usage of the model. In other words, the approach is well-suited for analyzing previously simulated or measured structure; however, it can not give an idea about the response of the DMTL structure by just using the proposed circuit model without performing any simulations or measurements. Therefore there is still a requirement for a new approach which is capable of not only analyzing a DMTL but also synthesizing it.

This chapter introduces a new model (HICAPLO model) with analytical expression to completely model and synthesize a DMTL structure. As an improvement to the previously presented modeling approach, the discontinuity inductances are eliminated, which can only be evaluated numerically in the previous approach. The removal of the inductances is compensated by a systematic modification of the length of the high- and low-impedance transmission lines in the circuit model. The remaining parameter is the value of the discontinuity capacitance. This capacitance is calculated by a parallel plate capacitance formulation including fringes.

On the other hand, the reduction of the number of components the degree of freedom of the model. While the scope of the *CLR* model is up to 50 μm bridge width, the model presented in this work deals with DMTLs having bridge width larger than 50 μm. Although, the proposed HICAPLO model shows best operational performance for bridge widths between 50 μm and 100 μm, it is shown that for bridge widths larger than 200 μm, the proposed model still works better than the *CLR* model. To give an idea about the performance of the *CLR* model for bridge widths larger than 50 μm, in Figure 3.3, the S-parameters obtained after the EM simulations and *CLR* modeling of a DMTL structure with bridge width 230 μm and signal line width 225 μm is presented.

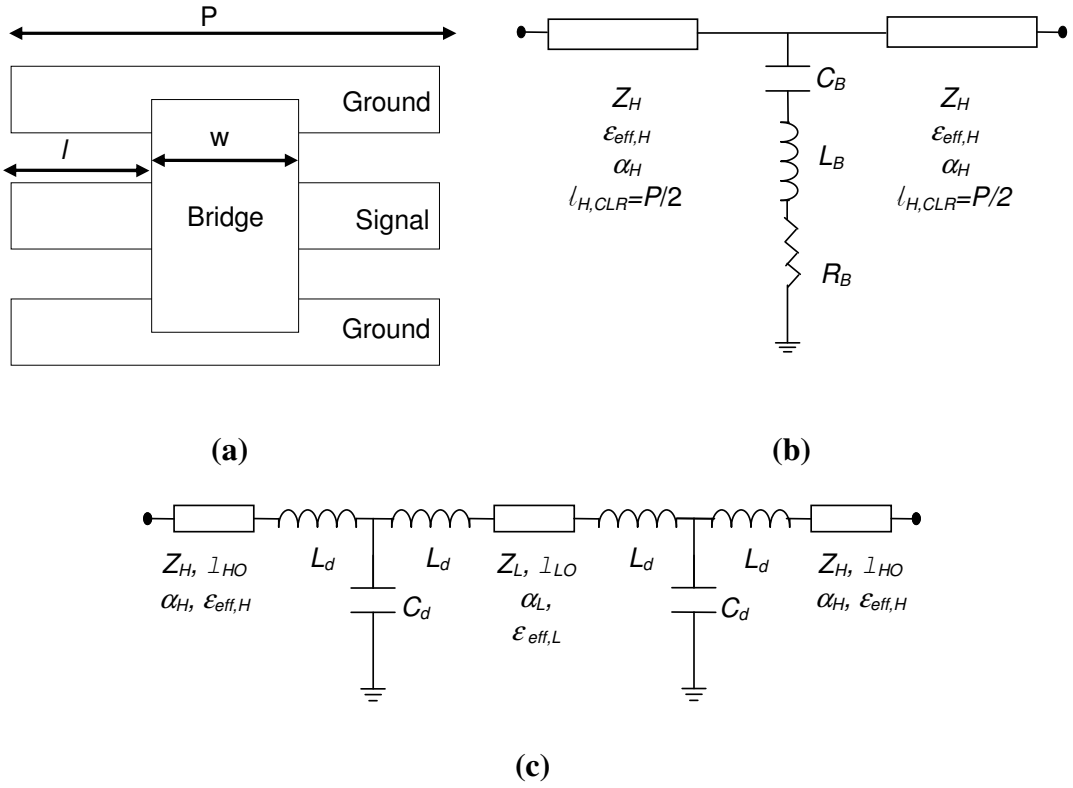



Figure 3.1 (a) Top view of one of the DMTL unit sections, where $w$ >50μm. (b) Lumped-element CLR model of the unit section of DMTL [7].(c) Low-impedance transmission line represented MEMS bridge model of the unit section of DMTL [29]

### 3.1.1. Theoretical Explanation the Proposed HICAPLO Model and Extraction of the Model Parameters

In the *CLR* model, the DMTL unit section is modeled by two short sections of high-impedance transmission lines and a lumped CLR model of the bridge [45] as Figure 3.1 (a) and (b) shows. The transmission line sections are of length $P/2=(w/2) + l$,

where $l$ is the distance from the reference plane to the edge of the MEMS bridge. The *CLR* model is discussed to be valid up to a bridge width of about 50 μm [29]. This means that the transmission line sections can be at most (50/2) + $l$ = 25+$l$ μm long for the CLR circuit model to be valid (Figure 3.2). Therefore, for a structure having a bridge width, $w$, equal to 50 μm, the bridge and the unloaded part of the structure can be modeled by two high-impedance transmission lines of length 25+$l$ μm and the lumped CLR model of a 50 μm long bridge. Next, a structure having a bridge width w larger than 50 μm should be examined. Here,, 50 μm long part of the bridge (25μm from left and 25 μm from right) and the unloaded part of the structure can be modeled by two high-impedance transmission lines of length 25+$l$ μm and the shunt capacitance of a 50 μm long bridge. To model the remaining ($w$-50) μm long loaded part, a low-impedance transmission line is employed in between the high impedance lines. The lumped capacitance representing the 50 μm portion of the bridge is divided into two parts each of which models 25 μm wide bridges. These parts are distributed around the low impedance line. Therefore, the improved model appear to consist of high- and low-impedance transmission lines, and shunt capacitances in between as shown in Figure 3.4.

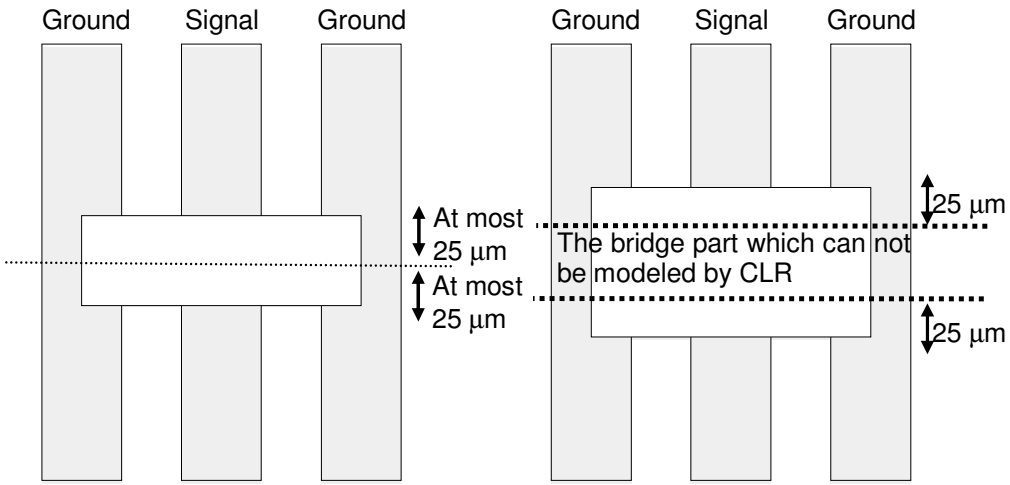



Figure 3.2 Two unit DMTL structures; one with bridge width smaller than 50 μm and the other with bridge width larger then 50 μm.

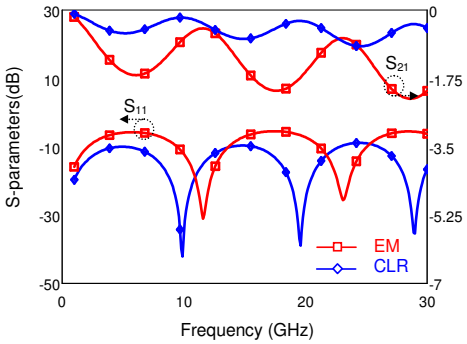



Figure 3.3 (a) S-parameter comparison of HFSS EM simulation and the *CLR* model of a DMTL structure with bridge width 230 and signal line width 225 μm.

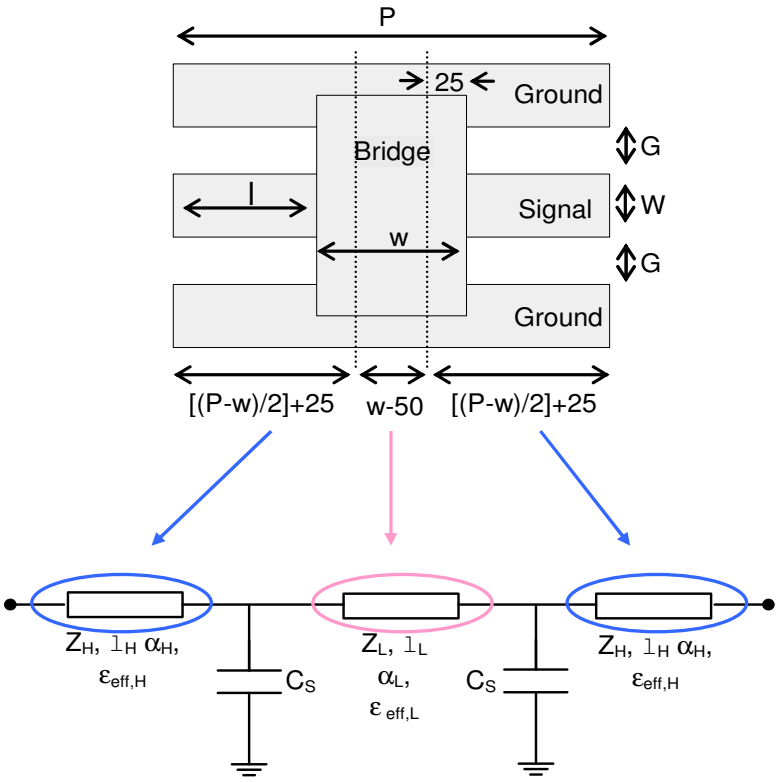



Figure 3.4. The proposed circuit model for the unit DMTL section, where the MEMS bridges are represented by using both low-impedance transmission lines and the *CLR* model.

#### *3.1.1.1. High-impedance and Low-impedance Transmission Line Parameters*

The high-impedance line parameters (characteristic impedance $Z_H$, effective permittivity $\varepsilon_{eff,H}$, line loss $\alpha_H$) are calculated using the CPW formulation in (2.1)-(2.4). For the calculation of the low-impedance line parameters ($Z_L$, $\varepsilon_{eff,L}$) representing the ($w$-50) μm long (where w is the width of the bridge) MEMS bridge, micro-strip line (MS) formulations (2.5)-(2.7) are used. As discussed in CHAPTER II, if the top cover is far away from the bottom plate, CPW with a top cover can be modeled using micro-strip line formulations as a limiting case. For the situation in DMTL case, the bridges can be thought as top covers and again micro strip line assumptions can be followed. However, for this case, $\varepsilon_r$ will be 1 in equation (2.5) since top cover will be closer to the CPW transmission line compared to the bottom plate.

The low-impedance line loss calculated from these formulations is not enough to model the exact loss. Therefore, the low-impedance line loss is not directly evaluated from these equations. Instead, a more detailed way to express low-impedance line loss is introduced in the latter parts of this chapter. However, for the sake of simplicity, until the low-impedance line loss formulation is introduced, a constant value, 100 dB/m will be used as low-impedance line loss for all of the DMTL structures. This simplification is made by considering the average loss needed to represent different low-impedance lines as it will be shown that 100 dB/m is an optimum value for the modeling purpose.

The stated set of equations provide the complete analytical representation of the low- and high impedance transmission line parameters where Table 3.1 and Table 3.2 gives the calculated values for these parameters for different DMTL structures which are designed on Pyrex 7740 glass substrates ($\varepsilon_{r=}$ 4.6, tanδ=0.005 ).

It will be instructive to examine one of the listed structures to better understand the estimation of the model parameters. Type IV, to illustrate has a signal line width, *W* of 80 μm and a length, *P* of 400 μm. The bridge height, *h* in the structure is 2 μm and the bridge width, *w* is 100 μm. To model the basic unit of this DMTL completely, the first requirement is to determine the parts which will be modeled by the *CLR* model and the parts which will use low-impedance transmission line model. In the *CLR* model part, two separate high-impedance transmission lines each having a length of (400-100) ÷ 2 + 25 = 175 μm is constructed. The other parameters of the high-impedance transmission lines are calculated using the CPW formulation in [34 ]. For the low-impedance line, the length, $l_L$, is determined to be *w*-50 μm =50 μm.

The parameters of the low-impedance line are calculated from the micro-strip formulation (2.5)-(2.7) and are listed in Table 3.2 illustrates Two parallel plate capacitances each of which will represent 25 μm long bridges are employed between low- and high-impedance transmission lines. The evaluated parallel plate capacitance including the fringe capacitances is 9.8 fF from (3.2). As previously mentioned, the low-impedance line loss is taken as 100 dB/m. Therefore, all the model parameters are obtained analytically by using the formulations and approximations proposed. In the next sections, the model results will be compared to the EM simulations and measurement results.

Table 3.1 Dimensions, calculated high-impedance line parameters for seven types of DMTL structures, @ 10 GHz, $P$=400 μm, $L$=400μm×20=8000 μm for all structures.

| Type | $G$ (μm) | $W$ (μm) | $h$ (μm) | $w$ (μm) | $Z_H$ (Ω) | $L_H$ (μm) | $\alpha_H$ (dB/m) | $\varepsilon_{eff,H}$ |
|---|---|---|---|---|---|---|---|---|
| I | 80 | 60 | 1.2 | 75 | 94.33 | 187.5 | 28.6 | 2.78 |
| II | 80 | 60 | 2.0 | 75 | 93.47 | 187.5 | 28.6 | 2.78 |
| III | 80 | 60 | 3.0 | 75 | 92.52 | 187.5 | 28.6 | 2.78 |
| IV | 80 | 60 | 2.0 | 100 | 93.47 | 175.0 | 28.6 | 2.78 |
| V | 80 | 60 | 1.2 | 100 | 94.33 | 175.0 | 28.6 | 2.78 |
| VI | 60 | 100 | 1.2 | 100 | 75.02 | 175.0 | 27.9 | 2.78 |
| VII | 70 | 80 | 2.0 | 75 | 82.89 | 187.5 | 27.7 | 2.78 |

Table 3.2 Dimensions, calculated low-impedance line parameters for seven types of DMTL structures, @10GHz, $P$=400 μm, $L$=400μm×20=8000 μm for all structures.

| Type | $G$ (μm) | $W$ (μm) | $h$ (μm) | $w$ (μm) | $Z_L$ (Ω) | $L_L$ (μm) | $\alpha_L$ (dB/cm) | $\varepsilon_{eff,L}$ |
|---|---|---|---|---|---|---|---|---|
| I | 80 | 60 | 1.2 | 75 | 6.95 | 25 | 100 | 1 |
| II | 80 | 60 | 2.0 | 75 | 11.00 | 25 | 100 | 1 |
| III | 80 | 60 | 3.0 | 75 | 15.00 | 25 | 100 | 1 |
| IV | 80 | 60 | 2.0 | 100 | 11.00 | 50 | 100 | 1 |
| V | 80 | 60 | 1.2 | 100 | 6.95 | 50 | 100 | 1 |
| VI | 60 | 100 | 1.2 | 100 | 4.26 | 50 | 100 | 1 |
| VII | 70 | 80 | 2.0 | 75 | 8.45 | 25 | 100 | 1 |

### *3.1.1.2. Parallel Plate Capacitance*

The only remaining parameter in the model is the parallel plate capacitance which models the 25 µm long discontinuity in left and right sides of the bridge. The simple parallel plate capacitance formula in (3.1) is not enough to give accurate results to the exact capacitance value since it does not account for the fringing fields shown in Figure 3.5. Therefore, another formulation in (3.2) is used [46]. The parallel plate capacitances of different DMTL structures are calculated using this formula and listed in Table 3.3.

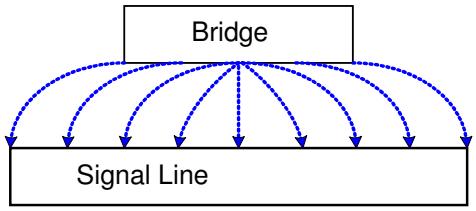



Figure 3.5. The side view of parallel plates and the fringing field in between.

$$C = \varepsilon_0 \frac{wW}{h} \tag{3.1}$$

$$C = \varepsilon_0 \left[ 1.15\left(\frac{wW}{h}\right) + 1.40J\left(\frac{t}{h}\right)^{0.222} + 4.12h\left(\frac{t}{h}\right)^{0.728} \right] \quad , \quad J=2*(W+w) \tag{3.2}$$

Table 3.3 Calculated $C_S$ values for seven types of DMTL structures, @10GHz, P=400 μm, L=400μm×20=8000 μm for all structures.

| Type | I | II | III | IV | V | VI | VII |
|---|---|---|---|---|---|---|---|
| $C_S$ (fF) | 14.87 | 9.80 | 7.30 | 9.80 | 14.87 | 24.34 | 12.80 |

One point to mention which will make the capacitance evaluation process clear is that, for types II and IV the evaluated capacitance values are same. If these two structures are observed, it will be noticed that their signal line width and bridge height are same. The difference in bridge widths is not important because what $C_S$ denote is the parallel plate capacitance between a 25 μm long bridge and the signal line, where the signal line width, $W$ and the bridge height, h are parameters. Since these two parameters are same in type II and type IV DMTL structures, $C_S$ is evaluated to be same.

### 3.1.2. Comparison of the Proposed HICAPLO Model and the *CLR* Model with the Simulations

The structures defined in Table 3.1 have been simulated using Ansoft HFSS v9.2™ in order to verify the validity of the calculated parameters and the model. The simulations were done for different periodic loading distances, $P$ in order to verify the periodicity independent behavior of our model. In other words, for each of the structures, not only $L$= 400×20=8000 μm (P=400 μm) long DMTLs with the same number of bridges are simulated but 4000 μm, 12000 μm, 20000μm long DMTL's are also simulated as shown in Figure 3.6. For each of these DMTL structures, corresponding four models are introduced. These models differ from each other in only high-impedance transmission line length, $L_H$ where all the other parameters are same. While forming the models all of the parameters are calculated except the parallel capacitance value which is left as a free variable. The model characteristics (S-parameters) are then fit to the EM simulation results obtained by

HFSS in the mean square error sense. Since the bridge capacitance, $C_S$ is not expected to depend on the loading periodicity; the mean square error is calculated considering all different loading periodicities.

In Table 3.4 the values of the shunt capacitance, these optimized and these calculated by using equation (3.2) for different DMTL structures are given. The results show that equation (3.2) is quite accurate. From the table, we can notice that Type IV has the worst matching between the calculated and the optimized values. Therefore, it will be beneficial to analyze Type IV as worst case. Figure 3.7 shows the return loss and insertion loss characteristics of Type IV structure for four different periodicities, where all of the model parameters are calculated from the formulations.

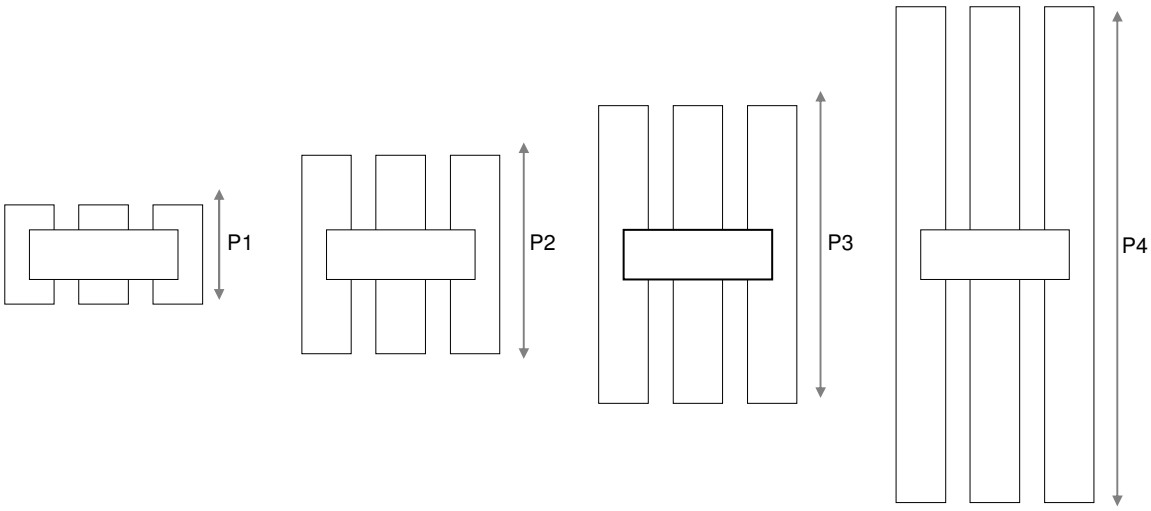



Figure 3.6. Different loading periodicities of a sample DMTL structure, where P1=200 μm, P2=400 μm, P3=600 μm, P4=1000 μm.

Table 3.4 The optimized and the calculated values of the shunt capacitance for different DMTL structures.

| **Type** | $C_S$ calculated by (3.2) (fF) | $C_S$ optimized for 200, 400, 600 and 1000 um periodicities (fF) | % Error between the calculated ad optimized value |
|---|---|---|---|
| I | 14.87 | 15.00 | 0.87 |
| II | 9.80 | 9.87 | 0.71 |
| III | 7.30 | 7.00 | 4.29 |
| IV | 9.80 | 10.40 | 5.77 |
| V | 14.87 | 15.15 | 1.85 |
| VI | 24.34 | 25.05 | 2.83 |
| VII | 12.80 | 12.20 | 4.92 |

As one can observe from the return loss and insertion loss characteristics, the *CLR* model is not suitable for any of the periodicities. On the other hand the proposed HICAPLO model is capable of modeling with the model parameter values determined from the formulations. This situation is valid for the other types of DMTL structures. To give an idea, Figure 3.8 (a-b-c-d-e-f) reveals the characteristics for different structures with different periodicities obtained after EM simulations, the *CLR* modeling, and proposed circuit modeling. In these figures, it is possible to observe that, the proposed model does not only give accurate results for S parameter magnitudes, but it also works for Z-parameter and $S_{21}$ phase approximation.

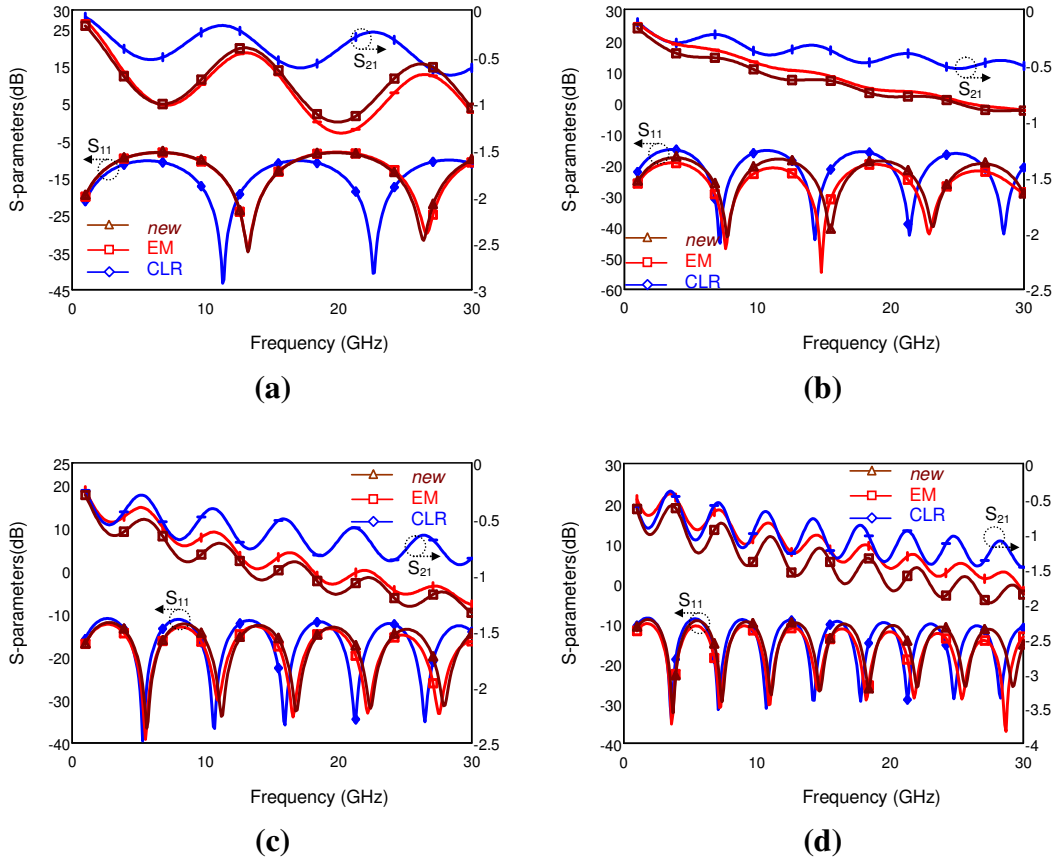



Figure 3.7. **(a)** EM and circuit simulation results for DMTL Type IV , where periodicity is 200 µm, **(b)** periodicity is 400 µm, **(c)** periodicity is 600 µm, and **(d)** periodicity is 1000 µm.

A better way to compare the performances of *CLR* and the proposed model is to use mean square error graphs, which are based on the expected value of the square of the error. Figure 3.9 shows the mean square error plots of the S-parameters of the *CLR* model and the proposed HICAPLO model, when compared with the simulations. It can be seen that the *CLR* model has a worst case mean square error between 0.1 and 0.8 for all types, while the proposed model has a worst case mean square error between 0.005 and 0.035 for all types, which shows that the performance of the HICAPLO model is much better than the *CLR* model.

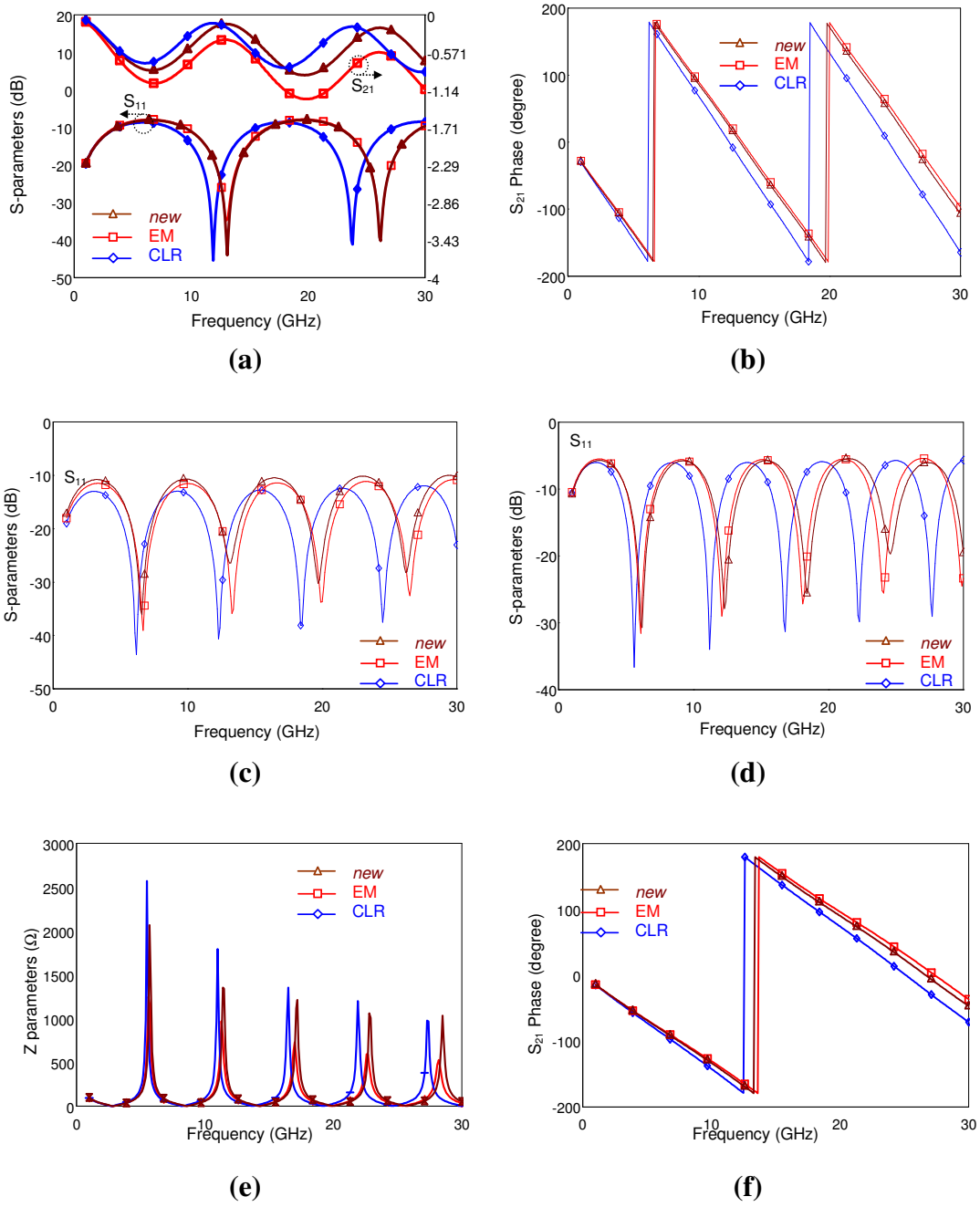
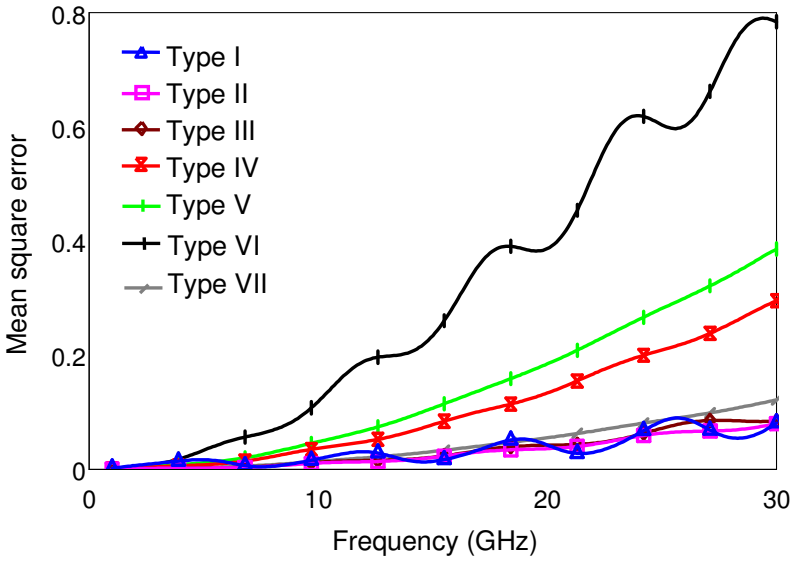
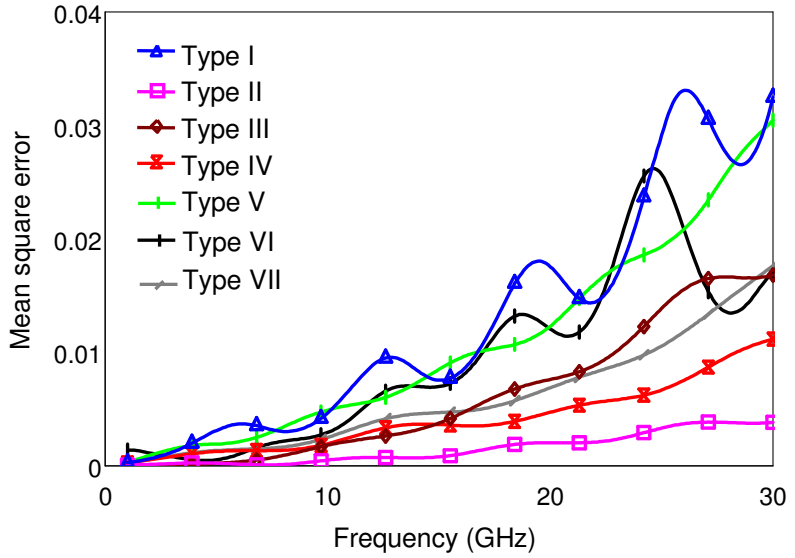



Figure 3.8. (a) EM and circuit simulation results for: DMTL Type VII, where periodicity is 200 µm (b) DMTL Type V, where periodicity is 400 µm, (c) DMTL Type V, where periodicity is 400 µm, (d) DMTL Type VI, where periodicity is 400 µm (e) DMTL Type VII, where periodicity is 600 µm, (f) DMTL Type II, where periodicity is 400 µm.




**(a)**




**(b)**

Figure 3.9 (a) Mean square error between the *CLR* model and simulation results **(b)** mean square error between the proposed HICAPLO model and simulation results.

### 3.1.3. Low-impedance Line Loss Formulation

In the proposed HICAPLO model, for the sake of simplicity, the loss of the low-impedance line is taken as 100 dB/m for all the structures, which is an approximate value. Although using this value is enough for modeling all the structures, for more advanced studies it is better to use loss values closer to the exact values.

The various simulation results enable us to formulate the low-impedance line loss by making appropriate approximations. To reach a final formulation, a number of steps are followed which basically depends on the idea of fitting the simulation data to the model response. The first step is to leave the low-impedance line loss as variable while keeping all the parameters as calculated by (2.1)-(2.7) and (3.2) fixed. Since the low-impedance line loss is reserved as variable it is tuned until return loss and insertion loss characteristics match between simulation and model results. The comparison and tuning is repeated for different signal widths, $W$, and bridge widths, w, while keeping $K=W+2G=220$ μm constant. Thus, the low-impedance line loss in the model is extracted for different structures. Figure 3.10 shows the extracted loss versus bridge width, $w$, for different signal line widths, W. In Figure 3.10 (a), in addition to the data points, fitted third order polynomials are also shown as dashed curves. The variation of line loss with bridge width suggests that a third order polynomial in the form:

$$\text{Loss} = A_3(W)\times w^3 + A_2(W)\times w^2 + A_1(W)\times w + A_0(W),$$

can be used to approximate the loss, where bridge width is the variable. The coefficients of the polynomial are named as $A_n(W)$, $n\in\{0,1,2,3\}$. On the other hand $A_n(W)$ itself can be approximated by a 3rd order polynomial in $W$ as:

$$A_n = F_3\times W^3 + F_2\times W^2 + F_1\times W + F_0.$$

The coefficients of $A_n(W)$ approximation, F, are obtained by considering the Loss approximation for different W values. The approximated F coefficients are listed in Table 3.5.

Table 3.5 $A_n(W)$ coefficients used in Loss formulation.

| | F3 | F2 | F1 | F0 |
|---|---|---|---|---|
| $A_3$ coefficients | -2.15E-09 | 6.16E-07 | -5.74E-05 | 1.64E-03 |
| $A_2$ coefficients | 9.43E-07 | -2.71E-04 | 2.51E-02 | -7.06E-01 |
| $A_1$ coefficients | -1.35E-04 | 3.85E-02 | -3.52E+00 | 9.65E+01 |
| $A_0$ coefficients | 6.43E-03 | -1.80E+00 | 1.60E+02 | -4.11E+03 |

With these approximations, it is now possible to calculate the loss of the low-impedance transmission line of a structure whose $K=W+2G$ width is 220 µm. Now the issue is to generalize this equation, so that it can be used for all $K$ values. Now, if $W$=100 µm is selected as constant and extracted loss values versus bridge widths for different $K$ values are plotted, the graph shown in Figure 3.10 (b) is obtained.

To express the low-impedance line loss of the DMTL structures for K values different then 220 µm, first the bottom points of the graphs shown in Figure 3.10 (b) are shifted to a specific location, as shown in Figure 3.10 (c), to be able to determine the extra loss needed to model the loss for other K values. This specific location is the bottom point of $K$=220 µm plot in Figure 3.10 (b). In other words, it is assumed that the low-impedance line loss is known for a specific bridge width for $K$=220 µm and from Figure 3.10 (c) the extra loss needed to determine the loss for the same bridge width for another K value is determined. The extra loss is plotted with respect to different K values in Figure 3.10 (d) for different signal line widths. Using these figures, the extra loss needed is approximated as:

$$\text{Extra Loss} = L_3(W_s)\times K^3 + L_2(W_s)\times K^2 + L_1(W_s)\times K + L_0(W_s)$$

where, $L_n = M_3\times W_s^3 + M_2\times W_s^2 + M_1\times W_s + M_0$ and $W_s$ is the shifted signal line width values and $M_3$ coefficients are as shown in Table 3.6.

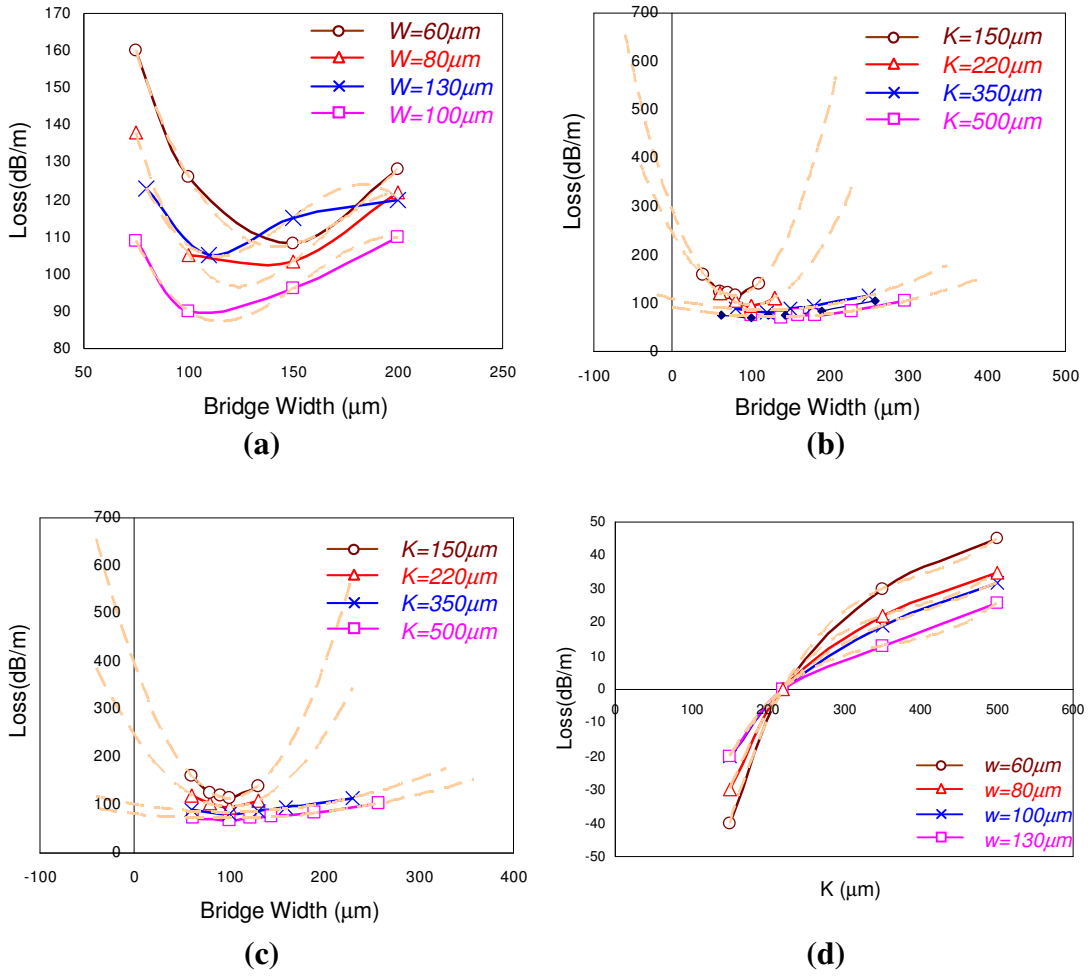



Figure 3.10 (a) Extracted loss versus bridge width, w, for different signal line widths, W. (b) Extracted loss values versus bridge widths for different K values. (c) Shifted extracted loss values versus bridge widths for different K values. (d) Extra loss plotted with respect to different K values for different signal line widths.

The estimated loss formulations are simulated using MATLAB. As an example, low-impedance line loss for *K*=500 µm case is investigated. In Figure 3.11 (a) the low-impedance line loss calculated for different *W* and *w* values are shown when *K*=220 µm. In Figure 3.11 (b) the extra loss needed to calculated loss for *K*=500 µm case is presented again for the same W and w values. Finally, in Figure 3.11 (c), the overall low-impedance line loss calculated for *K*=500 µm case is shown. As a second example in Figure 3.11 (d) the overall low-impedance line loss calculated for *K*=150 µm case is shown.

Table 3.6 M coefficients used in the extra loss formulation.

| | $M_5$ | $M_4$ | $M_3$ | $M_2$ | $M_1$ | $M_0$ |
|---|---|---|---|---|---|---|
| $L_3$ | -3.28E-15 | 2.43E-12 | -6.85E-10 | 9.15E-08 | -5.77E-06 | 1.39E-04 |
| $L_2$ | 3.19E-12 | -2.38E-09 | 6.77E-07 | -9.13E-05 | 5.83E-03 | -1.43E-01 |
| $L_1$ | -9.25E-10 | 7.00E-07 | -2.02E-04 | 2.78E-02 | -1.82E+00 | 4.59E+01 |
| $L_0$ | 8.39E-08 | -6.46E-05 | 1.90E-02 | -2.67E+00 | 1.78E+02 | -4.66E+03 |

The HICAPLO model, including the low-impedance line loss approximations evaluated by MATLAB, is investigated for different structures. To give an idea, simulation and model comparisons for K=150, K=220 µm, K=300 µm and K=500 µm cases are presented in Figure 3.12. Here, it should be noticed that model $S_{21}$ parameters show a great matching with the simulations as well as model $S_{11}$ parameters. Moreover, in this figure, beside the proposed HICAPLO model and EM simulations, the CLR model is also presented and the advantage of the proposed model is highlighted. Figure 3.12 (a)-(b) can be also examined in order to make a comparison of proposed model and the *CLR* model for bridge widths larger than 100 µm. Here, bridge width is 230 µm and although it is above the best operational performance range, the proposed model still gives a much better approximation of the DMTL structure than the *CLR* model.

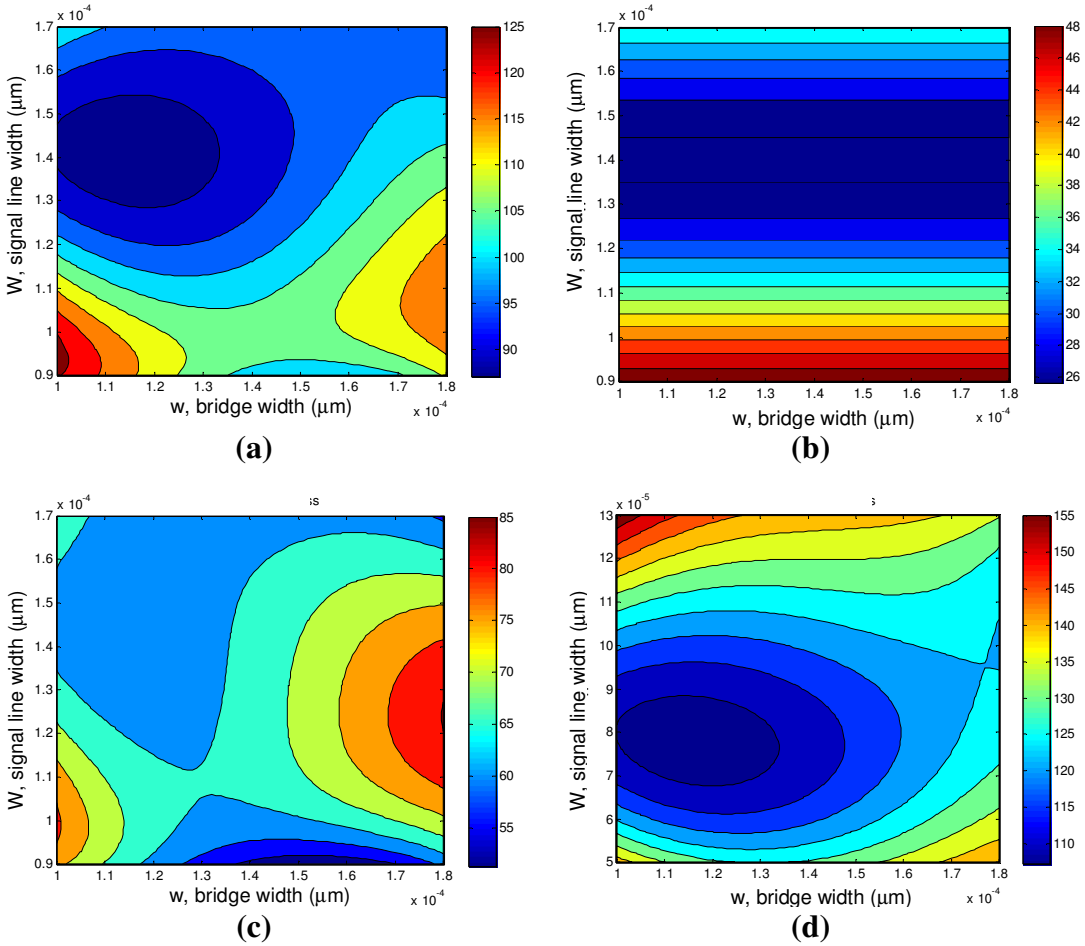



Figure 3.11 (a) Low-impedance line loss distribution for K=220 µm (b) Loss difference between K=220 µm case and K=500 µm case (c) Low-impedance line loss distribution for K=500 µm (d) Low-impedance line loss distribution for K=150 µm.

This section presented a complete modeling study on DMTL structures which have bridge widths larger than 50 µm. The model proposed HICAPLO model in this study consists of high-impedance transmission lines, shunt capacitances and a low-impedance transmission line in between. The main idea behind this model is the conclusion reached in [29] that CLR can model bridge widths of at most 50 µm. Although the approach discussed in [29] suggest a model which has many undetermined parameters such as series inductors and shunt capacitors, the proposed model in this paper decreases the number of unknowns by eliminating the series inductances and gives approximate analytical expressions for the remaining

parameters. One of the most important studies in this paper is the formulation of low-impedance line loss parameter, which plays an extremely significant role in overall loss calculation. The HICAPLO model is compared with CLR and it is observed that while CLR can not fit the simulation results, the proposed model gives very close results.

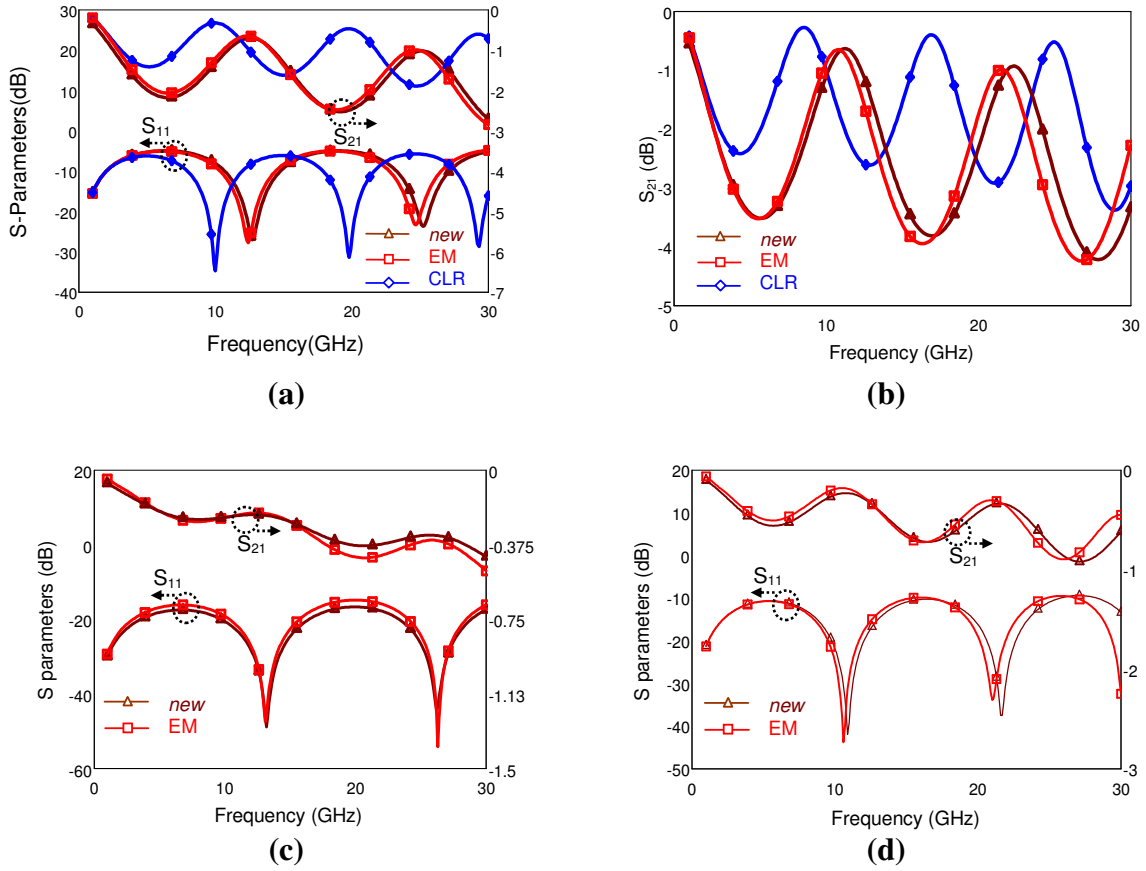



Figure 3.12 (a) EM and circuit simulation results for DMTL structure with signal line width, $W$=180 µm, $G$=20 µm, $w$=180 µm, $h$=1.7 µm and periodicity, P, is 400 µm, (b) for DMTL structure with signal line width, $W$=160 µm, $G$=30 µm $w$=180 µm, $h$=1.7 µm and P=400 µm (c) for DMTL structure with signal line width, $W$=120 µm, $G$=90 µm, $w$=75 µm, $h$=1.7 µm and P=400 µm, (d) for DMTL structure with signal line width, $W$=160 µm, $G$=170 µm, $w$=100 µm, $h$=1.7 µm and P=400 µm.

## 3.2. OPTIMUM DMTL PHASE SHIFTER DESIGN USING THE PROPOSED HICAPLO MODEL

As explained in Chapter II, DMTL structures are used can be continuous phase shifters by changing the loading parallel plate capacitance value when the height of the bridges over the signal lines are changed. Usually, it is possible to get large phase shift amounts by DMTL phase shifters, since the parallel plate capacitance is a parameter which can be altered easily. On the other hand, it is not enough to consider the amount of phase shift alone to determine the performance of a DMTL phase shifter, [27]. A better figure of merit that defines the quality of a phase shifter is te phase shift obtained per one decibel loss.

In general it can be said that, the phase shift will increase when the overall parallel plate capacitance, which is formed between signal line and bridge, is increased. This idea leads to a belief that when the parameters those are directly proportional with $C_b$ are increased, the capacitance value, therefore degree/dB performance will also increase. In this section it will be shown that the situation is quite different from this common belief. In addition, it will be exposed that the degree/dB performance has peaks for some bridge widths and signal line widths. Moreover, an innovative way which uses ABCD and S-parameters to express the phase shift per one decibel loss will be introduced. The final study of this section will be the design of an optimum phase shifter, which maximizes the degree/dB performance. This optimum phase shifter is selected among the structures with $2G+W$=220 μm, when the bridge height is decreased from 2 to 1.7 μm.

### 3.2.1. Effect of Model Parameters on the degree/dB Performance

The signal line width, *W*, bridge height, h and bridge width, *w* are the key parameters which define the parallel plate capacitance (3.1). Therefore, the phase shift amount will show variance with these parameters. It is obvious that when the difference between the bridge heights of the two positions of the bridge is large, the phase shift will be correspondingly large. Now, the issue is to determine the effect of *W* and *w* when the bridge height difference is kept constant.

To examine the dependence of the degree/dB performance on the bridge width, the simulation results of the DMTL structures defined in Table 3.7 are examined. For each structure, the height of the bridge is reduced with a different ratio and the resulting degree/dB performances for different frequencies are shown in Figure 3.13 . The phase shift amount is evaluated by comparing the $S_{21}$ phase of both states, where the loss is taken as the average insertion loss when the DMTL is loaded with matched loads. The degree/db performance is found by dividing the phase shift amount by the loss.

Table 3.7 Dimensions of four types of DMTL structures designed on Pyrex 7740 glass substrates, $H$=500 μm ($\varepsilon_r$= 4.6, tanδ=0.005 ).

| **Type** | $W$ (μm) | $W+2G$ (μm) | $P$ (μm) | $L$ (μm) | $h_{up}$ (μm) | $h_{down}$ (μm) |
|---|---|---|---|---|---|---|
| I | 60 | 220 | 400 | 8000 | 1.7 | 1.2 |
| II | 80 | 220 | 400 | 8000 | 2 | 1.2 |
| III | 100 | 220 | 400 | 8000 | 2 | 1.7 |
| IV | 100 | 500 | 200 | 4000 | 2 | 1.7 |

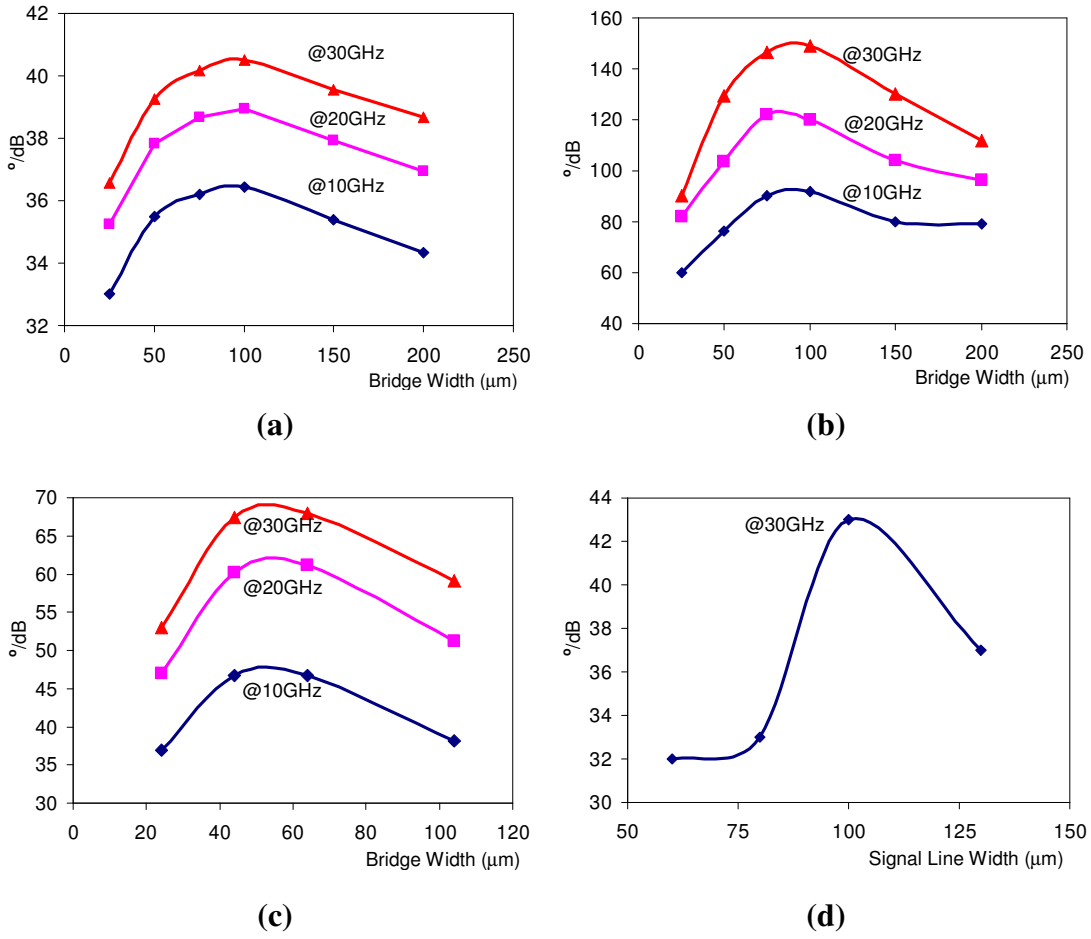



Figure 3.13. **(a)** degree/dB performance for Type I DMTL when *h* is changed from 1.7 to 1.2 µm**, (b)** Type III DMTL when *h* is changed from 2 to 1.2 µm**,(c)** Type IV DMTL when *h* is changed from 2 to 1.7 µm**, (d)** degree/dB performance variation for different signal line widths, where *K*=220 µm and *w*= 75 µm.

As the graphs indicate, degree/dB performances have some peak points at different bridge width values for different structures. As an example, for Type I structure the maximum degree/dB value is obtained for *w*=100 µm when h is changed from 1.7 to 1.2 µm. From Table 3.8, on the other hand, it is observed that with increasing bridge width, the percent change in capacitance value increases, which brings a rise in phase shift amount. Therefore, the reason for the drop in the degree/dB performance

beyond $w$=100 μm is the increase of loss in those regions. This fact implies that loss should be clearly defined in order to make acceptable observations on degree/dB performances.

Table 3.8 The capacitance values and the percent capacitance changes of Type I DMTL phase shifter for different bridge widths.

| Bridge width, $w$ (μm) | Capacitance when bridge height, $h_{down}$ is 1.2 μm (fF) | Capacitance when bridge height, $h_{up}$ is 1.7 μm (fF) | Percent Change in Capacitance Value (%) |
|---|---|---|---|
| 25 | 24.7 | 18.24 | 35.4 |
| 50 | 46.6 | 33.9 | 37.5 |
| 75 | 68.5 | 49.5 | 38.4 |
| 100 | 90.4 | 65.1 | 38.9 |
| 150 | 134.2 | 96.3 | 39.4 |
| 200 | 178 | 127.5 | 39.6 |

The previous studies, which aim to present expressions for both phase shift per unit length and loss for the loaded line per unit length, use the definitions introduced in [27]. The phase shift per unit length is found from the change in the phase constant as:

$$\Delta\phi = \beta_1 - \beta_2 = \omega\left(\frac{1}{v_1} - \frac{1}{v_2}\right) = \frac{\omega Z_O \sqrt{\varepsilon_{r,eff}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right) \text{ rad/m} \qquad (3.3)$$

where $Z_{lu}$ is the upstate (low bridge capacitance state) DMTL matching impedance and $Z_{ld}$ is the down state (high bridge capacitance state) DMTL matching impedance.

From this equation, it can be concluded that phase shift will increase when the difference between $Z_{ld}$ and $Z_{lu}$ gets higher. On the other hand, for large impedance difference, higher capacitive ratio is required, which results in an increase in the reflection coefficient of DMTL. Again in [27], the transmission line loss for unloaded CPW is defined as:

$$\alpha = \frac{8.686\times10^{-2} R_S \sqrt{\varepsilon_{r,eff}}}{4\eta_0 K K(k) K(k')(1-k^2)} \times \frac{2K}{W}\left(\pi + \ln\left(\frac{4\pi W(1-k)}{t(1+k)}\right)\right) + 2\left(\pi + \ln\left(\frac{4\pi S(1-k)}{t(1+k)}\right)\right) \text{dB/cm} \quad (3.4)$$

where t is the metal thickness, $R_S$ is the surface resistance given by

$$R_S = \sqrt{\pi f \mu_0 / \sigma}$$

where $\sigma$ is the conductivity of the metal. The loaded line loss, on the other hand is found by multiplying the unloaded line loss by the ratio of unloaded impedance $Z_0$ to the loaded impedance $Z_l$. The results obtained using these formulations are presented in [27]. The first remark made on the use of these equations is that the calculated loss is not enough to model the measured loss and there is a need for a correction factor of 1.4 for the unloaded line and a factor of 1.8 for the loaded line. The second remark which is not mentioned in [27] is that the given equations are not enough to model the phase shift or loss of DMTL structures which have bridge widths larger than 50 μm. To illustrate, the degree/dB performances of the structures defined in Table 3.1 are calculated using equations (3.3)-(3.4) and the results are presented in Table 3.9. As one can observe, although the loss is multiplied by 1.8 as stated in [27], the calculated $^{o}$/dB performance is not enough to model the simulated $^{o}$/dB. Moreover, the calculated values can not even predict the trend of $^{o}$/dB performance with respect to signal line or bridge width. The phase shift and loss calculations

depend on modeling unit DMTL sections by the *CLR* model is also investigated in this table. Here, it is shown that for bridge widths larger than 50 μm, the *CLR* model can not give close degree/dB performance values with the simulated ones, which is an expected situation.

Table 3.9 Dimensions, calculated high-impedance line parameters for seven types of DMTL structures, @ 10 GHz, $P$=400 μm, $L$=400μm×20=8000 μm for all structures.

| $G$ (μm) | $W$ (μm) | $h_{up}$ (μm) | $h_{down}$ (μm) | $w$ (μm) | 1/1.8×°/dB calculated from (3.3)-(3.4) | 1/1.8×°/dB modeled by the *CLR* | °/dB simulated |
|---|---|---|---|---|---|---|---|
| 80 | 60 | 2.0 | 1.7 | 75 | 19 | 21 | 16 |
| 80 | 60 | 2.0 | 1.7 | 100 | 17 | 25 | 17 |
| 60 | 100 | 2.0 | 1.7 | 75 | 15 | 26 | 23 |
| 60 | 100 | 2.0 | 1.7 | 100 | 14 | 31 | 22 |
| 70 | 80 | 2.0 | 1.7 | 75 | 17 | 23 | 20 |
| 70 | 80 | 2.0 | 1.7 | 100 | 16 | 28 | 20 |

### 3.2.2. Application of Proposed DMTL Modeling Approach in Degree/dB performance Calculation

The equations for degree/dB performance extracted using the *CLR* modeling become insufficient when bridge width, $w$ > 50 μm cases are examined as shown in the previous section. However, for most of the structures, the maximum degree/dB performance is achieved for $w$ > 50 μm for a given signal line and bridge height. Therefore, a way to represent degree/dB performance for such structures, is required to design and optimum performance.

The approach used in this study is based on extracting the ABCD parameters of the unit DMTL section. To calculate the phase shift per decibel loss, the overall ABCD parameters of the unit DMTL section which is modeled as shown in Figure 3.14 is found. The ABCD parameters of this unit section is obtained by cascading ABCD parameters of five pieces, namely high impedance transmission line, shunt capacitance, low impedance transmission line, another shunt capacitance and high impedance transmission line. The ABCD parameters of high-low impedance transmission lines and shunt capacitance are given in (3.5)-(3.7) [44]. The explicit expression of $\gamma$ in equation (3.5) is $\gamma=\alpha + j\beta$ , where $\alpha$ and $\beta$ are as in (3.9)-(3.10) [44 ]. For the high impedance line, these quantities and $Z_H$ are easily extracted from known equations. On the other hand, to find the dB/m loss of the low-impedance line and $Z_L$ value, the approximation explained in the modeling section is adopted.

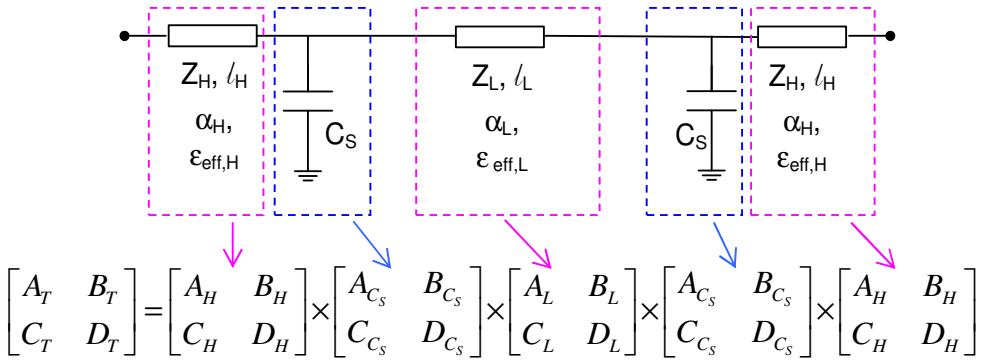



Figure 3.14. The previously proposed HICAPLO model and the overall ABCD parameter representation for the unit DMTL section, where the MEMS bridges are represented by using both low-impedance transmission lines and the CLR model.

$$\begin{bmatrix} A_H & B_H \\ C_H & D_H \end{bmatrix} = \begin{bmatrix} \cosh \gamma_H l_H & Z_H \sinh \gamma_H l_H \\ \dfrac{\sinh \gamma_H l_H}{Z_H} & \cosh \gamma_H l_H \end{bmatrix} \tag{3.5}$$

$$\begin{bmatrix} A_L & B_L \\ C_L & D_L \end{bmatrix} = \begin{bmatrix} \cosh \gamma_L l_L & Z_L \sinh \gamma_L l_L \\ \dfrac{\sinh \gamma_L l_L}{Z_L} & \cosh \gamma_L l_L \end{bmatrix} \tag{3.6}$$

$$\begin{bmatrix} A_{C_S} & B_{C_S} \\ C_{C_S} & D_{C_S} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ jwC_S & 1 \end{bmatrix} \tag{3.7}$$

$$C = \varepsilon_0 \left[ 1.15\left(\frac{wW}{h}\right) + 1.40J\left(\frac{t}{h}\right)^{0.222} + 4.12h\left(\frac{t}{h}\right)^{0.728} \right], \qquad J=2*(W+w) \tag{3.8}$$

$$\alpha = \text{Loss} / 8.686 \tag{3.9}$$

$$\beta = w + \frac{\sqrt{\varepsilon_{eff}}}{c} \tag{3.10}$$

$$S_{11} = \frac{A + B/Z_O - CZ_O - D}{A + B/Z_O + CZ_O + D} \tag{3.11}$$

$$S_{21} = \frac{2}{A + B/Z_O + CZ_O + D} \tag{3.12}$$

Once the [ABCD] $_T$ matrix is obtained, S parameters of the whole system are found from (3.11)-(3.12). Some simplifications are in order. First, since the unit DMTL section is a symmetrical structure $A_T=D_T$ must hold. Next, if we assume that $S_{11}=0$, from (3.11), it is obtained that:

$$Z_O = \sqrt{B/C} \tag{3.13}$$

This equation reduces (3.12) into:

$$S_{21} = \frac{1}{A + \sqrt{BC}} \tag{3.14}$$

Equation (3.14) is enough to find the overall loss and phase shift of a DMTL structure by using the equations (3.5)-(3.10). Of course, this quantity is calculated for both up and down state positions of the switches in the DMTL.

$$loss = \frac{10\log_{10}\left(\left|S_{21,up}\right|\right) + 10\log_{10}\left(\left|S_{21,down}\right|\right)}{2} \text{ rad/m} \tag{3.15}$$

$$phase\ shift = [\text{phase}(S_{21,up}) - \text{phase}(S_{21,down})] \times \frac{180}{\pi} \text{ degree/m} \tag{3.16}$$

Here, what should be noted is that the return loss is eliminated, i.e. exactly matched condition is assumed for both up and downstates which requires different loading of these states. Since this is not possible, the assumption that $S_{11}=0$ does no hold. However, if $Z_{lu}$ and $Z_{ld}$ are both close to $Z_0$, will be a very good approximation. As

long as this assumption holds, (3.15) and (3.16) can be used to obtain the degree/dB figure of merit. Consequently, it becomes possible to predict the degree/dB performance of a DMTL phase shifter without simulating it. Moreover, for a given structure, it will be possible to find the bridge width or signal line width which will satisfy the maximum degree/db performance. To visualize the introduced method, MATLAB is used to compute the defined equations. As an example, $P$=400 µm, $K=W+2G$=220 µm, upstate bridge height, $h_{up}$=2 µm and down state bridge height, $h_{down}$ =1.7 µm case is considered. In Figure 3.15 (a)-(b) degree/dB performance is shown with respect to signal line width W and bridge width w.

Here, the most remarkable result is that degree/dB performance is not directly proportional with the upstate capacitance value, which mostly determines the phase shift amount. Therefore, it is not a proper way to increase the bridge width of a DMTL structure continuously to obtain enhanced degree/dB performance. Every structure has a maximum degree/dB value and this optimum value is obtained at a point where minimum low-impedance line loss gives maximum available phase shift amount. For the example illustrated in Figure 3.15 where K= 220 µm, this optimum point is W=110 µm and w=110 µm point. As it is observed when the bridge width is increased to 160 µm, the low-impedance line loss increases therefore the degree/dB performance gets worse.

To validate the proposed DMTL modeling approach introduced in the previous section and the degree/dB evaluation technique explained in this section, 48 structures, which differ in bridge width and center conductor width, are designed and fabricated. Table 3.10 gives the details of these 48 (1-48) structures, where the bridge heights are not determined and left as a process variable. As it is observed, $K$ is kept constant as 220 µm and the center conductor width is varied. For three different CPW structures, four different periodicities and for each of these four periodicities four different bridge widths are defined. The measurement results of these structures will be presented in the following chapters.

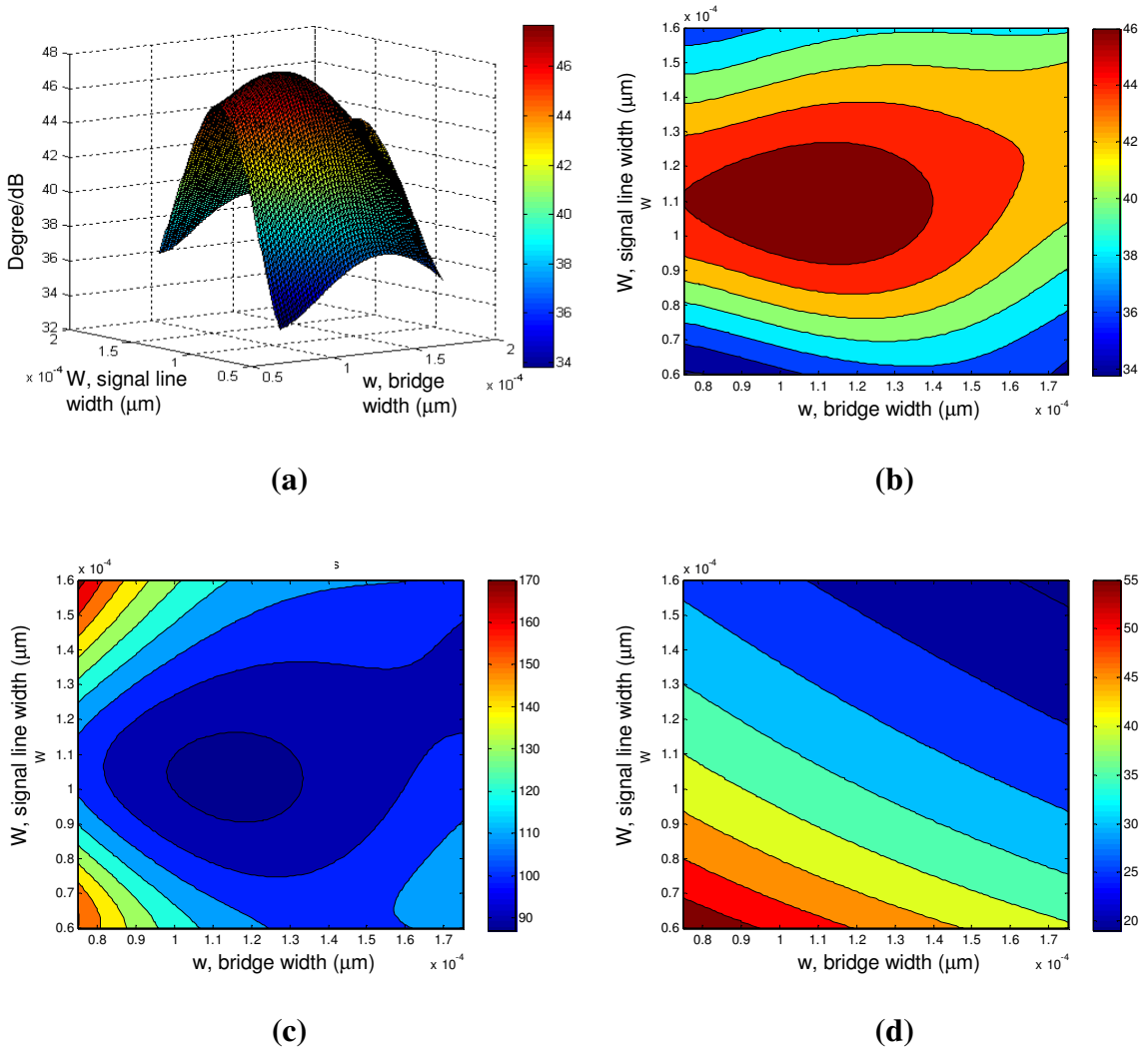



Figure 3.15. (a) 3D degree/dB illustration with respect to *W* and *w,* (b) 2D degree/dB illustration with respect to *W* and *w*, (c) low-impedance line loss, (d) matching impedance.

Table 3.10 Dimensions of the DMTL structures to be fabricated.

| **Type** | **G** (µm) | **W** (µm) | **P** (µm) | **w** (µm) |
|---|---|---|---|---|
| 1-16 | 80 | 60 | 200<br>400<br>600<br>1000 | 25<br>50<br>75<br>1000 |
| 16-32 | 70 | 80 | 200<br>400<br>600<br>1000 | 25<br>50<br>75<br>100 |
| 32-48 | 60 | 100 | 200<br>400<br>600<br>1000 | 25<br>50<br>75<br>1000 |
| 49 | 162 | 176 | 400 | 80 |

### 3.2.3. Optimum Phase Shifter Design using the Introduced Techniuque when K=500 µm.

To check the validity of the proposed technique, a specific example, *K*=500 µm case is investigated when the bridge height is decreased from 2 to 1.7 µm. For this case, from the simulation results with various *W* and *w* combinations, maximum degree/dB is obtained at *W*=176 µm and *w*=80 µm point.

Table 3.11 gives the other dimensions and parameter values of this optimum point. This structure is simulated using HFSS and its circuit model is constructed by the

HICAPLO method proposed in the previous section. Figure 3.16 (a)-(b) show the HFSS simulation results and the model results of this structure when the bridge height is 2 μm and the structure is loaded by 50 Ω. From these figures, it is observed that the proposed model and the simulation results agree well. Figure 3.16 (c) gives the degree/dB plot obtained by using the ABCD parameters and loss approximation, with respect to signal line width *W* and bridge width *w*. From this plot, a satisfying operational performance is observed at the point *W*=176 μm and *w*=80 μm. In fact, for larger bridge width and center conductor width, more degree/db performance seems to be possible. However, as practical limitations are considered, it is be better not to increase the DMTL dimensions that much. Figure 3.16 (d) gives the degree/dB performances of the circuit model and the HFSS simulations, which also show good compatibility. In this figure, what is denoted by loss is the insertion loss, where the return loss is equated to zero by equating $S_{11}$ parameter to zero. From Figure 3.16 .(c), at the position where W=176 μm and w=80 μm the degree/dB performance is predicted as 81 at 20 GHz, which is close with the simulation and model results shown in Figure 3.16 (d).

Table 3.11 Dimensions of the designed optimum DMTL phase shifter when *K*=220 μm, *W*=176 μm, *w*=80 μm, $h_{up}$=2 μm, and $h_{down}$=1.7 μm

| $L_H$ μm | $L_L$ μm | $Z_H$ Ω | $Z_{L\,up}$ Ω | $Z_{L\,down}$ Ω | $\alpha_H$ dB/m | $\alpha_L$ dB/m | $\varepsilon_{eff}$ | $\varepsilon_{eff}$ | $C_{Sup}$ fF | $C_{Sdown}$ fF |
|---|---|---|---|---|---|---|---|---|---|---|
| 185 | 30 | 82 | 4.05 | 3.47 | 41 | 92 | 2.8 | 1 | 78 | 91 |

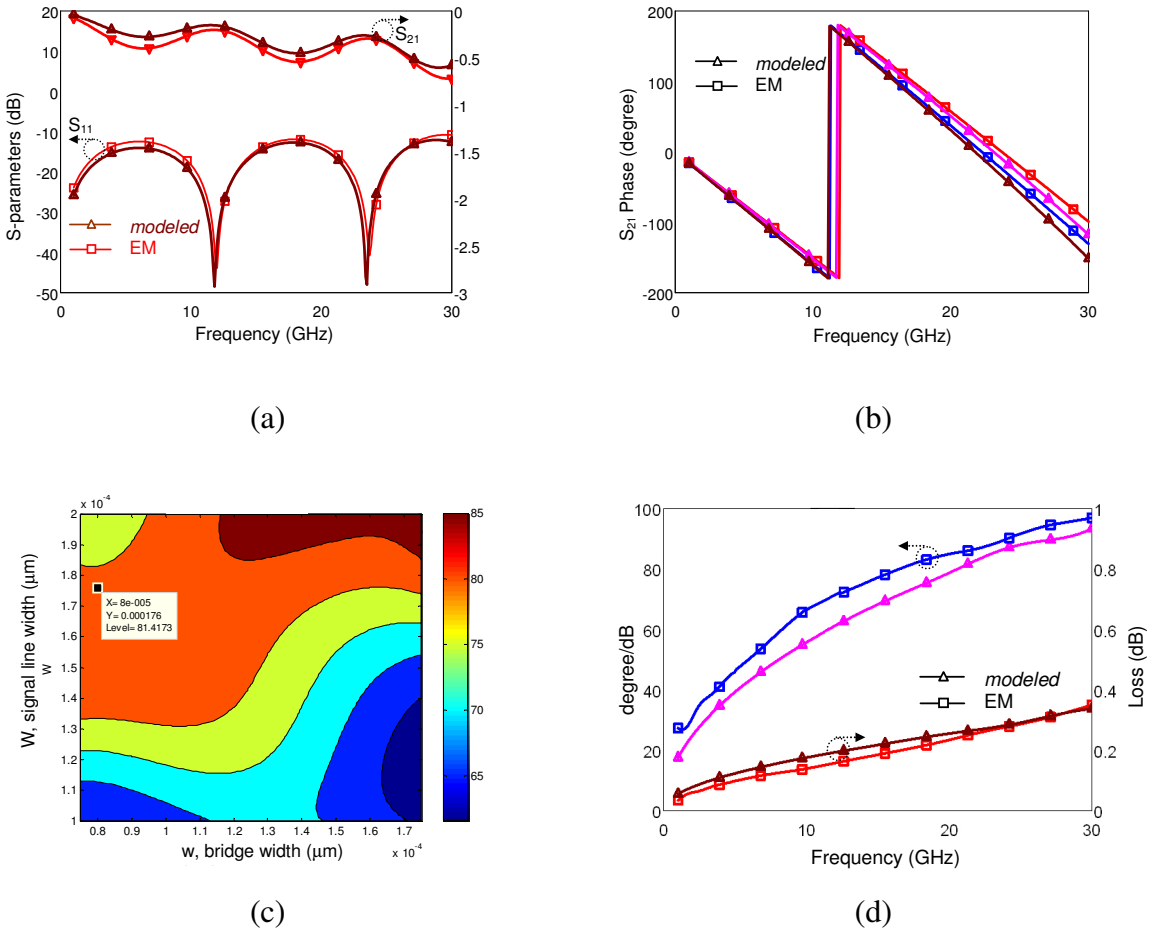



Figure 3.16 (a) up state S parameters (b) down state S parameters (c) S21 phase (d) degree/dB performance.

In addition to the 48 structures designed to verify the proposed DMTL modeling approach, the optimum phase shifter designed to give 81 degree/dB at 20 GHz is fabricated as a 49$^{th}$ structure. However, since the actual heights of the bridges are determined by the fabrication conditions, the optimum point may change after the fabrication, depending on the new up and down-state heights.

## 3.3. INSERTION OF OPEN-ENDED STUB THROUGH THE SIGNAL LINE OF DMTL PHASE SHIFTER

By preserving the standard DMTL topology, the maximum amount of phase shift for a defined bridge height ratio and loss is constant and can not be increased unless the structure geometry is changed. The geometry change should depend on the idea of increasing the difference between up and down state capacitances without increasing the difference in the loaded transmission line impedances. To ensure this condition, open-ended stubs (OES) will be placed through the signal line in this section.

### 3.3.1. Open-Ended CPW Series Stub Overview

Open-ended CPW stubs are formed by inserting interdigital fingers in the center conductor of a CPW transmission line as Figure 3.17 presents, [30]. This configuration is claimed to increase the overall series capacitance of the transmission line. The open-ended stub structure in Figure 3.17 is composed of a series gap through the center conductor and a step change in the center conductor width. Figure 3.18 (a)-(b) shows these discontinuities separately. In Figure 3.18 (a), the center conductor width is exposed to a step change from W to $W_1$. This discontinuity disturbs the original CPW electric and magnetic fields and gives rise to additional reactance [47]-[48]. This reactance can be modeled by lumped elements $L_{11}$, $L_{12}$, and $C_{11}$ as Figure 3.18 (a) shows. On the other hand, the series gap $g_2$ can be modeled as a lumped π-network with two fringing capacitances $C_{21}$ and $C_{22}$ on both sides and a coupling capacitance $C_{23}$ in the middle as Figure 3.18 illustrates [49].

From the foregoing analysis of OES in CPW center conductor part by part, it is possible to reach the final lumped model as Figure 3.19 illustrates, [49]. Here, the fringing capacitances are embedded in $C_{P1}$ and $C_{P2}$ and the step change inductances

are embedded in $L_{S2}$ and $L_{S3}$. $C_S$ is the main component of this model, which stands for the series capacitance added by the stub [50].

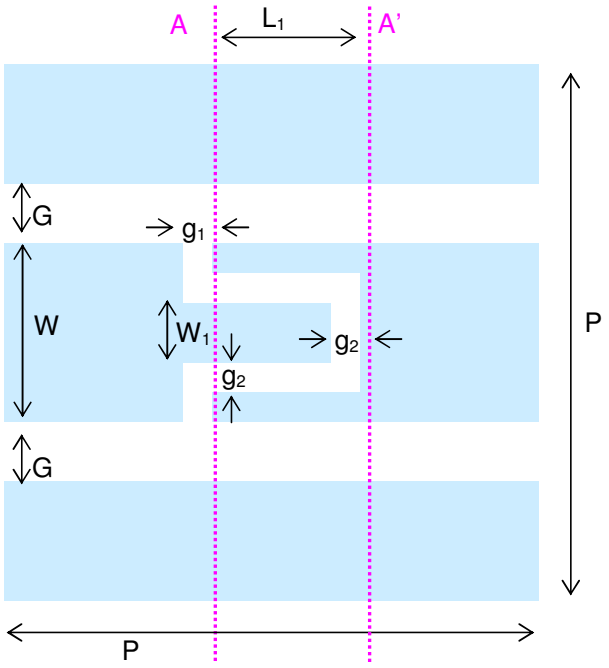



Figure 3.17. Open-End CPW series stub.

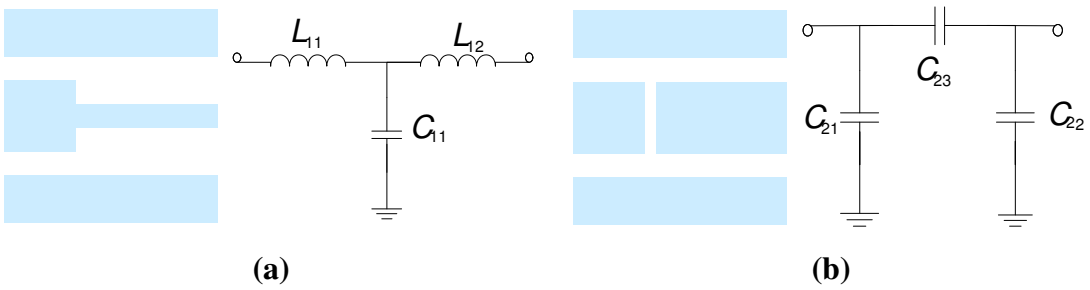



Figure 3.18. (a) Lumped element model of a step change in the width of the center conductor. (b) Lumped element model of a gap in the width of the center conductor.

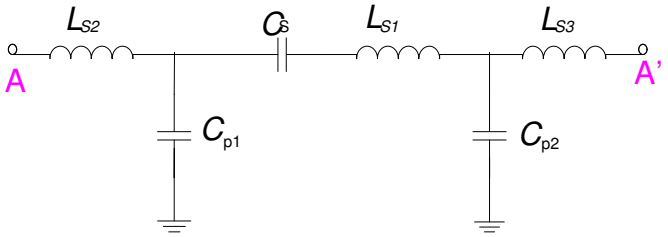



Figure 3.19. Open-End CPW series stub lumped element equivalent circuit model.

The series capacitance denoted by $C_S$ has a linear relation with the total length of the stub, $L_1$. Therefore, it is beneficial to use long stubs to obtain higher capacitances. On the other hand, for the given structure to be used as a series capacitance in the circuit, the periodic loading, $P$, should be less than $0.1\lambda_{g(CPW)}$. The other parameters which $C_S$ depends on can be extracted using the input impedance of a lossless transmission line with arbitrary load impedance formulation (3.17), where $Z_L$ is the load impedance, $l$ is the length of the transmission line and $\beta$ is the propagation constant [44]. When the transmission line is open-end, $Z_L$ value becomes infinite and (3.17) simplifies into (3.18). The out coming result is a reactance with a "-" sign which indicates that the effect of open-ended transmission line is capacitive on the input impedance provided that $\beta l>0$. This capacitive effect is inversely proportional to the characteristic impedance of the transmission line. If the $W+2G$ is kept constant, to have a larger capacitance, the characteristic impedance should be decreased which is possible by making the center conductor narrower.

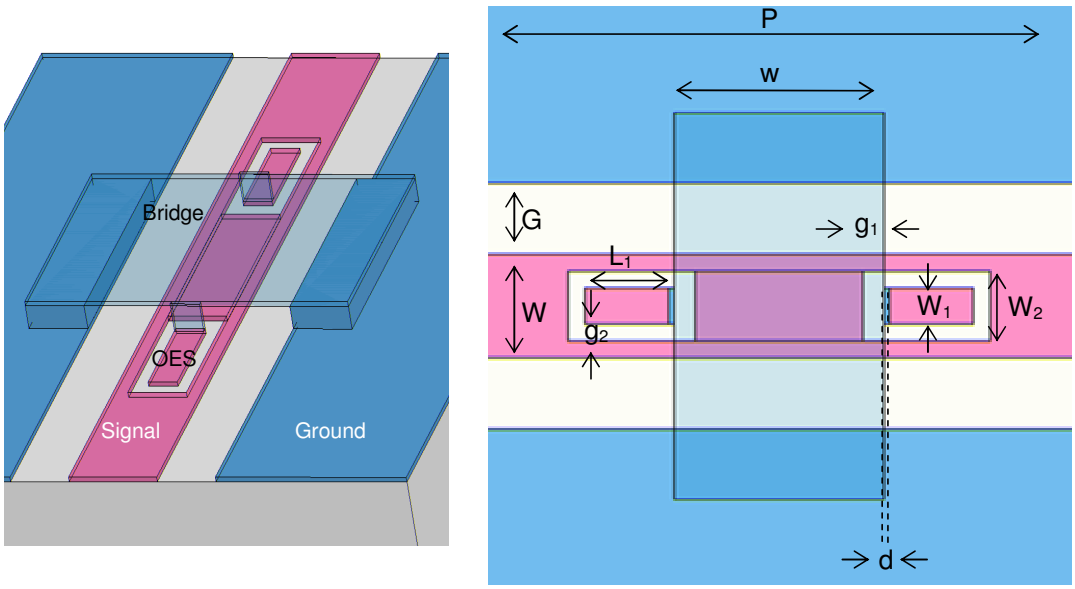
$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan \beta l}{Z_0 + jZ_L \tan \beta l} \tag{3.17}$$

$$Z_{in} = Z_0 \frac{1}{j \tan \beta l} = -jZ_0 \cot \beta l \tag{3.18}$$

$$Y_{in} = jY_0 \tan \beta l \tag{3.19}$$

### 3.3.2. Insertion of OES in the Center Conductor of Unit DMTL Section

An open ended series stub acts as a series capacitance assuming that the stub length is not larger than $0.1\lambda_{g(CPW)}$ as explained in the previous section. This series stub can be used in RF MEMS switch structures to increase the capacitance between the signal line and the ground by using the configuration which Figure 3.20 presents.




**(a)** **(b)**

Figure 3.20. Open-Ended CPW series stub embedded DMTL unit section **(a)** oblique view **(b)** top view

In this structure, the bridge is connected to ground by anchors as usual, which introduces a parallel plate capacitance. Moreover, additional wings on the bridge satisfy a connection between the bridge and the center conductor with the help of the open-ended stubs. This connection provides an open-ended stub capacitance between the signal line and ground. Figure 3.21 shows the developed lumped circuit model equivalent to this structure. The bridge is assumed to be modeled by the *CLR* model while forming this model. The region indicated by the dashed line represents the *CLR* model of the center conductor which lies between the wings of the bridge and the bridge. Therefore, $C_{CLR}$ and $L_{CLR}$ are the parameters used to represent the bridge where $TL_1$ is the transmission line passing under. $L_{OES}$ is the inductance that arises due to the step change in the width of the center conductor and $C_{OES}$ is the capacitance which open-ended stub adds between the bridge and the center conductor. The parameter $TL_2$ is the remaining part of the center conductor.

The introduced model is constructed in order to observe the capacitive effect of the wings. The structures defined in Table 3.12 are used to investigate this assumed capacitive effect by using the introduced model. The simulation outcomes are subjected to a parameter fitting process with the model results, while keeping $L_{OES}$, $C_{OES}$ and $L_{CLR}$ as variables. The parameters of the transmission lines and the parallel plate capacitance, $C_{CLR}$ are calculated since the required dimensions are known. At the end of the parameter fitting process, which depends on minimizing the square error, the variables are found as Table 3.12 shows.

The series discontinuity inductance, $L_{OES}$ seems to be affected a little by the bridge height variations, where it increases with increasing the stub width. The effect of bridge height variations can be explained by considering the path the signal flows. The signal covers different distances while it passes from OES to the bridge. When the bridge is at a higher position, the distance signal covers increases, which raises the inductance. The inductance used in the *CLR* modeling remains nearly constant.

On the other hand as an expected result, the series capacitance increases with increasing the stub width, which brings a decrease in the stub characteristic impedance.

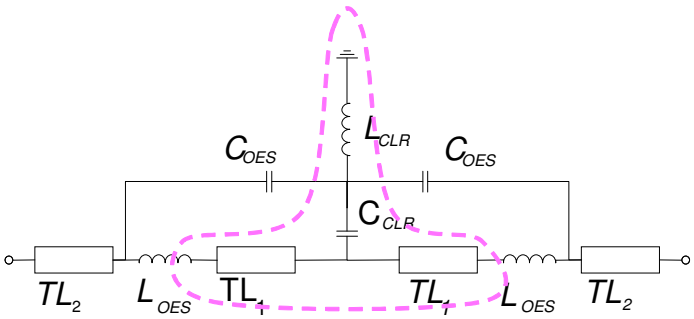



Figure 3.21. Open-Ended CPW series stub embedded DMTL unit section snapshot

Table 3.12. Dimensions of four types of OES embedded unit DMTL sections, where $W$=15 µm, $G$=10 µm, $w$=30 µm, $W_2$=10 µm, $g_1$=3 µm, $d$=0.6 µm, $L_1$= 14.5 µm.

| **Type** | $W_1$ (µm) | $g_2$ (µm) | $h$ (µm) | $C_{CLR}$ (fF) | $C_{OES}$ (fF) | $L_{OES}$ (nH) | $L_{CLR}$ (nH) |
|---|---|---|---|---|---|---|---|
| **VIII** | 5 | 2.5 | 3 | 2.18 | 5.56 | 0.0059 | 0.0021 |
| **IX** | 9 | 0.5 | 3 | 2.18 | 11.12 | 0.0052 | 0.0029 |
| **X** | 9 | 0.5 | 2 | 2.87 | 8.99 | 0.0052 | 0.0029 |
| **XI** | 9 | 0.5 | 1 | 4.85 | 9.01 | 0.0047 | 0.0029 |
| **XII** | 9 | 0.5 | 0.5 | 8.70 | 9.18 | 0.0043 | 0.0029 |
| **XIII** | 9 | 0.5 | 5 | 1.6 | 8.91 | 0.0062 | 0.0030 |

As the results point out, inserting OES through the center conductor adds an additional capacitance which connects the signal line to ground. Therefore, this configuration can be used as a circuit element which behaves like a shunt capacitance. The capacitance value obtained by this structure is larger than the standard air bridge type shunt capacitance as Table 3.12 demonstrates.

To present a more clear comparison Table 3.13 is formed. Here, to find $C_{TOTAL}$, the structure in Figure 3.20 is modeled by only two high impedance transmission lines and a shunt capacitance as Figure 3.22 illustrates. To find, $C_{shunt}$ the same structure, this time without OES, is modeled by a shunt capacitance. As the results show, $C_{TOTAL}$ is much larger than $C_{shunt}$. Therefore, the shunt capacitive effect of the structure is increased significantly when an open-ended stub is inserted through the center conductor.

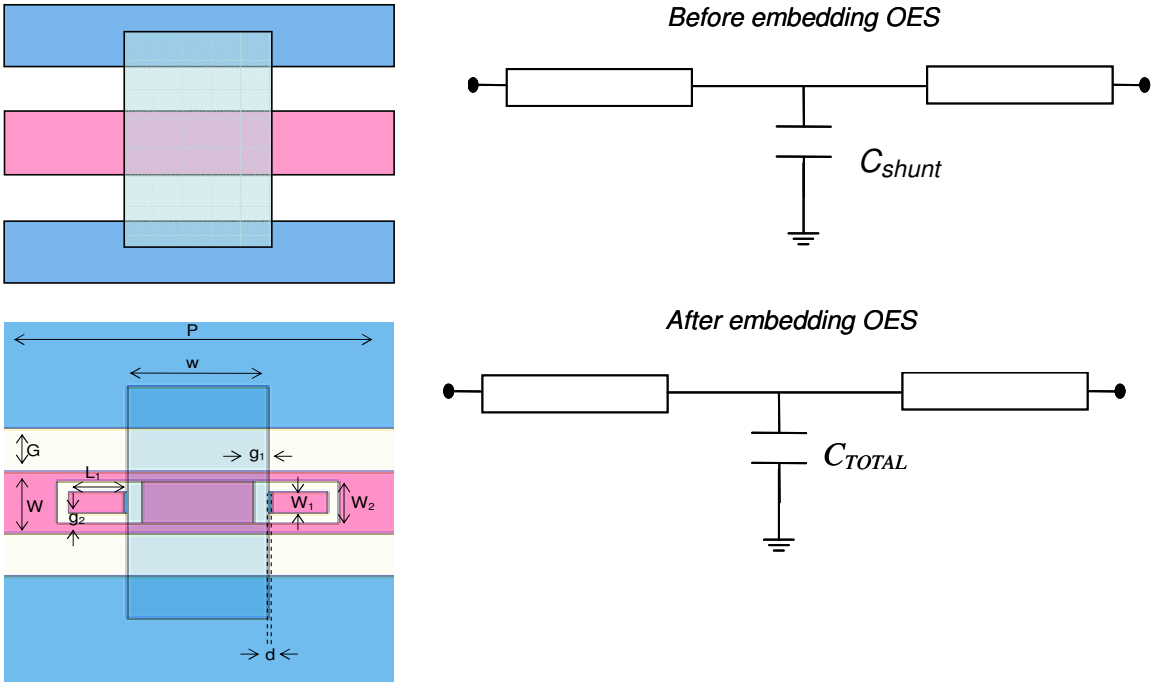



Figure 3.22. DMTL unit section before and after the insertion OES.

Table 3.13. Dimensions of four types of OES embedded unit DMTL sections, where $W$=15 µm, $G$=10 µm, $w$=30 µm, $W_2$=10 µm, $g_1$=3 µm, $d$=0.6 µm, $L_1$= 14.5 µm.

| **Type** | $W_1$ (µm) | $g_2$ (µm) | $h$ (µm) | $C_{shunt}$ (fF) | $C_{TOTAL}$ (fF) |
|---|---|---|---|---|---|
| **VIII** | 5 | 2.5 | 3 | 2.18 | 8.6 |
| **IX** | 9 | 0.5 | 3 | 2.18 | 18 |
| **X** | 9 | 0.5 | 2 | 2.87 | 14.4 |
| **XI** | 9 | 0.5 | 1 | 4.85 | 16.4 |
| **XII** | 9 | 0.5 | 0.5 | 8.70 | 20.6 |
| **XIII** | 9 | 0.5 | 5 | 1.6 | 13 |

Since the capacitive effect is increased considerably, this should bring an increase in the effective phase shift. Table 3.14 gives the phase shift obtained from one unit DMTL cell at 60 GHz for three structures. The structures α and β are standard DMTL unit sections without OES, where the only capacitive effect is from the parallel plate capacitance formed by the bridge. The other structures are the open-ended stub embedded unit DMTL sections, which are previously mentioned. It is obvious from the theoretical knowledge and the presented data that the phase shift improves as the total capacitance increases.

Since it is shown that the capacitance, hence the amount of phase shift can be increased, the next step is to make use of this idea in DMTL phase shifters. The first idea may be to use the structure proposed in Figure 3.20 and actuate the switch so that the height of the bridge decreases. This change in the bridge height will increase the shunt capacitance introducing a phase shift. However, the capacitance increase will be mainly caused by the change in $C_{CLR}$ in Figure 3.21, since the height change does not affect $C_{OES}$ much, as the structures TYPE IX and TYPE X in Table 3.12 illustrates. Consequently, using this configuration will not improve the performance of DMTL phase shifters.

Table 3.14. Total capacitance and phase shift amount of three types of unit DMTL sections, where $W$=15 µm, $G$=10 µm, $w$=30 µm, $W_2$=10 µm, $g_1$=3 µm, $d$=0.6 µm, $L_1$= 14.5 µm and $Z_{unloaded}$=48 Ω.

| **Type** | $W_1$ (µm) | $g_2$ (µm) | $h$ (µm) | $C_{TOTAL}$ (fF) | *Phase shift* (°) | $Z_{match}$ (Ω) |
|---|---|---|---|---|---|---|
| $\alpha$ | 0 | 0 | 3 | 2.18 | -18.86 | 43 |
| **VIII** | 5 | 2.5 | 3 | 8.6 | -22.23 | 38 |
| **IX** | 9 | 0.5 | 3 | 18 | -27.29 | 32 |
| $\beta$ | 0 | 0 | 0.25 | 20.8 | -27.04 | 31 |

What is required is to increase the difference between the upstate and downstate capacitances. This requirement can be met if the upstate capacitance can be made to compose of mostly the bridge capacitance $C_{CLR}$ and the effect of the OES is present only for downstate. Inserting notches under the wings of the bridge is a way to satisfy the stated requirement. Figure 3.23 shows the proposed configuration. With this configuration, when there is no actuation the bridge will not bend. Therefore, it will not be connected to the stubs and the dominant capacitance will be the bridge capacitance. When the bridge is actuated, it will bend and touch the stubs and this will add the additional stub capacitance to the overall shunt capacitance. To understand the amount of added capacitance a simplified version of the model introduced in Figure 3.21 can be used. This simplified version is based on the HICAPLO model shown in Figure 3.4; therefore, it will work for bridge widths larger than 50 µm. Figure 3.24 shows the proposed model, where $C_E$ represents the extra capacitance added by the stub. The region which is covered by the dashed line represents the previously proposed model of the center conductor which lies between the wings of the bridge and the bridge.

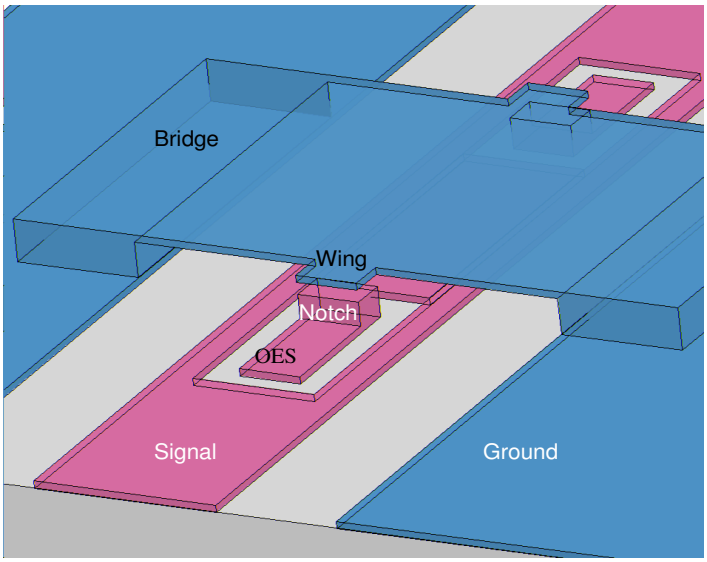



Figure 3.23. Open-Ended CPW series stub embedded DMTL unit section with notches inserted on the center conductor.

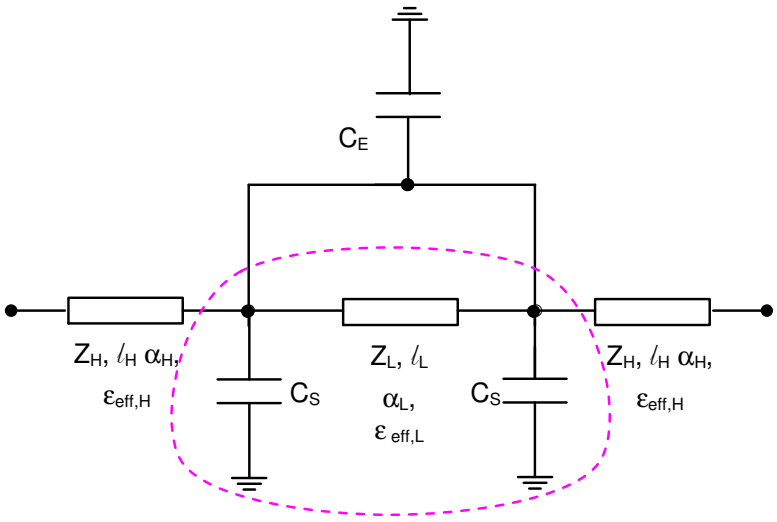



Figure 3.24. Proposed model for Open-Ended CPW series stub embedded DMTL unit section with notches inserted on the center conductor.

Before going into details of DMTL phase shifters, it will be beneficial to validate the proposed model for bridge widths larger than 50 µm and understand the effect of model parameters on the overall capacitance. For this purpose, with the use of the performed model, the capacitive effect of the OES in sample DMTL unit sections with bridge widths larger than 50 µm is investigated. Table 3.15 presents the analyzed structures which are based on the optimum phase shifter unit sections designed in section 3.2.3. This table is constructed using the model which Figure 3.24 proposes; however, as additional information, the CLR modeled parallel plate capacitance of the bridge is given for two bridge height values, namely 1.7 µm and 2 µm. To find $C_E$ value, the proposed model is compared and put through a parameter fitting process with the simulation outcomes.

Table 3.15. Four types of unit DMTL sections, where $W$=176 µm, $G$=162 µm, $w$=80 µm, $W_2$=100 µm, $g_1$=15 µm, $d$=5 µm, $C_{CLR,\ \mathrm{hdown=1.7\ \mu m}}$=91 fF, $C_{CLR,\ hup=2\ \mu m}$=78fF.

| **Type** | $L_1$ (µm) | $W_1$ (µm) | $h_{down}$ (µm) | $g_2$ (µm) | $C_E$ (fF) |
|---|---|---|---|---|---|
| **XIV** | 110 | 20 | 1.7 | 40 | 6.3 |
| **XV** | 110 | 90 | 1.7 | 5 | 42.8 |
| **XVI** | 210 | 90 | 1.7 | 5 | 79.2 |
| **XVII** | 85 | 90 | 1.7 | 5 | 36.4 |

From this analysis, conclusions in accordance with the ones obtained from Table 3.12 are observed such that, when the center conductor width, $W$, increases, the stub capacitance therefore the extra capacitance increases. Moreover, the changes in the length of the stub affect the extra capacitance almost linearly. Therefore, as a design consideration, the stub length and the stub width should be as huge as possible. On the other hand, for an optimum phase shifter, the characteristic

impedances of up and down states should not be very different and the overall loss of the structure should not increase because of the discontinuity losses in the center conductor. Keeping these considerations in mind, it is possible to list the advantages of designing OES embedded DMTL phase shifters as follows:

1. To increase the overall capacitance, beside the bridge capacitance an extra stub capacitance is defined. This extra capacitance depends on various parameters one of which is the stub length. Opposed to standard DMTL structures, increasing loading periodicity, *P* is significant in OES inserted DMTL structures since increasing P makes increasing stub length possible.

2. By the same height difference, OES gives improved phase shift since the up and down state capacitance ratio is larger.

First of the stated advantages is obvious considering the previous explanations. On the other hand, different OES embedded phase shifters are designed and simulated to observe the validity of the other stated advantages. For the designed phase shifters, loading periodicity, *P* is taken as 1000 μm to satisfy feasibility in the stub length adjustment. For some of the structures defined in Table 3.16, Figure 3.25 illustrates the simulation results. Here, the DMTL structures are composed by cascading 20 of the defined OES inserted unit sections. The simulated structures have up and down-state bridge heights as 2 and 1.7 μm. The insertion loss and $^{o}$/dB performance is evaluated at 10 GHz, where the ports are matched with $Z_{match}$. In Table 3.16 as well as the plotted TYPES, additional structures are presented under the same conditions. On the other hand, Table 3.17 illustrates the designed phase shifter parameters which do not include open-end stubs.

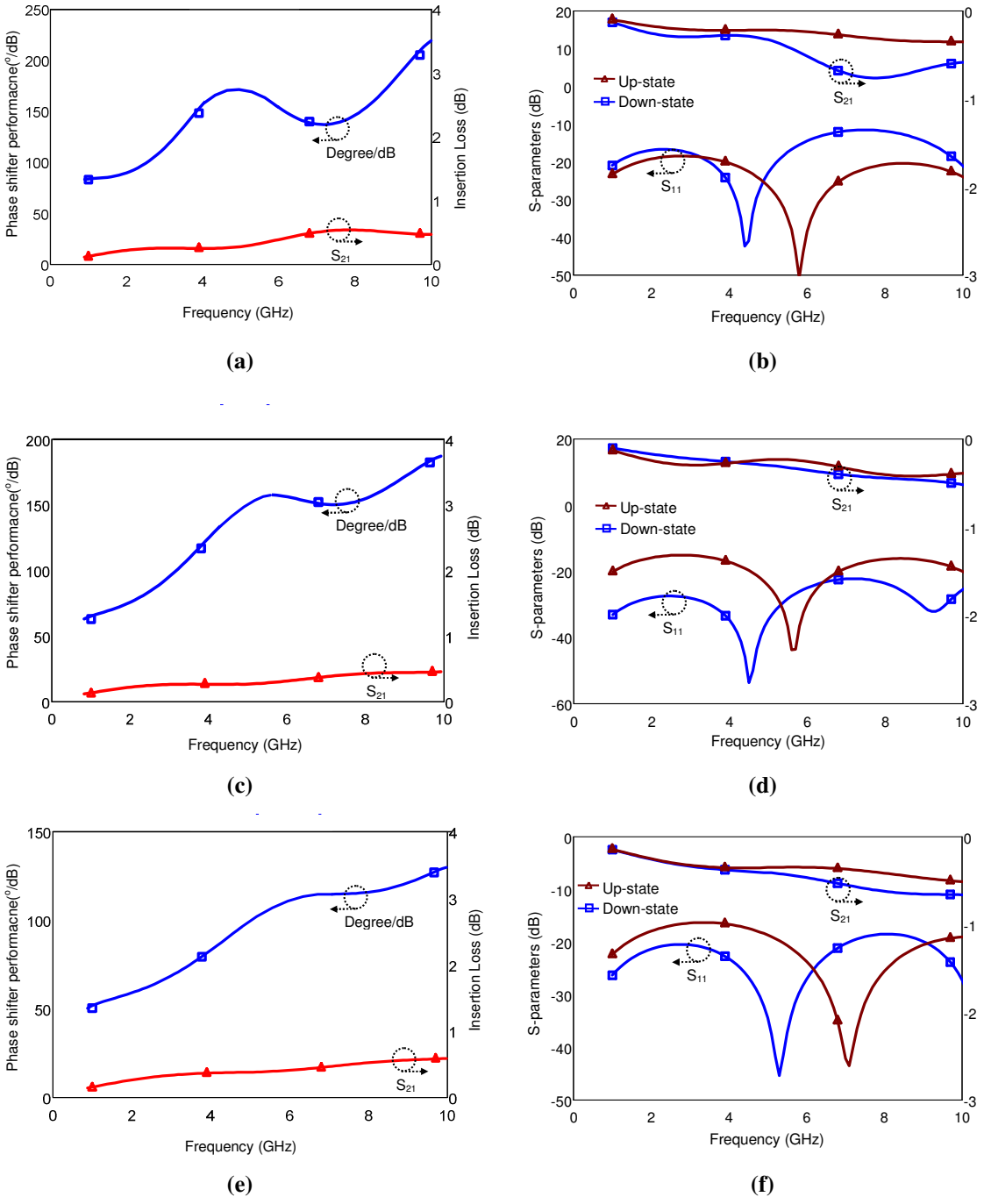



Figure 3.25 The simulation results of OES inserted DMTL : (a) TYPE XVIII when terminated by 47 Ω, (b) TYPE XX when terminated by 50 Ω, (c) TYPE XXII when terminated by 46 Ω.

Table 3.16. Designed OES embedded unit DMTL sections, where $d$=5 µm, $g_2$=5 µm.
.

| **Type** | $W$ µm | $G$ µm | $w$ µm | $L_1$ µm | $W_2$ µm | $S_{21}$ dB | °/dB µm | $Z_u$ Ω | $Z_d$ Ω | $Z_{match}$ Ω |
|---|---|---|---|---|---|---|---|---|---|---|
| **XVIII** | 176 | 162 | 25 | 320 | 90 | 0.48 | 217 | 51 | 44 | 47 |
| **XIX** | 176 | 162 | 50 | 320 | 90 | 0.45 | 187 | 50 | 37 | 43 |
| **XX** | 142 | 179 | 50 | 360 | 80 | 0.48 | 200 | 57 | 42 | 50 |
| **XXI** | 142 | 39 | 50 | 360 | 90 | 0.62 | 90 | 43 | 35 | 32 |
| **XXII** | 110 | 55 | 30 | 360 | 90 | 0.58 | 129 | 53 | 40 | 46 |
| **XXIII** | 110 | 55 | 20 | 360 | 50 | 0.48 | 146 | 57 | 43 | 50 |

Table 3.17. Designed unit DMTL sections without OES, $P$= 1000 µm

| **Type** | $W$ µm | $G$ µm | $w$ µm | $h_u$ µm | $h_d$ µm | $S_{21}$ dB | °/dB µm | $Z_u$ Ω | $Z_d$ Ω | $Z_{match}$ Ω |
|---|---|---|---|---|---|---|---|---|---|---|
| **XXIV** | 176 | 162 | 50 | 2.0 | 1.7 | 0.20 | 75 | 61 | 57 | 59 |
| **XXV** | 176 | 162 | 50 | 4.0 | 1.7 | 0.22 | 130 | 64 | 57 | 60 |
| **XXVI** | 176 | 162 | 50 | 6.5 | 1.7 | 0.26 | 185 | 68 | 57 | 61 |
| **XXVII** | 176 | 162 | 25 | 2 | 1.7 | 0.21 | 26 | 61 | 60 | 60 |
| **XXVIII** | 176 | 162 | 25 | 20.0 | 1.7 | 0.21 | 203 | 75 | 60 | 63 |

The first observation that should be done on these results is that, as the second listed advantage suggest, for the same amount of phase shift, more height difference is needed for a specific structure. For instance, when Type XIX and Type XXVI are compared, for nearly same amount of phase shift, OES inserted phase shifter uses a height ratio of 2 / 1.7 = 1.17, whereas the classical phase shifter needs a height ratio of 6.5 / 1.7 = 3.82. Likewise, when Type XVIII and Type XXVIII are compared, the

initial height of the bridge should be increased to a very large value to satisfy nearly the same amount of phase shift when OES is not used. The required height ratio becomes 20 / 1.7 = 11.7 and the difference between the matching impedances for up and downstate gets larger for the classical phase shifter, Type XXVIII.

On the other hand, by just actuating the switch, the ratio can be made at most 1.5, since for higher ratios the bridge collapses [7]. Therefore, for the classical phase shifter to prevent the switch from touching the center conductor when it collapses, a dump is needed to stop the bridge at the desired height. This dump should not touch the ground or the signal line, instead it should lie somewhere in between as Figure 3.26 shows. Assuming that the bridge will bend to the signal line in a linear way, the relation between the dump height and position with respect to the bridge height and bridge length can be driven as:

$$\frac{h_D}{h} \geq \frac{L_D}{L_B / 2} \tag{3.20}$$

Equation (3.20) presents an approach for the relation between the dump height and position. To make analysis clear, it will be advantageous to consider a specific example. Type XXVIII phase shifter will be a good example since it needs a high height ratio. Here, the known parameters are $h_D$=$h_{down}$=1.7 µm, $h$=$h_{up}$=20 µm, and $L_B/2$=200 µm. If the known parameters are placed in equation (3.20), the inequality given in (3.22) is obtained.

$$\frac{h_D}{h} \geq \frac{L_D}{L_B / 2} \tag{3.21}$$

$$\frac{1.7}{20} \geq \frac{L_D}{200\mu\text{m}} \quad 17 \geq L_D \tag{3.22}$$

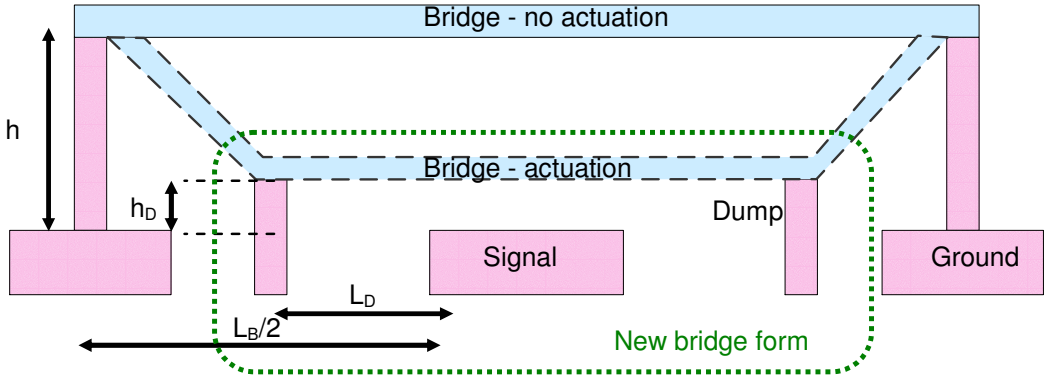



Figure 3.26. Proposed model for Open-End CPW series stub embedded DMTL unit section with notches inserted on the center conductor.

Now the assumption is that, the dumps are placed in accordance with the criteria obtained in (3.22). Then the bridge is actuated by a voltage $V_1$ which will pull the bridge towards the signal line. This $V_1$ voltage should be higher than the pull-down voltage in order to bring the bridge height down to 1.7 µm, which is smaller than the collapse height 20×2/3=13 µm. The bridge will be stopped by the dumps before it touches the signal line and there will appear a new bridge form which can be approximated as Figure 3.26 demonstrates. Here, the new bridge will have height of 1.7 µm. The distance between two dumps, $L_{anch}$ will be at most 176+17+17=210 µm, and at least ~176 µm. To examine reliability and the stability for this new bridge, the equations (3.23) and (3.24) should be considered.

$$V_1 = \sqrt{\frac{8k(20\mu m)^3}{27\varepsilon_0 A}} \quad V_2 = \sqrt{\frac{8k(1.7\mu m)^3}{27\varepsilon_0 A}} \quad \text{Volts} \tag{3.23}$$

$$k = 16\frac{Ewt^3}{L_{anch}^3} \tag{3.24}$$

Here, the pull-down voltage is defined as in CHAPTER II. $V_1$ is the pull-down voltage of the bridge before actuation and $V_2$ is the pull-down voltage of the bridge after it is actuated and turned into the new form, where $k$ is the spring constant. In equation (3.24), which defines $k$, $L_{anch}$ stand for the distance between the anchors, $w$ is the width of the bridge and t is the thickness of the bridge material.

For the new bridge form, the pull-down voltage, $V_2$ will be proportional to $\sqrt{(1.7\,\mu m)^3}$ and $\sqrt{(1/L_{anch})^3}$. Here $L_{anch}$ can be varied between 210 μm and 176 μm. Therefore, if the rest of the parameters in equation (3.23) are replaced by a constant "C", the pull down voltage can be expressed as $2.6\times10^{-7}C < V_2 < 4.5\times10^{-7}$ C. To prevent the bridge from collapsing, the applied actuation must be smaller than this voltage.

On the other hand, it was mentioned that in order to bring the bridge from 20 μm to 1.7 μm height position, there should applied a voltage of $V_1$, which is the pull-down voltage of the bridge in the initial condition, where it does not touch the dumps. This voltage is proportional to again $\sqrt{g_0^3}\times\sqrt{(1/L_{anch})^3}$. However, for the initial condition, $g_0$ is 20 μm and $L_{anch}$ is 200+200+176=576 μm. Since the other parameters are same with the previous condition they can be replaced with "C" again. The pull-down voltage, $V_1$ is approximated as $2.1\times10^{-5}$C. This voltage value is necessary in order to make the bridge touch the dumps. As it is observed, $V_1$ value is much larger than $V_2$, which means that the bridge will continue to collapse after it touches the dumps. Thus, such a structure is theoretically impossible.

Considering the fabrication process, the structure of the OES embedded DMTL phase shifters should be modified, where this modification should be in the wing and notch locations. If the present configuration is preserved, after the release step, the wings will be more stressed than the other parts of the bridge and curl up. The bending in the wings will increases when the usual annealing process is applied;

therefore, when the structure is actuated, the bridge will collapse on the center conductor before the wings touch the notches. Therefore, the DMTL unit sections are slightly modified as shown in Figure 3.27 in which the bridge is extended in both directions above the wings.

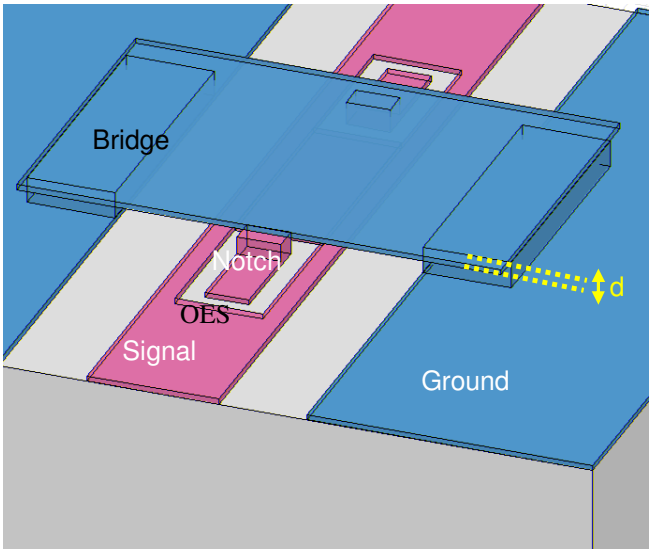



Figure 3.27. Open-Ended CPW series stub embedded DMTL unit section with notches inserted on the center conductor.

# CHAPTER IV

# FABRICATION OF THE DESIGNED DMTL PHASE SHIFTERS

The designed DMTL phase shifters are fabricated in the METU Micro Electronics Facilities (METU MET). Before fabrication, the layouts of the designs are prepared and transferred to masks. The fabrication is based on the surface micromachining techniques since the overall structure is composed of thin layers placed on top of each other. The fabrication mainly composed of depositing thin film materials and patterning them with photolithography and etching techniques. For the suspending structures, sacrificial layers, which are removed at the end of the process, are used.

In this chapter, the mask drawing step is explained in Section 4.1 Then, the properties of the fabrication techniques and the used materials are mentioned in Section 4.2. The fabrication flow is explained at the end of the chapter in Section 4.3, and the SEM pictures of the fabricated structures are presented in Section 4.5.

## 4.1. LAYOUT DRAWING AND MASK GENERATION

Masks are partially transparent plates used in the photolithography steps of a fabrication process. The pattern on the mask is transferred on a wafer which is covered by a photo definable material like photo resist. Depending on the polarity of the resist, after development some parts of the resist is removed and the pattern transfer job is finished.

The mask layouts used in this thesis are drawn using CADENCE and the related output files are sent to a commercial photo/print center. The received production results are chrome coated quartz glass masks, which are square in shape and have a side length of 5 inches. For the DMTL structures and the phase shifters designed in the previous chapters, 6 different layouts are drawn each of which is used in a different process step. These masks will be detailed in the following sections, but a summary can be presented as follows:

MASK NO 1: First metallization mask, which includes the metallization of CPW structures.

MASK NO 2: Electroplating mask, which defines the regions to be thickened.

MASK NO 3: Dielectric mask, which determines the positions where dielectric layer will be present.

MASK NO 4: Anchor etch mask, which defines the points where the sacrificial layer will be removed and the anchors of the bridges will be placed.

MASK NO 5: Second metallization mask, which determines the position of the bridges.

MASK NO 6: Back side metallization mask, which defines the areas where the bottom of the wafer will be coated by metal.

The layouts of the modeling study and the phase shifter designs are drawn in different mask sets, although their process steps are nearly identical. The only difference results during the electroplating step. In the DMTL electroplating mask, the parts of the CPW transmission lines which are not under the bridges are thickened to decrease the conductor loss. On the other hand, in the DMTL phase

shifter electroplating mask, the open-end stub connection points are thickened to generate notches at these points.

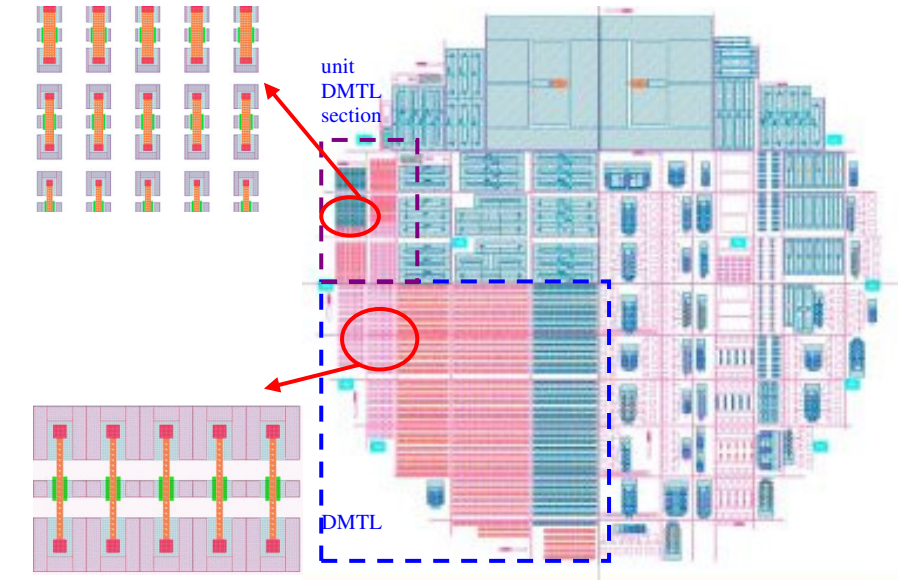
Figure 4.1 shows the mask sets for these two designs. In each of the snapshots, the mask layers are drawn on top of each other. Although the view seems complicated at the first glance, the zoomed snapshots can give a better idea. The light blue areas are the first metallization mask regions, where the light pink areas the electroplated regions. Orange parts stand for the bridges; green parts are the dielectric regions and the dark pink areas are the anchor points.

## 4.2. FABRICATION TECHNIQUES AND MATERIALS

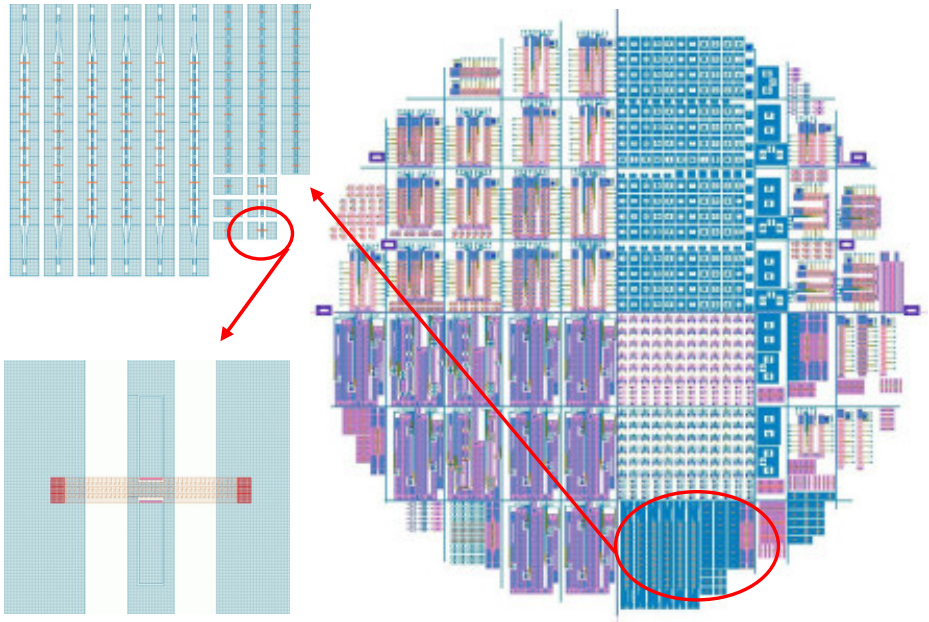
The fabrication, as stated previously, is based on surface micromachining techniques. The main steps of surface micromachining used in the process of the DMTL phase shifters are thin film deposition, photo resist spinning, lithography, electroplating, sacrificial layer coating, metal etching, and release. This part will describe these steps basically and give the properties of the materials used. The detailed process flow of RF MEMS group developed at METU MET will be presented in the next section.

### 4.2.1. Film Deposition

The film deposition techniques can be classified into two: physical vapor deposition (PVD) and chemical vapor deposition (CVD). In this study both types will be considered since for metals and dielectric layers different techniques are required.




(a)



(b)

Figure 4.1 Mask snapshots for (a) DMTL structures and DMTL unit sections. (b) DMTL phase shifters and open-end stubbed DMTL unit sections.

The deposition of the metals, which are gold and titanium in our case, is realized by using PVD technique. In PVD, a source material such as gold is transformed into gas phase in a chamber [51] and the atoms of the gas sticks to a wafer which is put in the same chamber. Sputtering is a type of PVD which is used in the metal depositions of the DMTL phase shifters. In sputtering, plasma is formed in the argon filled chamber by either applying an RF or a DC signal. Argon ions created because of this plasma hits the source and pulls the source atoms towards the wafer.

On the other hand, the deposition of the dielectric, which is silicon nitride in our case, is realized by CVD technique, which includes low-pressure CVD (LPCVD), plasma-enhanced CVD (PECVD), and photo-CVD. In CVD, different than the PVD the deposition is realized from a gas phase.

### 4.2.2. Photolithography

The deposited metal should be patterned in order to continue the fabrication process. The patterning is established by an etching step; however, before etching some parts of the metal should be protected so that the pattern does not vanish from the wafer. This protection is realized by photolithography steps which can be listed as: spinning photo resist (PR) all over the wafer, soft baking, exposing the wafer to UV through a mask, developing the PR, and hard baking it.

After PR is coated on one surface of the wafer with the help of a spinner, the wafer is placed on a hot plate and left there for 1-10 minutes depending on the PR type. This is known as soft bake and used to improve the adhesion property of the resist on the wafer and eliminate the solvent from the coated resist. When the soft bake step is over, the wafer is ready to be exposed to UV. The UV light can affect the resist in two ways. If the resist is positive, the parts which are exposed to UV become more

soluble in the developer; otherwise, if the resist is negative, the parts which are exposed to UV become less soluble in the developer.

After the wafer is exposed to UV, it should undergo a development stage. In this stage the more soluble portions of the resist are removed in a chemical solvent called developer. Therefore, the pattern on the mask can be observed on the wafer. The two things that should be cared during development are, first not to leave the wafer in the developer too long and cause overdeveloping by creating undercuts. Second, the wafer should be rinsed and dried carefully to be sure that there remained no developer on the wafer. The last stage of the lithography is the hard bake, which helps to harden the PR on the wafer before applying etchants on the wafer.

### 4.2.3. Etching and Electroplating

Etching can be made either in dry ambient or in wet ambient. Wet etching is applied during the removal of the metals and photo definable chemicals in this work. The metals which are not protected by the PR on top of them are removed by the etchant and therefore, the pattern on the mask is transferred to the structural layer. On the other hand, dry etching techniques are preferred in the patterning of dielectric layers. RIE etching is a kind of dry etching technique in which plasma created by an RF power etches the materials.

After hard bake, instead of etching, the metal regions which are not covered by PR can be thickened by using electroplating. In the electroplating process a liquid solution (electrolyte) is obtained which include metal ions. The wafer is placed in this liquid and an electrical potential is applied between a conducting area on the wafer and an electrode in the liquid. The ions in the solution are attached to the non-PR coated regions and the plating is satisfied.

### 4.2.4. Sacrificial Layer Coating and Release

After the first metallization process and dielectric deposition is finished, the sacrificial layer, which will be used as a support for the suspending structures like bridges, is coated. This sacrificial layer can be selected from a variety of materials including metals. For the process of DMTL structures, this layer is selected to be polyimide which is an organic and photo definable material.

The sacrificial layer is removed at the end of the process and the suspending structures are released. The sacrificial removal can not be realized by standard PR removing or etching methods. The reason is that, when the sacrificial layer is removed and the liquid placed instead of it begins to dry, the suspended structure is pulled down to the base metal because of surface tension and capillary forces, which causes stiction. To overcome the stiction problem, critical point drying (CPD) technique is used [7]. The procedure of this technique is as follows: the wafer, after sacrificial layer is removed by a chemical, is rinsed and then put in isopropyl alcohol (IPA). When all the water under the suspended structures is replaced by IPA, the wafer is put in critical point dryer chamber. In the chamber, IPA is replaced by liquid $CO_2$. As the temperature and the pressure of the chamber are increased, the $CO_2$ transforms into a supercritical phase. This supercritical $CO_2$ is taken out of the chamber and since no liquid exists under the bridges, the stiction is prevented.

## 4.3. MATERIALS

Any structure processed by METU RF MEMS fabrication scheme is composed of mainly four different materials which are glass, Au, Ti, and $Si_xN_y$. Beside these, as sacrificial layer polyimide and as lithography chemical S1828 photo resist are used. In this section these materials and the reason behind their selection will be briefly discussed.

For the structural layers, different metals can be considered some of which are gold, aluminum, and nickel. In the DMTL process, the preferred metal is gold because of its advantages over the other metals. Au has a lower Young Modulus and therefore a lower spring constant than Ni. Moreover, despite Al, since Au is inert, it can not be etched or damaged by most of the etchants. For instance, the chemicals which are used to remove the sacrificial layer attack Al but do not harm Au. On the other hand, the main drawback of Au is the difficulty of adhering to the other materials. Therefore, it should not be deposited on the substrate directly; instead an intermediate layer such as Ti should be first deposited to improve clinging. Otherwise, Au will peel off from the surface of the substrate. During the process of DMTL structures, the deposition of Ti and Au is satisfied by sputtering.

The dielectric layer to be deposited by PECVD under the bridges is determined to be silicon nitride. The effective permittivity of PECVD $Si_xN_y$ is about 7 and it has a dielectric breakdown in the order of $10^9$ V/m. The fact that it is not easy to wet etch silicon nitride highlights the need for dry etching techniques. For the nitride layers, the patterning is established by RIE dry etching in METU MET.

Between the bridge and the base metal, a sacrificial layer is deposited, which will be used as a support for the suspending structures. Sacrificial layer can be selected from a variety of materials including metals. For the process of DMTL structures, this layer is selected to be polyimide as explained previously. The main advantage of polyimide over metal sacrificial layer is the ease in its deposition and patterning. Since it is photo definable, a single photolithography step is enough for pattern transfer and development. Moreover, its planarization is better than the metals and it does not have any adhesion problem to the structural layers. The polyimide types used in DMTL structure processes at METU MET are PI 2737 (negative polyimide) or PI 2610 (positive polyimide) , which result in opposite patterns after development.

For the patterning of the materials other than polyimide, S1828 positive PR is used during photolithography. S1828 is used as a masking material during the etching of the thin film materials, such as metals or dielectrics. In the DMTL fabrication process, positive PR is preferred since its hard bake duration is shorter than that of a negative PR. After S1828 is coated over the material, either clear or dark-field masks are used to shape the material. Clean-field mask is used when the pattern on the mask is aimed to be protected. During DMTL fabrication, MASK NO 1, 3, 5, and 6 are clear-field masks. When the regions outside pattern is planned to be protected, dark-field mask is used as in MASK NO 2 and 4. Other than S1828 another positive photo resist, SPR 220, is used to determine which regions will be electroplated. S1828 is no suitable for this issue, since it dissolves in gold electroplating solution.

## 4.4. PROCESS FLOW USED IN DMTL FABRICATION

The DMTL structures are fabricated by processing the pre-defined materials by the explained techniques. In this part, detailed fabrication process will be explained with the help of flow schematics. The flow schematics show the process wafer from two different point of views, namely from AA' and BB' as Figure 4.2 illustrates. Figure 4.3 and Figure 4.4 shows the main steps of the fabrication, which do not include photo resist depositions. Moreover, the details such as durations or medium pressures are not mentioned in this part but, are given in APPENDIX I.

The fabrication begins with holding the glass wafer in piranha (sulfuric acid/hydrogen peroxide ratios is 4/1) and HF (HF/water ratio is 1/10) solutions as a first step before film deposition. There are two incomes of this procedure: first, it cleans the wafer surface; second, it adds some roughness to the wafer surface to improve the adhesion of the films to be deposited. After cleaning, first metal deposition is realized by sputtering 110 $A^o$ Ti and 800 $A^o$ Au on the top of the wafer.

Figure 4.4 (a) shows the Ti-Au coated wafer, where Ti is used for satisfying adhesion between Au and glass. After sputtering, SPR 220 photo resist is spun on the top of the wafer and the regions which are planned to be thickened by electroplating are released from photo resist with help of MASK NO 2. At this point, it should be mentioned that the regions, which are planned to be electroplated, are not same for standard DMTL's and OES inserted DMTL's. In OES inserted DMTL structures, the notch locations are released from photo resist, since notches are going to be built in these regions by electroplating. On the other hand, in standard DMTL structures, the regions which will not be located under the bridges will be thickened in order to decrease the conductor losses. The process flow graph shown in this chapter considers the second case and applies electroplating to the regions which will not be located under the bridges.

After Au electroplating is applied as Figure 4.3 (b) shows, the pre-released regions are plated. Next, the patterned resist is stripped from the surface and a fresh S1828 resist is spun on the electroplated wafer. With the help of MAKS NO 1, the metals regions which will be etched are determined and the resist in these regions are cleared. After Au and Ti is etched from the determined regions, CPW transmission line structure is present on the wafer as Figure 4.3 (c) demonstrates.

After the first metal layer process on the top side is finished, 110 $A^o$ Ti, 2500 $A^o$ Au and 200 $A^o$ Ti are deposited on the bottom side of the wafer by sputtering. After sputtering, S1828 is spun all over the bottom side and the resist patterning is established by MASK NO 3. Therefore, metals regions which will be etched are determined and the resist in these regions are cleared. Before starting the etching of the bottom side metals, the top side of the wafer is covered with S1828 for protection. Then the wafer is introduced Ti etchant, Au etchant and again Ti etchant successively and the shape shown in Figure 4.3 (d) is obtained. The back side shaping is necessary if there are other structures to be fabricated on the same wafer,

which do not need conductor back. The second Ti is deposited to prevent the etching of bottom side Au, while top side metals are being processed.

After parts (a) to (d) are completed, the wafer has CPW transmission line structure on the top side and patterned conductor back at the bottom side. The next process will be to spin and pattern silicon nitride on the parts of center conductor of CPW which will lie under the bridges. The nitride deposition is made by PECVD. Then S1828 resist is spun all over the top side and the resist patterning is established by using MASK NO 4. Finally, nitride patterning is established by applying RIE to the regions released after lithography (Figure 4.3 (e)). After nitride deposition and shaping is finished, remaining S1828 is removed from the wafer with acetone and isopropyl alcohol.

As a sacrificial layer, which will support the bridges negative polyimide, PI 2737 is used. It is spun on all over the top side of the wafer by using a spinner. The areas which will be the standing points of the anchors are determined by using MASK NO 5, which is a clear-field mask. After development of PI 2737, the anchor points are released (Figure 4.4 (a)-(b)).

The last process before release is the deposition of the second metal layer, which will form the bridges. The second metal layer is obtained by 4000 $A^o$ gold sputtering over the polyimide layer and inside the anchor points (Figure 4.4 (c)). The regions to be etched on the second metal are defined by using MASK NO 6, after S1828 is spun over the top of the second metal. While the gold is being etched from the top side of the wafer, the titanium layer at the back protects the gold under it. After the etching of Au is finished, the wafer looks as in Figure 4.4 (d). The remaining process is the release of wafer from polyimide. The procedure followed during release can be stated as follows:

1. The wafer is placed in beaker full of a chemical named SVC, which resolves organic materials and left there for about 1-2 days. Since SVC acts as a developer for the polyimide and resolves it, at the end of 1-2 days, polyimide is removed under the bridges.

2. The wafer is then transferred to a cleaner SVC beaker without removing the SVC, which remains under the bridges, during transfer to prevent stiction. This process is repeated two times.

3. After all the polyimide is removed under the bridges, the wafer is transferred directly into a beaker full of water, again without spoiling the SVC which remains on the top of the wafer. This process is repeated for three times.

4. After the wafer is cleaned in water, it is transferred to isopropyl alcohol beaker.

5. As a last step, the wafer is transferred to critical point dryer whose chamber is filled with alcohol.

6. After the CPD process is finished, the wafer is taken out of the dryer chamber and looks as in Figure 4.4 (e).

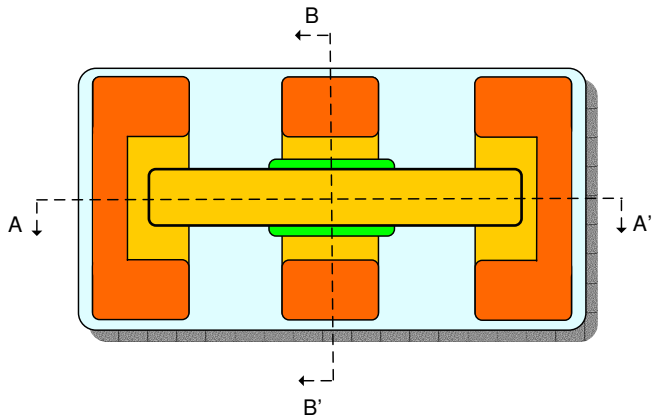



Figure 4.2 Top view of a processed DMTL unit cell, where AA' and BB' represents the view points used in drawing Figure 4.3 and Figure 4.4.

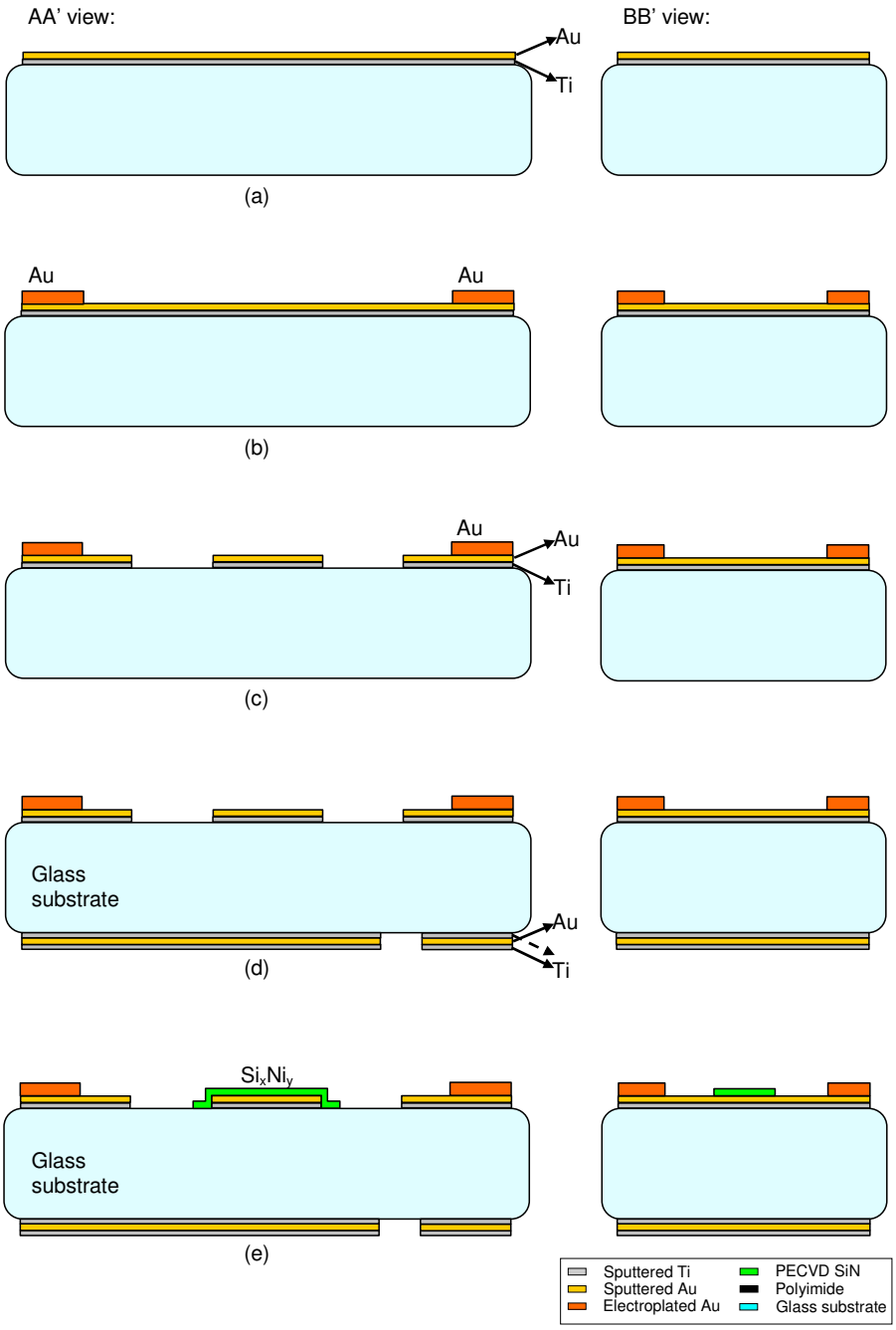



Figure 4.3. DMTL unit cell process flow diagram from AA' and BB' views of: (a) first metal deposition, (b) gold electroplating, (c) first metal patterning, (d) back side metallization and (e) nitride deposition and patterning.

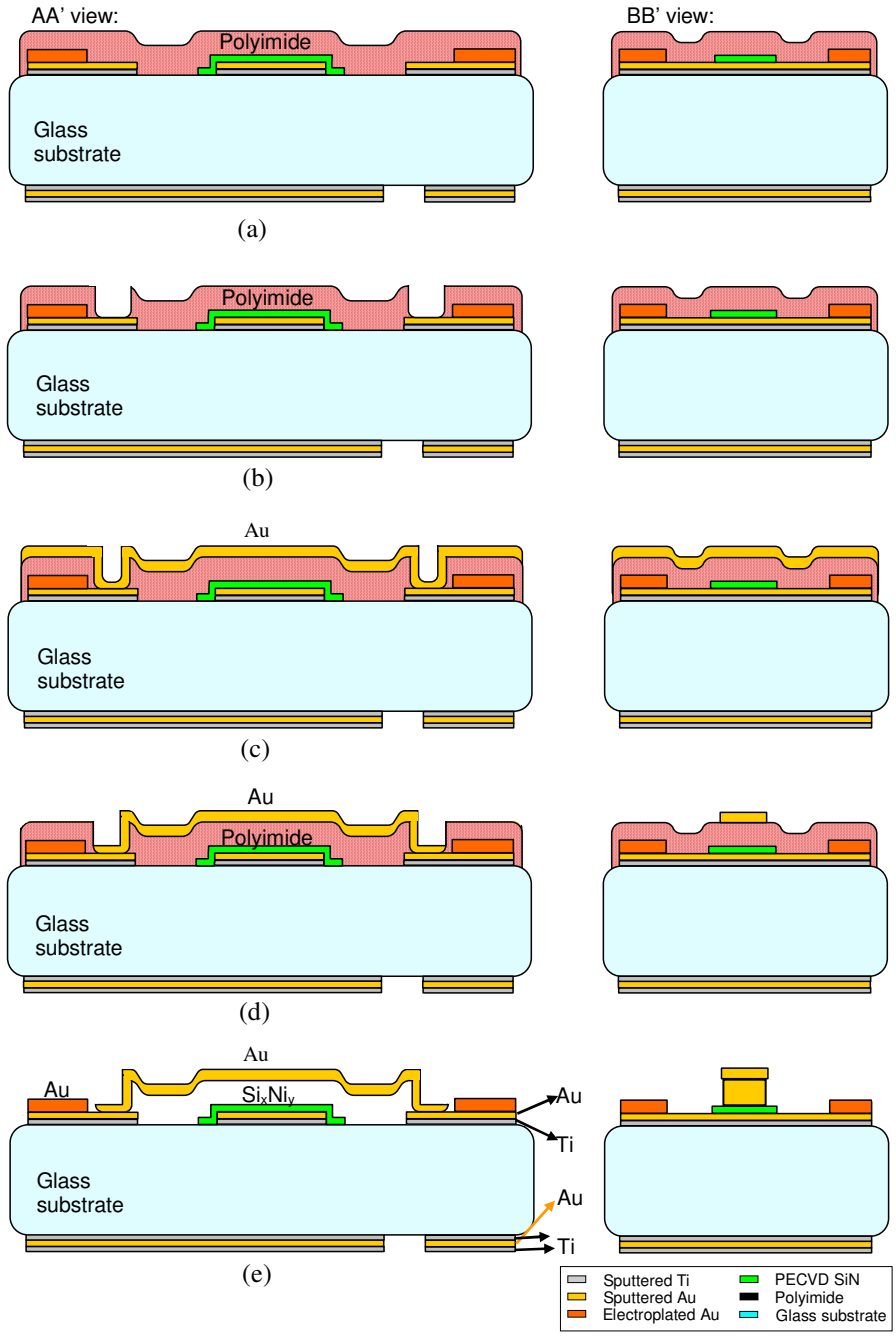



Figure 4.4. DMTL unit cell process flow diagram from AA' and BB' views of: (a) polyimide deposition, (b) polyimide patterning, (c) second metal deposition, (d) second metal patterning, (e) release.

SVC is an isotropic etchant for polyimide, which means it etches polyimide at the same rate in all directions. Under the second metal coated regions, such as under the bridges, polyimide release is more difficult since the only space that SVC can flow is the gap between the bridge and the first metal. To speed up the release, etch holes are cut on the top of the bridge as Figure 4.5 demonstrates. Therefore, SVC finds an alternative way to enter the gap between the bridge and the first metal. Reducing the film damping, increasing the switch speed and releasing some of the residual stress are the other advantages of using etch holes. On the other hand, there is a limitation on the size of the etch holes. The total hole area should be less than 60 % of the bridge area and the diameter of the holes should be less than 3-4 times the height of the bridge [7]. Up to these values, the effect of holes on the up-state capacitance and therefore on the pull-down force is insignificant since the fringing fields fill the gaps on the bridge.

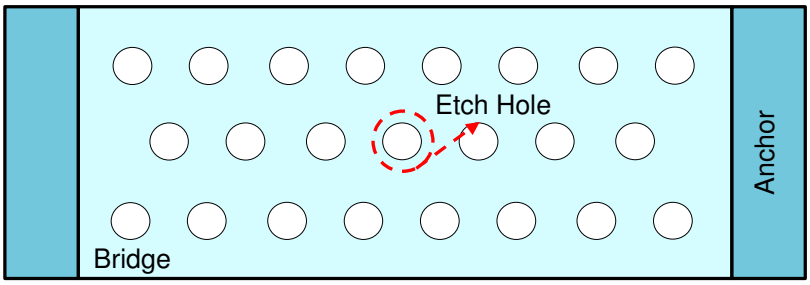



Figure 4.5. The top view of a bridge with etch holes inserted.

## 4.5. FABRICATION RESULTS

The 48 DMTL structures defined in CHAPTER III are fabricated using the mask layout shown in Figure 4.1 (a). The fabrication is based on the flow which Figure 4.5 summarizes. In this section, the SEM pictures of the fabrication results, surface profiler snapshots and the comments on the outputs are given.

### 4.5.1. SEM Pictures

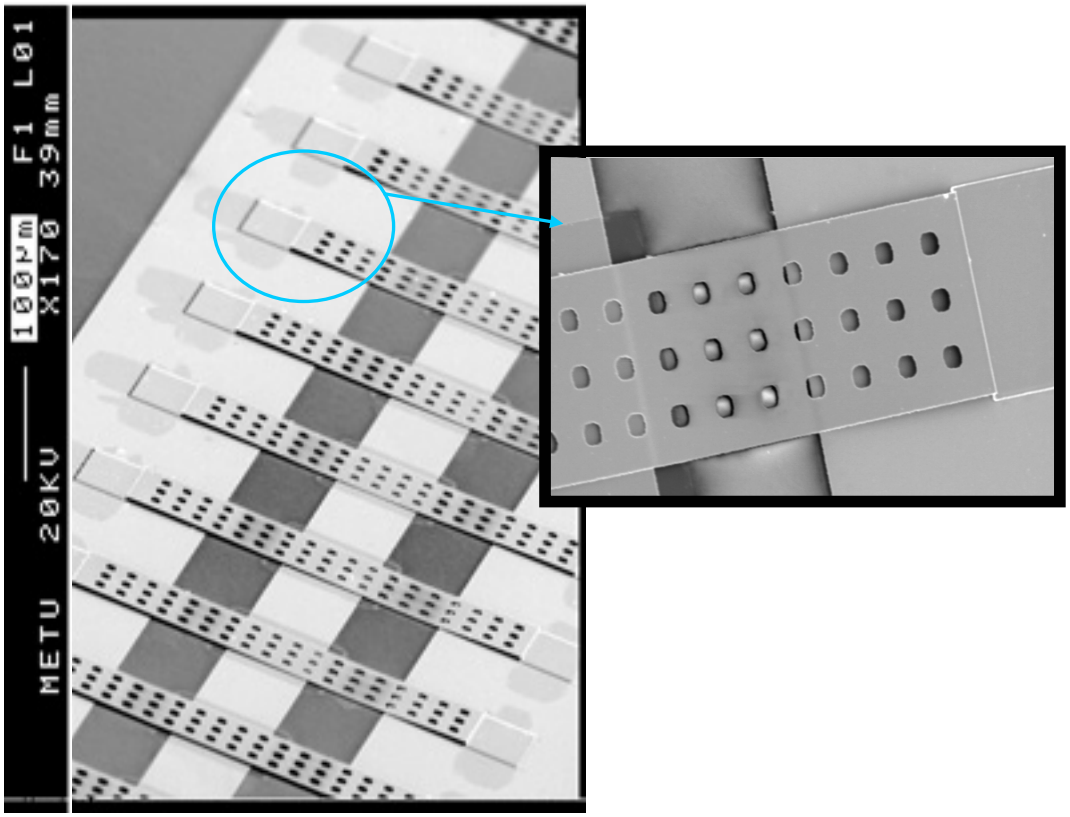
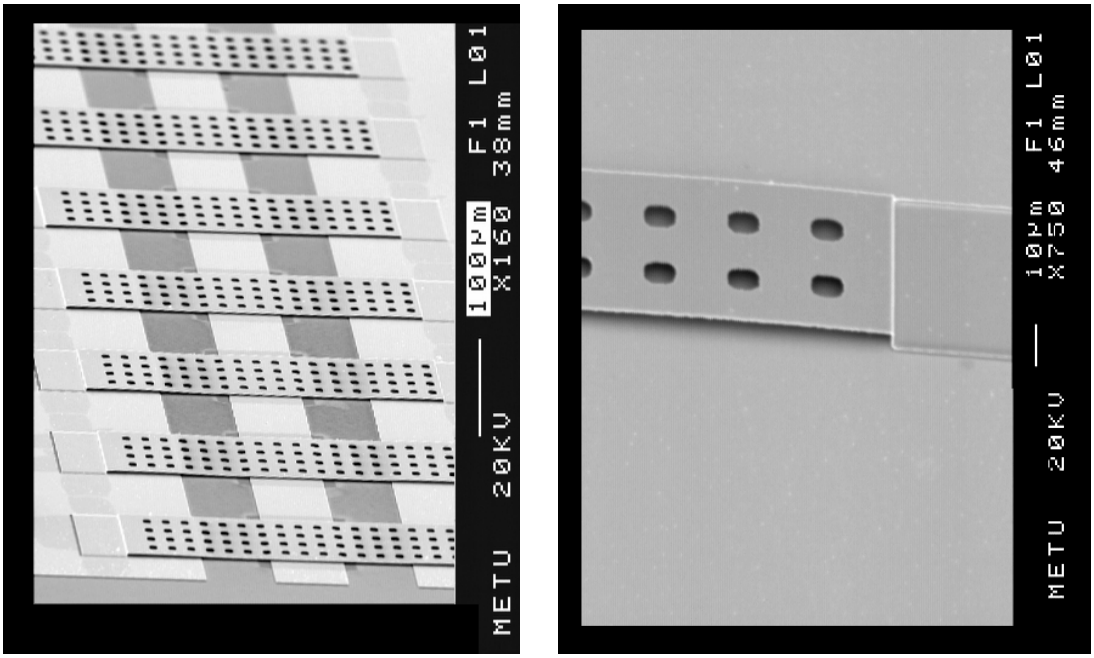
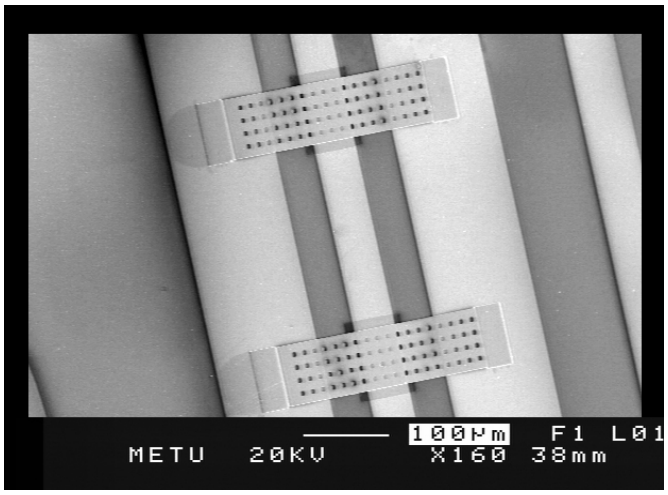



Figure 4.6 SEM picture of TYPE 24 DMTL structure and its close view through one of the anchors.




(a) (b)




(c)

Figure 4.7 SEM picture of (a) TYPE 28 DMTL structure. (b)TYPE 5 DMTL structure. (c)TYPE 10 DMTL structure.

From the SEM pictures, the bridges of the DMTL structures seem to be straight, whereas the real situation is quite different. The bridges show buckling characteristic because of compressive stress, which Figure 4.8 presents. The 3D view seen in this figure is taken from one of the fabricated DMTL structures with the help of Veeco Surface Profiler. This surface profiler offers fast, non-contact, three-dimensional measurement possibilities for the DMTL structures. Therefore, with the help of this tool, the metal thicknesses and the bridge heights can be measured. With the proposed process flow, the 1st metal thickness of the fabricated devices is measured as 0.3 µm, the electroplated metal thickness is measured as 2.5 µm and the second metal thickness is measured as 1.1 µm. On the other hand, the bridge heights can not be measured precisely because of their bended structure. The bending results from the intrinsic compressive stress of the deposited Au thin films. This intrinsic stress buckles the bridges when the structure is released from the sacrificial layer. The sputtering rate, pressure and temperature mainly affect the intrinsic stress of the bridges, where this stress varies in accordance with the material used.

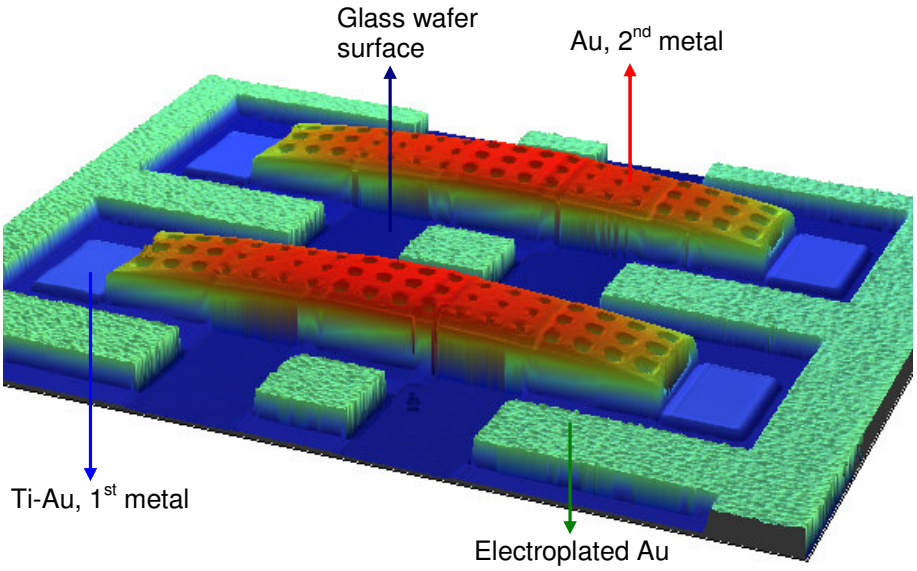
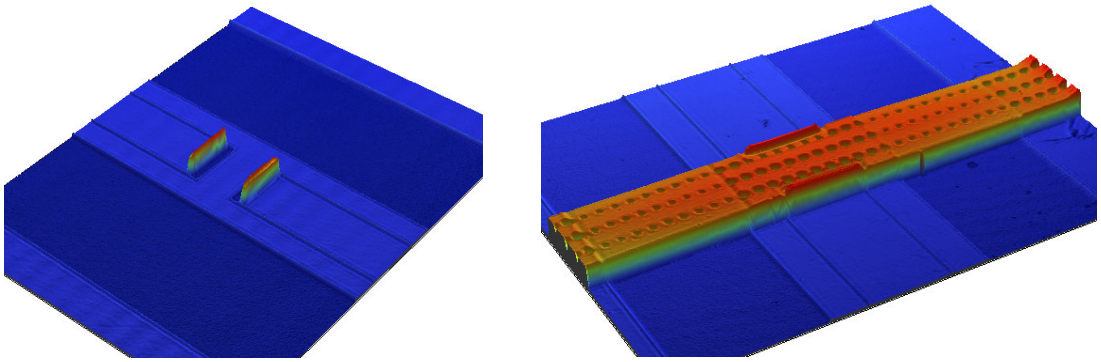
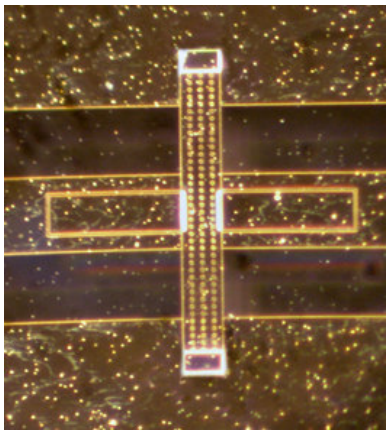



Figure 4.8 Surface Profiler 3D close view of DMTL NO 25.

Figure 4.9 shows the surface profiler snapshots and a microscope photograph of a fabricated OES embedded unit DMTL. The bridge has not been fabricated yet while capturing Figure 4.9 (a). Here, it can be observed that the notches can be built successfully at the end of the stubs. The measurement results of these structures can not be presented because the fabricated structures encounter a stiction problem.



(a) (b)



(c)

Figure 4.9 Surface Profiler snapshot of a fabricated OES embedded unit DMTL: (a) before the sputtering of second metal, (b) after the sputtering and patterning of second metal. (c) Microscope photograph of a fabricated OES embedded unit DMTL.

# CHAPTER V

# MEASUREMENT OF THE FABRICATION DMTL PHASE SHIFTERS

The S-parameters of the designed DMTL structures are measured in METU Microwave and Millimeter Wave Research Laboratory. The equipments used to take measurements can be listed as HP 8720D 0.05-20GHz vector analyzer, Keithly 2400 Sourcemeter, and Cascade ACP-GSG-150P probe station. Two different calibration techniques are used, namely, SOLT and TRL. To test the 48 DMTL structures which are designed to verify the validity of the proposed HICAPLO model, SOLT calibration is preferred; while to test the improved performance phase shifters and OES inserted phase shifters, TRL calibration is selected. The reason of these selections will be explained in Section 5.2.1. In this chapter, details of SOLT and TRL calibration, as well as the other measurement setups, will be presented in Section 5.1. The measurement results will be compared with the simulations and the models in Section 5.2.

## 5.1. MEASUREMENT METHODOLOGY

### 5.1.1. Measurement Setup

Figure 5.1 represents a simple diagram of the setup used in the measurement of the DMTL structures. The wafer with DMTL structures is placed on the probe station and the probes which have 220 μm separation between two ground tips are touched on both sides of the DMTL's. The probes are mounted on the probe station and connected to the network analyzer through Bias-Tee's. The Bias-Tee's are used to

mix the DC signal, which is supplied from Keithly Sourcemeter, and the RF signal then transfer them to the DMTL structures. For actuation, DC voltage is preferred and from the network analyzer, the S-parameter response is observed up to 20 GHz. The measurement results are saved in ASCII format in discs and they are converted into touchstone file format after they are transferred to computer.

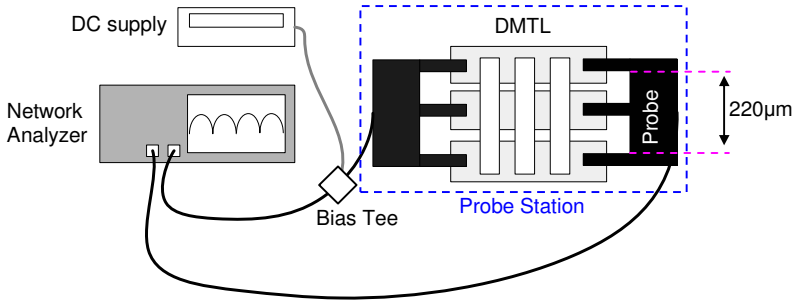



Figure 5.1 The measurement setup prepared for the DMTL structures.

Since the separation between the ground tips of the probes are limited to 220 µm, K=2G+W should be at most 220 µm for SOLT (short-open-line-through) calibrated measurements. On the other hand, for K≥ 220 µm type structures, TRL (through-reflect-line) calibration is used.

During measurement all the errors up to the probe tips, which result from both the coaxial cable and the probe losses must be removed. To remove these errors, different calibration techniques, which move the measurement reference planes to the end of the probe tips, are used. For the structures defined in this study, two calibration techniques, SOLT and TRL are used. For the structures DMTL NO 1-48, SOLT calibration is sufficient since their ground plane separations are limited to 220 µm. On the other hand, the optimized DMTL phase shifter and the OES inserted DMTL phase shifters have ground plane separations of 500 µm. Therefore, CPW lines which will satisfy a transmission between 500 µm and 220 µm should be connected at both sides of the DMTL lines. The effect of these transitions is present on the measured S-parameters. TRL calibration technique is used in these types of

structures in order to eliminate this effect from the measurements by de-embedding [52].

## 5.2. MEASUREMENT RESULTS

### 5.2.1. Measurement Results of the DMTL Structures Designed to Verify the Proposed HICAPLO Model

The 48 DMTL structures defined in CHAPTER III are fabricated following the process flow explained in CHAPTER IV. The sacrificial layer, therefore the height of the bridges are planned to be 2 µm. However, because of the compressive residual stress of the second metal and the annealing process which follows the release, the bridges are buckled after release; at the end, they appear with an average height more than 2 µm as opposed to what was planned. Table 5.1 shows the heights of the bridges for different DMTL structures which are located on different regions of the wafer before and after an annealing process. Since polyimide can not be deposited in a perfect uniformity, the structures appear to have different heights after release.

The heights presented in Table 5.1 are measured with the help of 3D scanning ability of the surface profiler without an actuation. Depending on the bridge and center conductor width the pull-down voltage varies as equation 2.18 assumes. On the other hand, experimental results show that an average value of 10 Volts can be taken as the pull-down voltage for the DMTL structures defined in Table 5.1. Moreover, it is assumed that the heights of the bridges just before they are actuated by 10 Volts should be $2h_{initial}/3$ as explained in CHAPTER II. However, as opposed to the theoretical knowledge, in practice the height change ratio is smaller, which can be limited to 20 % at most [27]. Therefore, making a decision about the height of a bridge at "just before collapse" state is not practically possible unless there is a measurement setup which is able to get the height data while the structure is being actuated.

Since there is an uncertainty about the actuated height of the bridge, an alternative way is considered to obtain two different bridge states, where the height is exactly known for each of these two states. After the initial heights of the bridges are measured, the wafer is exposed to annealing and as a result of the additional stress, the bridges bend. This bend causes an increase in the average heights of the bridges. Therefore, a new state is obtained with increased bridge heights. Of course, this method is not proposed for the practical usage of DMTL structures; but it is preferred where the heights of the bridges should be exactly known for the sake of accuracy in modeling studies. Table 5.1 also shows the bridge heights after annealing. It can be concluded that the increase in the height is about 25 %.

Both initial and final states of the measurements are compared with the HICAPLO model and the *CLR* model. Figure 5.2 presents the measurement, the *CLR* model and the proposed model results for DMTL structures NO 13-16 before annealing. In fact these structures are same with the ones compared in Figure 3.7 . An important point to mention about the results in Figure 5.2 is that, the insertion loss found by the *CLR* and the proposed HICAPLO model is multiplied by a factor of 0.83 before being converted to the dB scale. This sizing is necessary since the models and even the simulations can not predict the actual loss measured. Figure 5.3 also presents examples to the measurement results, where the insertion loss is again scaled. Figure 5.4 and Figure 5.5 give examples from the measurement of insertion phases for eight different structures.

It is observed that the measurement data fit the model results for different cases, where the periodicity, bridge and the center conductor widths are varied. Therefore, the proposed HICAPLO model is able to give the characteristic of a DMTL structure with bridge widths larger than 50 µm except for a scaling factor in the loss. The reason why the structures are terminated by different loads is to stay away from the matching impedance and to observe a clearer response.

Table 5.1. Before / after annealing bridge heights of the fabricated DMTL structures with bridge widths larger than 50 µm.

| **DMTL NO** | **G** (µm) | **W** (µm) | **w** (µm) | **P** (µm) | **$h_{final}$ after annealing** (µm) | **$h_{initial}$ before annealing** (µm) |
|---|---|---|---|---|---|---|
| **9** | 80 | 60 | 75 | 200 | 3.7 | 2.8 |
| **10** | 80 | 60 | 75 | 400 | 4.1 | 3.1 |
| **11** | 80 | 60 | 75 | 600 | 4.1 | 2.9 |
| **12** | 80 | 60 | 75 | 1000 | 4.1 | 3.1 |
| **13** | 80 | 60 | 100 | 200 | 3.6 | 2.8 |
| **14** | 80 | 60 | 100 | 400 | 3.7 | 2.6 |
| **15** | 80 | 60 | 100 | 600 | 3.6 | 2.4 |
| **16** | 80 | 60 | 100 | 1000 | 3.6 | 2.8 |
| **25** | 70 | 80 | 75 | 200 | 3.9 | 3.4 |
| **26** | 70 | 80 | 75 | 400 | 4.2 | 3.4 |
| **27** | 70 | 80 | 75 | 600 | 4.2 | 3.1 |
| **28** | 70 | 80 | 75 | 1000 | 3.8 | 3.3 |
| **29** | 70 | 80 | 100 | 200 | 3.4 | 3.4 |
| **30** | 70 | 80 | 100 | 400 | 3.8 | 3.0 |
| **31** | 70 | 80 | 100 | 600 | 3.9 | 3.0 |
| **32** | 70 | 80 | 100 | 1000 | 3.6 | 3.0 |
| **41** | 60 | 100 | 75 | 200 | 4.3 | 4.1 |
| **42** | 60 | 100 | 75 | 400 | 4.5 | 3.5 |
| **43** | 60 | 100 | 75 | 600 | 4.4 | 3.5 |
| **44** | 60 | 100 | 75 | 1000 | 4.4 | 3.8 |
| **45** | 60 | 100 | 100 | 200 | 3.6 | 3.5 |
| **46** | 60 | 100 | 100 | 400 | 4.0 | 3.2 |
| **47** | 60 | 100 | 100 | 600 | 3.9 | 3.0 |
| **48** | 60 | 100 | 100 | 1000 | 4.2 | 3.1 |

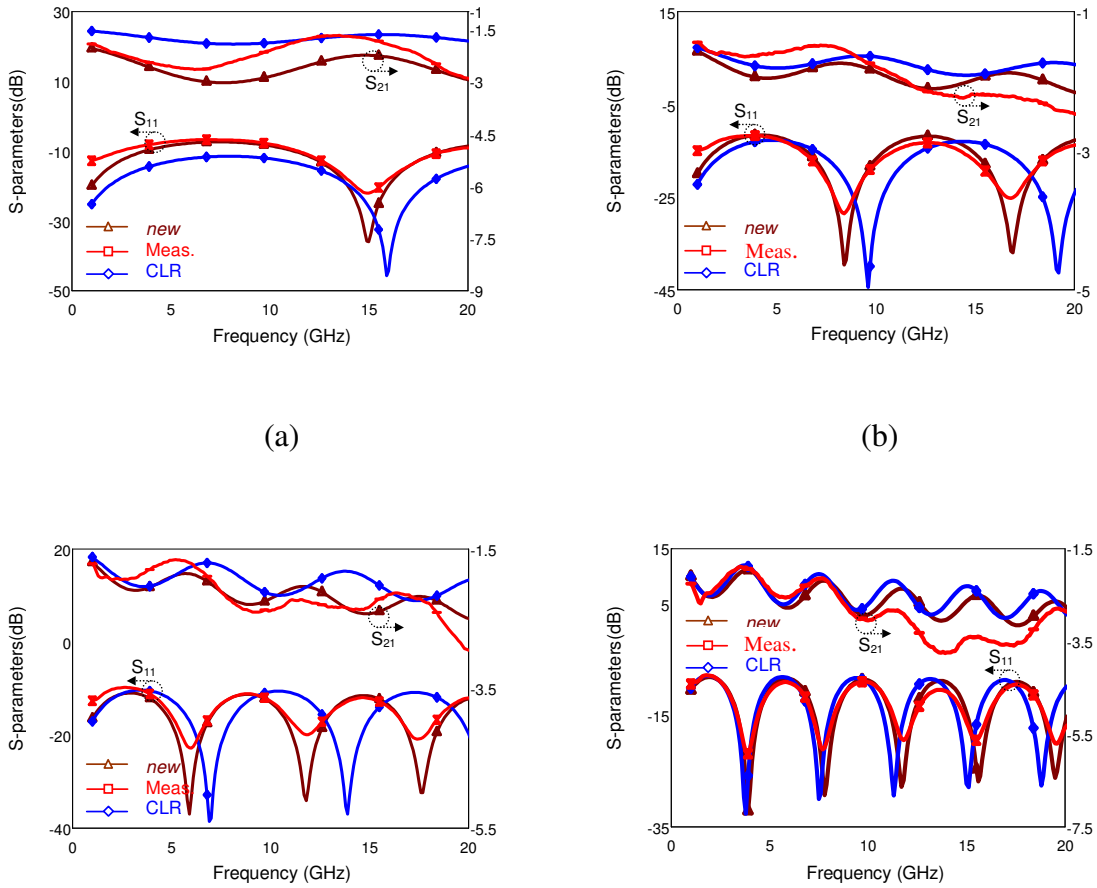



Figure 5.2 The measurement, *CLR* model and the new HICAPLO model results of (a) DMTL NO 13 terminated by 40 Ω, (b) DMTL NO 14 terminated by 50 Ω, (c) DMTL NO 15 terminated by 50 Ω, and (d) DMTL NO 16 terminated by 50 Ω.

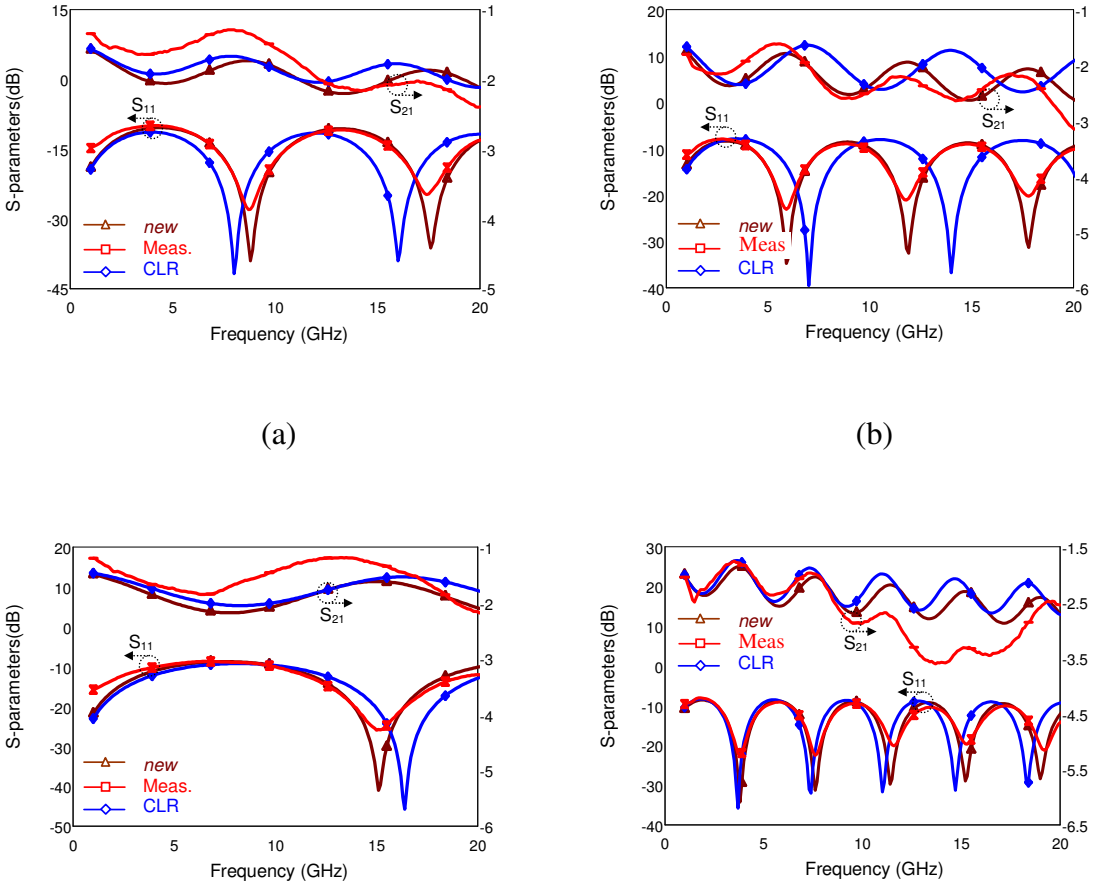
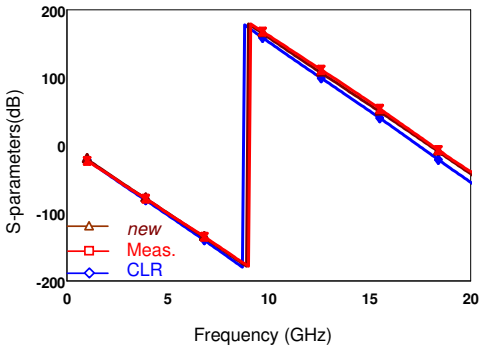
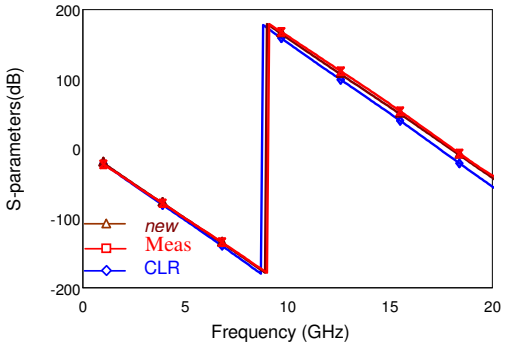


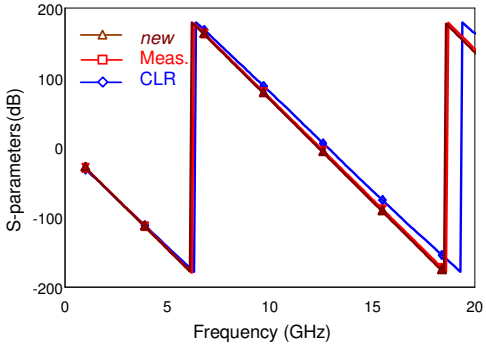

Figure 5.3 The measurement, *CLR* model and the new HICAPLO model results of (a) DMTL NO 10 terminated by 50 Ω, (b) DMTL NO 31 terminated by 40 Ω, (c) DMTL NO 41 terminated by 50 Ω, and (d) DMTL NO 48 terminated by 40 Ω.



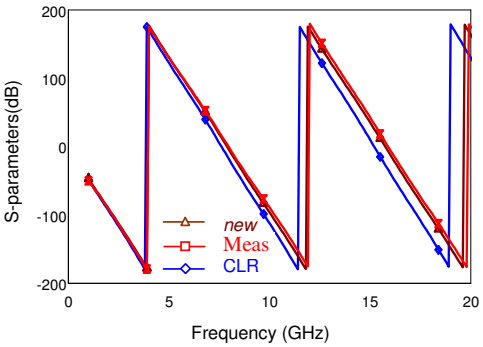

(a)




(b)




(c)




(d)

Figure 5.4 Measurement, *CLR* model and the new HICAPLO model $S_{21}$ phase results of (a) DMTL NO 25 terminated by 50 Ω, (b) DMTL NO 26 terminated by 50 Ω, (c) DMTL NO 27 terminated by 50 Ω, and (d) DMTL NO 32 terminated by 50 Ω.

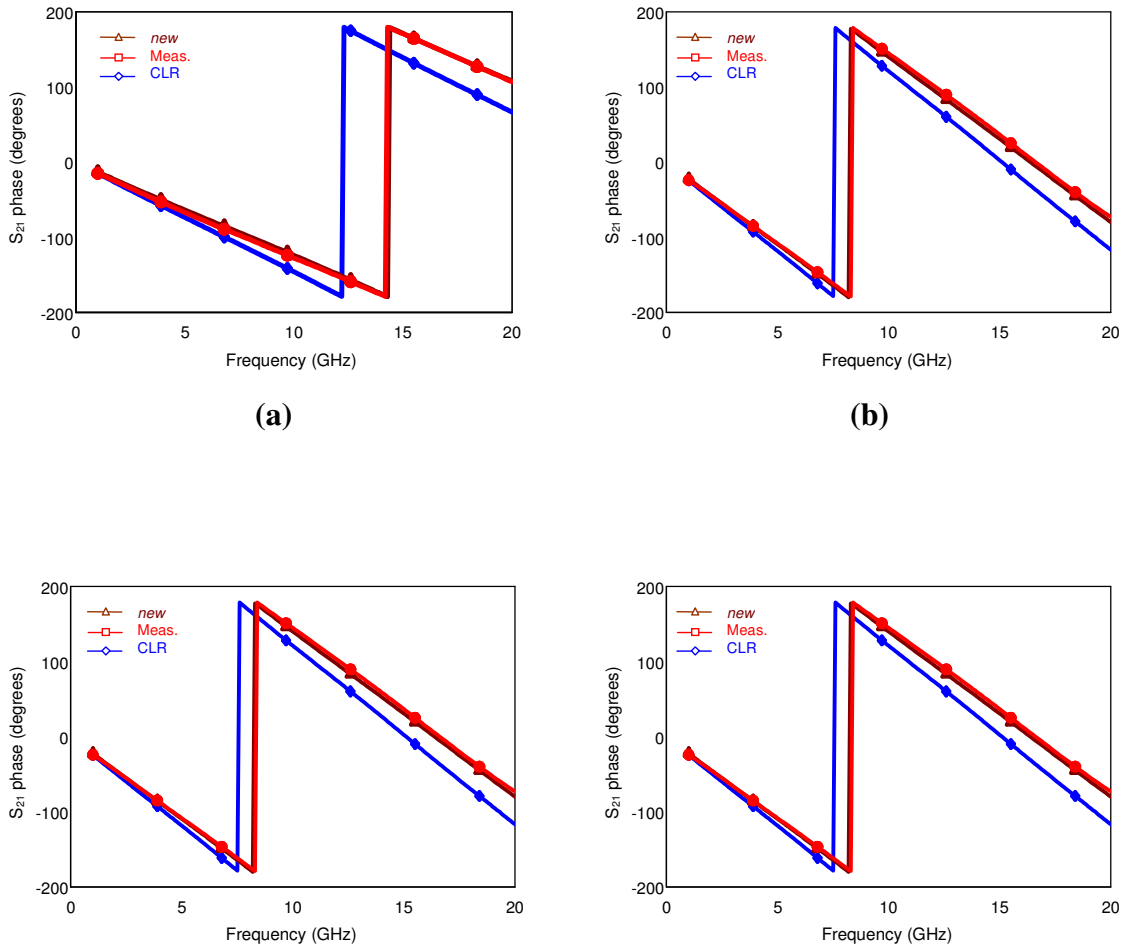
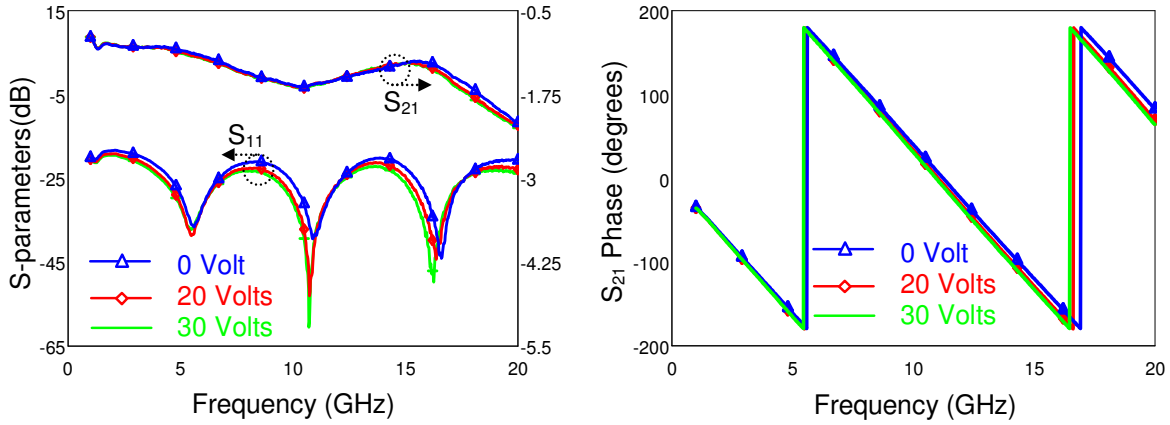



Figure 5.5 Measurement, *CLR* model and the proposed model $S_{21}$ phase results of (a) DMTL NO 45 terminated by 50 Ω, (b) DMTL NO 46 terminated by 50 Ω, (c) DMTL NO 12 terminated by 50 Ω, and (d) DMTL NO 29 terminated by 50 Ω.

Although it is not possible to measure the exact height of the actuated bridges, the HICAPLO model can be used to estimate this height. Figure 5.6 is a good example, where the proposed model is used to predict the height of the actuated bridge for

different voltages for DMTL NO 43. From the comparison of the model with the measurement results, the heights are found as: 2.22 µm for no actuation, 2.02 µm for 20 V actuation, and 1.95 µm for 30 V actuation. Notice that, no-actuation bridge height is different than what is denoted as up-state height in Table 5.1, because these measurements are taken from DMTL NO 43 structure from another wafer fabricated under different conditions.




**(a)** **(b)**

Figure 5.6 The measurement results of DMTL NO 43 structure for no actuation, 20 Volts, and 30 Volts actuation when terminated by 50 Ω.

An additional observation is made on two different unloaded CPW structures to see whether there is a need for a scaling factor in the insertion loss calculation. The K=W+2G value is selected as 220 µm for both structures, where first one has a center conductor width, W of 90 µm and the second one has a W of 110 µm. Figure 5.7 illustrates the situation for both of the structures. To fit the model results to the measured data, the insertion loss coming from the model is multiplied by a factor of 0.95 before being converted to the dB scale. Therefore, it can be concluded that, the models can not predict the measured insertion loss of both loaded and unloaded CPW structures, which may have been caused because of the fabrication materials.

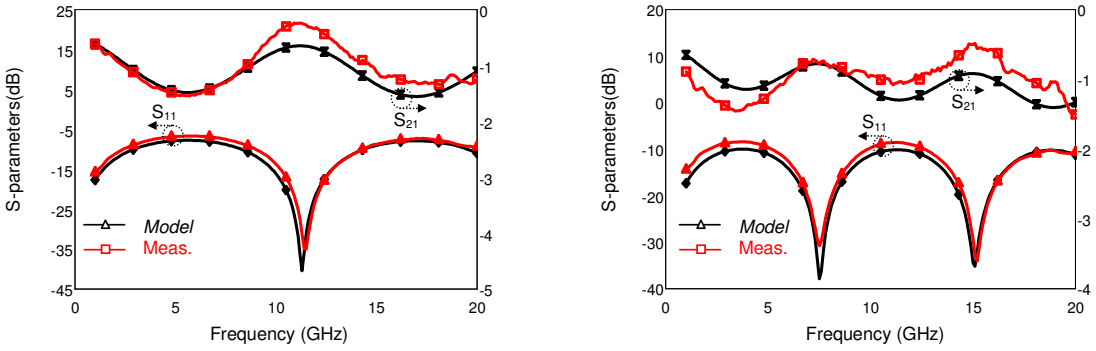



Figure 5.7 The measurement and the circuit model results of CPW transmission lines (a) for the structure with W= 90 µm (b) for the structure with W= 110 µm.

### 5.2.2. Measurement Results of the DMTL structures designed to verify the tecnique proposed to evaluate degree/dB performance

In CHAPTER III, a method was introduced to estimate the degree/dB performance of different types of DMTL phase shifters by using MATLAB. With the help of this method, the degree/dB performance of a DMTL phase shifter can be evaluated without a need for long duration simulations. The measurement results obtained for the DMTL structures defined in Table 5.1 can be used to verify this method. In Table 5.1, the center conductors vary between 60 µm and 100 µm, the bridge widths vary between 75 µm -100 µm, where periodicity is constant at 220 µm. Therefore, two-dimensional degree/dB plots similar to Figure Figure 3.16 can be drawn for K=220 µm by using MATLAB. Figure 5.8 illustrates these plots at @ 20 GHz, where $h_{up}$=4.1, and $h_{down}$=3.1 are selected as the up and down-state bridge heights. Four different figures are used to represent different periodicities and satisfy a comparison between DMTL NO 10-12-27-48 structures and the MATLAB results. While obtaining these plots, the scaling is again taken into consideration and the

insertion losses of the HICAPLO model are multiplied by 0.83 before they are converted into dB scale.

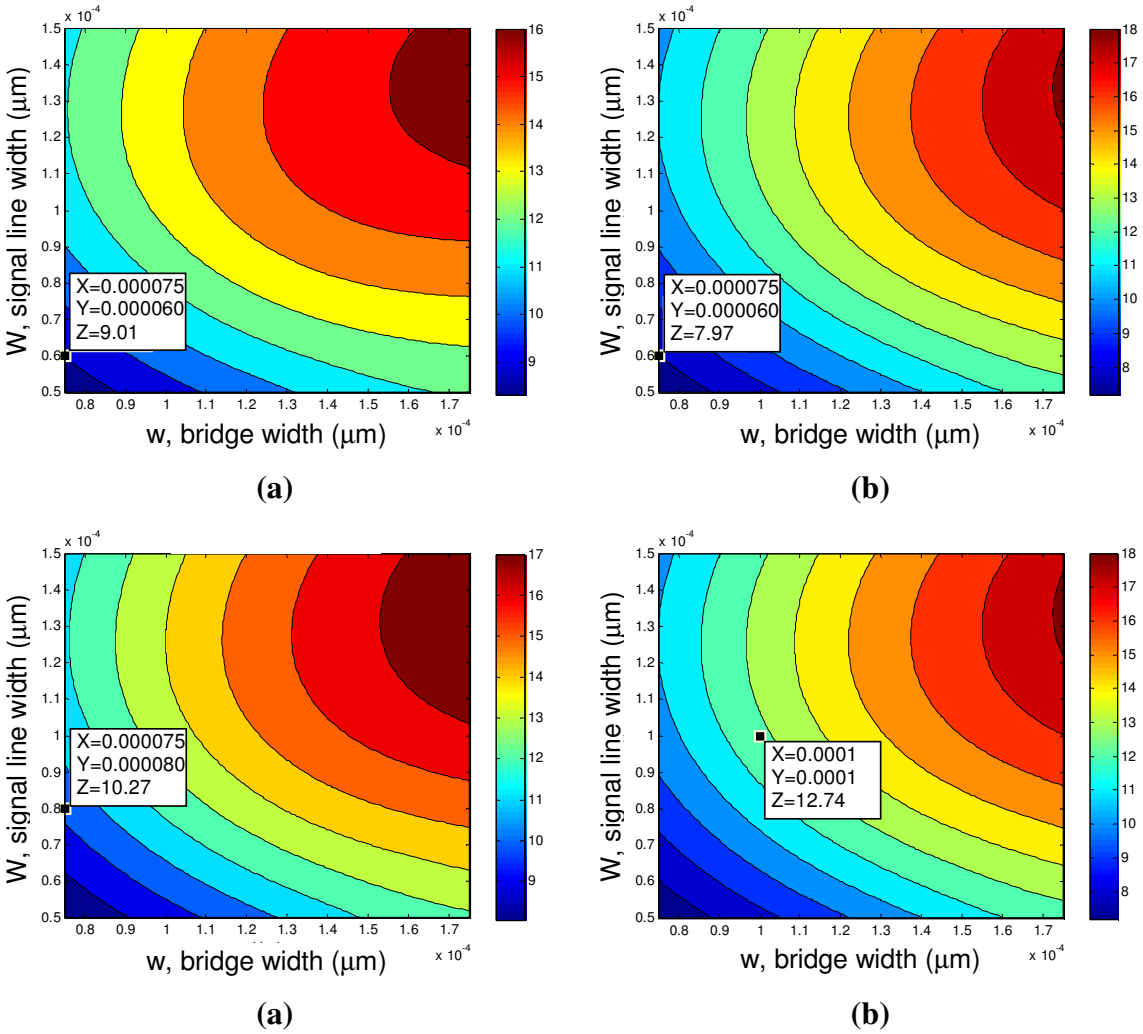



Figure 5.8 The degree/dB performance with respect to bridge width and center conductor width for (a) DMTL NO 10 with P= 400 µm. (b) DMTL NO 12 with P= 1000 µm. (c) DMTL NO 27 with P= 600 µm. (d) DMTL NO 41 with P= 1000 µm.

The measured phase shifts, the insertion losses, and the degree/dB performances are presented in Table 5.2 and Table 5.3. In these tables, beside the measurement results, the *CLR* and the proposed modeling results are also shown. The degree/dB performances of the proposed model, which are explicited in Table 5.4, are taken from the plots obtained by MATLAB and shown in Figure 5.8. From these tables, it can be concluded that the proposed model is able to approximate the phase shift of the DMTL phase shifters better than the *CLR* model is. Moreover, the MATLAB code works properly and gives close degree/dB performances to the measured ones, which means that the requirement of long duration simulations or calculations are eliminated.

Table 5.2. Measured, HICAPLO modeled and CLR modeled phase shifts of differend DMTL structures @ 20 GHz.

| **DMTL NO** | **state** | **Measured phase shift** (degrees) | **new model phase shift** (degrees) | ***CLR* model phase shift** (degrees) |
|---|---|---|---|---|
| **10** | up | -29.9 | -31.7 | -66.7 |
| | down | -45.7 | -49.1 | -89.7 |
| **12** | up | -154.2 | -164.1 | -175.1 |
| | down | -174.3 | -178.1 | -131.3 |
| **27** | up | -164.1 | -152.1 | -141.2 |
| | down | -143.6 | -128.8 | -115.1 |
| **48** | up | -171.1 | -171.2 | -137.2 |
| | down | -144.1 | -133.4 | -98.2 |

Table 5.3. Measured, HICAPLO modeled and CLR modeled insertion losses of different DMTL structures @ 20 GHz.

| **DMTL NO** | **state** | **Measured insertion loss** (dB) | **new model insertion loss** (dB) | ***CLR* model insertion loss** (dB) |
|---|---|---|---|---|
| **10** | up | -2.01 | -2.01 | -2.01 |
| | down | -2.00 | -2.01 | -2.01 |
| **12** | up | -2.67 | -2.65 | -2.65 |
| | down | -2.58 | -2.66 | -2.56 |
| **27** | up | -2.02 | -2.44 | -2.21 |
| | down | -2.13 | -2.17 | -2.06 |
| **48** | up | -2.41 | -2.51 | -2.34 |
| | down | -2.25 | -2.58 | -2.34 |

Table 5.4. Measured, HICAPLO modeled and CLR modeled degree/dB performances of different DMTL structures @ 20 GHz.

| **DMTL NO** | **Measured Degree/dB** | **new model Degree/dB** | ***CLR* model Degree/dB** |
|---|---|---|---|
| **10** | -7.90 | -9.01 | -11.46 |
| **12** | -7.73 | -7.97 | -16.80 |
| **27** | -9.88 | -10.27 | -12.15 |
| **48** | -11.61 | -12.74 | -16.69 |

# CHAPTER VI

# CONCLUSIONS AND FUTURE WORKS

This thesis work involves the design, fabrication and measurement of distributed MEMS transmission line (DMTL) structures. The main objective of this study is to develop an improved model which can be used for DMTL structures having bridge widths larger than 50 μm. Beside this main study, there are two concurrent tasks. The first task is to develop a degree/dB evaluation method which will eliminate the need for simulation or measurement results. The second one is to integrate open-ended stub transmission lines into DMTL structures to obtain better degree/dB performance. The designs are based on Ansoft HFSS v9.2 simulation results. For the fabrication, METU microelectronics facility is used. According to the literature search, design, fabrication and measurement results, the following conclusions are drawn:

1. DMTL structures find application area in several RF designs including antennas, phased array systems and matchers. Therefore, the study of DMTL's plays an important role in the analysis of these structures. Up to date mainly two different methods of modeling DMTL structures are proposed, namely the *CLR* model [45] and [29]. The CLR model is discussed to be non-valid for DMTL's with bridge widths larger than 50 μm. On the other hand the proposed model in [29] includes many parameters, which can not be analytically estimated.

2. The proposed HICAPLO model in this thesis improves the *CLR* model by adding a low impedance transmission line surrounded by two shunt parallel plate capacitances in the middle of the DMTL unit cell. By this way, the region which could not be modeled by the CLR is turned into a low impedance line and the remaining region (which is at most 50 μm) is modeled by a shunt capacitance. The low impedance line formulated part is a CPW line which is covered by a bridge, which can be counted as a top cover. To estimate the low impedance line parameters, CPW with top cover formulations are used, where the calculations are based on micro strip line approximations.

3. The low impedance line parameters are taken as the line impedance and the line loss. The low-impedance line impedance is directly evaluated form the micro-strip formulations, where during the analysis of the sample structures 100 dB/m is taken as an average constant line loss. However, for more specific applications which consider the loss performance of a DMTL, the low-impedance line loss should be clearly defined. In order to achieve this, an optimization is applied which fits polynomials to the loss values obtained after simulations. Thus, an analytical approximation is formed which can be used to evaluate the low-impedance line loss.

4. As a summary, the DMTL unit sections are modeled with two high-impedance transmission lines, two shunt capacitances standing for the parallel plate capacitance of 50 μm bridged line, and a low-impedance line lying between the shunt capacitances which represents the CPW line with top cover (bridge). This new modeling approach and the *CLR* model are compared with the simulation and measurement results and the new model is validated to fit the results better than the *CLR* model.

5. The ABCD parameters of the HICAPLO model is extracted from the circuit analysis and converted into S-parameters. Loss and the phase shift of the DMTL structures are expressed in terms of the S-parameters. The degree/dB performance is evaluated from a MATLAB code by using these parameters. Degree/dB plots with respect to bridge widths and signal line widths are obtained and the optimum DMTL phase shifters are determined.

6. Open-ended stubs (OES) are planned to be placed through the signal line of a DMTL structure in order to increase the maximum amount of phase shift for a defined bridge height ratio and loss.

   First, the effect of OES insertion in CPW structures is investigated. As a result of the simulations, it is observed that the effect of this structure as a discontinuity element can be modeled as a series capacitance. This capacitive effect is determined to be increased by increasing the length and the characteristic impedance of the stub.

   Next, these discontinuity elements are embedded in unit DMTL cells. A gap is formed between one end of the stub and the center conductor of the DMTL structure, where the other end of the stub is connected to the bridge with the help of a notch. Therefore, this time it is ensured that the open-end stub behaves as a shunt capacitance. The shunt capacitive effect of this configuration is validated by simulation results and a model which defines this configuration is created.

   The main issue is to increase the difference between up and down state capacitances. Therefore, the down state position of the bridge should bring more capacitive effect. Since more shunt capacitance is guaranteed when the bridge touches the open-end stub, this case can be counted as the down state position. For this case, the shunt capacitance is composed of both the parallel

plate capacitance and the open-end stub capacitance. On the other hand, in the up state position it should be satisfied that the only effective capacitive is the parallel plate capacitance. This condition is satisfied by separating the bridges from the notches in the up state position; therefore cutting the connection between the open-end stub and the bridge. As a result, there appears a capacitive difference between the up and down states, which comes from mainly the open-end stub capacitance. The increased difference in the capacitance brings an increase in the phase shift amount. This method is applied on various DMTL phase shifters and the obtained simulation results are strongly supporting the main idea.

The final remark of OES stub inserted DMTL structures is that, they satisfy a continuous phase shift until they touch the notches, where they satisfy a discrete increase in the phase shift value when they touch them.

7. The designed DMTL phase shifters are fabricated in METU micro electronics facilities. The process was based on sputtered gold base and structural layers on glass wafers; where sputtered titanium was used to satisfy adhesion between gold and glass. The parts of the CPW lines, which were not under the bridges, were thickened by gold electroplating to reduce the conductor losses. PECVD silicon nitride was used as dielectric layer, which would protect the bridges from electrostatic stiction to center conductor when actuated. Polyimide was used as the sacrificial layer. The photo sensitivity of the polyimide was selected as positive, which means that the parts exposed to UV light will dissolve in the developer. SVC was used to remove the polyimide from the wafer and critical point drying technique was used for release.

8. After release, the bridges were observed to buckle as a result of intrinsic compressive stress. To reduce this stress, different second metal sputtering

recipes were applied, which varied the temperature and the pressure of the chamber.

9. The measurements of the 48 DMTL structures, which would validate the proposed model and the degree/dB evaluation method, were realized at METU Microwave and Millimeter Wave Research Laboratory. Mainly two conclusions were highlighted when the measurement results are compared with the simulations and the model:
    a. The model results fitted the measurements except the need for a scaling factor in the insertion loss. The inefficient evaluation of the model for the insertion loss resulted from the fact that the model was set on the HFSS simulation results. Since HFSS underestimates the CPW transmission line losses, the model gave smaller insertion losses in dB scale when compared with the measurements. To overcome this problem, the insertion loss of the model was scaled by 0.83 before it was converted into dB scale.
    b. When the same correction factor is inserted in the MATLAB code, the degree/dB performance evaluations gave close results with the measurements.

The conclusions reached in this thesis study lead discussions and future works, which are related to both design and fabrication processes. These discussions and possible future studies can be listed as follows:

1. The OES inserted DMTL structures can be fabricated and the results can be compared with the simulation results in order to verify the improvement in degree/dB performance. Beside the DMTL phase shifter application, the series capacitive effect of OES or shunt capacitive effect of OES-air bridge connection can used when more reactive effect is needed in an RF circuit.

2. Beside the open-end stubs, other discontinuity elements, such as short-end stubs, t-junctions, air bridges may be considered as CPW reactance elements. Moreover, they can be integrated in other RF circuits such as DMTL phase shifters or matching networks.

3. The proposed HICAPLO model for DMTL structures can be improved in order to span for all bridge widths.

4. During fabrication, some steps may be reconsidered in order to obtain more uniform structures and to make the process steps easier. To speak on a specific example, the positive polyimide as sacrificial layer may be changed to negative polyimide, or electroplated copper. These alternative sacrificial layers were processed at METU MET previously and they became out of favor when positive polyimide was appeared on the scene. However, the difficulties arise during the cure process of positive polyimide and the troubles show during the release step reveals the requirement of reconsideration of the previous materials.

   Beside the sacrificial layer, the second metal deposition technique or medium properties may be arranged in order to have more uniform bridge structures and overcome the stress problems.

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# APPENDIX

## DETAILED PROCESS FLOW

*1st metal Sputtering*

- ⇨ DC sputter from Ti target, argon environment, 300 W, 383V DC bias, 120 $^{o}$C, $2.3\times10^{-3}$ mBar, 80 seconds up to an end point thickness of 110 A$^{o}$.
- ⇨ DC sputter from Au target, argon environment, 300 W, 440V DC bias, 120 $^{o}$C, $13\times10^{-3}$ mBar, 190 seconds up to an end point thickness of 820 A$^{o}$.

*Electroplating*

- ⇨ Spin adhesion promoter AP 140 at 2000 rpm, soft bake 1:30 minutes on 115°C hotplate.
- ⇨ Spin photo resist SPR 220 at 2000 rpm, soft bake 1:30 minutes on 115°C hotplate.
- ⇨ Align Mask and expose at 18 mW/cm$^2$ for 7 seconds.
- ⇨ Relax the PR coated wafer for 30 minutes in humidity environment.
- ⇨ Develop in MF24A for 70 seconds.
- ⇨ Rinse in deionized water for 2 minutes twice.
- ⇨ Edge bead remove using acetone.
- ⇨ Hard bake 115 minutes in 20°C oven.
- ⇨ Rest in oxygen plasma at 280 W for 2 minutes.
- ⇨ Electroplate gold at 62 mA for 20 minutes.

*Metal Ething*

- ⇨ Spin primer at 3750 rpm.
- ⇨ Spin photo resist S1828 at 3750 rpm, soft bake 1:30 minutes on 115°C hotplate.
- ⇨ Align Mask and expose at 18 $mW/cm^2$ for 8 seconds.
- ⇨ Develop in MF26A for 105 seconds.
- ⇨ Rinse in deionized water for 2 minutes tweice.
- ⇨ Hard bake 120 minutes in 20°C oven.
- ⇨ Rest in oxygen plasma at 280 W for 2 minutes.
- ⇨ Au etch in Transene Au etchant for 1:40 minutes.
- ⇨ Ti etch in HF: $H_2O_2$: DI (1:1:640) for 1:55 minutes.
- ⇨ PR strip using acetone and isopropyl alcohol

*Back Side metallization*

- ⇨ DC sputter from Ti target, argon environment, 300 W, 383 V DC bias, Room Temperature, $2.3\times10^{-3}$ mBar, 80 seconds up to an end point thickness of 110 $A^o$.
- ⇨ DC sputter from Au target, argon environment, 300 W, 383 V DC bias, Room Temperature, $5\times10^{-3}$ mBar, 550 seconds up to an end point thickness of 2500 $A^o$.
- ⇨ DC sputter from Ti target, argon environment, 300 W, 383 V DC bias, Room Temperature, $2.3\times10^{-3}$ mBar, 80 seconds up to an end point thickness of 200 $A^o$.

*Silicon Nitride Deposition and patterning*

- ⇨ Deposit $Si_xN_y$ using PECVD, 900 mTorr at 130 A/minute for 23 minutes
- ⇨ Spin adhesion promoter S1828 PR at 3750 rpm, soft bake 1:30 minutes on 115°C hotplate.
- ⇨ Align Mask and expose at 18 $mW/cm^2$ for 8 seconds.
- ⇨ Relax the PR coated wafer for 30 minutes in humidity environment.
- ⇨ Develop in MF26A for 60 seconds.
- ⇨ Rinse in deionized water for 2 minutes twice.
- ⇨ Hard bake 120 minutes in 20°C oven.
- ⇨ Rest in oxygen plasma at 300 W for 2:30 minutes
- ⇨ RIE etch in 60 sccm $CF_4$, 22 sccm $CHF_3$, 10 sccm $O_2$ at 70mTorr at 250 mW for
- ⇨ PR strip first using Acetone + isopropyl alcohol, then SVC-175 at 80 C° for 5 minutes.

*PI 2737 sacrificial layer lithography @ 150℃*

*2nd Metal Sputtering*

- ⇨ DC sputter from Au target, argon environment, 214 W, 383 V DC bias, at room temperature, $10\times10^{-3}$ mBar, 550 seconds up to an end point thickness of 4000 $A^o$.